A New On-Chip ESD Protection Circuit with Dual Parasitic SCR Structures for CMOS VLSI

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***Abstract*—A new CMOS on-chip electrostatic discharge (ESD) protection circuit which consists of dual parasitic SCR structures is proposed and investigated. Experimental results show that with a small layout area of 8800 μm^2, the protection circuit can successfully perform negative and positive ESD protection with failure thresholds greater than ± 1 and ± 10 kV in machine-mode (MM) and human-body-mode (HBM) testing, respectively. The low ESD trigger voltages in both SCR's can be readily achieved through proper circuit design and without involving device or junction breakdown. The input capacitance of the proposed protection circuit is very low and no diffusion resistor between I/O pad and internal circuits is required, so it is suitable for high-speed applications. Moreover, this ESD protection circuit is fully process compatible with CMOS technologies.**

I. Introduction

IT IS KNOWN that an on-chip electrostatic discharge (ESD) protection circuit is essential in CMOS chips. Generally, high failure threshold, small layout size, and low *RC* delay are required in the ESD protection circuits for high-density high-speed applications. In future CMOS scaled-down technologies, which may use silicides, lightly doped drain (LDD) structures, etc., the design of efficient ESD protection circuits that meet the above requirements becomes a challenging task.

To design efficient CMOS ESD protection circuits, the use of resistors and diodes in some early designs has been gradually changed to the use of three-layer devices, such as field-oxide MOSFET's, gate-oxide MOSFET's, and parasitic n-p-n or p-n-p bipolar junction transistors (BJT's) in CMOS technologies [1], [2]. Pelella and Domingos [2] have even predicted that the parasitic four-layer p-n-p-n device, called the SCR, in CMOS technologies could be extremely effective in protecting a chip against the damage caused by ESD transients if proper design and optimization could be done. ESD protection using SCR's in bipolar technologies has been reported by Avery [3].

Recently, the parasitic lateral SCR device has been used in CMOS on-chip ESD protection circuits [4]–[9], [14]. Due to its high current sinking/sourcing capability, very low turn-on impedance, low power dissipation, and large physical volume for heat dissipating, the parasitic lateral SCR device has been recognized as one of the most effective elements in CMOS on-chip ESD protection circuits. In using the parasitic SCR device in ESD protection, however, there exists a major disadvantage that the SCR device has a high trigger voltage. To perform the protection, the trigger voltage of an ESD protection circuit must be less than the voltage which could damage the input buffer or output driver. The typical trigger voltage of a parasitic lateral SCR device in the ESD protection circuits fabricated by the advanced 1-μm CMOS process with LDD and silicided diffusion is about 50 V if the space of its anode to cathode is 6 μm [4]–[6]. With such a high trigger voltage, the lateral SCR device cannot be used alone as the only protection element. Thus, a field-planted diode (FPD) and a diffusion resistor, called the "secondary protection" elements, have to be incorporated with the lateral SCR device in the protection circuit to provide the overall protection [5], [6].

To avoid the using of extra "secondary protection" elements, some efforts have been made to reduce the trigger voltage of the parasitic lateral SCR device [7]–[9], [14]. One method is to integrate a low-breakdown-voltage short-channel NMOSFET within the lateral SCR device to form a "LVTSCR" structure which has a good tunable trigger voltage in the range of 10 to 15 V [8], [9]. But it may not be generally feasible to combine the NMOSFET and the lateral SCR device in this manner [9]. The other method is to add a "NLCS" mask to make a recessed field implant in the lateral SCR device in order to lower its trigger voltage [7]. The experimental results have shown that the minimum breakdown voltage of such a SCR defined and measured at the initial current flow of 1 μA is lowered to 9 V and its corresponding trigger voltage to initiate the latching state is about 20 V. But this approach needs an extra mask and process step [7].

Since the current flow in an SCR device is always from its anode to its cathode, an SCR device can be used for the single-polarity ESD input only. In the previously proposed works [4]–[9], only a lateral SCR device is used in the ESD protection circuit between the I/O pads and power supply V_{ss} (or ground) node. When the ESD pulse has a positive voltage with respect to the V_{ss} node, the lateral SCR device will be triggered into its low-impedance on state to bypass the ESD energy through the SCR device

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to V_{ss}. But it cannot be triggered on if the ESD pulse has a negative voltage with respect to the V_{ss} node. For negative ESD protection, therefore, the parasitic junction diode formed by p-substrate and n-well in the structure of the lateral SCR device or the separated punchthrough device should be used [4]–[9]. This degrades the protection capability and other performance of the overall ESD protection circuits.

In this paper, a novel double-polarity ESD protection circuit using dual lateral SCR structures with a low trigger voltage is proposed [14]. In this protection circuit, a lateral SCR structure is arranged to discharge the positive ESD pulses whereas the other one is arranged for the negative ESD pulses. Based upon the understanding of CMOS transient latch-up [10]–[13], the low trigger voltage can be achieved through the proper design of device capacitances within the lateral SCR structure. Thus, no device or junction breakdown is involved and the performance degradations due to device breakdown after numerous ESD transients can be avoided. Moreover, no extra process steps or modifications to the conventional CMOS IC technology are needed. This new ESD protection circuit has been designed, fabricated, and tested. The experimental results show that it can perform very effective ESD protection with a small layout area. Besides, it has a low input capacitance and a very low turn-on resistance.

II. Protection Circuit

A. Circuit Configuration

The lumped equivalent circuit of the new double-polarity ESD protection circuit with dual lateral SCR structures is shown in Fig. 1(a) and its cross-sectional view is given in Fig. 1(b) where the n-substrate p-well CMOS process is used. In the p-well process, the n-substrate is biased at V_{DD} in normal operation. So the V_{DD} node is the common node in this ESD protection circuit. The circuit in Fig. 1 consists of a parasitic lateral p-n-p transistor $Q1(Q3)$ and a parasitic vertical n-p-n transistor $Q2(Q4)$ to form the upper (lower) lateral SCR structure against negative (positive) ESD pulses. The parasitic lateral p-n-p transistor $Q1(Q3)$ is formed by p-well as its emitter, n-substrate as its base, and p-well as its collector. The smaller distance between p-well emitter and p-well collector leads to a larger beta gain of $Q1(Q3)$. Thus, a beta gain greater than one can be achieved through layout design. The parasitic vertical n-p-n transistor $Q2(Q4)$ is composed of n^+ diffusion in p-well as its emitter, p-well as its base, and n-substrate as its collector. Although the beta gain of such a vertical n-p-n transistor is dependent upon the process, the typical maximum forward beta gain usually can be as high as 100.

To further enhance the turn-on speed of the upper (lower) lateral SCR during negative (positive) ESD transitions, a parasitic field-oxide NMOS (PMOS) $M_n(M_p)$ is used. The field-oxide NMOS is formed by the n-substrate/p-well/n^+ diffusion structure whereas the field-oxide PMOS is formed by the p-well/n-substrate/p-well structure. The threshold voltage of such a parasitic field-oxide NMOS (PMOS) is dependent upon certain process parameters like field-oxide thickness and doping concentration under field oxide. The typical value is around 30 ~ 50 V. This parasitic field-oxide NMOS (PMOS) can decrease the dc trigger voltage of the upper (lower) lateral SCR structure. The dc trigger voltage can also be adjusted by changing the space between anode and cathode of the lateral SCR structure. Generally, a smaller anode-to-cathode space leads to a lower dc trigger voltage. But this space is always limited by process technologies.

The layout of an ESD protection circuit can also improve its ESD robustness. The demonstrated example of layout arrangement in Fig. 1(b) of the ESD protection circuit provides two identical lower lateral SCR paths from the central V_{in} node to its adjacent right and left V_{DD} nodes for positive ESD protection. Similarly, it also has two identical upper lateral SCR paths from the adjacent right and left V_{DD} nodes to the central V_{in} node for negative ESD protection. This increases the capability of current sourcing/sinking and heat dissipation.

All the ESD protection circuits presented in this section are based upon the p-well CMOS process. But the principles are equally applicable and realizable in an n-well process if the realization of the parasitic SCR devices is modified accordingly. Thus, the fabrication process of this proposed protection circuit is fully compatible with that of both p-well and n-well CMOS IC's.

B. Circuit Operations and Design Concepts

When a negative ESD pulse voltage greater than a certain threshold occurs at the I/O pad, the upper SCR structure in Fig. 1(a) is quickly triggered on by the transient currents generated by the well–substrate junction capacitances C_{c1} and C_{c2} in the transistors $Q1$ and $Q2$, respectively. The field-oxide NMOS with its gate connected to V_{DD}(common) also provides a trigger current to the base of the transistor $Q1$. This extra current makes the lateral SCR enter more quickly into its on state. After being turned on, a low-impedance path through the p-n-p-n structure is formed between the V_{DD} and V_{in} nodes and then the negative ESD pulse is quickly bypassed without damaging the internal circuits. Because the ESD pulse is of the transient type, the turn-on behavior of the SCR devices is related to the ac trigger voltage rather than the dc one. The ac trigger voltage can be adjusted through the design of the ratio between $C_{e1}(C_{e2})$ and $C_{c1} + C_{c2}$. The larger the value of $C_{c1} + C_{c2}$ with respect to C_{e1} and C_{e2}, the greater the transient voltages drop on C_{e1} and C_{e2} to forward bias the base–emitter junctions of the transistors $Q1$ and $Q2$ during the occurrence of negative ESD pulses [10]. This leads to a low ac trigger voltage, which could be much lower than the dc trigger voltage. Such a low ac trigger voltage can be achieved without using any device and junction breakdown. After the negative ESD pulse, $Q1$ and $Q2$ have to turn off. This can be achieved by designing a smaller p-well resistance R_w, a smaller

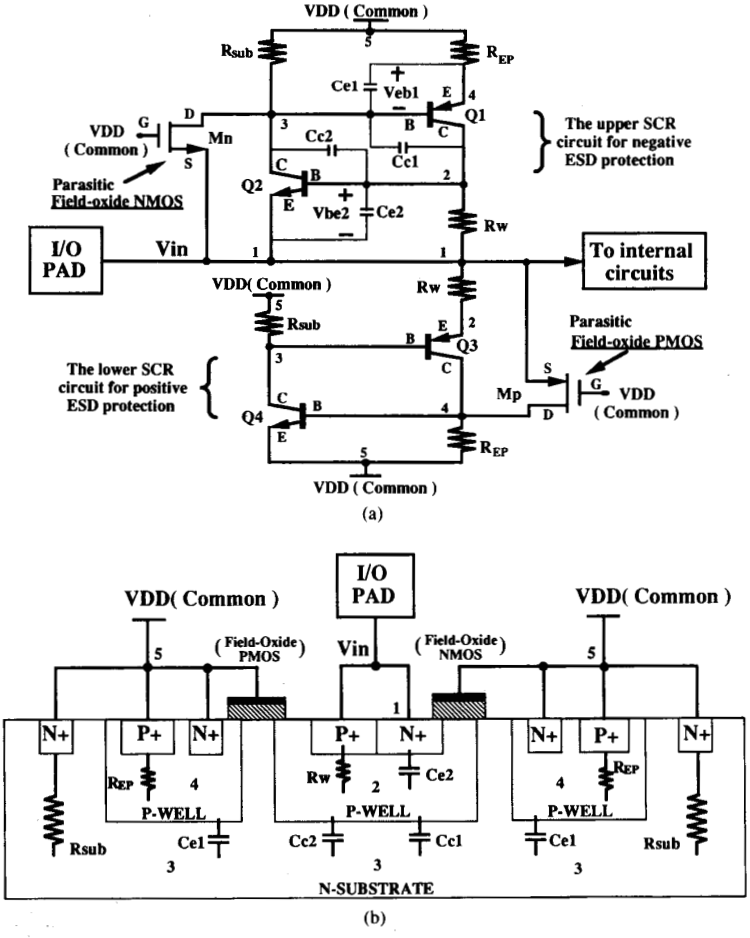

Fig. 1. (a) The ESD protection circuit with dual SCR structures for positive and negative ESD pulses. (b) The cross-sectional view of the ESD protection circuit shown in (a).

n-substrate resistance R_{sub}, and a larger p-well resistance R_{EP}. Theoretical models have been developed to design the above mentioned capacitances and resistances [13].

When a positive ESD pulse occurs at the I/O pad, V_{in} becomes greater than V_{DD}(common) + 0.6 V and the transistor $Q3$ quickly turns on because its base is the n-substrate biased at V_{DD}(common). Then the collector current of $Q3$ flowing into the p-well causes a voltage drop on R_{EP} and the base–emitter junction of the transistor $Q4$ becomes forward biased to turn on this SCR structure. The parasitic field-oxide PMOS can enhance the turn-on speed of the lower SCR. As soon as the lower SCR is triggered on, the positive ESD energy is quickly discharged through the low-impedance path. After the positive ESD pulse, both transistors $Q3$ and $Q4$ turn off. The turn-on speed of the lower SCR can also be enhanced through the increase of the beta-gain product of the transistors $Q3$ and $Q4$ and the resistance R_{EP}.

The layout of the proposed protection circuit can be produced as shown in Fig. 1(b) to meet the above requirements on device resistances and capacitances. Such a proper design can improve the ESD robustness. Moreover, the trigger voltage can be decreased to enhance the turn-on speed.

C. Circuit Simulation

SPICE simulations have been done to verify the validity of design concepts and operational principles of the proposed ESD protection circuit. Fig. 2 shows the SPICE simulation results of the suitably designed upper SCR circuit for negative ESD protection. It is shown that a negative 5-V pulse is enough to turn on the SCR. Thus, the low triggering voltage can be achieved through appropriate circuit design without involving device or junction breakdown. After the negative pulse, the SCR turns off quickly because the base–emitter voltages of transistors $Q1$ and $Q2$ quickly drop to zero as shown in Fig. 2. Fig. 3(a) and (b) shows the SPICE simulation results of both SCR circuits under positive and negative human-body-mode (HBM) ESD pulses with ESD voltages of +1000 and −1000 V, respectively. The curves show that the ESD energy can be quickly bypassed through the SCR circuits

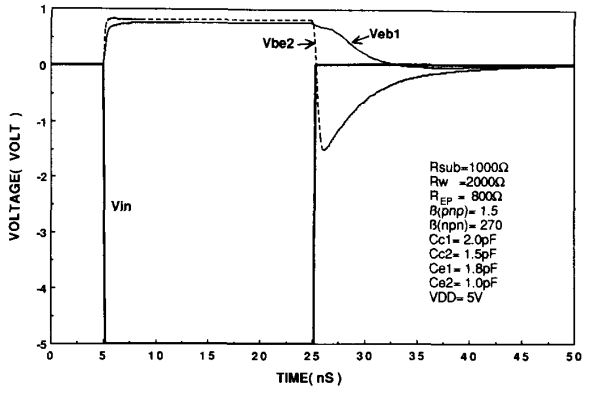

Fig. 2. SPICE simulation results of the upper SCR circuit in Fig. 1(a) under a negative 5-V transition.

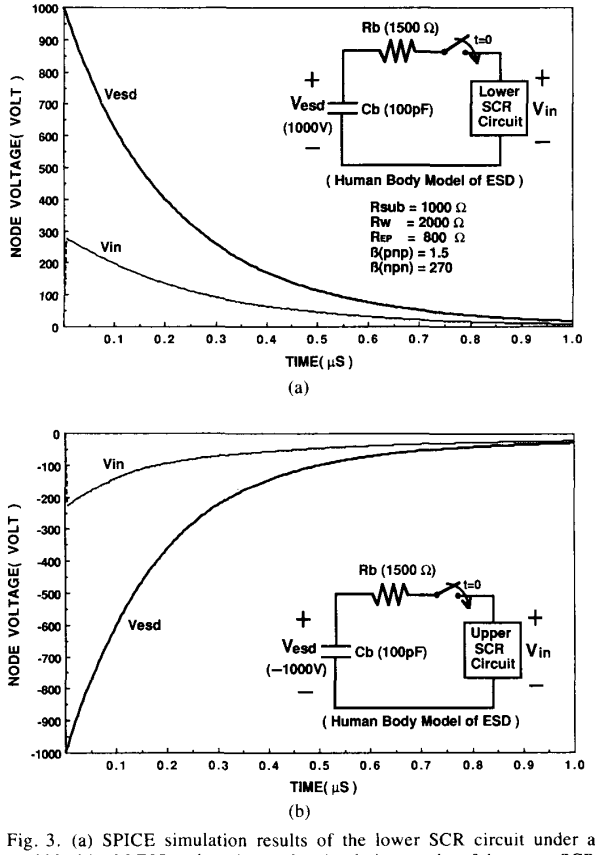

Fig. 3. (a) SPICE simulation results of the lower SCR circuit under a +1000-V HBM ESD pulse. (b) SPICE simulation results of the upper SCR circuit under a −1000-V HBM ESD pulse.

around I/O pads and the internal circuits of the chip can be protected.

III. Experimental Results

One set of such new dual-SCR ESD protection circuits with different layout dimensions has been implemented by using the 1.0-μm retrograde p-well bulk CMOS process.

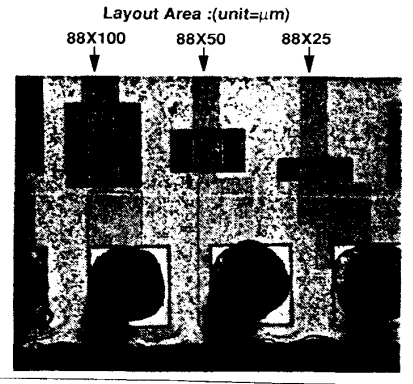

Fig. 4. Chip photomicrograph of the proposed ESD protection circuits.

The chip photomicrograph of some fabricated ESD protection circuits with different layout dimensions is shown in Fig. 4. The testing results of ESD failure thresholds for the protection circuits with different layout dimensions are listed in Table I. The results definitely show that failure thresholds can be greater than ± 1 and ± 10 kV in machine-mode (MM) and human-body-mode (HBM) testing, respectively, for the new ESD protection circuit with a layout area as small as 8800 μm^2. This successfully verifies the ESD protection capability of the proposed circuit.

The measured dc I–V characteristic of the dual SCR structures in the fabricated protection circuit is shown in Fig. 5, where the dc trigger voltage of the upper SCR is about 28 V and the holding voltage (current) is about 1.5 V (2.4 mA) with a turn-on resistance of 6 Ω. The measured maximum forward beta gains of the parasitic vertical n-p-n transistor and the lateral p-n-p transistor are about 92 and 1.53, respectively. Because the product of these two beta gains is much greater than one, the turn-on speed of parasitic lateral SCR structures is very quick.

In order to find the ESD trigger voltage of the fabricated protection circuit, a test structure to measure the ac trigger voltage as the ESD trigger voltage of the upper SCR is illustrated in Fig. 6. The V_{DD} node is connected in series with the resistor $R = 1$ kΩ, which is biased at 5 V, and the output of the pulse generator is connected to the I/O pad. The applied voltage pulses generated from the pulse generator have a fixed maximum voltage of +5 V and a tunable negative voltage level. If the upper SCR is triggered on by the negative pulse, the voltage observed at CH2 will be near the low voltage level of the negative pulse due to the low holding voltage of the SCR. Otherwise, it will remain at 5 V. When ± 5-V square pulses are applied to the upper SCR in the DUT block, it is still off so that the voltage waveform at the oscilloscope channel CH2 remains unchanged at +5 V as shown in Fig. 7(a). This guarantees that the upper SCR is never triggered on by the normal chip input signals as the lower SCR is. When the negative level of the applied voltage square pulse decreases to −16 V, the upper SCR of the fabricated protection circuit is triggered on and the voltage at the common node (CH2) decreases from +5 to −14.5 V

TABLE I
LAYOUT AREA OF THE FABRICATED ESD PROTECTION CIRCUITS (WIDTH × LENGTH, UNIT: μm × μm)

		88 × 25	88 × 50	88 × 100	100 × 100	164 × 100
ESD Failure Threshold Voltage	Machine mode (MM)	150 V	500 V	> 1000 V*	> 1000 V*	> 1000 V*
	Human-body mode (HBM)	1800 V	5500 V	> 10 kV*	> 10 kV*	> 10 kV*

(*Limited by the ESD testing equipment.)

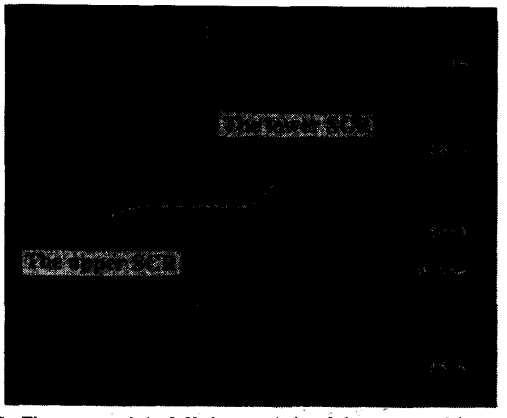

Fig. 5. The measured dc *I–V* characteristic of the upper and lower SCR structures in the fabricated ESD protection circuit with 88 × 100-μm^2 layout area. (Vertical scale: 2 mA/div; horizontal scale: 10 V/div.)

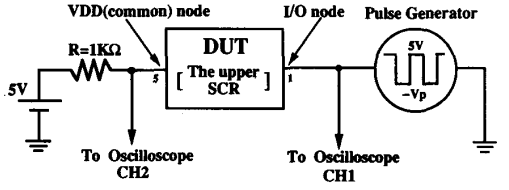

Fig. 6. The experimental setup to measure the ac triggering voltage of the fabricated ESD protection circuits.

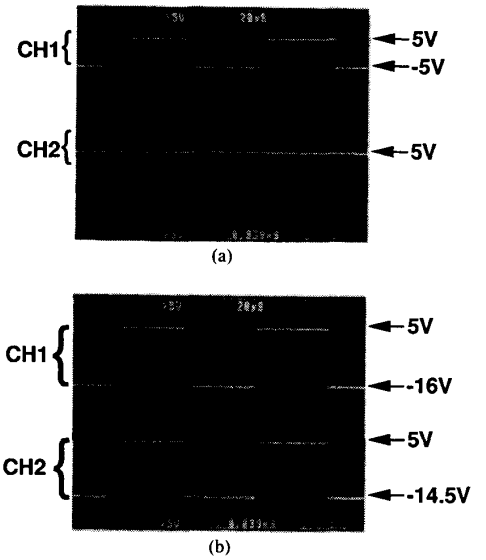

Fig. 7. The voltage waveforms in measuring the ac triggering voltage. CH1 is the applied square-pulse voltage. CH2 is the voltage observed at the V_{DD}(common) node of the ESD protection circuit. (a) The case when the upper SCR remains off. (b) The case when the upper SCR is triggered on. (Vertical scale: 10 V/div; horizontal scale: 20 μs/div.)

as shown in Fig. 7(b). Thus the ac trigger voltage is 21 V. In this way, the ac trigger voltage can be measured.

The measured dc and ac trigger voltages of the fabricated upper SCR in various ESD protection circuits with different layout dimensions and different minimum anode-to-cathode spaces are listed in Table II. These measured results show that the ac pulse-type trigger voltages are about 30% lower than their corresponding dc trigger voltages. This also confirms that the low ESD trigger voltage in the upper SCR of the proposed protection circuit can be achieved through suitable layout design. The ac/ESD trigger voltage can be further decreased if a larger well–substrate junction capacitance (C_{c1} + C_{c2}) in the lateral SCR structure is made. In Table II, it is also shown that the lateral SCR structure with a smaller minimum anode-to-cathode space has lower ac and dc trigger voltages.

As shown in Table II, the ac trigger voltage of 20 ~ 30 V is about 30% lower than its dc case. For a better input/output pad protection, the required ac/ESD trigger voltage is about 12 V. This much lower ac/ESD trigger voltage can be achieved by applying the design principles mentioned in Section II.

The zero-biased input capacitance measured at 100 kHz of the fabricated ESD protection circuits in various layout dimensions is also listed in Table II. Since the input capacitance is small enough and no diffusion resistor is used in this proposed ESD protection circuit, the propagating delay of signals from the I/O pad through this ESD protection circuit to its internal circuit is very small. Therefore, it is very attractive in high-speed applications.

IV. CONCLUSION

A new CMOS on-chip ESD protection circuit with dual lateral SCR structures has been successfully designed and fabricated. In this protection circuit, a lateral SCR struc-

TABLE II
LAYOUT AREA OF THE FABRICATED ESD PROTECTION CIRCUITS (WIDTH × LENGTH, UNIT: $\mu m \times \mu m$)

		88 × 25	88 × 50	88 × 100	100 × 100	164 × 100
Trigger Voltage	DC condition	30.3 V	27.6 V	28.1 V	44.7 V	44.1 V
	AC pulse-type condition	22.0 V	20.3 V	21.0 V	31.7 V	31.2 V
Zero-biased input capacitance (at 100 kHz)		0.36 pF	0.48 pF	0.57 pF	0.71 pF	0.89 pF
The minimum anode-to-cathode space		6 μm	6 μm	6 μm	9 μm	9 μm

ture is arranged for the positive ESD protection whereas the other one is arranged for the negative ESD protection. The testing results show that it can effectively perform the ESD protection with a small layout area. The low ESD trigger voltage of the proposed ESD protection circuit can also be achieved through the proper circuit and layout design. Since no device or junction breakdown is involved during the ESD transients, the performance and robustness of this protection circuit are not degraded by numerous ESD events. Without changing or adding any process step, this ESD protection circuit can be implemented by the p-well CMOS process. It can also be implemented dually by the n-well process as well. With very low input capacitance (less than 1 pF) and the above-described advantages, this proposed ESD protection circuit is very suitable for high-speed scaled-down CMOS VLSI.

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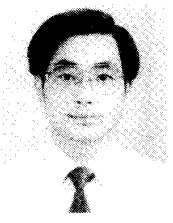

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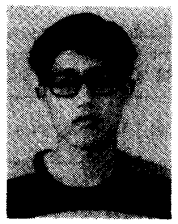

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