Numerical Analysis of the Looping Effect in GaAs MESFET's

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***Abstract*—The looping effect in the I_D-V_D characteristics of GaAs MESFET's on semi-insulating substrates has been studied using a two-dimensional numerical analysis. Both the transient and the steady-state behaviors of the looping phenomenon are simulated and discussed. Peak voltage- and frequency-dependent behaviors of the looping effect are analyzed. The I_D-V_D loop is due to the difference in the distribution of ionized EL2 concentration when the drain voltage rises and falls because of the trapping process of EL2's. The output conductance is also found to be frequency-dependent and is explained by the frequency-dependent modulation of the potential barrier height at the channel/substrate interface due to the drain-voltage variation.**

Nomenclature

- C_n Electron capture coefficient of EL2 traps.
- D_n Diffusion coefficient for electrons.
- $\vec{E}$ Electrical field.
- e_n Electron emission rate of EL2 traps.
- E_0 Critical electrical field.
- E_{CT} Energy difference between the conduction band edge and the EL2 level.
- f Frequency.
- I_D Drain current.
- $\vec{J}_n$ Electron current density.
- k Boltzmann constant.
- n Free-electron concentration.
- N_C Effective density of states in the conduction band.
- N_A Shallow acceptor concentration.
- N_A^- Ionized shallow acceptor concentration.
- N_D Shallow donor concentration.
- N_D^+ Ionized shallow donor concentration.
- N_T EL2 concentration.
- N_T^+ Ionized EL2 concentration.
- q Electron charge.
- t Time.
- T Temperature.
- v_{sat} Saturation velocity for electrons.
- V_D Drain voltage.
- V_G Gate voltage.
- ψ Electrostatic potential.
- μ_0 Low-field mobility for electrons.
- μ_n Field-dependent mobility for electrons.
- ϵ Permittivity of GaAs.

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I. Introduction

IT IS WELL KNOWN that the low frequency I_D-V_D characteristics of GaAs MESFET's fabricated on semi-insulating substrates exhibit the anomalous looping phenomenon (i.e., the hysteresis of drain current) [1]-[3]. The loops in the I_D-V_D curve are usually observed on a curve tracer or an oscilloscope when a continuous, periodic voltage with a frequency around 100 Hz is applied to the drain contact of a GaAs MESFET. The degree of the I_D-V_D loop is found to be frequency-dependent and peak-voltage-dependent [3]. The frequencies at which the looping phenomenon can be clearly seen usually range from 1 to 100 Hz. Although the loops are observed at normal operation voltage range, they are negligible when the drain voltage is small. It is believed that the phenomenon is attributed to the slow transient behaviors of the deep traps existing in semi-insulating substrates.

The looping effect not only complicates the analysis of the characteristics of MESFET's but also has a great influence on device performance. A complete understanding of the physical mechanism that governs the behavior of the phenomenon is important before this problem can be solved or circumvented. There have been several attempts in the past to study this effect by numerical or analytical methods [4], [5]. Son and Tang have studied the hysteresis in the I_D-V_D relationship by applying a single period of sinusoidal wave in the drain voltage [4]. However, this is not what people usually measure on a curve tracer, which displays a steady-state I_D-V_D curve using a continuous ac voltage on the drain. The shape of the loop in the I_D-V_D curve is kept fixed on the oscilloscope. A single period of the drain-voltage variation, unless it is very long, is usually not long enough to make the device reach steady state, so the I_D-V_D loop is still in transient state, which can be confirmed by the fact that the distributions of the ionized EL2 concentration at the start of the voltage pulse is quite different from that at the end of the voltage pulse [4, fig. 7]. In [5], Lee and Forbes used an effective time constant to model both the processes of electron capture and electron emission for the deep traps in the semi-insulating substrate. But in practice, the tran-

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sient behavior of the electrons captured by the ionized deep traps cannot be described by a single exponential function with a fixed time constant [6], [7]. Besides, the process of electron emission takes a much longer time to reach steady state than the process of the electron capture does [3], [6]. So, such a simplification of using an effective time constant cannot accurately describe the behaviors of the deep traps and the looping phenomenon.

In this work, the looping effects of the MESFET's both in transient state and in steady state are analyzed in depth by a fully two-dimensional numerical method. The Shockley–Read–Hall model is used to describe the behavior of the EL2 traps. The frequency-dependent and the peak-voltage-dependent behaviors of the looping effect are considered and explained.

II. Device Structure

The ion-implanted GaAs MESFET's used in this study is shown in Fig. 1. Different implantation profiles are chosen for the channel and the source and drain regions. In the vertical direction they are represented by the Gaussian function. The lateral spreading of implanted ions in the source and drain regions is described the complementary error function [8]. For the channel, the projected range, the straggle parameter, and the peak concentration are 0.076 μm, 0.05 μm, and 1.2×10^{17} cm^{-3}, respectively. For the source and drain regions, the projected range, the straggle parameter, the lateral spreading parameter, and the peak concentration are 0.1 μm, 0.07 μm, 0.07 μm, and 1.0×10^{17} cm^{-3}, respectively. The device threshold voltage is about -1 V. The gate length is 1 μm, and the spacing between the source/drain contacts and the gate is also 1 μm. The EL2 concentration N_T and the shallow-acceptor concentration N_A are chosen to be 5×10^{16} and 1×10^{15} cm^{-3}, respectively. Both N_T and N_A assumed in this study are typical values found in normal LEC substrates [9], [10]. The total depth of the simulated device structure is 3 μm which is deep enough to encompass all physical phenomena. In the study, the work function difference of the gate metal–semiconductor contact is assumed to be 0.8 eV.

III. Physical Models and Numerical Methods

The basic equations used in this study are shown in the following:

1) Poisson's equation:

$$\nabla^2 \psi = -\frac{q}{\epsilon}(-n + N_D^+ - N_A^- + N_T^+) \tag{1}$$

where N_T^+ is the ionized EL2 concentration. It is assumed that the shallow donors and acceptors are all ionized.

2) Drift-diffusion current continuity equation for electrons:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot \vec{J}_n - [C_n N_T^+ n - e_n(N_T - N_T^+)] \tag{2}$$

where C_n and e_n are, respectively, the electron capture

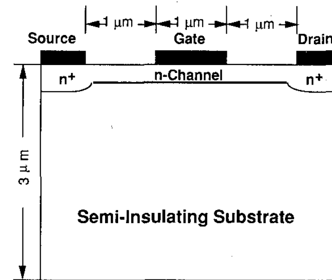

Fig. 1. Device structure of the ion-implanted GaAs MESFET on a semi-insulating substrate used in this study.

coefficient and the electron emission rate of the EL2 levels. The current density $\vec{J}_n$ is determined from

$$\vec{J}_n = qn\mu_n\vec{E} + qD_n\nabla n. \tag{3}$$

The field-dependent mobility μ_n is related to the electric field by [11]

$$\mu_n = \frac{\mu_0 + \dfrac{v_{\text{sat}}}{|\vec{E}|}\left(\dfrac{|\vec{E}|}{E_0}\right)^4}{1 + \left(\dfrac{|\vec{E}|}{E_0}\right)^4} \tag{4}$$

and the diffusion coefficient D_n by the Einstein relationship.

3) Rate equation for electron traps:

$$\frac{\partial}{\partial t}(N_T - N_T^+) = C_n N_T^+ n - e_n(N_T - N_T^+). \tag{5}$$

The relationship between C_n and e_n can be expressed as

$$e_n = C_n N_C \exp(-E_{CT}/kT) \tag{6}$$

where E_{CT} is the energy difference between the conduction band edge and the EL2 level and is assumed to be 0.69 eV at $T = 300$ K [12]. The temperature dependence of the electron emission rate e_n has been studied by many authors [13]. AT $T = 300$ K, an emission rate e_n of 0.04514 s^{-1} is used. C_n is then determined by (6).

In the above equations, the hole current and the terms associated with holes in the rate equation (5) are neglected because holes are minority carriers and the EL2's are electron traps. The surface states existing near the surface regions of the MESFET's can also give some anomalous effects such as gate lag and kink effects [3]. In this paper, these effects are not considered. We assume there are no surface states and the Neumann boundary condition is used for the top free surface region. The equations are discretized by the finite difference method and the full implicit BEF (Backward Euler Formula) algorithm is used for the time-dependent terms. The decoupled Gummel method [14] is used to solve these coupled equations. These physical models and numerical methods have been used and described elsewhere [6].

IV. Simulation and Discussions

In this simulation, the source voltage is 0 V, the gate voltage is kept fixed, and the drain voltage is allowed to swing between 0 and 2.5 V with a periodic symmetric triangular wave. For frequencies ranging from 1 Hz to 1 kHz, about five-to-ten periods of triangular function are enough to let the device reach steady state. The criterion of reaching steady state is that the shapes of the loops in the I_D–V_D curves do not change with time. Before the looping phenomenon in steady state is discussed, we first consider the transient behaviors of the phenomenon at f = 1 kHz, which will help to understand the looping effect in steady state.

A. Transient Behaviors

The simulated I_D–V_D occurred at the first period (t = 0–1 ms), the second period (t = 1–2 ms), and the tenth period (t = 9–10 ms) of drain voltage variation are shown in Fig. 2(a)–(c), respectively. The gate bias is fixed at 0 V and the frequency is 1 kHz. Before applying the periodic voltage to the drain contact, the drain voltage is 0 V and the device is in equilibrium. At the tenth period, the I_D–V_D curve has reached the steady state. Comparing Fig. 2(a) with Fig. 2(b), the loop phenomenon observed at the first period is more severe than that which occurred at the second period. At the tenth period, shown in Fig. 2(c), the loop in the I_D–V_D curve disappears. To explain the phenomenon that the loop in the I_D–V_D curve decays as the number of period increases, the depth profiles for the ionized EL2 concentration and the conduction band edge along the center of the gate at V_D = 0 V are shown in Fig. 3(a) and (b), respectively. In this figure, profile 1 is for V_D = 0 V and t = 0 ms, profile 2 is for V_D = 0 V and t = 1 ms, profile 3 is for V_D = 0 V and t = 2 ms, profile 4 is for V_D = 0 V and t = 10 ms. Besides, in Fig. 3(a), profile 5 is for V_D = 2.5 V and t = 9.5 ms. Profile 1 is quite different from profile 2, so it is expected that the looping phenomenon at the first period is quite severe, as shown in Fig. 2(a). Profile 3 is slightly different from profile 2, so it is expected that the looping phenomenon at the second period, as shown in Fig. 2(b), is less than that at the first period. By the time the drain voltage reaches the tenth period, the ionized EL2 distribution has already reached steady state. The profiles at t = 9.5 ms (profile 4) and at t = 10 ms (profile 5) are nearly identical. Therefore, the loop in the I_D–V_D curve is not observed.

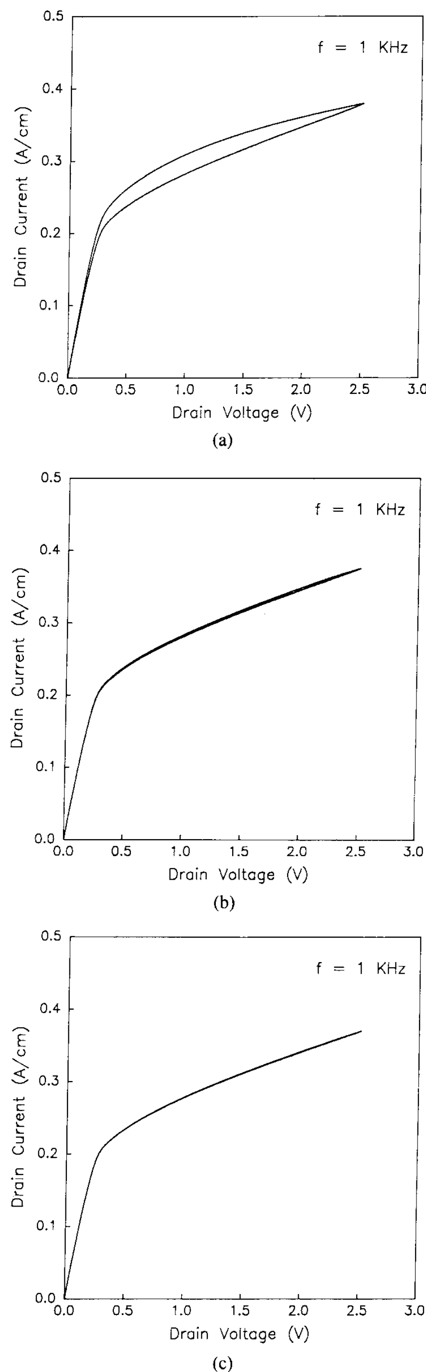

Fig. 2. Loops in I_D–V_D curve at (a) the first period, (b) the second period, and (c) the tenth period. The frequency is 1 kHz and the gate voltage is 0 V.

The transient phenomenon described above can be explained by the trapping and the detrapping processes of EL2's in the substrate. When the drain voltage suddenly rises, the process of electron capture dominates, and when the drain voltage suddenly falls, the process of electron emission dominates [6]. Because, the electron emission process has a longer time constant than the electron capture process [3], [6], the average capture rate is far larger than the average emission rate. At 1 kHz, the EL2 traps cannot completely respond to the ac signal. It is expected that at the first period, the number of captured electrons after the drain voltage rises from 0 to 2.5 V is more than the number of emitted electrons after the drain voltage falls from 2.5 to 0 V. Therefore, as shown in Fig. 3(a), the ionized EL2 concentration in the substrate side right at the end of the first period (i.e., t = 1 ms) is lower than

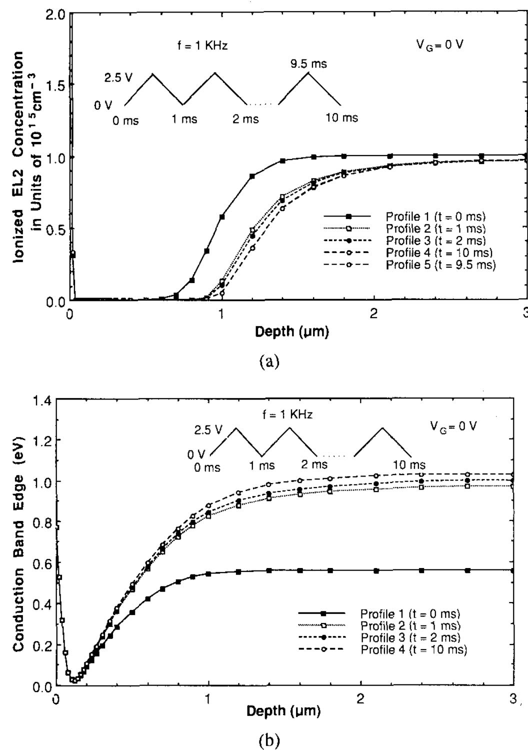

Fig. 3. Depth profiles for (a) the ionized EL2 concentration and (b) the conduction band edge. Profile 1 is for t = 0 ms and V_D = 0 V, profile 2 is for t = 1 ms and V_D = 0 V, profile 3 is for t = 2 ms and V_D = 0 V, and profile 4 is for t = 10 ms and V_D = 0 V. In (a), profile 5 is for t = 9.5 ms and V_D = 2.5 V. In (b), the energy reference level is the conduction band edge of the source contact, which is set at 0 eV.

that at the start of the first period (i.e., t = 0 ms). Since the point that the ionized EL2's distribution rises corresponds roughly to the edge of the depletion region in the substrate side at the channel/substrate interface, we can clearly see that the depletion edge also moves deeper into the substrate. So the depletion region width is wider at the end of the first period. This is why the current is lower when the drain voltage swings back from 2.5 to 0 V (see Fig. 2(a)). In the second period (t = 1–2 ms), the number of captured electrons is still more than the number of emitted electrons, so the ionized EL2 concentration in the substrate side continues to decrease. As the period number continues to increase, at V_D = 0 V, the edge of the depletion region shifts farther and the potential barrier height continues to increase until the steady state is reached.

B. Looping Effect and its Frequency Dependence

Because of the trapping effect, the I_D–V_D curve observed is different at different frequencies even at steady state, i.e., after many cycles of voltage excursion when the I_D–V_D curve is steady. Fig. 4(a)–(e) presents the simulated steady I_D–V_D curves with the drain voltage swings at 0.1 Hz, 1 Hz, 10 Hz, 100 Hz, and 1 kHz, respectively. The drain voltage swings between 0 and 2.5 V with a triangular wave. It is clearly seen that the loop in the I_D–V_D curve is very small at 0.1 Hz but becomes larger as the frequency increases. The strongest looping effect is observed when the frequency is at 10 Hz. At higher frequencies, the effect becomes smaller and finally it disappears at 1 kHz. In addition, the I_D–V_D loop is small for the gate voltage near the threshold voltage. The calculated results agree with the experimental results reported by Rocchi [3].

The frequency-dependent looping effect is directly related to the trapping and detrapping of the EL2's near the channel/substrate interface. As the drain voltage swings back and forth, the electrons are captured or emitted. After the I_D–V_D curve reaches steady state, the number of electrons captured should be the same as the number emitted during each voltage excursion. When the drain voltage swing is very fast, say 1 kHz or higher, with a period much shorter than the time constants of the trapping and detrapping processes, the EL2's in the substrate will not have enough time to respond to the changes of the drain voltage. The number of electrons captured or emitted is very small. So the EL2 distribution and the depletion region width at the channel/substrate interface at the same drain voltage will stay the same regardless of whether the drain voltage goes up or down. The resulting I_D–V_D curves, therefore, do not have any loop, just as the result obtained at 1 kHz. If the drain voltage swings at a very low frequency, say 0.1 Hz, the EL2's will have enough time to totally respond to the voltage change. At each drain voltage during the voltage swing, a steady state of ionized EL2 distribution is established. So the ionized EL2 distribution, the interface depletion region, and the I_D–V_D curve are not dependent on the direction of the voltage swing. The loop, therefore, does not appear in the I_D–V_D curve.

When the frequency of the drain voltage swing is between 1 and 100 Hz, i.e., with a period close to the time constant of the trapping process, steady-state ionized EL2 distributions cannot be reached during the voltage change. Electron emission will be dominant at a certain part of the voltage cycle and electron capture will be dominant at the other part of the voltage cycle. Fig. 5(a) and (b) shows the depth profiles of the conduction band edge along the center of the gate at V_D = 0 and 2.5 V, respectively. The frequencies are 0.1 Hz, 10 Hz, and 1 kHz. The energy reference level is the conduction band edge of the source contact, which is set at 0 eV. From Fig. 5(a), when the drain voltage is small or close to 0 V, for frequencies larger than 0.1 Hz, the potential barrier at the channel/substrate interface is higher than that in steady state (0.1 Hz) and the number of electrons that can inject into the substrate and be trapped is small, so the electron emission is the dominant process. From Fig. 5(b), when the drain voltage is close to the peak (2.5 V), for frequencies higher than 0.1 Hz, the potential barrier at the channel/substrate interface is lower than that in steady state (0.1 Hz) and more carriers can gain enough energy to overcome the interface potential barrier and inject into the substrate and

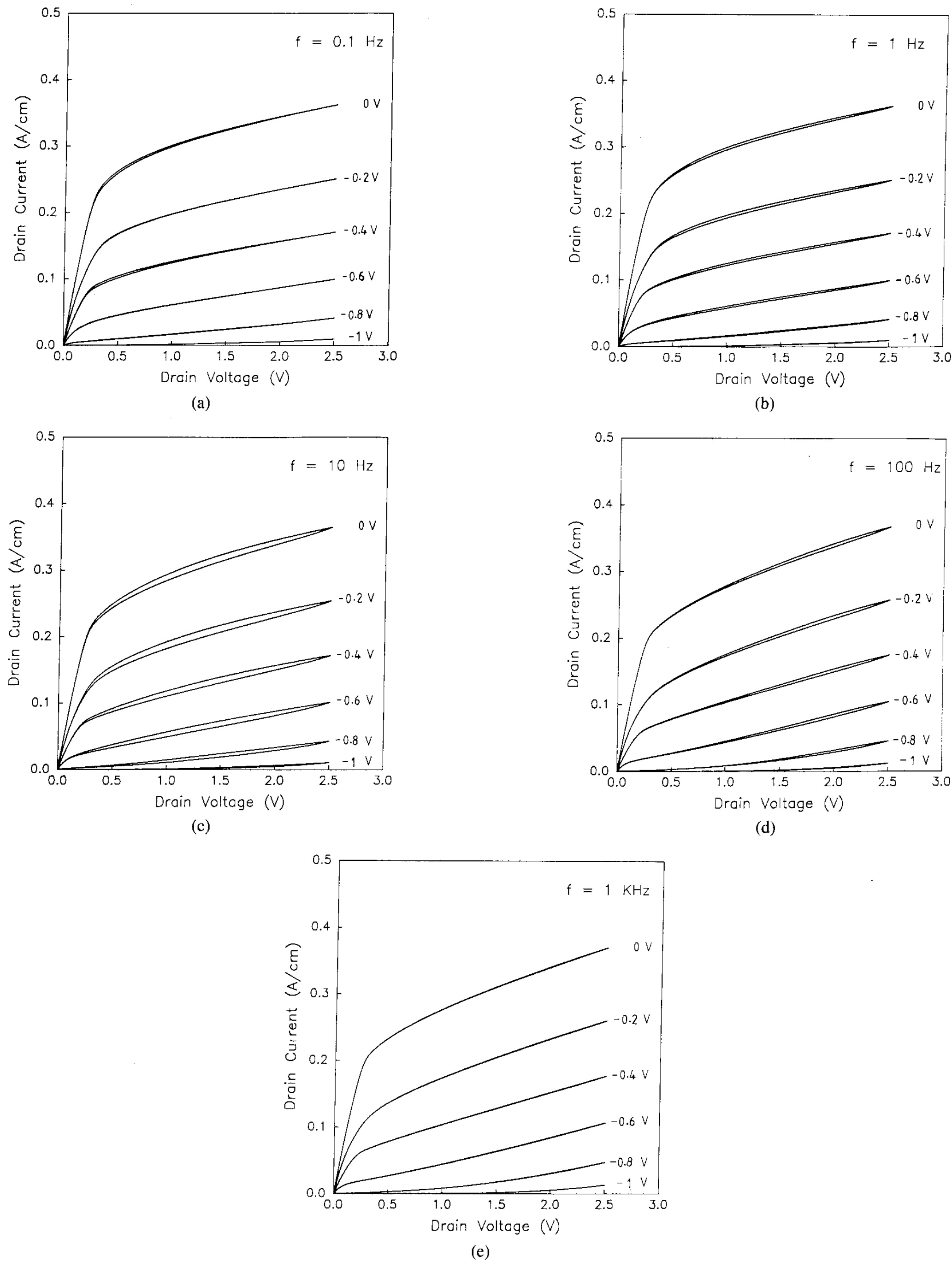

Fig. 4. Calculated I_D–V_D characteristics at f = (a) 0.1 Hz, (b) 1 Hz, (c) 10 Hz, (d) 100 Hz, and (e) 1 kHz.

get trapped. So the capture process dominates at this stage. When the drain voltage rises, the emission-dominant process will gradually change to the capture-dominant process, and when the drain voltage falls, the capture-dominant process will change to the emission-dominant process. At the end of the emission-dominant process, the number of ionized EL2's on the substrate side will be larger and the edge of the depletion region will be closer to the interface. While at the end of the capture process, because of the captured electrons, there will be less of ionized EL2's in the substrate side, moving the edge of the depletion region away from the interface. This difference in ionized EL2 distribution is verified by the simulated result shown in Fig. 6(a), in which the depth profiles

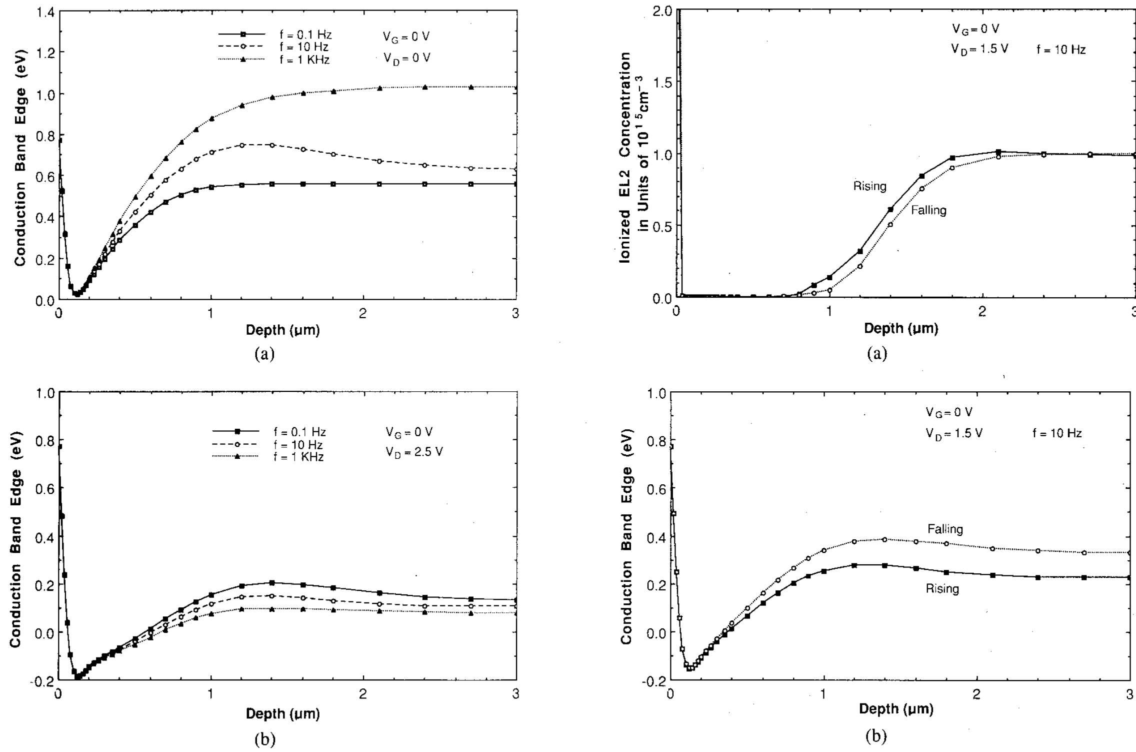

Fig. 5. Depth profiles for the conduction band edge at $f = 0.1$ Hz, 10 Hz, and 1 kHz at (a) $V_D = 0$ and (b) $V_D = 2.5$ V. The gate voltage is 0 V. The energy reference level is the same as that in Fig. 3(b).

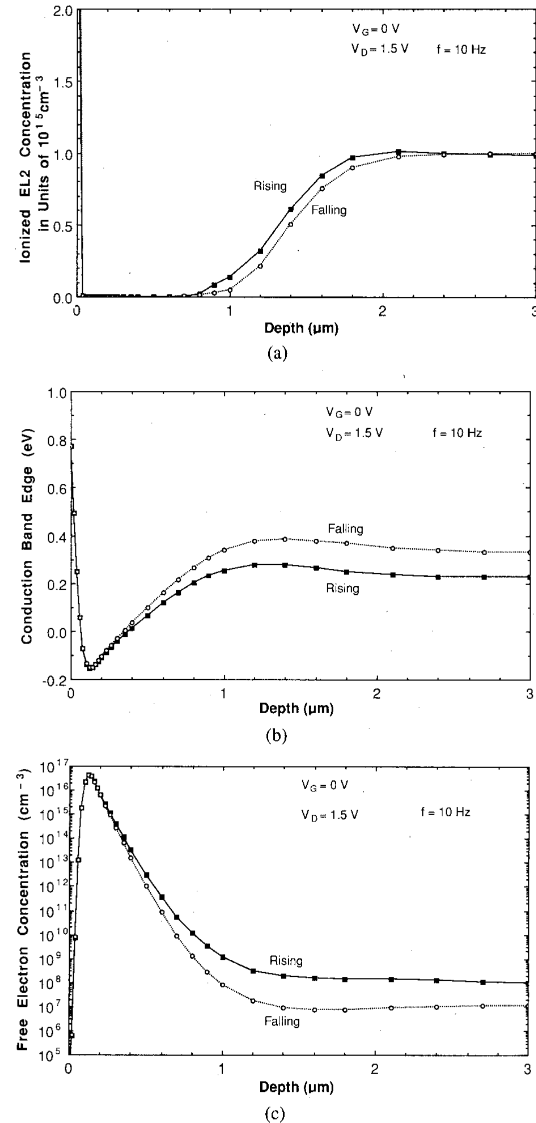

Fig. 6. Depth profiles for (a) the ionized EL2 concentration, (b) the conduction band edge, and (c) the free-electron concentration at $V_D = 1.5$ V when the drain voltage is rising and falling. In (b), the energy reference level is the same as that in Fig. 3(b).

for the ionized EL2's are shown at $V_D = 1.5$ V during the rise and fall of the drain voltage at $f = 10$ Hz. The corresponding conduction band edge and the free electron concentration are shown in Fig. 6(b) and (c), respectively. In Fig. 6(b), the energy reference level is the same as that in Fig. 5. When the drain voltage is falling, because of the captured electrons during the capture-dominant period, the potential barrier is higher and the free electron concentration in the substrate side is lower than those when the drain voltage is rising. So, when the voltage falls, the depletion region is wider, the interface potential barrier is higher, and the resulting current is lower. When the voltage rises, the depletion region is narrower, the interface potential barrier is lower, and the current is higher. A loop, therefore, appears in the I_D–V_D curve. The explanation for the gate-voltage-dependent looping effect is that for the gate voltage near the threshold voltage, the channel is nearly pinched off and the drain current is low so that the difference in the drain current when the drain voltage is rising and falling is not significant.

C. Frequency-Dependent Output Conductance

It can be noticed from Fig. 4 that in the linear region of the I_D–V_D curves the output conductance decreases as the frequency increases, while in the current saturation region of the I_D–V_D curves the output conductance increases as the frequency increases. This can be also explained by the frequency-dependent modulation of the interface potential barrier due to the drain voltage variation. From Fig. 5(a), the interface potential barrier at $V_D = 0$ V increases as the frequency increases, while from Fig. 5(b), the interface potential barrier at $V_D = 2.5$ V decreases as the frequency increases. With higher potential barrier at the channel/substrate interface, the effective active channel thickness is smaller due to a stronger self-backgating effect. Therefore, at small drain voltages around 0 V, the active channel thickness and the drain-current decrease as the frequency increases, while at large drain voltages around the peak voltage (2.5 V), the active channel thickness and the drain current increase as frequency increases. Therefore, at low drain voltages, the

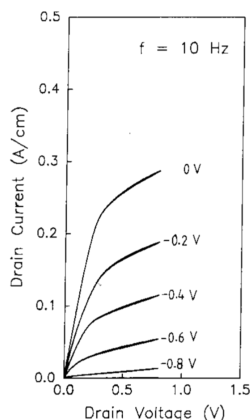

Fig. 7. Calculated I_D–V_D characteristic at $f = 10$ Hz with a peak voltage of 0.8 V.

output conductance is lower at higher frequencies, while at high drain voltages, the output conductance is higher at higher frequencies. It should be noticed, however, that the change in output conductance occurs around 1 to 100 Hz. When the frequency is very low, ≤ 0.1 Hz, the output conductance will be the same as that at dc, and when the frequency is very high, the output conductance will be saturated because the ionized EL2 distribution is "frozen" and cannot respond to the fast voltage changes.

D. Peak Voltage Dependence

Fig. 7 shows the calculated I_D–V_D characteristic with the drain voltage varied between 0 and 0.8 V. The frequency is 10 Hz. Comparing this figure with Fig. 4, we can see that the looping effect is dependent on the peak voltage of the applied drain bias. The looping effect in Fig. 7 is significantly reduced. The result agrees with the experimental results reported by Rocchi [3]. This phenomenon can be easily explained as follows: the number of electrons injected into the substrate is small when the peak voltage of the drain bias is small. As a result, for peak voltages small enough, the distribution of the ionized EL2 traps in the substrate side is hardly influenced by the applied drain voltage and there is no difference whether the drain voltage rises or falls. Therefore, the loop in the I_D–V_D curve cannot be clearly seen.

V. Conclusion

The looping effects both in the transient state and in the steady state have been studied by a fully two-dimensional numerical method. The looping effect in the transient state is usually stronger than that in the steady state. The steady-state looping effect is significant for frequencies ranging from 1 to 100 Hz. At 0.1 Hz and 1 kHz, the looping effect nearly disappears. The effect is related to the trapping and detrapping processes of the EL2's and their time response to the drain voltage change. The output conductance of the I_D–V_D curves is also frequency-dependent and is explained by the frequency-dependent modulation of the potential barrier height due to the drain voltage variation. The effect depends on the peak voltage of the drain voltage swing. At small V_D, such as 0.8 V, the looping effect is greatly reduced. From this study, we know that the trapping effect has a great influence on device characteristics. DC characterization is not enough to predict the device performance at ac operation conditions.

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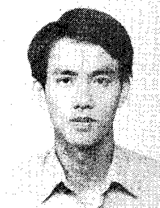

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While at Caltech, he worked on GaAs-based integrated optics. He was credited with the design and fabrication of several important optoelectronic components, including the first integrated optoelectronic circuit, which consists of a laser and a Gunn device fabricated on the same substrate. After graduation, he joined Bell Laboratories, where he worked on integrated optics and semiconductor lasers. He joined Rockwell International in 1979 and worked on GaAs integrated circuits. He did extensive work on substrate-related effects such as the orientation effect and the backgating effect. In 1982 he was promoted to Project Leader and later to Manager with responsibility for the development of ultra-high-speed integrated circuits using high electron mobility transistors. He received the Engineer of the Year award in 1982 for his contribution in GaAs IC and HEMT technologies. In 1987 he joined National Chiao-Tung University, where he is now a Professor and the Director of the Semiconductor Research Center. He is also the Director of the National Submicron Device Laboratory in charge of the construction of the first submicrometer device research center in the country. He is also currently manager of the Advanced Device Concept Department in Rockwell's Science Center. His current research interests are in the areas of III–V optoelectronic devices, MBE technology, heterostructure devices and physics, and device simulation.