Switched-capacitor pipelined logarithmic A/D and D/A convertors

M.-H. Cheng
T.-C. Huang

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Abstract: The paper presents two switched-capacitor circuits with modest complexity to implement a pipelined logarithmic digital–analogue convertor (LDAC) and logarithmic analogue–digital convertor (LADC), respectively, which spend only one clock time per conversion. In addition, the effect of the capacitor-ratio mismatch on the conversion errors of the convertor circuits is discussed. Hence, from the available maximum capacitor-ratio value and mismatch of the present integrated circuit (IC) technology, the feasible bit length of the pipelined LDAC and LADC can be computed.

1 Introduction

The difference between linear and logarithmic analogue–digital convertors is that the former keep the constant absolute accuracy, whereas the latter preserve the constant relative accuracy. Thus, for applications such as data compression, transmission and unit conversion [1, 2], which need a large dynamic range, the logarithmic convertor is usually employed. Recently, Lefas [3, 4] proposed two different approaches and applied switched-capacitor circuits to implement an LADC. One [3] employs the concept of successive approximation to realise the data conversion. For an N-bit LADC, this approach needs $2N - 1$ different capacitors, and its conversion time is N clocks. The other [4] applies the concept of charge redistribution and needs only two capacitors. However, it requires 2^N clocks to complete one data conversion.

Since digital signal-processing speed is increasing and the trend for merging the digital and analogue block in an IC chip is flourishing, the LADC and LDAC with higher conversion speeds are in great need. Thus, in this paper, we present two switched-capacitor circuits to implement a pipelined LADC and LDAC, respectively, which spend only one clock period per conversion. The major iterative operation of the convertors is an amplification with two switched gains, which is either some value A or its reciprocal $1/A$, dependent on a data bit. Clearly, it is suitable for switched-capacitor circuit realisation. In addition, we also discuss the worst effect of the capacitor-ratio mismatch on the conversion errors of the pipelined LDAC and LADC circuits. Hence, the feasible bit length of the LDAC and LADC can be calculated from the available maximum capacitor-ratio value and mismatch of the present IC technology.

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The authors are with the Department of Control Engineering, National Chiao Tung University, Hsinchu 30039, Taiwan, Republic of China

2 LDAC algorithm and switched-capacitor pipelined LDAC

Consider an N-bit logarithmic digital data $b_0 b_1 \cdots b_{N-1}$, with each bit b_i as 1 or 0. Then, the corresponding analogue value V_a is expressed as follows:

$$V_a = r^{b_0 2^0 + b_1 2^1 + \cdots + b_{N-1} 2^{N-1}} V_{ref} \quad (1)$$

where V_{ref} is the reference voltage, and r is the desired logarithmic base. Replacing each bit b_i of eqn. 1 by D_i, with $D_i = 1$ if $b_i = 1$, and $D_i = -1$ if $b_i = 0$, for $i = 0, 1, \ldots, N - 1$, we can obtain the following equation:

$$V_a = r^{D_0 2^{-1} + D_1 2^0 + \cdots + D_{N-1} 2^{N-2}} V_{ref} r^{(2^N - 1)/2} \quad (2)$$

Then, the analogue output V_a can be obtained iteratively by the following algorithm:

Step 0 (initialise): $V_a(N) = r^{(2^N - 1)/2} V_{ref}$
Step 1 (loop for): for $i = N - 1$ to 0
Step 2 (iterate): $V_a(i) = V_a(i + 1) r^{D_i 2^{i-1}}$
Step 3 (loop end): end for

Thus, $V_a(0)$ is the desired analogue output V_a. From the algorithm, an N-bit pipelined LDAC can be realised by cascading N amplification stages which can function as Step 2. The function of Step 2 can be realised by a switched-capacitor voltage gain circuit, in which the gain is dependent on the ratio of the precharging and evaluation capacitors. Thus, by interchanging the precharging and evaluation capacitors, the voltage gain will change to be reciprocal to the original. An offset-compensated voltage gain circuit, shown in Fig. 1, is developed to implement the function of Step 2. Two-phase non-overlapping clocks ϕ_P and ϕ_E set the circuit to precharge when $\phi_P = 1$ and to evaluate when $\phi_E = 1$. Data bit b_i is used to select the charging and evaluation capacitors, thus, the voltage gain is determined. When $b_i = 1$ and $\phi_P = 1$, the switch transistors Q_1, Q_2, Q_5, Q_6 and Q_7 are on, and the capacitor C_1 precharges to voltage V_{in}. As $\phi_E = 1$, the transistors Q_8 and Q_9 are on, and C_2 evaluates to drive $V_{out} = V_{in} C_1/C_2$. Similarly, when $b_i = 0$, the circuit precharges on C_2 as $\phi_P = 1$ and evaluates to drive $V_{out} = V_{in} C_2/C_1$ as $\phi_E = 1$. Therefore this circuit successfully accomplishes the function of Step 2. Moreover, this circuit is also offset-compensated [6].

Therefore the pipelined LDAC can be implemented by cascading the gain circuit of Fig. 1 with a different capacitor-ratio at each stage. For simplicity, we represent the circuit of Fig. 1 as a block with indicated capacitor ratio. The circuit shown in Fig. 2 is a 4-bit pipelined LDAC, where the block with T in the centre is an edge-

triggered time-delay element. Thus, by extension, an even N-bit LDAC requires N gain stages and $N(N+2)/4$ edge-triggered delay elements. We see that ϕ_1 connects to the precharge strobe of the odd stages and the evaluate strobe of the even stages. The evaluate strobe of the even

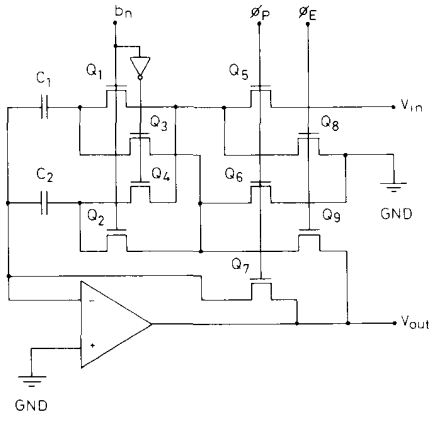

Fig. 1 *Two switched gains, offset-compensated voltage amplifier circuit*

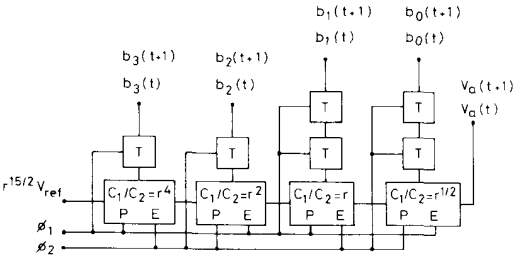

Fig. 2 *4-bit pipelined LDAC circuit*

stages and the precharge strobe of the odd stages are wired to ϕ_2. Hence, the precharging and evaluation operations are alternating for the even and odd stages. The advantages of such a connection are:

(*a*) it conforms to the operation of the gain circuits

(*b*) it can reduce the number of the delay elements.

The operation sequence of this circuit can be depicted by the timing diagrams of input data b_i, two-phase non-overlapping clocks ϕ_1 and ϕ_2, and analogue output V_a, which are shown in Fig. 3. Clearly, the conversion time is one clock period.

For N gain stages of an N-bit LDAC, the largest capacitor-ratio occurred at stage N is $r^{2^{N-2}}$ for $r > 1$, or $r^{-2^{N-2}}$ for $r < 1$. Usually, the following logarithmic bases, $r = 0.84$ (1.5 dB/step) or $r = 0.96$ (0.375 dB/step), are employed in commercial LDAC and LADC integrated

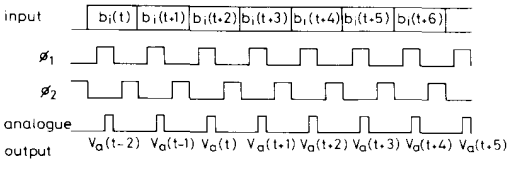

Fig. 3 *Timing diagrams of b_i, ϕ_1, ϕ_2 and V_a of Fig. 2 circuit*

circuits [7]. Thus, the largest capacitor-ratio for a 6-bit pipelined LDAC is 16.275 for $r = 0.84$ or 1.922 for $r = 0.96$. Such capacitor-ratios are feasible for the present IC technology.

3 LADC algorithm and switched-capacitor pipelined LADC

Similar to the method of the successive approximation for the linear ADC, the following algorithm will convert the analogue input V_{in} to its corresponding logarithmic digital output $b_0 b_1 \cdots b_{N-1}$:

Step 0 (initialise): $V_c(N) = V_{ref} r^{(2^{N-1}-1)/2}$

Step 1 (loop for): for $i = N - 1$ to 0

Step 2 (compare): if $V_{in} > V_c(i+1)$, then $b_i = 1$, $D_i = 1$ else $b_i = 0$, $D_i = -1$

Step 3 (iterate): if $i \neq 0$ then $V_c(i) = V_c(i+1) r^{D_i 2^{i-1}}$

Step 4 (loop end): end for

Based on the scheme proposed by Temes [5] for linear pipelined ADC, from the algorithm, we developed a 6-bit pipelined LADC, shown in Fig. 4, where the block with D in the centre is a level-triggered time-delay element. This circuit consists of five gain stages, three sample-hold circuits, 12 delay elements and six comparison stages, where each comparison stage contains a comparator and three switches. Therefore, an even N-bit pipelined LADC consists of $N - 1$ gain stages, $N/2$ sample-hold circuits, N comparison stages with $N/2$ switches for each stage and $N(N+2)/4$ delay elements. It is found that the required numbers of sample-hold circuit, delay element and switch at each comparison stage are nearly reduced by half in comparison with the conventional scheme proposed by Temes [5]. The reason is that this circuit takes only half of the clock period to complete all the operations of a loop of the algorithm. Therefore the circuit complexity is modest.

The operation of the circuit is discussed below. First, we consider the operation of the first gain stage and its adjacent gain stage. When $\phi_1 = 1$, the first gain stage will precharge $V_{ref} r^{3 1/2}$ to the capacitor, which is decided by the comparison result between V_{in} and $V_{ref} r^{3 1/2}$, and at the same time its adjacent gain stage is evaluating. As $\phi_2 = 1$, the first gain stage is evaluating to an output V_R, then the next gain stage is precharging this V_R to the capacitor, which is chosen by the comparison result between V_{in} and V_R. The operation procedure of the following two adjacent gain stages is the same as described above. Therefore the operation sequence of the circuit can be depicted by the timing diagrams of the switches S_A, S_B and S_C, the clocks ϕ_1, ϕ_2 and the output data bits which are shown in Fig. 5. Hence, the circuit can successfully implement a 6-bit pipelined logarithmic analogue/digital conversion in one clock period.

4 Error analysis of capacitor-ratio mismatch

Assume that the ideal capacitor-ratio is C_1/C_2 and its maximum relative error is ε, thus the physical capacitor-ratio is $C_1(1+\varepsilon)/C_2$. Hence, the maximum relative output error for our N-bit LDAC circuit will be $(1+\varepsilon)^N$, because N cascaded gain stages are employed. To constrain the error under the least significant bit, the following criterion should be met:

$$r^{-1/2} > (1+\varepsilon)^N > r^{1/2} \tag{3}$$

where $r < 1$. Thus, for a 6-bit LDAC, the maximum capacitor-ratio mismatch is 1.44% for $r = 0.84$, or 0.34% for $r = 0.96$. The same derivation can also be applied to the LADC. However, the exponent N in eqn. 3 will be changed to $N - 1$ because there are only $N - 1$ cascaded gain stages in the N-bit pipelined LADC. As a result, for a 6-bit LADC, the allowed maximum capacitor-ratio mismatch is 1.72% for $r = 0.84$, or 0.4% for $r = 0.96$.

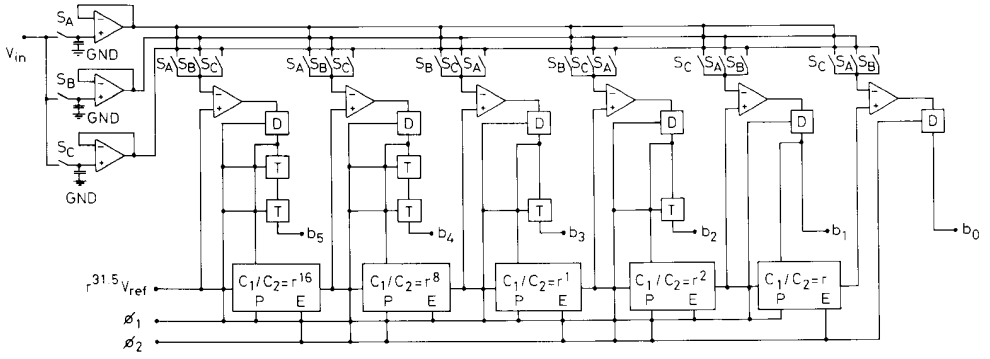

Fig. 4 *6-bit pipelined LADC circuit*

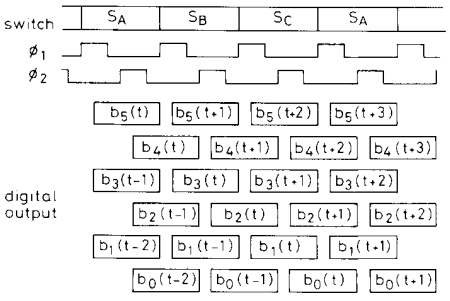

Fig. 5 *Timing diagrams of S_A, S_B, S_C, ϕ_1, ϕ_2 and output b_i of Fig. 4 circuit*

5 Conclusion

We have developed two switched-capacitor circuits with modest complexity for a pipelined LADC and LDAC, respectively, which complete one conversion per clock. This circuit is also offset-compensated. Moreover, we also discuss the effect of the capacitor-ratio mismatch on the conversion error. Therefore if the desired logarithmic base is chosen, from the needed maximum capacitor-ratio and capacitor-ratio mismatch of the circuits, we can compute the feasible bit length of the pipelined LDAC and LADC for the available IC technology.

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