Single-Fault Fault-Collapsing Analysis in Sequential Logic Circuits

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Abstract—**This paper studies single-fault fault collapsing in sequential logic circuits. Two major phenomena, self-hiding (SH) and delayed reconvergence (DR), which arise from the existence of feedback paths and storage elements in sequential circuits, are analyzed and found to cause the dominance relationship which is valid in combinational circuits but no longer valid in sequential circuits. A fault-collapsing procedure is proposed to collapse faults in sequential circuits. It first collapses faults in the non-SAD (self-hiding and delayed-reconvergence) gates of the combinational part of the sequential circuit and then further collapses faults by identifying the prime fan-out branches. Finally, it collapses faults in feedback lines. The collapsed faults constitute a sufficient representative set of prime faults. This procedure has been applied to collapse faults for 31 benchmark sequential circuits [1] and the number of faults has collapsed to 43% of the original number.**

I. Introduction

In testing, fault collapsing is usually employed to ease the burden of test generation and fault simulation. For combinational circuits, procedures have been proposed to collapse faults based on the equivalence and dominance relationships. For examples, Schertz and Metze [2] introduced a three-stage procedure to collapse faults in combinational circuits. Chang and Breuer [3] introduced a multiple-fault checkpoint-labeling procedure for sequential circuits, the checkpoints obtained being the lines for which faults need to be considered for testing. For *single-fault* sequential circuit fault collapsing, to the best of the author's knowledge, there have been no reported studies or results. Although Breuer and Friedman [4] stated that "the dominance relationship used in fault collapsing for combinational circuits is not valid for sequential circuits" and that "collapsing techniques based on fault equivalence on gates (for combinational circuits) can still be used (for sequential circuits)," no explicit results on how to collapse faults were presented.

In sequential circuits, owing to the existence of storage elements and feedback paths, fault propagation becomes quite complicated. Faults of dominance, after passing through delay elements and feedback paths, do not necessarily hold the relationship anymore. An example is demonstrated in Fig. 1, where C_{M1} is the combinational part of circuit $M1$. The output fault β (E struck-at-0) of G1 dominates the input fault α (B stuck-at-1) of $G1$ if only the combinational part C_{M1} of the circuit is to be considered. However, if the whole sequential circuit is considered, there is a test sequence: {(0, 0, 0), (0, 0, 1), (1, 1, 1) | (A, B, C)}, which can detect the fault α but not the fault β; i.e. α is not dominated by β. As will be explained later, this is caused by the "self-hiding" effect of the fault.

In this paper, the goal is to study the conditions which invalidate the dominance relationship in synchronous sequential circuits. It is to be shown that self-hiding and delayed reconvergence are two major phenomena which invalidate the relationship. For a non-SAD (self-hiding

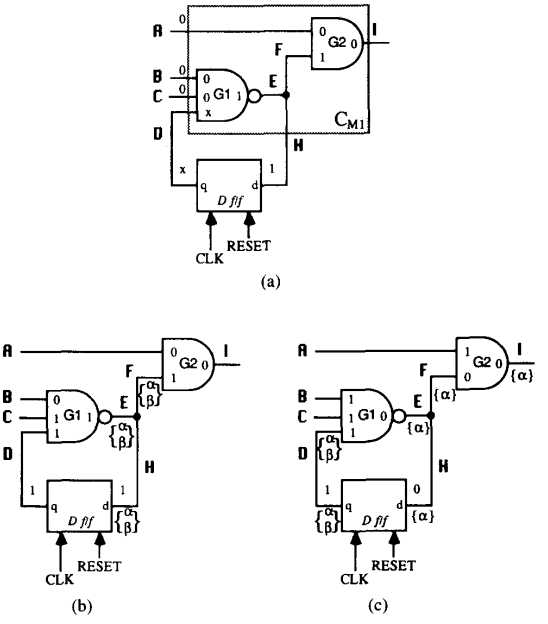

Fig. 1. An example of circuit $M1$, where C_{M1} is the combinational part of M1. (a) States of the circuit when the initialization pattern (0, 0, 0) is applied. (b) States and the propagation fault lists for $G1$ when the pattern (0, 0, 1) is applied. (c) States and the propagation fault lists for $G1$ when the pattern (1, 1, 1) is applied.

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and delayed-reconvergence) gate in the combinational part of a sequential circuit, the relationship still holds, and faults of the equivalence and dominance relationships can still be collapsed. Furthermore, the equivalence relationship between faults at the prime fan-out branches and their corresponding fan-out stems is also analyzed. Then new fault relationships in the delay elements (D flip-flops) are also identified to collapse the faults at feedback lines. A fault-collapsing procedure for single faults in nonredundant sequential circuits is then proposed to obtain a sufficient representative set of prime faults. Finally, this procedure is applied to 31 benchmark circuits [1] to collapse faults. The number of faults, after applying this procedure, can be reduced to 43% of the original number.

II. Model and Definitions

In this paper, only the synchronous sequential circuit is treated. This section discusses the circuit model and definitions which are to be used in the later sections.

A synchronous sequential circuit, M, is represented by the Huffman's model as shown in Fig. 2, where the network C_M is the combinational part of M, and D is a set of delay elements which are clocked and are able to be set/reset. Faulty signals which occur either at the network C_M or at the inputs/outputs of the delay elements D, may pass through C_M and be stored in D before propagating to primary outputs. To analyze the fault relationships for this synchronous sequential circuit, it is assumed that all dealy elements are D-type flip-flops and that faults are stuck-at-1 and stuck-at-0 faults.

For the purposes of clarity for the following analysis, the following definitions of g-equivalence/dominance, c-equivalence/dominance, and s-equivalence/dominance are given to distinguish between fault relationships in a single gate, in combinational circuits, and in sequential circuits, respectively.

Definition 1: Two faults, α and β, are said to be *g-equivalent* in a single gate if and only if the function under that fault α is equal to the function under the fault β for every input combination of the gate.

Definition 2: A fault β (g-dominant fault) is said to *g-dominate* another fault α (g-dominated fault) in a single gate if and only if every test for α is also a test for β.

Definition 3: Two faults, α and β, are said to be *c-equivalent* in a combinational circuit if and only if the function under the fault α is equal to the function under the fault β for every input combination of the circuit.

Definition 4: A fault β is said to *c-dominate* another fault α in a combinational circuit if an only if every test for α is also a test for β.

Definition 5: Two faults, α and β, are said to be *s-equivalent* in a sequential circuit if and only if the function under the fault α is equal to the function under the fault β for any input sequence of the circuit.

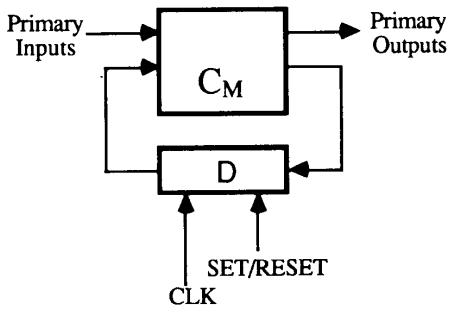

Fig. 2. Huffman's model of a synchronous sequential circuit M, where C_M is the combinational part of M, and D is a set of delay elements which are clocked and are able to be set/reset.

TABLE I
Controlling Value, d, Inversion Parity, p, and $v = (d \oplus p)$ for Wire, D Flip-Flop, and Each Type of Unate Gate

Gate Type	Controlling Value (d)	Inversion Parity (p)	$v = d \oplus p$
wire	0/1	0	0/1
BUFF	0/1	0	0/1
NOT	0/1	1	1/0
AND	0	0	0
OR	1	0	1
NAND	0	1	1
NOR	1	1	0
D f/f	0/1	0	0/1

Defintion 6: A fault β is said to *s-dominate* another fault α in a sequential circuit if and only if every test sequence for α is also a test sequence for β.

Given a gate G, $\boldsymbol{d}$ and $\boldsymbol{p}$ are the controlling value and the inversion parity of G, respectively, and $\boldsymbol{v} = (\boldsymbol{d} \oplus \boldsymbol{p})$. For an example, for a NAND gate G, the controlling value $\boldsymbol{d} = 0$, the inversion parity $\boldsymbol{p} = 1$, and $\boldsymbol{v} = (0 \oplus 1) = 1$. Table I shows the values for $\boldsymbol{d}$, $\boldsymbol{p}$, and $\boldsymbol{v}$ for each type of unate gate, the wire, and the D flip-flop.

With the above definitions, the following lemma and theorems can be stated without proof.

Lemma 1: For a gate G, the s-a-($\neg \boldsymbol{v}$) fault at the output of G g-dominates the s-a-($\neg \boldsymbol{d}$) fault at each input of G (($\neg \boldsymbol{v}$) denoting the complement value of $\boldsymbol{v}$). ◇◇

Theorem 1: If G is a gate in a nonredundant combinational circuit, the s-a-($\neg \boldsymbol{v}$) fault at the output of G c-dominates the s-a-($\neg \boldsymbol{d}$) fault at each input of G; i.e., the g-dominant fault of G also c-dominates the g-dominated fault of G in a nonredundant combinational circuit. ◇◇

Theorem 2: If G is a gate in a combinational circuit, all the input s-a-$\boldsymbol{d}$ faults and the output s-a-$\boldsymbol{v}$ fault of G are c-equivalent; i.e., the g-equivalent faults of a gate are also c-equivalent in a combinational circuit. ◇◇

III. Fault Analysis in the Combinational Network of Sequential Circuits

The discussion of the behavior of fault propagation in a synchronous sequential circuit can be divided into two parts. The first part is on the propagation in the combinational network of the sequential circuit, and the other is on the propagation in delay elements. In this section, fault propagation in the combinational network is first discussed.

A. Intergate and Intragate Fault Analysis

1) Self-Hiding: When a faulty signal propagates in the combinational network of a sequential circuit, the signal may pass through a feedback path and propagate to the node from which the faulty signal originates. A self-hiding phenomenon may occur. As described previously for the circuit example of Fig. 1, the fault α (B stuck-at-1) is c-dominated, but not s-dominated, by the fault β (E stuck-at-0) in C_{M1}. For the test sequence, {(0, 0, 0), (0, 0, 1), (1, 1, 1) | (*A*, *B*, *C*)}, the first pattern (0, 0, 0) is to initialize the D flip-flop, and the second pattern (0, 0, 1) activates both the faults α and β. Hence, α and β are included in the fault list of the line *E* of *G*1 (Fig. 1(b)). This fault list propagates to the lines *F* and *H*. After the next test pattern (1, 1, 1) is applied, the fault list for the line *H* passes through the D flip-flop and propagates to the line *D*. Under this pattern, the logic value 0 of the line *E* masks the fault β. As a result, only the fault α can propagate through *G*1 and *G*2 to the output *I*. The fault signal originating at the line *E* for the fault β propagates to the line *E* again and this faulty signal is masked by the fault β itself. Hence the s-dominance relationship between the fault α and the fault β does not hold, and the g-dominated fault α can be extracted from the propagating fault list under the applied test sequence. This phenomenon is called self-hiding.

Definition 7: A closed path is said to be an *O-path* with respect to an input of a gate if and only if the path originates from and terminates at the input of the gate and has an odd inversion parity.

In Fig. 1, *G*1 has an O-path, [*D*, *E*, *H*, *D*], with respect to the input *D* of *G*1. It should be pointed out that an O-path must pass through at least one delay element (D flip-flop) and a gate may have more than one O-path with respect to one of its inputs.

Definition 8: A pair of g-dominant and g-dominated faults of a gate is said to be *self-hiding* if the pair of faults originates from the gate and passes through an O-path (or O-paths) to the gate itself, and the g-dominated fault is not on the O-path (or O-paths).

Lemma 2: For a gate *G* in sequential circuit, if there exist the self-hiding phenomenon for the g-dominant fault at the output of *G* and the g-dominated fault at an input X_j of *G*, the gate *G* has O-paths with respect to at least one gate input X_j, where $j \neq i$.

Proof: For the gate *G*, let α and β be the g-dominated fault at the input X_i and the g-dominant fault at the output of *G*, respectively.

Case 1) If there is no closed path passing through *G*, the fault β cannot feed back to mask itself. No self-hiding phenomenon can occur.

Case 2) Suppose that *G* has closed paths which originate from and terminate at the gate input X_i only. In this case, the fault α is able to propagate to the faulty gate *G* itself only when the value of the input X_i is equal to the controlling value. Hence, the value of the gate output is $(\boldsymbol{d} \oplus \boldsymbol{p})$, and the g-dominant fault β of the output of *G* is also activated. Thus, the g-dominant fault β must be included in the propogating fault list with respect to the gate *G*. Hence, the g-dominant fault at the output of *G* and the g-dominated fault at the input X_i of *G* do not have the self-hiding phenomenon.

Case 3) Suppose that each closed path originating from and terminating at the gate input X_j, where $j \neq i$, has an even inversion parity. While the propagating fault list, $\{\alpha, \beta\}$ or $\{\beta\}$, with respect to *G* propagates back to the gate input X_j, the fault-free value of the gate input X_j is equal to the controlling value of the gate. Hence, the value of the gate output is $(\boldsymbol{d} \oplus \boldsymbol{p})$, and the g-dominant fault β of the output of *G* is activated for this case. Thus, the g-dominant fault β must be included in the propagating fault list when it propagates back to *G* if it is faulty. There exists no self-hiding phenomenon for the g-dominant fault at the output of *G* and the g-dominated fault at the input X_i of *G*. Hence, if the self-hiding phenomenon exists for the g-dominant fault at the output of a gate and the g-dominated fault at an input of the gate in a sequential circuit, the gate must have O-paths with respect to at least one other input of the gate. ◇◇

Definition 9: A gate in a sequential circuit is said to be *non-SH* (self-hiding) if and only if the gate has O-paths with respect to at most one gate input.

Lemma 3: For a non-SH gate in a sequential circuit, if the gate has no O-paths, the g-dominated faults at all of its inputs may be s-dominated by its corresponding output g-dominant fault. ◇◇

Lemma 4: For a non-SH gate in a sequential circuit, if the gate has only O-paths with respect to one gate input, the g-dominated fault at this gate input may be s-dominated by its corresponding output g-dominant fault. ◇◇

For a non-SH gate, all of its gate inputs, if the gate has no O-path, or the gate input, from which the O-path originates, are *s-dominatable*. By s-dominatable is meant that

the fault at this input could be s-dominated by its corresponding g-dominant fault at the gate output. Also, for a non-SH gate, the g-dominated fault at the s-dominatable input and the g-dominant fault at the output do not have the self-hiding phenomenon.

For the example circuit of Fig. 1, $G1$ has an O-path with respect to only the input D. It is a non-SH gate and the line D is an s-dominatable input of $G1$. However, the stuck-at-1 fault at the line B and the stuck-at-0 fault at the line E may have the self-hiding phenomenon. For $G2$, it does not have any O-path, it is also a non-SH gate, and both inputs A and F are s-dominatable inputs of $G2$.

2) Delayed Reconvergence: In sequential circuits, in addition to the self-hiding phenomenon, there is another phenomenon which invalidates the fault dominance relationship. This is due to the fact that faulty signals, originating from a fault, may pass and be stored in delay elements and then reconverge with the signals themselves. An example circuit, $M2$, is shown in Fig. 3 to demonstrate this phenomenon, where C_{M2} is the combinational part of the circuit. For the faults α (A stuck-at-1) and β (E stuck-at-0) in $G1$, from Theorem 1, the fault α is c-dominated by the fault β in C_{M2}. However, for this circuit, it can be seen that a test sequence: {(0, 0, 1), (0, 1, 1), (0, 0, 0) | (A, B, C)}, can detect α but not β. For this test sequence, the pattern (0, 0, 1) is to initialize the D flip-flop, and the pattern (0, 1, 1) is to activate the faults α and β (Fig. 3(b)). Under this pattern, α and β are included in the fault list of line E, and this fault list propagates to the lines F, H, and I. The faults are then stored in the delay element D flip-flop. With the last pattern (0, 0, 0) applied, the fault list at the line I passes through the D flip-flop and propagates to the line J. Also, with this pattern, the fault β is activated and this fault propagates to the input F of $G2$ and reconverges with the fault β of the fault list at the input line J of $G2$ (Fig. 3(c)). In this situation, only the fault α propagates to the line K. Hence, α is not s-dominated by β in the sequential circuit $M2$. This phenomenon is called delayed reconvergence.

Definition 10: A pair of g-dominant and g-dominated faults of a gate is said to exhibit delayed reconvergence if the two faults, originating from the gate and passing through paths, where some pass through delay elements, reconverge at some gates with different inversion parities.

With the above definition, one can define a non-DR (delayed-reconvergence) gate as follows.

Definition 11: A gate in a sequential circuit is said to be *non-DR* if and only if the gate is on paths

1) which do not reconverge at any gate; or
2) which reconverge at gates but every path passing through each of these gates does not pass through any delay element; or
3) which pass through different numbers of delay elements and reconverge at some gates and the paths which pass through any of these gates have the same inversion parity.

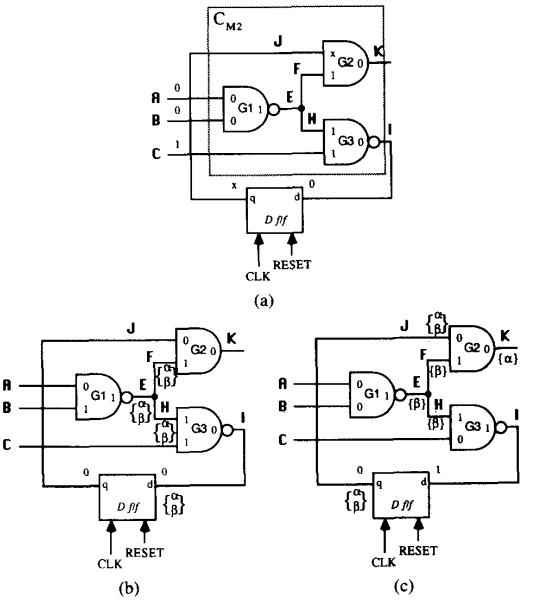

Fig. 3. An example circuit $M2$, where C_{M2} is the combinational part of $M2$. (a) States of the circuit when the initialization pattern (0, 0, 1) is applied. (b) States and the propagation fault lists for $G1$ when the pattern (0, 1, 1) is applied. (c) States and the propagation fault lists for $G1$ when the pattern (0, 0, 0) is applied.

By Definition 11, for the non-DR gate of cases 1 and 2, it is just like a gate in a combinational circuit. No delayed reconvergence can occur. For case 3, since the propagation paths which pass through different numbers of delay elements all have the same inversion parity, all the corresponding sensitized inputs of the reconvergent gate have the same logic value. For this situation, either the g-dominant fault alone or both the g-dominant fault and the g-dominated fault of the gate may propagate to the output of the reconvergent gate. Hence, for a non-DR gate in a sequential circuit, there is no delayed reconvergence at the reconvergent gate for the gate.

For the circuit of Fig. 3, $G1$ has two propagation paths to $G2$. The propagation path including lines E and F does not pass the D flip-flop and has an even inversion parity, and the other propagation path, including lines E, H, I, and J, passes through one D flip-flop and has an odd inversion parity. From Definition 11, $G1$ is a DR gate. Similarly, since $G2$ and $G3$ are on paths which do not reconverge at any gate, they are non-DR gates.

The DR phenomenon is very similar to SH from the point of view of fault propagation, except that for the SH phenomenon, the fault effect passes through cyclic paths (O-paths) to the gate from which it originates, while for the DR phenomenon, it propagates through delay elements and reconverges with the fault effect itself at another gate.

Theorem 3: For a nonredundant sequential circuit, only self-hiding or delayed reconvergence makes a fault pair

which is g-dominant and g-dominated be not s-dominant and s-dominated.

Proof: This theorem can be proved by proving that a pair of g-dominant and g-dominated faults which do not have the self-hiding *and* delayed-reconvegence will keep the s-dominance relationship.

For a pair of g-dominant and g-dominated faults, if there exists a sequence of tests to test the g-dominated fault, both the g-dominant and the g-dominated faults must first be activated. For this test sequence, both faults propagate along the sensitized paths with respect to the g-dominated fault. If the two faults do not have self-hiding and delayed reconvergence, they will neither pass through O-paths to the faulty gate itself nor pass through paths with delay elements and reconverge with different inversion parities. They will propagate to the primary outputs under this test sequence; i.e., the g-dominant fault will not be masked by itself. Thus, the s-dominance relationship for this fault pair holds. ◊◊

3) Dominance Fault Collapsing:

Definition 12: A gate in a sequential circuit is said to be *non-SAD* (self-hiding and delayed-reconvergence) if and only if the gate is both non-SH and non-DR.

Theorem 4: If G is a non-SAD gate in a nonredundant sequential circuit, the s-a-($\neg v$) fault at the output of G s-dominates the s-a-($\neg d$) fault at each s-dominatable input of G.

Proof: Since G is a non-SAD gate, it has at least one s-dominatable input. Since the circuit is nonredundant, there exists a test sequence which detects the s-a-($\neg d$) fault at the s-dominatable input. Since the s-a-($\neg d$) fault at the s-dominatable input of G is g-dominated by the s-a-($\neg v$) fault at the output of G, the test sequence which activates the g-dominated fault must activate the g-dominant fault. From Theorem 3, the g-dominated fault at the s-dominatable input of G and the g-dominant fault at the output of G have neither self-hiding nor delayed reconvergence. Under the test sequence, the g-dominant fault in the fault list with respect to G cannot be masked alone. Thus, the test sequence which detects the s-a-($\neg d$) fault at the s-dominatable input of G must detect the s-a-($\neg v$) fault at the output of G; i.e., the s-a-($\neg v$) fault at the output of G s-dominates the s-a-($\neg d$) fault at the s-dominatable input of G. ◊◊

As shown in Fig. 1, both $G1$ and $G2$ are non-SAD. Since line D is an s-dominatable input of $G1$, the stuck-at-1 fault (g-dominated fault) at line D is s-dominated by the stuck-at-0 fault (g-dominant fault) at line E. Similarly, since $G2$ does not have an O-path, both inputs A and F are s-dominatable inputs of $G2$. Hence, the stuck-at-1 faults at lines A and F are s-dominated by the stuck-at-1 fault at line I.

Corollary 1: In a nonredundant sequential circuit, if the g-dominant fault at the output of a non-SAD gate s-dominates the g-dominated fault at an s-dominatable input of the gate, the g-dominant fault also c-dominates the g-dominated fault. ◊◊

It is obvious that if faults at a gate are of s-dominance, they are also of c-dominance.

4) Equivalence Fault Collapsing:

Theorem 5: For a gate G in a sequential circuit, all the input s-a-d faults and the output s-a-v fault of G are s-equivalent.

Proof: When any of the input s-a-d faults or the outputs s-a-v fault occurs at the gate G, the output value stays at the stuck-at-value of v. Thus, the functions of the circuit under these two cases are the same for any input sequence. That is, all the input s-a-d faults and the output s-a-v fault of G are s-equivalent. ◊◊

From Theorems 2 and 5, the equivalence relationship is a combinational circuit holds for a sequential circuit. That is, g-equivalence is eqivalent to s-equivalence for a sequential circuit.

B. Fan-Out Fault Analysis

Definition 13: In a sequential circuit, a fan-out branch is said to be *prime* if and only if all the propagation paths from other fan-out branches of its fan-out stem to the primary outputs pass through this fan-out branch.

It is noted that the prime fan-out branch defined herein is similar to the singular fan-out branch mentioned in [3]. As shown in Fig. 1, for the fan-out branches F and H of the stem line E, since all the paths from the branch H to the primary output pass through the branch F, F is prime.

Theorem 6: In a sequential circuit, faults at a prime fan-out branch and at its corresponding fan-out stem are s-equivalent.

Proof: When a fault occurs at a prime fan-out branch or at its corresponding fan-out stem, the value of the fan-out branch is at its stuck-at value, and the function of the circuit under the fault is not influenced by the values of other fan-out branches of its corresponding stem. Thus, the function is the same for the circuit under the fault at the prime fan-out branch or at its corresponding fan-out stem. Hence, faults at a prime fan-out branch and at its corresponding fan-out stem are s-equivalent. ◊◊

IV. Fault Analysis in the Delay Elements (D Flip-Flops)

In this section, the behavior of faults at the delay elements is discussed. As mentioned in Section II, only D-type flip-flops are treated, and the flip-flops are able to be set/reset. However, the method and results can be extended to other types of flip-flops. It is also assumed that only a single stuck fault occurs at the input or output of the flip-flops and no faults occur at the clock line or the set/reset lines.

Definition 14: In a sequential circuit, a D flip-flop is said to be *non-SAD* if and only if the D flip-flop is on paths

1) which do not reconverge at any gate; or
2) which reconverge at gates but every path passing through each of these gates does not pass through any other delay elements; or
3) which pass through different numbers of delay elements and reconverge at gates and the paths which pass through any of these gates have the same inversion parity.

For the example circuits of Fig. 1 and Fig. 3, each flip-flop is non-SAD since there is only one flip-flop in each circuit. It is to be mentioned that, since a D flip-flop has only one input, no self-hiding phenomena can occur for the D flip-flop in a circuit.

Theorem 7: In a nonredundant sequential circuit, the output fault of a non-SAD D flip-flop s-dominates the input fault of the flip-flop.

Proof: The proof of this theorem is similar to that of Theorem 4. ◇◇

Definition 15: A D flip-flop which has a set/reset signal line is said to be *settable/resettable* if and only if the set/reset signal line is used to initialize the D flip-flop in test process.

Theorem 8: In a sequential circuit, for a settable (resettable) D flip-flop, the stuck-at-1(0) faults at the input and the output of the flip-flop are s-equivalent.

Proof: For a settable D flip-flop in a sequential circuit, initially set the state of the flip-flop to be 1. The output stuck-at-1 fault of the flip-flop is not activated, and the input stuck-at-1 fault of the flip-flop is blocked by the clocking signal. Hence, under the initialization pattern, the function of the circuit is independent of either of the faults. When the clocking signal is on, the D flip-flop always stays at 1 because of the stuck-at-1 fault, regardless of whether it is at the input or the output and the output value of the flip-flop is 1. Thus, the functions of the circuit under the two faults are the same for any test sequence after the initialization. Hence, the input and the output stuck-at-1 faults of a settable D flip-flop are s-equivalent. Similarly, the input and the output stuck-at-0 faults of a resettable D flip-flop are s-equivalent. ◇◇

V. Fault-Collapsing Procedure

With the above theorems, the fault-collapsing procedure for the synchronous nonredundant sequential circuit can be given as follows:

Procedure for Single-Fault Fault Collapsing

Step 1) Partition the given circuit M into two parts: the set of D flip-flops and the combinational part C_M, and levelize the circuit C_M.

Step 2) Determine all the SAD gates, the prime fan-out branches, and the SAD D flip-flops.

Step 3) Flag both ***S-A-1*** (stuck-at-1) and ***S-A-0*** (stuck-at-0) on each primary input, each nonprime fan-out branch, and the output of each nonsettable/resettable and SAD D flip-flop.

Step 4) Flag ***S-A-0*** on the output of each settable and SAD D flip-flop.

Step 5) Flag ***S-A-1*** on the output of each resettable and SAD D flip-flop.

Step 6) For each gate **G** (selected first from the lowest level in C_M):
IF all the inputs of **G** are of the ***S-A-d*** value,
THEN flag ***S-A-v*** on the output of **G**;
IF **G** is SAD, THEN flag ***S-A-***($\neg v$) on the output of **G**;
Remove ***S-A-d*** on each input of **G**.

Step 7) The flagged faults constitute an representative set of prime faults (RSPF).

From the above procedure, each fault in the circuit can be collapsed into a fault class of equivalence/dominance. To identify the SAD gates, the prime fan-out branches, and the SAD D flip-flops, the following procedures, based on each corresponding definition, are given.

Procedure for Determination of SAD/Non-SAD Gates

```
{
  /*Determination of SH/non-SH gates */
  FOR each gate G in the circuit; {
    Initiate the state of each line to be at "X";
    Mark the state of G according to Table II;
    DO {
      Determine the state of each gate except G according to Tables III and IV;
    } UNTIL no state changes;
    IF there is at most one "C" state at the input of G,
    THEN label G to be non-SH,
    ELSE label G to be SAD.
  }
  /*Determination of DR/non-DR gates */
  FOR each non-SH gate G in the circuit; {
    Initiate the state of each line to be at "XX";
    Mark the state of G according to Table V;
    DO {
      Determine the state of each gate except G according to Tables VI–VII;
    } UNTIL no state changes;
    IF there exists at least one "CC" state on any gate in the circuit,
    THEN label G to be SAD,
    ELSE label G to be non-SAD.
  }
} /*End of procedure for determination of SAD/non-SAD gates */
```

In Tables II, III, and IV, the states "X," "E," "O," and "C" denote the path inversion parity. "X" means

TABLE II
INITIALIZATION TABLE FOR EACH TYPE OF GATE IN THE PROCEDURE FOR DETERMINING SH/NON-SH GATES

Gate Type	Each Input	Output
AND	E	E
NAND	E	O
OR	O	O
NOR	O	E

TABLE III
EVALUATION FOR AND GATES, OR GATES, AND D FLIP-FLOPS IN THE PROCEDURE FOR DETERMINING SH/NON-SH GATES

Output Current State	Input			
X	X	E	O	C
E	E	E	C	C
O	O	C	O	C
C	C	C	C	C

TABLE IV
EVALUATION FOR NOT, NAND, AND NOR GATES IN PROCEDURE FOR DETERMINING SH/NON-SH GATES

Output Current State	Input			
X	X	O	E	C
E	E	C	E	C
O	O	O	C	C
C	C	C	C	C

TABLE V
INITIALIZATION FOR EACH TYPE OF GATE IN PROCEDURE FOR DETERMINING DR/NON-DR GATES

Gate Type	Output
AND	0E
NAND	0O
OR	0O
NOR	0E

TABLE VI
EVALUATION FOR AND AND OR GATES IN PROCEDURE FOR DETERMINING DR/NON-DR GATES ($m \neq n$)

	XX	nE	nO	nC	mE	mO	mC	CE	CO
XX	XX	nE	nO	nC	mE	mO	mC	CE	CO
nE	nE	nE	nC	nC	CE	CC	CC	CE	CC
nO	nO	nC	nO	nC	CC	CO	CC	CC	CO
nC	nC	nC	nC	nC	CC	CC	CC	CC	CC
mE	mE	CE	CC	CC	mE	mC	mC	CE	CC
mO	mO	CC	CO	CC	mC	mO	mC	CC	CO
mC	mC	CC	CC	CC	mC	mC	mC	CC	CC
CE	CE	CE	CC	CC	CE	CC	CC	CE	CC
CO	CO	CC	CO	CC	CC	CO	CC	CC	CO

TABLE VII
EVALUATION FOR NAND AND NOR GATES IN PROCEDURE FOR DETERMINING DR/NON-DR GATES ($m \neq n$)

	XX	nE	nO	nC	mE	mO	mC	CE	CO
XX	XX	nO	nE	nC	mO	mE	mC	CO	CE
nE	nO	nO	nC	nC	CO	CC	CC	CO	CC
nO	nE	nC	nE	nC	CC	CE	CC	CC	CE
nC	nC	nC	nC	nC	CC	CC	CC	CC	CC
mE	mO	CO	CC	CC	mO	mC	mC	CO	CC
mO	mE	CC	CE	CC	mC	mE	mC	CC	CE
mC	mC	CC	CC	CC	mC	mC	mC	CC	CC
CE	CO	CO	CC	CC	CO	CC	CC	CO	CC
CO	CE	CC	CE	CC	CC	CE	CC	CC	CE

TABLE VIII
EVALUATION FOR D FLIP-FLOPS IN PROCEDURE FOR DETERMINING DR/NON-DR GATES

X	X
nE	$(n + 1)$E
nO	$(n + 1)$O
nC	$(n + 1)$C
CE	CE
CO	CO

"don't care." "E" and "O" mean the even and the odd inversion parity, respectively. "C" denotes the state when "E" and "O" meet together; i.e., it represents a conflicting inversion parity. In Tables V–VIII, the state is represented by two words. The left word is an integer which denotes the number of D flip-flops passing through. "C" denotes the state when two different values meet together. The right word is the path inversion parity, and its notations are similar to those of Tables II, III, and IV.

Procedure for Determination of Prime Fan-out Branches

```
{
  FOR each fan-out stem in the circuit; {
    Initiate the state of each line to be at "X";
    FOR each fan-out branch,
      find all the paths from the branch to primary
      outputs until any of the primary outputs of this
      fan-out stem is reached;
    IF there exists one fan-out branch which reaches
      primary outputs and besides this
      fan-out branch, all other fan-out branches
      reach only the fan-out stem,
    THEN label this fan-out branch to be prime.
  }
} /*End of procedure for determination of prime fan-
  out branches*/
```

Procedure for Determination of SAD/Non-SAD D Flip-Flops

```
{
  FOR each D flip-flop in the circuit; {
    Initiate the state of each line to be at "XX";
```

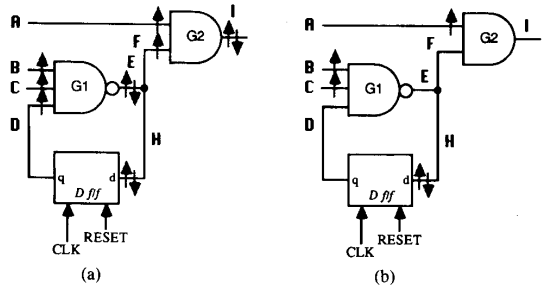

Fig. 4. (a) The 11 equivalent faults for the circuit $M1$ after collapsing with the s-equivalence relationship. (b) The five prime faults for the same circuit after collapsing with the s-equivalence and s-dominance relationships.

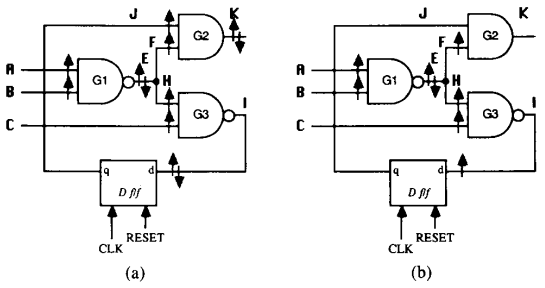

Fig. 5. (a) The 12 equivalent faults for the circuit $M2$ after collapsing with the s-equivalence relationship. (b) The eight prime faults for the same circuit after collapsing with the s-equivalence and s-dominance relationships.

Mark the state of the D flip-flop to be at "0E";
DO {
Determine the state of each gate except the D flip-flop according to Tables VI–VIII,
} **UNTIL** no state changes;
IF there exists at least one "CC" state on any gate in the circuit,
THEN label the D flip-flop to be **SAD**,
ELSE label the D flip-flop to be **non-SAD**.
}
} /*End of procedure for determination of SAD/non-SAD D flip-flops */

VI. Experimental Results on Benchmark Circuits

A. Run Examples

The circuit examples of Figs. 1 and 3 can be used to demonstrate the above fault-collapsing procedure. First, consider the circuit of Fig. 1:

Step 1) Partition the circuit and levelize the combinational part.
Step 2) Identify $G1$ and $G2$ to be non-SAD gates, the D flip-flop to be a non-SAD flip-flop, and line F to be prime.
Step 3) Flag both S-A-1 and S-A-0 on lines A, B, C, and H.
Step 6) For $G1$, remove S-A-0 on line B and S-A-0 on line C;
for $G2$, remove S-A-0 on line A.
Step 7) The RSPF consists of the stuck-at-1 fault at line A, the stuck-at-1 fault at line B, the stuck-at-1 fault at line C, and the stuck-at-1 and stuck-at-0 faults at line H.

The set of equivalent faults and the representative set of prime faults of the circuit are marked in parts (a) and (b) of Fig. 4. The circuit originally has 16 total faults. After applying equivalent-fault fault collapsing, the number of equivalent faults is reduced to 11. After applying prime-fault fault collapsing, the number of prime faults is further reduced to 5.

With the same step-by-step procedure applied to the circuit of Fig. 3, the total number of faults is reduced from 18 to 12 and 8 respectively for the number of equivalent faults and prime faults respectively. The reduced

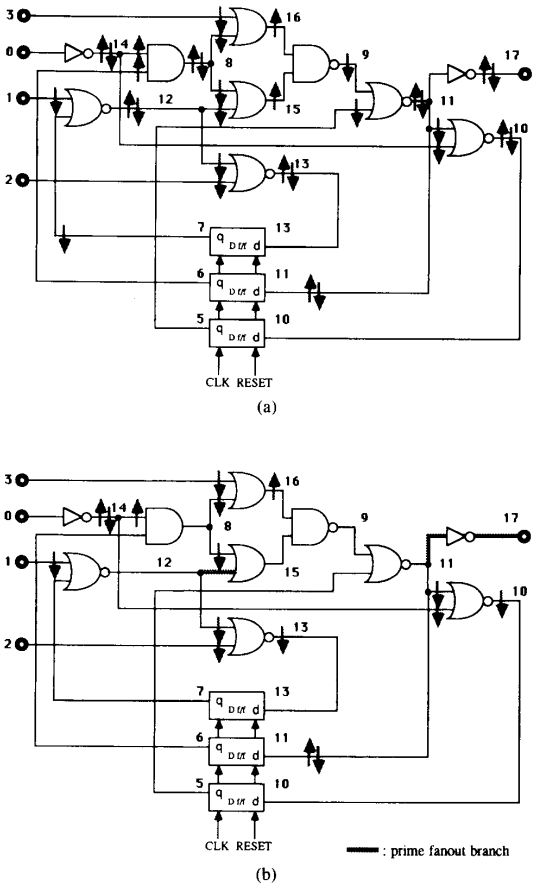

Fig. 6. (a) The 32 equivalent faults for the benchmark circuit s27 after collapsing with the s-equivalence relationship. (b) The 16 prime faults for the same circuit after collapsing with the s-equivalence and s-dominance relationships. The fan-out branches, line 12 → 15 and line 11 → 17, are prime.

equivalent and the prime faults are marked in Fig. 5(a) and (b), respectively.

Another circuit example, the benchmark circuit s27 [1], is shown in Fig. 6. The number of faults is reduced from 52 to 32 equivalent faults (shown in Fig. 6(a)), and 16

TABLE IX
RESULTS OF APPLYING FAULT-COLLAPSING PROCEDURE TO 31 BENCHMARK CIRCUITS

Circuit Name	No. of Gates	No. of non-SAD Gates	No. of Fan-Out Stems	No. of prime FOB's	No. of D f/f's	No. of Non-SAD D f/f's	No. of Total Faults	No. of Equivalent Faults	No. of C_prime Faults	No. of S_prime Faults
s27	10	10	4	2	3	3	52	32	25	16
s208	96	67	32	0	8	1	416	215	169	182
s298	119	82	34	8	14	6	596	308	266	252
s344	160	62	40	4	15	0	670	342	269	316
s349	161	60	41	4	15	0	680	350	275	324
s382	158	91	49	4	21	7	764	399	328	342
s386	158	88	26	0	6	0	772	384	295	340
s400	164	89	53	4	21	7	806	426	352	371
s420	196	135	66	0	16	1	840	430	340	368
s444	181	93	65	4	21	7	888	474	388	419
s510	211	67	73	0	6	0	1020	564	441	534
s526n	194	92	54	7	21	6	1052	553	473	492
s526	193	90	54	7	21	6	1052	555	474	494
s641	379	311	57	0	19	4	1278	467	398	409
s713	393	295	80	0	19	4	1426	581	496	521
s820	289	105	39	0	5	0	1640	850	702	786
s832	287	97	39	0	5	0	1664	870	718	806
s838	390	265	134	0	32	1	1676	857	679	740
s953	395	237	158	0	29	23	1906	1079	826	896
s1196	529	509	155	0	18	17	2392	1242	962	928
s1238	508	484	165	0	18	17	2476	1355	1034	1018
s1423	657	216	180	33	74	6	2846	1515	1212	1333
s1488	653	381	76	0	6	0	2976	1486	1110	1285
s1494	647	370	76	0	6	0	2988	1506	1123	1302
s5378	2779	2035	855	0	179	13	10590	4603	4033	4238
s9234	5597	3638	1013	60	228	7	18468	6927	5752	6522
s13207	7951	5734	1224	187	669	74	26358	9815	8234	8481
s15850	9772	6572	1518	242	597	58	31694	11725	9556	10406
s35932	16065	3861	5295	0	1728	0	71224	39094	30085	37366
s38417	22179	13695	4569	833	1636	74	76678	31180	25778	27647
s38584	19253	8238	3946	40	1452	2	76864	36303	30386	34447

prime faults (shown in Fig. 6(b), where all the gates and flip-flops are identified as non-SAD and the branches of line 12 → 15 and line 11 → 17 as prime) after applying the procedures.

B. Results on Benchmark Circuits

The above procedures have been implemented in C language on a SUN SPARC 330 workstation and applied to 31 benchmark circuits [1], and the results are listed in Table IX, where D flip-flops are assumed to be resettable. Besides the total number of original faults, the table also gives the numbers of equivalent faults and prime faults after collapsing; the analyzed characteristics of the circuits, such as the numbers of D flip-flops, fan-out stems, and gates; and the numbers of non-SAD D flip-flops, prime fan-out branches, and non-SAD gates. For the prime fault, the number of C_prime faults is the number of faults obtained by applying the prime-fault fault-collapsing procedure to the combinational parts of the circuits, assuming that the circuits are in the full-scan mode. The number of S_prime faults is the number of faults obtained by applying the above fault-collapsing procedure to the whole part of these circuits. Comparing the values of these two columns, for most of the cases, the numbers of S_prime faults are greater than those of C_prime faults. This means that most fault dominance relationships are invalidated by inclusion of delay elements. It is interesting to note that, for circuits s27, s298, s1196, and s1238, the numbers of S_prime faults are smaller than those of C_prime faults. This is because new fault equivalence/dominance relationships, which originally did not exist in combinational networks, are introduced by inclusion of the feedback paths and the delay elements. For an example, the equivalence relationship between the prime fan-out branch and its associated fan-out stem is created when feedback paths are connected to the combinational network. Also, it can be seen that, in general, the percentage of the numbers of reduced faults is proportional to the percentages of non-SAD gates and non-SAD D flip-flops of the total gates and the total D flip-flops, respectively, of a circuit. The average final equivalent faults, C_prime faults, and S_prime faults to the orginal total faults after reduction are approximately 50%, 40%, and 43%, respectively. It is to be mentioned that the proposed procedures are derived for nonredundant circuits. However, the procedures can also be applied to redundant circuits except that nonredundant faults may be collapsed to redundant faults for which no tests can be found. Since for the above benchmark circuits, many contain redundant faults, the final fault sets obtained in Table IX are not guaranteed to contain faults that are all detectable. A fault set derived from the procedures can be treated as an initial fault set of target faults [5] for a circuit for the later test generation. The run times for determination of SAD gates, prime fan-out branches, and SAD D flip-flops for the 31

TABLE X
RUN TIMES FOR DETERMINING SAD GATES, PRIME FAN-OUT BRANCHES, AND SAD D FLIP-FLOPS FOR THE 31 BENCHMARK CIRCUITS

Circuit Name	CPU Time for Determination of SAD Gates	CPU Time for Determination of Prime FOB's	CPU Time for Determination of SAD D f/f's
s27	0	0	0
s208	0.03	0.03	0.02
s298	0.10	0.05	0.02
s344	0.25	0.05	0.02
s349	0.25	0.05	0.02
s382	0.10	0.08	0
s386	0.13	0.02	0
s400	0.12	0.10	0.02
s420	0.13	0.10	0.02
s444	0.17	0.13	0.02
s510	0.33	0.08	0.02
s526n	0.38	0.17	0.03
s526	0.42	0.18	0.02
s641	0.20	0.07	0.03
s713	0.28	0.12	0.03
s820	0.47	0.13	0.02
s832	0.48	0.13	0.02
s838	0.50	0.38	0.07
s953	0.58	0.20	0.05
s1196	0.52	0.17	0.03
s1238	0.55	0.18	0.03
s1423	2.07	0.75	0.15
s1488	1.70	0.38	0.02
s1494	1.65	0.43	0
s5378	13.18	8.85	1.52
s9234	34.57	54.10	3.52
s13207	60.85	70.52	15.38
s15850	157.48	143.12	16.53
s35932	599.48	543.50	80.58
s38417	1090.40	922.40	102.77
s38584	1801.98	682.45	78.58

benchmark circuits are listed in Table X, where the time unit is in CPU seconds on a SUN SPARC 330 workstation.

For the benchmark circuits, it is to be mentioned that:

1) The benchmark circuit s400 has one floating input and one floating output which have either no driver or no load. In the run results, a primary input and a primary output had been added.
2 The benchmark circuits s9234, s13207, s15850, and s38417 have irregular circuit parts [3] which have no primary outputs, and the circuit functions have nothing to do with these circuit parts.

VII. CONCLUSIONS

In this paper, a study of fault collapsing for synchronous sequential circuits has been presented. Two phenomena, self-hiding and delayed reconvergence, are identified which invalidate the combinational fault dominance relationship in sequential circuits. These phenomena are caused by the existence of feedback paths and storage elements in sequential circuits. From this analysis, a single-fault fault-collapsing procedure for synchronous nonredundant sequential circuits has been proposed to reduce the faults that a test needs to be generated for. This procedure can be applied not only to a non-scan-mode circuit but also to a full-scan-mode circuit and a partial-scan-mode circuit by cutting the inputs and the outputs of scannable D flip-flops as the primary outputs and the primary inputs of the circuit, respectively. This procedure has been applied to collapse faults for 31 benchmark sequential circuits, and a 57% reduction in the number of faults has been obtained. The set of collapsed faults derived by applying this procedure constitutes a sufficient representative set of prime faults for each circuit. It is believed that this is the maximum fault reduction so far reported for sequential circuits.

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REFERENCES

[1] F. Brglez, D. Bryan, and K. Kozminski, "Combinational profiles of sequential benchmark circuits," in *Proc. IEEE Int. Symp. Circuits Syst.*, 1989, pp. 1929–1394.
[2] D. R. Schertz and G. Metze, "A new representation for faults in combinational digital circuits," *IEEE Trans. Comput.*, vol. C-21, pp. 858–866, Aug. 1972.
[3] S.-J. Chang and M. A. Breuer, "A fault-collapsing analysis in sequential logic networks," *Bell Syst. Tech. J.*, vol. 60, no. 9, pp. 2259–2271, Nov. 1981.
[4] M. A. Breuer and A. D. Friedman, *Diagnosis and Reliable Design of Digital Systems.* Woodland Hills, CA: Computer Science Press, 1976.
[5] M. Abramovici, P. R. Menon, and D. T. Miller, "Checkpoint faults are not sufficient target faults for test generation," *IEEE Trans. Comput.*, vol. C-35, pp. 769–771, Aug. 1986.

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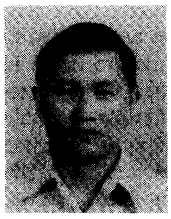

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