

# Direct Evidence of Gate Oxide Thickness Increase in Tungsten Polycide Processes

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**Abstract**—The increase of the “effective” gate oxide thickness for W-polycide processes is studied. The samples with as-deposited and annealed W polycide are analyzed by secondary ion mass spectrometry, transmission electron microscopy (TEM), and high-frequency *CV* measurements. The TEM cross section shows that the gate oxide thicknesses are  $\sim 244$  and  $\sim 285$  Å for as-deposited and  $1000^\circ\text{C}$  annealed samples, respectively. The TEM results agree with that from *CV* measurements. The TEM analyses provide a direct physical evidence of an additional oxide thickness ( $\sim 41$  Å) during the W-polycide annealing.

## I. INTRODUCTION

RECENTLY, more IC manufacturers choose to use tungsten (W) polycide gates instead of Ti-salicide processes in their CMOS technologies, even down to submicrometer regimes, due to the manufacturability of W-polycide gates. However, in the chemical-vapor-deposited tungsten polycide processes, there are two major concerns. One is the peeling problem [1], and the other is the current-drive degradation of MOS devices due to gate oxide thickening during the W-polycide processes [2]–[4]. It has been reported that the “effective” gate oxide thickness becomes thicker based on the *CV* measurement [4]. Wright and Saraswat [2] used an ion implanter to introduce fluorine into the gate oxide, and from the *CV* measurement and ellipsometer data they concluded that the “effective” oxide thickness increased by the additional oxide thickness rather than the change of the oxide dielectric constant. In this paper, we use transmission electron microscopy (TEM), instead of ellipsometer measurements, to directly prove that the gate oxide is indeed physically becoming thicker. To our best knowledge, this direct evidence has not yet been reported elsewhere.

## II. EXPERIMENTAL

A  $250\text{-}\text{\AA}$  gate oxide was grown at  $920^\circ\text{C}$  in a dry  $\text{O}_2$  ambient. The gate was formed by a  $2500\text{-}\text{\AA}$   $\text{POCl}_3$ -doped polysilicon and a  $2500\text{-}\text{\AA}$   $\text{WSi}_x$  film. The tungsten silicide was deposited using the GENUS 8710 system. After the polycide pattern was defined, the polycide films were annealed at  $800$ ,  $920$ , and  $1000^\circ\text{C}$ , respectively, all in  $\text{O}_2/\text{N}_2$  ambients. The ambient was initially filled with  $\text{O}_2$  at a flow

rate of  $14$  l/min for  $20$  min, followed by  $\text{N}_2$  with a flow rate also at  $14$  l/min for  $10$  min. Instead of furnace annealing, some wafers were annealed by rapid thermal annealing (RTA) at  $1100^\circ\text{C}$  in  $\text{O}_2$  ambient with a flow rate at  $2$  l/min for  $20$  s. The as-deposited and annealed samples were then analyzed by secondary ion mass spectrometry (SIMS), high-resolution transmission electron microscopy, and high-frequency *CV* measurements. SIMS was used to measure the amount of fluorine diffused into oxides. The TEM cross sections were observed at the  $\langle 110 \rangle$  pole under multibeam bright-field diffraction conditions for accurate delineation of the morphology of various polysilicon/oxide/substrate interfaces.

## III. RESULTS AND DISCUSSION

Fig. 1(a) and (b) shows the SIMS profile of fluorine in W polycide before and after  $1000^\circ\text{C}$  annealing, respectively. Very high concentration of fluorine is found in gate oxides for the sample annealed at  $1000^\circ\text{C}$  (see Fig. 1(b)). The concentration of fluorine is approximately  $\sim 3 \times 10^{21}$  atom/ $\text{cm}^3$ , compared to  $5 \times 10^{18}$  for the as-deposited sample. The TEM cross section (Fig. 2(a)) from the as-deposited W-polycide sample shows that the gate oxide thickness is  $\sim 244$  Å and that the polysilicon/gate oxide interface is quite smooth. Fig. 2(b) shows the TEM cross section for the  $1000^\circ\text{C}$  annealed sample. The gate oxide thickness is  $\sim 285$  Å and the polysilicon/gate oxide interface is much rougher when compared to that in Fig. 2(a). Comparison between Fig. 2(a) and (b) provides direct physical evidence of an additional oxide thickness ( $\sim 41$  Å) during the W-polycide annealing.

The results from *CV* measurements and TEM analyses for samples annealed at different temperatures are summarized in Table I. The table shows that the oxide thicknesses are the same for the polysilicon gate sample annealed at  $1000^\circ\text{C}$  and for the as-deposited and after  $800^\circ\text{C}$  annealed W-polycide samples. The “effective” gate oxide thickness for W-polycide samples is increased as the annealing temperature is above  $920^\circ\text{C}$ . Additional oxide thickness increases of  $6\%$  and  $12\%$  are found for samples annealed at  $920$  and  $1000^\circ\text{C}$ , respectively. For RTA annealing at  $1100^\circ\text{C}$  for  $20$  s, a  $5.2\%$  thickness increase was found. The RTA  $1100^\circ\text{C}$  annealing reduces the amount of fluorine diffusion into oxides, and the increased oxide thickness is equivalent to that of the  $920^\circ\text{C}$  furnace annealing. The additional oxide thickness obtained from *CV* measurements agrees with that from TEM analyses.

From the above arguments, we conclude that the increased

Manuscript received June 19, 1991; revised August 26, 1991.  
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IEEE Log Number 9104127.

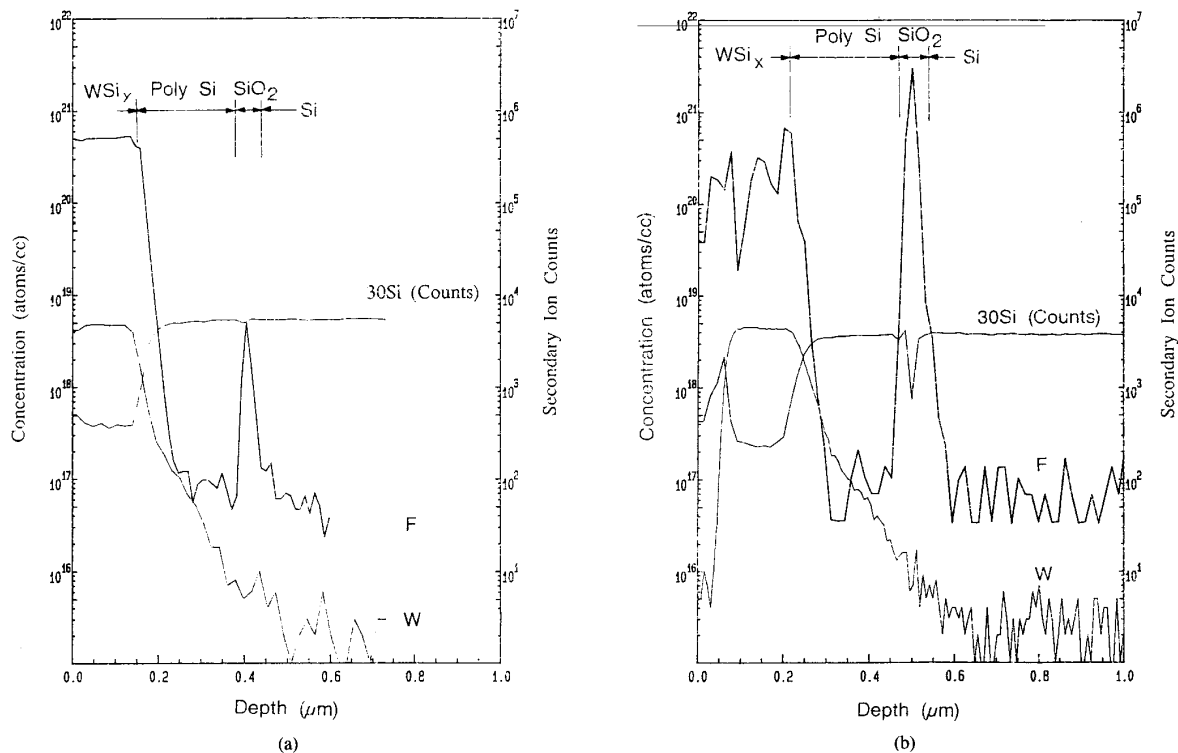


Fig. 1. (a) The SIMS profile of fluorine for the sample with as-deposited W polycide. (b) The SIMS profile of fluorine for the W-polycide sample after  $1000^\circ\text{C}$ ,  $\text{O}_2/\text{N}_2$  anneal.

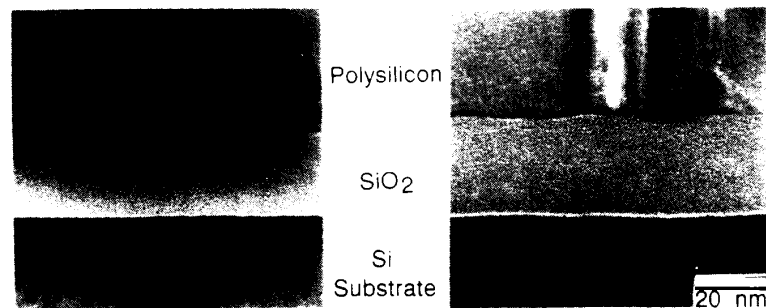


Fig. 2. (a) The TEM cross section from the as-deposited W-polycide sample. The gate oxide thickness is  $\sim 244 \text{ \AA}$ . (b) The TEM cross section from a  $1000^\circ\text{C}$ ,  $\text{O}_2/\text{N}_2$  annealed sample. The gate oxide thickness is  $\sim 285 \text{ \AA}$ .

TABLE I  
OXIDE THICKNESSES FROM  $CV$  AND TEM MEASUREMENTS FOR  
SAMPLES ANNEALED AT DIFFERENT CONDITIONS

Process Conditions	$T_{ox}$ ( $\text{\AA}$ ) (from $CV$ )	$T_{ox}$ ( $\text{\AA}$ ) (from TEM)
Poly gate + $1000^\circ\text{C}$ anneal in $\text{O}_2/\text{N}_2$	250	—
$\text{WSi}_x$ polycide + no anneal	247	244
$\text{WSi}_x$ polycide + $800^\circ\text{C}$ anneal in $\text{O}_2/\text{N}_2$	250	—
$\text{WSi}_x$ polycide + $920^\circ\text{C}$ anneal in $\text{O}_2/\text{N}_2$	265	—
$\text{WSi}_x$ polycide + $1000^\circ\text{C}$ anneal in $\text{O}_2/\text{N}_2$	280	285
$\text{WSi}_x$ polycide + RTA $1100^\circ\text{C}$ , $\text{O}_2$ , 20 s	263	—

“effective” oxide thickness is indeed due to the oxide growth during annealing. As proposed in [2], this phenomenon is due to the interaction of fluorine with oxides. Fluorine is a strong reductant that can break the Si-O bonds and displace oxygen at these sites. The released oxygen then diffuses to the interfaces, oxidizes silicon and polysilicon, and results in the additional oxide thickness.

#### IV. SUMMARY

We have shown that fluorine diffused from tungsten silicide films to gate oxides causes additional oxide growth.

From *CV* measurements, TEM analyses, and SIMS results, we have directly shown that the increased "effective" oxide thickness is actually due to the oxide growth during W-polycide annealing.

#### ACKNOWLEDGMENT

The authors would like to acknowledge help in wafer fabrication from S. L. Ying, C. H. Fang, M. H. Liaw, J. J. Lin, and Dr. L. S. Tsai.

#### REFERENCES

- [1] C. S. Yoo, T. H. Lin, and N. S. Tsai, "Si/W changes and film peeling during polycide annealing," *Japan. J. Appl. Phys.*, vol. 29, pp. 2535-2540, 1990.
- [2] J. Wright and K. C. Saraswat, "The effect of fluorine in silicon dioxide gate dielectrics," *IEEE Trans. Electron Devices*, vol. 36, pp. 879-889, 1989.
- [3] Y. Shioya, S. Kawamura, I. Kobayashi, M. Madeda, and K. Yanagida, "Effect of fluorine in chemical-vapor-deposited tungsten silicide film on electrical breakdown of SiO<sub>2</sub> film," *J. Appl. Phys.*, vol. 61, pp. 5102-5109, 1987.
- [4] R. A. Chapman *et al.*, "0.5 micron CMOS for high performance at 3.3 V," in *IEDM Tech. Dig.*, 1988, pp. 52-55.