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Surface & Coatings Technology 202 (2007) 1287–1291
SURFACE & COATINGS TECHNOLOGY
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Characteristics of poly-Si TFT combined with nonvolatile SONOS memory and nanowire channels structure

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Available online 23 August 2007

Abstract

In this work, we study a polycrystalline silicon thin-film transistor (poly-Si TFT) combined with a silicon–oxide–nitride–oxide–silicon (SONOS) stack gate dielectric and nanowire channels structure for the applications of transistor and nonvolatile memory. The proposed device named with NW SONOS-TFT has superior electrical characteristics of transistor and also can exhibit high program/erase (P/E) efficiency under adequate bias operation. The V_{th} decreases from 2.45 V to 1.76 V and subthreshold swing reduces from 0.57 V/decade to 0.42 V/decade. The programming V_{th} shift is improved from 2.2 V to 3.3 V at 14 V for 1 s and the erasing V_{th} shift is improved from −0.3 V to −1.3 V at −14 V for 1 s. The dramatic improvement can be attributed to the tri-gate structure and corner effect. In addition, the memory device has a promising data retention behavior at 85 °C and a 0.8 V memory window after 5×10^3 P/E cycles operations. Hence, the NW SONOS-TFT is suitable for application in the future system-on-panel display.
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Keywords: Poly-Si; SONOS; Nanowire; Nonvolatile memory; Thin film transistor (TFT)

1. Introduction

Polysilicon thin-film transistors (poly-Si TFTs) have attracted much considerable attention because of their wide application in active matrix liquid-crystal-displays (AMLCD), memory devices such as dynamic random access memories (DRAMs) [1], static random access memories (SRAMs) [2], and electrically erasable programmable read-only memories (EEPROMs) [3]. Especially, the application in AMLCDs is the primary trend, leading to the rapid development of poly-Si TFT technology. Recently, the high performance of poly-Si TFTs were demonstrated to be integrated with peripheral driving circuits [4]. In order to make the display more compact, reliable and further reduction in the cost, system-on-panel (SOP) integrated with functional devices on the LCD panel, such as controller [5], and memory [6], has been proposed for display technology development. However, high-power dissipation in the TFT-LCD panel is still a problem for the application in portable information devices. Therefore, reducing power consumption is required to maintain a long battery life for portable electronic applications. It is well known that the non-volatile memory is widely utilized for data storage in portable electronics system due to its properties of low-power consumption and nonvolatility. The conventional nonvolatile memory with floating-gate structure faces a limit due to its complicated fabrication process for integration on a display panel. As a result, the SONOS-type memory has become a promising candidate for SOP application due to its full process compatibility. However, achieving fast programming/erasing efficiency and long retention at the same time remains a challenge for SONOS devices.

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doi:10.1016/j.surfcoat.2007.07.111

Recently, various approaches have been proposed for improving the SONOS performance and reliability by using dielectric engineering [7–9]. In addition, SONOS-type poly-Si TFT fabricated by sequential lateral solidified (SLS) method is also reported to improve the P/E efficiency by field-enhanced tunneling at Si protrusions regions [10]. However, the variation of the location of Si protrusions by laser recrystallization method may be still a concern. Based on our previous study [11], the poly-Si TFT with nanowire channels can exhibit good gate control due to its tri-gate structure. Besides, the nonvolatile nanocrystal memory with narrow channel width structure was demonstrated to improve the P/E efficiency [12]. Thus, in this paper, the poly-Si TFT combined with nonvolatile SONOS memory and nanowire channels, named as NW SONOS-TFT, is proposed to obtain high performance transistor and P/E efficiency memory device.

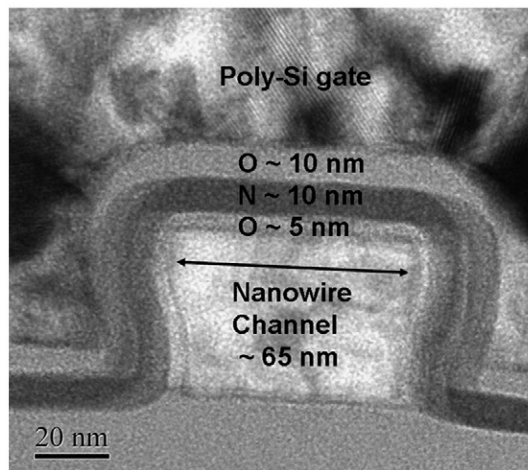


Fig. 2. Transmission electron microscopy of one of channels in the SONOS-TFT with the NW structure.

2. Experiment

In this study, the SONOS-TFT with a gate length of 5 μm and ten strips of 65-nm nanowire channel (NW) was fabricated. The standard device with a single channel structure with $W=1$ μm (STD) was also prepared for comparison. Fig. 1(a) presents the top view of the device with the NW structure. The schematic plots of TFT with an oxide–nitride–oxide (ONO) is shown in Fig. 1(b).

The devices were fabricated on 6-in. silicon wafer with a 400-nm thick layer of thermal oxide layer substrate. A thin amorphous silicon (a-Si) with a thickness of 50-nm was deposited by low-pressure chemical vapor deposition (LPCVD) at 550 °C. The deposited a-Si layer was recrystallized by solid-phase crystallization (SPC) at 600 °C for 24 h in a N_2 ambient. After electron beam (ebeam) direct writing and reactive ion etching (RIE), the active region was formed. Then, the 25-nm-thick ONO multilayer gate dielectric of the bottom tetra-ethyl-ortho-silicate (TEOS) oxide (5-nm)/silicon nitride (10-nm)/top TEOS oxide (10-nm) were deposited by LPCVD. Subsequently, a 150-nm-thick in-situ n^+ doped poly-Si layer was deposited and transferred to a gate electrode. After gate formation, self-aligned phosphorous

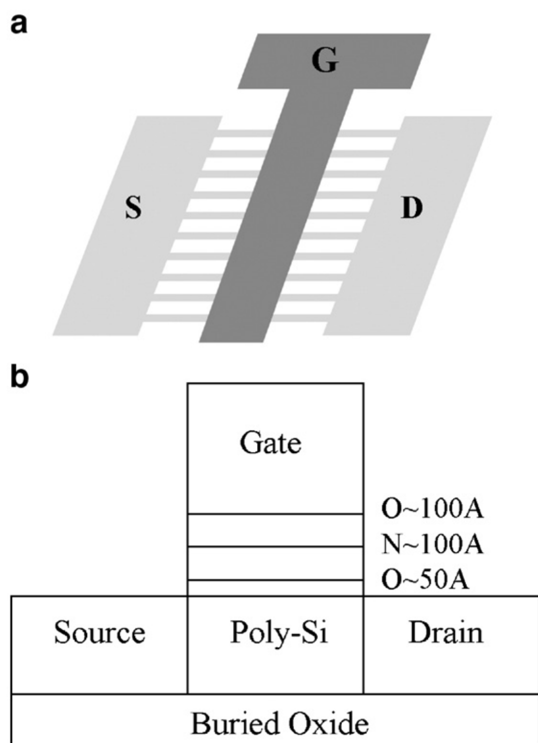
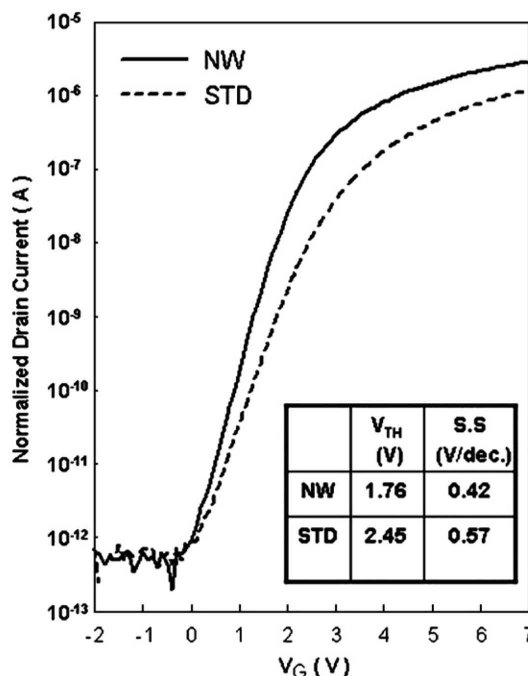


Fig. 1. (a) Schematic plots of poly-Si TFT with multiple nanowire channels structure, and (b) Cross-section view of device with oxide–nitride–oxide gate dielectric.



	V_{TH} (V)	S.S (V/dec.)
NW	1.76	0.42
STD	2.45	0.57

Fig. 3. Typical I_D–V_G characteristics of the STD and the NW SONOS-TFTs. The parameters of threshold voltage and subthreshold swing are extracted in the insert tables.

implantation was performed with a dose of 5×10^{15} cm^{-2} and the dopant was activated by rapid thermal annealing. Then, a 200-nm TEOS oxide layer was deposited by LPCVD as the passivation layer. Next, the 5×5 μm^2 contact holes were defined and Al metallization was performed. Finally, the devices were sintered at 400 °C in nitrogen ambient for 30 min.

3. Results and discussion

Fig. 2 shows the TEM photography of a single nanowire channel cross-section. It is clearly observed that the nanowire channel is surrounded by the control gate to form the tri-gate structure. The physical channel width of NW SONOS-TFT is also confirmed 65 nm and the thickness of O/N/O are 5 nm/10 nm/10 nm, respectively. Fig. 3 presents the normalized I_D–V_G curves of the STD and the proposed NW SONOS-TFTs. The electrical parameters are also extracted in the insert tables. Comparing the STD device, the NW device has superior electrical performance, such as the higher on-current, smaller threshold voltage (V_{th}) and subthreshold swing (S.S). Due to the increase of the effective channel width and the enhancement of the control of the channel region by the tri-gate structure, the drive current and V_{th} can be improved in NW SONOS-TFT. Additionally, the drain current at the corner region turns on earlier than that at the surface of the channel due to the crowding of the gate fringing field at the corner edges [13], the additional corner current can increase the drain current as the corner numbers increasing. Therefore, the pronounced enhancement of device with the NW structure is attributed mainly to the good gate control by the tri-gate structure and the larger electrical field induced by its corner effect.

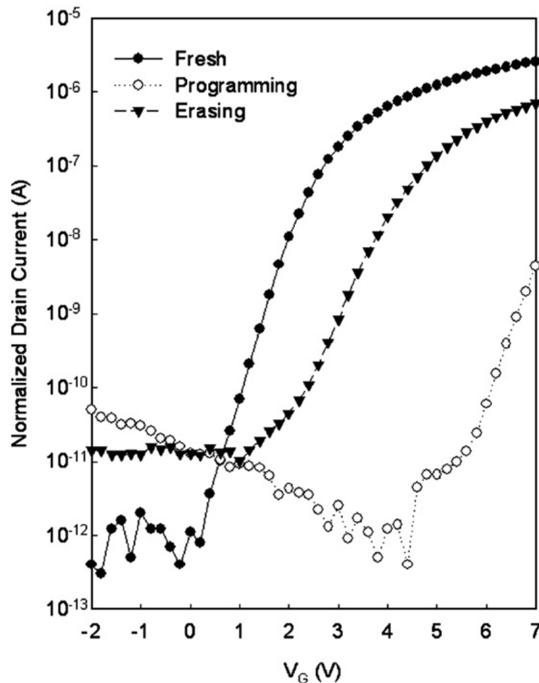


Fig. 4. The I_D–V_G curves of device before memory operation (Fresh) and after the programming/erasing operations.

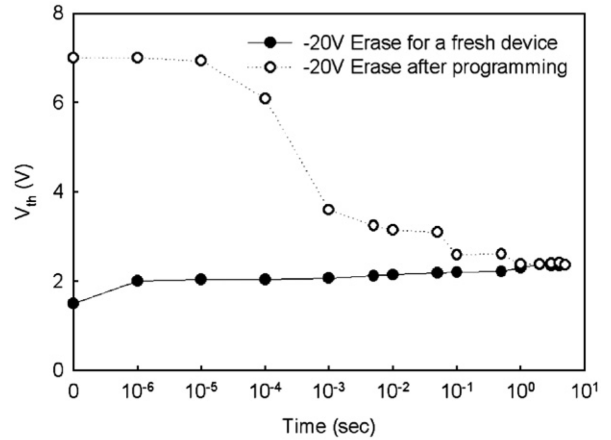


Fig. 5. Self-convergent characteristic of NW SONOS-TFT with a −20 V erasing bias.

In addition, the SONOS-TFT also can be used as a nonvolatile memory device under adequate gate voltage operation. In this work, the SONOS-TFT memories are programmed and erased by tunneling mechanism. Fig. 4 presents the I_D–V_G curves of device before memory operation (Fresh) and after the programming/erasing operations. During programming operation, electrons

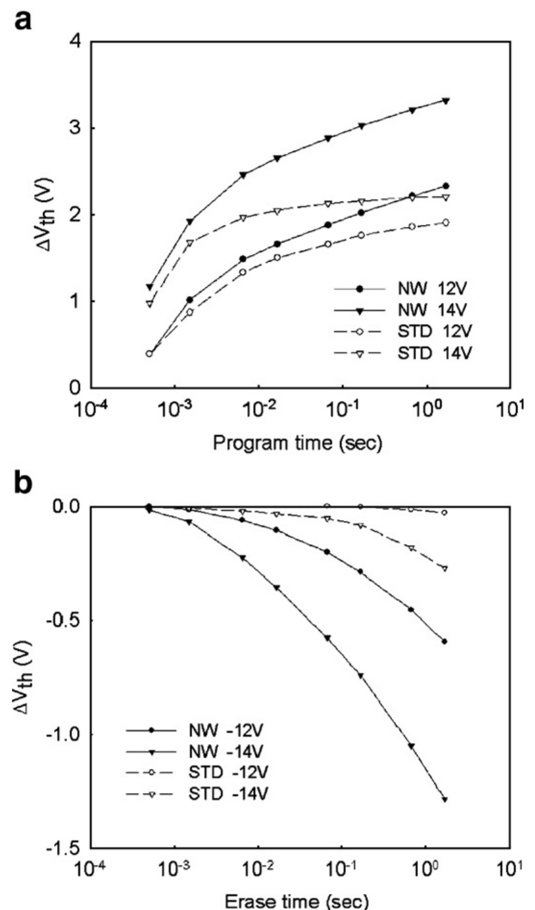


Fig. 6. (a) Programming characteristics, and (b) erasing characteristics of memory devices for NW and standard structures.

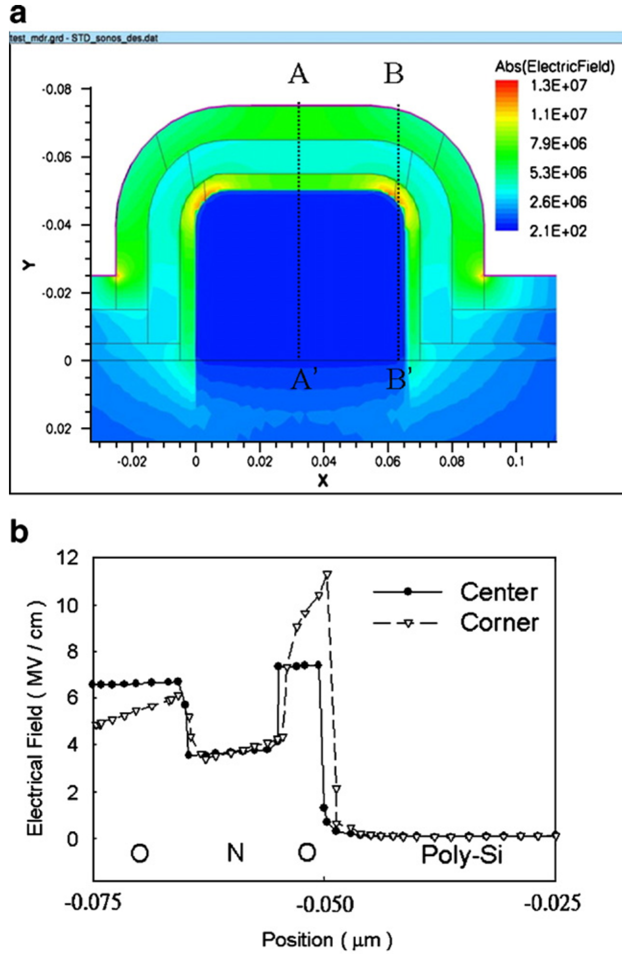


Fig. 7. Simulation results of (a) the electrical field contour plot of the nanowire with a gate bias of 14 V, and (b) the electrical fields in ONO gate dielectric at center and corner regions.

injection form inverted substrate into the nitride layer and be captured by the traps in the nitride layer to increase V_{th}. If the programming time is long enough, the V_{th} will saturate, and the saturated V_{th} value is bias-dependent [14]. Oppositely, during erasing operation, the captured electrons inject back to substrate form the nitride layer. However, the erased V_{th} will also saturate, and the saturated V_{th} value is determined by the charge balance between the gate injection into the ONO layer and the de-trapping out of the ONO layer [15]. Therefore, when the SONOS-TFT is functioned as a nonvolatile memory, it has a new reset state threshold voltage different from that in fresh device.

In order to demonstrate the reset state threshold voltage caused by dynamic balance of gate injection and electron de-trapping, the fresh device was erased with a negative bias without any programming operation. As shown in Fig. 5, the threshold voltage rises as the erasing time increases and saturates in the end. Comparing the erasing characteristic of a programmed device with the same negative bias, it is observed that the saturated threshold voltages are self-convergent. Hence, the self-convergent property should be considered as the SONOS-TFT is functioned as a memory device.

Fig. 6(a) and (b) shows the programming and erasing characteristics of NW and standard devices. It can be seen that the memory device with multiple nanowire channels has the superior program/erase (P/E) efficiency and larger memory window shift than STD device. Especially, for the erasing characteristic, it shows that the erasing speed is very slow and the memory window is neatly no shift even at a gate voltage of −12 V in the standard device. The memory characteristics for NW SONOS-TFT improved because the corner effect induced large electrical field at the corners can greatly enhance the programming and erasing performance. Therefore, the P/E efficiency is really improved by the multiple nanowire channels structure.

To verify the hypothesis, we performed the simulations of electrical field for single nanowire by ISE-TCAD simulator. Fig. 7(a) presents the contour plot of electrical field with a gate bias of 14 V. The 2-D simulation shows that maximum electrical field is concentrated near the corners obviously. Fig. 7(b) illustrates the electrical fields along the AA′ (center) and BB′ (corner) direction, receptively. It can be found that the maximum electrical

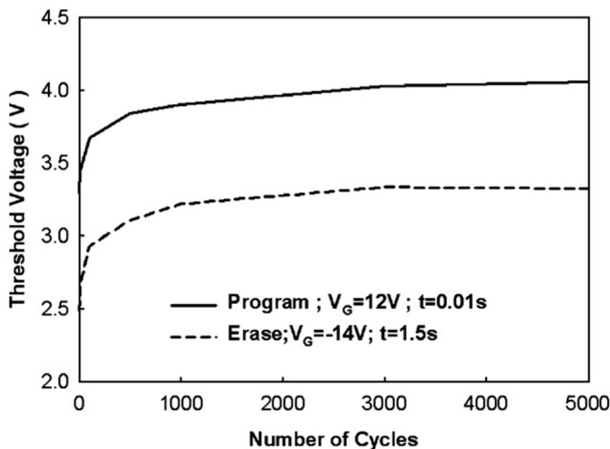


Fig. 8. Endurance characteristic of the NW SONOS-TFT. Memory window remains 0.8v after 10^5 P/E cycles without much degradation.

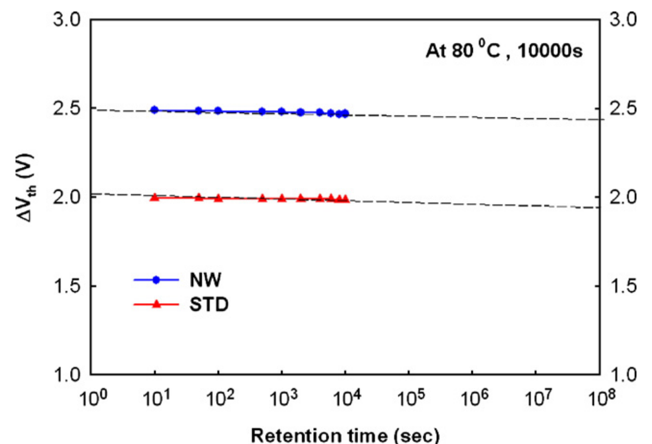


Fig. 9. Data retention characteristics of STD and NW devices at 80 °C. Memory window of both devices are not closure after 10 years.

field is about 11 MV/cm at the corner and 7.5 MV/cm at the center near the SiO_2/poly-Si interface. Thus the tunneling current through the tunneling oxide is larger at the corners than at the center of nanowire. Similarly, the erasing characteristic also can be improved by the corner effect induced large electrical field during erasing operation. Therefore, the pronounced enhancement of device with the NW structure is attributed to the large number of corners and their corner effect.

Fig. 8 shows the retention characteristics for NW and standard SONOS-TFTs at 80 °C. The devices are programmed and then measured at raised temperature. The results indicate that both devices exhibit large memory windows and neatly no degradation at a 10-year retention time tested at 80 °C. The endurance characteristic of NW SONOS-TFT with 12 V 10 ms and −14 V 1.5 s stress is shown in Fig. 9. It can be seen that the programmed/erased threshold voltage both increase as the number of cycles increases at the beginning and saturates to retain a constant memory window. The increase in threshold voltages could be due to the programming and erasing efficiencies are not compatible. However, the memory window is not closure obviously and the memory window can remain a 0.8 V after 5×10^3 P/E cycles.

4. Conclusions

A novel poly-Si TFT combined with nonvolatile SONOS memory and nanowire structure is demonstrated in this study. The SONOS-TFT can be functioned as a transistor or a nonvolatile memory at the same time. Due to the tri-gate structure and additional corner current induced by corner effect, the NW SONOS-TFT has the superior electrical characteristics than a standard device. Under an adequate gate bias operations, the proposed device exhibits superior memory characteristics with high program/erase efficiency. The simulation of electrical field results verified that the enhancement of P/E efficiency in NW SONOS-TFT is mainly attributed to the large number of corners and their corner effect. In addition, the good retention and endurance are also obtained in this device. The fabrication of SONOS-TFTs with nanowire channels is quite easy and involves no additional processes. Such a SONOS-TFT is very promising to be used for application in the future system-on-panel display.

Acknowledgment

This work was performed at the National Nano Device Laboratory and was supported by the National Science Council of the Republic of China under Contract Nos. NSC-96-2120-M-110-001. Also, this work was partially supported by the MOEA Technology Development for Academia Project # 95-EC-17-A-07-S1-046 and MOE ATU Program #95W803.

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