by a factor of 160. The modified amplifier needs 10 μs for each step compared to 1.66 ms when the conventional class-A amplifier is used. So low power dissipation and high driving capability can be met by "adaptive biasing with differential feedback." Additionally it is shown that the adaptive biasing technique given by Degrauwe *et al.* works excellently and opens a wide range of applications in battery-supplied devices.

V. Summary

A one-stage CMOS operational amplifier with dynamic biasing has been presented. The basis for this amplifier was a concept given by Degrauwe *et al.* [3]. This concept has been modified to achieve true rail-to-rail common-mode range over the full supply voltage range. Simulation and measurements are in good correlation and show the expected results, especially in the critical operating area.

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Design Techniques for High-Frequency CMOS Switched-Capacitor Filters Using Non-Op-Amp-Based Unity-Gain Amplifiers

Chung-Yu Wu, Ping-Hsing Lu, and Ming-Kai Tsai

Abstract—**A fully differential non-op-amp-based unity-gain amplifier (UGA) is proposed, whose 3-dB frequency can be as high as 250 MHz in 3.5-μm p-well CMOS technology. Suitable predistortions can be introduced under the aid of CAD tools to reduce the parasitic effects. Experimental results have successfully proven the capability of the proposed structures in the realization of high-frequency switched-capacitor filters over the megahertz range. Filter accuracy can be further enhanced by using the tunable-gain UGA, which enables tuning on filter parameters.**

I. Introduction

SINCE a unity-gain amplifier (UGA) can work over a wider bandwidth as compared to a conventional op amp, high-frequency switched-capacitor filters using unity-gain amplifiers have been explored in recent years [1]–[3]. However, all UGA's used in these SC filters are high-gain op amps with unity-gain feedback, called unity-gain buffers (UGB's). Thus the frequency response of such filters is still degraded by the unity-gain frequency and settling behavior of the op amps. Moreover, the accuracies of these filter responses are degraded by parasitic capacitances.

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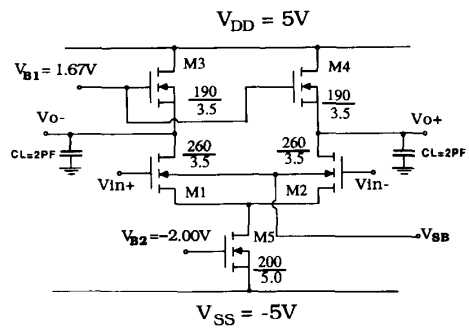


Fig. 1. The fully differential HF UGA with tunable gain by varying the substrate bias of the input coupled NMOS transistor pair.

The purpose of this work is to develop a new design concept for high-frequency SC filters which uses balanced non-op-amp type UGA's with tunable gain to replace conventional op-amp-based UGB's. The proposed UGA has a normal gain of unity, but it has a greater bandwidth, better settling behavior, smaller chip area, and less transistors than an op-amp-based UGB. The new UGA also has a fully differential balanced configuration that provides high design versatility as well as high immunity to clock-feedthrough noise and power-supply variations [4], [5]. The balanced configuration and the proper predistortion by the CAD tools can reduce the error due to linear parasitic capacitances. The residual error and the error due to nonlinear parasitic capacitances and process variations can be further compensated by tuning the gain of

the UGA. It is feasible, therefore, to use a simple UGA in the design of HF SCF's with negligible parasitic errors.

II. Fully Differential HF Unity-Gain Amplifier (UGA)

Fig. 1 shows the proposed fully differential amplifier with unity gain. This is a source-coupled input stage with enhancement-mode NMOS transistors as load devices. The differential-mode gain can be expressed as

$$A_{dm} = -\frac{g_{mi}}{g_{ml}+g_{dl}+g_{di}} \cong -\frac{2\sqrt{\left(\frac{W}{L}\right)_i \cdot \frac{\mu_n C_0}{2} \cdot I_{Di} \cdot (1+\lambda V_{DSi})}}{g_{ml}+g_{dl}+g_{di}} \quad (1)$$

where $g_{ml}(g_{mi})$ is the transconductance of the load (input) NMOS, $g_{dl}(g_{di})$ is the output conductance of the load (input) NMOS, $(W/L)_i$ is the dimension ratio of the input NMOS, μ_n is the electron surface mobility, C_0 is the channel capacitance per unit area, I_{Di} is the drain current of the input NMOS, V_{DSi} is the drain–source voltage of the input NMOS, and λ is the equivalent Early-effect factor.

Once the bias current and the dimension ratio $(W/L)_i$ are determined, a fully differential UGA with negligible output offset can be obtained by pertinent selection of $(W/L)_l$ and V_{B1}. Moreover, the amplifier gain is insensitive to the variations of temperature and process. Simulations indicate that the amplifier gain only changes 0.15% as temperature changes from -65 to 125° C, whereas in the Monte Carlo analysis of the amplifier gain an under 10% variation of the threshold voltage of the transistors results in only a mean deviation of 0.011 dB and a sigma of 0.129 dB. Simulation results also indicate that the amplifier gain only changes $\pm 0.3\%$ and $\pm 0.5\%$, respectively, for a change of ± 0.1 V in V_{B1} and V_{B2}. Thus a simple biasing circuit could be used to generate V_{B1} and V_{B2} for the UGA.

The signal swing V_{sw} of the UGA is determined by the bias voltage V_{B1} as

$$V_{sw} = V_{GSl} - V_{T0l} \cong \sqrt{2} \cdot (V_{B1} - V_{T0l}) \quad (2)$$

where the V_{T0l} is the zero-bias threshold voltage of the load device. Since the signal swing is not full rail, the dynamic range is decreased due to harmonic distortion.

The proposed UGA has a tunable gain. The tuning can be done through the adjustment of the substrate bias V_{SB} of the source-coupled input pair. As V_{SB} becomes more negative, the threshold voltages of the input NMOS transistors M_1 and M_2 become larger. To keep the same drain current, the gate–source voltage of the input NMOS has to increase and thus the voltage at the coupled source node is lowered toward V_{SS}. Since the substrate bias and the drain current of the load NMOS M_3 and M_4 remain unchanged, the output voltage almost retains its original value and does not change with V_{SB}. This means that V_{DSi} is increased, which increases g_{mi} due to the equivalent Early effect, as may be seen from (1). This results in a slight gain increase as shown in Fig. 2, where the SPICE-simulated differential gain and the upper 3-dB frequency as a function of V_{SB} are shown. It can be seen that the gain A_{dm} changes quasi-linearly from 0.831 to 1.097 and the upper 3-dB frequency increases up to 262 MHz when V_{SB} changes from -0.9 to -5.0 V. This makes the tuning more effective than that in the conventional op-amp-based UGB whose gain is never greater than 1. When V_{SB} changes from -0.9 to -5.0 V, the dc output voltage V_{out} has only a negligible change of 13 mV. Similar to the tuning in a continuous-time filter [6], the tuning of V_{SB} can be performed automatically. This will be investigated in more detail in the future.

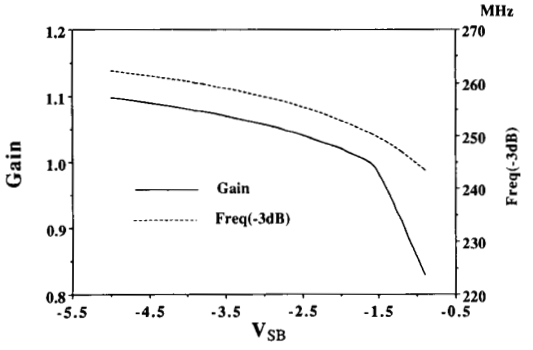


Fig. 2. The responses of the gain and the upper 3-dB frequency of the tunable-gain UGA versus the adjustable substrate bias of the input transistors.

Note that the above-described tuning technique is not applicable in an n-well CMOS process where all NMOS's lie on the same p-substrate. As the channel length is scaled down, the body effect is less significant due to charge sharing. This means that the same change of V_{SB} leads to a smaller increase of V_{DSi}. But this effect is somehow offset by the increase of λ for shorter channel length. Thus, tuning still could be achieved by changing g_{mi} in (1).

III. Fully Differential Bilinear SC Integrators

Fig. 3 shows the fully differential bilinear SC integrator using the proposed UGA. In this circuit, $C_1 = \alpha \cdot C$ is the sampling capacitor and $C_{22} = 1/2 \cdot (1-\alpha) \cdot C$ is the integrating capacitor. The floating integrating capacitor C_{22}, which also enhances the common-mode rejection, is derived from two integrating capacitors connected in series, each with the capacitance value $(1-\alpha)C$. Moreover, C_{p1} represents the top-plate parasitic capacitances of C_1 and other parasitic capacitances associated with switches and wires connected to that node, and C_{p2} represents the

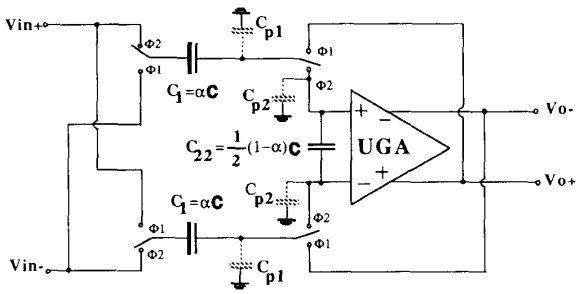


Fig. 3. The fully differential bilinear SC integrator.

input capacitance of the UGA and parasitic capacitances due to switches and interconnections. Because the input of a UGA is not at virtual ground, parasitic capacitances can substantially cause deviations in the normal network response.

Now, considering these parasitic capacitances and assuming that the gain is A ($A \cong 1$), we have

$$(V_0^+ - V_0^-) = A \cdot \left[\frac{C}{C + C_{p1} + C_{p2}}\right] \cdot \alpha \cdot \frac{(1+z^{-1})}{(1-z^{-1})} \cdot (V_{in}^+ - V_{in}^-). \quad (3)$$

If $A = 1$, $C_{p1} = 0$, and $C_{p2} = 0$, (3) becomes an ideal bilinear SC integrator. If only the linear parts of C_{p1} and C_{p2} are considered, these linear parasitic capacitances affect only the magnitude of the gain expression and do not contribute to any parasitic damping [2]. It is possible to reduce the linear parasitic effect by performing the predistortion on the integrating capacitor $C'_{22} = 1/2 \cdot [(1-\alpha) \cdot C - C_{p1} - C_{p2}]$. But this predistortion could not completely cancel the parasitic effect because of the inaccuracy in extracting C_{p1} and C_{p2} as well as the nonlinear parasitic capacitances from switches, which introduce intermodulation distortion. It is also seen from (3) that the coefficient of the transfer function is affected by the deviation of the UGA's gain, which may result from process variations or circuit operation at a higher frequency. The incomplete predistortion of the linear parasitic capacitances and the gain deviation after fabrication can be further compensated by using the gain tuning technique mentioned in Section II.

IV. Experimental Results and Discussions

The experimental chip was fabricated by 3.5-μm double-poly p-well CMOS technology. A photomicrograph of the test chip is shown in Fig. 4. In designing the chip, suitable predistortion was performed.

A. Fully Differential UGA

The simulated and experimental results of the simple unity-gain amplifier shown in Fig. 1 are listed in Table I.

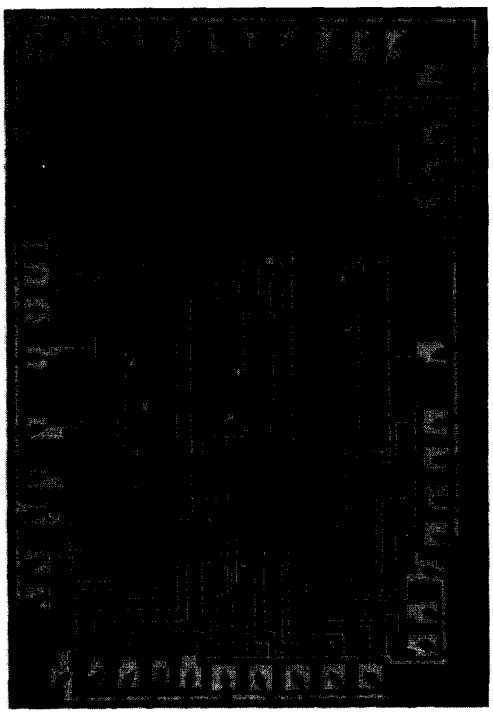


Fig. 4. Photomicrograph of the experimental chip.

With a 2-pF capacitance loading in the UGA, a simulated upper 3-dB frequency higher than 250 MHz and a slew rate faster than 400 V/μs can be obtained. According to the simulation results, both characteristics can be improved with MOS channel length scaling. The price paid for such a high-frequency response and excellent settling behavior is larger power consumption and smaller signal swing. Using the UGA in the filter design, the maximum speed would be limited by the switches.

Since the output drivers have not yet been embedded at the output nodes of the fabricated UGA, it has to drive a heavy capacitance load of approximately 14.9 pF. Thus the measured upper 3-dB frequency is only 47.7 MHz, but it is consistent with the simulated value of 45.4 MHz.

B. Bilinear SC Biquad

An SC high-Q bandpass bilinear biquad with a center frequency f_0 of 1 MHz, a quality factor Q of 10, a passband gain A of 1, and a sampling frequency f_s of 15.9 MHz was designed by using the integrator of Fig. 3 and the UGA of Fig. 1. The measured frequency responses (both gain and phase) of the fabricated filter are shown in Fig. 5. The measured performance characteristics of the fabricated SC bandpass biquad are summarized in Table II.

Fig. 6 shows the transmission characteristics (upper trace B) and the noise spectrum with grounded inputs

TABLE I
THE SPICE-SIMULATED AND THE MEASURED CHARACTERISTICS OF THE UGA ($V_{DD} = -V_{SS} = 5$ V)

	Simulated Values (SPICE) ($C_L = 2$ pF)	Experimental Values ($C_{Leff} \approx 14.9$ pF)
Passband Gain	0.0032 dB ($A = 1.00035$)	0.06 dB ($A = 1.00693$)
−3-dB Bandwidth	252 MHz (45.4 MHz$^{\Theta}$)	47.7 MHz
CMRR (Freq. = 10 kHz)	29.6 dB*	49.2 dB
PSRR+ (Freq. = 10 kHz)	24.3 dB*	30 dB
PSRR− (Freq. = 10 kHz)	0.63 dB*	20 dB
Signal Swing	1.5 $V_{p\text{-}p}$	1.3 $V_{p\text{-}p}$
Slew Rate*	$+751/-438$ V/μs	$+101/-78$ V/μs
Settling Time (0.1%, ±0.5 V)	7.3 ns*	N/A
Output Offset	0.0033 V	0.023 V
Power Dissipation	50 mW	52 mW
Chip Area		0.076 mm^2

*Data obtained from a single output node.
$^{\Theta}$Simulation with $C_L = 14.9$ pF for comparison.

TABLE II
SIMULATED AND MEASURED RESULTS OF THE BILINEAR SC HIGH-Q BANDPASS BIQUAD ($V_{DD} = -V_{SS} = 5$ V)

	Specifications	Simulated Values (SWITCAP)	Experimental Values
Center Frequency	1 MHz	1 MHz	932.5 kHz
−3-dB Bandwidth	100 kHz	96 kHz	88.2 kHz
Quality Factor Q	10	10.41	10.57
Passband Gain	0dB	−0.056 dB	−0.236 dB
Clock Frequency		15.91 MHz	15.91 MHz
Output In-band Noise (for −10-dB BW: from 800 kHz to 1.07 MHz)			≤ 181 μV_{rms}
Dynamic Range for 1% IM for 3%IM			> 58 dB > 61 dB
CMRR (F = center freq.)			36 dB
PSRR+ (F = center freq.)			30 dB
PSRR− (F = center freq.)			20 dB
Power Dissipation			110 mW
Area			0.51 mm^2

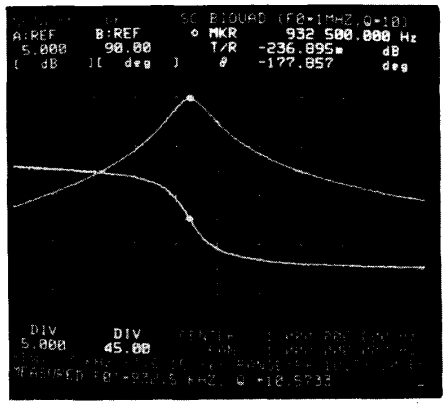


Fig. 5. The measured frequency responses (both gain and phase) of the fabricated UGA-based SC biquad.

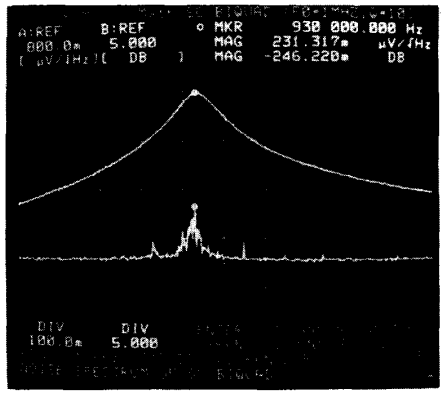
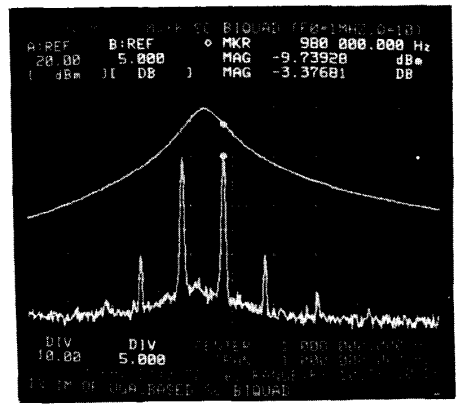
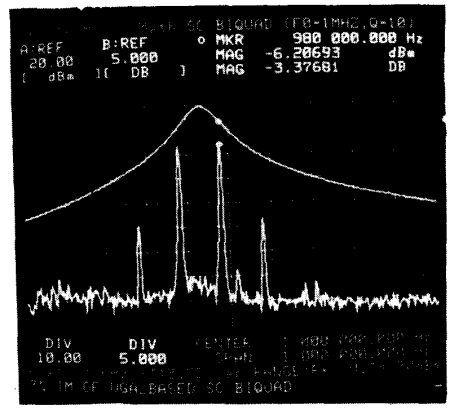


Fig. 6. Noise characteristics (lower trace) of the fabricated SC biquad and the transmission characteristics (upper trace) for reference.



(a)



(b)

Fig. 7. The intermodulation measurement at a single-ended output node of the SC biquad: (a) 1% IM, and (b) 3% IM.

(lower trace A). For the -10-dB bandwidth from 800 kHz to 1.06 MHz, the total output in-band noise is below 181 μV_{rms}. The 1% (3%) intermodulation measured at a single-ended output node is shown in Fig. 7(a) (Fig. 7(b)). It is seen that the equivalent maximum output signal is 150 mV_{rms} (220 mV_{rms}) and the dynamic range is 58 dB (61 dB). The high intermodulation may stem from the unbalanced measurement at a single-ended output node and the imperfect settling of the SC integrator without output driver.

The shift of the center frequency in the fabricated SC biquad is about -6.75% as may be seen from Fig. 5 or Table II. This small shift occurs even if the predistortion is performed on the chip layout. Thus the shift may result from process variations, incomplete predistortion, asymmetrical layout, and nonlinear parasitic capacitances.

If there exists a little deviation in amplifiers' gains and the unmatched errors on the capacitance ratios after fabrication, the deviated center frequency Ω_0', quality factor Q', and passband gain A' can be derived as functions of the actual deviated gain A_1' and A_2' and the

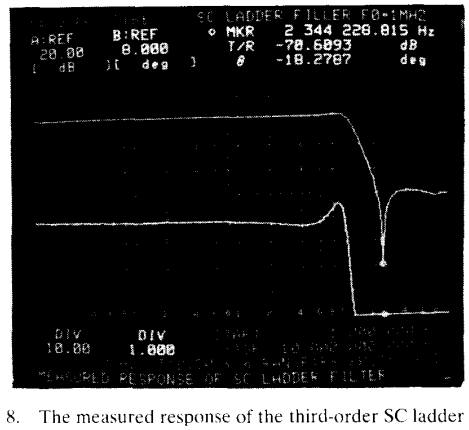


Fig. 8. The measured response of the third-order SC ladder filter.

TABLE III
SIMULATED AND MEASURED RESULTS OF THE BILINEAR SC LADDER LOW-PASS FILTER ($V_{DD} = -V_{SS} = 5$ V)

	Specifications	Simulated Values (SWITCAP)	Experimental Values
Passband Frequency	1 MHz	1.0105 MHz	1.034 MHz
Passband Ripple	0.177 dB	0.162 dB	0.81 dB
Stopband Frequency	2.281 MHz	2.171 MHz	2.065 MHz
Stopband Attenuation	> 30.41 dB	30.91 dB	31.87 dB
Passband Gain Peak		0 dB	2.57 dB
Transmission Zero Atten.		55.25 dB	59.7 dB
Clock Frequency		21.1 MHz	21.1 MHz
Max. Signal Level (THD < 1%)			0.45 $V^*_{p\text{-}p}$
Output In-band Noise (from 1 kHz to 1 MHz)			$\leq 122\ \mu V_{rms}$
Dynamic Range			> 62 dB
CMRR (Freq. = 10 kHz)			70 dB
PSRR+ (Freq. = 10 kHz)			36 dB
PSRR− (Freq. = 10 kHz)			37 dB
Power Dissipation			165 mW
Area			1.01 mm^2

*Doubling the signal level at a single output node for a single (unbalanced) input signal.

deviated capacitance ratios α'_1, α'_2, α'_3, and β'_1:

$$\Omega'_0 = \frac{2}{T}\sqrt{A'_1 \cdot A'_2 \cdot \alpha'_3 \cdot \beta'_1} \tag{4}$$

$$Q' = \frac{1}{\alpha'_2}\sqrt{\frac{\alpha'_3}{A'_1 \cdot A'_2 \cdot \beta'_1}} \tag{5}$$

$$A'(f_0) = \frac{-\alpha'_1}{\alpha'_2}. \tag{6}$$

It can be realized that the errors in the filter response due to gain and capacitance-ratio deviations can be compensated by tuning the amplifiers' gains A'_1 and A'_2 if the tunable UGA's mentioned in Section II are used. Since the gains A'_1 and A'_2 could be tuned from +9.7% to −16.9%, the tunable range of Ω'_0 and Q' is in the same range as may be realized from (4) and (5). The tuning could cover the above-mentioned −6.75% shift in the center frequency. Note that the tuning does not change the passband gain as in (6).

C. SC Ladder Filter

A HF three-order elliptic SC bilinear ladder filter with a pass frequency f_p of 1 MHz, a stop frequency f_S of 2.281 MHz, a passband attenuation A_{max} of 0.177 dB, and a stopband attenuation A_{min} of 30.41 dB was designed by the UGA and the bilinear integrator. The measured frequency response of the fabricated filter is shown in Fig. 8. Note that the sharp attenuation in the stopband indicates the effect of the transmission zero. However, the lower trace B indicates that the passband peak is 2.57 dB and the passband ripple is 0.81 dB. The gain deviation is mainly caused by the deviated capacitance ratios due to process variation or incomplete predistortion, as may be seen in (6). The higher ripple appearing nearly at the passband edge is mostly due to the degraded frequency response of the third UGA A_3, which must drive heavy output bounding-pad capacitances because there is no output driver embedded. The

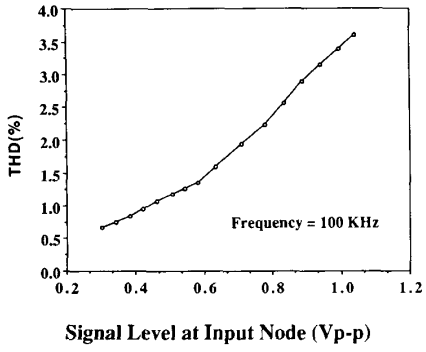


Fig. 9. The measured THD of the fabricated SC ladder filter.

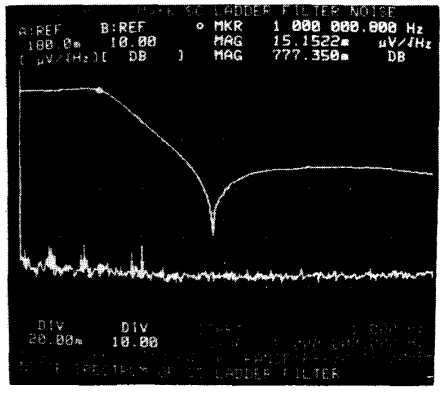


Fig. 10. Noise characteristics (lower trace) of the fabricated SC ladder filter and the transmission characteristics (upper trace) for reference.

measured performance parameters of the fabricated low-pass filter are summarized in Table III.

The measured total harmonic distortion (THD) at a single-ended output node for a single (unbalanced) input signal is shown in Fig. 9, which strays below 1% up to only 0.6 V_{p-p}. This phenomenon might result from the smaller signal swing of the UGA and the single-ended measurement. If the THD could be measured in the balanced output ports for a balanced input, its value would be much smaller than that measured at a single-ended node since the even-order harmonic distortions could be effectively eliminated.

The noise spectrum (lower trace B) obtained by grounding the filter inputs, compared to the transmission characteristic (upper trace A), is shown in Fig. 10 The total in-band noise including the signal feedthrough (from 1 kHz to 1 MHz) is below 122 μV_{rms}. The maximum dynamic range is still over 62 dB.

V. Conclusions

A fully differential simple HF UGA with tunable gain is proposed and applied to the design of HF bilinear SC circuits. The HF bilinear SC filters designed by the proposed simple non-op-amp-based UGA's were fabricated in 3.5-μm CMOS technology. It is shown from the measured results that the filtering can be performed successfully over the megahertz range with a reasonable accuracy before tuning.

Acknowledgment

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