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Formation of germanium nanocrystals by rapid thermal oxidizing SiGeO layer for nonvolatile memory application

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Abstract

A new method to fabricate Ge nanocrystals by rapid thermal oxidizing SiGeO layer for nonvolatile memory application was investigated in this study. The oxidation process nucleated the Ge nanocrystals embedded in the dielectric layer was clearly observed by transmission electron microscope analysis. Moreover, an over-oxidation phenomenon for the formation of GeO_2 in this work was found at higher temperature oxidation according to the X-ray photoelectron spectroscopy analysis. The obvious memory window was found in the capacitance–voltage hysteresis curve, and the program efficiency of holes was superior to electrons due to the electronic affinity of GeO_2 smaller than silicon substrate for a structure of Ge nanocrystals surrounded with GeO_2 layer. Furthermore, the Ge nanocrystals surrounded with GeO_2 layer structure has good retention time and endurance.

Keywords: Germanium nanocrystal; Germanium oxide; Rapid temperature oxidation; Nonvolatile memory

1. Introduction

In the past few years, the portable electronic products have been widely applied, such as digital cameras, notebook computers, mp3 walkmans, intelligent IC card, and USB Flash. These electronic products play an important role in the Digital Age and they are all fabricated based on conventional floating gate (FG) memory. Nevertheless, all of the charges stored in the FG will leak into the substrate if there is a leakage path in the tunnel oxide in the conventional FG memory. Hence, some novel structures of memory using discrete charge storage nodes have been attracted for the promising candidates to replace conventional FG memory [1,2]. Nonvolatile memory (NVM) devices with nanocrystals are considered as a possible solution for the next generation of nonvolatile memory devices, due to their high density, good data retention/endurance, low power consumption, and low voltage operation [3].

The semiconductor nanocrystal NVM has been widely investigated in recent years, such as silicon (Si) nanocrystal, germanium (Ge) nanocrystal and Zine–Oxide (ZnO) nanocrystal [3–5]. Germanium nanocrystal has better charge storage capacity than silicon nanocrystal and Zine–Oxide nanocrystal due to its smaller energy band gap (~0.6 eV) than silicon substrate. The self-assembling and direct growth of germanium nanocrystals embedded in SiO_2 layer has successfully been implemented [3,5]. However, a high temperature (~900–1000 °C) or long time (~30–60 min) oxidation process were widely used to nucleate Ge nanocrystal. [3,5,6]. Hence, the larger thermal budget is necessary for the formation of the Ge nanocrystals. In this study, a new method to fabricate Ge nanocrystals by rapid thermal oxidizing SiGeO thin film for NVM application was proposed. The SiGeO thin film was

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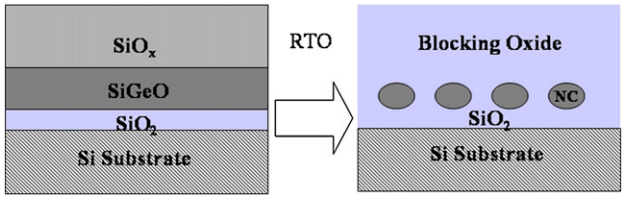

Fig. 1. Schematic cross sections of as deposition for a Si substrate/SiO_2/SiGeO thin film/SiO_x structure, and Ge nanocrystals embedded in the dielectric after RTO process.

deposited by co-sputtering method (Si and Ge target) in the oxygen environment. In addition, the process is ease and compatible with the current fabrication technology.

2. Experimental

First, the 6 inch *p*-type Si wafers were cleaned with a standard RCA process which this process can effectively remove native oxide, particles and metal ion from the surface of Si wafer [7], followed by a dry oxidation process in an atmospheric pressure chemical vapor deposition (APCVD) furnace to form a 5-nm-thick tunnel oxide. Subsequently, a 6-nm-thick SiGeO layer was deposited onto the tunnel oxide by co-sputtering Si and Ge target at the 80 W and 60 W DC power, respectively. Then, 20-nm-thick silicon oxide (SiO_x) layer deposited on SiGeO thin film in the same chamber by sputtering a Si target in the oxygen environment. A rapid thermal annealing in an oxygen ambiance (called RTO, oxygen ~ 80 sccm) at the condition of 600 °C and 900 °C for 60 s, were respectively executed to precipitate Ge nanocrystal embedded in oxidized SiGeO layer, as shown in Fig. 1. Furthermore, the sputtered SiO_x is further oxidized to enhance the quality serving as blocking oxide during RTO process. Al gate electrode was finally patterned to form metal/oxide/insulator/oxide/Si (MOIOS) structure. Transmission electron microscope (TEM) and X-ray photoelectron spectroscopy (XPS) were adopted for the micro-structure analysis and chemical states analysis. The electrical characteristics, including the capacitance–voltage (C–V) hysteresis, program holes/electrons efficiency, endurance and retention characteristics were also performed. The Capacitance–Voltage (C–V) characteristics were measured at high frequency 1 MHz by HP4284 Precision LCR Meter.

3. Results and discussion

Fig. 2 exhibits a cross-sectional TEM of as deposition for a Si substrate/tunnel oxide/SiGeO layer/SiO_x layer stacked structure. It is clearly observed that the SiGeO film is uniform and its thickness is about 8–9 nm due to oxygen incorporated with Si and Ge. After the RTO process at 600 °C for 60 s, the Ge nanocrystals are precipitated from SiGeO layer and the size of Ge nanocrystal is about 8–10 nm with the aerial density of 4.44×10^{11} cm^{-2} by HRTEM analysis, as shown in Fig. 3. To further investigate the chemical state of these nanocrystals, the XPS analysis was applied and corrected possible charging effect of the film which the binding energy was calibrated using the C 1s (284.6 eV) spectra of hydrocarbon. The inset of Fig. 3 indicates that the Ge and GeO_2 peaks are located at the 1217 eV and 1220 eV binding energy in the XPS analysis of Ge 2*p* spectra [8]. Base on the XPS analysis, it is considered that the Ge nanocrystals and GeO_2 are formed and embedded in the SiO_2 layer after RTO process.

In the RTO process, the Ge is nucleated in the Si-rich SiGeO layer and the silicon of SiGeO layer also can be formed completely SiO_2 phase. However, the exceeding oxidation causes a part of nucleated Ge nanocrystals to become the GeO_2 component which is not found in the as deposited layer (SiGeO). Hence, the nanocrystals are composed of Ge nanocrystal and GeO_2, which are both charge trapping center in previous investigations [3,9]. It can be further surmised by the HRTEM image of Fig. 3, which exhibits that the Ge nanocrystal is surrounded by dielectric layer for GeO_2.

Fig. 4 shows a cross-sectional TEM of SiGeO layer after the RTO process at 900 °C for 60 s and the XPS analysis of charge trapping layer indicates that only GeO_2 peak existed in the Ge 2*p* spectra, as shown in the inset of Fig. 4. Therefore, an over-oxidation phenomenon of Ge nanocrystal was to completely form GeO_2 nano-dot after higher temperature oxidation by XPS analysis. The Ge nanocrystals can be nucleated from the SiGeO film at lower temperature oxidation process (600 °C), as a result of negative Gibbs free energy of chemical bond of Si–O at room temperature [10]. In addition, the isolated Ge nanocrystals embedded in SiO_2 can be performed after lower temperature rapid oxidation process, which reduces the thermal budget of the thermal treatment. Moreover, it is considered that the formation of Ge nanocrystals and GeO_2 nano-dot are influenced by temperature for the SiGeO layer.

Fig. 5 exhibits the capacitance–voltage (C–V) characteristics for the stacked structure with oxidized SiGeO layer as charge trapping layer and control sample (without Ge in the charge trapping layer). The memory window is about 0.9 V under 5 V to (−5 V) bidirectional voltage sweep for RTO

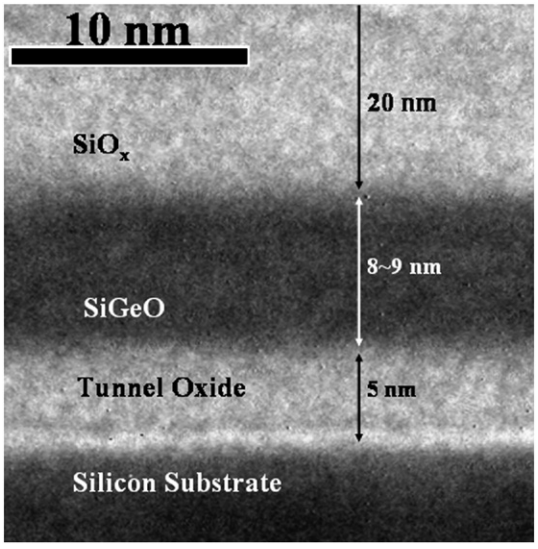

Fig. 2. The cross-sectional TEM images of as deposition. The SiGeO layer is about 8–9 nm.

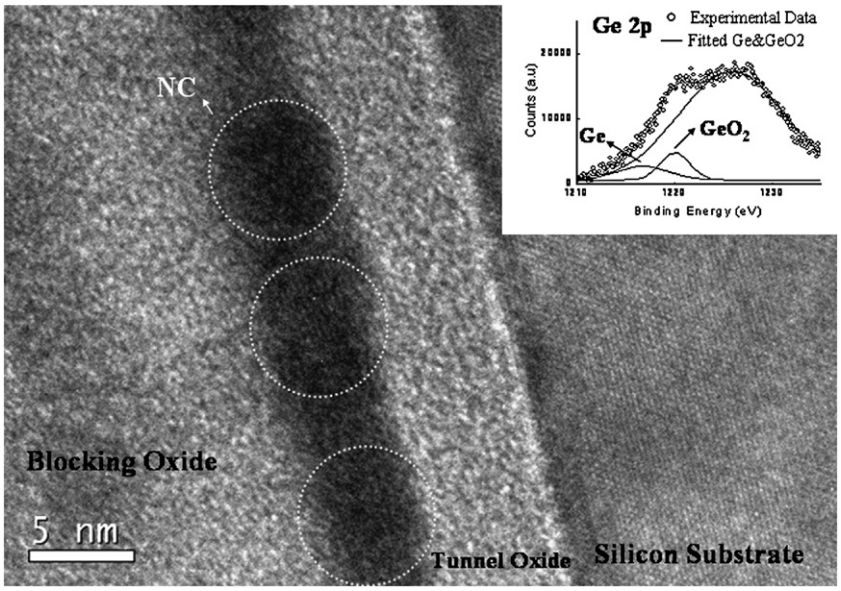

Fig. 3. The cross-sectional TEM images of Ge nanocrystals embedded in the dielectric after RTO process at 600 °C for 60 s. The size of nanocrystal and density is about 8–10 nm and 4.44×10^{11} cm^{-2}, respectively. The inset of Fig. 3 is the XPS analysis of Ge 2*p* form Ge nanocrystals. It indicates that it has Ge and GeO_2 at the 1217 eV and 1220 eV binding energy. Straight line and empty circles indicate experimental and fitting results, respectively.

condition of 600 °C (Ge&GeO_2). The memory window is also observed for RTO condition of 900 °C (GeO_2). Nevertheless, the control sample hasn't any memory capacity under ±5 gate voltage operation in Fig. 5. Hence, the memory effect for this MOIOS structure is dominated by ratio of Ge. The flat-band voltage shift is clearly observed under low voltage operation for the application of low power consumption nonvolatile memory devices. However, the device after RTO 600 °C treatment has better charge storage capability than the device after RTO 900 °C treatment, because of many existing trapping states between Ge and GeO_2. The low temperature RTO process in our research is more suitable for the application on the nonvolatile memory.

The program holes/electrons efficiency of the SiGeO layer after the RTO process at 600 °C for 60 s are shown in Fig. 6. It can't be found that flat-band voltage is shifted after different positive gate voltage stress in which the electrons should be injected into charge trapping layer, as shown in Fig. 6(a). However, it is found that the flat-band voltage is shifted increasing with stress duration for different negative gate voltage stress in which the holes should be injected into charge trapping layer from Si substrate, as shown in Fig. 6(b). Fig. 7 exhibits the schematic energy band diagram base on electronic

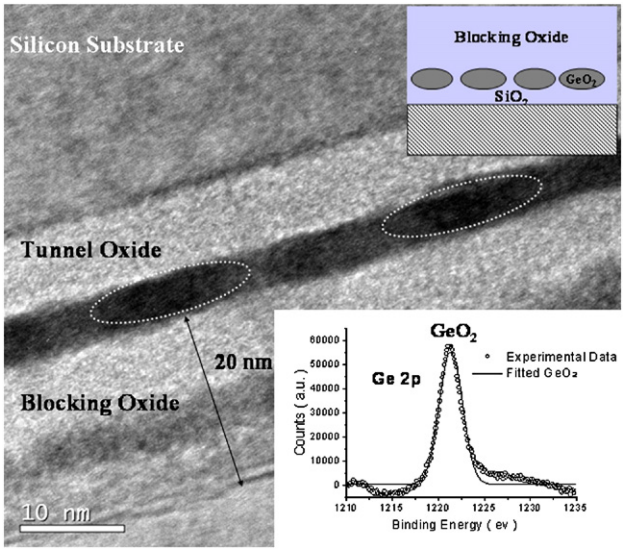

Fig. 4. The cross-sectional TEM images of GeO_2 nano-dot embedded in the dielectric after RTO process at 900 °C for 60 s. The inset of Fig. 4 is the XPS analysis of Ge 2*p* form Ge nanocrystals. It indicates that it has GeO_2 peak in the Ge 2*p* spectra. Straight line and empty circles indicate experimental and fitting results, respectively.

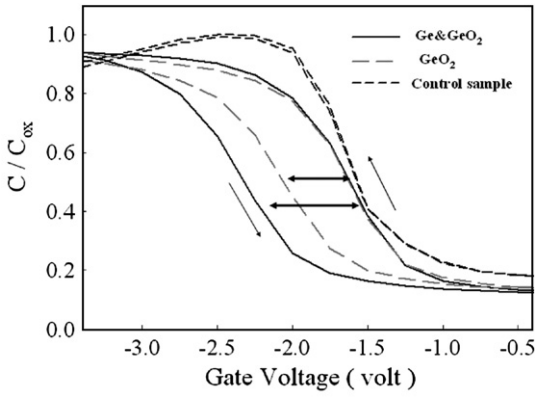

Fig. 5. The capacitance–voltage (C–V*)* hysteresis of the MOIOS structure after the bidirectional voltage sweeps from 5 V to (−5 V) and (−5 V) to 5 V. The memory window is about 0.9 V for RTO condition of 600 °C (Ge&GeO_2) and the memory window is about 0.5 V for RTO condition of 900 °C (GeO_2).

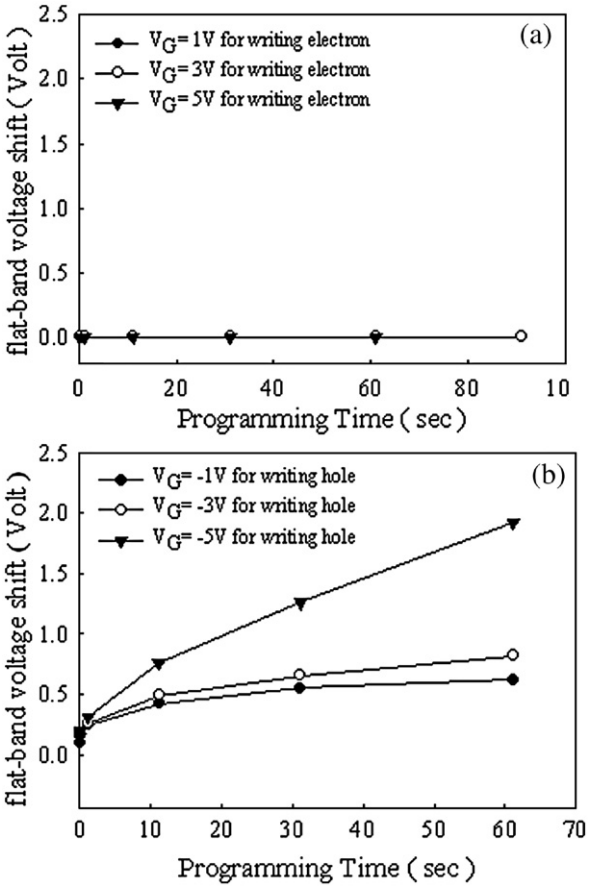

Fig. 6. The program electrons and holes efficiency of Ge nanocrystal surrounded with GeO_2 at different program Gate voltage and programming time.

affinity of material for Ge nanocrystal embedded in GeO_2 layer. The superior hole injection behavior to electron injection results from the lager band offset ($rE_C \sim 3.26$ eV) for GeO_2 to Si substrate in conduction band. The Ge nanocrystal is surrounded with GeO_2 and the band gap and electronic affinity of GeO_2 are about 5.9 eV and 0.75 eV [11]. In the present investigations, it is considered that the GeO_2 is pinned to SiO_2 resulting in higher

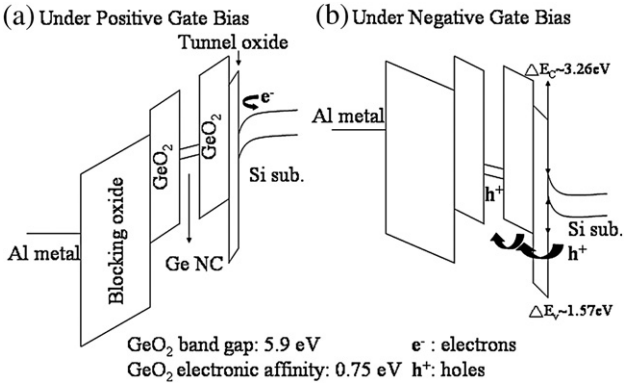

Fig. 7. A simple schematic energy band diagram is (a) under positive gate bias and (b) under negative gate bias, respectively. The energy gap of GeO_2 is about 5.9 eV. The conduction band offset and valence band offset of GeO_2 are about 3.26 eV and 1.57 eV.

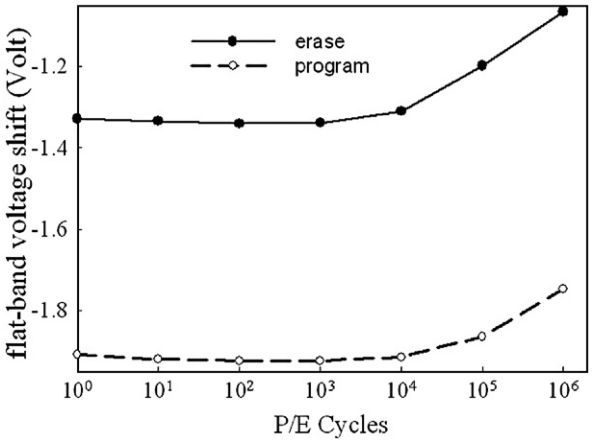

Fig. 8. The endurance of Ge nanocrystals embedded in the dielectric after RTO process by programming −5 V for 20 s and erasing 5 V for 20 s.

band offset for the conduction band of silicon substrate [11,12]. Hence, the electrons can't be injected to the conduction band of Ge nanocrystal under positive gate bias, as shown in Fig. 7(a). The holes are easier written into valence band of Ge nanocrystal as shown in Fig. 7(b); nevertheless, the direct tunneling mode needs more program time to obtain enough memory window which is defined "1" or "0" for holes. This problem can be solved by using a band-to-band tunneling-induced hot hole injection method (BBHH) for Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET) structure [13].

For the electrical reliability test, the endurance and charge retention characteristic were investigated in this study. The endurance and retention characteristics of the Ge nanocrystals surrounded with GeO_2 are shown in Figs. 8 and 9. The endurance is found that memory window can be maintained 0.6 V after 10^4 cycles under cycling the structure between −5 V for 20 s (write-holes injection to the Ge nanocrystals) and 5 V for 20 s (erase-holes injection from the nanocrystals); even so, both writing and erasing curve have a raised tendency to shift positive voltage after 10^4 cycles. The electron injection is not sensitive under the positive gate voltage operation in the above

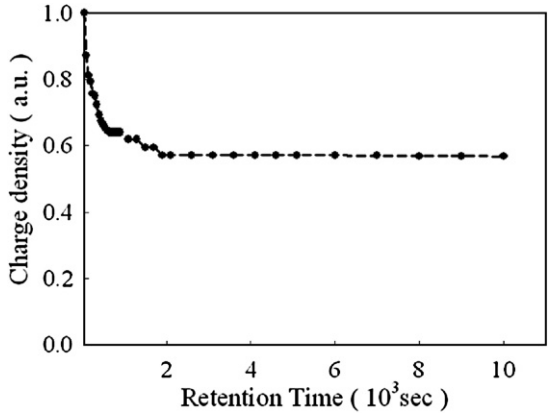

Fig. 9. The retention characteristics of Ge nanocrystals was used constant negative gate voltage stressing (−5 V) for 20 s. The device is only written holes into charge storage layer. The device is only written by using hole injection.

discussion. However, the flat-band voltage shift is found under positive bias after numerous cycles. It is considered that trap states are generated between tunnel oxide and Si substrate, resulting in some electrons stored in those trap states under channel inversion state [14]. Thus, all the threshold voltage shift are increased to 0.2 ~ 0.3 V after 10^6 cycles.

The retention characteristics were investigated at room temperature by using the constant negative gate voltage stressing (−5 V) for 20 s in which was obtained a memory window of 1.0 V, as shown in Fig. 9 and the charge density was estimated by *C-t (capacitance to time)* measurements [15]. It is clearly observed that the charge density decays rapidly with time leading to 40% charge loss before 2000 s. However, the stable charge storage can be conserved and the memory window also can be retained 0.7 V. In the previous research, the memory effect for nanocrystals embedded in dielectric is resulted from (1) interface states between the silicon substrate, (2) traps inside the dielectric layer, (3) nanocrystal confined state, and (4) interface states between nanocrystals and the surrounding dielectric [16–18]. The charge retention ability of the deep trap is better than shallow trap due to lower charge escaping probability for the deep trap. Hence, the rapid decay in the retention test is due to the charge stored in shallow trap states which is higher energy compared with silicon substrate leading to charges escaping to substrate [15,19,20].

4. Conclusion

In conclusion, the Ge nanocrystals surrounded with GeO_2 memory was fabricated by co-sputtering in the oxygen environment followed by a low temperature (at 600 °C for 60 s) RTO process. This structure exhibits obvious memory window of 0.9 V is observed after ±5 V voltage sweep due to the contribution of Ge nanocrystals and GeO_2 formation. The hole injection is only found under negative gate voltage stress due to the lager band offset for conduction band. However, the reduced memory effect is found for over-oxidation process which causes the Ge nanocrystal to become GeO_2 nanocrystal completely. In addition, the endurance and date retention of the Ge nanocrystal memory device can be maintained unto 10^4 cycles and 10^4 s. Furthermore, the process is ease and compatible with the current fabrication technology; it is promising for the application of memory design, and low power devices.

Acknowledgements

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References

[1] S. Tiwar, F. Rana, K. Chan, H. Hanafi, W. Chan, D. Buchanan, IEDM Tech. Dig. (1995) 521.
[2] P. Pavan, R. Bez, P. Olivo, E. Zanoni, Proc. IEEE. 85 (1997) 1248.
[3] C.H. Tu, T.C. Chang, P.T. Liu, H.C. Liu, C.C. Tsai, L.T. Chang, T.Y. Tseng, S.M. Sze, C.Y. Chang, Appl. Phys. Lett. 89 (2006) 052112.
[4] J.H. Jung, J.Y. Jin, I. Lee, T.W. Kim, H.G. Roh, Y.H. Kim, Appl. Phys. Lett. 88 (2006) 112107.
[5] P. Normand, D. Tsoukalas, K. Beltsios, Appl. Phys. Lett. 80 (2002) 15.
[6] T.C. Chang, S.T. Yan, P.T. Liu, C.W. Chen, S.H. Lin, S.M. Sze, Electrochem. Solid-State Lett. 7 (2004) G17.
[7] W.A. Cady, M. Varadarajan, J. Electrochem. Soc. 143 (1996) 6.
[8] W.K. Choi, Y.W. Ho, S.P. Ng, V. Ng, J. Appl. Phys. 89 (2001) 2168.
[9] T.C. Chang, S.T. Yan, P.T. Liu, C.W. Chen, S.H. Lin, S.M. Sze, Appl. Phys. Lett. 84 (2004) 2581.
[10] I. Barin, 3rd ed., Thermochemical Data of Pure Substances, vols. I and II, VCH, Weinheim, 1995.
[11] V.V. Afanas’ev, A. Stesemans, Appl. Phys. Lett. 84 (2004) 2319.
[12] T.H. Hou, U. Ganguly, E.C. Kan, IEEE Electron Device Lett. 28 (2007) 2.
[13] S.I. Hsieh, H.T. Chen, Y.C. Chen, C.L. Chen, Y.C. King, IEEE Electron Device Lett. 27 (2006) 4.
[14] D.J. DiMaria, J. Appl. Phys. 84 (4) (2006) 2100.
[15] C.H. Cho, B.H. Kim, T.W. Kim, S.J. Park, N.M. Park, G.Y. Sung, Appl. Phys.Lett. 86 (2005) 143107.
[16] C.H. Tu, T.C. Chang, P.T. Liu, H.C. Liu, S.M. Sze, C.Y. Chang, Appl. Phys. Lett. 89 (2006) 162105.
[17] C.Y. Ng, T.P. Chen, M. Yang, J.B. Yang, L. Ding, C.M. Li, A. Du, A. Trigg, IEEE Electron Device Lett. 53 (2006) 4.
[18] V. Ioannou-Sougleridis, A.G. Nassiopoulou, J. Appl. Phys. 94 (2003) 4084.
[19] P.F. Lee, W.L. Liu, Z.T. Song, J.Y. Dai, Appl. Phys. Lett. 56 (1999) 150.
[20] T. Takagahara, K. Takeda, Phys. Rev., B 46 (1992) 15578.