Mixed-Mode Simulation of DX Trap-Induced Slow Transient Effects on AlGaAs/GaAs HEMT Inverters

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Abstract—**A mixed level device and circuit simulation has been performed to analyze DX trap-induced slow transient effects on the performance degradation of AlGaAs/GaAs HEMT circuits. The variation of the output pulsewidth and the hysteretic characteristics of the input–output voltage transfer function in DCFL HEMT inverters have been simulated. In the model, a DX trap rate equation is calculated in the AlGaAs layer. The self-consistent Schrödinger and Poisson equations are solved numerically at each cross section of a device. A two-region Grebene–Ghandhi model is employed to derive the *I–V* characteristics. Connections between individual HEMT devices in simulated circuits are treated as nodes of circuit equations. In the simulation, all of the device equations and the circuit equations are iteratively solved until a self-consistent solution is achieved. Our simulation confirms that the output pulse broadening and narrowing effects in a string cascaded DCFL HEMT inverters are a consequence of the inverter voltage transfer function shift caused by deep traps.**

I. Introduction

BECAUSE of their potential for ultra-high-speed LSI applications, $Al_xGa_{1-x}As/GaAs$ high electron mobility transistors (HEMT's) have received considerable interest. Fully functional 4K SRAM and 16 × 16 multiplier circuits have been successfully demonstrated [1], [2]. However, there has been increasing concern that deep traps in the Si-doped $Al_xGa_{1-x}As$ layer, commonly known as DX centers, may play a crucial role in the performance degradation of HEMT devices and circuits. The major detrimental effects include low-temperature current collapse [3], low-frequency noise [4], device threshold voltage shifts [5], [6], and remarkable slow current transients when a device is subject to a gate or a drain voltage pulse [6]–[8]. Recently, it has been reported that the trap-induced transient effects may result in a significant variation of the output pulsewidth in a string of direct-coupled FET logic (DCFL) inverters [9], [10]. In some cases, complete disappearance of output pulses is observed. Such phenomena impose a severe limitation on full utilization of the performance advantage of the HEMT technology in high-precision analog and certain digital circuits. It is therefore of obvious importance to investigate the origin of these effects and to quantify them. In this paper, we intend to develop a numerical model to explore the correlation of the DX trapping mechanism and electron transport physics with the anomalous circuit behavior in HEMT inverters. A mixed-mode device and circuit simulation in this respect provides a better understanding of fundamental physical problems than the SPICE simulation with an analytical model. Using this approach, we simulate the hysteretic characeristics of the input–output voltage transfer function in a DCFL HEMT inverter caused by the DX traps. The pulsewidth broadening and narrowing effects related to the hysteretic loop is explained. The dependence of the logic threshold voltage shift in a HEMT inverter on the input pulse frequency and duty cycle is also evaluated.

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II. Physical Model and Numerical Technique

A. DX Trap Rate Equation

In our mixed level simulation, a DX trap rate equation taking into account shallow donor states is included in the device model [11]

$$\frac{\partial N_{dd}^{+}}{\partial t} = e_n\left(1 + \frac{n_s}{n_c}\right)\left(N_{dd} - N_{dd}^{+}\right) - c_n(n_c + n_s)N_{dd}^{+} \tag{1}$$

where N_{dd} is the concentration of the DX centers, n_s is the electron concentration in the shallow donor states, and n_c is the electron concentration in the conduction band. c_n and e_n are expressed as follows:

$$c_n = \sigma_n\left(\frac{3kT}{m^*}\right)^{1/2}$$

and

$$e_n = c_n(N_c/g_t)\exp\left(-\frac{E_c - E_d}{kT}\right)$$

where m^* is the electron mass, k is the Boltzmann constant, T is temperature, σ_n is the electron capture cross section, g_t is the degeneracy factor for the DX traps, N_c is the effective density of states of the conduction band,

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and E_d is the DX trap energy (a single level of DX centers assumed). For an aluminum composition of 0.3 and a doping level of 1.0×10^{18} $1/\text{cm}^3$, we choose the following experimental data by Ploog *et al.* [12], [13] about the DX trap parameters in AlGaAs material; The electron capture cross section is estimated to be 3×10^{-19} cm^{-2} at room temperature. Thermal barriers for electron emission and capture are about 0.44 and 0.33 eV, respectively. The DX trap energy E_d and the shallow donor state energy are 130 and 6 meV below the conduction band edge. N_{dd} is equal to 7.0×10^{17} $1/\text{cm}^3$. In the above equation, the effective electron emission and capture rates are $e_n[1 + (n_s/n_c)]$ and $c_n(n_c + n_s)$, respectively. The inclusion of the shallow donor states electrons n_s has a significant contribution to the effective rates at low temperatures. The readers should be reminded that i) the above equation reduces to the familiar Shockley–Read–Hall equation if n_s is neglected and ii) the steady-state solution of the N_{dd}^+ in (1) satisfies the Fermi–Dirac distribution.

B. Current–Voltage Model

In order to derive the I–V characteristics of the devices, the quanitization effects of the two-dimensional electron gas (2DEG) in the GaAs quantum well are calculated to obtain an accurate description of the charge modulation by the gate bias. A self-consistent conduction band-edge profile and the 2DEG wave functions are solved from the mutually coupled Poisson and Schrödinger equations in our model. The Schrödinger equation for the wave function $\psi_i(y)$ in the ith subband is

$$\left(-\frac{\hbar^2}{2m^*}\frac{\partial^2}{\partial y^2} + V(y)\right)\psi_i(y) = e_i\psi_i(y) \tag{2}$$

and

$$V(y) = -q\phi(y) + V_h(y) + V_{ex}(y) \tag{3}$$

where $2\pi\hbar$ is the Planck constant, e_i is the ith eigenenergy, $V_h(y)$ is the heterojunction conduction-band discontinuity, $\phi(y)$ is the electrostatic potential, and $V_{ex}(y)$ is the local exchange-correlation potential [14] which represents the effect of the quantum-mechanical many-body exchange interaction between electrons. x is defined as the channel direction and y is defined as the direction perpendicular to the channel. In our quantization calculations, (2) is solved for the lowest five eigenstates. The wave functions solved from (2) are used to calculate the spatial distribution of electrons $n(y)$ in the one-dimensional Poisson equation, i.e.,

$$\nabla \cdot [\epsilon(y)\nabla\phi(y)] = -q[N_{dd}^+(y) + N_{sd}^+(y) - n(y)] \tag{4}$$

where N_{dd}^+ and N_{sd}^+ are ionized DX centers and shallow donor concentrations.

During the transient simulation, the DX rate equation is evaluated at each time step to determine the N_{dd}^+ at each grid point in the AlGaAs layer. The initital condition of the DX traps varies at each grid point and is determined by the device bias history. The Schrödinger and Poisson equations are then calculated self-consistently. It should be emphasized that they are both time- and x-direction dependent. In other words, we need to solve (2) and (4) to generate the relationship between the channel electron contribution and the gate-to-channel potential at each cross section of a device and at each time step. An assumption of a constant quasi-Fermi level in the perpendicular direction is adopted to deduce bulk electron concentrations in the conduction band and in the shallow donor states in the AlGaAs layer. These values are used in (4) and also in the DX rate equation again at the next time step. In the calculation of the drain current, a simple two-region Grebene–Ghandhi model [15] is utilized to manifest the slow transient effects. The detail of the computation method has been described elsewhere [11], [16]. A constant mobility of 8500 $\text{cm}^2/\text{V} \cdot \text{s}$ is assumed in the quasi-linear region which is treated by the gradual channel approximation. A saturation velocity of 2×10^7 cm/s is adopted to partially account for the velocity overshoot effect in the velocity saturation region. Iterations are required at each time step to achieve a self-consistent I–V result.

C. Circuit Simulation

The analysis of the DX trap-induced slow transient effects of a DCFL HEMT inverter is complicated. While the driving FET exhibits a gate pulse transient in switching, the load FET suffers from a drain pulse transient. The overall transient response in HEMT inverters depends on the mutual interaction of the gate transient and the drain transient. The mixed-mode feature of this approach enables us to correlate the fundamental physical effects with circuit behavior directly. In our calculation, the device equations and the circuit equations are grouped separately. The device equations have been formulated in Sections II-A and II-B. In the circuit analysis, connections between individual HEMT devices are treated as nodes of circuit equations which are governed by the Kirchhoff current and voltage laws. In the simulation, the device equations and the circuit equations are iteratively solved until all of them are satisfied.

At the beginning of the circuit analysis, a steady-state simulation is usually performed to obtain the DX trap condition in each FET. During the transient simulation, the solution from a previous time step is used as the initial condition.

III. Results

Both enhancement-type FET (E-FET) and depletion-type FET (D-FET) have a 1-μm gate. The thickness of the AlGaAs layer under the gate is 335 Å in an E-FET and 485 Å in a D-FET including a 35-Å undoped spacer each. The doping concentration in the AlGaAs layer is 1.0×10^{18} cm^{-3}. The Schottky-barrier height on $Al_{0.3}Ga_{0.7}As$ is close to 1.1 eV [17]. The threshold voltage is 0.19 V in the E-FET and −0.6 V in the D-FET.

Lg=1.0 μm

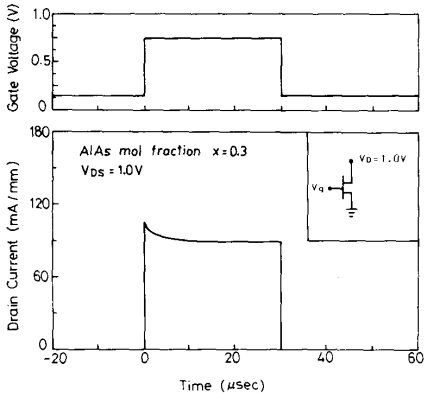

Fig. 1. Gate-pulsed-induced slow transient effect in an E-FET. The gate voltage and the simulated drain current are plotted as functions of time. The circuit diagram is shown in the inset.

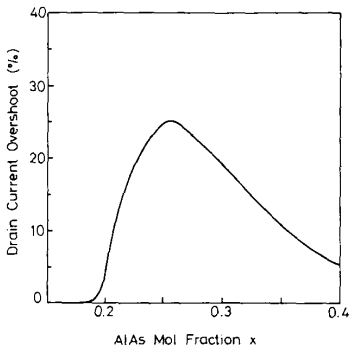

Fig. 2. The magnitude of the gate-pulse-induced current overshoot in terms of the percentage of the steady-state current as a function of Al-mol fraction.

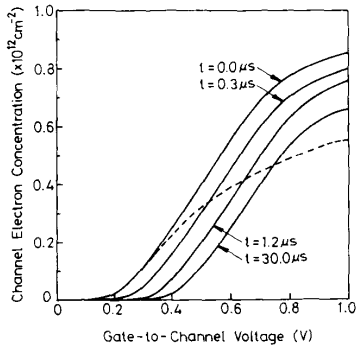

Fig. 3. Channel electron concentration versus gate-to-channel voltage in an E-FET. The dashed line represents a dc result. The gate voltage switches from 0.15 to 0.75 V and the drain bias is 0 V.

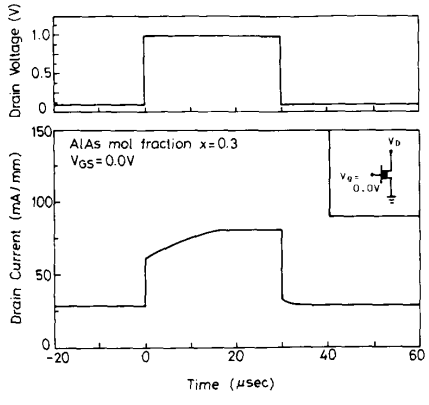

Fig. 4. Drain-pulse-induced current transient characteristics in a D-FET. The drain voltage and the simulated drain current are drawn as functions of time. The circuit diagram is shown in the inset.

Parasitic source and drain resistances are 1.0 Ω · mm in both E-FET and D-FET. The simulation result in Fig. 1 shows that the drain current in the E-FET exhibits a significant transient response to a gate pulse from 0.15 to 0.75 V in the microsecond range. The current overshoot persists over ~ 10 μs, which is related to the electron capture time of the DX traps. The mechanism of the current overshoot at the rising edge of the gate pulse has been discussed in [6] and [11]. The magnitude of the overshoot current in terms of the percentage of the steady-state current is plotted in Fig. 2 as a function of aluminum composition. The overshoot percentage depends on many factors such as bias voltages, device structure parameters, and so on. In the present simulation, a maximum value of about 25% at an aluminum composition of 0.25 is obtained. In addition, our simulation reveals that a higher aluminum composition in the AlGaAs layer does not necessarily lead to a higher steady-state current level due to partial neutralization of the DX traps. The influence of the DX trapping effect on the device threshold voltage shift is studied. Fig. 3 illustrates the temporal variation of the change modulation relationship in the E-FET as a positive gate pulse is applied at $t = 0$. The gate voltage is pulsed from 0.15 to 0.75 V and the drain bias is 0 V. The dashed line in the figure represents a dc result. Here, "dc" means that the DX traps are always in thermal equilibrium. A time-dependent device threshold-voltage shift is observed. The dc curve intersects the $t = 30$ μs line at about 0.75 V. In the calculation of the dc result, the DX traps occupation is derived using the Fermi–Dirac statistics. In the transient curves, the DX traps condition is evaluated from (1). The coincidence of the dc curve and steady-state curve (30 μs is considered as steady state) at the pulse voltage of 0.75 V justifies the numerical scheme used in this work. The simulated feature is consistent with the experimental result by Chandra *et al.* [6, fig. 3] in principle. A drain current transient in the D-FET in response to a drain voltage pulse from 0.1 to 1.0 V is shown in Fig. 4. In contrast, we observe a current undershoot at the rising edge of the pulse. The process of electron emission from the DX traps dictates the undershoot transient. In comparison with the gate transient, the time constant of the drain transient is longer because the DX trap emission barrier is higher than the capture barrier. In a DCFL

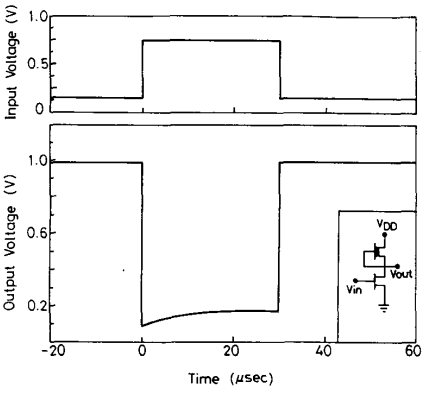

Fig. 5. Transient characteristics of the output voltage in a DCFL inverter. The input and output voltage waveforms are plotted with time. V_{dd} = 1.0 V. The DCFL inverter diagram is shown in the inset of the figure.

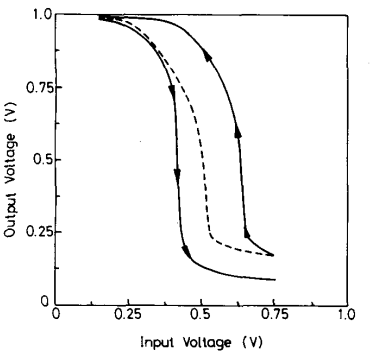

Fig. 6. Simulated input-output voltage transfer function in a DCFL inverter. The dashed line represents the static voltage transfer curve.

inverter, the transient characteristics of the output voltage is simulated in Fig. 5. V_{dd} = 1.0 V. In the simulation, the inverter is initially "soaked" at an input voltage of 0.15 V for a sufficiently long time. An input pulse from 0.15 to 0.75 V is applied at $t = 0$. The pulse duration is 30 μs. The combined influence of the gate transient and the drain transient in the driving and the load FET's results in a hysteretic nature of the input-output transfer curve (VTC) in the inverter. The simulation result is shown in Fig. 6. The dashed line is the static VTC. The hysteresis is caused by the change of the DX trap conditions in both E-FET and D-FET in the pulse duration. The opening of the hysteretic loop at the input voltage is 0.75 V corresponds to the output-voltage undershoot in Fig. 5. The shift of the logic threshold voltage amounts to $\sim$0.19 V in Fig. 6. The variation of the VTC with the DX trap condition has a profound singificance for circuit performance. As a matter of fact, the shift of the VTC is directly responsible for the pulsewidth broadening and narrowing phenomena observed in the output of an inverter chain.

In order to explain the DX trap induced pulse broadening effect, let us assume an ideal VTC which has a sharp transition at the switching voltage in Fig. 7(a). The VTC shifts rightward with time because of electron capture in the E-FET and electron emission in the D-FET during the excitation of the input pulses. The voltage level of the input pulses is purposely chosen to be 0.45 V for a low state and 0.75 V for a high state to demonstrate the broadening effect in a single inverter stage. In practice, the voltage levels of the pulses should be determined by the intersections of the static VTC and its folded curve. With such voltage levels, the pulse broadening effect may still appear in a sufficiently long chain of inverters under certain conditions [9], [10]. However, the simulation of a long inverter chain using the mixed-mode approach is CPU time prohibitive. According to the VTCs in Fig. 7(a), an input voltage of 0.45 V should yield a low output level for $t_0 \le t \le t_1$ and a high output level for $t_1 \le t$. Fig. 7(b) plots the input and the output voltage waveforms. The first two output pulses are apparently merged. For a comparison, we also plot the output voltage without the DX trap effect (dotted curve) in the figure. To verify the above explanation, we perform a simulation in a two-stage inverter chain. The input pulse has a period of 0.24 μs and 50% duty cycle. Fig. 8 shows the input and the

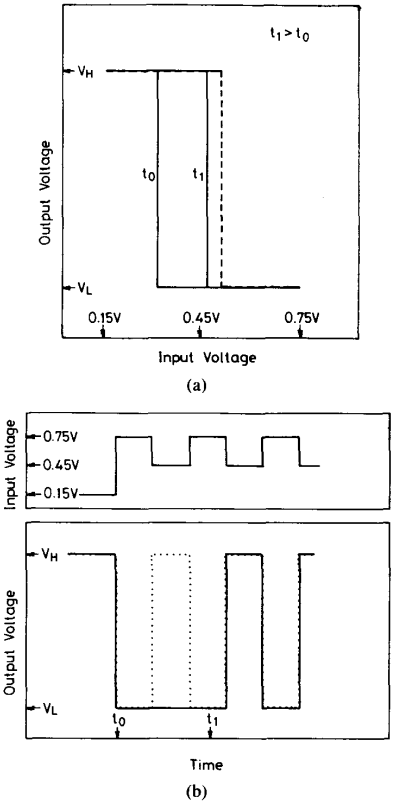

Fig. 7. (a) Hypothetical voltage transfer curves in a DCFL HEMT inverter. The dashed line represents a static VTC. (b) Input and output voltage waveforms according to Fig. 7(a). The dotted curve is the output voltage without the DX traps effect.

Lg=1.0 μm

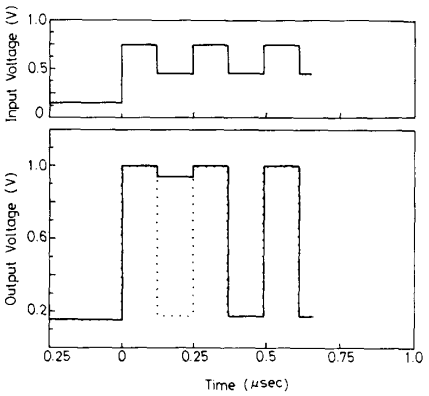

Fig. 8. The input and the simulated output voltage waveforms in a two-stage inverter chain. The dotted curve shows the output voltage without the DX trap effect.

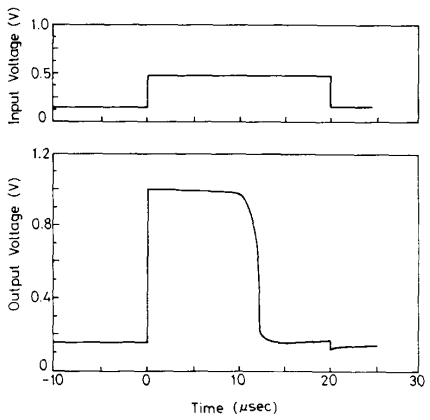

Fig. 9. The input and the simulated output voltage waveforms in a two-stage inverter chain.

simulated output waveforms. The simulated output voltage without the DX trap-induced transient effects is shown in the dotted curve. The output pulse broadening effect is clearly demonstrated in this figure.

In some cases, the pulse narrowing effect in a HEMT inverter chain also occurs. For example, we choose a low state voltage of 0.15 V and a high state voltage of 0.48 V. The pulsewidth is 20 μs. The circuit initial condition is the same as previously described. The simulated output waveform after two cascaded inverters is drawn in Fig. 9. The reduction of the output pulsewidth by 40% is obtained. The output waveform exhibits undershoots at $t = \sim 16$ μs (very slightly) and at $t = 20$ μs, which have the same physical origin as the feature observed in Fig. 5.

Some factors affecting the hysteretic characteristics of the VTC in a DCFL inverter are examined. Fig. 10 shows the logic threshold voltage shift as a function of the pulse frequency. The circuit initial condition and the bias voltages are the same as in Fig. 5. The pulse duty cycle is 50%. At high frequencies ($< 10^8$ Hz), the hysteretic characteristics disappear since electron capture and emission mechanisms cannot catch up with the input signal. Likewise, aluminum composition in HEMT devices has a strong influence on the hysteretic characteristics. The low-frequency threshold-voltage shift as a function of aluminum composition x is plotted in Fig. 11. Although the logic threshold voltage shift can be minimized by adjusting various device parameters and circuit operating conditions, an essential approach is to choose $x \leq 0.2$ in HEMT circuits for the immunity from the DX traps effect.

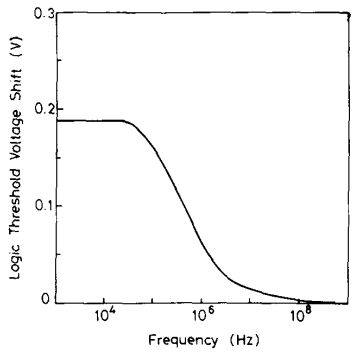

Fig. 10. Logic threshold voltage shift versus input pulse frequency. The pulse duty cycle is 50%.

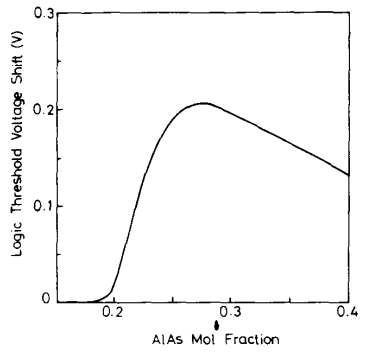

Fig. 11. Logic threshold voltage shift versus AlAs mol fraction.

IV. Conclusion

The DX trap-induced slow transient effects in HEMT devices and circuits have been analyzed using a mixed mode simulation. The gate transient and the drain transient in discrete devices have been quantitatively studied. In DCFL HEMT inverters, we conclude that the observed pulsewidth variation is attributed to the shift of the voltage transfer function. The DX traps have an adverse impact on the aplication of the HEMT technology. The extent of the influence varies with device structure parameters and circuit operation conditions. We have shown that the reduction of the aluminum composition below 0.2 can greatly reduce the DX trap-induced performance degradation in HEMT devices and circuits.

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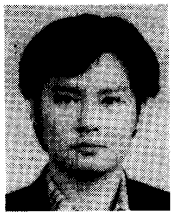

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