New Observation of Gate Current in Off-State MOSFET

Ming-Jer Chen, *Member, IEEE*

***Abstract*—For a gate-controlled p^+-n diode having gate-p^+ overlap area of 3.7×10^{-4} cm^2, the work reports a new observation of the leakage current through a 235-Å gate oxide: the gate current components both due to Fowler–Nordheim electron tunneling through the gate-p^+ overlap oxide and due to hot-electron injection have been separately detected. The corresponding gate current has been found to be dominated by Fowler–Nordheim electron tunneling prior to significant surface avalanche impact ionization. This observation is important for device application and for reliability study.**

I. Introduction

Recently, the gate current in thin-oxide n-channel MOSFET's has been extensively investigated [1], [2]. The importance of such current for device application as well as for reliability study has also been addressed [1], [2]. Chang *et al.* [1] and Chen *et al.* [2] have concluded that for oxides of less than 100–110 Å the gate current is dominated by Fowler–Nordheim (F-N) electron tunneling and for oxides greater than 100–110 Å the gate current is dominated by hot-carrier injection. Based on a 235-Å-gate oxide p-channel MOSFET used in our work, however, the dominant mechanisms responsible for the measured gate current have been found to be inconsistent with such conclusion and will be reported in this paper.

II. Experiment

The structure of the device in this experiment consists of on-chip 864 gated p^+-n diodes in parallel. Fig. 1 shows the cross section of six such diodes. This structure has been fabricated by the conventional n^+ polysilicon-gate n-well CMOS process. The gate oxide has been grown at 920°C for 39 min in an O_2/TCA ambient, followed by an annealing process at 920°C for 30 min in a N_2 ambient. The gate oxide thickness, measured by an ellipsometer, is about 235 Å. Based on an autospreading resistance probe, the junction depth and surface doping concentration of the n-well have been determined to be 2.47 μm and 1.5×10^{16} cm^{-3}, respectively. Also, the junction depth and surface doping concentration of the p^+ region have been determined to be 0.44 μm and 4×10^{19} cm^{-3}, respectively. The total peripheral length is 124 416 μm. We estimate the effective lateral diffusion length for the p^+ region is 0.3 μm and thus the total gate-p^+ overlap area is $124\,416 \times 0.3$ μm^2 ($\cong 3.7 \times 10^{-4}$ cm^2). The fabricated structure has been mounted on a ceramic 24-pin package which has been inserted into an RMC-Cryosystems LTS-22 chamber for temperature-dependent measurement.

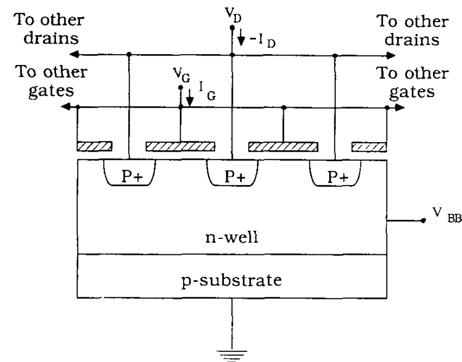

Fig. 1. Schematic cross section of six gate-controlled p^+-n diodes in parallel.

Under the back-gate bias $V_{BB} = 0$ V, the measured drain current I_D, and the measured gate current I_G both versus the gate voltage V_G ranged from -10 to 10 V are shown in Fig. 2. The data in Fig. 2 are presented for two different temperatures, -23 and -60°C, and for two different drain voltages, $V_D = -7$ V and $V_D = -10$ V. Under the temperature of -23°C and $V_D = -10$ V, moreover, Fig. 3 presents the measured result of the drain and gate currents versus the gate voltage for two different back-gate biases $V_{BB} = 0$ V and $V_{BB} = -3$ V.

III. Discussion

For a drain current lower than about 10^{-7} A, the measured drain *I–V* characteristics, as illustrated in Figs. 2 and 3, are due to band-to-band tunneling in the gate-p^+ overlap region [3]–[5]. This can be identified by noting from Fig. 3 that the drain current is insensitive to the back-gate bias until a kink appears, and by noting from Fig. 2(a) and (b) that the drain current increases as the temperature increases until a kink appears. Moreover, Figs.

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The author is with the Institute of Electronics, National Chiao-Tung University, Hsin-Chu, Taiwan 30039, Republic of China.

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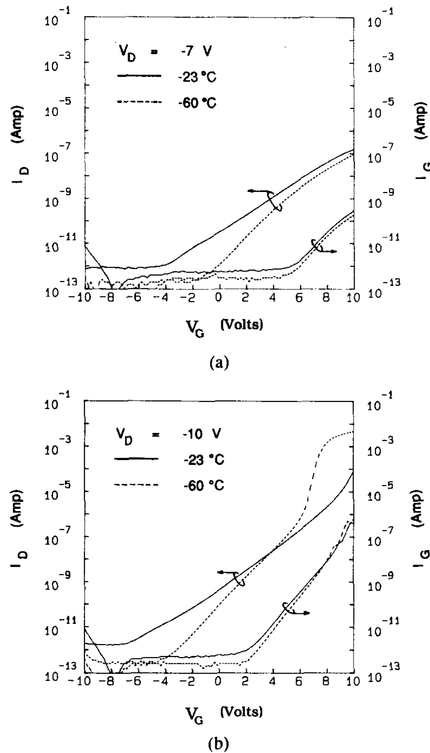

Fig. 2. The measured drain and gate currents versus gate voltage with two different temperatures of $-23°C$ and $-60°C$ for (a) $V_D = -7$ V and (b) $V_D = -10$ V.

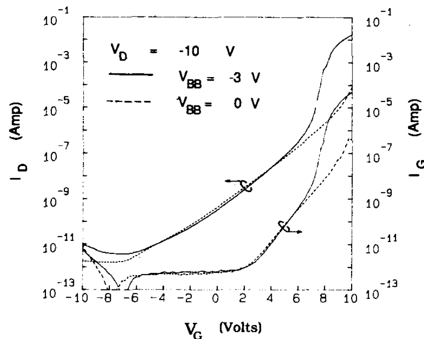

Fig. 3. The measured drain and gate currents versus gate voltage with two different back-gate biases of -3 and 0 V for $V_D = -10$ V at temperature of $-23°C$.

2 and 3 demonstrate a kink on the drain I–V curve as the drain current exceeds about 10^{-7} A. Such kink is attributed to the amplification of the band-to-band tunneling current by avalanche impact ionization [3]–[5]. This can be given verification by noting from Fig. 2(b) that for the drain current above 10^{-7} A the drain current decreases due to a reduction in the impact-ionization coefficient as the temperature increases. Also, it can be noted from Fig. 3 that as the value of back-gate bias is changed from -3 to 0 V, the onset of the kink on the drain I–V curve is shifted from $V_G \cong 6$ V to $V_G \cong 9$ V, indicating the effect of back-gate bias on the surface lateral field required for impact ionization.

Accompanied by the measured drain current mentioned above, the corresponding gate currents are also presented in Figs. 2 and 3. For the case of $V_D = -7$ V, we attribute the measured gate current shown in Fig. 2(a) to F-N electron tunneling since the gate current increases slightly with the temperature [2], [6]. The gate current for $V_D = -10$ V shown in Fig. 2(b) also demonstrates such temperature dependence until a kink appears. Such kink is observed as the gate current exceeds about 10^{-9} A. We attribute this kink to hot-electron injection since the corresponding gate current decreases due to a reduction in impact ionization coefficient as the temperature increases. More importantly, it can be verified by noting, from Fig. 3, that the kink appearing on the gate I–V curve for $V_{BB} = -3$ V is drastically suppressed for $V_{BB} = 0$ V, indicating the role of the lateral field for hot electrons injected into the oxide.

Straightforwardly, the calculation of the theoretical F-N currents has been performed using the following expression [6]:

$$\frac{I_G}{A_{DG}} = C \cdot E_{ox}^2 \cdot \exp\left(-\frac{\beta}{E_{ox}}\right)$$

where A_{DG} ($=3.7 \times 10^{-4}$ cm^2) is the gate-p$^+$ overlap area and the values of both the pre-exponential constant C ($=2.3 \times 10^{-6}$ A/V^2) and the physical constant β ($=2.385 \times 10^8$ V/cm) have been chosen to be identical to the experimentally fitted data as cited in [7]. The oxide field strength E_{ox} is given by

$$E_{ox} = \frac{(V_G - V_D - (V_{FB} + \psi_S))}{t_{ox}}$$

where t_{ox} ($=235$ Å) is the oxide thickness, V_{FB} is the flat-band voltage for the MOS system on the p$^+$ region, and ψ_S is the associated surface potential. Fig. 4 shows the calculated F-N currents for $(V_{FB} + \psi_S) = 0$ and -0.8 V, where the measured gate current versus the gate voltage for $V_D = -10$ V and $V_{BB} = 0$ V as given in Fig. 3 is also presented for comparison. From Fig. 4, it can be observed that the $(V_{FB} + \psi_S)$ value of -0.8 V yields better agreement with experimental results than the value of 0 V.

Based on the above experimental results, we conclude that in a 235-Å gate-oxide p-channel MOSFET the gate current components contributed by F-N electron tunneling through the gate–drain overlap oxide and by hot-electron injection have been separately detected. Moreover, the gate current has been found to be dominated by F-N electron tunneling through the gate–drain overlap oxide prior to significant avalanche impact ionization. This new observation has not been reported previously. Otherwise, earlier similar work [1], [2] has concluded that for oxides of less than 100–110 Å the gate current is dominated by

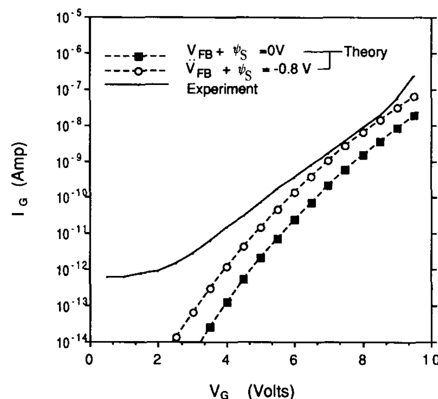

Fig. 4. Comparison of the measured gate current versus gate voltage for $V_D = -10$ V and $V_{BB} = 0$ V at -23°C and the theoretical F-N tunneling currents calculated for $(V_{FB} + \psi_S) = 0$ and -0.8 V.

F-N electron tunneling and for oxides greater than 100–110 Å the gate current is dominated by hot-carrier injection. This is indeed contrary to the results of our work. To account for this discrepancy, two plausible explanations are suggested here. One explanation takes into account the different types of gate-controlled diode junctions used, i.e., the boron-implanted p^+-drain to n-well junction used in our work, and the arsenic-implanted n^+-drain to p-substrate used in [1] and [2]. The arsenic-implanted n^+ region has a steeper doping gradient and thus delivers a higher electric field, which would increase the effect of the hot-carrier injection. On the other hand, we can attribute this contradiction to the different gate-drain overlap areas used, i.e., 5×10^{-8} cm^2 in [1], 15×10^{-8} cm^2 in [2], and 3.7×10^{-4} cm^2 in our work. Based on the theoretical and experimental F-N currents shown in Fig. 4, it can be seen that for a 235-Å gate-oxide p-channel MOSFET but with the gate–drain overlap areas identical to those in [1] and [2], the corresponding gate currents contributed by F-N electron tunneling are too low to be detected by the present measurement instrument such as the semiconductor device parameter analyzer HP 4145.

IV. Conclusion

For a 235-Å gate-oxide p-channel MOSFET with the gate–p^+ overlap area of 3.7×10^{-4} cm^2, the gate current components contributed by F-N electron tunneling through the gate–drain overlap oxide and by hot-electron injection have been separately detected. Since the gate current is important for device application and for reliability study, this work, based on one of the two proposed explanations, suggests a relatively large peripheral length around the gate–drain overlap region in order to accurately monitor the dominant mechanisms responsible for the leakage current through the oxide.

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Ming-Jer Chen (S'77–M'90) was born in Taiwan, Republic of China, on April 1, 1954. He received the B.S. degree with highest honors from the National Cheng-Kung University in 1977, and the M.S. and Ph.D. degrees from National Chiao-Tung University in 1979 and 1985, respectively, all in electrical engineering. His doctoral work involved the modeling and prediction of CMOS latch-up.

From 1979 to 1980, he worked for Telecommunication Laboratories, Taiwan, where he was responsible for design and implementation of a multiprocessor distributed system. From 1985 to 1986, he conducted post-doctoral research on CMOS latch-up at National Chiao-Tung University. Since 1986, he has become an Associate Professor in the Department of Electronics and the Institute of Electronics, National Chiao-Tung University. His primary research areas of interest have been in the modeling and optimization of semiconductor devices and integrated circuits. Currently, he is thoroughly involved in BiCMOS integration, nonvolatile memories, low-temperature devices, VLSI implementation of a neural network and its system setup for the hearing impaired, and device reliability concerning ESD, latch-up, leakage, and hot-carrier effect.

Dr. Chen is a member of Phi Tau Phi.