Numerical Analysis of the Frequency-Dependent Output Conductance of GaAs MESFET's

Shih-Hsien Lo, *Student Member, IEEE,* and Chien-Ping Lee, *Member, IEEE*

***Abstract*—The small-signal output conductance of GaAs MESFET's on semi-insulating substrate has been studied using two-dimensional numerical analysis. Frequency-, temperature-, and drain-bias-dependent behaviors of the output conductance are analyzed. It is confirmed that the bulk EL2 traps contribute significantly to the low-frequency-dependent behavior of the output conductance. Devices with different background trap concentration and acceptor concentration have been analyzed and compared. For devices with higher trap concentration and higher acceptor concentration, the output conductance is lower but exhibits stronger frequency dependence.**

Nomenclature

- C_n Electron capture coefficient of EL2 traps.
- D_n Electron diffusion coefficient.
- e_n Electron emission rate of EL2 traps.
- E_{CT} Energy difference between the conduction band edge and the EL2 level.
- E_G Energy gap of GaAs.
- f Frequency.
- I_D DC drain current.
- $\tilde{I}_D$ AC drain current.
- $\vec{J}_n$ Electron current density.
- k Boltzmann constant.
- K Degree in Kelvin.
- n Free electron concentration.
- N_A Shallow acceptor concentration.
- N_C Effective density of state in the conduction band.
- N_D Donor concentration.
- N_V Effective density of state in the valence band.
- N_T EL2 concentration.
- N_T^+ Ionized EL2 concentration.
- q Electron charge.
- t Time.
- T Temperature.
- V Volt.
- V_D DC drain voltage.
- $\tilde{V}_D$ AC drain voltage.
- V_G DC gate voltage.
- $\tilde{Y}_D$ Small-signal output conductance.
- $\tilde{Z}_D$ Small-signal output resistance.
- ϵ Permittivity of GaAs (F/cm).
- μ Electron mobility (cm^2/V · s)
- Ψ Electrostatic potential.
- ω Angular frequency (radian/s).

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The authors are with the Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsin-Chu, Taiwan, Republic of China.

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I. Introduction

IT IS well known that the small-signal output conductance of GaAs MESFET's fabricated on semi-insulating substrates are frequency-dependent (below about 1 MHz) [1]–[9]. The small-signal output conductance from dc measurements differs significantly from the value obtained at high frequencies. The shift in output conductance varies widely depending on the bias condition and the device structure. At high frequencies, the output conductance saturates and the saturation frequency is very sensitive to the temperature of operation [4], [7], [8]. The change in output conductance has a great impact on device performance, and it is a serious problem for many analog and digital circuits.

A complete understanding of the real causes of the frequency-dependent phenomena will provide correct information for large-signal device modeling and predict the performance of MESFET's and complex integrated circuits. Many authors have recognized that the frequency-dependent behavior of the output conductance is closely related to the slow time response behavior of the deep traps near the channel–substrate interface [1], [2], [5]. Until now, all the reported works concerning this behavior have been based on experimental measurements [1]–[9]. Detailed numerical simulation, which can quantitatively calculate the influence of the deep traps on the output conductance is still nonexistent.

In this work, the frequency dependence of the output conductance of GaAs MESFET's is studied by a two-dimensional sinusoidal steady-state analysis [10]. The bulk electron traps—EL2's are taken into consideration by an Ideal and simplified Shockley–Read–Hall trap model. The temperature-dependent and drain-bias-dependent behavior is simulated and compared with published experimental results. In addition, devices with different trap concentrations and different acceptor concentrations are simulated and compared.

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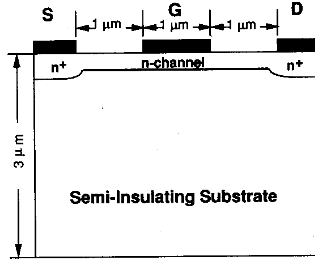


Fig. 1. Device structure of the ion-implantation GaAs MESFET on semi-insulating substrate used in the study.

II. Device Structure

The device structure for the GaAs MESFET's used in this study is shown in Fig. 1. This is a selectively ion-implanted MESFET structure [11]. The doping profile for the channel is represented by a Gaussian function. The gate length is 1 μm, and the spacing between the source/drain contacts and the gate is 1 μm. The total depth of the simulated device is 3 μm, which is deep enough to encompass all physical phenomena that occur. Different implant profiles with a higher dose and a deeper depth are used for the source and drain regions. The threshold voltages range from -0.6 to -1 V depending on the chosen background acceptor concentration (N_A) and the EL2 concentration (N_T) in the substrate. For $N_T/N_A = 5 \times 10^{16}$ cm^{-3}/5×10^{15} cm^{-3} and $N_T/N_A = 1 \times 10^{16}$ cm^{-3}/1×10^{15} cm^{-3}, the threshold voltages are around -0.6 and -1 V, respectively. Both N_T and N_A assumed in this study are typical values found in normal LEC substrates [12].

III. Basic Equations and Numerical Methods

The time-dependent equations used in the study are described as follows:

1) Rate equation for traps

$$-\{C_n n N_T^+ - e_n(N_T - N_T^+)\} = -\frac{\partial}{\partial t}(N_T - N_T^+). \quad (1)$$

2) Continuity equation

$$-\frac{1}{q}\nabla \cdot \vec{J}_n - \{C_n n N_T^+ - e_n(N_T - N_T^+)\} = \frac{\partial n}{\partial t}. \quad (2)$$

3) Electron drift-diffusion current equation

$$\vec{J}_n = -q\mu_n n \nabla \Psi + qD_n \nabla n. \quad (3)$$

4) Poisson's equation

$$\nabla^2 \Psi + \frac{q}{\epsilon}(-n + N_D - N_A + N_T^+) = 0. \quad (4)$$

The Schockley–Read–Hall model is used in (1) to describe the electron emission and capture processes for the EL2 traps. Because EL2's are electron traps, the terms related to hole emission and hole capture have been neglected. The emission rate (e_n) is related to the capture coefficient (C_n) by

$$e_n = C_n N_c \exp(-E_{CT}/kT) \quad (5)$$

where E_{CT} is the energy difference between the EL2 level and the conduction band edge. The emission rate is temperature-dependent and is described by a semi-empirical formula as [13]

$$e_n = 3.42 \times 10^7 T^2 \exp(-0.825 \cdot q/kT) \text{ s}^{-1}. \quad (6)$$

The energy level of EL2 is also temperature-dependent and is described by [14]

$$E_{CT} = 0.75 - 3.36 \times 10^{-4} T^2/(T + 204) \text{ eV} \quad (7)$$

The temperature dependence of other physical parameters, like the effective density of states in the conduction band (N_C), the effective density of states in the valence band (N_V), the intrinsic carrier concentration (n_i), and the energy gap of GaAs (E_G), has also been considered in the calculation. In (2), the hole continuity equation is neglected. In (3), Einstein's relation is assumed to hold between the mobility and the diffusion coefficient. To simplify the calculation, a two-region mobility model is used to describe the field-dependent mobility term. Since we are mainly interested in the low-frequency response of the devices, the mobility model does not have significant effect on the result. For the temperature range (275–325 K) we are interested in, the low-field mobility and the saturation velocity for electrons are assumed to be 5000 cm^2/V $\cdot$ s and 1.5×10^7 cm/s, respectively.

The surface traps also seem to be strongly related to the low-frequency-dependent behavior of device characteristics such as transconductance [15], but does not seem to contribute to the drain-induced effects such as the low-frequency-dependent behavior of the output conductance [16], [17]. In this study, only contributions from the bulk EL2 traps are considered. The surface between the gate and the source/drain is assumed to satisfy the Neumann boundary condition and the surface traps are neglected.

Before the small-signal calculation, a dc solution needs to be first obtained. The coupled equations, (1)–(4), can be simplified and rewritten similar to that described in [18]. The Newton's method is used in our calculation. For small-signal analysis, various methods have been compared by Laux [10]. The sinusoidal steady-state analysis is the superior approach and is used in this study. When a drain bias, which consists of a dc part and an ac term that varies as $e^{j\omega t}$, is added, using Taylor's expansion, all variables and all equations in (1)–(4) can been linearized and split into a dc part and an ac part. Finally, a large ac matrix is obtained. After the ac matrix is solved, the ac drain phase terms are calculated and the output conductance which is defined as

$$\tilde{Y}_D = \frac{1}{\tilde{Z}_D} = \frac{\tilde{I}_D}{\tilde{V}_D} \quad (8)$$

can be calculated. In (8), $\tilde{Y}_D$, $\tilde{Z}_D$, $\tilde{I}_D$, and $\tilde{V}_D$ are the output conductance, the output resistance, the ac drain voltage, and the ac drain current, respectively.

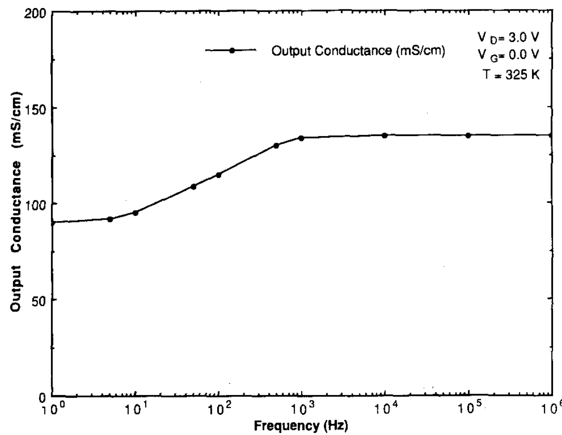


Fig. 2. Calculated output conductance versus frequency. The temperature is 325 K and the N_T/N_A is 5×10^{16} cm^{-3}/5×10^{15} cm^{-3}. The drain voltage and the gate voltage are 3 and 0 V, respectively.

IV. Results and Discussions

In order to study the role of the bulk deep traps on the low-frequency-dependent behavior of the output conductance, we have considered not only the frequency but also the effects of temperature and the drain bias on the output conductance and compared them with published experimental results. Five devices with different bulk EL2 concentrations (N_T) and different acceptor concentrations (N_A) have been simulated and compared to each other.

A. Frequency-Dependent Output Conductance

The calculated small-signal output conductance as a function of frequency is shown in Fig. 2. In order to have a good comparison with the experimental results shown in [7] and [8], the temperature used is 325 K. Results calculated for other temperatures will be discussed later. The drain and the gate are biased with 3 and 0 V, respectively. The EL2 concentration N_T and acceptor concentration N_A are 5×10^{16} and 5×10^{15} cm^{-3}, respectively. The threshold voltage is around -0.6 V. From Fig. 2, we can see that the output conductance increases very slightly before 10 Hz but undergoes a drastic increase between 10 Hz and 1 kHz. After that it saturates at its maximum value at a frequency of approximately 1 kHz. The calculated percentage shift of the output conductance can reach 50%. The experimental results reported in [6] and [7] also show, at $T = 325$ K, that the output conductance starts to increase at a frequency of 10 Hz and reaches its saturated maximum value at 1 kHz. These results agree very well with our calculated results. Hence, based on our calculation, we can conclude that the bulk deep traps are indeed the cause of the low-frequency-dependent behavior of the output conductance.

In order to understand how the deep traps affect the small-signal output conductance, the depth profiles for the real parts of the ac amplitude of the ionized EL2 concentration, the electron concentration, and the electrostatic potential along the gate edge near the drain side are shown

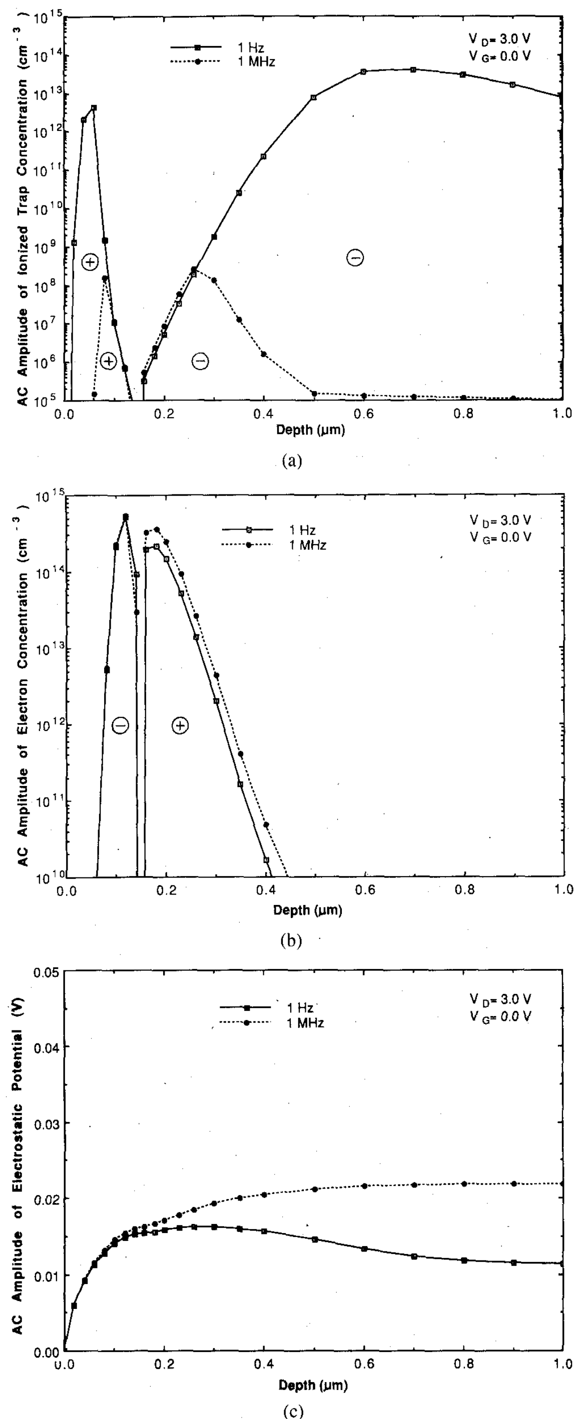


Fig. 3. Calculated ac amplitudes of (a) the ionized trap concentration, (b) the electron concentration, and (c) the electrostatic potential profiles along the gate edge on the drain side at 1 Hz and 1 MHz. The temperature, the N_T/N_A and the dc voltages are the same as those used in Fig. 2. The amplitude of the ac drain voltage is 0.05 V.

in Fig. 3(a)–(c), respectively. The amplitude of the ac drain voltage is 0.05 V. Two different frequencies, 1 Hz and 1 MHz, are chosen for comparison. At high current

levels (i.e., V_G is far greater than V_T), the imaginary parts of these solutions are far less than their real parts at frequencies between 0.1 Hz to 1 MHz. Therefore, the imaginary part of the output conductance $\tilde{Y}_D$ and that of the output resistance $\tilde{Z}_D$, defined by (8), can be neglected. From Fig. 3(a) and (b), one can see that, responding to the ac signal applied to the drain, the small-signal perturbation of the electron concentration occurs near the Schottky depletion edge and the interface (about 0.15 μm from the surface) between the channel and the substrate but the small-signal perturbation of the ionized EL2 concentration occurs near the Schottky depletion edge and the center of the depletion region in the substrate side. The ac amplitude of the ionized trap concentration is positive on the channel side and negative on the substrate side (see Fig. 3(a)). On the other hand, the ac amplitude of the electron concentration, shown in Fig. 3(b), has the opposite sign as the ionized trap concentration. This phenomenon can be easily explained as follows: the ac drain voltage increases the channel potential and the gate depletion edge extends deeper, so the total electron concentration is reduced. Consequently, the ionized trap concentration on the channel side increases due to the reduction of capture probability which is proportional to the electron concentration. But on the substrate side, the ac drain voltage increases the amount of electron injection from the channel into the substrate and effectively increases the electron concentration and the capture probability, so the ionized trap concentration is reduced. Because the capture probability is proportional to the product of the electron concentration and the ionized EL2 concentration and because there are more ionized EL2's and less free electrons existing far from the interface in the substrate side, the ac perturbation of the ionized EL2 concentration occurs around the depletion region in the substrate side.

As shown in Fig. 3(a), for two different frequencies (1 Hz and 1 MHz), the amplitude at 1 Hz is far greater than that at 1 MHz (larger than five orders of magnitude). That is due to the slow time response of the EL2's. At high frequencies (usually, higher than 1 kHz at T = 325 K), the processes for the electron emission and capture through the EL2's cannot completely respond to the fast ac voltage signal, so the magnitude of the ac amplitude is very small. Because of the difference in the distribution of the ac perturbation of the ionized EL2's, the profiles of the ac amplitude of the electrostatic potential at the two frequencies are quite different (see Fig. 3(c)). To see more clearly, two-dimensional contour plots of the ac amplitude of the potential distributions at 1 Hz and 1 MHz are shown in Fig. 4(a) and (b), respectively. At 1 MHz, the substrate potential is higher because the interface depletion width cannot respond to the fast ac signal and the interface potential barrier will not have time to increase the voltage drop due to the addition of the ac drain voltage. Therefore, at higher frequencies, the higher substrate potential can cause more electron injection from the channel as shown in Fig. 3(b). That is the reason why the output conductance is larger at higher frequencies.

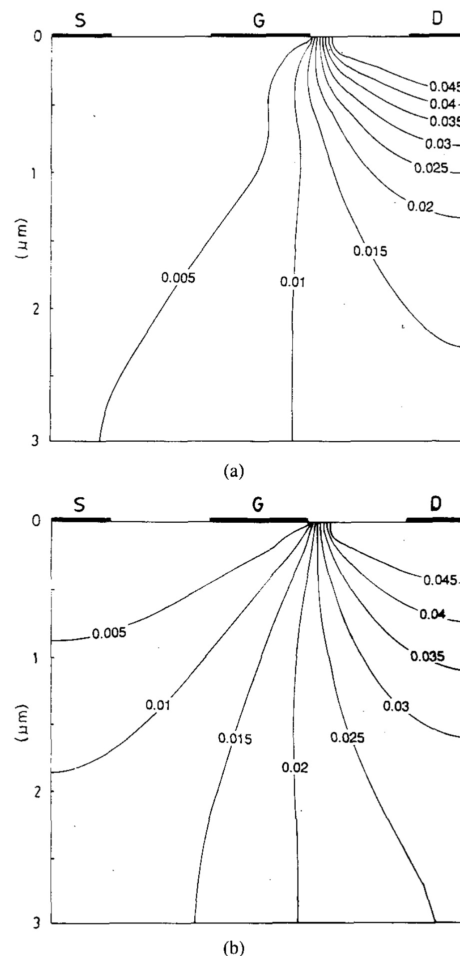


Fig. 4. Contour plots for the electrostatic potential distribution at frequencies of (a) 1 Hz and (b) 1 MHz. The temperature, the N_T/N_A and the voltages are the same as those used in Fig. 2.

B. Different Drain Bias Effects

Calculated small-signal output resistance (i.e., inverse of output conductance) as a function of frequency at different drain voltages is shown in Fig. 5. N_T and N_A values are the same as those used in Fig. 2. The temperature is 300 K, the dc gate voltage is 0 V and the dc drain voltage is varied from 1 to 5 V. From Fig. 5, clearly, the output resistance increases monotonically as the drain voltage is increased at all frequencies. At a drain voltage of 1 V, which is slightly larger than the saturation voltage of the device, the percentage drop in output resistance is 17% (for frequency varied from 0.1 Hz to 1 MHz). But, as the drain voltage increases, the change in output resistance is also increased. At a drain voltage of 5 V, the percentage drop reaches 40%. These results agree with Golio's measurement done at different drain voltages [8].

To explain the phenomenon that the output resistance increases monotonically with drain voltage, we plotted the electron mobility profile along the channel, shown in Fig. 6. The mobility is calculated along the valley where the

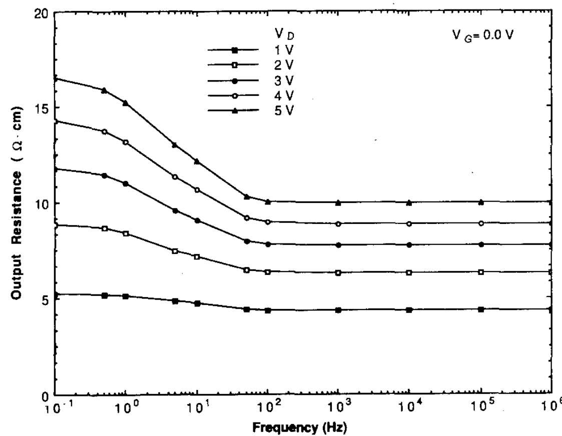


Fig. 5. Calculated output resistance versus frequency with various drain voltages. The temperature is 300 K and $N_T/N_A = 5 \times 10^{16}$ cm^{-3}/5×10^{15} cm^{-3}. The gate bias is 0 V.

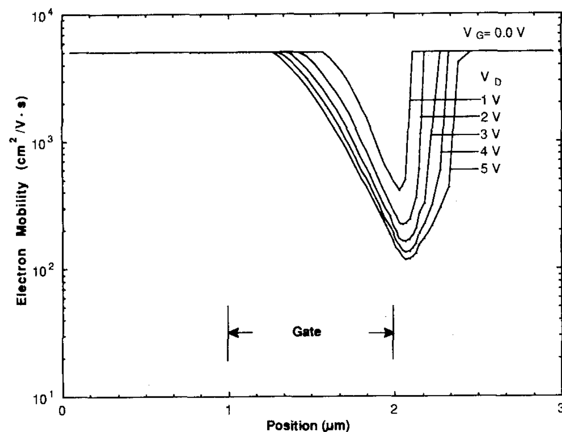
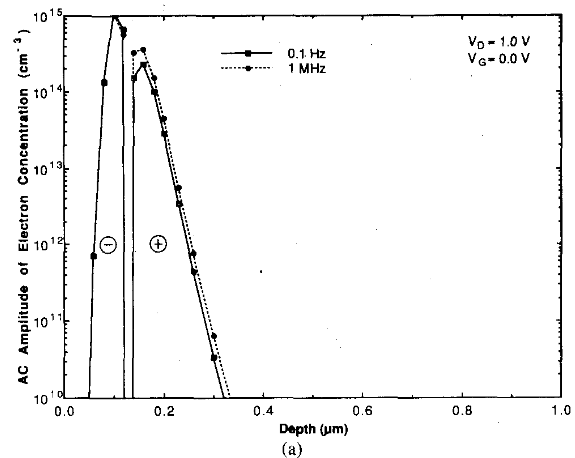


Fig. 6. Calculated mobility profiles along the valley where the electron conduction band is lowest in the channel. The dc drain voltage range, the gate bias, and the N_T/N_A are the same as those used in Fig. 5.



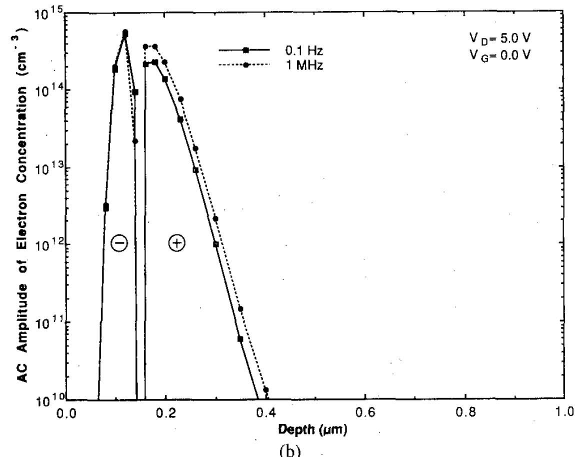


Fig. 7. Calculated ac amplitude of the electron concentration profiles at f = 0.1 Hz and f = 1 MHz as (a) V_D = 1 V and (b) V_D = 5 V.

electron conduction band is the lowest in the channel. As shown in Fig. 6, most of the channel except near the gate edge on the drain side is in the low-field region where it has constant mobility, i.e., $\mu_n = 5000$ cm^2/V · s. When the drain voltage is increased, the velocity saturation region (i.e., the low-mobility region and $\mu_n < 5000$ cm^2/V · s) expands toward both the gate side and the drain side. From basic FET analysis, the output resistance is mainly determined by the resistance in the velocity saturated region, where the channel is narrowest. The more the channel is in the low-mobility region, the higher the resistance is. Therefore, we can conclude the output resistance increases with the drain voltage is due to an expansion of the high-field, low-mobility region in the channel as the drain voltage is increased.

The depth profiles of the ac amplitude of the electron concentration along the gate edge near the drain side at f = 0.1 Hz and f = 1 MHz are shown in Fig. 7(a) for V_D = 1 V and Fig. 7(b) for V_D = 5 V. The amplitude of the added ac drain voltage is 0.05 V. Some interesting phenomena are noticed from these two figures. First, the channel/substrate interface at V_D = 5 V is deeper than at V_D = 1 V due to higher substrate current injection at high drain voltages. Second, the small-signal perturbation of the electron concentration in the channel side at V_D = 5 V occurs farther from the gate than at V_D = 1 V. This is because at higher drain voltages, the channel potential is higher and the gate depletion edge extends deeper. Third, the distribution of the small-signal electron concentration in the substrate side at V_D = 5 V is broader than at 1 V. This is because, at higher drain voltages, the substrate potential is higher and the electrons can be injected deeper into the substrate. Fourth, for the two profiles in the substrate side at 0.1 Hz and 1 MHz, the quantitative difference at V_D = 1 V is almost the same as at V_D = 5 V. Therefore, the difference of the output conductance at the two different frequencies, 0.1 Hz and 1 MHz, is almost the same in spite of different drain bias.

C. Temperature Effects

The calculated small-signal output conductances, which have been normalized to the magnitude at 1 MHz, as a

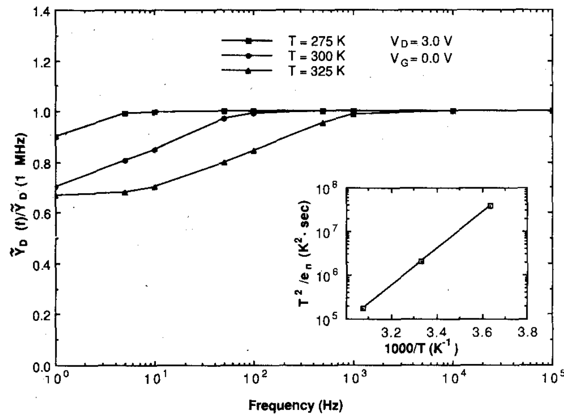


Fig. 8. Calculated output conductance versus frequency with different temperatures. The temperatures are 275, 300, and 325 K. The voltages and N_T/N_A are the same as those used in Fig. 2. The insert shows the temperature-dependent emission rate of EL2.

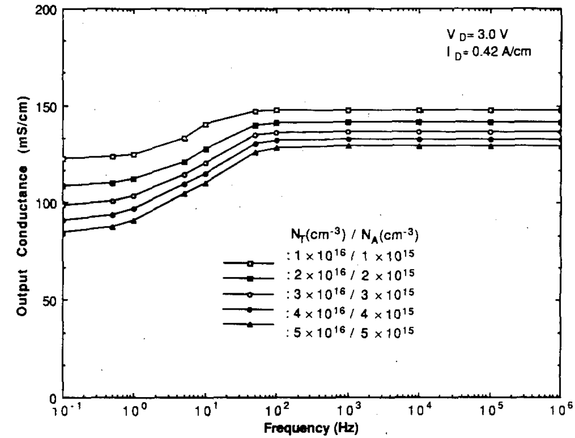


Fig. 9. Calculated output conductance versus frequency for five devices with different N_T/N_A. These N_T/N_A are ranged from 1×10^{16} cm^{-3}/1×10^{15} cm^{-3} to 5×10^{16} cm^{-3}/5×10^{15} cm^{-3}. The drain voltages are 3 V and these gate voltages are chosen so that these devices have the same current level ($I_D = 0.42$ A/cm).

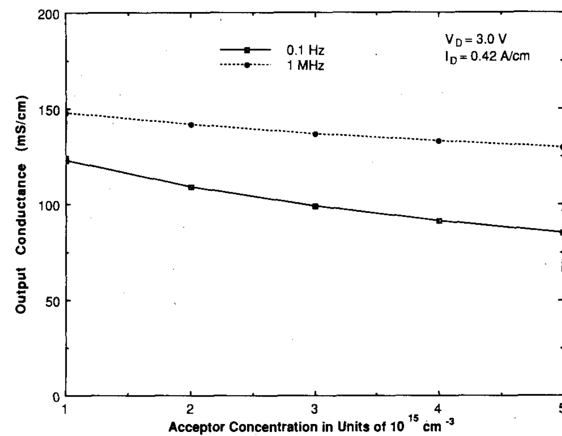


Fig. 10. Calculated output conductance versus acceptor concentration at 0.1 Hz and 1 MHz.

function of frequency at three different temperatures (275, 300, and 325 K) are shown in Fig. 8. The dc voltages and the N_T/N_A values are the same as those used in Fig. 2. The electron emission rate determined from (6) are 1.99 $\times 10^{-3}$, 4.3×10^{-2}, and 5.88×10^{-1} s^{-1} at $T = 275$, 300, and 325 K, respectively. From Fig. 8, as the temperature is increased from 275 to 325 K, the saturated frequency where the output conductance reaches its maximum shifts to higher values, and the shifts are about one order of magnitude for every 25 K increase in temperature. Lam *et al.* [7] and Golio *et al.* [8] have reported experimental results on the temperature-dependent behavior of the output conductance. The measured saturated frequency shifts with temperature agree well with our calculated results shown in Fig. 8. From the calculations, it is clear that the temperature dependence of the saturated frequency of the output conductance is related to the temperature-dependent emission rate of the bulk EL2 traps.

D. Effects of Impurity Concentration on Output Conductance

Five devices with the same N_T/N_A but different values of N_T and N_A are compared. These ratios are 1×10^{16} cm^{-3}/1×10^{15} cm^{-3}, 2×10^{16} cm^{-3}/2×10^{15} cm^{-3}, 3×10^{16} cm^{-3}/3×10^{15} cm^{-3}, 4×10^{16} cm^{-3}/4×10^{15} cm^{-3}, and 5×10^{16} cm^{-3}/5×10^{15} cm^{-3}. The temperature is 300 K and the dc drain voltage is 3 V. Because the magnitude of the output conductance is strongly dependent on the dc current level [7], [8], in order to make the comparison meaningful, the gate voltages of these devices were chosen so that they have the same dc drain current level. The drain current chosen is 0.42 A/cm and the corresponding gate voltages are −0.31, −0.2, −0.125, −0.06, and 0 V for the five devices. The calculated results are shown in Fig. 9. The output conductance decreases as N_T and N_A are increased. This phenomenon can be explained by the decreased substrate current which is a strong function of N_T and N_A [18]. For devices with higher N_T and N_A values, the substrate current in the semi-insulating layer is smaller, so the output conductance is lower. The calculated output conductance versus acceptor concentration at frequencies of 0.1 Hz and 1 MHz are shown in Fig. 10. The difference in output conductance at these two frequencies increases as N_T and N_A are increased. To give a better explanation for this phenomena, the two depth profiles of the ac amplitude of the electron concentration for $N_T/N_A = 1 \times 10^{16}$ cm^{-3}/1×10^{15} cm^{-3} and $N_T/N_A = 5 \times 10^{16}$ cm^{-3}/5×10^{15} cm^{-3} are shown in Fig. 11(a) and (b). The amplitude of the added ac drain voltage is 0.05 V. From these two figures, some interesting points can be pointed out. First, the positin of channel/substrate interface for the device with $N_T/N_A = 5 \times 10^{16}$ cm^{-3}/5×10^{15} cm^{-3} is shallower than for the device with $N_T/N_A = 1 \times 10^{16}$ cm^{-3}/1×10^{15} cm^{-3} because of the compensation of the channel

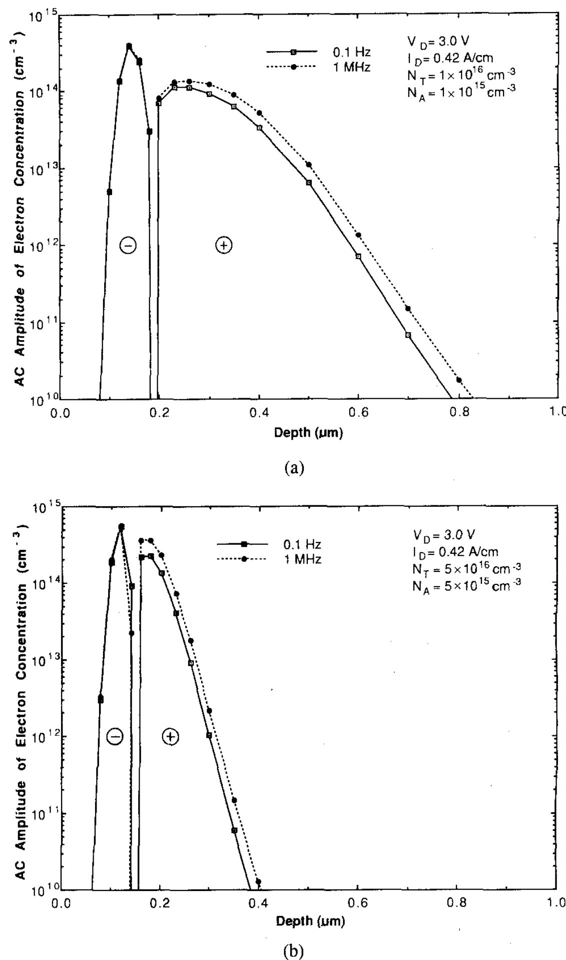


Fig. 11. Calculated ac amplitude of the electron concentration profiles along the gate edge on the drain side at frequencies of 0.1 Hz and 1 MHz for (a) $N_T/N_A = 1 \times 10^{16}$ cm^{-3}/1×10^{15} cm^{-3} and (b) $N_T/N_A = 5 \times 10^{16}$ cm^{-3}/5×10^{16} cm^{-3}.

doping by the increased acceptor concentration. Second, the ac perturbation of the electron concentration in the substrate side as shown in Fig. 11(a) is broader than that shown in Fig. 11(b). This explains why the devices with smaller values of N_T and N_A have larger output conductances. Third, from Fig. 11(a) in which the device has smaller values of N_T and N_A, the difference between the profile at 0.1 Hz and that at 1 MHz is insignificant. The two profiles in the channel side are almost indistinguishable. But as shown in Fig. 11(b) in which the device has higher values of N_T and N_A, there is significant difference both on the channel side and on the substrate side. The ratios of the largest ac amplitude of the electron concentration in the substrate at 1 MHz to that at 0.1 Hz are 1.63 and 1.24 for the device with $N_T/N_A = 5 \times 10^{16}$ cm^{-3}/5×10^{15} cm^{-3} and the device with $N_T/N_A = 1 \times 10^{16}$ cm^{-3}/1×10^{15} cm^{-3}, respectively. That explains why the shift of the output conductance is more severe for the devices with larger values of N_T and N_A. From the calculated relationship between the output conductance of GaAs MESFET's and their deep trap concentration and acceptor concentration, we clearly see the role of the substrate properties on the frequency-dependent behavior of the output conductance. In general, if the trap and the acceptor concentrations are higher, the output conductance is smaller but the shift of the output conductance at high frequencies is higher.

It has been shown that the short-channel effects in GaAs MESFET's can be reduced by having higher trap and acceptor concentrations [18]. Based on our analysis, higher trap and higher acceptor concentrations indeed give a lower output conductance of the MESFET. But, at the same time, the output conductance of the devices will have stronger frequency dependence. This is an unwanted effect, which can degrade the device and circuit performance. So there is a tradeoff between the two effects and the trap and the acceptor concentrations should be properly chosen to optimize the device performance.

V. Conclusion

Small-signal output conductance of ion-implanted GaAs MESFET's on semi-insulating substrates have been studied using two-dimensional numerical analysis. The effects of frequency, temperature, drain bias, and the trap and acceptor concentrations on the output conductance have been investigated. It is confirmed that the deep traps EL2 contribute significantly to the low-frequency behavior of the output conductance. The ac perturbations of the ionized trap concentration, the electron concentration, and the electrostatic potential occur around the Schottky depletion edge and the channel/substrate depletion region. The EL2 concentration and the background acceptor concentration play important roles in determining the output conductance and its frequency dependence. With higher trap and acceptor concentrations, the output conductance is smaller due to lower substrate currents, but has a higher frequency dependence due to more ionized electron traps.

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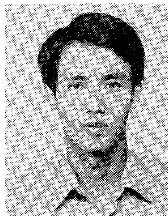

Shih-Hsien Lo (S'90) was born in Taiwan, Republic of China, in 1964. He received the B.S. degree in electrical engineering from National Cheng-Kung University in 1986 and the M.S. degree in electronics engineering from National Chiao-Tung University in 1988. Currently he is working toward the Ph.D. degree at the National Chiao-Tung University.

His research interests are in the areas of numerical modeling and electrical characterization of GaAs MESFET devices.

*

Chien-Ping Lee (M'80) received the B.S. degree in physics from the National Taiwan University in 1971 and the Ph.D. degree in applied physics from the California Institute of Technology, Pasadena, in 1978. While at Caltech, he worked on GaAs-based integrated optics.

He was credited with the design and fabrication of several important optoelectronic components, including the first integrated optoelectronic circuit, which consists of a laser and a Gunn device fabricated on a same substrate. After graduation, he joined Bell Laboratories, where he worked on integrated optics and semiconductor lasers. He joined Rockwell International in 1979 and worked on GaAs integrated integrated circuits. He did extensive work on substrate-related effects such as the orientation effect and the backgating effect. In 1982 he was promoted to be a Project Leader and later a Manager with responsibility for the development of ultra-high-speed integrated circuits using high-electron-mobility transistors. He received the Engineer of the Year award in 1982 for his contribution in GaAs IC and HEMT technologies. In 1987 he joined the National Chiao-Tung University, where he is now a Professor and the Director of the Semiconductor Research Center. He is also the director of the National Submicron Device Laboratory in charge of the construction of the first submicrometer device research center in the country. He is currently manager of the Advanced Device Concept Department in Rockwell's Science Center. His current research interests are in the areas of III-V optoelectronic devices, MBE technology, heterostructure devices and physics, and device simulation.