The GaAs IC based *pin*-FET receiver[6] was replaced by a calibrated power meter to make power measurements, and variable optical attenuators provided the system loss.

Power amplifier: For a mean transmitter power of +3·3 dBm, after the isolator, an amplified signal power of +17·4 dBm was measured at the output connector of the fibre amplifier. Fig. 4 shows the bit error rate of the system, both back-to-back and with the amplifier present. These curves indicate no

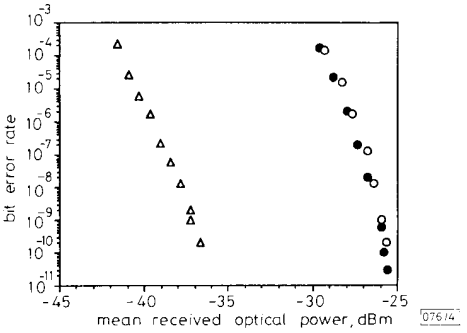

Fig. 4 *System BER against mean received optical power*
- ● back-to-back system
- ○ with power amplifier
- △ as preamplifier

significant amplifier associated degradation, a result consistent with the large post amplifier loss. Furthermore, these results demonstrate that transient changes in the gain due to signal saturation happen too slowly to cause any penalty for a 2·5 Gbit/s $2^{15}-1$ NRZ PRBS, despite the fact that the lifetime of the upper laser level of this transition is around 100 μs.

In-line amplifier (repeater): With the amplifier configured as shown in Fig. 2, attenuators *A* and *B* were adjusted to maximise the total system range. A link loss of 48·2 dB was achieved representing an increase in system range of approximately 19 dB over the unamplified system. Table 1 gives the system power budget at a bit error rate of 1 in 10^9.

To assess system sensitivity to amplifier input level, attenuators *A* and *B* were adjusted so that the gain of the amplifier was compressed by about 1 dB and the total received power for a 1 in 10^9 error rate was degraded by about 1 dB. The power budgets for both these cases are also shown in Table 1. This demonstrates that a 12 dB change in amplifier input signal level causes only a small change in the overall system performance.

Preamplifier: Fig. 4 shows the BER of the system with the amplifier configured as a preamplifier. The sensitivity, now measured at the input connector of the amplifier, was improved to −37·3 dBm (490 photon/bit). Accounting for input coupling losses we estimate an input to the doped fibre of −38·5 dBm (370 photon/bit). From measurements of the level of amplified spontaneous emission at the amplifier output, the signal-spontaneous beat noise limited noise figure was estimated to be around 5 or 6 dB. This is a reasonable value for a four-level amplifier, taking into account fibre background loss, splice loss and connector loss.

Table 1 POWER BUDGETS FOR IN-LINE AMPLIFIER

	Maximum system range	Gain compressed by 1 dB	Power penalty of 1 dB
Transmitter power [dBm]	+3·3	+3·3	+3·3
Attenuation A [dB]	15·3	9·3	21·2
Power into amplifier [dBm]	−12·0	−6·0	−17·9
Amplifier gain [dB]	19·3	18·1	19·7
Power out of amplifier [dBm]	+7·3	+12·1	+1·8
Attenuation B [dB]	32·9	38·0	26·6
Rx Power for 1 in 10^9 BER [dBm]	−25·6	25·9	24·8
System range (A + B) [dB]	48·2	47·3	47·8

Conclusions: A low-noise Pr^{3+}-doped fluorozirconate fibre amplifier has exhibited a gain of 24 dB at 1·3 μm for a launched pump power of around 800 mW at 1·01 μm. The 3 dB gain saturation output power was measured as +18 dBm, with a maximum output power of +20·5 dBm. A connectorised version of the amplifier was employed as a power amplifier, an in-line repeater and a preamplifier in a 2·488 Gbit/s system. As a power amplifier a maximum launched signal power of +17·4 dBm was obtained, with no measurable degradation to the receiver sensitivity. Operation as an in-line repeater allowed a 19 dB increase in range over the unamplified system. In a preamplifier format a receiver sensitivity of −37·3 dBm (490 photon/bit) was measured at the input connector to the amplifier. To the best of our knowledge, this represents the highest sensitivity for a direct detection receiver at this bit rate and wavelength.

These results indicate that the benefits, peculiar to fibre amplifiers, of high gain, low noise, highly-linear amplification and large saturated output power, are now available within the crucially important second telecommunications window around 1·3 μm.

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BANYAN NETWORK NONBLOCKING WITH RESPECT TO CYCLIC SHIFTS

Indexing terms: Codes and coding, Network theory

The nonblocking property of banyan network with respect to cyclic shifts is proved. The property is used to design a fair nonblocking copy network for multicast packet switching. The performance of the designed copy network is evaluated.

Introduction: Recently, banyan networks[1] have been adopted in constructing the switching fabrics for future integrated services digital networks.[2–3] Selfrouting, ease of fault diagnosis,

and suitability for VLSI implementation are the main reasons why banyan networks are so attractive. Besides, in large systems, banyan networks were shown to be more cost-effective than single-stage crossbar networks.[4] The performance of large banyan networks may not be acceptable, however, because of internal blocking. Fortunately, this unpleasant property can be removed if the banyan network is preceded by a sorter.

Many properties of banyan networks have been determined previously. For example, the regular SW banyan network with spread and fanout of 2 is isomorphic to many other interconnection networks such as the omega network, indirect binary n-cube network, and baseline network.[5] In this Letter, the nonblocking property of banyan network with respect to cyclic shifts is proved. This property is used to design fair switching networks.

Nonblocking property under cyclic shift: Consider an n-stage banyan network. Let the inlets and outlets be numbered from top to bottom by 0, 1, ..., and $2^n - 1$. In stage k, $0 < k < n$, there are 2^{k-1} remaining subnetworks. For convenience, label the switch nodes according to the Beckmann number scheme.[3] That is, a switch node in stage k is labelled by $(a_{n-k}a_{n-k-1} \cdots a_1, b_n b_{n-1} \cdots b_{n-k-2})$ so that $a_{n-k}a_{n-k-1} \cdots a_1$ denotes the label of the switch node numbered from the top within the subnetwork and $b_n b_{n-1} \cdots b_{n-k-2}$ represents the label of the subnetwork numbered. Fig. 1 illustrates this numbering scheme for a four-stage banyan network. According to

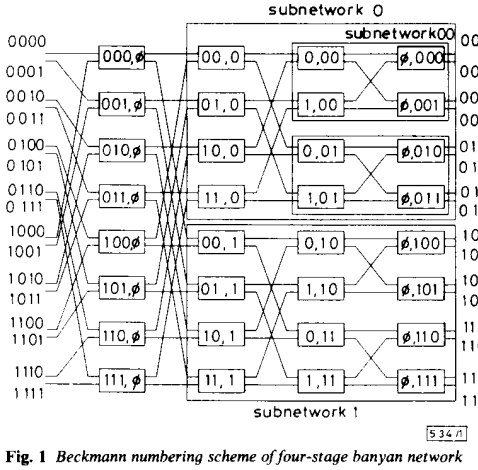

Fig. 1 *Beckmann numbering scheme of four-stage banyan network*

the connection pattern of banyan network, the node $(a_{n-k}a_{n-k-1} \cdots a_1, b_n b_{n-1} \cdots b_{n-k-2})$ in stage k is connected to the node $(a_{n-k-1} \cdots a_1, b_n b_{n-1} \cdots b_{n-k-1})$ in stage $k+1$ via the output link b_{n-k-1} (0 or 1). Furthermore, the path $\langle x, y\rangle$ connecting inlet $x = a_n a_{n-1} \cdots a_1$ to outlet $y = b_n b_{n-1} \cdots b_1$ passes through nodes $(a_{n-1} \cdots a_1, \phi)$, $(a_{n-2} \cdots a_1, b_n)$, $\cdots$ and $(\phi, b_n \ldots b_2)$.

The inlets of an n-stage banyan network are said to be cyclically shifted by an offset of l if inlet i is connected to outlet $(i + l) \bmod 2^n$ for $i = 0, 1, \ldots, 2^n - 1$. Fig. 2 illustrates a cyclic shift by an offset of 3 for a four-stage banyan network. We shall prove in the following that banyan network is nonblocking with respect to cyclic shifts.

If $l = 0$, i.e. inlet i is connected to outlet i for all i, then the banyan network is clearly nonblocking because it satisfies the concentration and monotone conditions stated in Reference 3. Suppose $l \neq 0$. Without loss of generality, assume inlet $x = a_n a_{n-1} \cdots a_1$ is connected to outlet $y = b_n b_{n-1} \cdots b_1$. Let $x' = a'_n a'_{n-1} \cdots a'_1$ be another inlet and $d = d_n d_{n-1} \cdots d_1$ be the distance from x to x', i.e. $x' = (x + d) \bmod 2^n$. Because cyclic shifts are investigated, x' must be connected to $y' = b'_n b'_{n-1} \cdots b'_1 = (y + d) \bmod 2^n$.

Consider the two paths $\langle x, y\rangle$ and $\langle x', y'\rangle$. If these two paths are node-disjoint, i.e. there is no switch node passed through by both paths, then $\langle x, y\rangle$ and $\langle x', y'\rangle$ cannot block each other. Suppose these two paths meet at a switch node in stage k, i.e. $(a_{n-k}a_{n-k-1} \cdots a_1, b_n b_{n-1} \cdots b_{n-k+2}) = (a'_{n-k}a'_{n-k-1} \cdots a'_1, b'_n b'_{n-1} \cdots b'_{n-k+2})$. It is clear that

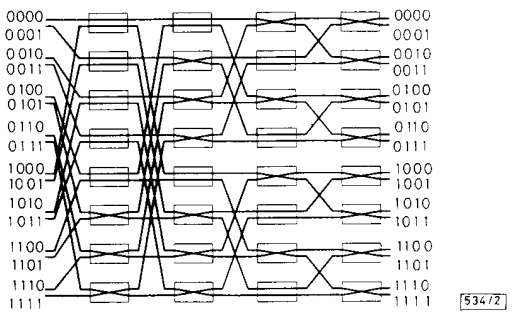

Fig. 2 *Cyclic shift by offset of 3 in four-stage banyan network*

$a_{n-k}a_{n-k-1} \cdots a_1 = a'_{n-k}a'_{n-k-1} \cdots a'_1$ implies $d_1 = d_2 = \cdots = d_{n-k} = 0$. Furthermore, $b_n b_{n-1} \cdots b_{n-k+2} = b'_n b'_{n-1} \cdots b'_{n-k+2}$ implies $d_{n-k+1} = 1$ (otherwise $d_i = 0$ for $i = 1, 2, \ldots, n$ and thus $x = x'$). As a result, y'_{n-k+1} and y_{n-k+1} are different because $y'_{n-k+1} = y_{n-k+1} + d_{n-k+1}$. Therefore, the two paths $\langle x, y\rangle$ and $\langle x', y'\rangle$ will not use the same output link of the switch node. In other words, $\langle x, y\rangle$ and $\langle x', y'\rangle$ cannot block each other. This completes the proof.

Applications: The above nonblocking property of the banyan network can be used to design fair switching networks. In particular, let us consider the multicast packet switch proposed in Reference 3. The multicast packet switch consists of two components, namely a nonblocking copy network and a point-to-point routing network (a Batcher-banyan network). The nonblocking copy network consists of a running adder, a dummy address encoder, and a broadcast banyan network. If a top–down (bottom–up) running adder is adopted, then the lowest (upmost) inlet suffers the worst performance. It can be seen from the performance curves plotted in Reference 3 that unfairness may cause the performance of the least priority inlet unacceptable even for a small switching system.

To make the copy network become fair for all the inlets, a banyan network performing cyclic shifts can be placed in front of it. Notice that the banyan network cyclically shifts the inlets by an offset of $j \bmod 2^n$ in the jth slot. Fig. 3 illustrates the resulting switching system with eight inlets and outlets.

Let us now evaluate the performance of the proposed fair nonblocking copy network. Let $P_L(i)$ denote the packet loss rate of the ith inlet when a top–down running adder is adopted and no cyclic shift is performed. It is not hard to see that the packet loss rate of the proposed fair nonblocking copy network is equal to $\sum_{i=0}^{N-1} P_L(i)/N$, where $N = 2^n$. Fig. 4 compares the packet loss rate of the fair nonblocking copy network with that of the least priority inlet when no cyclic shift is performed. The comparison is made assuming there are 64 inlets. The least priority inlet is considered because it usually requires that the loss rate of packets generated by each inlet is below a predetermined threshold in designing a packet

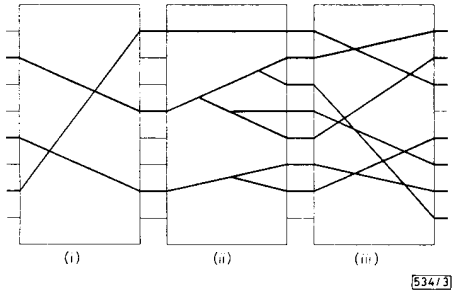

Fig. 3 *Fair multicast packet switch with eight inlets and outlets*

(i) Banyan network for cyclic shift
(ii) Nonblocking copy network
(iii) Point-to-point routing network

switch. For simplicity, it is assumed that each inlet generates packets independently with identical rate ρ. Furthermore,

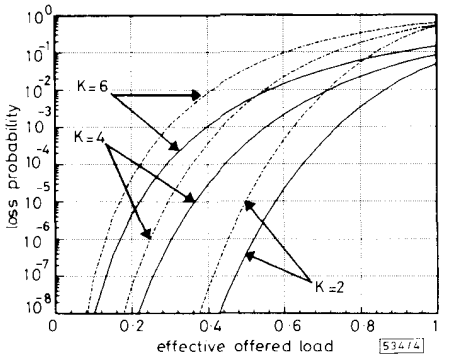

Fig. 4 *Performance of fair nonblocking copy network*
——— fair copy network
—·—·— least priority inlet

every broadcast packet requests a constant number of copies, say K. Under the above assumptions, $P_L(i)$ can be enumerated easily; in fact

$$P_L(i) = \sum_{j=[N/K]}^{i} \binom{i}{j} (1-\rho)^{i-j}\rho^j$$

where $[N/K]$ is the integer part of N/K. Because the number of copies requested by each broadcast packet is equal to K, the effective offered load is given by ρK. From Fig. 4 it can be seen that, under a fixed effective offered load, the packet loss rate increases as K increases. Moreover, with respect to the least priority inlet, adding the proposed fairness mechanism results in an order of magnitude decrease in the packet loss rate. The decrease is even larger if there are more inlets.

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PRECISE DETERMINATION OF OPEN CIRCUIT CAPACITANCE OF COPLANAR PROBES FOR ON-WAFER AUTOMATIC NETWORK ANALYSER MEASUREMENTS

Indexing terms: Calibration, Probes, Measurement

When coplanar probes are used, the open circuit reflection standard in the SOLT calibration technique is usually the most questionable of the four. This standard is described in the 'cal kit' as a capacitance, the value of which is determined in a 'cut and try' way. A more direct method is proposed in this Letter.

Introduction: The SOLT calibration technique makes use of four standards: a short, an open, a load and a through. It allows compensation for the 12 systematic error vectors of the ANA. The correctness of this compensation relies on the reproducibility of the measurements made from the standards, and on the accuracy of the standards definition ('cal kit'). An inaccurate cal kit will result in inaccurate error vectors and therefore in poor S-parameter measurements.

Using a preliminary calibration with an approximate C_{open} entered in the cal kit, we measure the S parameters of a long length of coplanar line terminated in an open circuit (long open stub). A model of this stub must be available, but the exact values of the elements need not be known. Taking into account the effect of an inaccurate cal kit on the measurement result, an optimisation method is used to determine the exact value C^0_{open} of C_{open}. The characteristics of the line (impedance, length, propagation constant) are also precisely determined.

Error vectors affected by inaccurate cal kit: To determine the exact capacitance C^0_{open} of each probe, we consider a pure reflection preliminary calibration (1 port) and measurement of the S_{11} parameter of an open line. The error vectors are: e_d the directivity error, e_r the tracking error, and e_s the source match error. The short circuit and load are entered in the cal kit as ideal standards. The 'open' standard has an exact reflection coefficient Γ^0_{open} (unknown) and this is entered in the cal kit as an approximate value Γ_{open} (modelled as capacitance C_{open}). The calibration process uses three uncorrected S_{11} measurements on the three standards: load (M_1), short (M_3), open (M_4).[2] The three error vectors are then calculated. The vector e_d depends only on the load and therefore is not affected by the approximate Γ_{open}. The approximate vectors e_s and e_r depend on M_1, M_3, M_4 and Γ_{open}.

$$e_s = \frac{M_1 - M_3}{M_3 - M_4} + \frac{M_1 - M_4}{M_3 - M_4}\left(\frac{1}{\Gamma_{open}}\right) \quad (1)$$

$$e_r = \frac{(M_1 - M_3)(M_1 - M_4)}{M_3 - M_4} + \frac{(M_1 - M_3)(M_1 - M_4)}{M_3 - M_4}\left(\frac{1}{\Gamma_{open}}\right) \quad (2)$$

If the true value Γ^0_{open} is entered in the cal kit, e^0_s and e^0_r, the true values of e_s and e_r, are obtained. The differences Δ_{es} and Δ_{er} between approximate and true error vectors are

$$\Delta e_s = e_s - e^0_s = \frac{(M_1 - M_4)}{M_3 - M_4}\left(\frac{1}{\Gamma_{open}} - \frac{1}{\Gamma^0_{open}}\right) \quad (3)$$

$$\Delta e_r = e_r - e^0_r = \frac{(M_1 - M_3)(M_1 - M_4)}{M_3 - M_4}\left(\frac{1}{\Gamma_{open}} - \frac{1}{\Gamma^0_{open}}\right) \quad (4)$$

From eqns. 3 and 4 we see that the differences Δ_{er} and Δ_{es} are linked together.

$$\Delta e_r/\Delta e_s = M_1 - M_3 \quad (5)$$

Eqns. 1 and 2 show that

$$\frac{e_r}{1 + e_s} = \frac{e^0_r}{1 + e^0_s} = M_1 - M_3 \quad (6)$$

If follows from eqns. 3–6 that

$$\frac{\Delta e_r}{e^0_r} = \frac{\Delta e_s}{1 + e^0_s} = \frac{\Gamma^0_0}{(1 + \Gamma^0_{open})} \times \left[\frac{1}{\Gamma_{open}} - \frac{1}{\Gamma^0_{open}}\right] \quad (7)$$

the value of which depends solely on Γ_{open} and Γ^0_{open}.