

Fig. 3. Magnitude of spectral components of (12) versus harmonic number using: (a) Sampled true Fourier transform, times 1/T, (b) Original EFFFT method [1], (c) De-aliased version of (b), (d) the same as (c) except that the spectral components of a ramp between $t_s - \Delta t$ and t_s has been subtracted.

ponents of a ramp that rises to value U_s between n = 199 and n = 200.

$$U_{s}[(t-t_{s}+\Delta t)/\Delta t][u(t-t_{s}+\Delta t)-u(t-t_{s})].$$
 (13)

where $\Delta t = T/N$. The components to be subtracted are the sampled true Fourier transform of (13) times 1/T, or

$$U_{s} \exp \left(-j\omega_{n}t_{s}\right) \left\{ \frac{\left[1-\exp \left(j\omega_{n}\Delta t\right)\right]}{\omega_{n}^{2}T\Delta t} - \frac{1}{j\omega_{n}T} \right\}. \tag{14}$$

The result is shown in Fig. 3(d) and the maximum deviation of curve (d) from (a) is 0.43 dB. This remaining error is due to the piecewise linear approximation model not being perfect.

IV. DISCUSSION AND CONCLUSIONS

It has been shown that frequency aliasing errors introduced during the FFT analysis of step-like signals can be substantially decreased by a simple de-aliasing procedure. For example, the results shown in Fig. 2(c) were obtained with a de-aliased version of the original EF-FFT method, namely by postmultiplication of the original EF-FFT results with $\sin^2(n/N)$. Of course de-aliasing with (9) does not mean removing all alias error because to do so would mean that the function is precisely known between sample points. Rather, use of (9) implies that a piecewise linear approximation is acceptable between data points. To obtain even more accurate final spectra it would be necessary to increase the sampling rate or to use a quadratic or higher order curve-fitting procedure in the dealiasing technique [5], [6], [9].

The attractive features of the aliasing error reduction method introduced here, compared to increasing the sampling rate, are that data reacquisition is not required, computer requirements are small, and the spectra are of high accuracy up to the Nyquist frequency. The applicability is limited to functions that can be modeled with linear transitions between data points, as opposed to step transitions unless the precise timing and shape of the step transitions are known. Since most data sets are comprised of samples from slowly varying analog signals, the de-aliasing procedure provides enhanced spectral accuracy with but minor additional mathematical complexity.

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A Real-Time C-V Measurement Circuit for MOS Capacitors Under Current Stressing

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Abstract—A dynamic large signal C-V measurement circuit is presented to measure real time C-V characteristics of a MOS structure under current stressing conditions. The real time information on the generation and filling of traps and surface states can thus be obtained. With this circuit it has been shown that, for an Al-gate MOS structure, charges on traps and interface surface states recover immediately after the stressing is removed.

I. Introduction

As very large scale integration (VLSI) technology advances, metal-oxide-semiconductor (MOS) devices keep shrinking their dimensions, not only on the channel length and the source and drain regions, but also on the thickness of the gate dielectric. For example, 16-Mb dynamic random access memories (DRAM) require an oxide thickness of 12.5 nm for the gate dielectric [1], and 1-Mb electrically erasable programmable read only memories (EE-PROM) use oxynitride as the tunneling dielectric [2]. As a result, one of the key requirements for making high density MOS VLSI

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devices is to make high yield and reliable gate dielectrics. Much work had been devoted to study the oxide breakdown mechanism since oxide breakdown is one of the main causes for integrated circuit failures [3]-[8]. For these results, oxide was sandwiched into a MOS capacitor structure, and it was then either constant voltage- or current-stressed and its capacitance-voltage (C-V) and current-voltage (I-V) characteristics measured. The C-V and I-Vcharacteristics obtained can reveal the generation and filling of oxide traps and interface states [3]-[6], [8]. It has been generally recognized that the generation and filling of traps and interface states plays an important role in determining the reliability of oxides [4], [5]. However, in these studies, the C-V characteristics measured were not real time ones. That is, the device was stressed and then considerable time elapsed before its C-V characteristics were measured. During this time lapse some of the trapped charges recover. As a result, the charge trapping information obtained was representative of the instantaneous distribution.

In this paper, a real-time C-V measurement circuit is presented for MOS capacitors which are under constant current stress. For this system, the MOS device is kept current-stressed and its stressed C-V characteristics can be measured instantaneously when desired. The charge filling information on oxide traps and surface states can be obtained in real time during the stressing process even to the point of capacitor breakdown.

II. DESCRIPTION OF THE CIRCUIT

The block diagram of the measuring circuit is shown in Fig. 1, where DUT is the MOS capacitor to be measured. During the stressing period, the waveform generator is set to give a voltage, V_{st} , which is large enough to keep D1 off, and the constant current I stresses the DUT capacitor. The voltage obtained at V_{01} is the terminal voltage across the DUT capacitor. When the C-V characteristic is to be measured, the waveform generator is triggered to give a negative-going "sampling" triangular wave. Since OP1 is a half-wave voltage follower, the voltage at V_{01} also becomes a negative-going triangular wave. This causes a displacement current $i = C(dV_1/dt)$ to flow through the DUT capacitor. The output of OP2, V_{02} (= αRC , where α is the slope of the negative-going triangular wave), is proportional to the magnitude of the DUT capacitor. Both outputs, V_{01} and V_{02} , can be fed to digital sampling oscilloscopes for waveform display or later data processing. The MOS capacitor can be stressed in either polarity. When the MOS capacitor stressed in the reverse polarity (i.e., the device is stressed with the semiconductor in the inversion condition), the C-V measurement of this system is similar to that of the quasi-static C-V technique [9]. To measure the C-V characteristic during the sampling period, the sweep rate of the negative-going triangular wave should be slow (in general, slower than 0.05 V/s) in order to keep the MOS capacitor in the quasic state equilibrium condition. However, when the DUT capacitor is stressed in the positive polarity (i.e., the device is stressed with the semiconductor in the accumulation condition), the sweep rate of the triangular wave can be as high as the slew rates of the amplifiers allow.

III. MEASURMENT RESULTS

To show the differences between C-V curves measured by this circuit and by a conventional LCR meter, Fig. 2 shows C-V curves for an Al-gate 200 Å oxynitride MOS capacitor stressed at a constant current of $4.2 \cdot 10^{-5}$ A/cm² for 0, 15 s, and 3 min as measured by this circuit and by a conventional LCR meter (at 1 MHz). For the LCR meter measurement, 30 s-1 min time interval had elapsed due to connection of wires and meters and the measurement

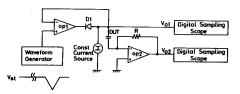


Fig. 1. The block diagram of the real time stressing and C-V measurement circuit.

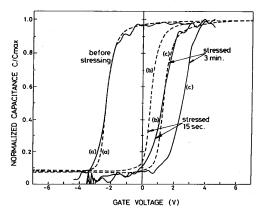


Fig. 2. The C-V characteristics of two of the same oxynitride MOS capacitors after they were stressed for (a) 0 (b) 15 s and (c) 3 min as measured by the real-time measurement system (solid curves) and by a conventional LCR meter at 1 MHz (dashed curves).

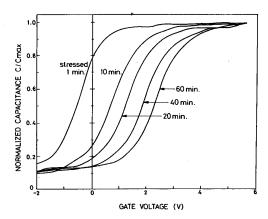


Fig. 3. The successive C-V characteristics of an MOS capacitor after it was stressed for 1, 10, 20, 40, and 60 min to breakdown. No significant distortion on the successive C-V curves is observed.

was done at 1 MHz. It is seen that the *LCR* curves always stay at the left of their respective real-time curves. This means the trapped charges electrons in the stressed oxide recovered during the time for connecting wires and meters.

The circuit can continuously measure the C-V curves of a MOS capacitor, either as it is under stressing or after stressing. Fig. 3 shows a series of C-V curves successively measured on a MOS capacitor stressed at a constant current to the point where the capacitor was about to break down. When breakdown of the device

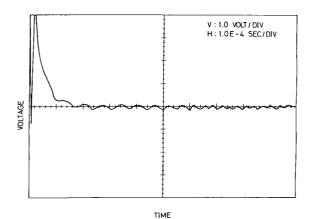


Fig. 4. The waveform observed at V_{02} at the instant that the capacitor went to breakdown.

occurred, the waveform of Fig. 4 appeared at V_{02} . From these two figures, it can be confirmed that oxide breakdown under stressing is a sudden phenomenon and that it is caused by charge trappings in the oxide since the shape of the the C-V curve near breakdown did not differ from the unstressed curve not only shifted horizontally [5]. The peak of the waveform of Fig. 4 indicates that a transient of current flowed through the oxide at the instant of breakdown, and after that the device was open.

IV. Conclusion

In this paper, a C-V measurement circuit for an MOS capacitor under current stressing has been presented. The circuit is simple, yet, able to measure the C-V curves in real time. Because of this, the instantaneous charge filling on traps and surface states can be observed. Using this system, it has been shown that for Al-gate, MOS structures, charges on traps or interface surface states recover immediately after removal of the current stress. It has also been demonstrated that the breakdown of the oxide is a sudden phenomenon and is caused mainly by charge trapping in the oxide.

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Single Op-Amp Sinusoidal Oscillators Suitable for Generation of Very Low Frequencies

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Abstract-This paper presents some op-amp-based single-elementcontrolled sinusoidal oscillator structures which can generate very low frequencies (VLF). They do not have the drawbacks of the previously known op-amp oscillators proposed for VLF generation and yet, require only a single op-amp along with a few RC elements.

I INTRODUCTION

Very low frequency (VLF) oscillators are required in many biomedical, geophysical, and control instrumentation systems. In the last decade, a large number of op-amp-based single-resistancecontrolled oscillators (SRCO) have been presented in the literature, see [1]-[9], [11]-[13], and the references cited therein. Many of these circuits have the facility for generating VLF oscillators in either of the following two ways.

a) In some of the above-mentioned oscillators, the expression for the frequency of the oscillations is of the type

$$f = \frac{[1 - n]^{1/2}}{2\pi RC} \tag{1}$$

where n is the frequency-controlling resistor ratio. Such oscillators can generate VLF oscillations by making the parameter n close to 1. The sensitivity of f with respect to the parameter n is given by

$$S_n^f = \frac{n}{f} \frac{\partial f}{\partial n} = -\frac{n}{2(1-n)} \tag{2}$$

which will be quite large when (1 - n) is small. Thus all VLF oscillators, which rely upon a difference term (as in (1)) to generate very low frequencies, suffer from the drawback of having frequency sensitivities that are very high.

b) The other approach to generate VLF oscillations is to devise oscillator structures having resistive scale-factors in the expression for f in the form:

$$f = \frac{[k]^{1/2}}{2\pi RC} \tag{3}$$

so that the frequency can be scaled down by making the frequencycontrolling resistor ratio k small. Such VLF oscillators do not have

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