Focal-Plane-Arrays and CMOS Readout Techniques of Infrared Imaging Systems

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Abstract— **A discussion of CMOS readout technologies for infrared (IR) imaging systems is presented. First, the description of various types of IR detector materials and structures is given. The advances of detector fabrication technology and microelectronics process technology have led to the development of large format array of IR imaging detectors. For such large IR FPA's which is the critical component of the advanced infrared imaging system, general requirement and specifications are described. To support a good interface between FPA and downstream signal processing stage, both conventional and recently developed CMOS readout techniques are presented and discussed. Finally, future development directions including the smart focal plane concept are also introduced.**

Index Terms— **Detector, focal plane array, infrared imaging, readout circuit, thermal image.**

I. Introduction

SINCE the 1950's, the infrared (IR) imaging system technology has been developed for various applications including IR search and track, medical examination [1], astronomy [2], [3], forward-looking infrared (FLIR) systems, missile guidance, and other strategic equipment [4], [5]. Recently, a dual-use technology concept has been proposed which emphasizes the integration of commercial and military IR imaging systems to meet both economic and defense challenges [6]. This concept has led to the increasing research and development efforts in applying the commercial CMOS very large scale integration (VLSI) technologies in the design of IR imaging systems. Incorporating the rapid advancement in CMOS VLSI with the progress in infrared focal-plane array (IR FPA) technologies like detector material, sensing structure, optics, coolers, readout electronics, image enhancement, and intelligent signal processing results in the revolution of IR image systems to a new generation with significant performance improvement.

In general, the IR FPA can be divided into two major parts, namely the detector array and the readout electronics. As compared to the conventional discrete design, the IR FPA has the inherent advantages of high packing density, low cost, reduced signal leads through the dewar, high feasibility on-chip signal processing, and high flexibility for system integration. In the high-sensitivity applications, the IR FPA's are typically fabricated with narrow bandgap semiconductor detectors and silicon multiplexer and operated in the cryogenic environment. Thus, very challenging technologies for detection materials and system interface are required. Moreover, high-performance and low-temperature mixed-mode circuit design are also required for the readout electronics [7]. To achieve the optimal overall performance of the IR FPA's, suitable tradeoff among circuit performance, power dissipation, chip area, and image resolution should be made. A number of readout structures have been developed for different system applications and concerns.

In this paper, the CMOS readout techniques for IR image system are presented and discussed. The IR detector materials and structures for used in thermal image are described in Section II. In Section III, the architectures and operational requirements of IR FPA are discussed. In Section IV, the CMOS readout techniques for IR detectors are discussed including the state-of-the-art structure. In Section V, future directions for IR sensor readout are presented. Finally, a summary is given.

II. Infrared Detectors for Use in Thermal Imaging

All real objects are thought to exist at temperatures above absolute zero, which means that the thermal radiation exists always. The infrared radiation which is detected just above the visible spectrum was found in 1900 as a function of temperature and wavelength [8]. Since then, various infrared detectors have been developed to convert incident infrared radiation, directly or indirectly, into electrical signals. Among these detectors, two major classes known as photon detectors and thermal detectors are discussed here.

In the photon detectors, photons are converted directly into free current carriers by photoexciting electrons across the energy bandgap of the semiconductor to the conduction band. This produces a current, voltage, or resistance change of the detectors. The photoexcitation is caused by the sufficiently short wavelength radiation interacting directly with the lattice sites. Therefore, the temperature of the detector must be low enough so that the number of carriers thermally excited across the bandgap is less significant. To maintain a low temperature, the cooling system or the dewar is required, which increases the system cost. Generally, the sensitivity of photon detectors depends on the spectral absorption and photoexcitation. The spectral response of photon detectors depends on the energy

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TABLE I
GENERAL PROPERTIES OF PHOTON AND THERMAL DETECTORS

Parameter	Photon Detector	Thermal Detector
Response time	Fast	Slow
Spectral responsively	Narrow and selective	Wide and flat
Sensitivity	High	Low
Operating temperature	Cryogenic	Room
Cost	Expensive	Economical
System requirement	Cooling System	Optical Chopper

gap of the semiconductor as well as the optical radiation wavelength.

In the thermal detectors, the incident radiation absorbed by the crystal lattice leads to a temperature change which changes the physical or electrical property of the detector. Most thermal detectors are operated at room temperature and have a wide spectral response. Since the operation of thermal detectors involves a change in temperature, they have a inherently slow response and a relatively low sensitivity compared to photon detectors [9]. The response time and sensitivity of a thermal detector are influenced by the heat capacity of detector structure as well as the optical radiation wavelength. In some applications of thermal detectors, an optical chopper is also needed [10], [11]. Some comparisons between photon detectors and thermal detectors are summarized in Table I.

In the following subsections, the most commonly used IR radiation sensing structures of photon detectors in arrays, namely, photovoltaic detectors, photoconductive detectors, and Schottky barrier detectors are described. Moreover, two mostly used structures of thermal detectors, pyroelectric detectors and bolometers, are also discussed.

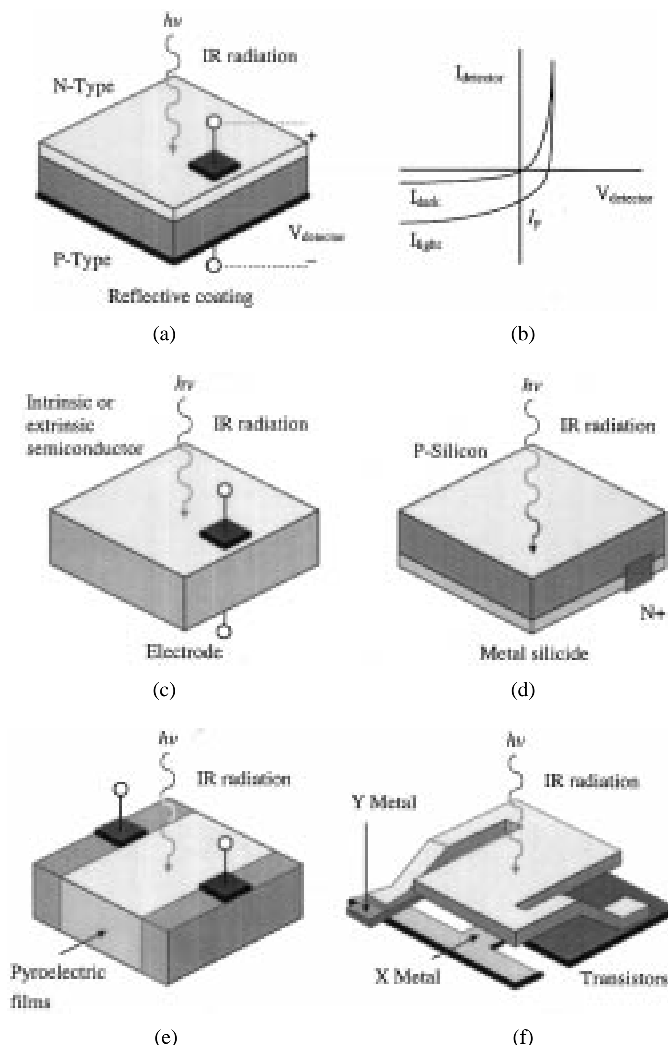

Fig. 1. (a) The device structure of photovoltaic detector, (b) the I–V curve of the PV detector, (c) the device structure of the photoconductive detector, (d) the device structure of the Schottky barrier detector, (e) the device structure of the pyroelectric detector, and (f) the device structure of the bolometer.

A. Photovoltaic (PV) Detectors [12]–[14]

The structure of a photovoltaic (PV) detector is based on a P–N junction device as shown in Fig. 1(a). The reflective coating on the bottom of the detector provides the double chances (injection and reflection) of photon absorption. Under the IR radiation, the potential barrier of the P–N junction leads to the photovoltaic (PV) effect. An incident photon with the energy greater than the energy band gap of the junction generates electron-hole pairs and the photocurrent is excited. The resultant I–V curve of the PV detector when exposed to IR radiation is similar to that of normal P–N junction device but shifted downward as shown in Fig. 1(b). The amount of the photon excited current is denoted by I_p, the photocurrent. Normally, the photovoltaic detector is operated under zero or near zero biasing condition to obtain a large output shunt resistance without the device breakdown treat. The output shunt resistant of PV detectors is expressed as R_oA where R_o is the shunt resistance normalized to the detector area A under zero bias. Generally, high value of R_oA is an important requirement for PV detectors to achieve a good sensitivity and a good input injection. Due to the zero biasing condition of PV detectors, the power consumed is nearly zero and the heat generation problem can be avoided.

The thermal noise and the $1/f$ noise are the major noise sources of the PV detector, which degrade the detector performance. The ultimate performance of an ideal detector is defined as the background-limit-IR-performance (BLIP) [15], which is only affected by the photon noise due to the fluctuation of the incident optical radiation. All other noises in detectors should be kept below the photon noise to achieve the BLIP performance. In long-wavelength IR (LWIR) detection, the fabrication of the low-noise PV detector using narrow bandgap materials is quite challenging [16], [17].

B. Photoconductive (PC) Detectors [12], [18]

The mechanism of photoconductive (PC) detectors is to produce the conductance change under the IR radiation. In PC detectors, the increase of the conductance of photoconductive material under an applied constant electric field is caused by the free carriers generated by the photon energy. The structure of PC detectors is shown in Fig. 1(c). The detector material

can be either an intrinsic or an extrinsic semiconductor. The spectral response of a semiconductor material can be controlled by the doping of the intrinsic semiconductor to make PC detectors applicable in LWIR detection [16], [19]. In the case of intrinsic semiconductor, the incident IR radiation is absorbed to generate holes and electrons. In the case of extrinsic semiconductors, the photon energy is absorbed by the impurity, and only the majority carriers are excited. Under the applied constant bias, the resultant current level is proportional to the incident photon flux.

In PC detectors, the photoconductive gain is defined as the ratio of carrier lifetime to detector transit time. The gain usually varies from 0.5 to greater than unity. If carrier lifetime is longer than transit time, the free carriers can transit cross the detector without recombination and the current gain is greater than one. Since the current flows under a constant electric field, the photoconductive detector consumes power and generates heat. This makes it not suitable for large IR array applications. Moreover, an additional noise source called the generation-recombination noise exists in PC detectors besides the thermal and the $1/f$ noise sources.

C. Schottky Barrier Detectors [20]–[22]

The structure of Schottky barrier detectors with the silicide (PtSi) thin film which can be fabricated by using the conventional CMOS process is shown in Fig. 1(d). The IR radiation photons injected from the backside of the silicon substrate are absorbed in the silicide layer. Fractions of the excited carriers are emitted over the Schottky barrier into the silicon. Since the carrier recombination can be avoided due to the Schottky barrier, charges are accumulated in the silicide layer. The accumulated charges can be transferred out through a structure like the charge-coupled device (CCD). Due to the process compatibility of Schottky barrier detectors with CMOS, it is easy to merge detector arrays with readout circuits and other VLSI circuits or systems monolithically [23], [24]. The problems of bonding and hybrid process can be solved in high-density IR FPA applications [25]. However, low quantum efficiency and low spectral response limit the applications of Schottky barrier detectors on the medium wavelength IR (MWIR) image detection [22]. Recently, new technology of Schottky barrier detectors for LWIR have been under development [26].

D. Pyroelectric Detectors [27], [28]

The basic structure of the pyroelectric detector is shown in Fig. 1(e). The pyroelectric material is a special dielectric material with spontaneous and permanent polarization. In the pyroelectric material, the change of dielectric constant is proportional to the temperature dependent spontaneous polarization. When IR radiation is incident and absorbed, the resultant heating makes a change in electrical polarization which causes charges to flow to the connected external readout circuit. Since the polarization is temperature dependent, a chopper is needed to cut the heat source, i.e., the photon flux and reset the polarization condition. Some techniques have been proposed to improve the influence of nonideal chopper effect on the nonuniformity in uncooled pyroelectric staring array systems [10], [11]. The ambient operating temperature and the flat spectral response make the pyroelectric detector useful in some IR image detection applications. However, slow response time and low sensitivity result in the limitation on readout performance. New process technology, new material, and improved structure of pyroelectric detectors are under development to improve performance of pyroelectric detectors [29]–[31].

E. Bolometer Detectors [32], [33]

The operating principle of bolometer detectors is that the temperature change caused by the absorption of IR radiation leads to a change in electrical resistance of the material. Unlike the photoconductive detectors, the resistance change in bolometer detectors is caused directly by the heating of material instead of direct photon-lattice interaction and carrier generation. The general detector structure of bolometer detectors using the micromaching technology is shown in Fig. 1(f). The X–Y metals are used as interconnection tracks and the transistor switch beneath each pixel enables addressing. As a thermal detector, larger conductivity in bolometer detectors ensures faster response but higher temperature change which lowers the sensitivity. This makes a tradeoff on the structure design of bolometer detectors. The application of superconducting materials on bolometer detectors is also under development. The dramatic resistance change versus temperature in superconducting materials leads to a high sensitivity of bolometer detectors [34]–[36].

III. Structures and Operational Requirements of IR FPA

A. IR FPA Structures

Recently, the development of IR FPA technologies has made the design of high-sensitivity, high-density, large-format, and high-spectral-resolution IR image systems quite feasible. Moreover, the progress on VLSI techniques and detector fabrication technologies dramatically reduce complexity and cost of IR systems. The application of various developed technologies on the design of IR FPA's has resulted in the advantages of simplified electrical interconnection, reduced signal number leads through the dewar, higher performance reliability, and simplified package. Some commonly used structures of the three major classes of IR FPA's, namely, hybrid array, monolithic array, and pseudomonolithic array, are discussed below.

1) Hybrid Array: The most commonly used IR FPA structures in the hybrid array [37] are flip-chip and Z-plane technologies [38] as shown in Fig. 2(a) and (b), respectively. In Fig. 2(a), the IR detector array chip and silicon readout chip are compounded by the indium bump grown on the aligned pixels of both chips. This is the most used structure in the hybrid array technology. In the Z-plane technology shown in Fig. 2(b), the readout chips are stacked one on top of another and then the detector array is mounted to the third-dimensional plate on the edge. In the Z-plane structure, one readout chip is

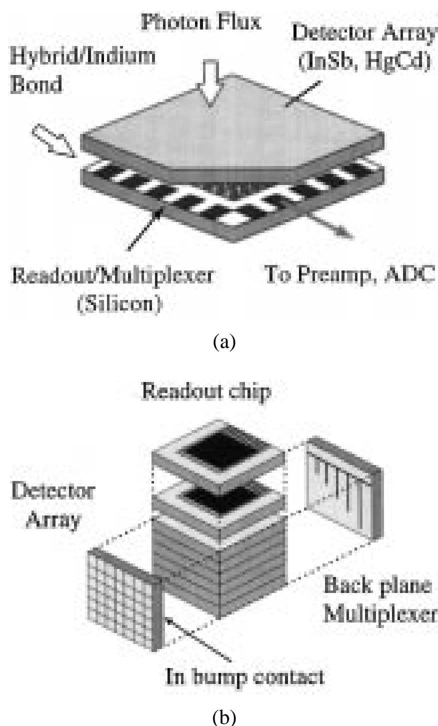

Fig. 2. The technologies of the hybrid array structures: (a) the flip-chip array technology [5] and (b) the Z-plane technology [4].

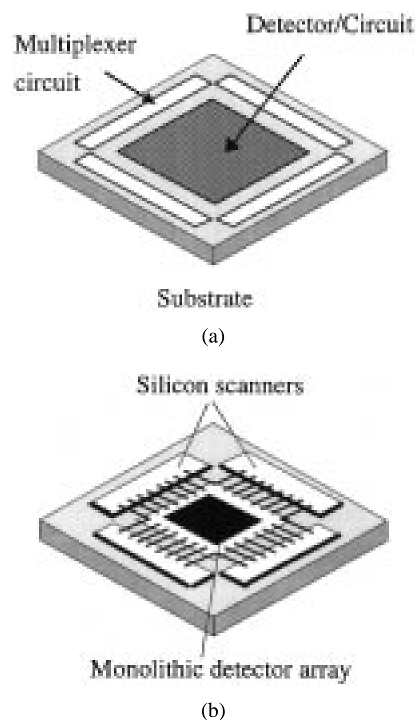

Fig. 3. (a) The structure of monolithic array technology [4] and (b) the structure of pseudomonolithic array technology [4].

used by one channel of detectors so that many electrical circuit techniques like complex input circuit, gain offset correction, A/D converter, filter, smart, and neural function, as well as image signal processing stage can be implemented on the readout chip [39]. However, the image resolution is limited by the readout chip thickness. In the application of hybrid array technology, uniformity of indium bumps, chip alignment, as well as thermal expansion effect and mechanical damage on the detectors should be considered during the hybridization process [40].

2) Monolithic Array: The monolithic array technology is currently developed to solve the hybrid process problems by building IR detectors like PtSi Schottky barriers [22], micromachining bolometers [41], [42], or extrinsic detectors on the silicon substrate [43]. Thus, both IR detectors and readout circuits can be fabricated in a monolithic chip as shown in Fig. 3(a). Both production and reliability of IR FPA's can be improved under monolithic design. However, the detector types and materials must be compatible with the silicon process. This limits the applications of the monolithic array on IR image systems.

3) Pseudomonolithic Array: As an alternative method to the indium-bumping hybrid array and monolithic array technologies, the readout chip and detector chip can be compounded through the via-hole technique [44], in the so-called pseudomonolithic array as shown in Fig. 3(b). Both readout chip surface and detector chip surface must be polished to achieve a precise flatness and parallelism before combining as a single chip. Then some detector fabrication processes and routing metallization processes are applied on the combined single chip. The pseudomonolithic technology retains some advantages of silicon-like processing, but its reliability still needs to be optimized.

B. Operational Requirements for IR FPA

In different applications of IR image systems, there exist certain specific requirements for the design of IR FPA's. In general, the requirements involve a broad range of electrical circuit and detector array parameters like detector bias control, injection efficiency, charge storage capacity, integration time, noise, dynamic range, readout rate, array size and pitch, power, and operating temperature. Some general discussions of these requirements are summarized below.

1) Detector Bias Control: The dark current, injection efficiency, detector $1/f$ noise, and reponsivity are affected by the detector bias. Moreover, operation ability and linearity of spectral response are also affected directly by the bias. Therefore, a strict and stable detector bias control is necessary in IR FPA's.

2) Injection Efficiency and Bandwidth: The injection efficiency is defined as the ratio of the current flowing into the readout circuit to the detector current. High injection efficiency and wide input bandwidth lead to good responsibility and readout performance. To achieve high injection efficiency and wide bandwidth, the input impedance of the interface circuit should be lower than the shunt resistance of IR detectors.

3) Charge Storage Capacity: In most readout structures of IR FPA's, the photon excited carriers are accumulated on the integrating capacitor and transferred to voltage outputs. Therefore, the charge storage capacity is determined by both background and dark current levels of IR detectors as well as the value of the integrating capacitor. Maximum charge

storage capacity can be achieved by keeping background and dark currents small and by using a large integrating capacitor. However, the capacitance value is limited by pixel size and the chip area of readout circuit.

4) Noise: The temporal noise sources in IR FPA's include the photon noise, the detector noise, and the noise from readout electronics. The random and time-invariant noise source associated with the fabrication process of detectors and readout circuits is the fixed-pattern noise (FPN). Those noise sources contributed by readout electronics such as transistor white noise and reset noise (KTC or clocking noise) must be minimized so that their levels are below the background photon noise to achieve the BLIP. Generally, layout arrangement and circuit techniques can be used to reduce the noise level of readout circuits.

5) Dynamic Range: The dynamic range is defined as the ratio of maximum charge capacity to noise floor. The required dynamic range of IR FPA's is determined by the ratio of the brightest signal level to the weakest. Larger dynamic range is preferred but limited by storage capacitance, linearity, and noise level.

6) Readout Rate: The readout rate is chosen according to the specific IR system requirement and limited by the allowable chip power dissipation as well as the circuit operation speed. Usually a higher readout rate is needed for multiple sampling applications in image compensation function. Higher readout rate is also needed to avoid the saturation of the signal after integration.

7) Integration Time: Like the readout rate, the integration time is chosen according to the application consideration. Generally, the saturation frequency of the integrating capacitor and the detector sensitivity determine the proper length of integration time.

8) Array Size and Pitch: The array size and pitch are usually determined by the IR FPA technology. Higher image resolution requires larger array size and smaller pixel pitch. However, a larger pixel size is needed to increase the integration capacitance and improve the performance of charge capacity and dynamic range. Thus, the optimal design tradeoff should be made between the application flexibility and resolution performance.

9) Power Dissipation: This is a typical requirement in the applications of the IR FPA using a photon detector instead of a thermal detector. Power dissipation is limited by the heat loading of the cryogenic cooling system which determines the system cost.

10) Operating Temperature: The operating temperature is determined by the detected wavelength range and the material of IR detectors. For each detector, there is a unique operating temperature.

It is important to determine the operational requirements in the design of an IR FPA for specific applications. A complete analysis of operational parameters like IR background radiation level, spectral response band, operating temperature, detector structure, signal contrast ratio, sensitivity, and resolution should be set before the design tradeoff. Therefore, all the operational requirements discussed above have unique optimized orientations for IR image systems in different applications.

IV. CMOS Readout Techniques for IR Detectors

In the development of IR FPA's, the readout circuit electronics are the second major part next to the IR detector array. Readout electronics are deigned to support a good interface between IR detectors and the following signal processing stage. Different circuit techniques have been developed for IR FPA's with different materials and structures. In the following discussion, only the circuit techniques based on silicon CMOS VLSI technology are addressed.

Generally, the pixel pitch of IR FPA's is reduced with the increasing array size and resolution. Moreover, the total power dissipation of IR FPA's is limited by the image system. These two major factors often put constraints on circuit design space and complexity. Thus, the design of IR FPA readout electronics requires a tradeoff between circuit performance and complexity.

Some simple readout structures like source-follower per detector (SFD) [45], [46], direct injection (DI) [47]–[49], and gate-modulation input (GMI) [45], [50] are still commonly used in large staring IR FPA's because of the small pixel area and power consumption. In addition, more complex circuit techniques like buffered direct injection (BDI) [47], [51] and capacitive transimpedance amplifier (CTIA) [52], [53] have been developed to provide excellent bias control, high injection efficiency, linearity, and noise performance. Simple and high-performance circuit techniques have been a challenging work in the design of readout circuits for IR FPA's. Recently, some new readout structures like the share-buffered direct injection (SBDI) [54], [55], switch current integration (SCI) [56], and buffered gate modulation input (BGMI) [57], have been proposed to achieve better compromise between pixel pitch limitation and readout performance.

In the following, some of the commonly used CMOS readout techniques as well as the state-of-the-art structures will be presented. The noise reduction strategies used to improve IR image performance are also discussed.

A. Readout Circuits

1) Source-Follower Per Detector [45], [46]: A simple readout circuit called the source-follower per detector (SFD) is shown in Fig. 4 where an NMOS source-follower composed of MNI and MNL, a reset PMOS gate M-Rst, and a multiplexing NMOS device M-Sel are used in each cell. The integration capacitance is the summation of detector shunt capacitance C_{detector} and input node capacitance of the SFD. The integration capacitor is reset to high and then discharged by the photocurrent I_{detector}. After an integration period, the cell voltage signal is sampled to the output stage serially through the device M-Sel controlled by the clock *Select*. The simple structure of the SFD makes it suitable for the applications of high density, large format, and low power IR FPA. However, since the photon excited carrier charges are integrated on the input node capacitance of the detector directly, the detector bias voltage changes through integration.

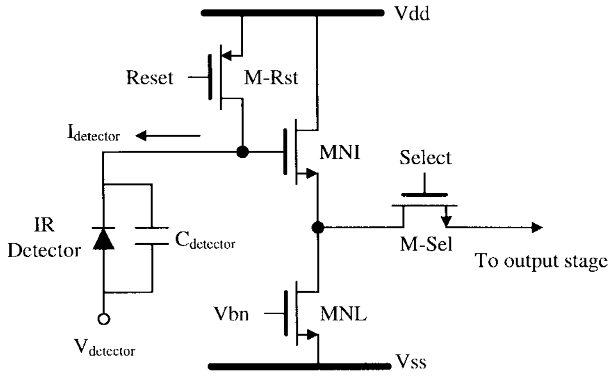

Fig. 4. The source follower per detector (SFD) readout circuit.

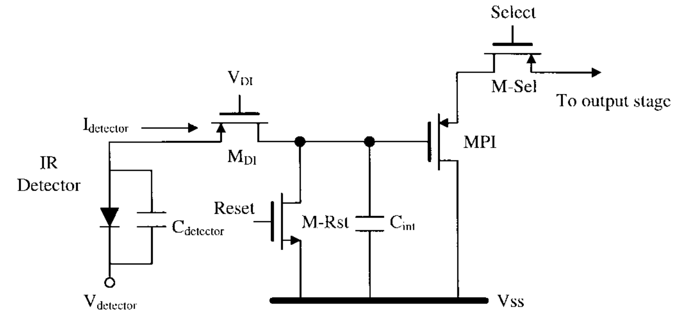

Fig. 5. The direct injection (DI) readout circuit.

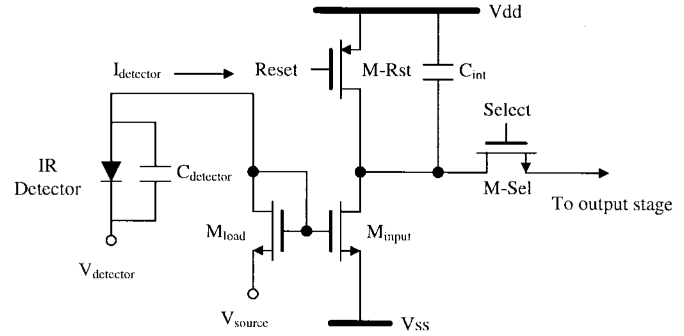

Fig. 6. The gate modulation input (GMI) readout circuit.

It can result in variations of detector characteristics and nonlinearity of readout current, which limit the application of SFD. Moreover, the SFD is susceptible to KTC noise induced by the integration-and-reset function and fixed pattern noise (FPN) caused by the process-dependent threshold voltage variations. Usually, a correlated double sampling (CDS) stage is used to reduce the KTC noise of the SFD readout circuit.

2) Direct Injection [47]–[49]: Another simple readout circuit called the direct injection (DI) is shown in Fig. 5. In the DI circuit, a common-gate PMOS device M_{DI} is used to bias and sense the current of the IR detector. The detector current I_{detector} passing through the gate M_{DI} is further integrated on the integration capacitor C_{int} which can be reset by the NMOS device M-Rst. The integrated voltage is readout through the PMOS source follower MPI and the multiplexing device M-Sel. In the DI circuit, a better bias control than the SFD during integration is supported by the common gate device M_{DI}. Like the SFD circuit, the DI circuit has a simple structure and no active power dissipation. This makes it suitable for high-density IR FPA applications. The injection efficiency of a readout circuit is defined as the ratio of the current flowing into the readout circuit to the detector photocurrent I_{detector}. The injection efficiency of the DI is determined by the ratio of detector shunt resistance to input resistance of M_{DI}. Thus, a lower input resistance means a higher injection efficiency and better detectivity since the input resistance of the PMOS device M_{DI} is proportional to its overall current including the background current level. Thus, the DI is not suitable for the applications of low-background IR image readout. Moreover, a stable and low noise dc bias V_{DI} is needed in the DI circuit. Both threshold voltage nonuniformity and KTC noise are still problems of the DI readout circuit.

3) Gate-Modulation Input [45], [50]: The gate modulation input (GMI) readout circuit has a current-mirror configuration with the tunable source bias V_{source} to control the current gain as shown in Fig. 6. The injection current flowing into the master device M_{load} is mirrored and amplified by the slave device M_{input} and integrated on the integration capacitor C_{int} with the reset PMOS device M-Rst. The current gain of the current mirror M_{load} and M_{input} is tunable by the adjustable bias V_{source}. Similar to that in the DI circuit, the injection efficiency of the GMI is dependent on the ratio of detector shunt resistance to input resistance of M_{load}. However, the inherent current gain of the GMI leads to higher detection sensitivity and reduced input referred noise as compared to the DI. Moreover, the adaptive current gain in the GMI can be controlled by the background level and thus the realizable background suppression leads to a higher dynamic range. However, both injection efficiency and current gain of the GMI are sensitive to the variations of V_{source} and threshold voltages. To obtain a large total dynamic range in the GMI circuit, the current gain should be kept high and uniform. This leads to strict requirements on MOSFET threshold-voltage uniformity and dc bias stability of V_{source} which are difficult to be controlled.

4) Buffered Direct Injection [47], [51]: A complex readout circuit called the BDI circuit is shown in Fig. 7 where the circuit structure is similar to the DI except that an additional inverted gain stage with the gain $-A$ is connected between gate node of the common-gate input device M_{BDI} and detector node. The input impedance can be decreased by a factor of A due to the negative feedback structure. Thus, the injection efficiency is increased to near unity. Usually, the inverted gain stage can be implemented by a differential pair or inverter. The detector bias control of the BDI is more stable than those of SFD and DI due to the virtual-short property of the gain stage. Moreover, both equivalent input referred noise and operational bandwidth can also be improved as compared to the DI circuit. Since the detector bias is controlled by the input voltage V_{com} of the differential pair instead of V_{DI} and gate-to-source voltage of M_{DI} in the DI circuit, both the threshold voltage nonuniformity problem and strict low-noise bias requirement of the DI are immune. However, the additional gain stage consumes active power during integration. This additional power loading can be reduced by proper design of the gain

Fig. 7. The buffered direct injection (BDI) readout circuit.

Fig. 8. The capacitive transimpedance amplifier (CTIA) readout circuit.

stage with low bias current. Generally, the BDI is suitable for those applications which require high readout performance and can afford additional circuit complexity, chip area, and power dissipation.

5) Capacitive Transimpedance Amplifier [52], [53]: The schematic of the capacitive transimpedance amplifier (CTIA) is shown in Fig. 8 where the integration capacitor $C_{\rm int}$ is placed on the feedback loop of the amplifier with a reset device M-Rst to discharge the integration capacitor and reset the amplifier output to the reference voltage $V_{\rm com}$. The detector bias is also controlled by $V_{\rm com}$ through the virtual-short feature of the amplifier. Thus, a good detector-bias control can be obtained in the CTIA as the BDI. Due to the Miller effect on the integration capacitor, its capacitance can be made extremely small to obtain low-noise and high-sensitivity performance. Unlike DI and BDI, the input impedance of the CTIA is independent of detector current. However, the feedthrough effect of the reset clock can be coupled to the detector node and affect the stability of both detector bias and amplifier operational point. Moreover, additional area and power consumption of the inverted gain stage are needed in the CTIA. Usually, the inverted gain stage is implemented by a differential amplifier to provide low detector bias offset and a CDS stage is used to eliminate the KTC noise.

6) Share-Buffered Direct Injection [54], [55]: Recently, an improved BDI readout circuit called the SBDI has been proposed. In the SBDI, the gain stage is implemented by the differential pair with the shared half circuit techniques as shown in Fig. 9. The differential pair consists of the common left-half circuit Mb, MNS, and MPS which is shared by all the cells in the same row and the two MOS devices MP and MN which are implemented in each cell circuit. The source node of MP and the gate node of MN are biased by the shared half circuit through two global lines. Under this arrangement, both chip area and power dissipation of the amplifier in the SBDI can be reduced to nearly 50% of those in BDI or CTIA circuits. But high injection efficiency, good detector bias control, threshold voltage variation immunity, and low noise performance of the BDI circuit can be maintained in the SBDI. In the SBDI circuit of Fig. 9, a dynamic discharging output stage is also introduced to save the static power dissipation and improve readout speed by applying a dynamic discharging gate MNDy and clock Dyrst. The discharging gate MNDy controlled by clock Dyrst is dynamically turned on to overcome the speed bottleneck of output stage at discharging phase and consumes only dynamic power. Generally, the SBDI can offer a better tradeoff between circuit area, power consumption, and circuit performance. This makes it more suitable for high density, large-array, and high-performance applications in IR FPA's.

7) Switch Current Integration [56]: A new readout structure called the SCI is shown in Fig. 10 where the integration capacitors are put outside the FPA and shared by the cells in the same column. The detector current $I_{\rm detector}$ is selected row by row, switched to the shared integration capacitor through the row select switch MR-Sel, and integrated. Thus, the structure performs the current switching and integration as its name implies. As shown in Fig. 10, the shared buffer technique is used to realize the gain stage of the SCI. Therefore, good performance of both SBDI and BDI can be retained in the SCI readout structure. The cascode current mirror M_1–M_4 acts as the current buffer before the select switch and offers a current mode gain determined by the dimension ratio of M_2 and M_4. This current gain can improve the detection sensitivity and reduce the input referred noise. When the row-select signal R-Sel is low, each cell in the same row is selected through MR-Sel and connected to the shared integration capacitor stage. The switched current is integrated on the shared capacitor and then sampled to the output stage through MC-Sel controlled by the column-select signal C-Sel. Since the integration capacitor is moved out of the cell circuit and the focal plane, the pixel size limitation of the readout circuit can be released. Moreover, both dynamic range and charge capacity can be increased by making a large integration capacitor along the column direction in the shared off-focal-plane integration capacitor stage. The integration time of the SCI readout structure is limited by one row processing time. This could lead to the reduced detection sensitivity. But the reduced sensitivity can be compensated by increasing the current gain of the current mirror.

8) Buffered Gate Modulation Input [57]: In the GMI circuit of Fig. 6, the amplified background current is integrated directly, and thus a large amount of charges must be accommodated within a unit cell. Under this situation, a large integrating capacitor is required to avoid saturation. However, the realization of a large capacitor is a problem in the design of high-density large IR FPA system. To solve this problem, the improved circuit of the GMI called the BGMI is proposed as shown in Fig. 11 where a current-mode background sup-

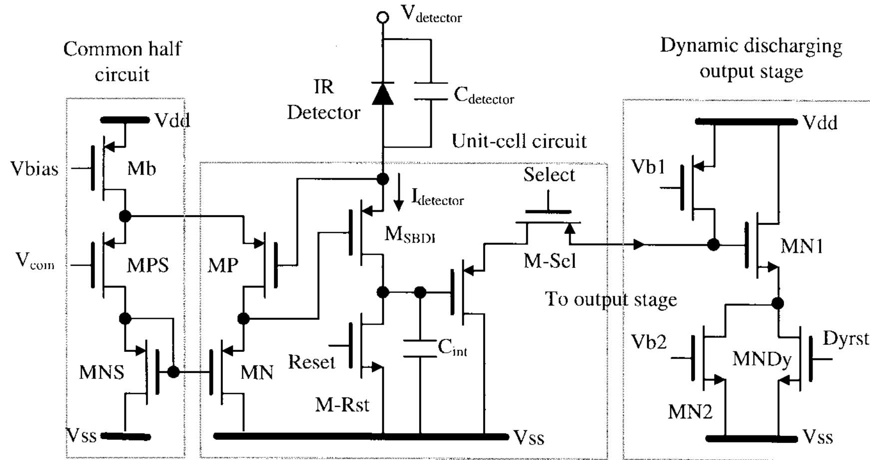

Fig. 9. The SBDI readout circuit with dynamic discharging output stage.

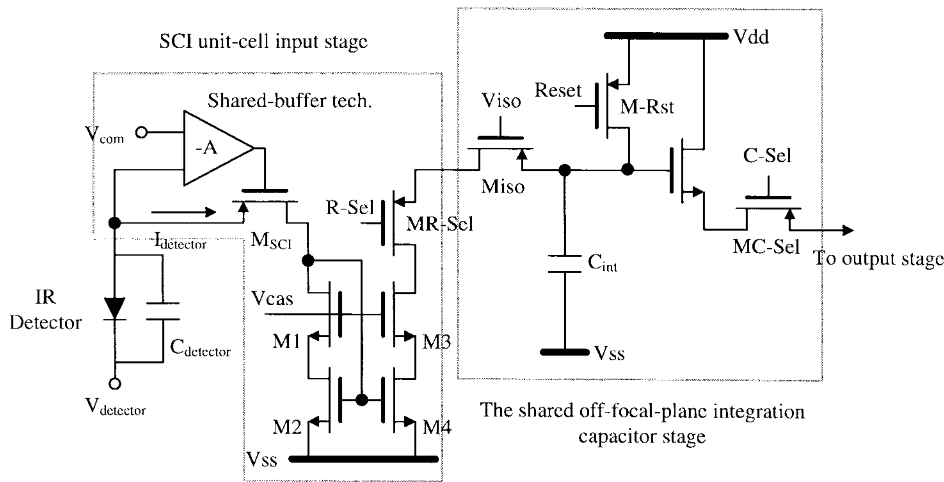

Fig. 10. The unit-cell input stage and off-FPA shared integration capacitor stage of the SCI readout structure.

pression circuit is incorporated with the SCI circuit to achieve higher dynamic range and better readout performance. Thus, a large integrating capacitor can be achieved. As shown in Fig. 11, the unit-cell circuit of the BGMI consists of a shared buffer as the input stage, the unbalance current mirror M_1 and M_2, and the row select switch $M_{\text{R-Sel}}$. The shared-buffer technique provides a good bias control for the IR detector, whereas the unbalance current mirror has a large current gain due to the threshold voltage difference between M_1 and M_2 caused by the intentional device channel-length unbalance. Through the use of the threshold voltage difference, the strict requirement of low- noise tunable dc source bias V_{source} in the GMI and the inevitable FPN due to the threshold voltage process dependent variation can be avoided.

As shown in Fig. 11, the detector current is switched from the BGMI unit-cell input stage to the shared off-FPA integration capacitor stage. In the shared integration capacitor stage, the amplified current from the cell is mirrored through a cascade current mirror and subtracted by a dc tunable current before being integrated on the capacitor C_{int}. Thus, the current-mode background suppression is achieved. To generate the dc tunable current, the threshold-voltage compensated current source [5] M_{B1}, M_{B2}, and M_{B3} is used with the adjustable voltage V_{Tune} added to the source node of M_{B2}. This current source can generate a dc current nearly independent of MOS threshold voltages. Thus, the background pedestal removal of IR FPA readout with good immunity from threshold-voltage variations can be achieved. The resultant input referred spatial noise is relatively small and the strict requirement of threshold-voltage uniformity can be released. The suppression current is also adjustable through the voltage V_{Tune}. After the background suppression, the signal current is integrated on the integration capacitor, and the integrated signal voltage is alternatively sampled to the common output stage through the P-type source follower as a buffer.

Since only one row of the integration capacitor stage is needed in the whole chip and the infrared background current is low, the additional power dissipation of background suppression circuits is still tolerable. The good readout performance and adaptive gain control make BGMI suitable for the IR FPA readout applications with large background level range.

B. Noise Reduction of IR Image

Temporal noise and pattern noise are two main noise types of IR image systems. The temporal noise sources include shot, thermal, $1/f$ (flicker), generation-recombination, KTC,

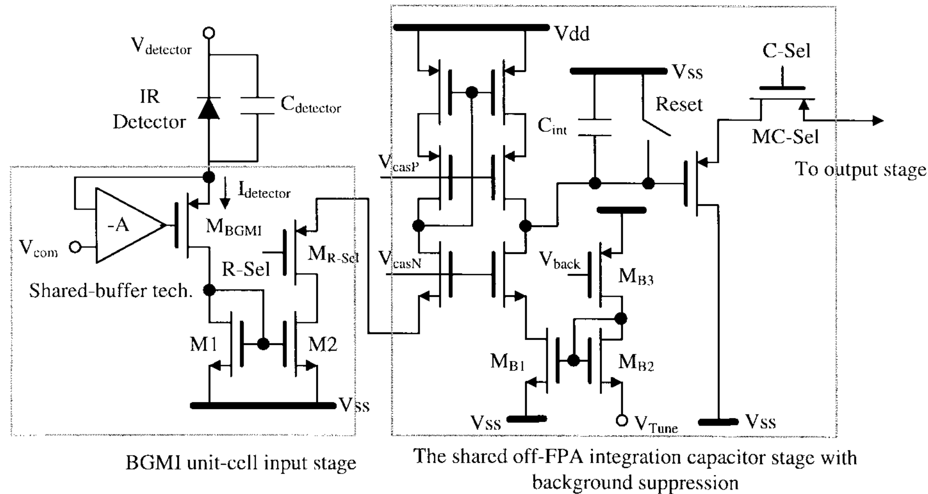

Fig. 11. The BGMI readout structure with adaptive current gain control and background suppression.

and photon noise which are contributed by detectors and readout circuits. The pattern noise is caused by the process dependent variations which produce offset drifts among detector channels. Usually, the temporal noise can be reduced by detector technology, operational condition, circuit techniques, and system arrangement, whereas the fixed pattern noise can be reduced by calibration techniques [59], [60]. The two-point and multipoint calibrations are commonly used to reduce the FPN [16], [61]. The required number of calibration points is dependent on the infrared radiation determined by the range of object temperature variations. A larger radiation means a larger output voltage swing and more nonuniformity of response. For the same range of temperature variations, the infrared radiation of the MWIR detector is larger than that of the LWIR detector. Thus, the number of calibration points of MWIR readout is usually more than that of LWIR readout. The noise sources contributed by readout circuits should be carefully reduced to achieve a BLIP. Some general strategies of noise reduction for readout circuits like CDS [62], modified CDS [63], multiple correlated sample read (MCS) [64], and chopper-stabilized input circuit (CSI) [65] have been proposed.

V. Future Directions

In the future, the performance of thermal imaging systems with cooled or uncooled FPA technologies will be further enhanced by the development of new detection methodologies and signal processing techniques. Moreover, the concept of military and commercial dual-use technology in IR imaging systems will lead to the cost-driven and application-oriented development. In this section, some advanced development directions on IR imaging systems such as on-FPA signal processing, optical link, background suppression, and smart-FPA concept are discussed briefly.

A. On-Chip A/D Conversion

The on-chip A/D conversion is an advanced circuit technology which is applied to IR FPA chips more recently [66], [67]. Through the conversion, instead of analog, the digital output signal of IR FPA chips avoids noise coupling during the transfer out of cooling systems and dewars. Thus, the system design can be simplified and the cables and IC chip counts can be reduced. However, the additional power and area consumption on the FPA may not be acceptable in some applications. Thus, the on-chip A/D conversion is usually used in high-performance scanning array applications. Some new structures of on-chip A/D conversion have been proposed for the design of staring arrays by using sigma–delta modulation or semi-parallel architectures [68].

B. Optical Link

The loading of cable capacitance in a readout chip, the loading of parasitic heat from thermal detectors, and the noise coupling effect degrade the system performance seriously. This can be improved by optical link techniques [69]. An analog optical modulator on the FPA is designed to transfer output signals to the laser diodes outside the dewar through optical fibers. In this configuration, all the noise, loading, and coupling effects of the conventional cables can be avoided. The optical signals can also be digitized before sending to the optical link. This can further improve performance at the expense of additional power dissipation.

C. Background Suppression

The background suppression is used to improve detection sensitivity, dynamic range, and application range. High background charges could saturate the finite integration capacitance and cause malfunction of IR image systems. Typically, the background suppression is done in the charge domain which cannot solve the above problem. New current-mode background suppression like BGMI described above and current memory structure [68] have been proposed to achieve a better performance of IR image readout.

D. Smart Focal Plane Array

The on-FPA signal processing technologies are used to support a front-end signal processing which can significantly reduce the downstream system loading and improve readout performance [70], [71]. Some smart functions such as

bad pixel substitution [72], pixel averaging [73], and neural-FPA concept [74] have been introduced in the IR FPA. The bad pixel substitution by using quad-cell readout and pixel averaging techniques can improve both yield and signal-to-noise ratio of FPA's [72]. Neural network concept can be applied to achieve the on-chip image extraction and motion detection. Recently, a new sensing structure has been proposed to implement CMOS silicon retina systems using multi-emitter bipolar junction transistors (BJT's) [75]. The new BJT-based silicon retina can perform some smart functions like edge detection, pattern recognition, and motion detection in simple and compact detector arrays [76]. Thus, it is suitable for the development of IR smart FPA. Other image processing functions including contrast and quality enhancement, image compensation, and nonlinearity fix may be implemented on-chip to achieve smart FPA's. The development of smart functions can satisfy the needs of IR image applications in system performance, productivity, availability, and specific requirement.

VI. Summary

In this paper, IR detectors, FPA structures and requirements, CMOS readout techniques, and the future development trend of IR imaging systems are presented and discussed. All the structures and technologies discussed above have their uniqueness and features for different applications. Due to the development of commercial uncooled IR imaging systems and the fast advancement of submicrometer CMOS technologies, a high-performance and low-cost IR imaging system will be developed through the inventions of new circuit techniques and structure. Moreover, the emerging technologies of CMOS visible-light imaging systems [77]–[80] will share the advantages of the developed IR imaging systems due to their similarities. Both will be driven by rapid development and wide applications of multimedia systems. A new generation of CMOS imaging systems is highly expected.

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References

[1] R. J. Dempsey, D. G. Davis, R. G. Jr. Buice, and R. A. Lodder, "Biological and medical applications of near infrared spectrometry," *Appl. Spectr.,* vol. 50, no. 2, pp. 18A–34A, Feb. 1996.

[2] N. Itoh, K. Yanagisawa, T. Ichikawa, K. Tarusawa, and H. Kataza, "Kiso observatory near-infrared camera with a large format array," in *Proc. SPIE, Infrared Technology XXI,* 1995, vol. 2552, pp. 430–437.

[3] D. C. Murphy, S. E. Persson, M. A. Pahre, A. Sivaramakrishnan, and S. G. Djorgovski, "An infrared camera for the Palomar Observatory 60-inch telescope," *Publications Astronomical Soc. of the Pacific,* vol. 107, pp. 1234–1242, 1995.

[4] D. A. Scribner, M. R. Kruer, and J. M. Killiany, "Infrared focal-plane array technology," *Proc. IEEE,* vol. 79, no. 1, pp. 66–85, 1991.

[5] E. R. Fossum and B. Pain, "Infrared readout electronics for space science sensors: State of the art and future directions," in *Infrared Technology XIX, Proc. SPIE 2020,* 1993, pp. 262–285.

[6] L. S. Johns, "Dual-use technology programs," in *Infrared Technology XX, Proc. SPIE 2269,* 1994, pp. 2–7.

[7] R. K. Kirshchman, *Low-Temperature Electronics.* New York: IEEE Press, 1989.

[8] E. L. Dereniak and D. G. Crowe, *Optical Radiation Detectors.* New York: Wiley, 1984.

[9] L. J. Kozlowski, J. M. Arias, and W. E. Tennant, "Experimental comparison of staring IR sensor technologies including PV HgCdTe, PV InGaAs, and quantum well GaAs/AlGaAs," in *Solid State Crystals: Materials Science and Applications, Proc. SPIE,* Oct. 1994, vol. 2373, pp. 354–360.

[10] C. Hanson, "Uncooled thermal imaging at Texas Instruments," in *Infrared Technology XIX, Proc. SPIE,* July 1993, vol. 2020, pp. 330–339.

[11] J. Koepernik, H. Budzier, and G. Hofmann, "Influence of nonideal chopper design on nonuniformity in uncooled pyroelectric staring array systems," in *Infrared Technology XXI, Proc. SPIE,* July 1995, vol. 2552, pp. 624–635.

[12] L. Goldminz, B. Sabbah, Z. M. Friedman, and Y. Nemirovsky, "Mercury-cadmium-telluride photovoltaic and photoconductive focal-plane arrays," *Opt. Eng.,* vol. 32, pp. 952–957, May 1993.

[13] H. Zogg, A. Fach, C. Maissen, J. Masek, and S. Blunier, "Photovoltaic lead-chalcogenide on silicon infrared sensor arrays," *Opt. Eng.,* vol. 33, pp. 1440–1449, May 1994.

[14] H. Zogg, A. Fach, J. John, J. Masek, P. Muller, C. Paglino, and S. Blunier, "Photovoltaic IV–VI on Si infrared sensor arrays for thermal imaging," *Opt. Eng.,* vol. 34, pp. 1964–1969, July 1995.

[15] R. L. Petritz, "Fundamentals of infrared detectors," *Proc. IRE,* vol. 47, pp. 1458–1467, 1959.

[16] H. Zogg, A. Fach, J. John, J. Masek, P. Muller, C. Paglino, and W. Buttler, "Pb/sub 1-x/Sn/sub x/Se-on-Si LWIR thermal imaging system," in *Infrared Technology XXI, Proc. SPIE,* July 1995, vol. 2552, pp. 404–410.

[17] V. Gopal, "Spatial noise limited NETD performance of a HgCdTe hybrid focal plane array," *Infrared Phys., Technol.,* vol. 37, pp. 313–320, 1996.

[18] L. J. Kozlowski, J. M. Arias, and W. E. Tennant, "Experimental comparison of staring IR sensor technologies including PV HgCdTe, PV InGaAs, and quantum well GaAs/AlGaAs," in *Solid State Crystals: Materials Science and Applications, Proc. SPIE,* Oct. 1994, vol. 2373, pp. 354–360.

[19] J. Wolf, "Low-background far-infrared detectors and arrays," *Opt. Eng.,* vol. 33, pp. 1492–1500, May 1994.

[20] T. Seto, A. Mori, R. Ishigaki, S. Itoh, N. Yutani, M. Kimata, N. Tubouchi, A. Akiyama, and T. Sasaki, "Performance of 1M-IRCSD imager with PtSi Schottky-barrier detectors," in *Infrared Technology XIX, Proc. SPIE,* July 1993, vol. 2020, pp. 404–414.

[21] A. Akiyama, T. Sasaki, T. Seto, A. Mori, R. Ishigaki, S. Itoh, N. Yutani, M. Kimata, and N. Tubouchi, "1040 × 1040 infrared charge sweep device imager with PtSi Schottky-barrier detectors," *Opt. Eng.,* vol. 33, pp. 64–71, Jan. 1994.

[22] M. Kimata, H. Yagi, N. Yutani, K. Endo, and M. Nunoshita, "Schottky-barrier infrared focal plane arrays," *J. Japan Soc. Infrared Sci. Technol.,* vol. 5, pp. 33–42, 1995.

[23] H. Yagi, N. Yutani, J. Nakanishi, M. Kimata, M. Nunoshita, T. Seto, and M. Kamei, "Monolithic photovoltaic IV–VI-on-Si infrared sensor array with integrated readout electronics," *IEEE Trans. Electron Devices,* vol. 39, p. 2676, Nov. 1992.

[24] ——, "Monolithic Schottky-barrier infrared image sensor with 71% fill factor," *Opt. Eng.,* vol. 33, pp. 1454–1460, 1994.

[25] M. Kimata, H. Yagi, N. Yutani, K. Endo, and M. Nunoshita, "1040 × 1040 infrared charge sweep device imager with PtSi Schottky-barrier detectors," *Opt. Eng.,* vol. 33, pp. 64–71, 1994.

[26] R. L. Petritz, "Blocking injected dark current in impurity-band-conduction photodetectors using a PtSi Schottky barrier," *Appl. Phys. Lett.,* vol. 67, pp. 774–776, 1995.

[27] N. M. Shorrocks, A. Patel, M. J. Walker, and A. D. Parsons, "Uncooled pyroelectric arrays for contactless temperature measurements," in *Smart Focal Plane Arrays and Focal Plane Array Testing, Proc. SPIE,* 1995, vol. 2474, pp. 98–109.

[28] ——, "Integrated thin film PZT pyroelectric detector arrays," *Microelectron. Eng.,* vol. 29, pp. 59–66, 1995.

[29] P. W. Kruse, "Uncooled IR focal plane arrays," in *Infrared Technology XXI, Proc. SPIE,* July 1995, vol. 2552, pp. 556–563.

[30] N. Neumann, R. Kohler, R. Gottfried-Gottfried, and N. Hess, "Pyroelectric sensors and arrays based on P(VDF/TrFE) copolymer films," in *Seventh Int. Symp. Integrated Ferroelectrics,* Mar. 1995, vol. 11, pp. 1–14.

[31] N. M. Shorrocks, A. Patel, M. J. Walker, and A. D. Parsons, "Integrated thin film PZT pyroelectric detector arrays," in *1st European Meeting on Integrated Ferroelectrics,* July 1995, vol. 29, pp. 59–66.

[32] N. Butler, R. Blackwell, R. Murphy, R. Silva, and C. Marshall, "Low cost uncooled microbolometer imaging system for dual use," in *Infrared Technology XXI, Proc. SPIE,* July 1995, vol. 2552, pp. 583–591.

[33] A. Tanaka, S. Matsumoto, N. Tsukamoto, S. Itoh, T. Endoh, A. Nakazato, Y. Kumazawa, M. Hijikawa, H. Gotoh, T. Tanaka, and N. Teranishi, "Silicon IC process compatible bolometer infrared focal plane array," in *8th Int. Conf. Solid-State Sensors and Actuators and Eurosensors IX,* 1995, vol. 2, pp. 632–635.

[34] N. Bluzer and M. G. Forrester, "Superconducting quantum detectors," *Opt. Eng.,* vol. 33, pp. 697–703, Mar. 1993.

[35] B. R. Johnson, M. C. Foote, H. A. Marsh, and B. D. Hunt, "IEpitaxial YBa/sub 2/Cu/sub 3/O/sub 7/ superconducting infrared microbolometers on silicon," in *Advanced Microdevices and Space Science Sensors, Proc. SPIE,* July 1994, vol. 2267, pp. 24–30.

[36] F. M. Tong, N. M. Ravindra, L. Ganapathi, S. Giles, and R. Rao, "High T/sub c/ YBa/sub 2/Cu/sub 3/O/sub 7-delta/superconducting transition-edge microbolometers," *Infrared Phys. Technol.,* vol. 36, pp. 1053–1058, Dec. 1995.

[37] D. H. Pommerenig, D. D. Enders, and T. E. Meinhardt, "Hybrid silicon focal plane array development: An update," in *Proc. Society Pho-Opt. Instrumentation Engineering,* vol. 267, pp. 23–30, 1981.

[38] J. C. Carson, "Application of advanced 'Z' technology focal plane architectures," in *Proc. Society Pho-Opt. Instrumentation Engineering,* 1988, vol. 930, pp. 164–182.

[39] E. T. Young, M. Scutero, G. H. Rieke, E. E. Haller, and J. W. Beeman, "High performance Ge:Ga arrays for the far infrared," in *Infrared Detectors and Instrumentation, Proc. SPIE,* Apr. 1993, vol. 1946, pp. 68–77.

[40] V. Gopal, "Spatial noise limited NETD performance of a HgCdTe hybrid focal plane array," *Infrared Phys. Technol.,* vol. 37, pp. 313–320, Apr. 1996.

[41] M. Ueno, O. Kaneda, T. Ishikawa, K. Yamada, A. Yamada, M. Kimata, and M. Nunoshita, "Monolithic uncooled infrared image sensor with 160×120 pixels," in *Infrared Technology XXI, Proc. SPIE,* July 1995, vol. 2552, pp. 636–643.

[42] A. Tanaka, S. Matsumoto, N. Tsukamoto, S. Itoh, T. Endoh, A. Nakazato, Y. Kumazawa, M. Hijikawa, H. Gotoh, T. Tanaka, and N. Teranishi, "Silicon IC process compatible bolometer infrared focal plane array," in *8th Int. Conf. Solid-State Sensors and Actuators and Eurosensors IX, Dig. Tech. Papers,* 1995, vol. 2, pp. 632–635.

[43] J. Wolf, "Low-background far-infrared detectors and arrays," *Opt. Eng.,* vol. 33, pp. 1492–1500, May 1994.

[44] I. M. Baker and R. A. Ballingall, "Photovoltaic CdHgTe-silicon hybrid focal planes," in *Proc. Society Pho-Opt. Instrumentation Engineering,* 1984, vol. 510, pp. 121–129.

[45] A. M. Fowler, R. G. Probst, J. P. Britt, R. R. Joyce, and F. C. Gillett, "Evaluation of an indium antimonide hybrid focal plane array for ground-based infrared astronomy," *Opt. Eng.,* vol. 26, pp. 232–240, 1987.

[46] N. Lum, J. Asbrock, R. White, R. Kelchner, L. Lum, L. Pham, C. McCreight, M. McKelvey, R. Jr. McMurray, W. Forrest, and J. Garnett, "Low-noise, low-temperature, 256×256 Si:As IBC staring FPA," in *Infrared Detectors and Instrumentation, Proc. SPIE,* Apr. 1993, vol. 1946, pp. 100–109.

[47] N. Bluzer and R. Stehlik, "Buffered direct injection of photocurrents into charge coupled devices," *IEEE Trans. Electron Devices,* vol. 25, no. 2, pp. 160–166, 1978.

[48] J. T. Longo, D. T. Cheung, A. M. Andrewheung, A. M. Andrews, C. C. Wang, and J. M. Tracy, "Infrared focal planes in intrinsic semiconductors," *IEEE Trans. Electron Devices,* vol. 25, no. 2, 1978.

[49] K. Chow, J. P. Rode, D. H. Seib, and J. D. Blackwell, "Hybrid infrared focal-plane arrays," *IEEE Trans. Electron Devices,* vol. 29, no. 1, 1982.

[50] L. J. Kozlowski, W. V. McLevige, S. A. Cabelli, A. H. B. Vanberwyck, D. E. Cooper, E. R. Blazejewski, K. Vural, and W. E. Tennant, "Attainment of high sensitivity at elevated operating temperatures with staring hybrid HgCdTe-on-Sapphire focal plane arrays," *Opt. Eng.,* vol. 33, no. 3, pp. 704–715, 1994.

[51] P. Norton, "Infrared image sensors," *Opt. Eng.,* vol. 30, no. 11, pp. 1649–1660, 1991.

[52] L. Kozlowski, S. Cabelli, R. Kezer, and W. Kleinhans, "10×132 CMOS/CCD readout with 25 μm pitch and on-chip signal processing including CDS and TDI," in *Infrared Readout Electronics, Proc. SPIE,* 1992, vol. 1684, pp. 222–230.

[53] C. Staller, L. Ramiirez, C. Niblack, M. Blessinger, and W. Kleiinhans, "A radiation hard, low background multiplexer design for spacecraft imager applications," in *Infrared Readout Electronics, Proc. SPIE,* 1992, vol. 1684, pp. 175–181.

[54] C. Y. Wu, C. C. Hsieh, F. W. Jih, T. P. Sun, and S. J. Yang, "A new share-buffered direct-injection readout structure for infrared detector," in *Infrared Technology XIX, Proc. SPIE,* 1993, vol. 2020, pp. 57–64.

[55] C. Y. Wu and C. C. Hsieh, "New design techniques for a complementary metal-oxide semiconductor current readout integration circuit for infrared detector arrays," *Opt. Eng.,* vol. 34, no. 1, pp. 160–168, Jan. 1995.

[56] C. C. Hsieh, C. Y. Wu, F. W. Jih, T. P. Sun, and S. J. Yang, "A new switch-current integration readout structure for infrared focal plane array," in *Infrared Technology XX, Proc. SPIE,* July 1994, vol. 2269, pp. 718–726.

[57] C. C. Hsieh, C. Y. Wu, F. W. Jih, T. P. Sun, and H. Chang, "A new CMOS readout circuit design for the IR FPA with adaptive gain control and current-mode background suppression," in *IEEE Proc. ISCAS'96,* May 1996, vol. 1, pp. 137–140.

[58] S. Y. Chin and C. Y. Wu, "A 10-b 125-MHz CMOS digital-to-analog converter (DAC) with threshold-voltage compensated current sources," *IEEE J. Solid-State Circuits,* pp. 1374–1380, Nov. 1994.

[59] M. D. Nelson, J. F. Johnson, and T. S. Lomheim, "General noise processes in hybrid infrared focal plane arrays," *Opt. Eng.,* vol. 30, no. 11, pp. 1682–1700, 1991.

[60] I. M. Mason, P. H. Sheather, J. A. Bowles, and G. Davies, "Blackbody calibration sources of high accuracy for a spaceborne infrared instrument: The along track scanning radiometer," *Appl. Opt.,* vol. 35, no. 4, pp. 629–639, 1996.

[61] A. Lambrecht, M. Tschirschwitz, R. Grisar, U. Schiessl, J. Wolf, and D. Lemke, "Sub-threshold operated lead-salt lasers for calibration of IR-astronomy detectors," *Infrared Phys. Technol.,* vol. 37, no. 1, pp. 173–179, 1996.

[62] R. J. Kansy, "An response of a correlated double sampling circuit to $1/f$ noise," *IEEE J. Solid-State Circuits,* vol. 15, pp. 373–375, 1980.

[63] H. M. Wey and W. Guggenbuhl, "An improved correlated double sampling circuit for low noise charge-couple devices," *IEEE J. Solid-State Circuits,* vol. 37, no. 12, pp. 1559–1565, 1990.

[64] E. T. Young, M. Scutero, G. Rieke, T. Milner, F. J. Low, P. Hubbard, J. Davis, E. E. Haller, and J. Beeman, "Far-infrared focal plane development for SIRT," in *Infrared Readout Electronics, Proc. SPIE,* Apr. 1992, vol. 1684, pp. 63–74.

[65] A. Lockwood and W. Parrish, "Predicted performance of indium antimonide focal plan arrays," *Opt. Eng.,* vol. 26, no. 3, pp. 228–231, 1987.

[66] W. J. Mandl, "Focal plane analog-to-digital conversion development," in *Smart Focal Plane Arrays and Focal Plane Array Testing, Proc. SPIE,* Apr. 1995, vol. 2474, pp. 63–71.

[67] U. Ringh, C. Jansson, C. Svensson, and K. Liddiard, "CMOS analog to digital conversion for uncooled bolometer infrared detector arrays," in *Smart Focal Plane Arrays and Focal Plane Array Testing, Proc. SPIE,* Apr. 1995, vol. 2474, pp. 88–97.

[68] B. Pain, S. Mendis, R. Schober, R. Nixon, and E. Fossum, "Low-power, low-noise analog circuits for on focal-plane signal processing of infrared sensors," in *Infrared Detectors and Instrumentation, Proc. SPIE,* 1993, vol. 1946, pp. 365–374.

[69] A. R. Johnston, D. T. H. Liu, S. Forouhar, G. F. Lutes, J. Maserjian, and E. R. Fossum, "Optical links for cryogenic focal-plane array readout," in *Infrared Detectors and Instrumentation, Proc. SPIE,* 1993, vol. 1946, pp. 375–383.

[70] P. Bauer, L. Audaire, P. Rambaud, M. Pirot, F. Bauer, and J. Simonne, "On the way to a smart infrared sensor," *ESSCIRC'95, 21st European Solid-State Circuits,* Sept. 1995, pp. 330–333.

[71] C. Jansson, U. Ringh, and K. Liddiard, "On-chip analog-to-digital conversion suitable for uncooled focal plane detector arrays employed in smart IR sensors," in *Smart Focal Plane Arrays and Focal Plane Array Testing, Proc. SPIE,* Apr. 1995, vol. 2474, pp. 72–87.

[72] R. Cannata, "Introduction to infrared focal plane electronics," *The SPIE Short Course Note,* San Diego, CA, July 1993.

[73] R. Panicacci, S. Kemeny, L. Matthies, B. Pain, and E. R. Fossum, "Programmable multiresolution CMOS active pixel sensor," in *Int. Soc. Optical Engineering, Proc. SPIE,* Feb. 1996, vol. 2654, pp. 72–79.

[74] H. H. Thodberg, "Review of bayesian neural networks with an application to near-infrared spectroscopy," *IEEE Trans. Neural Networks,* vol. 7, no. 1, pp. 56–72, 1996.

[75] C. Y. Wu and C. F. Chiu, "A new structure of the 2-D silicon retina," in *IEEE J. Solid-State Circuits,* vol. 30, pp. 890–897, Aug. 1995.

[76] C. F. Chiu and C. Y. Wu, "The design of rotation-invariant pattern recognition using the silicon retina," *IEEE J. Solid-State Circuits,* vol. 32, pp. 526–534, Apr. 1997.

[77] R. H. Nixon, S. E. Kemeny, C. O. Staller, and E. R. Fossum, "256×256 CMOS active pixel sensor camera-on-a chip," in *ISSCC Dig. Tech. Papers,* 1996, pp. 178–179.

[78] C. H. Aw and B. A. Wooley, "A 128×128-pixel standard-CMOS image sensor with electronic shutter," in *ISSCC Dig. Tech. Papers,* 1996, pp. 180–181.

[79] A. Bakker and J. H. Huijsing, “Micropower CMOS temperature sensor with digital output,” in *IEEE J. Solid-State Circuits,* vol. 31, no. 7, pp. 933–937, 1996.

[80] K. S. Szajda, C. G. Sodini, and H. F. Bowman, “A Low-noise, high-resolution silicon temperature sensor,” *IEEE J. Solid-State Circuits,* vol. 31, no. 9, pp. 1308–1313, 1996.

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