

Investigation of the low dielectric siloxane-based hydrogen silsesquioxane (HSQ) as passivation layer on TFT-LCD

Ta-Shan Chang^a, Ting-Chang Chang^{b,d,*}, Po-Tsun Liu^{c,e}, Shu-Wei Tsao^b, Feng-Sheng Yeh^a

^a Institute of Electronics Engineering, National Tsing Hua University, Hsin-Chu, Taiwan, ROC

^b Department of Physics and Institute of Electro-Optical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan, ROC

^c Department of Photonics & Display Institute, National Chiao Tung University, Hsin-Chu, Taiwan, ROC

^d Center for Nanoscience & Nanotechnology, National Sun Yat-Sen University, 70 Lien-hai Rd., Kaohsiung, Taiwan, ROC

^e National Nano Device Laboratory, 1001-1 Ta-Hsueh Rd., Hsin-Chu, Taiwan, ROC

Available online 15 August 2007

Abstract

Spin-on low-k passivation is achieved on inverted-staggered back-channel-etched hydrogenated amorphous silicon thin-film transistors (TFT). The low-k passivation material, siloxane-based hydrogen silsesquioxane (HSQ), has been investigated for different process temperatures. Performance is improved with decreased temperature. At 300 °C, the TFT performance of HSQ passivation is superior to those of other TFTs. The hydrogen bonds of HSQ assist hydrogen incorporation to eliminate the density of states between the back channel and the passivation layer. The characteristics of HSQ passivated TFT have been studied in this work.

© 2007 Published by Elsevier B.V.

Keywords: TFT; Passivation; Low-k; HSQ

1. Introduction

Inverted-staggered back-channel-etched (BCE) hydrogenated amorphous silicon thin-film transistors (a-Si:H TFTs) have been used as the switching devices in active matrix liquid crystal displays (LCDs) [1,2]. With larger displays, performance requirements of TFT devices become even more demanding. There is a great need for improving the aperture ratio and stability for BCE a-Si:H TFTs high resolution LCDs. In a large panel LCD, the transmittance and RC time delay are the important factors which need to be improved. To overcome these issues, low dielectric (low-k) materials with high transmittance and good planarization passivated on high resolution and high aperture ratio TFT-LCD panels have been proposed recently [3–7]. In BCE a-Si:H TFT processes, a passivation layer is necessary to protect the back channel from damage and contamination during subsequent processing. For the conventional BCE TFT devices, plasma-enhanced chemical vapor deposition (PECVD) silicon nitride (SiN_x) is used as the passivation layer. However, PE-SiN_x with its relatively high dielectric constant (~7), high stress and low transmittance, limits the brightness and

resolution of the display. For conventional structures, it is hard to extend the ITO pixel electrode to control the liquid crystal which limits the aperture ratio of TFT-LCD panel, as shown in Fig. 1(a). Therefore, the hydrogen silsesquioxane (HSQ) dielectric layer passivated on the TFT has been proposed to increase the aperture ratio and decrease the RC time delay between the gate line and data line, as shown in Fig. 1(b) [7].

In this work, low-k dielectric HSQ ($k \sim 2.8$) was used to passivate a BCE a-Si:H TFT with different process temperatures. HSQ film has high transmittance in the visible light, good planarization properties and low stress. In a-Si:H TFT devices fabrication, process temperature affected the device performance very much. For a-Si:H TFT fabrication, low temperatures are required. HSQ passivated TFTs with different process temperatures were fabricated. Transmittance and stress of the HSQ films were studied. Also, characteristics of a-Si:H TFTs with HSQ passivation will be discussed.

2. Experimental procedure

The BCE a-Si:H TFT process consists of a bottom gate, a silicon nitride (SiN_x) gate insulator, undoped a-Si:H (i), phosphorus doped a-Si:H (n⁺ a-Si:H), source/drain electrodes and a passivation layer.

* Corresponding author.

E-mail address: tcchang@mail.phys.nsysu.edu.tw (T.-C. Chang).

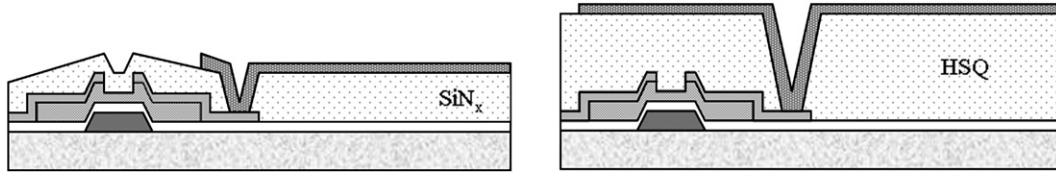


Fig. 1. The schematic diagram of the BCE a-Si:H TFT passivated by HSQ.

First, chromium was deposited on 4 inch substrate by sputtering and then was lithographically patterned to form the gate electrodes. Subsequently, SiN_x , undoped a-Si:H and phosphorous-doped a-Si:H layers were deposited on the Cr patterned substrate in a PECVD reactor sequentially without breaking vacuum. The SiN_x layer was deposited with a mixture of SiH_4 and NH_3 gases at a substrate temperature of 300°C and the undoped a-Si:H was deposited from a gas mixture of H_2 and SiH_4 at 300°C . The film thickness of the Cr, SiN_x , a-Si:H and n^+ a-Si:H was 300, 300, 180 and 40 nm, respectively. The active region was defined by a second photolithographic process after the tri-layer deposition. Aluminum was deposited with thermal coater, and the source/drain metal contacts were defined by third photolithography. Before the passivation formation, the substrate was divided into three groups, standard, HSQ, and PE- SiN_x samples. Finally, PE- SiN_x and HSQ were deposited on BCE a-Si:H TFT devices as passivation layers, respectively.

The samples were spin-coated with HSQ solution at 2000 rpm for 20 s. The low-k film, HSQ, coated on the standard sample was baked sequentially on hot-plates at 150°C , 200°C , and 250°C for 1 min. Afterward, the resultant samples were thermally cured in a quartz furnace at 300°C , 330°C , and 350°C for 1 h under N_2 ambient, respectively. All the electrical measurements were performed by using a Hewlett-Packard (HP) 4156A semiconductor parameter analyzer. The thicknesses were measured by n&k.

3. Results and discussions

The Fourier transform infrared spectra (FTIR) of HSQ films before and after a series of curing temperatures are shown in Fig. 2. The important peaks that appeared in the FTIR spectrum of HSQ films are indicated as follows. The peak near 2250 cm^{-1}

is identified as a Si–H stretching bond. The Si–H group makes the film surface hydrophobic and prevents the absorption of moisture. In addition, a Si–O stretching cage-like peak is present near 1130 cm^{-1} ; a Si–O stretching network peak near 1070 cm^{-1} ; a Si–O bending cage-like peak near 860 cm^{-1} , and a Si–O bending network peak is near 830 cm^{-1} [8–10]. The spectra of HSQ films cured at different temperatures are almost the same. Fig. 3 shows the optical transmittance of HSQ film and PE- SiN_x film, respectively. The optical properties are measured by ultraviolet visible spectrometer. In the visible range (300–800 nm), the optical transmittance of HSQ film is larger than PE- SiN_x film which has low transmittance (<90%). Table 1 show the stress and adhesion of HSQ and PE- SiN_x films, respectively. The stress is tensile for HSQ films, and SiN_x films have the compressive stress. The magnitude of the stress of PE- SiN_x film is ten times higher than the HSQ film. The adhesion force in Table 1 shows that the adhesion of PE- SiN_x is larger than HSQ film. The adhesion of the HSQ film is high enough for this film to act as a passivation layer for BCE a-Si:H TFT without peeling. From these properties, the deposited HSQ film can be thick for the high transmittance at here to the substrate and have low stress. On the contrary, in order to avoid dimming of the LCD panel and fracture of the glass substrate, PE- SiN_x can only be deposited in very thin layers because of its low transmittance and high stress.

Fig. 4 shows the I_d-V_g transfer characteristics of BCE a-Si:H TFTs with 350°C , 330°C , and 300°C curing of the HSQ passivation layer, respectively. The 350°C and 330°C cured HSQ passivated a-Si:H TFT have a lower on-current, higher off-current, poor subthreshold swing (S.S.) and a higher threshold voltage (V_T). These degraded characteristics resulted

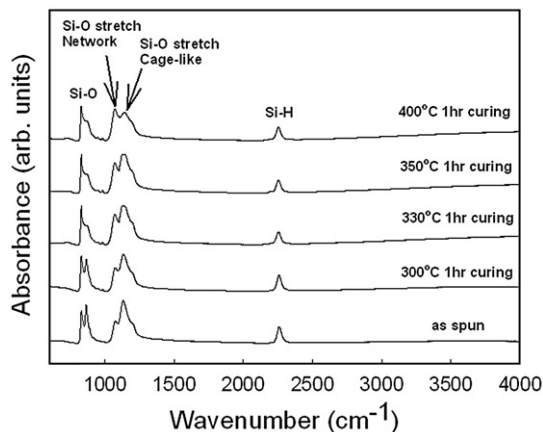


Fig. 2. FTIR spectra of HSQ before and after a series of curing temperatures.

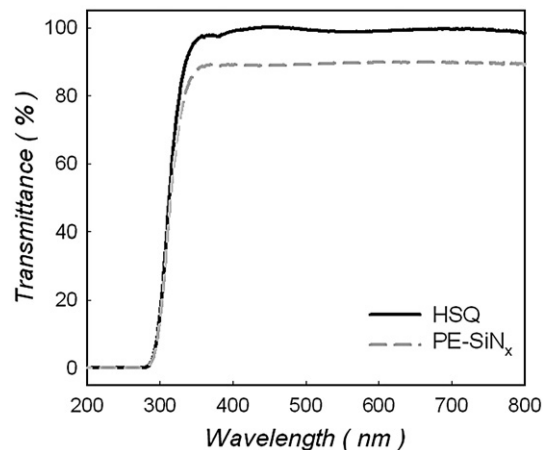


Fig. 3. The optical transmittance of HSQ and PE- SiN_x dielectric film deposited on glass substrate.

Table 1
(a) Stress comparison of HSQ and PE-SiN_x films, respectively (b) Adhesion comparison of HSQ and PE-SiN_x films, respectively

Stress	Thickness (Å)	Stress (MPa)	
HSQ	5000	56.5	Tensile
PE-SiN _x	2800	679	Compressive

Adhesion	Thickness (Å)	Stress (MPa)
HSQ	5000	29.71
PE-SiN _x	2800	41.14

from breaking the Si–H bonds of a-Si:H layers by temperature induced stress during the curing process. Thus, the high temperature curing step made the a-Si:H film generate large traps which deteriorated the TFT device performance. The 300 °C cured HSQ passivated TFT shows superior characteristics. This implied that this lower temperature does not lead to break the Si–H bonds. A TFT device fabricated with this layer could still have good I_d – V_g transfer characteristics. Fig. 5(a) and (b) shows the standard (STD) without any passivation layer and PE-SiN_x passivated a-Si:H TFT devices which were compared with 300 °C curing HSQ passivated TFT, respectively. In Fig. 5(a), HSQ passivated TFT has the higher on current, lower V_T than STD TFT. On the other hand, HSQ passivated TFT presented the similar characteristics to PE-SiN_x passivated TFT in Fig. 5(b), except the lower off-current. The on-current value of each TFT is shown in Fig. 6(a) and (b). In Fig. 6(a), 300 °C curing HSQ passivated TFT has the highest on current. The 350 °C and 330 °C cured HSQ passivated TFTs have poor on-current because of broken Si–H bonds and lower the μ . The on-current of 300 °C cured HSQ passivated TFT is also higher than PE-SiN_x passivated TFT as shown in Fig. 6(b). This may be due to minor interface states between the TFT back channel and the passivation layer. From the previous work [11], trap states at the back channel lead to worse electrical characteristics, such as off-current and S.S. The on-current, S.S., and off-current of HSQ passivated a-Si:H TFTs are improved by incorporating the hydrogen originated from the HSQ film. The

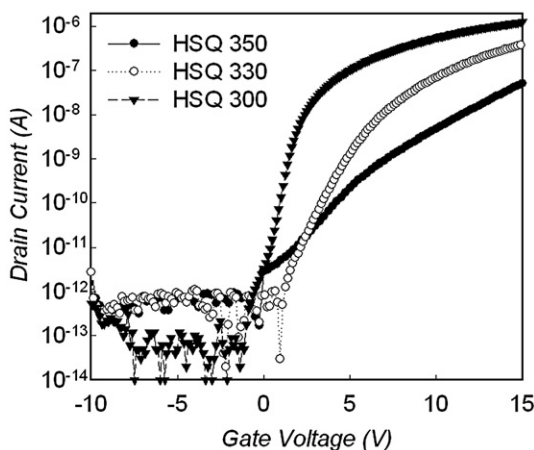


Fig. 4. The I_d – V_g transfer characteristics of BCE a-Si:H TFTs with 350 °C, 330 °C, and 300 °C curing HSQ passivation, respectively.

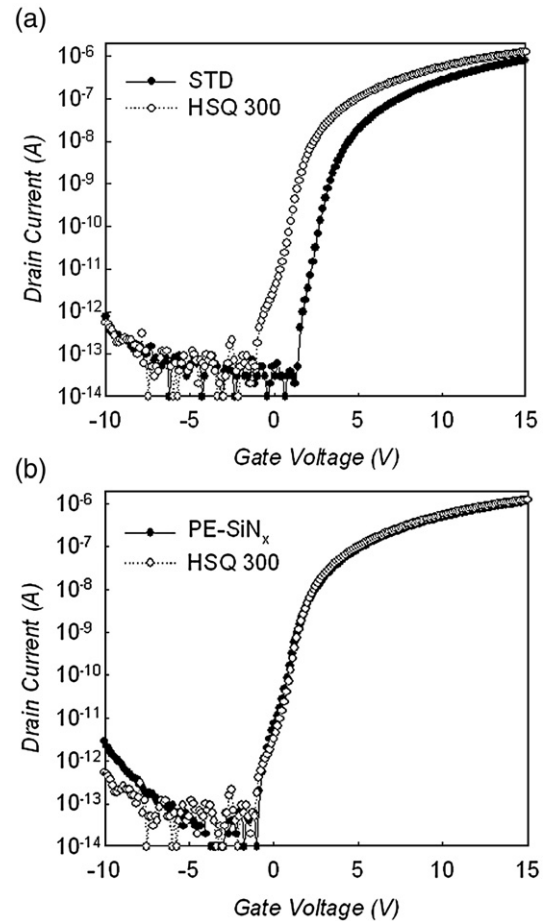


Fig. 5. (a) The I_d – V_g transfer characteristics of BCE a-Si:H TFTs with standard, and 300 °C curing HSQ passivation, respectively. (b) The I_d – V_g transfer characteristics of BCE a-Si:H TFTs with the PE-SiN_x and 300 °C curing HSQ passivation, respectively.

passivation at the HSQ/a-Si:H interface decreased the density of defect states, leading to the superior characteristics of TFTs. From the above comparison, 300 °C curing HSQ passivated TFTs have a better on/off ratio, higher mobility (μ) and lower V_T due to the hydrogen incorporation from HSQ passivation film. Because of instability of a-Si:H TFTs, the I_d – V_g transfer curves should be measured for many times to ensure that the TFT device is stable. The instability of different TFTs are shown in Fig. 7. The TFTs with passivation layer have stable characteristics whose V_T variation is small. The STD TFTs with the larger V_T variation (ΔV_T) may be due to the uncovered back channel. The TFT devices without passivation layer are damaged or contaminated easily. The most important instability in a-Si:H TFTs is a threshold voltage variation that is observed after the prolonged application of a gate voltage (bias stress). The stress conditions during testing were as follows: $V_g = +20V$, $V_s/V_d = \text{grounded}$ (to prevent the electrical field distortion), room temperature, and 5000 s, respectively. The threshold voltage variation as a function of stress time for STD, PE-SiN_x, and HSQ 300 °C passivated TFTs are shown in Fig. 8, respectively. The threshold voltage variation (ΔV_T) of STD, HSQ, and PE-SiN_x passivated TFTs are 1.58, 1.28, and 1.10, respectively. A moderate ΔV_T for a TFT with a passivation layer

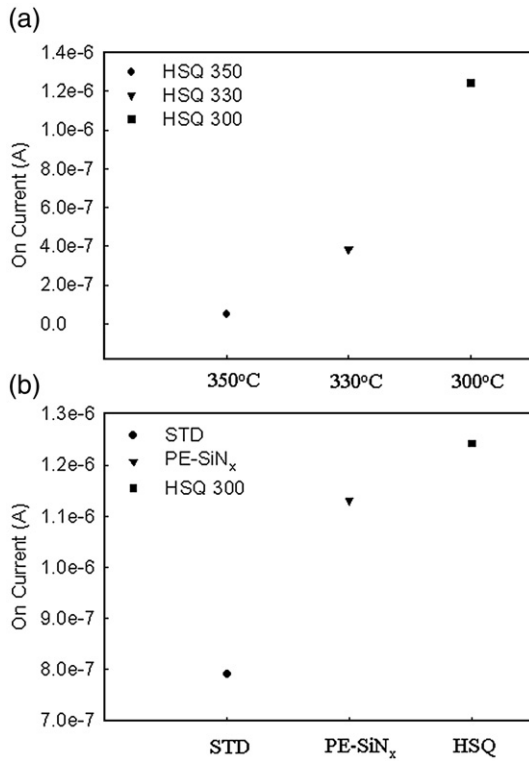


Fig. 6. (a) On current of BCE a-Si:H TFTs with 350 °C, 330 °C, and 300 °C curing HSQ passivation, respectively. (b) On current of BCE a-Si:H TFTs with the HSQ passivation, the SiN_x passivation and standard, respectively.

was observed. The good electrical characteristics are due to back channel protection. For HSQ passivation, hydrogen incorporation decreased the trap states at the back channel which leads to better electrical performance than STD. However, ΔV_T of HSQ passivated TFT is little higher than PE-SiN_x passivated TFT's. If this is due to the PE-SiN_x dense film, one way to improve this phenomenon is to increase the thickness of the HSQ to enhance the protection.

4. Conclusion

In this study, HSQ passivated a-Si:H TFTs have been demonstrated and their properties studied. In addition to lowering

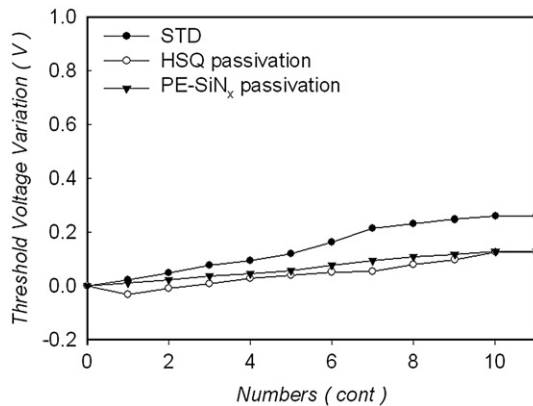


Fig. 7. Threshold voltage variation of the HSQ passivated a-Si:H TFT after many times measurement.

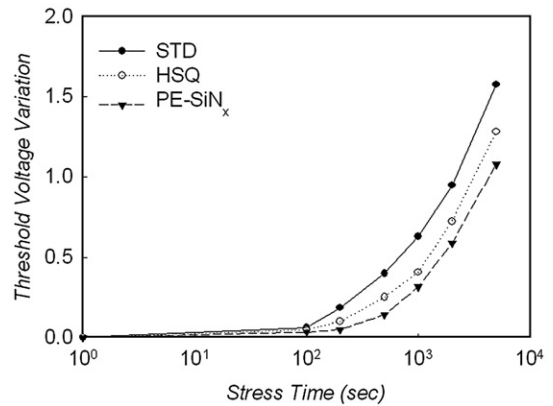


Fig. 8. Threshold voltage variation of the HSQ passivated a-Si:H TFT after stress.

the RC time delay with a lower dielectric constant, analyses shows that the low-k HSQ film has a high transmittance in visible light range and low stress. The good planarization of a HSQ film can provide a higher aperture ratio. When used HSQ as a passivation layer on a TFT, the optimum process temperature is 300 °C. The improved electrical characteristics of HSQ-passivated a-Si:H TFTs result from the incorporation of hydrogen. Furthermore, the back channel protection moderated the threshold voltage variation seen in TFTs. Thus, HSQ may be used as a passivation layer which is compatible with BCE a-Si:H TFT.

Acknowledgement

This work was performed at the National Nano Device Laboratory and supported by the Republic of China National Science Council through a grant No. NSC-94-2120-M-110-005, NSC-94-2215-E-009-031 and Dow Corning Taiwan Inc. Also, this work was partially supported by MOEA Technology Development for Academia Project# 94-EC-17-A-07-S1-046.

References

- [1] H. Yamamoto, H. Matsumaru, K. Shirahashi, M. Nakatani, A. Sasano, N. Konishi, K. Tsutsui, T. Tsukada, IEDM Tech. Dig. (1990) 851.
- [2] Y. Tanaka, M. Shibusawa, M. Dohjo, O. Tomita, S. Uchikoga, SID International Symposium Digest of Technical Papers, vol. 23, SID, Boston, 1992.
- [3] R. Jeyakumar, K.S. Karim, S. Sivorthaman, A. Nathan, Proc. 23rd International Conference on Microelectronics (MIEL 2002), Yugoslavia, 12–15 May 2002, p. 543.
- [4] J.H. Kim, H.S. Soh, Proc. AMLCD, 1997, p. 5.
- [5] Je-Hsiung Lan, Jerzy Kanicki, Proc. SPIE 3421 (170) (1998).
- [6] Wan-Shick Hong, Kwan-Wook Jung, Joon-Hoo Choi, Byung-Keun Hwang, Kyuha Chung, IEEE Electron Device Lett. 25 (June 2004) 381.
- [7] T.S. Chang, T.C. Chang, P.T. Liu, T.S. Chang, F.S. Yeh, Thin Solid Films 498 (2006) 70.
- [8] V. McGayay, A. Acovic, B. Argarwala, G. Endicott, M. Shapiro, S. Yankee, Int. VLSI Multilevel Interconnection Conf. Proc., 1996, p. 116.
- [9] M.J. Loboda, C.M. Grove, R.F. Schneider, J. Electrochem. Soc. 145 (1998) 2861.
- [10] D. Thomas, G. Smith, Dielectrics for ULSI Multilevel Interconnection Conf., 1997, p. 361.
- [11] M.J. Powell, J. Pritchard, J. Appl. Phys. 54 (6) (June 1983) 3244.