time. No difference was noticed for the average output power between the mode-locked and CW modes of operation. To measure the width and peak power of the pulses we took

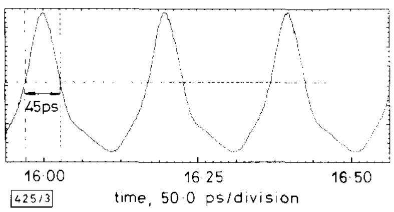

Fig. 3 *Electronically observed mode-locked pulse train*
Pulse width = 45 ps
delay = 16·0 ns

advantage of the low power green light (0·542 μm) that was intracavity generated by self-frequency-doubling both in the form of guided and Cerenkov[5] radiations. Fig. 4 shows the square root of the measured guided green average power as a function of the laser (1·085 μm) average output power for mode-locked and CW operation. The ratio of the average mode-locked green power to the CW power is ~19 at all the laser output powers and is equal to the ratio of the peak fundamental (1·085 μm) power to the CW power so that 13 mW CW corresponds to 250 mW peak power. From this, and assuming a Gaussian pulse shape, an 8 ps pulse width (FWHM) can be calculated. The same result was obtained by

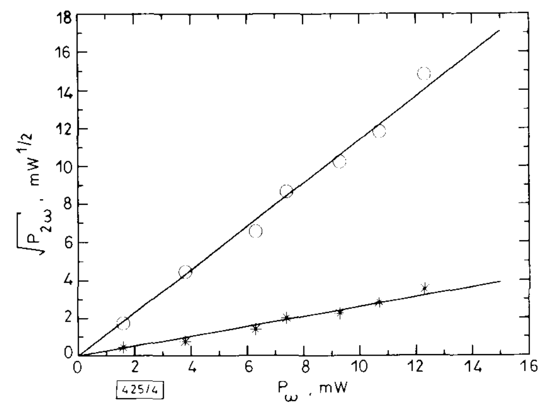

Fig. 4 *Average $\sqrt{P_{2\omega}}$ as function of average P_ω in CW and mode-locked operation*
* CW operation
○ mode-locked operation

recording the Cerenkov green power. Finally the 10 ps FWHM pulse trace recorded in a nonbackground-free autocorrelation measurement[6] indicated complete mode-locking and yielded a 7 ps pulse width assuming a Gaussian pulse shape, and a time-bandwidth product of 0·71 ($\Delta\lambda = 4$ Å, resolution = 1 Å) which is close to the minimum of 0·62 for FM mode-locked lasers.[6]

Conclusion: We have reported for the first time an integrated FM mode-locked singlemode waveguide laser in Nd:MgO:LiNbO$_3$. With 45 mW of absorbed optical pump power and 7 V RMS/6·2 GHz RF drive signal the laser output consisted of a 6·2 GHz periodic train of 250 mW peak power and 8 ps wide pulses at 1·085 μm. Similar performances should be obtained by using an GaAlAs diode laser as the pump source and result in a compact and efficient device useful for many applications.

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OVERFLOW CONTROLLER IN COPY NETWORK OF BROADBAND PACKET SWITCH

Indexing terms: Digital communication systems, Algorithms

An overflow controller for a copy network in a broadband packet switch is proposed and designed. This overflow controller implemented by a new dummy address encoding process has five modes of operation to determine how the input multicast packet is served (switched). The controller can not only resolve the overflow problem but also make the copy network a high throughput network.

Introduction: One essential feature of a broadband packet switch is to support multicast services such as video conferencing or entertainment video. For this purpose, the switch has to have the capability of point-to-multipoint (multicast) connection. Examples of multicast broadband packet switches are the Starlite system,[1] the broadcast packet switch,[2] and the nonblocking copy network.[3] However, the overflow problem in these switches that occurs when the total number of copy requests summed over all input packets per slot exceeds the number of output links, was not addressed in References 1 and 2, and just simply mentioned by regulating the input packets in Reference 3.

In this Letter, an overflow controller implemented by a *new* dummy address encoding process in a copy network is addressed. The overflow controller permits only the number of packets which totally have min(M, N) copy requests (CRs) to be served, where M is the sum of copy requests of all incoming packets and N is the number of input/output links, and the copy network is to replicate served packets according to the copy requests contained in the address intervals of their packet headers. This copy network can thus overcome the overflow problem and achieve full use.

Network operation and design: As shown in Fig. 1, the copy network consists of a running adder network (RAN) and an address comparator (AC), an overflow controller (OC), and a concentrator and broadcast banyan network (CBBN). It serves N input links synchronously and cyclically on a time slot basis. At the beginning of a time slot, the RAN sums up the copy requests of packets in all input links cyclically from residual copy requests of the packet in the service-incomplete link of the last time slot; the AC of each link then detects

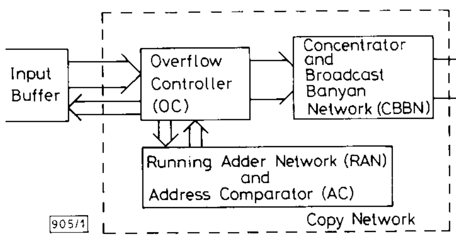

Fig. 1 *Block diagram of copy network*

whether an overflow has occurred at this link or not. The overflow may happen at more than one link in a slot, and the addresses of overflow links are stored cyclically in the OC. In each slot, the OC serves the packets lying between the first two overflow links in a first-come-first-served manner, and it splits copy requests of the packet in the latter one of the two overflow links into two parts. The former part of the copy requests of this packet together with the copy requests of the packets belonging to the links before it forms a set of N copy requests. The latter parts of the copy requests of this packet are named the residual copy requests. The copy network will serve the N copy requests at this time slot, whereas the residual copy requests will remain in the input buffer of the network and wait for the operation of the next time slot.

Fig. 2 shows the configuration of the RAN and ACs if an $N = 8$ copy network is considered. Notice that the last running sum is fed back to the input of adder node A of the first link so that the copy requests can be added up cyclically. In the RAN, there is an output of running sum S_k corresponding to each link k, $1 \leq k \leq N$. The S_k is fed to the ACs of itself and the next link, respectively. Each AC performs comparison of the adjacent running sums to determine whether there is an overflow or not and generates an address interval (S_{k-1}, S_k) output to the OC. For the adjacent running sums S_{k-1} and S_k, the overflow occurs at this link if $S_{k-1} > S_k$. Whenever an overflow occurs, an INH_k signal is stimulated. As shown in Figs. 3 and 4, this INH_k signal will inhibit a flipflop of its adder node in the RAN such that S_{k-1} of the previous slot remains unchanged, and disable the AC of itself such that no

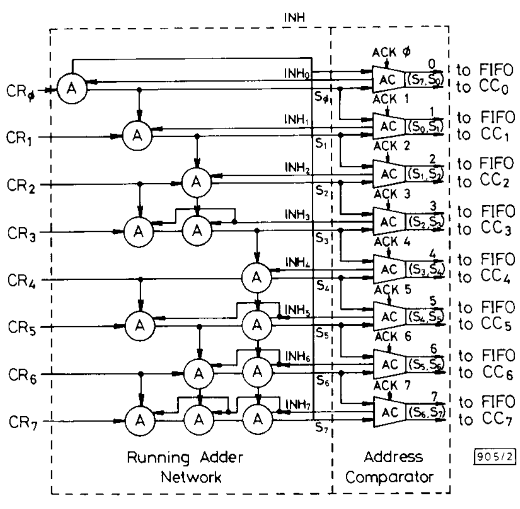

Fig. 2 *Functional block diagram of running adder network and address comparator*

A = adder node
CR = copy request
AC = address comparator
FIFO = first-in-first-out
CC = control cell

comparison is performed during the active period of the INH_k signal. Also the INH_k signal will trigger the AC to send its link address to a first-in-first-out (FIFO) in the OC to mark that link k is an overflow one. The INH_k signal will be reset by an ACK signal from the OC. The ACK signal is generated whenever a multicast packet is completely served.

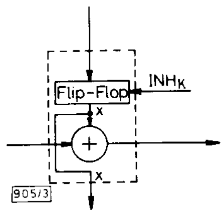

Fig. 3 *Adder node of running adder network*

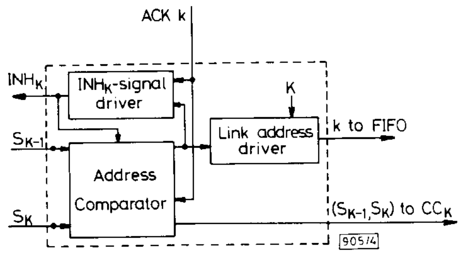

Fig. 4 *Address comparator k*

The overflow controller determines the flow of the incoming multicast packets. Fig. 5 shows the block diagram of the OC. It has a common FIFO and control cell (CC) for each link. The FIFO sequentially stores the input link addresses where overflows have occurred, but it stores all high bits if it contains nothing. The first two link addresses in the FIFO are called the current transmission group (CTG) which denotes that the copy requests of packets within these two links will be served at the present slot. In this Figure the CTG is from link f to link g. Fig. 6 shows the configuration of control cell k (CC_k). It has a register, a dummy address encoder (DAE), and a switch. The register temporarily stores the input multicast packets I_k from the input buffer. The copy requests (CR_k) of the input packet are also sent to the RAN as input. The DAE_k

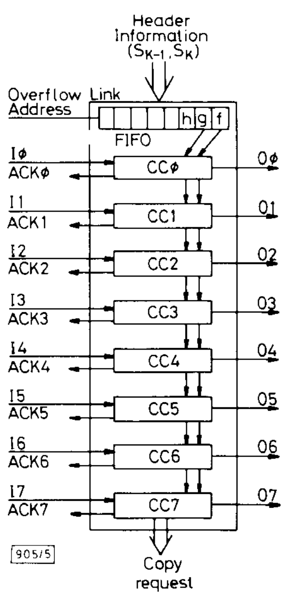

Fig. 5 *Functional block diagram of overflow controller*

receives header information (S_{k-1}, S_k) from the AC and forms three pieces of dummy header information $(S_{k-1}, S_k - 1)$, $(S_{k-1}, N - 1)$, and $(0, S_k - 1)$. The switch determines the operation mode with the CTG (f, g) and its link address k via the following control mechanism. Let $p = (g - f) \mod N$, $q = (k - f) \mod N$, and the CC_k operate in one of the five operation modes.

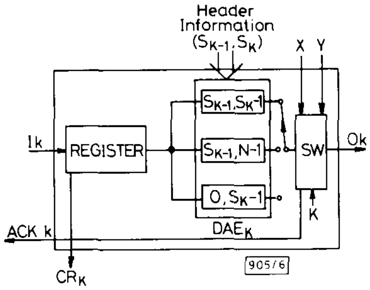

Fig. 6 *Functional block diagram of control cell k*

DAE = dummy address encoder
SW = switch
CC = control cell

Mode 1: if $q > p$, its input multicast packet is not permitted to transmit

Mode 2: if $q = 0$, its input multicast packet is transmitted with header $H_k = (0, S_k - 1)$, and $ACK\ k$ signal is sent

Mode 3: if $q < p$, its input multicast packet is transmitted with header $H_k = (S_{k-1}, S_k - 1)$, and $ACK\ k$ signal is sent

Mode 4: if $q = p$, its input multicast packet is transmitted with header $H_k = (S_{k-1}, N - 1)$

Mode 5: if g is absent (all bits are high), the input multicast packet k is transmitted with header $H_k = (S_{k-1}, S_k - 1)$, $1 \le k \le N$, the contents of the FIFO are reset to the initial state where the first word of the FIFO is set to zero (notice that the other words are still all high) line 0 is set to an inhibit state, and the $ACK\ k$ signal is sent.

Mode 1 denotes the operation of link k which is out of the CTG, modes 2, 3, and 4 denote the operation of link k which is the first link, the middle links, and the last link of the CTG, respectively, and mode 5 denotes the operation of the overflow controller which is in an underflow condition. The multicast packet of link g in the CTG may be transmitted twice. For the first time, the CC_k is operated in mode 4 at the present slot; the second time it is operated in mode 2 in the next slot. The ACK signal is not sent in mode 4 because there are still copy requests of the multicast packet waiting in the buffer for transmission in the next slot. At the end of a slot, link addresses f and/or g will be deleted if it is completely served. Using this mechanism, the overflow can be overcome and full use of the output lines can be achieved.

For clarity, an example is illustrated in Table 1, where $X_k(j)$ denotes the variable X of link k at the jth slot, X may be CR, S, INH, or H. In this example, two consecutive time slots i and $i + 1$ are demonstrated. At the beginning of the ith slot, we assume the overflow controller is as in initial state where only $f = 0$ in the FIFO and $S_7(i - 1) = 0$.

The CBBN has similar operation to that in Reference 3. Its function is to replicate packets to the outputs of the copy network nonblockingly according to the address interval in the packet header.

Conclusion: This Letter describes an overflow controller in the copy network of a broadband packet switch. An overflow control algorithm so that the network can pass the copy requests as the same number of output ports as possible is proposed. There are five modes of operation for each input packet in the overflow controller, with which the overflow problem can be resolved and the high throughput for the network achieved.

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3rd January 1991

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Table 1 EXAMPLE

Time slot i

k	$CR_k(i+1)$	$CR_k(i)$	$S_k(i)$	$[S_{k-1}(i), S_k(i)]$	$INH_k(i)$	Mode	$H_k(i)$	$ACK\ k$
0	2	2	2	(0, 2)	0	2	(0, 1)	1
1	3	3	5	(2, 5)	0	3	(2, 4)	1
2	2	4	1*	(5, 1)	1	4	(5, 7)	0
3	3	2	3	(1, 3)	0	1		0
4	2	1	4	(3, 4)	0	1		0
5	1	2	6	(4, 6)	0	1		0
6	4	3	1*	(6, 1)	1	1		0
7	3	2	3	(1, 3)	0	1		0

Time slot $i + 1$

k	$CR_k(i+2)$	$CR_k(i+1)$	$S_k(i)$	$[S_{k-1}(i), S_k(i)]$	$INH_k(i)$	Mode	$H_k(i)$	$ACK\ k$
0	#	2	5	(3, 5)	0	1		0
1	#	3	0*	(5, 0)	1	1		0
2	2	4	1*	(6, 1)	1	2	(0, 0)	1
3	3	2	3	(1, 3)	0	3	(1, 2)	1
4	2	1	4	(3, 4)	0	3	(3, 3)	1
5	1	2	6	(4, 6)	0	3	(4, 5)	1
6	4	3	1*	(6, 1)	1	4	(6, 7)	0
7	3	2	3	(1, 3)	0	1		0

# denotes 'don't care'
* denotes overflow link