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DESIGN NOTE

A timing stabilized laser diode based range simulator

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Abstract. A timing stabilized laser diode based range simulator has been demonstrated. Range simulation is achieved by locking the time delay between the reference signal generator and the time base of the output light pulse using a double phase-lock-loop. Phase stabilization to within 1.0×10^{-5} rad $Hz^{-1/2}$ has been implemented within the range $-\pi$ to $+\pi$ rad.

It is well known that a transistor may be operated in the avalanche breakdown region to generate a fast-rising, high current laser pulse output [1–4]. This light pulse may be used as the light source for such applications as laser range finders, missile laser fuse systems and fibre OTDR [5–9]. But under these applications, the timing and the amplitude of the returned light are the most important factors for signal detection. The standard detection method is to adjust the timing delay from the reference signal to the returned signal, achieved using an analogue or digital delay line added into the reference signal generator, to generate a sampling gate signal to the boxcar integrator for returned pulse signal detection [10–12]. In this set-up, however, the phase noise inherent in the reference signal, the electron device, and the laser diode pulse driver are still exhibited in the system. In order to improve timing stabilizaion (i.e. reduce timing jitter), an active timing stabilized system was employed in the mode-locked Nd:YAG laser [13]. In this design note, we seek to demonstrate such a system based on a laser diode source. By comparison with [14], the advantages of the system are (1) that the timing jitter can be stabilized at any value of the phase difference, from $-\pi$ to $+\pi$ rad, and (2) that the linearity and the dynamic range characteristics of the voltage controlled phase shifter are improved by use of the phase-lock-loop technique [14]. Thus we believe that this system is suitable for use as a timing simulator.

The block diagram of the timing stabilization system is shown in figure 1. The reference trigger signal of frequency f_r is obtained from the synthesizer output. Two types of phase-lock-loop circuits are employed in the system. The phase-lock-loop PLL1 is used as a voltage controlled phase delay unit. It consists of a $-\pi$ to $+\pi$ phase detector, a loop filter of PI type (proportional and integrating) and a voltage controlled oscillator. When the PLL1 is worked, the phase offset between the two input signals to the phase comparator is adjusted by the voltage applied to the PI loop filter input. Thus the phase shift is controlled, from $-\pi$ to $+\pi$ rad, by the output of the loop filter PLL2. After phase shift in the loop, the output signal from the VCO, which has been narrowed using a monostable device to generate a short pulse trigger signal, is applied to the base of the avalanche transistor. The collector of this transistor is biased at 150 V, i.e. the avalanche region. The pulse width of the output of the laser diode is controlled by the length of the 50 Ω delay line according to the relation $t_w = 2L/c$, and is selected as 10 ns. The size of the current pulse used to drive the laser diode is controlled by the bias voltage to the transistor collector and the series 100 Ω variable resistor to the laser diode according to the relation $I = V_{br}/Z_o + Z_r$, where V_{br} is the collector–emitter voltage within the avalanche region (negative resistance region) of the transistor and Z_o and Z_r are the impedances of the delay line and the 100 Ω variable resistor respectively. The light output from the laser diode is coupled into a fibre coupler. The 100 M length of fibre spliced to the fibre coupler is used to simulate the reflection of light from a target, and the magnitude of the returned signal can be altered by adjusting the flatness of the fibre end. One end of the fibre coupler is placed within optically matching oil to eliminate reflected light.

Timing stabilization is implemented by the phase-lock-loop PLL2, where the light pulse returned from the fibre end is first detected via a fast comparator. Thus an output pulse is regenerated. The 2 × dividers are used to generate 50% duty cycle square-wave signals, thus eliminating the effects of duty cycle variation on phase detection. The phases of these two output signals from the dividers are then compared with each other in a

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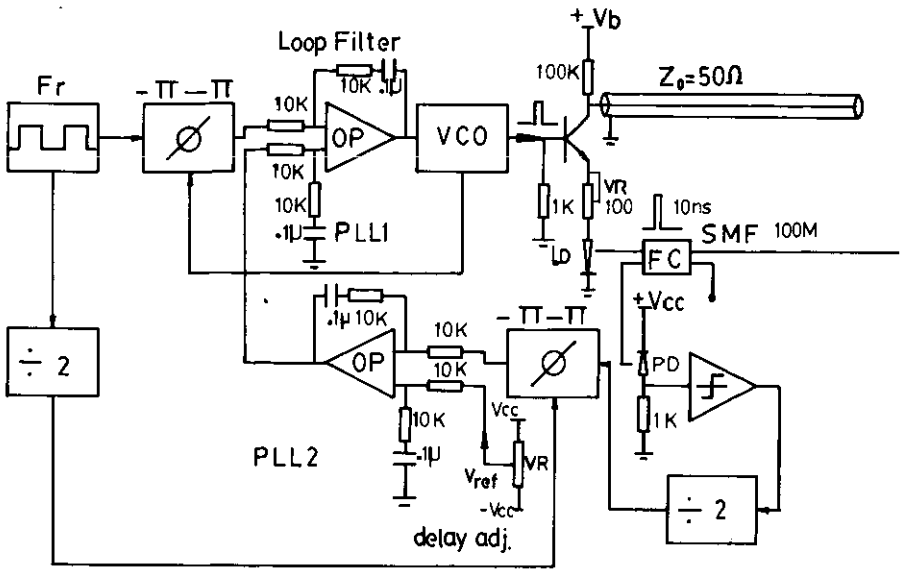

Figure 1. The block diagram of the timing stabilized system, based on a double phase-lock loop: ϕ, phase comparator; VCO, voltage controlled oscillator; LD, laser diode; FC, fibre coupler; SMF, single-mode fibre; F_r, reference signal generator.

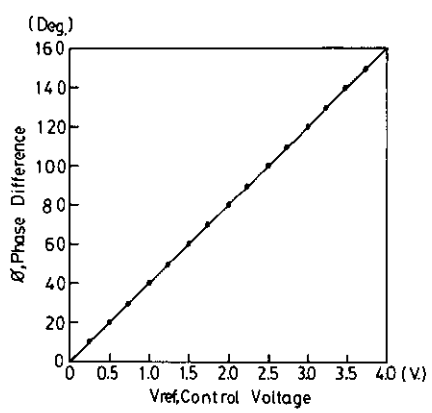

Figure 2. Relation between phase difference (time delay) of laser pulse output and phase delay control voltage, V_{ref}.

phase comparator with a range of $-\pi$ to $+\pi$ rad. The output error signal is compared with a reference voltage at the input port of the loop filter LP2. The output signal from the loop filter LP2 controls the phase delay in PLL1 until the error signal at the loop filter is at a null situation. The phase fluctuations can be stabilized to within 1.0×10^{-5} rad $Hz^{-1/2}$. For example the reference frequency 100 kHz in our system corresponds to timing jitter of less than 16 ps. The relation between the control voltage and the phase delay of the output pulse signal is shown in figure 2. It is clear that our timing stabilized, adjustable laser diode based range simulator system exhibits good phase linearity.

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References

[1] Motorola Inc. 1980 *High speed switching transistor handbook* chapter 9
Herman E B and Robert A B 1966 Avalanche transistors drive laser diodes hard and fast *Electronics* 137–9
[2] Carroll R 1971 Different ways of driving a pulsed injection laser *Electronics* 59–62
[3] Dong S, Krause W, Volker F and Weber H 1986 Fast $\lambda/4$ and $\lambda/2$ Voltage Pockels cell driver for an internally seeded and cavity dumped regenerative laser amplifier *Rev. Sci. Instrum.* **57** 539–43
[4] Ahola R and Myllyla 1984 A time-of-flight laser sensor for to and fro motions *Proc. IECON'84 Tokyo* 812–8
[5] Goldstein B S and Dalrymple G F 1967 Gallium arsenide injection laser radar *Proc. IEEE* **55** 181–8
[6] Koechner W 1968 Optical ranging system employing a high power injection laser diode *IEEE Trans. Aerosp. Electron. Syst.* **AES-4** 81–91
[7] Salathe R, Bolleter W and Gilgen H 1977 Long range injection radar *Appl. Opt.* **16** 2621–3
[8] Mamon G, Youmans D G, Sztenkay Z G and Mongan C E 1978 Pulsed GaAs laser terrain profiler *Appl. Opt.* **17** 868–77
[9] Healey P 1985 Review of long wavelength single-mode optical fiber reflectometry techniques *IEEE J. Lightwave Technol.* **LT-3** 876–86
[10] Berkeley Nucleonics Corp. 1985 *Service Manual Digital Delay Generators Mode-7030A*
[11] Hewlett Packard Corp. 1985 *Service Manual 500 MHz Pulse Generator Model HP-8131A*
[12] Stanford Research System 1986 *Service Manual DG535 Four Channel Digital Delay/Pulse Generator*
[13] Mark J W 1989 Subpicosecond laser timing stabilization *IEEE J. Quantum Electron.* **QE-25** 817–27
[14] Gardner F M 1980 *Phaselock Techniques* (New York: Wiley)