# 國 立 交 通 大 學

## 電機學院通訊與網路科技產業研發碩士班

## 碩 士 論 文

有效控制靜態耗電流之高功率高線性度 AB 類音頻放大器

High Output-Power High Linearity CMOS Class AB Audio
Amplifier with Quiescent Current Control

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# High Output-Power High Linearity CMOS Class AB Audio Amplifier with Quiescent Current Control
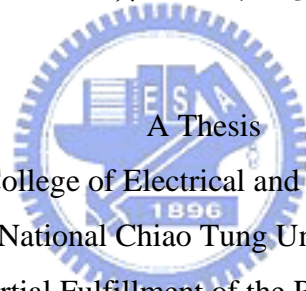
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# 有效控制靜態耗電流之高功率高線性度 AB 類音頻放大器

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## 國立交通大學電機學院產業研發碩士班

## 摘　　　要

隨著行動化個人多媒體時代的來臨，具有較高功率轉換效率之 D 類音頻放大器逐漸的備受重視。但是其線性度較差的缺點往往需要透過較複雜的時脈調變機制或是補償控制來彌補。這對於某些需求僅僅著重在高輸出功率，高線性度，低失真的傳統應用來說，並不一定是最適合架構。

此篇論文將以業界的商用規格為目標，設計具有高輸出功率, 低失真之 AB 類線性音頻放大器。並包含音量控制，耳機輸出，短路保護等功能。

一般而言，線性音頻放大器之負載阻抗約為 8 歐姆，輸出級必須具備極大的電流驅動能力。輸出級的設計對放大器的靜態耗電流、功率轉換效率與線性度有決定性的影響。本論文創新之處在於利用精簡的架構控制輸出級之靜態耗電流，避免靜態耗電流與線性度受到製程漂移之影響，造成不穩定的現象。此 AB 類輸出級的架構採用共源極組態之功率電晶體並搭配誤差放大器，藉由降低誤差放大器之增益達到控制靜態耗電流的目標。此誤差放大器之增益將隨著輸出功率增加而提高，當增益提高時，線性度也隨之上升。另外，誤差放大器寬廣的輸出共模範圍，使受其控制的功率電晶體可以用較小的面積達到所需的輸出功率。

晶片製作是採用聯華電子 0.5um +/-20V2P2M 製程。並且可在寬廣供應電壓範圍 10~18V 之間使用。當供應電壓為 18V，負載為 8 歐姆，輸出功率為 2W 時，總諧波失真大約為 0.060 %

High Output-Power High Linearity CMOS Class AB Audio
Amplifier with Quiescent Current Control

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Industrial Technology R & D Master Program of
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## ABSTRACT

With the advent of a highly-mobilized and individualized multimedia age, Class-D audio amplifiers with better power efficiency, among the applications of its kind, have gained a lot of attentions. However, in view of the fact that traditionally high output power, good linearity, and low distortion are expected in amplifiers alike, Class-D audio amplifiers may not be an ideal choice since it requires a complicated clock modulation or a compensatory control mechanism to make up to its poor output linearity.   To look for an applicable alternative, therefore, this thesis puts forth a Class-AB linear audio amplifier that not only meets the design specification of business application, but also equips with features such as volume control, earphone output ports, short-circuit protection, and other functions desired in a multimedia product.

In general, a linear audio amplifier has a load impedance of approximately 8 ohm, so its output stage must have a compatibly large current drive, whose design has a significant influence on the quiescent current, power efficiency, and linearity. These deciding factors in designing a linear audio amplifier thus reveal the originality of this thesis: to rid the unwanted quiescent current of the output

stage and unstable linearity resulted from process variation with a succinct structure. The Class-AB output stage adopts common-source power transistors with error amplifiers. By decreasing the gain of the error amplifier, the quiescent current is successfully controlled. Since the gain of the error amplifier will increase as the output power rises, it will therefore enhance the linearity. Besides, its output common mode range is the same as the supply voltage, which is sufficient enough to drive a smaller-sized power transistor to achieve the desired output power.

The chip is fabricated by the UMC 0.5um +/-20V2P2M high voltage process. It could undertake a high supply voltage ranging from 10V to 18V. The total harmonic distortion is approximately 0.060 % provided that the load impedance is 8 ohm and the output power is 2 watt under an 18V supply voltage.

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# CHAPTER 1

# Introduction

## 1.1    Background

With the advent of a highly-mobilized and individualized multimedia age, Class-D audio amplifiers with better power efficiency, among the applications of its kind, have gained a lot of attentions. However, in view of the fact that traditionally high output power, good linearity, and low distortion are expected in amplifiers alike, Class-D audio amplifiers may not be an ideal choice since it requires a complicated clock modulation or a compensatory control mechanism to make up to its poor output linearity.

Take audio amplifier applications, such as flat panel monitors and flat panel TVs, for example. These systems are usually equipped with a considerably high DC voltage source of 12V, 18V, or even 40V in order to drive their LCD display devices. In these cases, instead of using the relatively more complicated Class-D amplifiers, applying linear audio amplifiers would simply result in a high output power and high linearity as expected.

Most audio amplifiers have very small output resistance load, usually somewhere between 4 to 32Ω. Therefore, to ensure a desired amount of signal power delivery at the load with signal distortion within tolerance, the output stage usually consists of a voltage buffer with high input impedance and very low output impedance. Generally, these linear output stages can be divided into three categories [1], as shown in Table1-1. Among the three, Class-AB output stage, with better power efficiency and satisfactory linearity, is by far more applicable in practice. Therefore, we will next introduce some Class-AB output stage structures in the hope that we can compare them with structures of other kinds to find out their

advantages and disadvantages.

| Type | Maximum power efficiency | Linearity | characteristic |
|---|---|---|---|
| Class-A | <25% | Good | Poor power efficiency |
| Class-B | <78.5% | Poor | Crossover distortion |
| Class-AB | 25% ~ 78.5% | Good | Suitable performance |

**Table 1-1** Comparison of linear output stage

### 1.1.1　　Review of the class-AB output stage architecture

## (1) Common-Drain configuration [1]
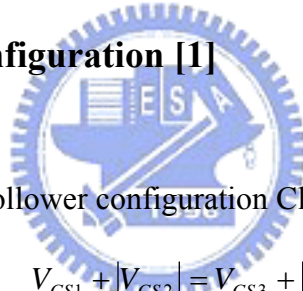
Fig.1.1 shows a Source-follower configuration Class-AB output stage. From KVL,

$$V_{GS1} + |V_{GS2}| = V_{GS3} + |V_{GS4}| \tag{1.1}$$

With the body effect ignored, $V_{GS3} + |V_{GS4}|$ is constant if the bias current $I_{B1}$ is constant.

Under these conditions, increasing $V_{GS1}$ decreases $|V_{GS2}|$ and vice versa. Assume all devices

have same threshold voltage in the quiescent condition. Equation 1.1 can be re-written as

$$\sqrt{\frac{2I_{D1}}{k_n^{'}(W/L)_1}} + \sqrt{\frac{2I_{|D2|}}{k_p^{'}(W/L)_2}} = \sqrt{\frac{2I_{B1}}{k_n^{'}(W/L)_3}} + \sqrt{\frac{2I_{B1}}{k_p^{'}(W/L)_4}} \tag{1.2}$$

If $V_O = \dfrac{V_{DD} - V_{SS}}{2}$, then $I_{D2} = -I_{D1}$ and (1.2) can be rearranged to give

$$I_{D1} = I_{D4}\left(\frac{1/\sqrt{k_n^{'}(W/L)_3} + 1/\sqrt{k_p^{'}(W/L)_4}}{1/\sqrt{k_n^{'}(W/L)_1} + 1/\sqrt{k_p^{'}(W/L)_2}}\right)^2 \tag{1.3}$$

The key point of equation 1.3 is that the quiescent current in the output transistors is

well-controlled with respect to the bias current that flows in the diode-connected transistors.

.An important problem with this circuit is that its output swing is limited by the source

follower configuration at the output node. Assume $V_{SS} = -V_{DD}$ . $V_O < 0$, $V_{sg2} > |V_{t2}|$, and M$_2$

acts as a source follower. Therefore,

$$V_{O(\min)} = V_{SS} + V_{OV5} + V_{sg2} = -V_{DD} + V_{OV5} + V_{sg2} \qquad (1.4)$$

The maximum output voltage can be derived by similar reasoning. From (1.4), the output

swing can't reach the supply voltage, and the difference varies with the biasing condition.

Since the source is the output node, the MOS device becomes dependent on the body effect.

The body effect causes the threshold voltage $|V_{t2}|$ to increase as the output voltage is

decreased. Also, the source-gate overdrive voltage rises while the output current increases. In

practice, the output voltage swing can be increased by increasing the W/L ratios of the output

devices to reduce their overdrives. However, in such doing, the required transistor sizes are

sometimes too large to be economical.
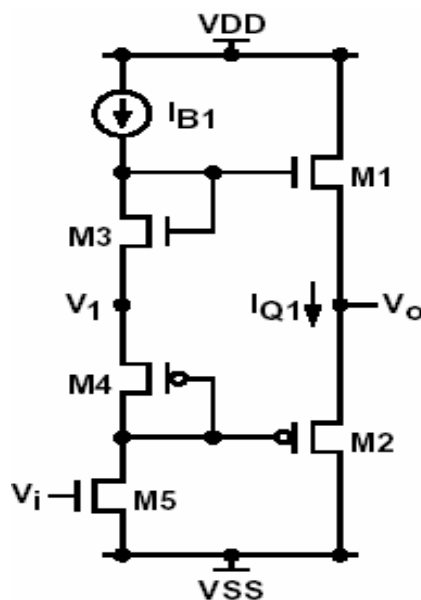


**Figure 1.1** Source follower Class-AB output stage.

## (2)　Common-Source configuration

　　The problem of limited output swing in Common-Drain configuration can be improved by another alternative [2]. Fig.1.2 shows a Class-AB Push-Pull Common-Source output stage.

Let $I_{B1} = I_{B2} = I_{B3}$, and $\dfrac{1}{K}\left(\dfrac{W}{L}\right)_1 = \left(\dfrac{W}{L}\right)_{11}$, $\left(\dfrac{W}{L}\right)_3 = \left(\dfrac{W}{L}\right)_{12}$, $\dfrac{1}{K}\left(\dfrac{W}{L}\right)_2 = \left(\dfrac{W}{L}\right)_{13}$, $\left(\dfrac{W}{L}\right)_4 = \left(\dfrac{W}{L}\right)_{14}$. Then, $V_{GS1} = V_{GS11}$, $V_{GS3} = V_{GS12}$, $V_{GS2} = V_{GS13}$, $V_{GS4} = V_{GS14}$, and

$$I_{Quiescent} = I_{D1} = I_{D2} = KI_{B1} \tag{1.5}$$

Equation (1.5) shows that the quiescent current of this circuit can be controlled by the W/L ratio. $M_3$ and $M_4$ form a floating resistor which is biased by $M_{11}$, $M_{12}$, $I_{B2}$, and $M_{13}$, $M_{14}$, $I_{B3}$ respectively. Compared with the aforementioned Common-Drain configuration, the output voltage in discussion here can reach $(V_{DD} - V_{OV1})$, or $(V_{ss} + V_{OV2})$ as the maximum output swing. $M_1$ and $M_2$ in the Common-Source Configuration form large output impedance at the output node. For general application, the pole at $V_O$ can be significant. However, the loading impedance in a linear audio amplifier can be as small as 8 ohm. Such a large output impedance will cause serious signal loss and poor linearity.
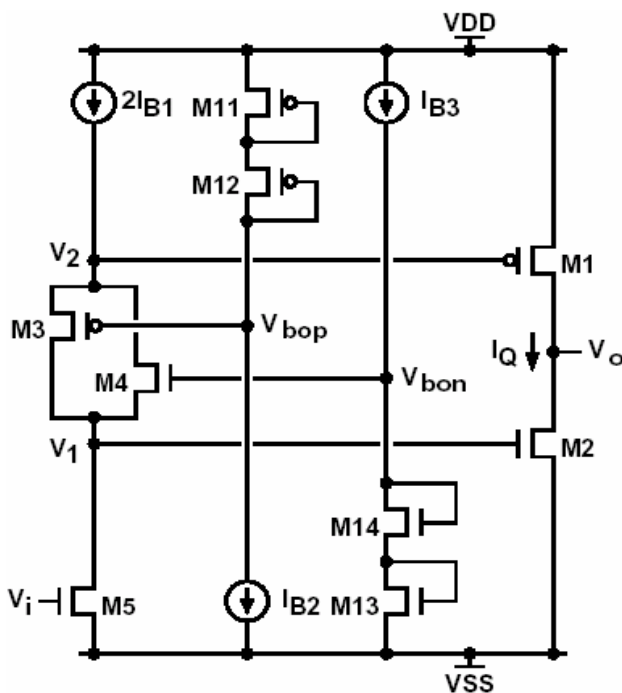


**Figure 1.2** Common Source configuration of Class-AB output stage.
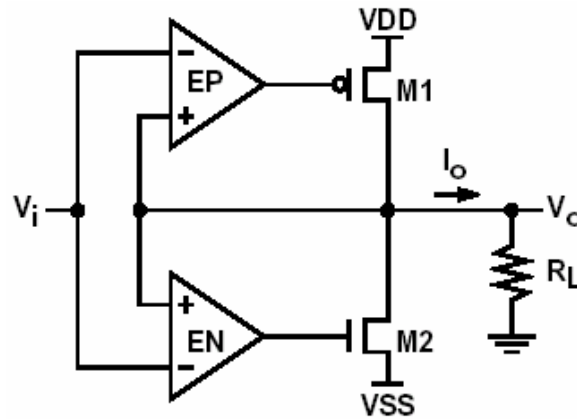
**Figure 1.3** Common Source configuration of Class-AB output stage with error amplifier.

## (3)    Common-Source configuration with Error Amplifier

Another solution is the use of quasi-complementary configurations [1]. Fig.1.3 shows two comm.-source transistors together with two differential error amplifiers. The combination of the error amplifier and the common-source device simulates the behavior of a source follower with high dc transconductance. The function of the amplifier is to sense the voltage difference between the input and output of the stage and to drive the gates of the output transistors so as to minimize the voltage difference. This operation can also be viewed as a negative shunt feedback. A key advantage of the use of a negative feedback here is that it reduces the output resistance.
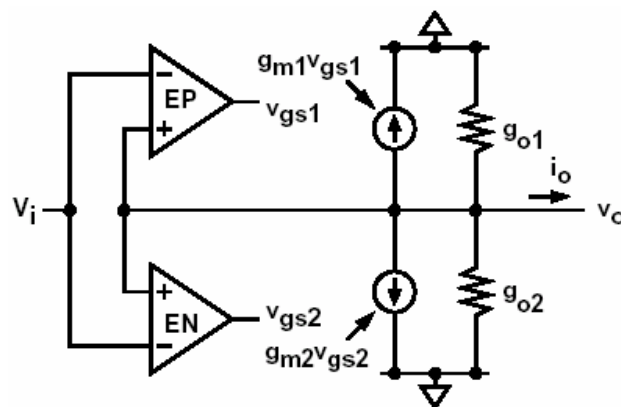


**Figure 1.4** Small-signal model of the output stage in Fig.1.3

To find the output resistance, consider the small-signal model of this output stage shown in Fig 1.4. The transconductance $G_O$ and output impedance are

$$G_O = -\left.\frac{i_O}{V_O}\right|_{Vi=0} = g_{m1}A_{EP} + g_{m2}A_{EN} + g_{O1} + g_{O2} \tag{1.6}$$

$$R_O = \frac{1}{g_{m1}A_{EP} + g_{m2}A_{EN}} // r_{O1} // r_{O2} \tag{1.7}$$

This equation shows that increasing the gain A of the error amplifier reduces $R_O$ and that $R_O$ is much smaller than the drain-source resistance of M$_1$ and M$_2$ because of the negative feedback.

Fig 1.5 shows the dc model which includes the input-referred offset voltages of the error amplifiers. Assume $-V_{tn} = V_{tp} = V_t$ and $k_p'(W/L)_1 = k_n'(W/L)_2 = k'(W/L)$. Also assume that the error amplifier are designed so that $I_Q = -I_{D1} = I_{D2}$ when $V_{OSP} = V_{OSN} = 0$ and

$V_i = 0$. Under these conditions, $V_O = 0$, $V_{OV} = \sqrt{\dfrac{2I_Q}{k'(W/L)}}$ and $V_{gs1} = -V_t - V_{OV}$,

$V_{gs2} = V_t + V_{OV}$. With nonzero input and offsets, the output may not be zero. As a result, the differential input to the error amplifier EP changes from zero to $V_O - (V_i - V_{OSP})$. Similarly, the differential input to the error amplifier EN changes from zero to $V_O - (V_i - V_{OSN})$.
Assume that the output of each error amplifier changes by its gain A times the change in its input,
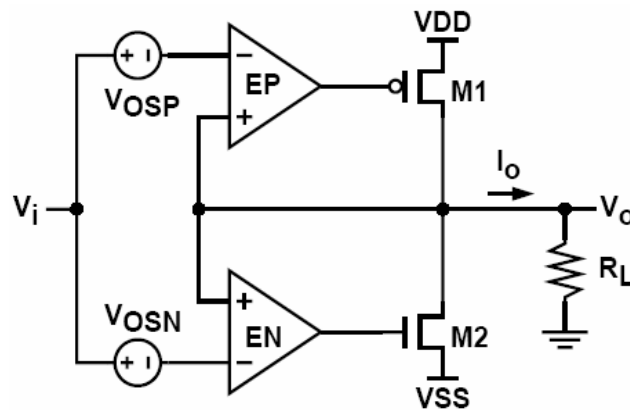


**Figure 1.5** A dc model of the output stage in Fig.2.10.

$$V_{gs1} = -V_t - V_{OV} + A[V_O - (V_i - V_{OSP})] \tag{1.8}$$

$$V_{gs2} = V_t + V_{OV} + A[V_O - (V_i - V_{OSN})] \tag{1.9}$$

$$I_{d1} = -\frac{k'_p}{2}\left(\frac{W}{L}\right)_1 (V_{gs1} - V_{tp})^2 = -\frac{k'}{2}\frac{W}{L}(V_{gs1} + V_t)^2 \tag{1.10}$$

$$I_{d2} = \frac{k'_n}{2}\left(\frac{W}{L}\right)_2 (V_{gs2} - V_{tn})^2 = \frac{k'}{2}\frac{W}{L}(V_{gs2} + V_t)^2 \tag{1.11}$$

Also, $I_O = \dfrac{V_O}{R_L}$. From KCL at the output, $I_{d1} + I_{d2} + I_O = 0$, and we can get

$$V_O = \frac{V_i - \dfrac{V_{OSP} + V_{OSN}}{2}}{1 + \dfrac{1}{k'\dfrac{W}{L}A[2V_{OV} - A(V_{OSP} - V_{OSN})]R_L}} \tag{1.12}$$

If $V_{OSP} = V_{OSN} = 0$,

$$V_O = \frac{V_i}{1 + \dfrac{1}{k'\dfrac{W}{L}A2V_{OV}R_L}} = \frac{V_i}{1 + \dfrac{1}{2Ag_m R_L}} \cong V_i\left(1 - \frac{1}{2Ag_m R_L}\right) \tag{1.13}$$

If $A(V_{OSP} - V_{OSN}) \ll 2V_{OV}$ and $2Ag_m R_L \gg 1$,

$$V_O = \frac{V_i - \dfrac{V_{OSP} + V_{OSN}}{2}}{1 + \dfrac{1}{k'\dfrac{W}{L}A2V_{OV}R_L}} = \frac{V_i - \dfrac{V_{OSP} + V_{OSN}}{2}}{1 + \dfrac{1}{2Ag_m R_L}} \cong V_i - \frac{V_{OSP} + V_{OSN}}{2} \tag{1.14}$$

Therefore, the input offset voltage of the buffer is approximately $-(V_{OSP} + V_{OSN})/2$

Although quasi-complementary circuits reduce its output impedance and improve the output swing, they suffer from two problems. First, these circuits present difficult design problems in frequency compensation. Second, if an offset occurs between error amplifier EP and EN, the current balance between the output drivers $M_1$ and $M_2$ no longer exists and the current flow through these devices is therefore uncontrolled. From a design standpoint, the

quiescent current is chosen to be barely high enough to limit crossover distortion to an acceptable level. Although further increases in the quiescent current reduce the crossover distortion, they also worsen the problem of power dissipation. Therefore, a well-defines quiescent current with nonzero offset is a key design constraint.

One way to control the quiescent current is to sense and feedback a copy of the current [3]. Fig. 1.6 shows the simplified schematic of the circuit [4]. The feedback circuit of the two error amplifiers tries to insure that the voltages in the loop sum to be zero. $M_9$-$M_{12}$ altogether contribute to current sensing. When $V_{OS}$ is positive, $M_6$ tries to turn off and so does $M_{6A}$. $I_{M9}$ reduces thus reducing $I_{M12}$. A reduction in $IM12$ reduces $I_{M8A,}$ thus decreases $V_{GS8A}$. Ideally $V_{GS8A}$ decreases by an amount equal to $V_{OS}$. A similar result holds for negative offsets and offsets in the error amplifier A2. With careful design, this circuit could control the quiescent current by correcting offset voltage in the error amplifier. However, the minimum output voltage will be limited by diode connecting of $M_8$, and

$$V_{OUT(min)} = V_{SS} + V_{OV17} + V_{GS8}$$ (1.15)
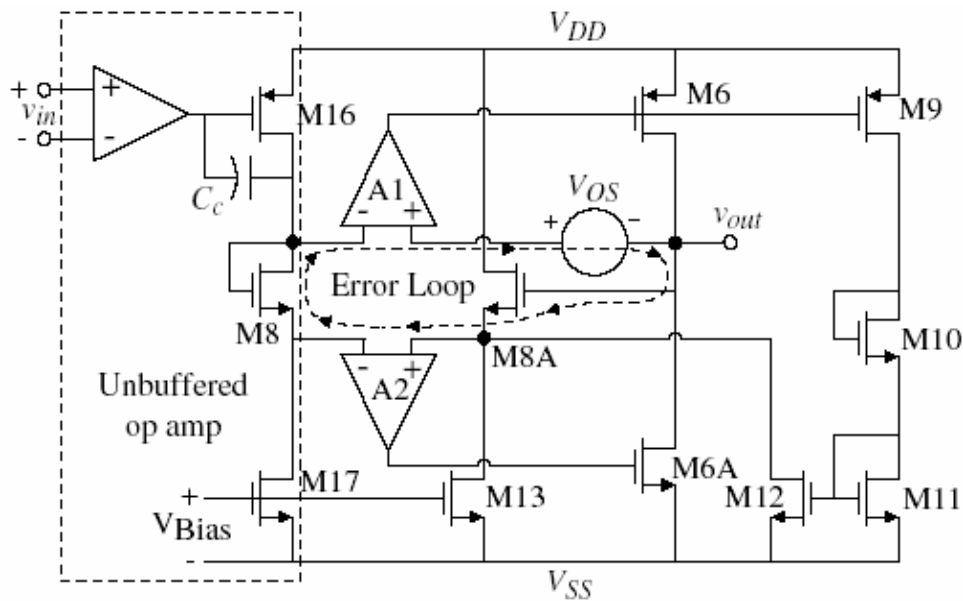


**Figure 1.6** Class AB output stage with offset correction circuit [4].

Another way to limit the quiescent current variations is to design the error amplifier to have low gain [5] [6]. The quiescent current is controlled by the gate-source voltages on the power transistors, which in turn are controlled by the outputs of the error amplifiers. Therefore, reducing the error-amplifier gain reduces the gate-source voltage variations and the quiescent current for a given variation in the offset voltage.

To study this situation quantitatively [7], define the quiescent current in the output devices as the common-mode component of the current flowing from $V_{DD}$ to $-V_{SS}$ with $V_i=0$,

Then $I_Q = \dfrac{I_{D2} - I_{D1}}{2}$. Substituting (1.8)-(1.11) into above equation gives

$$I_Q = \frac{k'}{4}\frac{W}{L}\left((V_{ov} + A[V_o + V_{OSN}])^2 + (-V_{ov} + A[V_o + V_{OSP}]^2\right) \tag{1.16}$$

Since $V_O = 0$ if $V_{OSP} = V_{OSN} = 0$, (1.16) shows that

$$I_Q\Big|_{\substack{VOSP=0 \\ VOSN=0}} = \frac{k'}{4}\frac{W}{L}\left((V_{ov})^2 + (-V_{ov})^2\right) = \frac{k'}{2}\frac{W}{L}(V_{ov})^2 \tag{1.17}$$

From, (1.14) with $V_i=0$,

$$V_o + V_{OSP} \cong \frac{V_{OSP} - V_{OSN}}{2} \tag{1.18}$$

$$V_o + V_{OSN} \cong -\frac{V_{OSP} - V_{OSN}}{2} \tag{1.19}$$

Substituting (1.18) and (1.19) into (1.16) gives

$$I_Q = \frac{k'}{2}\frac{W}{L}\left(V_{ov} - A\left[\frac{V_{OSP} - V_{OSN}}{2}\right]\right)^2 \tag{1.20}$$

Define $\Delta I_Q$ as the change in $I_Q$ caused by nonzero offsets; that is,

$$\Delta I_Q = I_Q\Big|_{\substack{VOSP=0 \\ VOSN=0}} - I_Q \tag{1.21}$$

Substituting (1.20) and (1.17) into (1.21) gives

$$\Delta I_Q = \frac{k'}{2}\frac{W}{L}A(V_{OSP} - V_{OSN})\left[V_{ov} - A\left(\frac{V_{OSP} - V_{OSN}}{4}\right)\right] \tag{1.22}$$

To evaluate the magnitude of $\Delta I_Q$, we will compare it to the quiescent current with zero

offsets by dividing (1.22) by (1.17). The result is

$$\frac{\Delta I_Q}{I_Q\big|_{\substack{VOSP=0\\VOSN=0}}} = A\left(\frac{V_{OSP}-V_{OSN}}{V_{OV}}\right)\left[1-A\left(\frac{V_{OSP}-V_{OSN}}{4V_{OV}}\right)\right] \qquad (1.23)$$

If $A(V_{OSP}-V_{OSN}) << 4V_{OV}$,

$$\frac{\Delta I_Q}{I_Q\big|_{\substack{VOSP=0\\VOSN=0}}} \cong A\left(\frac{V_{OSP}-V_{OSN}}{V_{OV}}\right) \qquad (1.24)$$

Therefore, to keep the fractional change in the quiescent current less than a given amount, the maximum error-amplifier gain is

$$A < \left(\frac{V_{OV}}{V_{OSP}-V_{OSN}}\right)\left(\frac{\Delta I_Q}{I_Q\big|_{\substack{VOSP=0\\VOSN=0}}}\right) \qquad (1.25)$$

For example, if $V_{OV}$ =200mV, $V_{OSP}-V_{OSN} \approx$ 5mV, and up to 20 percent variation in quiescent current is allowed, (1.25) shows that the error amplifier gain should be less than about 8 [5] [6].
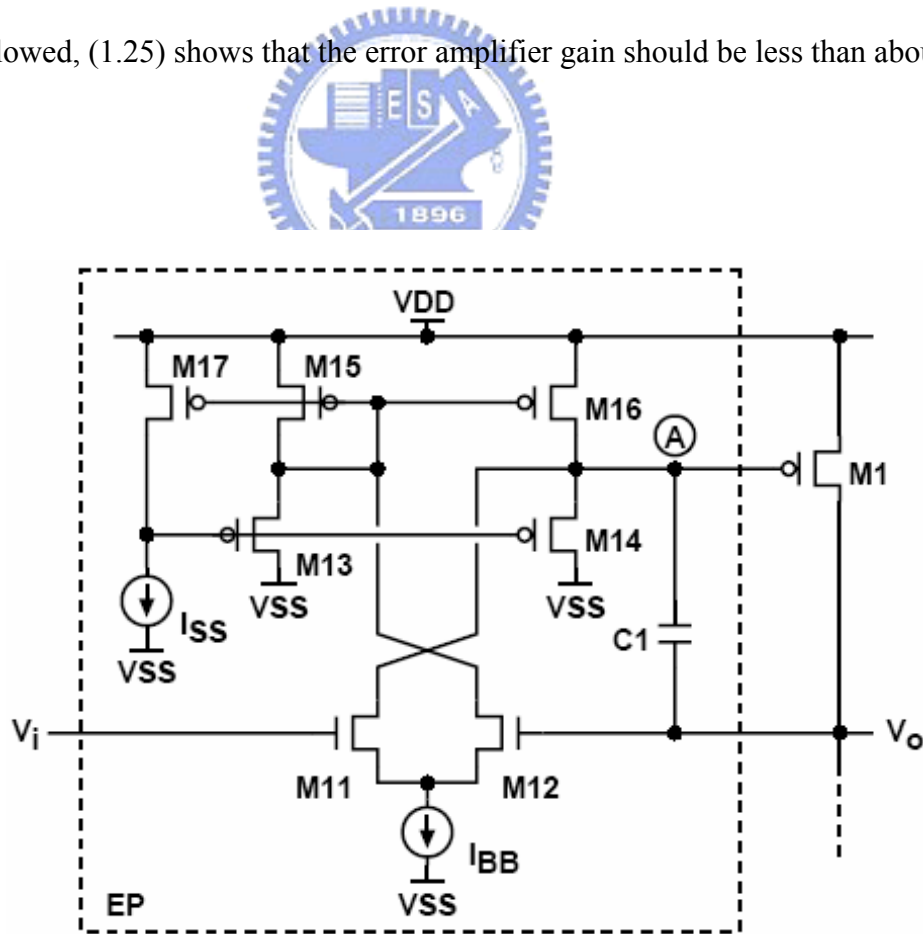


**Figure 1.7** Schematic of the error amplifier EP and power transistor $M_1$ in Fig.1.5

Fig.1.7 shows the schematic of the error amplifier EP and $M_1$ from Fig. 1.5 [6]. A complementary structure used to drive $M_2$ is not shown. The difference between $V_i$ and $V_o$ is sensed by the differential pair $M_{11}$ and $M_{12}$, which is biased by the tail current source $I_{BB}$. The load of the differential pair consists of two parts: source-follower transistors $M_{13}$ and $M_{14}$ and current mirror $M_{15}$ and $M_{16}$. It can be considered a general one-stage CMOS amplifier consisted of transistors $M_{11}$, $M_{12}$, $M_{15}$ and $M_{16}$, and the purpose of the source-follower transistors is to reduce the output impedance of the error amplifier EP to set its gain to a well-defined low value. The gates of the source-follower transistors are biased by a negative feedback loop including $M_{15}$, $M_{17}$, $I_{SS}$, and $M_{13}$. This circuit adjusts the voltage at the gate of $M_{13}$ so that $M_{17}$ operates in the active region and conducts $I_{SS}$.

Since $M_{15}$ and $M_{17}$ form a current mirror, and so do $M_{15}$ and $M_{16}$ with $(W/L)_{15}=(W/L)_{16}$

$$\left|I_{D15}\right| = \left|I_{D16}\right| = \left|I_{D17}\right| \frac{(W/L)_{15}}{(W/L)_{17}} = \left|I_{SS}\right| \frac{(W/L)_{15}}{(W/L)_{17}} \tag{1.26}$$

With $V_i = V_O$, $I_{D11} = I_{D12} = I_{BB}/2$. From KCL,

$$\left|I_{D14}\right| = \left|I_{D16}\right| - \left|I_{D11}\right| = \left|I_{SS}\right| \frac{(W/L)_{15}}{(W/L)_{17}} - \frac{\left|I_{BB}\right|}{2} \tag{1.27}$$

Since $I_{D13} = I_{D14}$ when $I_{D11} = I_{D12}$, $V_{SD16} = V_{SD15} = V_{SG15} = V_{SG1}$

Therefore, ignoring channel-length modulation,

$$\left|I_{D1}\right| = \left|I_{D15}\right| \frac{(W/L)_1}{(W/L)_{15}} = \left|I_{SS}\right| \frac{(W/L)_1}{(W/L)_{17}} \tag{1.28}$$

This equation shows that the drain current in $M_1$ is controlled by $I_{SS}$ and a ratio of transistor sizes if the offset voltage of the error amplifier EP is zero so that $V_O = 0$ when $V_i = 0$. In practice, $(W/L)_1 >> (W/L)_{17}$ so that little power is dissipated in the bias circuits.

Another design consideration therefore comes out from these equations. To keep the gain of the error amplifier low under all conditions, $M_{14}$ must never cut off. Therefore, from (1.27), $\left|I_{D16}\right|$ should be greater than the maximum value of $I_{D11}$. Since the maximum value of $I_{D11}$ is $I_{BB}$, gives

$$\left| I_{D16} \right| = \left| I_{SS} \right| \frac{(W/L)_{15}}{(W/L)_{17}} > I_{BB} \tag{1.29}$$

Consider the entire small signal current from the differential pair flows at the error-amplifier output and the transconfuctance is $G_m = g_{m11} = g_{m12}$, The output resistance of the error amplifier is dominated by source-follower transistor $M_{14}$. $R_O = \dfrac{1}{g_{m14} + g_{mb14}}$

Therefore, the gain of the error amplifier EP is

$$A = G_m R_O = \frac{g_{m11}}{g_{m14} + g_{mb14}} \tag{1.30}$$

A drawback of this error amplifier is that the output swing is limited. Review Fig. 1.7. We want a large swing at node A, the gate of $M_1$, to provide a strong gate drive for $M_1$. However, the maximum voltage of node A is limited by

$$(V_i - V_{GS11} + V_{OV11}) \tag{1.31}$$

Form (1.31), the maximum source-gate voltage of $M_1$ is

$$V_{DD} - (V_i - V_{GS11} + V_{OV11}) \tag{1.32}$$

With good linearity desired, $V_O$ should precisely follow $V_i$. When driving a low impedance load, output current increases as both $V_i$ and $V_O$ rise. (1.32) shows that the higher $V_i$ the smaller capable source-gate voltage of $M_1$, which means we need a larger-sized $M_1$ to achieve the desired output current.

Compared with Fig.1.7, Fig.1.8 shows an alternative error amplifier [7], which has a better output swing. A complementary structure used to drive $M_1$ is not shown. In the balanced quiescent condition, the drain currents of transistors $M_{15}$ and $M_{16}$ are equal to half the bias current $I_{BB}$. Because the sizes of transistors $M_{10}$ and $M_{11}$ are the same as those of transistors $M_{12}$ and $M_{13}$, respectively, and the drain currents of these four transistors are the same, the drain voltage of transistor M13 is the same as the gate voltage if the channel length modulation is ignored. Thus the drain current of the output transistor $M_2$, the quiescent current, is given by $I_{D2} = I_{D13} \dfrac{(W/L)_2}{(W/L)_{13}}$

$$\tag{1.33}$$
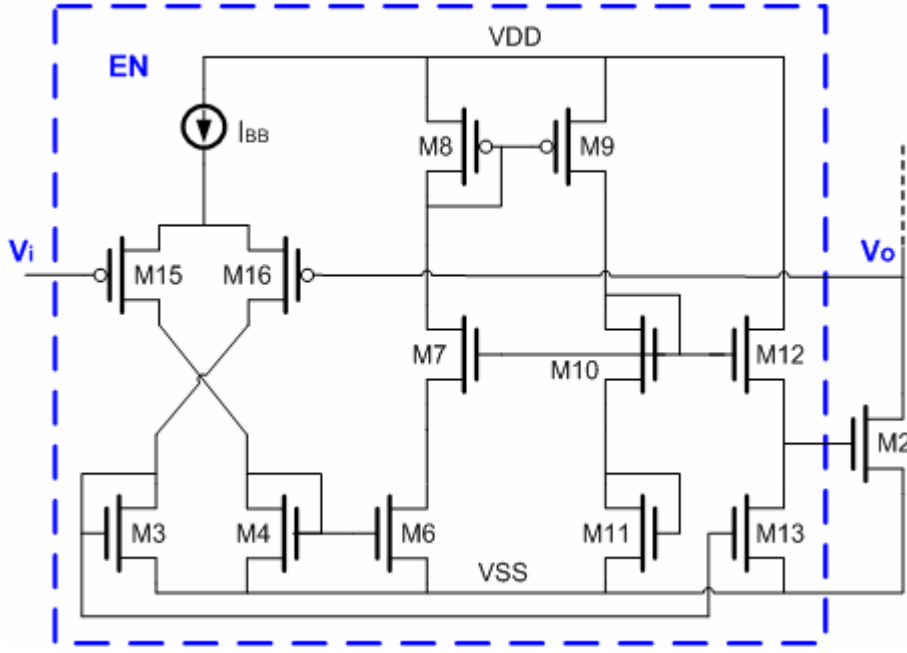
**Figure 1.8** An alternative error amplifier in Fig. 1.5

The drain current $I_{D13}$ of M13 is $I_{D13} = I_{D3} \dfrac{(W/L)_{13}}{(W/L)_3}$ (1.34)

Since the drain current of M$_3$ is equal to half of the bias current I$_{BB}$, we can drive the output

current by combining (1.33) and (1.34), which is given by

$$I_{D2} = \frac{1}{2}\frac{(W/L)_2}{(W/L)_3} I_{BB}$$ (1.35)

(1.35) shows that the quiescent current of M$_2$ is linearly related to the bias current I$_{BB}$ and the

W/L ratio of the two transistors M$_3$ and M$_2$. If we want to decrease the quiescent current

without sacrificing the current drive capability, we can make M13 larger. If we increase the

size of M13 by a factor of K, the gate over-drive of M$_2$, $V_{GS2} - V_{t2}$, is given by

$$
\begin{aligned}
V_{GS2} - V_{t2} &= V_{GS10} + V_{GS11} - V_{GS12} - V_{t2} \\
&= \sqrt{\frac{2(W_{11}/W_3)(I_{BB}/2)}{\mu C_{OX}(W_{10}/L_{10})}}(1-\sqrt{K}) + \sqrt{\frac{2(W_{11}/W_3)(I_{BB}/2)}{\mu C_{OX}(W_{11}/L_{11})}} + (V_{t10} - V_{t12})
\end{aligned}
$$ (1.36)

assuming W$_{12}$ = W$_{10}$, W$_4$ = W$_3$, W$_6$ = W$_{11}$, and L$_{12}$ =L$_{10}$. (1.36) shows that increasing the ratio

of K minimizes the overdrive voltage, and therefore decreases the quiescent current. However,

increasing the ratio of K will deteriorate the linearity. It needs to be traded off carefully.

There is another disadvantage worth noticing here in this circuit. Consider channel length modulation effect, that $V_{DS8} \neq V_{DS9}$, and $V_{GS10} = V_{DS10} \neq V_{DS12}$ will result in the difference of current, say, $I_{M9} \neq I_{M8}$ and $I_{M9} \neq I_{M12}$. The difference increases with the supply voltage, which again causes an unwanted offset in quiescent current.

## (4) Combined Common-Drain Common-Source Configuration

The gain of error amplifiers, as discussed in the previous section, is limited to establish adequate control on the output current. Its bandwidth is usually limited, too, to avoid stability problems. These two limitations make a common-source configuration suffer from an increase in harmonic distortion, especially at high frequencies.

An alternative to overcome this problem is to use a combination of the common-drain and common-source configurations as shown in Fig.1.9 [8] [9]. The key aspect of this circuit is that it uses two buffers connected to the output: The transistors $M_{11}$-$M_{-12}$ and error amplifiers EP, EN with offset voltage $V_{OS}$ can be considered a Class-B quasi-complementary buffer. It works only when the output swing is large, but turns off with a zero or small output. Another Class-AB common-drain buffer is consisted of $M_1$-$M_4$, which controls the quiescent output current and improves the frequency response as we shall discuss later. $V_{OS}$ can be introduced by intentionally mismatching the input differential pair in each error amplifier. The circuit can be designed so that, when $V_O = V_1 = 0$, the introduction of $V_{OS}$ turns off M11 and M12. Error amplifiers, EP and EN, both can have a high gain, which decreases the harmonic distortion, and they are often designed as onstage amplifiers with the gain $\approx g_m r_O$.

The output swing is dominated by a common-drain buffer. Consider the $V_1$ voltage range which is limited by the diode connected $M_3$ and $M_4$. Then,

$$V_O(\max) \approx V_1(\max) = V_{DD} - |V_{OV5}| - V_{gs3} \qquad (1.37)$$

By adding one extra branch as show in Fig.1.10, this limitation can be overcome. The new branch consisted of transistors $M_7$ and $M_8$ operates in parallel with the branch containing $M_3$ to $M_6$ to produce $V_1$. The swing of V1 in Fig.1.9 is limited by the threshold voltages of M3 and M4 as discussed earlier. In contrast, the new branch in Fig.1.10 can drive $V_1$ within an overdrive of either supply while $M_7$ and $M_8$ operate in the active region. Improving the swing of $V_1$ also improves the output swing.

Consider the frequency response of the circuit shown in Fig.1.7 qualitatively. The circuit has two paths from $V_1$ to output. The path through the common-source transistors $M_{11}$ and $M_{12}$ may be slow because of the need to limit the bandwidth of the error amplifiers to guarantee stability of the circuit. On the other hand, the path through the common-drain transistors $M_1$ and $M_2$ is fast because source followers are high-bandwidth circuits. Since currents from the two output buffers are added up, the fast path will dominate for high-frequency signals and it simplifies the design required to guarantee stability.

There is also a notable drawback of this circuit, that is, to use large-sized transistors to achieve a desired output swing. In addition to the huge-sized power transistors $M_{11}$ and $M_{12}$, $M_1$-$M_4$ have to be relatively large enough to get an appropriate threshold voltage under their bias condition. The size of $M_2$ and $M_4$ is about half of $M_{11}$ and so are the n-channel transistors, $M_1$, $M_3$ and $M_{12}$. [9]

**Figure 1.9** Combined common-drain, common source output stage.
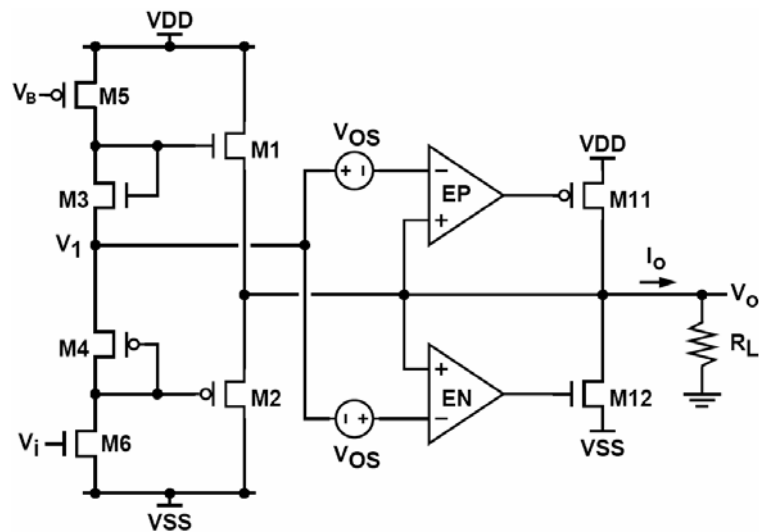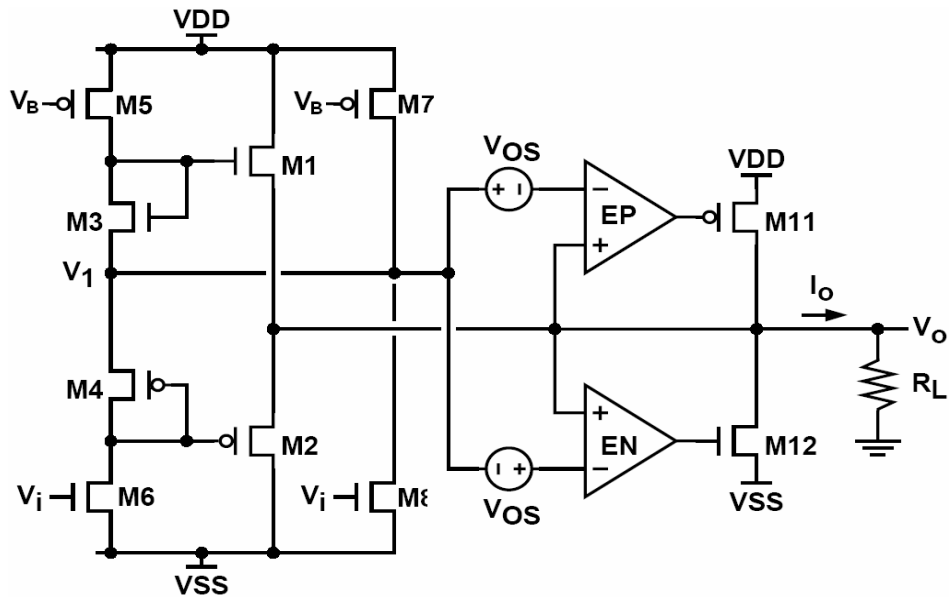
**Figure 1.10** Combined common-drain, common source output stage with high swing.

## (5)    Parallel Common-Source Configuration

Fig.1.11 shows another circuit with similarities discussed in previous section [10]. This circuit combines two buffers in parallel at the output. The error amplifiers $EP_1$ and $EN_1$ with $M_1$ and $M_2$ form the first buffer, which controls the operation of the output stage with Vi=0. The error amplifiers $EP_2$ and $EN_2$ with $M_{11}$ and $M_{12}$ form the second buffer, which dominates the operation of the output stage for large-magnitude output voltages.
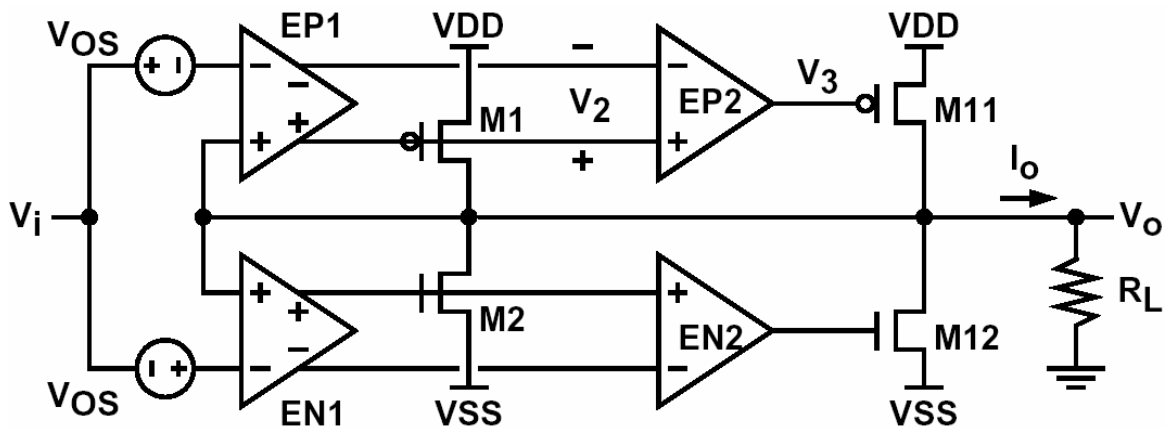


**Figure 1.11** Parallel common-source configuration of output stage

This behavior stems from small offset voltages intentionally built into the amplifiers $EP_1$ and $EN_1$. With $EP_2$ and $EN_2$ properly adjusted to have high gain, and $EP_1$ and $EN_1$ to have low gain, these offsets have little effect on the drain currents of $M_1$ and $M_2$. Therefore, $M_1$ and $M_2$ operate in the active region when Vi=0, and the first buffer operates in Class-AB mode. On the other hand, the product $V_{OS}A_{EP1}A_{EP2}$ and $V_{OS}A_{EN1}A_{EN2}$ are conditioned by design to be big enough to force $V_{gs11}>V_{t11}$ and $V_{gs12} < V_{t12}$ so that M11 and M12 are off when $V_i$=0. The second buffer operates in Class-B mode to avoid higher quiescent current introduced by power transistors $M_{11}$ and $M_{12}$.

In general, more amplifiers contribute to more poles and zeros in the frequency domain. This should be taken into serious consideration to avoid stability problems when designing each amplifier in Fig.1.11. Fig.1.12 and Fig.1.13 show the schematics of $EP_1$ and $EP_2$, respectively. Further detail frequency response analysis shall be left aside here.

Now consider the effect of the offset voltage, $V_{OS}$, which is introduced by making $(W/L)_3 \cong 0.8(W/L)_4$ [10]. Assume that $V_O = 0$ when $V_i = 0$. Increasing $V_{OS}$ reduces

$$I_{D3} \text{ because of } I_{D3} = I_{B1}\frac{(W/L)_3}{(W/L)_3 + (W/L)_4}. \tag{1.38}$$

$$\text{Since, } I_{D3} = |I_{D5}| + I_{B2}, \text{ and } I_{D1} = (I_{D3} - I_{B2})\frac{(W/L)_1}{(W/L)_5} \tag{1.39}$$
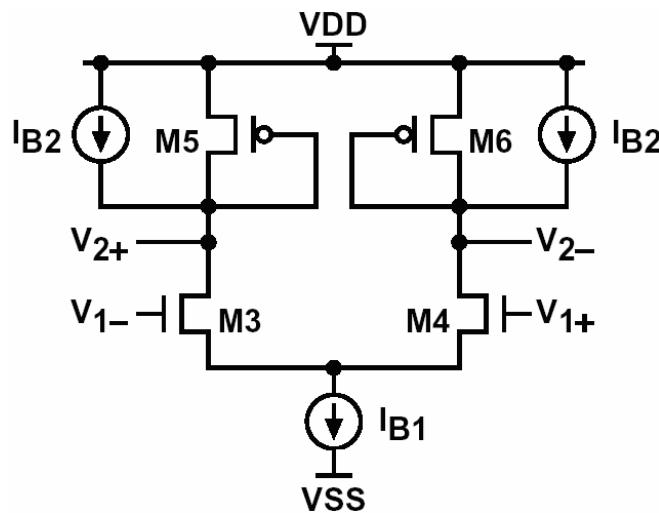


**Figure 1.12** The error amplifier $EP_1$ shown in Fig.1.11
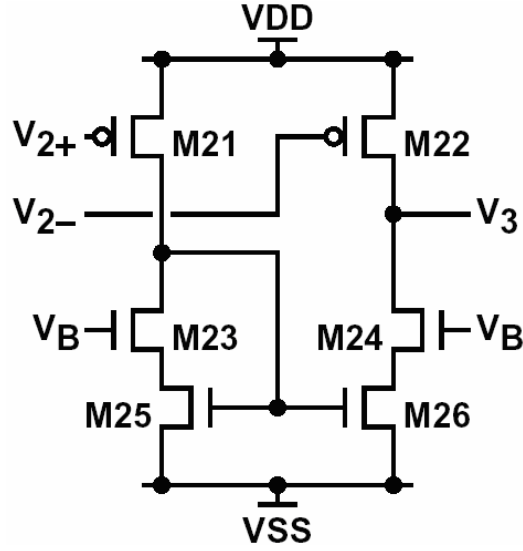
**Figure 1.13** The error amplifier EP$_2$ shown in Fig.1.11

$I_{D3}$ must be greater than $I_{B2}$ to prevent M$_5$ from cutoff and avoid losing control over the quiescent current. Therefore, the offset must be chosen small enough so that $|I_{D5}| > 0$. In practice, however, there are some mismatches of the error amplifiers caused by unexpected random effects. Since we intend to bias M$_{11}$ in cutoff region, the random components must not be larger than the systematic offset in magnitude and opposite in polarity. Therefore, V$_{OS}$ is chosen to be bigger than the expected random offsets.

Consider the transfer characteristic of this circuit. When |Vi | is small, and M$_{11}$ and M$_{12}$ are not turned on, the output is

$$V_O = \frac{V_i}{1 + 1/(A_{EP1} g_{m1} R_L/2 + A_{EN1} g_{m2} R_L/2)} \tag{1.40}$$

When $V_i$ is large, M$_{11}$ can be turned on, and the output becomes

$$V_O \approx V_i - V_{OS} \tag{1.41}$$

if A$_{EP2} \rightarrow \infty$.

To determine the range of input voltages for which M$_{11}$ and M$_{12}$ are both off, assume that the gains $A_{EP1}$ and $A_{EP2}$ are constant.,

$$V_3 = [V_O - (V_i - V_{OS})]A_{EP1}A_{EP2} + V_K \tag{1.42}$$

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where $K$ is a constant. When $V_{2+} = V_{2-}$ at $EP_2$, gives

$$V_3 = V_K = V_{gs25} = V_{OV25} + V_{t25} + V_{SS} \tag{1.43}$$

Then, define $V_{i(min)}$ as the minimum input to turn on $M_{11}$. Let $V_3 = V_{DD} - |V_{tp11}|$, substituting (1.42) with (1.43) into (1.40) gives

$$Vi(min) = V_{OS}(1 + A_{EP1}g_{m1}R_L) - \frac{(V_{DD} - V_K - |V_{tp11}|)(1 + A_{EP1}g_{m1}R_L)}{A_{EP1}A_{EP2}} \tag{1.44}$$

If $A_{EP2} \to \infty$, gives

$$Vi(min) = V_{OS}(1 + A_{EP1}g_{m1}R_L) \tag{1.45}$$

The derivative analysis shows that $M_{11}$ and $M_{12}$ remain off for only a small range of input voltages. Therefore, the nonlinearity introduced by turning on $M_{11}$ or $M_{12}$ occurs when $|V_i|$ is small. As a result, this circuit is suitable for ISDN (Integrated Service Digital Network) line-driving application for which it was designed because the required four-level output code does not include zero, avoiding distortion that would be introduced by turning $M_{11}$ and $M_{12}$ on or off [10] if a zero-level output pulse were required.

Similar to Fig.1.10, this parallel common-source configuration with two sets of buffers will need a larger chip area. When an output stage is designed with a large current drive and a smaller impedance of the output load, bigger-sized output power transistors will be needed. When applying this kind of circuit to an audio amplifier, it should be seriously considered that transistors $M_1$ and $M_2$ will take up a large chip area as another set of power transistors, $M_{11}$ and $M_{12}$.

The drawbacks of different output stages introduced in Sec. 1.1.1. are summarized in Table 1-2. Among these different output stages, Common-Drain and Common Source configurations in particular are apparently not suitable to be used in audio amplifiers. Counterparts such as Combined Common-Drain Common-Source and Parallel Common Source configurations are uneconomical in size for consuming larger chip area. On the other

hand, while Common-Source with error amplifier configuration may seem relatively economical of size, the error amplifier in this design has to deal with the problem of quiescent current at the expense of linearity and output power performance.

| Drawbacks of different Class-AB output stages | | |
|---|---|---|
| **Configuration** | **Ref.** | **Drawbacks** |
| Common-Drain | - | Small output swing |
| Common-source | - | High output impedance<br>High signal distortion |
| Common-source with error amplifier | [3] | Output swing limited by offset cancellation circuit |
| | [6] | Poor linearity due to error amplifier's low gain<br>The use of larger-sized power MOS due to a limited output swing of the error amplifier |
| | [7] | Small supply voltage range |
| Combined Common-Drain Common-Source | [8]<br>[9] | Uneconomical in size due to the use of two sets of power MOS |
| Parallel Common-Source | [10] | Uneconomical in size due to the use of two sets of power MOS |

**Table 1-2** Design Specifications of this work

## 1.2    Motivations

In view of the aforementioned disadvantages, we decide to put forth a better output stage structure by improving the Common-Source with error amplifier configuration.    Compared with its counterparts in Table 1-2, the structure of Common-Source with error amplifier output stage is simpler and consequently is economical of chip size. The objective of this thesis is to design a new kind of error amplifier that ameliorates all the drawbacks listed in Table 1-2, which is economical of size, has high output power and high linearity, and works under a wider range of supply voltage.

## 1.3    Main result

The chip of our design is fabricated by the UMC 0.5um +/-20V2P2M high voltage process. It can works under 10V to 18V of supply voltage. With a supply voltage of 15V and an output resistor load of 8Ω, output power will be 2W with 0.062% THD. The quiescent current of this chip is 20mA typically. The chip dimension is 2210um x 3497um with an additional test key.

## 1.4    Thesis organization

This thesis aims to improve the design of linear audio amplifier output stage. In Chapter 2, we will further discuss in detail the structure of Class-AB output stage proposed by this thesis. Also, we will show how the functions of mute, standby, and volume control are realized in actual circuit design. Finally, in the last part of Chapter 2, we will provide the results of pre-simulation. In chapter 3, the complete layout and results of post-simulation will be shown. Chapter 4 mainly concludes the distinguishing features and contributions of this thesis, and it also provides possible work and improvements from a future perspective.

# CHAPTER 2

# Architecture and circuit design

## 2.1　Design specification and consideration

Class-AB single-ended audio amplifier with high supply voltage and high output power is not that popular a research target in the academic arena, so we turn to search for some product specifications of several well-established semiconductor corporations for reference. These include companies such as *STMicroelectronics, TEXAS INSTRUMENTS, National Semiconductor*, and so on. They all have products with similar applications of single ended Class-AB audio amplifiers that work under a wide supply voltage range, 10V~18V. However, limited by our choices of process and packaging, we in the end choose ST-TDA7469L [11] to be the reference of our design spec., and lay down our design targets as in Table 2-1.

(Testing condition Vs = 14V; R$_L$ = 8Ω, Temp=25℃)

| Symbol | Parameter | Test condition | Value | Unit |
|--------|-----------|----------------|-------|------|
| Vs | Supply voltage range | | 10~18 | V |
| Iq | Total quiescent current | | <50 | mA |
| P$_O$ | Output power | THD=1%, R$_L$=8Ω | >1.3 | W |
| THD | Total harmonic distortion | P$_O$=1W, f=1kHz | <0.4 | % |
| BW | Unit gain bandwidth | | >0.6 | MHz |
| Ipeak | Out peak current | | <1.1 | A |
| PSRR | Power supply rejection ratio | F=1kHz | >50 | dB |

**Table 2-1** Design Specifications of this work

## 2.2    Full circuit architecture

Fig.2.1 shows the block diagram of this chip [11]. The stereo audio channel consists of two buffered amplifiers, $OP_{1A}$ and $OP_{1B}$, and two volume control amplifiers, $VC_A$ and $VC_B$. Another open loop buffered amplifier, $OP_{1C}$, is just for testing. The two unit gain buffers, $OP_{2A}$ and $OP_{2B}$, are to be used as earphone output, and their structures are the same as $OP_{1A}$ and $OP_{1B}$, respectively, but differently sizing. Both of the two volume control amplifiers are controlled by a simple analog to digital converter, A_D. The mute control circuit is also contained in A_D. The function block, BIAS, including the standby control function, produces all needed current sources for each circuit.

We define the output reference voltage as $V_{REF} = \dfrac{V_{DD} - V_{SS}}{2}$. The 8 Ohm load resistance will connect the output and $V_{REF}$ through a capacitor outside the chip. $V_{REF}$ is also taken as the common mode voltage in the close loop buffered amplifier. The unit gain amplifier, $OP_{VREF}$, is used to drive the reference voltage, $V_{REF}$.
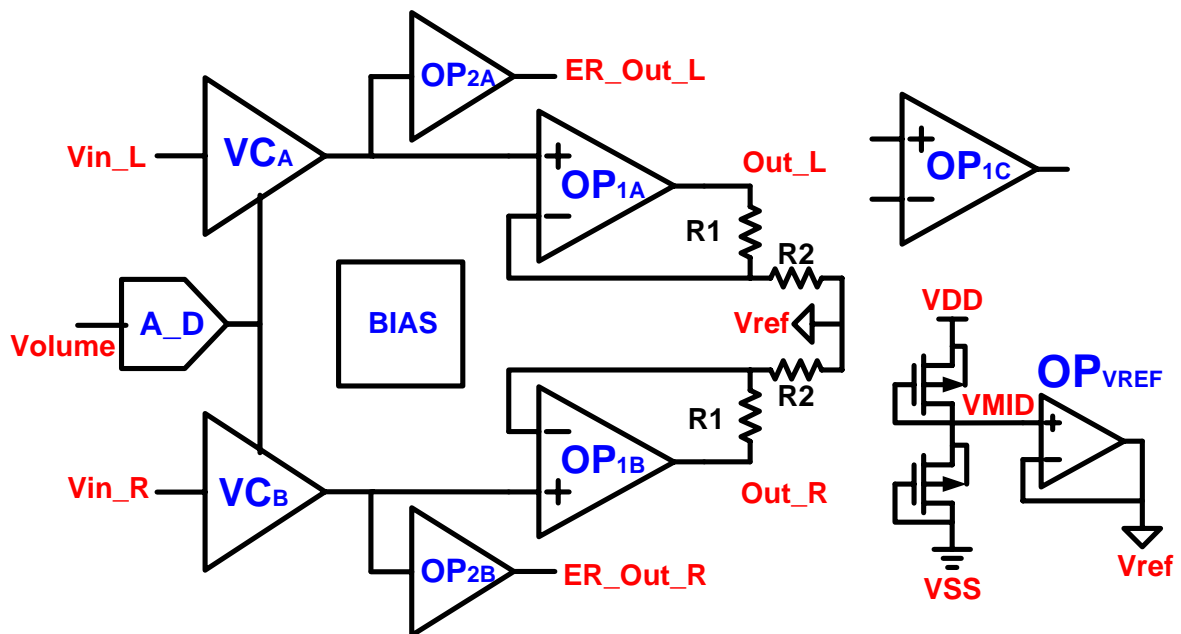


**Figure 2.1** The block diagram of this chip

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## 2.3    Buffered amplifier

Table 2-1 lists the required design targets. The design constraints include a highly supply voltage ranging from 10V to 18V, and an impedance load as low as 8 Ohm. Our design target is to achieve < 0.4% THD, and control the system's quiescent current as low as 50mA. In section 1.1.1, we introduced a lot of architecture and circuits of Class-AB output buffers. Some of them ([6] [8] [9]) may take up too much chip area to be used in high-power output applications, and some [7] may not be suitable for a high supply voltage range (10V~18V) to maintain stable linearity and acceptable quiescent current. Also, two other attractive structures can be referred to as in [12] [13]. However, to meet the high-power output requirement, these simple structures have big problems to compromise between current consumption, linearity and chip area.
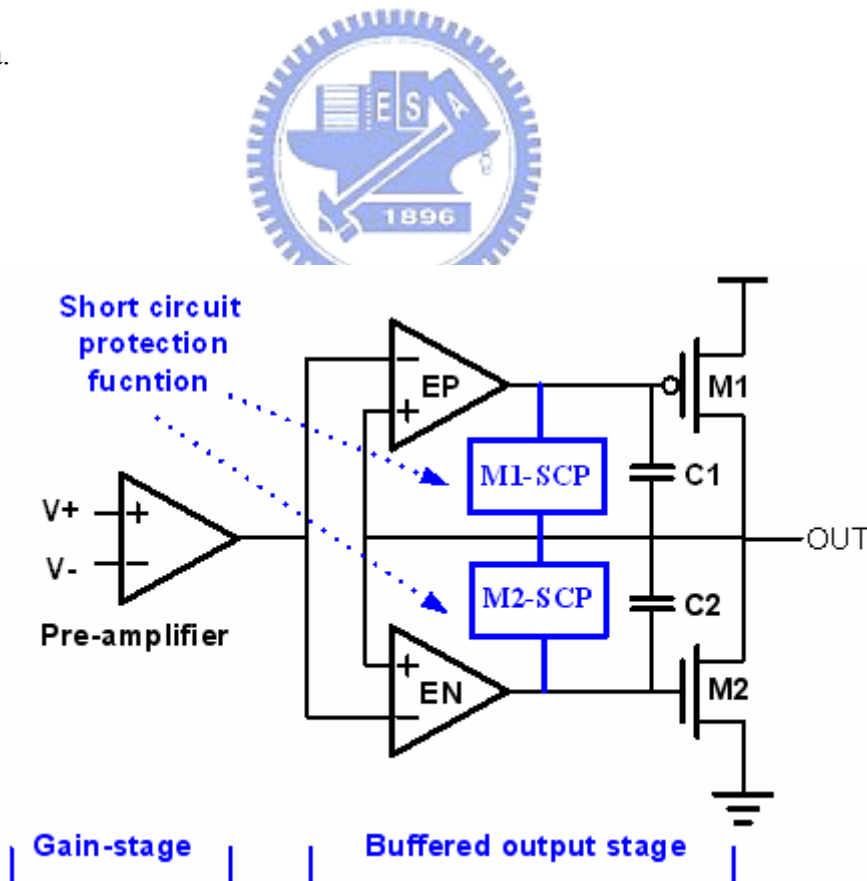


**Figure 2.2** The block diagram of buffered amplifier

### 2.3.1 Architecture of buffered amplifier

We as a result propose a new set of error amplifiers which form the common-source configuration output stage with the function of short circuit protection. Besides, we use a two-stage amplifier as the pre-amplifier to get a high gain in the gain stage. These two parts form a buffered amplifier as show in Fig.2.2.

### 2.3.2 Error amplifier for output buffer

Fig.2.3 shows a schematic of the error amplifier EP and $M_1$ from Fig.2.2. A complementary structure used to drive $M_2$ is shown in Fig.2.4. For convenience, we take EP as the example for the following discussion. The error amplifier EP shown in Fig.2.3 can be recognized as an OTA by ignoring transistors $M_{P10B}$, $M_{P11B}$, $M_{P13}$, and $M_{P14}$. This OTA could provide a high output swing to drive the power transistor $M_1$. The difference between $V_{in2}$ and $V_{EP\_OUT}$ is sensed by the differential pair $M_{P1}$ and $M_{P2}$, which is biased by the tail current source $I_{BP}$ with a current mirror. The load of the differential pair consists of a chain of current mirror branches used to define the quiescent current. Applying similar ideas derived from the circuit shown in Fig.1.7, the source-follower transistors $M_{P13}$ and $M_{P14}$ will reduce the output impedance of the error amplifier EP to set its gain to a well-defined low value. The gates of source-follower transistors are biased by a negative feedback loop including $M_{P11}$, $M_{P11B}$, $M_{P10B}$, and $M_{P13}$. Here the constant current source $I_{SS,}$ as shown in Fig.1.7, is replaced by a variable current mirror source, $M_{P10B}$, which will change its drain current as the input differential pair senses any difference.
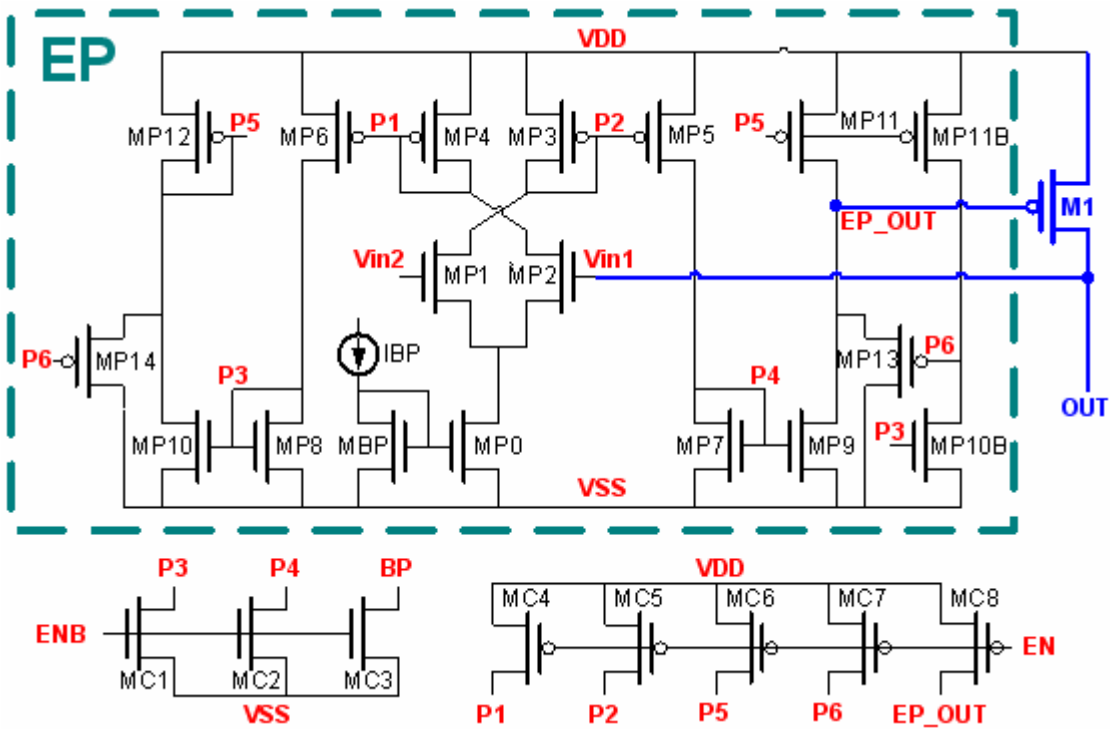
**Figure 2.3** Schematic of the error amplifier EP

| MOS | MBP | MP0 | MP1 | MP2 | MP3 | MP4 | MP5 | MP6 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| W/L(μm) | 10/4 | 10/4 | 45/5 | 45/5 | 10/4 | 10/4 | 10/4 | 10/4 |
| M | 1 | 40 | 20 | 20 | 4 | 4 | 4 | 4 |
| MOS | MP7 | MP8 | MP9 | MP10 | MP11 | MP12 | MP13 | MP14 |
| W/L(μm) | 5/4 | 5/4 | 5/4 | 5/4 | 50/4 | 50/4 | 10/4 | 10/4 |
| M | 2 | 2 | 2 | 2 | 36 | 36 | 4 | 4 |
| MOS | M1 | MP11B | MP10B | MC1 | MC2 | MC3 | MC4 | MC5 |
| W/L(μm) | 106/3 | 50/4 | 5/4 | 10/4 | 10/4 | 10/4 | 10/4 | 10/4 |
| M | 198 | 36 | 4 | 1 | 1 | 1 | 1 | 1 |
| MOS | MC6 | MC7 | MC8 | | | | | |
| W/L(μm) | 5/4 | 5/4 | 10/4 | | IBP=10uA | | | |
| M | 1 | 1 | 1 | | | | | |

**Table 2-2** Transistors W/L ratio of Fig.2.3
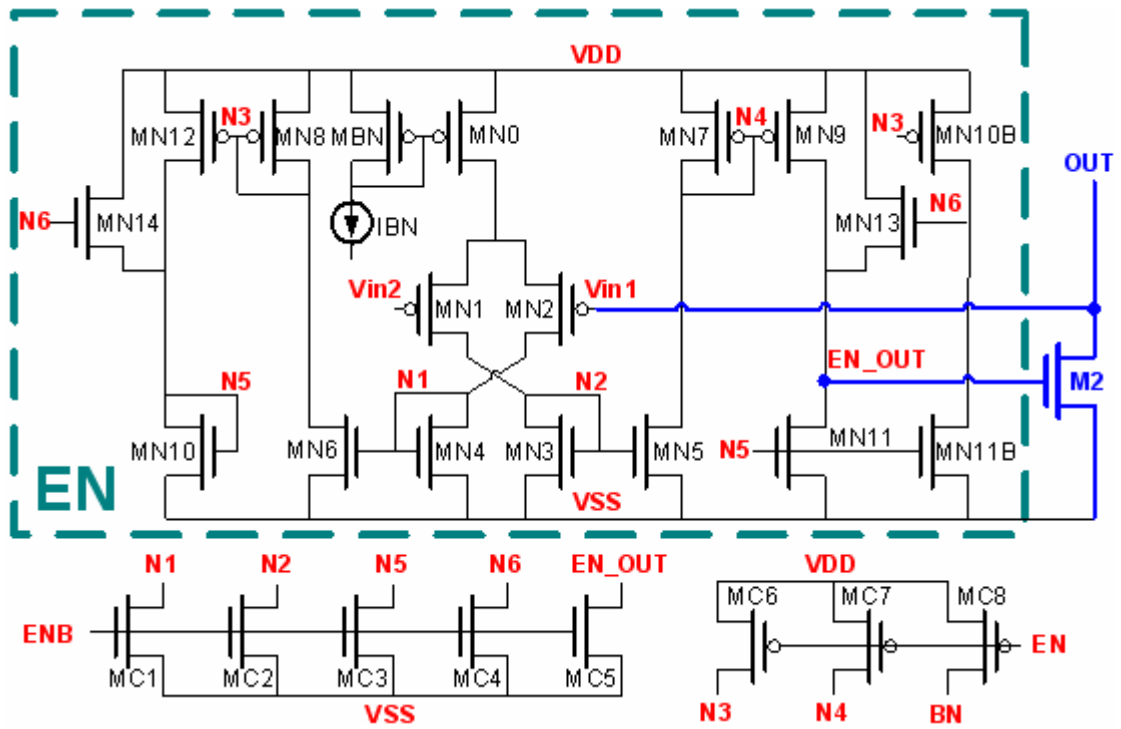
**Figure 2.4** Schematic of the error amplifier EN

**Table 2-3** Transistors W/L ratio of Fig.2.4

| MOS | MBN | MN0 | MN1 | MN2 | MN3 | MN4 | MN5 | MN6 |
|---|---|---|---|---|---|---|---|---|
| W/L(μm) | 25/4 | 25/4 | 50/5 | 50/5 | 10/4 | 10/4 | 10/4 | 10/4 |
| M | 1 | 20 | 24 | 24 | 4 | 4 | 4 | 4 |
| MOS | MN7 | MN8 | MN9 | MN10 | MN11 | MN12 | MP13 | MP14 |
| W/L(μm) | 5/4 | 5/4 | 5/4 | 5/4 | 50/4 | 50/4 | 9/4 | 9/4 |
| M | 2 | 2 | 2 | 2 | 20 | 20 | 2 | 2 |
| MOS | M2 | MN11B | MN10B | MC1 | MC2 | MC3 | MC4 | MC5 |
| W/L(μm) | 66/2.5 | 50/4 | 5/4 | 5/2.5 | 5/2.5 | 5/2.5 | 5/2.5 | 5/2.5 |
| M | 182 | 20 | 4 | 1 | 1 | 1 | 1 | 1 |
| MOS | MC6 | MC7 | MC8 | | | | | |
| W/L(μm) | 5/3 | 5/3 | 5/3 | | IBN=10uA | | | |
| M | 1 | 1 | 1 | | | | | |

To further analyze this newly proposed circuit, let us begin with the quiescent condition. Setting all the transistors symmetrical, $(W/L)_1=(W/L)_2$, $(W/L)_3=(W/L)_4$, $(W/L)_5=(W/L)_6$, $(W/L)_7=(W/L)_8$, $(W/L)_9=(W/L)_{10}$, $(W/L)_{11}=(W/L)_{12}$, and $(W/L)_{13}=(W/L)_{14}$, the tail current $I_{P0} = I_{BP} \dfrac{(W/L)_{P0}}{(W/L)_{BP}}$ will be equally distributed into $M_{P1}$ and $M_{P2}$. Ignoring channel length modulation,

$$I_{P5} = I_{P6} = I_{P7} = I_{P8} = \frac{I_{BP}}{2} \frac{(W/L)_{P0}}{(W/L)_{BP}} \frac{(W/L)_{P5}}{(W/L)_{P3}} \tag{2.1}$$

$$I_{P9} = I_{P10} = \frac{I_{BP}}{2} \frac{(W/L)_{P0}}{(W/L)_{BP}} \frac{(W/L)_{P5}}{(W/L)_{P3}} \frac{(W/L)_{P9}}{(W/L)_{P7}} \tag{2.2}$$

Setting $(W/L)_{10B}=2(W/L)_{10}$, gives

$$I_{P10B} \cong 2I_{P10} \tag{2.3}$$

Setting $(W/L)_{11}=(W/L)_{11B}$, gives

$$I_{P11} \cong I_{P11B} = I_{P10B} \cong 2I_{P10} = 2I_{P9} \tag{2.4}$$

Since $\left| I_{P11} \right| = \left| I_{P13} \right| + I_{P9}$,

$$\left| I_{P13} \right| = \left| I_{P11} \right| - I_{P9} \cong 2I_{P9} - I_{P9} = I_{P9} \tag{2.5}$$

Therefore, the quiescent current of the output buffer is well-defined as

$$I_{quiescent} \approx I_1 = 2I_{P10} \frac{(W/L)_1}{(W/L)_{P11}} = I_{BP} \frac{(W/L)_{P0}}{(W/L)_{BP}} \frac{(W/L)_{P5}}{(W/L)_{P3}} \frac{(W/L)_{P9}}{(W/L)_{P7}} \frac{(W/L)_1}{(W/L)_{P11}} \tag{2.6}$$

This equation shows that the drain current in $M_1$ is controlled by $I_{BP}$ and the (W/L) ratio of transistors, if the offset voltage of the error amplifier EP is zero, $V_O = 0$ when $V_i = 0$. To find the gain of the error amplifier in the quiescent condition, we assume that the input differential voltage is small enough so that $M_{P10B}$ can be regarded as a constant current source. Considering the entire small signal current from the differential pair flows at the error-amplifier output, EP_OUT, the transconductance is

$$G_m = \frac{g_{mP1}}{2} \frac{1}{g_{mP3}} g_{mP5} \frac{1}{g_{mP7}} g_{mP9} + \frac{g_{mP2}}{2} \frac{1}{g_{mP4}} g_{mP6} \frac{1}{g_{mP8}} g_{mP10} \left( \frac{1}{g_{mP12}} // \frac{1}{g_{mP14}} \right) g_{mP11}. \tag{2.7}$$

In the quiescent condition, $g_{mP1} = g_{mP2}$, $g_{mP3} = g_{mP4}$, $g_{mP5} = g_{mP6}$, $g_{mP7} = g_{mP8}$,

$g_{mP9} = g_{mP10}$, $g_{mP11} = g_{mP12}$, $g_{mP13} = g_{mP14}$, and $g_{mP12} >> g_{mP14}$ because $I_{P12} \cong 2I_{P14}$, and

the W/L ratio of $M_{P12}$ is usually much lager than $M_{P14}$ so as to reduce the quiescent current.

Therefore, we can simplify (2.7) as

$$G_m = g_{mP1} \frac{1}{g_{mP3}} g_{mP5} \frac{1}{g_{mP7}} g_{mP9} \tag{2.8}$$

The output resistance of the error amplifier is dominated by the source-follower transistor

$M_{P13}$, and
$$R_O = \frac{1}{g_{mP13} + g_{mb\ P13}} = \frac{1}{g_{mP13}(1+\eta)} \tag{2.9}$$

The coefficient $\eta = \dfrac{g_{mb\ P13}}{g_{mP13}}$, and

$$A_{EP} = G_m R_O = g_{mP1} \frac{1}{g_{mP3}} g_{mP5} \frac{1}{g_{mP7}} g_{mP9} \frac{1}{g_{mP13}(1+\eta)} \tag{2.10}$$

Since $g_m = \sqrt{2k'(W/L)I_d}$, and $I_{P1} = I_{P3}$, $I_{P5} = I_{P7}$, $I_{P9} = I_{P13}$. (2.10) can be re-written as

$$A_{EP} = \sqrt{\frac{(W/L)_{P1}}{(W/L)_{P3}} \frac{(W/L)_{P5}}{(W/L)_{P7}} \frac{(W/L)_{P9}}{(W/L)_{P13}}} \frac{1}{(1+\eta)} \tag{2.11}$$

The above equation shows that the gain of the error amplifier is well-defined by the W/L

ratio of transistors with appropriate bias. In practice, the drain current of $M_{P10B}$ will vary with

the input differential voltage, $V_d=(V_{in1}-V_{in2})$. If $V_d$ is negative, $M_{P1}$ will conduct more tail

current than $M_{P2}$. As the difference increases, so does $I_{P9}$, too, but $I_{P11}$ decreases. When

$I_{P9} = I_{P11}$, $M_{P13}$ will be cutoff, and the output impedance of the error amplifier is no longer

dominated by the source-follower transistor, $M_{P13}$. The output impedance of the error

amplifier $R_O \approx (r_{O\ P9} // r_{O\ P11})$, and voltage gain will highly increase to the order about an

$g_m r_O$. This results in an additional benefit. The higher gain of the amplifiers enhances the

linearity of output buffer under higher output power operation.

Consider the boundary condition of the above situation. This happens at $I_{P1} = 2I_{P2}$, and

$$I_{P1} = \frac{1}{2} k'(W/L)_{P1} (V_{in} + \frac{V_d}{2} - V_t)^2 = \frac{2}{3} I_{P0} = \frac{2}{3} \frac{(W/L)_{P0}}{(W/L)_{BP}} I_{BP} \tag{2.12}$$

$$I_{P2} = \frac{1}{2}k'(W/L)_{P2}(V_{in} - \frac{V_d}{2} - V_t)^2 = \frac{1}{3}I_{P0} = \frac{1}{3}\frac{(W/L)_{P0}}{(W/L)_{BP}}I_{BP} \qquad (2.13)$$

From (2.12), and (2.13), the threshold input differential voltage, which cuts off the transistor M$_{P13}$, is

$$V_d = \sqrt{\frac{I_{BP}}{3k'(W/L)_{P1}}\frac{(W/L)_{P0}}{(W/L)_{BP}}(2 - \sqrt{2})} \qquad (2.14)$$

However, in practice, there are always some mismatches of the error amplifiers caused by unexpected random effects. If the random offset voltage, V$_{OS}$, is higher than $V_d$ shown in (2.14), the gain of the error amplifier will increase considerably, and the quiescent current will be out of control. Therefore, $V_d$ is chosen to be bigger than the expected random offset voltage.

In section 1.1.1, (1.24) shows how to estimate the possible variation of the quiescent current at a given offset voltage. This equation, however, should be modified since the gain of the error amplifier shown in Fig.2.2 will be changed with V$_{OS}$ increasing. Now, define $A_{OS}$ as the changed gain of both two error amplifiers, EP and EN, when V$_{OSP}$ and V$_{OSN}$ exist as shown in Fig.1.5. The equation (1.24) becomes

$$\frac{\Delta I_Q}{I_Q\big|_{\substack{VOSP=0 \\ VOSN=0}}} \cong A_{OS}\left(\frac{V_{OSP} - V_{OSN}}{V_{OV,M1}}\right) \qquad (2.15)$$

The $A_{OS}$ represents the gain of error amplifiers, EP and EN, affected by V$_{OSP.}$ Review (2.10), the ratio, $\frac{g_{mP1}}{g_{mp3}}$ and $\frac{g_{mP5}}{g_{mp7}}$, will not be affected by V$_{OSP}$, but $\frac{g_{mP9}}{g_{mp13}}$ will. Therefore,

$$\frac{(A_{EP})_{OS}}{A_{OS}\big|_{VOSP=0}} \cong \frac{(g_{mP9})_{OS}}{g_{mP9}}\frac{g_{mP13}}{(g_{mP13})_{OS}} = \sqrt{\left(1 + \frac{\Delta I_{d9}}{I_{d9}}\right)\left(\frac{1}{1 - \Delta I_{d13}/I_{d13}}\right)} \qquad (2.16)$$

Considering how V$_{OSP}$ affects the input differential pair;

$$\left|\frac{\Delta I_{P1}}{I_{P1}}\right| = \left|\frac{\Delta I_{P2}}{I_{P2}}\right| = \frac{\left(V_{OV\,P1} + \frac{V_{OSP}}{2}\right)\frac{V_{OSP}}{2}}{V_{OV\,P1}^2} \qquad (2.17)$$

Assuming $V_{OV,MP1} >> V_{OSP}/2$, $\left| \dfrac{\Delta I_{P1}}{I_{P1}} \right| = \left| \dfrac{\Delta I_{P2}}{I_{P2}} \right| = \dfrac{V_{OSP}}{2V_{OV,MP1}}$ (2.18)

Applying similar reasoning to (2.2), and (2.5),

$$\frac{\Delta I_{d9}}{I_{d9}} = \frac{V_{OSP}}{2V_{OV,MP1}} \frac{(W/L)_{P5}}{(W/L)_{P3}} \frac{(W/L)_{P9}}{(W/L)_{P7}}$$ (2.19)

$$\frac{\Delta I_{d13}}{I_{d13}} = 2\frac{\Delta I_{d9}}{I_{d9}} = \frac{V_{OSP}}{V_{OV,MP1}} \frac{(W/L)_{P5}}{(W/L)_{P3}} \frac{(W/L)_{P9}}{(W/L)_{P7}}$$ (2.20)

Substituting (2.19) and (2.20) with (2.16) and rearranging properly,

$$\frac{(A_{EP})_{OS}}{A_{OS}\big|_{VOSP=0}} = \sqrt{\frac{2V_{OV,MP1} + V_{OSP}\dfrac{(W/L)_{P5}}{(W/L)_{P3}}\dfrac{(W/L)_{P9}}{(W/L)_{P7}}}{2V_{OV,MP1} - 2V_{OSP}\dfrac{(W/L)_{P5}}{(W/L)_{P3}}\dfrac{(W/L)_{P9}}{(W/L)_{P7}}}}$$ (2.21)

The above equation shows an important result. To minimize the variation of $A_{OS}$ affected by $V_{OS}$, the W/L ratio of $\dfrac{(W/L)_{P5}}{(W/L)_{P3}} \dfrac{(W/L)_{P9}}{(W/L)_{P7}}$ must not be too big.

## 2.3.3 Short circuit protection

Consider the block diagram shown in Fig.2.2 without short circuit protection function. If we accidentally connect the output to $V_{SS}$ or $V_{DD}$, or operate the chip improperly, M1 or M2 will be damaged or the whole system will be overheated because of the unexpectedly large output current caused by a short-circuited output.

Fig.2.5 shows the schematic of a short circuit protection function for the power transistor $M_1$. A complementary structure used to protect $M_2$ is shown in Fig.2.6. Consider the transistors $M_{EP1} \sim M_{EP5}$, which form an one-stage error amplifier, ESP, used to sense output current. By connecting ESP, $M_{SP1}$, $M_{SP5}$ and $M_{SP2}$ as a feedback loop, the differential inputs of ESP, OUT and $V_{SEN\_P}$ can be regarded as virtually short-circuited. Thus the drain current of $M_1$ can be sensed accurately by $M_{SP1}$ with a ratio of $\dfrac{(W/L)_{MSP1}}{(W/L)_{M1}}$. $M_{SP5}$ and $M_{SP0}$ form a current mirror so that $I_{MSP5}$ will provide a nearly constant current to bias $M_{SP2}$. Without $I_{MSP5}$,

$M_{SP2}$ may be in triode region when $M_{SP1}$ senses a very small current. Under a condition like this, the feedback loop may be unstable. By adding a compensation capacitor CC1, and appropriately biasing $M_{SP2}$, the problem of stability can be resolved.
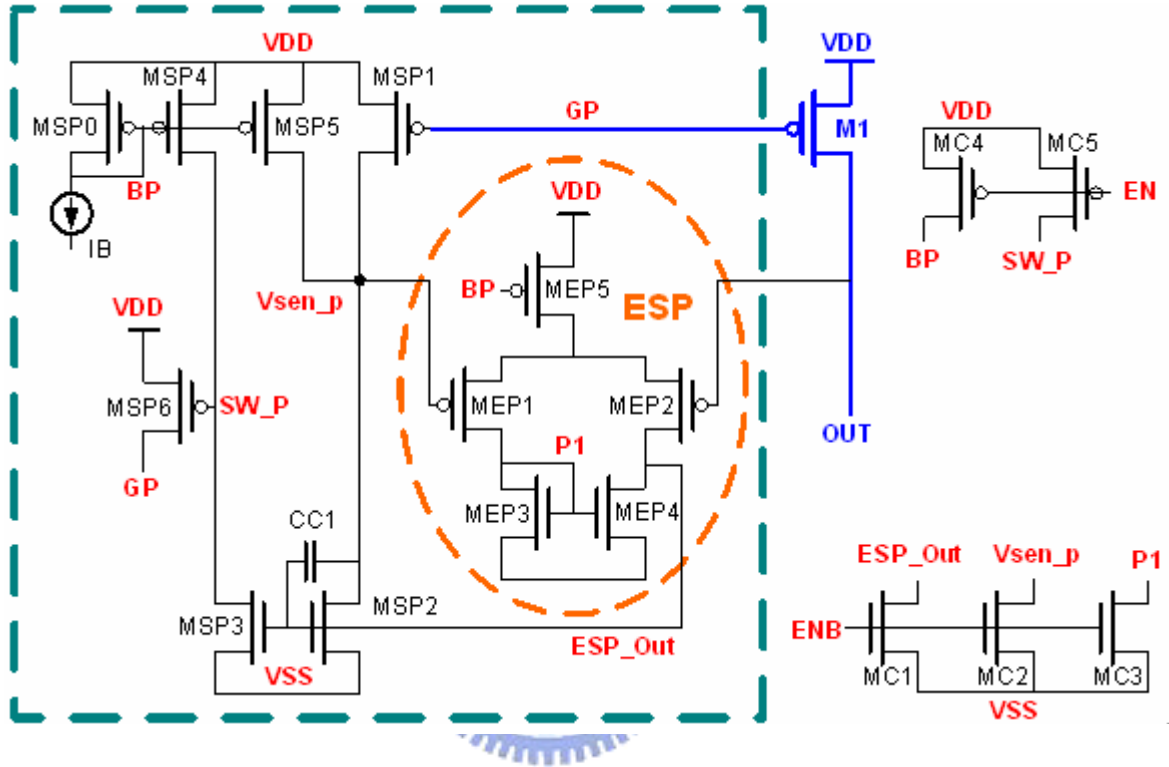


**Figure 2.5** Schematic of M1 short circuit protection

| MOS | M1 | MSP0 | MSP1 | MSP2 | MSP3 | MSP4 | MSP5 | MSP6 |
|---|---|---|---|---|---|---|---|---|
| W/L(μm) | 106/3 | 6/3 | 6.6/50 | 6/12 | 6/12 | 6/3 | 6/3 | 50/3 |
| M | 198 | 2 | 1 | 1 | 1 | 12 | 4 | 10 |
| MOS | MEP1 | MEP2 | MEP3 | MEP4 | MEP5 | MC1 | MC2 | MC3 |
| W/L(μm) | 6/4 | 6/4 | 6/6 | 6/6 | 6/3 | 6/2.5 | 6/2.5 | 6/2.5 |
| M | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| MOS | MC4 | MC5 | | | | | | |
| W/L(μm) | 6/3 | 6/3 | | IB=5uA | | | | |
| M | 1 | 1 | | CC1=0.5P | | | | |

**Table 2-4** Transistors W/L ratio of Fig.2.5
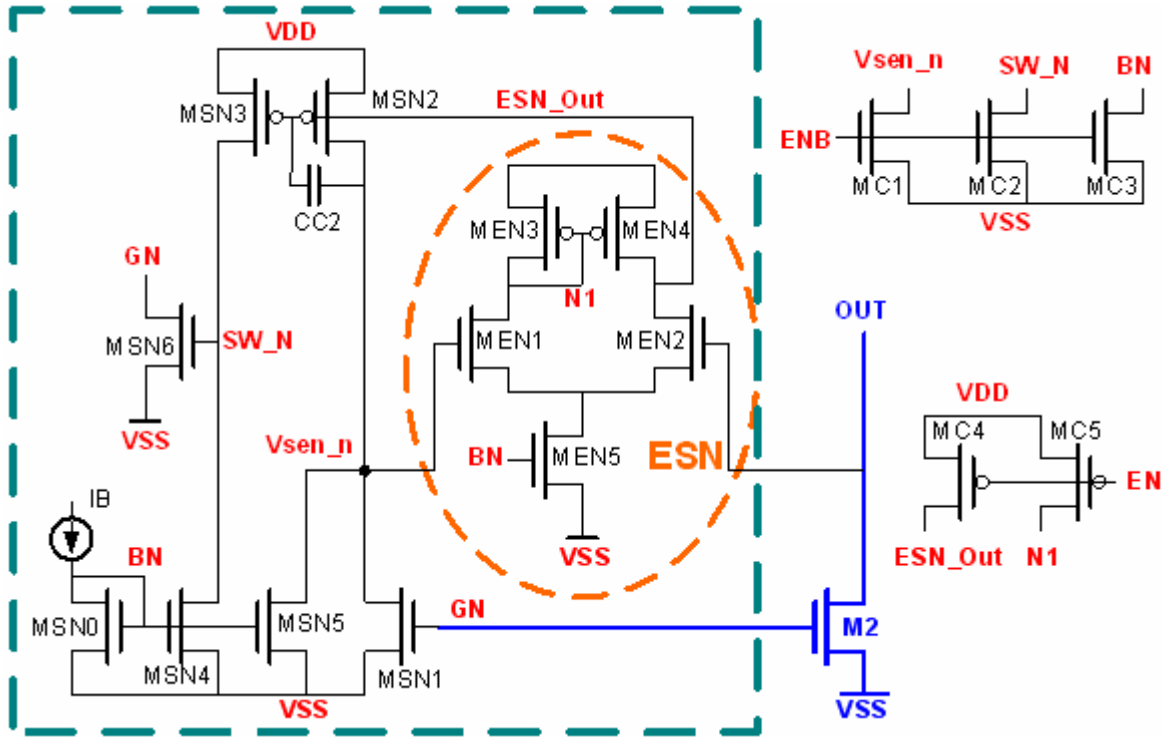
**Figure 2.6** Schematic of M2 short circuit protection

| MOS | M2 | MSN0 | MSN1 | MSN2 | MSN3 | MSN4 | MSN5 | MSN6 |
|---|---|---|---|---|---|---|---|---|
| **W/L(μm)** | 66/2.5 | 6/6 | 5/50 | 6/6 | 6/6 | 6/6 | 6/6 | 6/2.5 |
| **M** | 182 | 2 | 1 | 2 | 2 | 26 | 4 | 2 |
| **MOS** | **MEN1** | **MEN2** | **MEN3** | **MEN4** | **MEN5** | **MC1** | **MC2** | **MC3** |
| **W/L(μm)** | 6/6 | 6/6 | 6/6 | 6/6 | 6/6 | 6/2.5 | 6/2.5 | 6/2.5 |
| **M** | 1 | 1 | 1 | 1 | 2 | 1 | 1 | 1 |
| **MOS** | **MC4** | **MC5** | | | | | | |
| **W/L(μm)** | 6/3 | 6/3 | | | **IB=5uA** | | | |
| **M** | 1 | 1 | | | **CC2=0.5P** | | | |

**Table 2-5** Transistors W/L ratio of Fig.2.6

$M_{SP1}$, $M_{SP2}$, $M_{SP3}$, and $M_{SP4}$ can be considered as a current comparator. The transistor $M_{SP2}$ mirrors a constant current from $M_{SP0}$, and $M_{SP1}$ senses a current from $M_1$. When $I_{SP1}$ is bigger than the set current $I_{SP4}$, $M_{SP3}$ will be in triode region, and the voltage at node SW_P will be pulled down to turn on the transistor $M_{SP6}$. As $M_{SP6}$ is turned on, the source-gate voltage of M1 will be limited, which enables the function of short circuit protection.

When designing a circuit as shown in Fig.2.5, we will probably focus on the condition where Vout > Vref, under which M1 is turned on. Otherwise, when $V_{OUT} < V_{REF}$, the Class-AB output stage will cutoff M1. However, we shall not neglect the effects of the circuit where $V_{OUT} < V_{REF}$.    When $V_{OUT}$ is much lower than $V_{REF}$, the drain-source voltage of $M_{SP5}$ is much higher than its gate-source voltage. Considering channel length modulation, $I_{MSP5}$ may become larger than $I_{MSP4}$. When the system starts, the voltages at all nodes will be $V_{SS}$ in the beginning. After M1 charges node OUT for a short period of time, $V_{OUT}$ reaches $V_{REF}$. If $I_{MSP5}$ gets larger than $I_{MSP4}$ due to channel length modulation, $M_{SP6}$ will be turned on, which cuts off M1and consequently stops it from charging node OUT. All these reactions will result in a deadlock. Therefore, the criteria for enabling short circuit protection is

$I_{MSP1(Sen\sin g)} > I_{MSP4} - I_{MSP5}$ . That is to say, $I_{MSP4}$ and $I_{MSP5}$ should not be set compatible in case of malfunction.
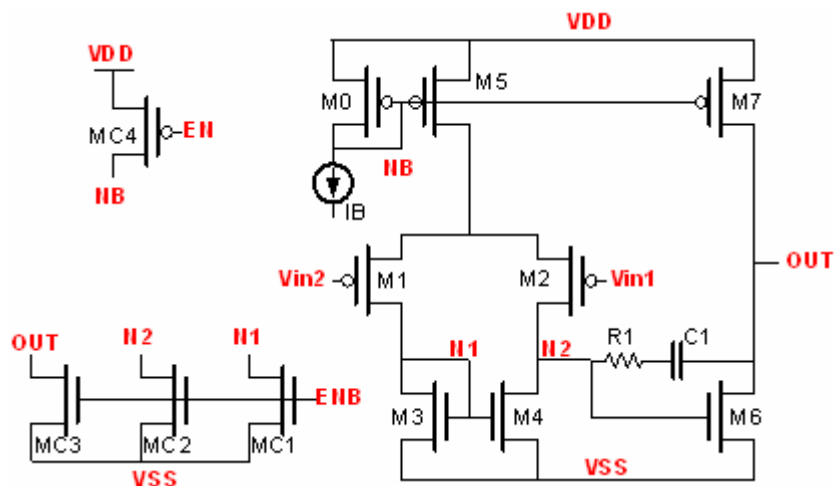


**Figure 2.7** Schematic of pre-amplifier using in Fig.2.2

| MOS | M0 | M1 | M2 | M3 | M4 | M5 | M6 | M7 |
|---|---|---|---|---|---|---|---|---|
| W/L(μm) | 6/6 | 6/20 | 6/20 | 6/6 | 6/6 | 6/6 | 6/6 | 6/6 |
| M | 2 | 10 | 10 | 2 | 2 | 4 | 30 | 30 |
| MOS | MC1 | MC2 | MC3 | MC4 | IB=1uA | | | |
| W/L(μm) | 6/2.5 | 6/2.5 | 6/2.5 | 6/3 | R1=40K | | | |
| M | 1 | 1 | 1 | 1 | C1=1.5P | | | |

**Table 2-6** Transistors W/L ratio of Fig.2.7

## 2.3.4   Frequency compensation

The circuit proposed in this thesis is applied to the audio band. Human ears respond to sound vibrations frequencies between 200Hz and 20KHZ. It is there anticipated that bandwidth is probably not the main concern for an audio amplifier. Take the specifications in Table 1-1 for example, since the design target for Unit Gain Bandwidth is merely0.6MHz, a common two-stage amplifier as shown in Fig.2.7 as the pre-amplifier will do. This pre-amplifier is designed with a high DC gain and a low bandwidth (0.8MHz). The buffered output stage as discussed in Sec. 2.3.2. is designed with a dominant pole 10 times larger than the unit gain frequency of the pre-amplifier, which saves the complex problem of frequency compensation.

To simplify the stability analysis of the buffered output stage, that $pole \approx \dfrac{1}{2\pi RC}$ is appropriated here. The circuit shown in Fig.2.3 contains several poles, including nodes, P1, P2, P3, P4, P5, EP_OUT, and OUT. Consider this transistor size listed in table 2-2. The power transistor M1 must be large enough to drive a desired output power, and transistors $M_{P11}$, $M_{P11B}$, $M_{P12}$ can't be too small to define the quiescent current. Therefore, the parasitical capacitance at node EP_OUT will be the maximum. To obtain a higher gain in the differential

pair, $M_{P1}$ and $M_{P2}$ are usually chosen of a larger size. We can therefore derive the comparisons of parasitical capacitance at these nodes from the size of each transistor as

$$OUT > EP\_OUT > P1 > P2 > P5 > P3 > P4 . \tag{2.22}$$

Although node OUT carries the biggest parasitical capacitance, it is connected to a resistors as small as 8 Ohm that helps push its pole to the high frequency domain. As a result, the order of poles at all node in the frequency domain will be

$$EP\_OUT < P1 \approx P2 < P5 < P3 \approx P4 < OUT . \tag{2.23}$$

As mentioned earlier that $M_{SP13}$ will be cutoff as the voltage $V_{OUT}$ increases, it will change the equivalent resistance at EP_OUT from $\dfrac{1}{g_{mP13}}$ to $(r_{O,P9} // r_{O,P11})$, and the pole of EP_OUT will thus move to the lower frequency domain. Therefore, it should be carefully considered whether the moved dominate pole would affect the stability of the pre-amplifier.
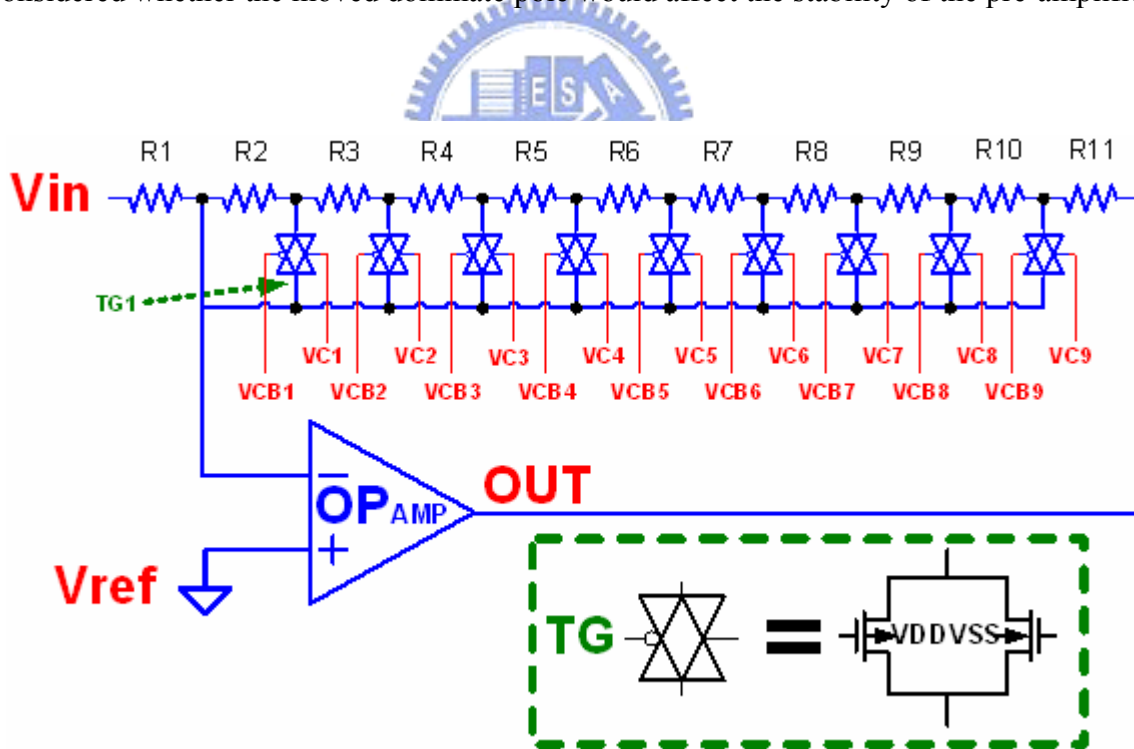


| R1=480K | R2=90K | R3=120K | R4=90K | R5=70K | R6=50K |
|---------|--------|---------|--------|--------|--------|
| R7=40K  | R8=30K | R9=20K  | R10=20K | R11=30K |        |

**Figure 2.8** Schematic of Volume control circuit

| MOS | M0 | M1 | M2 | M3 | M4 | M5 | M6 | M7 |
|---|---|---|---|---|---|---|---|---|
| W/L(μm) | 5/8 | 5/10 | 5/10 | 5/8 | 5/8 | 5/8 | 5/8 | 5/8 |
| M | 2 | 10 | 10 | 1 | 1 | 2 | 20 | 20 |
| MOS | MC1 | MC2 | MC3 | MC4 | IB=1uA | | | |
| W/L(μm) | 5/2.5 | 5/2.5 | 5/2.5 | 5/3 | R1=0 | | | |
| M | 1 | 1 | 1 | 1 | C1=0.7P | | | |

**Table 2-7** An alternative list of W/L ratio of transistors in Fig.2.7.

## 2.4    Volume control circuit

Fig.2.8 shows the block diagram of the Volume control circuit which is made up of an inverting feedback OPAMP and 9 transmission gates. The schematic of the OPAMP is the same as Fig.2.7, but the dimensions of transistors are different (See Table 2-7). When the switch of a transmission gate is active, the corresponding parallel resistor will become short circuited. When all the transmission gates are switched open, the inverting close loop gain of OPAMP reaches the maximum. As TG1 is active, its close loop gain decreases. When these transmission gates are inactivated in order, a 10 level volume control is therefore made possible.

Since human hearing is measured by the log scale, resistors in this design should be specially chosen so that the 10 level close loop gain is linear in log scale.

That is $\quad \alpha \dfrac{R_2 + R_3 + ... + R_{10} + R_{11}}{R_1} = \dfrac{R_3 + R_4 + ... + R_{10} + R_{11}}{R_1}$ ,

$$\alpha \dfrac{R_3 + R_4 + ... + R_{10} + R_{11}}{R_1} = \dfrac{R_4 + R_5 + ... + R_{10} + R_{11}}{R_1} ,$$

$$...$$

$$\alpha \dfrac{R_{10} + R_{11}}{R_1} = \dfrac{R_{11}}{R_1} \qquad\qquad \text{, and so on.}$$

Therefore, the fixed difference of each volume level is $20\log\alpha$ .

## 2.5    DC control 10 level volume

Fig.2.9 shows a simple analog to digital converter. Transistors, MS1~MS9, are mirrored current sources, which are connected to the corresponding NMOS, MV1~MV9, below, to form 9 inverters. By setting that the closer the NMOS is to the right in Fig2.10, the smaller W/L ratio it has, the respective switching voltage of the 9 inverters will be in order as a rising sequence. As VCON increases gradually, these 9 inverters will be switched on one by one. That is to say, one single DC Voltage VCON is enough to generate a set of 9 control signals, VC[1:9] and VCB[1:9], which is used to control the 9 transmission gates in Fig.2.8. On the other hand, inverters MS10 and MV10 are used as a control signal generator for the MUTE function. When VMUTE gets larger than 2.5V, BUF_EN exports signal 0, and BUF_ENB, 1. This will turn off power transistors M1 and M2 in Fig.2.2.

INV_C, as shown in Fig.2.9, is a inverter chain. It is illustrated in detail in Fig2.10. The INV_C as an inverter chain is used to make the switch signal transient very fast.
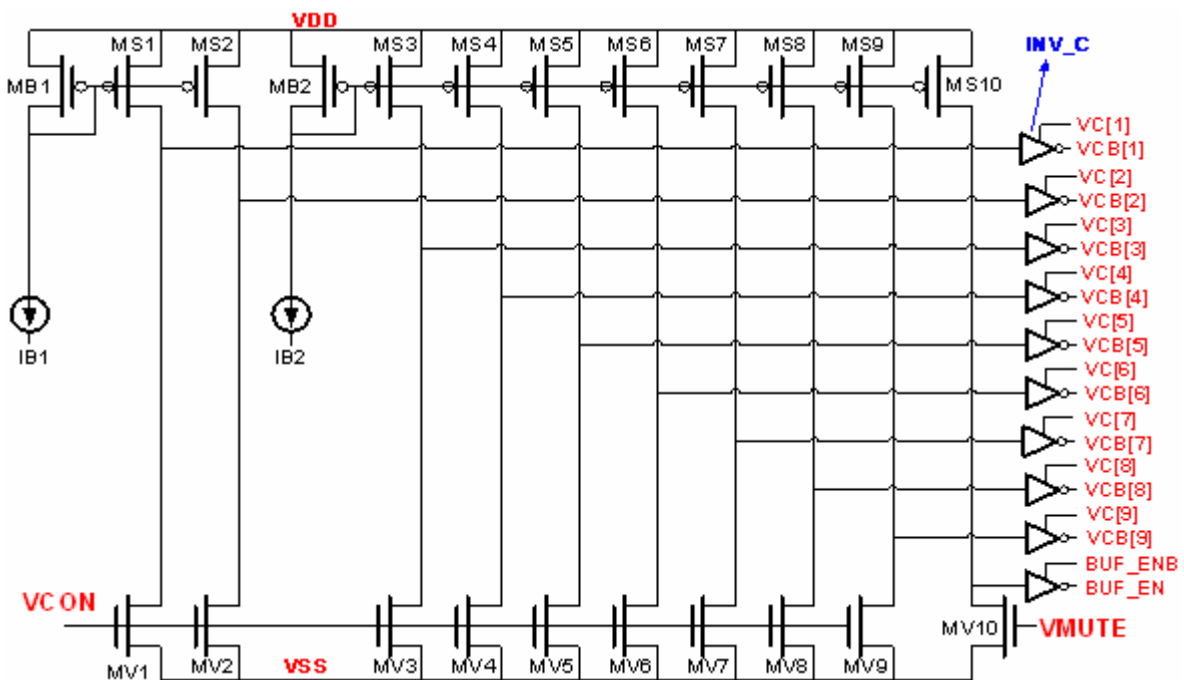


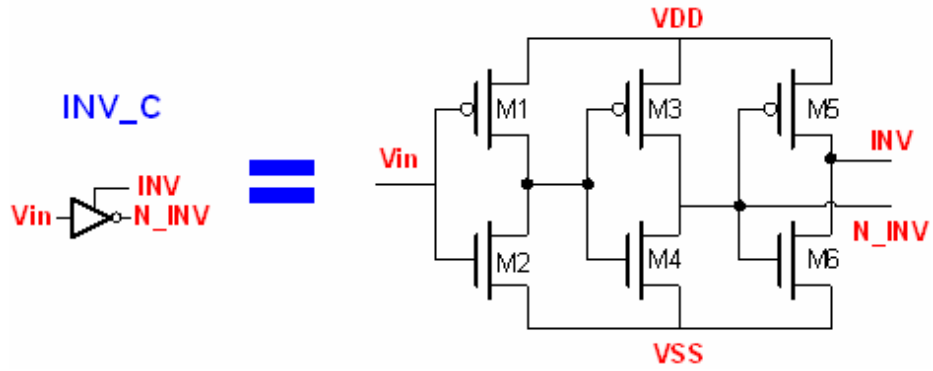**Figure 2.9** A simple Analog to Digital converter

**Figure 2.10** Schematic of symbol INV_C shown in Fig.2.9

| MOS | MB1 | MB2 | MS1 | MS2 | MS3 | MS4 | MS5 | MS6 |
|---|---|---|---|---|---|---|---|---|
| W/L(μm) | 4/5 | 4/5 | 4/5 | 4/5 | 4/5 | 4/5 | 4/5 | 4/5 |
| M | 5 | 1 | 1 | 1 | 1 | 1 | 1 | 2 |
| MOS | MS7 | MS8 | MS9 | MS10 | MV1 | MV2 | MV3 | MV4 |
| W/L(μm) | 4/5 | 4/5 | 4/5 | 4/5 | 4/2.5 | 4/3 | 4/4 | 4/6.5 |
| M | 2 | 3 | 3 | 1 | 20 | 2 | 2 | 1 |
| MOS | MV5 | MV6 | MV7 | MV8 | MV9 | MV10 | M1 | M2 |
| W/L(μm) | 4/14 | 4/12.5 | 4/19 | 4/18 | 4/24 | 4/15 | 5/4 | 5/4.7 |
| M | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 1 |
| MOS | M3 | M4 | M5 | M6 | | | | |
| W/L(μm) | 5/5 | 5/5 | 5/5 | 5/5 | IB1=2uA | | | |
| M | 1 | 1 | 1 | 1 | IB2=2uA | | | |

**Table 2-8** Transistors W/L ratio of Fig.2.9 and Fig.2.10
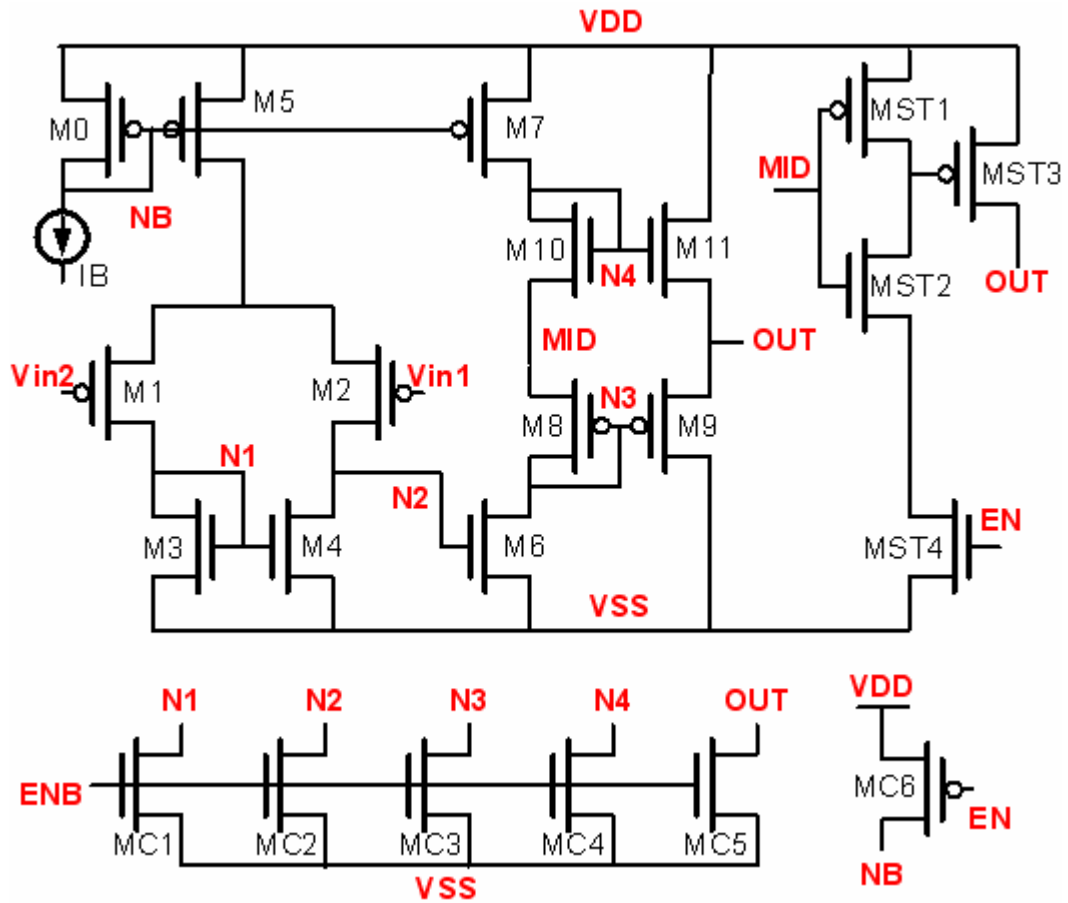
**Figure 2.11** Schematic of OPAMP used as a buffer for driving Vref

| MOS | M0 | M1 | M2 | M3 | M4 | M5 | M6 | M7 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| W/L(μm) | 5/12 | 5/9 | 5/9 | 5/9 | 5/9 | 5/12 | 5/9 | 5/12 |
| M | 2 | 4 | 4 | 2 | 2 | 2 | 4 | 2 |
| MOS | M8 | M9 | M10 | M11 | MST1 | MST2 | MST3 | MST4 |
| W/L(μm) | 20/4 | 20/4 | 20/4 | 20/4 | 5./3 | 5/25 | 32/5 | 5/2.5 |
| M | 2 | 8 | 2 | 8 | 1 | 1 | 18 | 1 |
| MOS | MC1 | MC2 | MC3 | MC4 | MC5 | MC6 | **IB=5uA** | |
| W/L(μm) | 5/25 | 5/25 | 5/25 | 5/25 | 5/25 | 5./3 | | |
| M | 1 | 1 | 1 | 1 | 1 | 1 | | |

**Table 2-9** Transistors W/L ratio of Fig.2.11.

## 2.6    Reference voltage generator

In Fig.2.1, we use two diode connecting PMOS to generate the reference voltage,

$V_{MID} = \dfrac{V_{DD} - V_{SS}}{2}$ . Any current flowing out or into VMID will change its voltage. This is why

we need the unit gain buffer, OP$_{VREF}$. Usually, a very large capacitor is used to connect VREF

and VSS to avoid unexpected interference from the power supply. According to the

application notes of TDA7496L, a 470uF capacitor is advised. Fig.2.11 shows the amplifier,

OPVREF, with a common-drain output stage. With an output capacitor load so big as 470uF,

the output node of the amplifier will be the dominate pole in frequency domain. Consider the

transient at the start. It may take a very long time to charge the 470uF capacitor load to the

required voltage, $\dfrac{V_{DD} - V_{SS}}{2}$ . Transistors MST1~MST4 are therefore used to shorten the

charging time. When the system is shut down, the control signals will be EN=Low,

ENB=High. All of the voltage at node N1, N2, N3, N4, MID, OUT will be Low, too. However,

when the system starts, the control signal is reversed, and the VMID will be high enough to

trigger the inverter, MST1 and MST2, to turn on transistor MST3. Before the voltage VOUT

is charged to $\dfrac{V_{DD} - V_{SS}}{2}$ , VSW will be reversed again, and turn off MST3.

# CHAPTER 3

# Simulation result and discussion

## 3.1 Chip layout

The chip of our design is fabricated by the UMC 0.5um +/-20V2P2M high voltage process. To be economical, we only use two layers of metal. The chip dimension is 2210um x 3497um as shown in Fig.3.1, and Fig.3.2 shows its function blocks accordingly.
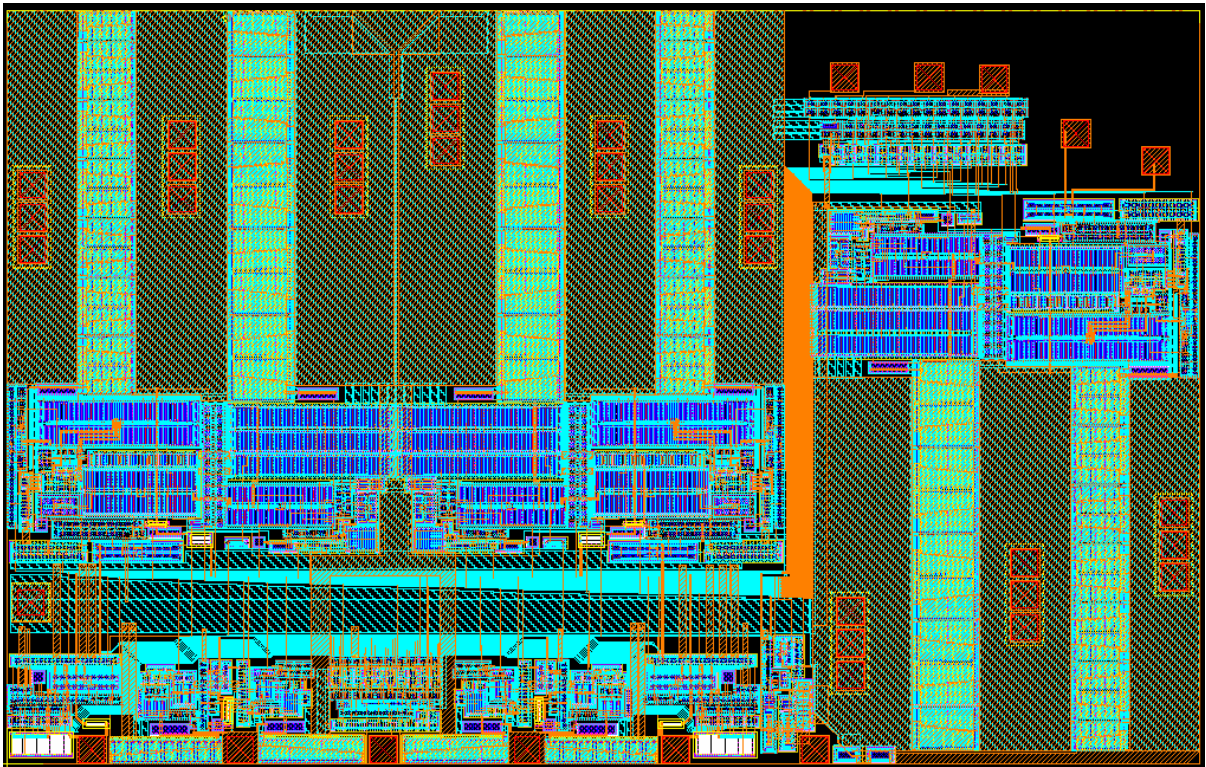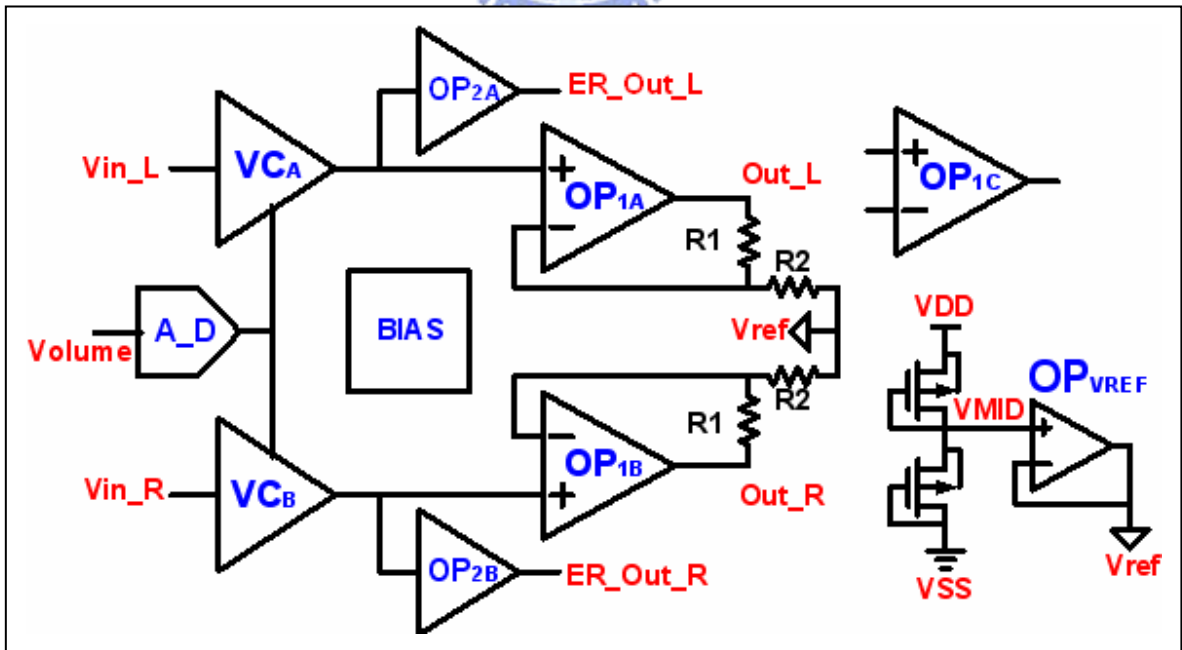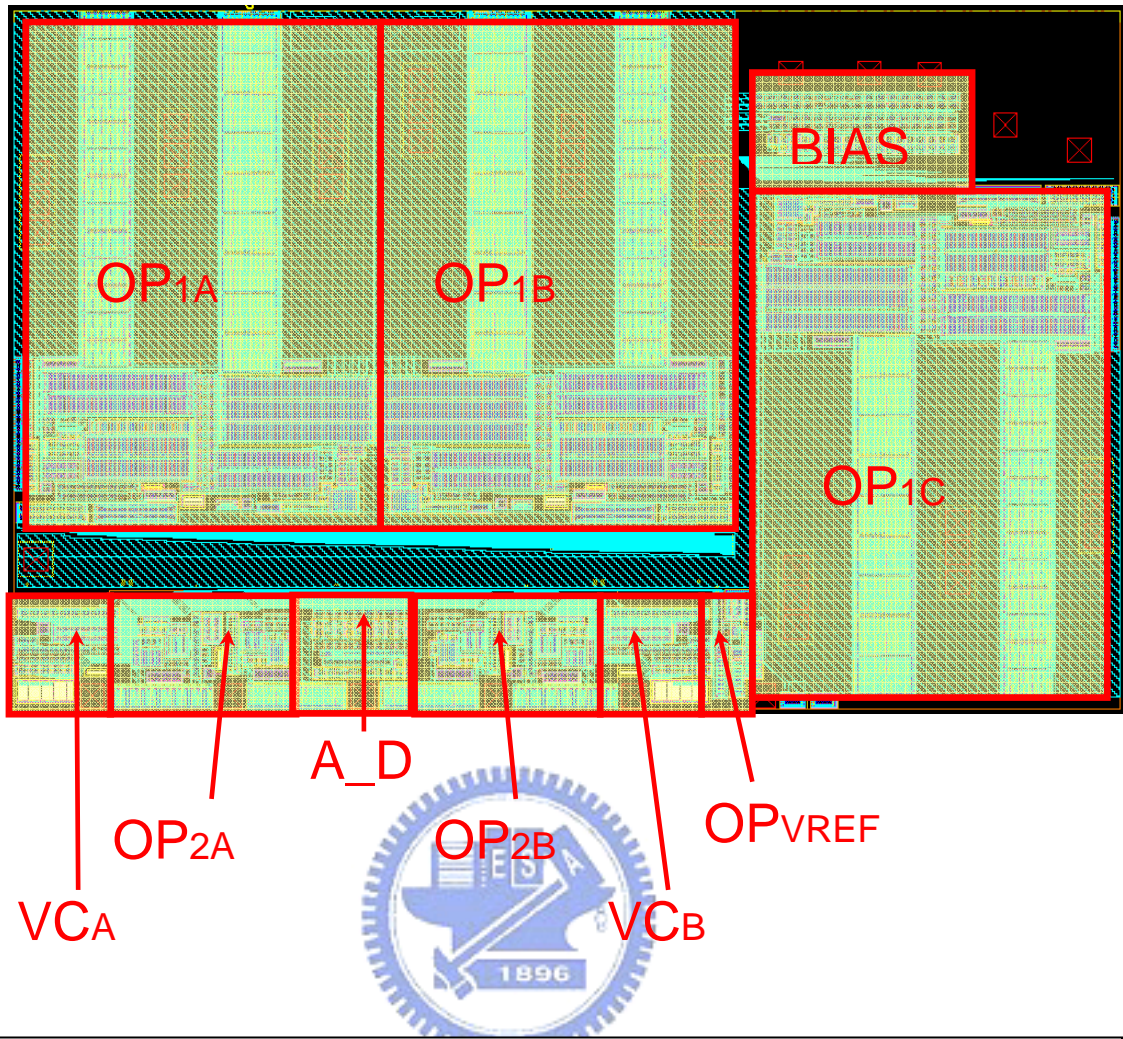


**Figure 3.1** Chip layout view

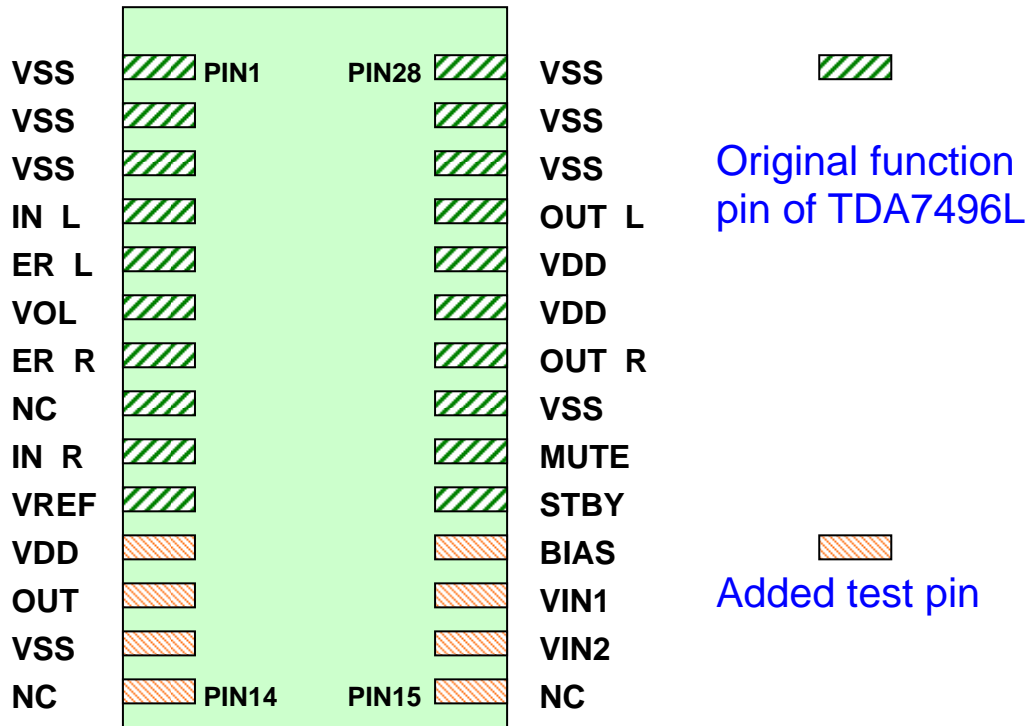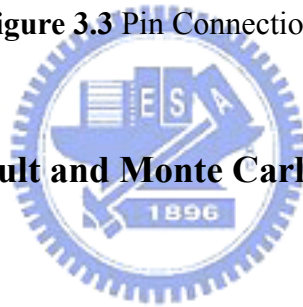**Figure 3.2** Chip layout view and its according function blocks

**Figure 3.3** Pin Connection after packaging

## 3.2 Pre-Simulation result and Monte Carlo analysis

(1) Buffered amplifier

| Frequency Response of buffered amplifier | | | VDD=10V | VDD=18V |
|---|---|---|---|---|
| FF 0℃ | Gain | | 108 dB | 113dB |
| | PM | | 96° | 99° |
| | GB | | 0.63 MHz | 0.99MHz |
| TT 30℃ | Gain | | 103dB | 109dB |
| | PM | | 87° | 91° |
| | GB | | 0.63MHz | 0.74MHz |
| SS 70℃ | Gain | | 101dB | 108dB |
| | PM | | 84° | 77° |
| | GB | | 0.45 MHz | 0.54MHz |

With $R_L=8\Omega$, $C_L=30pF$

**Table 3-1**. The frequency response
pre-simulation result of buffered amplifier

| Quiescent current of buffered amplifier | | |
|---|---|---|
| | VDD=10V | VDD=18V |
| FF 70℃ | 9.1mA | 12mA |
| TT 30℃ | 7.6mA | 11mA |
| SS 0℃ | 7.6mA | 9.5mA |

With $R_L=8\Omega$, $C_L=30pF$

**Table 3-2.** The quiescent current
pre-simulation result of buffered amplifier

| The output peak current of power MOS | | |
|---|---|---|
| | M1 | M2 |
| FF 0℃ | 1.15A | 0.95A |
| TT 30℃ | 1.05A | 1.13A |
| SS 70℃ | 0.91A | 0.82A |

VDD=14V $R_L=0.01\Omega$, $C_L=30pF$

**Table 3-3** The Output peak current of power MOS

**<Monte Carlo Analysis>**

We will refer to Monte Carlo Analysis and paper [13] to evaluate how big an impact mismatching would have on quiescent current. (3.1) and (3.2) show that the error of threshold voltage is inversely proportional to the square root of the MOS size.

$$\Delta V_{TH} = \frac{A_{VTH}}{\sqrt{WL}} \tag{3.1}$$

$$\frac{\Delta \beta}{\beta} = \frac{A_\beta}{\sqrt{WL}}, \quad \beta = \mu C_{OX} W/L \tag{3.2}$$

Set $A_\beta$ to be 10%, and $A_\beta$ is hereby derived by Vth in Table 3-4. Fig.3.4 shows the error

percentage of quiescent current yielded by mismatching out of 100 Monte Carlo Analyses.

| Device | Delta-$V_{th}$ in different Corner | | |
|---|---|---|---|
| | SS | TT | FF |
| **Symmetry HVNMOS** | 0.182 | 0 | -0.182 |
| **Asymmetry HVNMOS** | 0.178 | 0 | -0.178 |
| **Symmetry HVPMOS** | -0.291 | 0 | 0.291 |
| **Asymmetry HVPMOS** | -0.340 | 0 | 0.340 |

**Table 3-4** The value of Delta-Vth for different
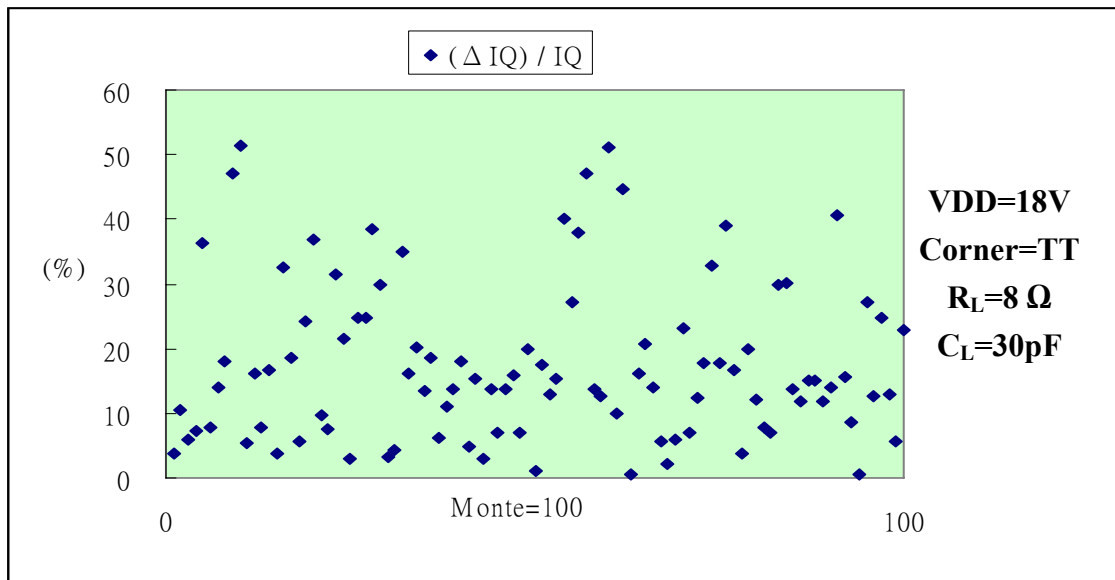transistors and corners of the UMC process



**Figure 3.4** The quiescent Monte Carlo analysis of buffered amplifier
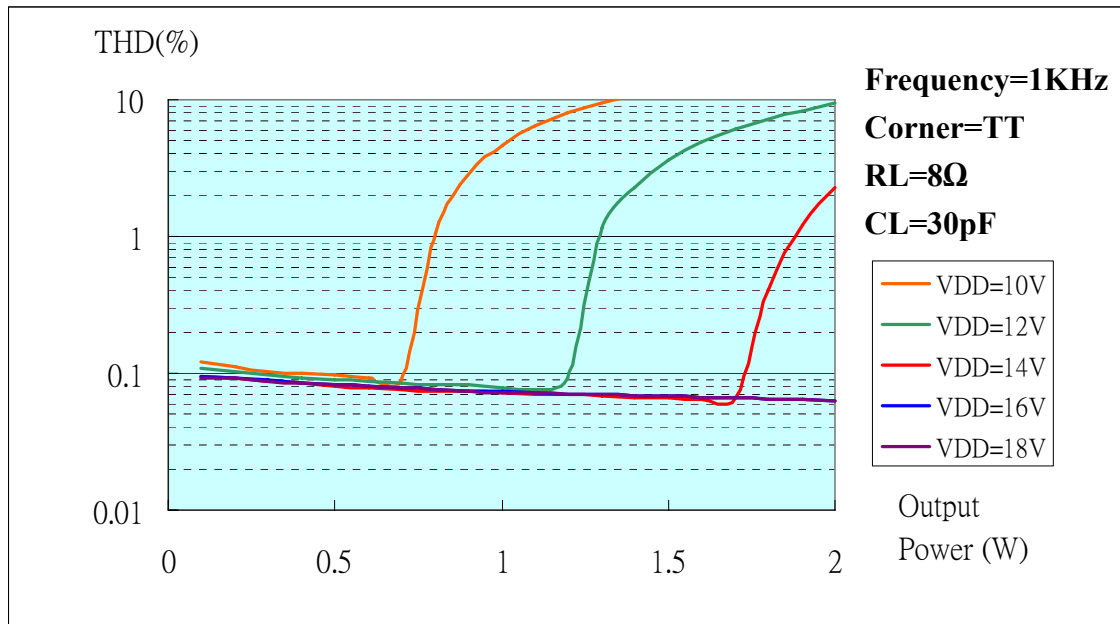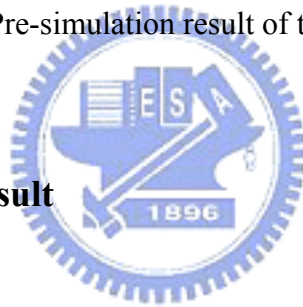
(2) Total harmonic distortion



THD(%)

Frequency=1KHz
Corner=TT
RL=8Ω
CL=30pF

VDD=10V
VDD=12V
VDD=14V
VDD=16V
VDD=18V

Output Power (W)

**Figure 3.5** The Pre-simulation result of total harmonic distortion

## 3.3 Post-Simulation result

(1) Buffered amplifier

| Frequency response of buffered amplifier | | | | | |
|---|---|---|---|---|---|
| | | Pre-Simulation | | Post-Simulation | |
| Supply voltage | | VDD=10V | VDD=18V | VDD=10V | VDD=18V |
| FF 0℃ | Gain | 108 dB | 113dB | 109dB | 115dB |
| | PM | 96° | 99° | 81° | 81° |
| | GB | 0.63 MHz | 0.99MHz | 1.29MHz | 1.50MHz |
| TT 30℃ | Gain | 100dB | 106dB | 104dB | 110dB |
| | PM | 70° | 70° | 72° | 75° |
| | GB | 0.75MHz | 0.79MHz | 0.67MHz | 0.80MHz |
| SS 70℃ | Gain | 101dB | 108dB | 106dB | 112dB |
| | PM | 84° | 77° | 59° | 60° |
| | GB | 0.45 MHz | 0.54MHz | 0.46MHz | 0.50MHz |
| With $R_L$=8Ω, $C_L$=30pF | | | | | |

**Table 3-5** The frequency response
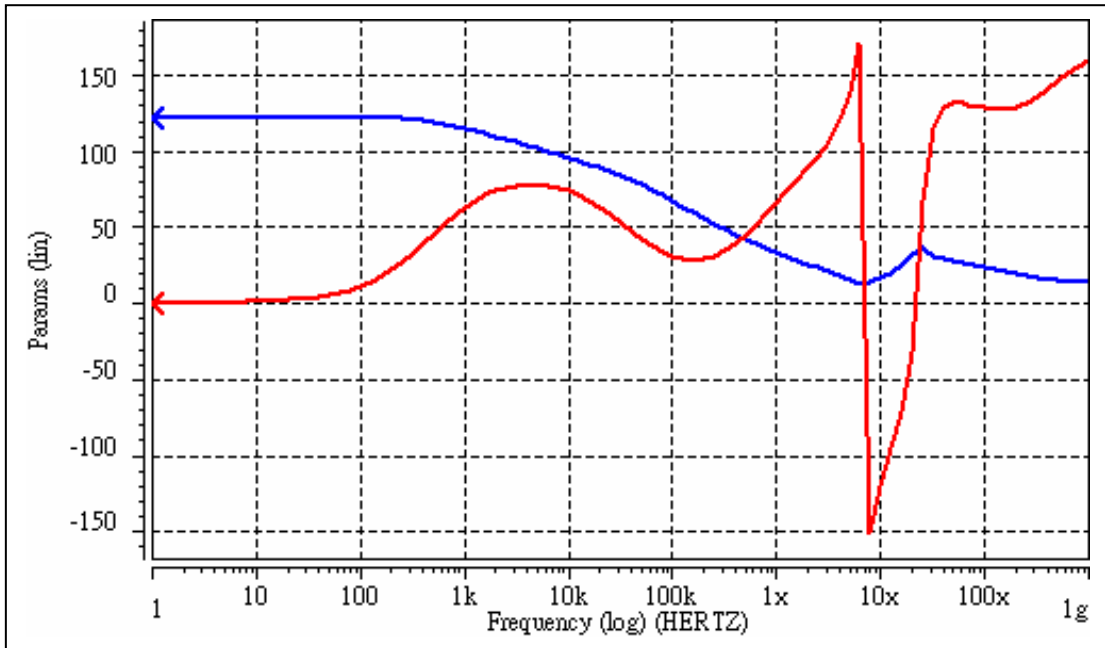post-simulation result of buffered amplifier

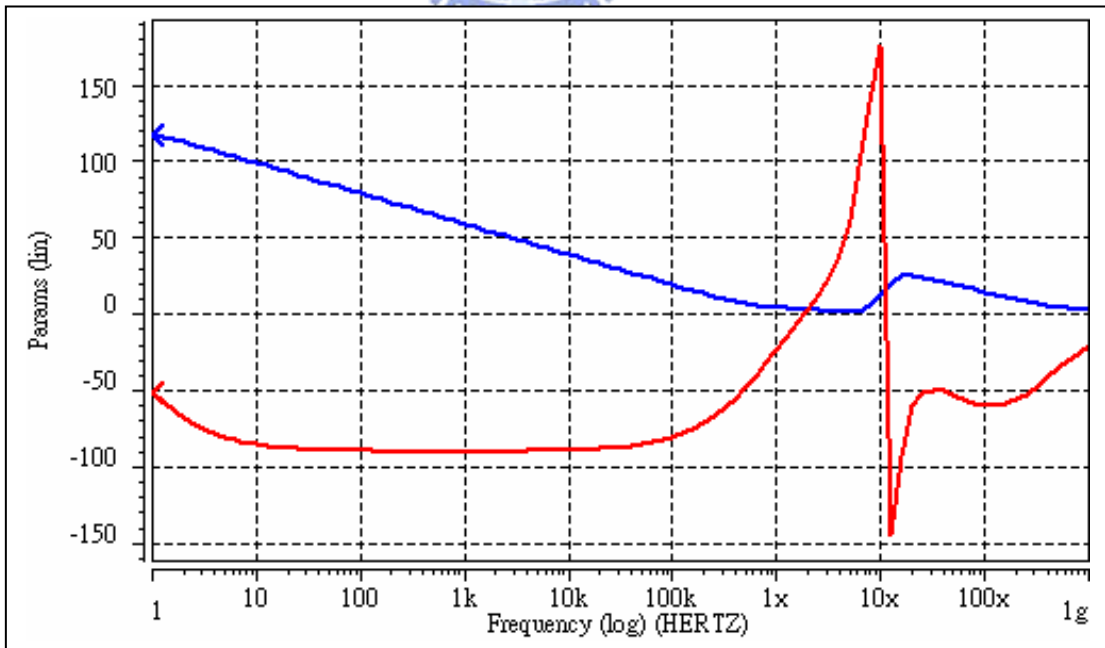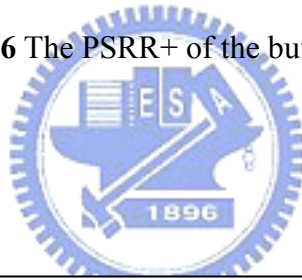**Figure 3.6** The PSRR+ of the buffered amplifier



**Figure 3.7** The PSRR- of the buffered amplifier

(2) Total harmonic distortion
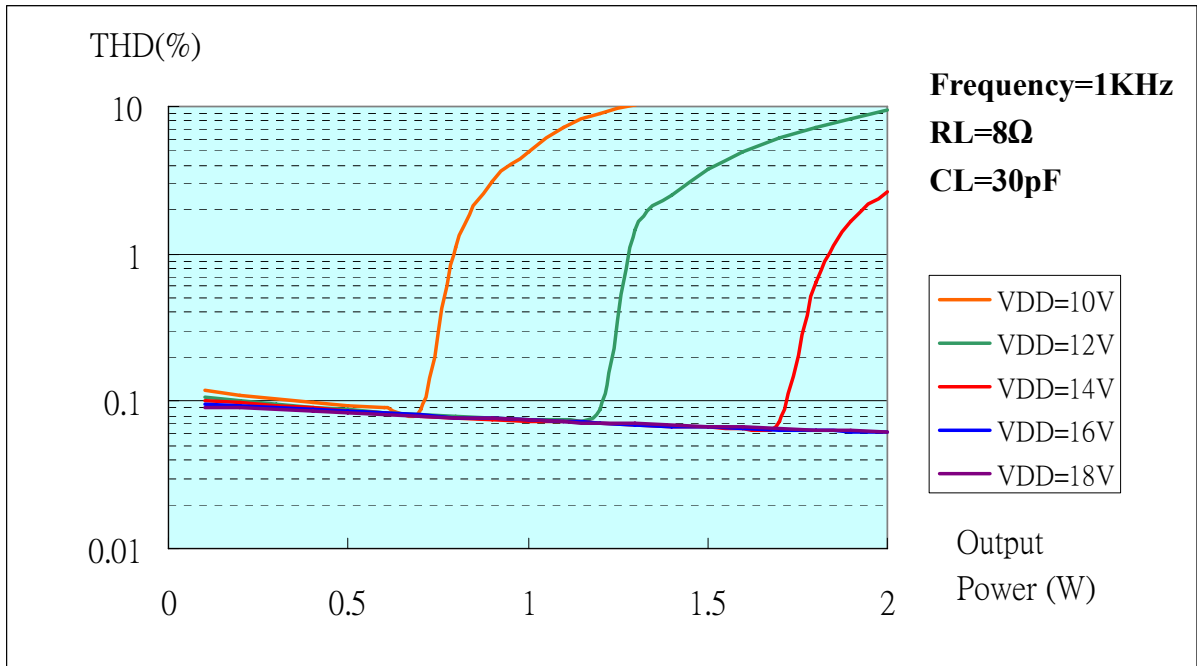


**Figure 3.8** The post-simulation of total harmonic distortion

(3) Volume control amplifier

| Frequency Response | | | VDD=10V | VDD=18V |
|---|---|---|---|---|
| **FF 0℃** | **Gain** | | 103dB | 109dB |
| | **PM** | | 72° | 73° |
| | **GB** | | 1.01MHz | 1.02MHz |
| **TT 30℃** | **Gain** | | 100dB | 106dB |
| | **PM** | | 71° | 72° |
| | **GB** | | 0.73MHz | 0.78MHz |
| **SS 70℃** | **Gain** | | 98dB | 103dB |
| | **PM** | | 59° | 60° |
| | **GB** | | 0.64MHz | 0.63MHz |
| With $C_L$=3pF | | | | |

**Table 3-6** The frequency response post-simulation
result of the volume control amplifier shown in

(4) DC control 10 level Volume



**VDD=14V, Corner=TT**
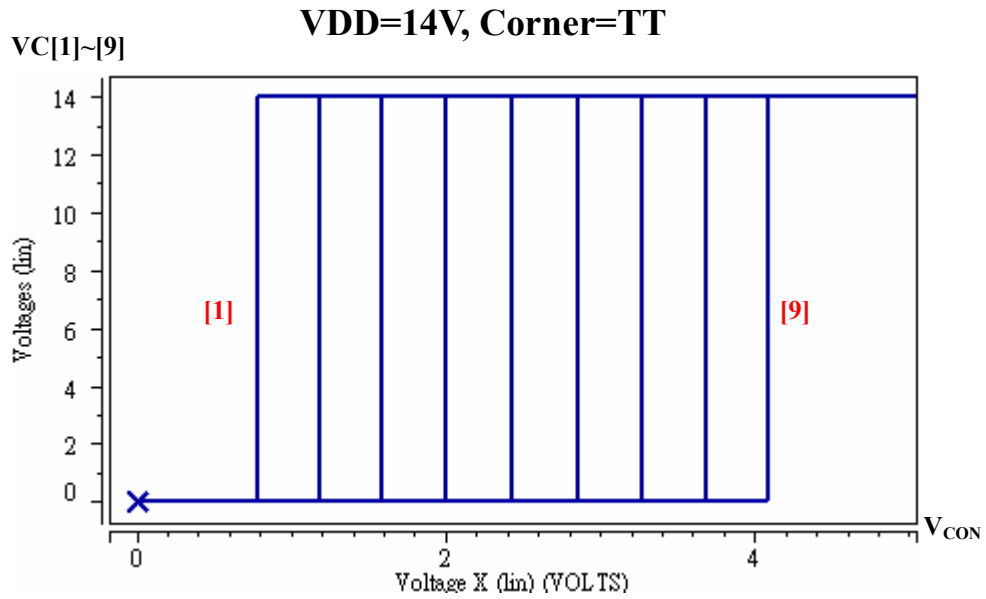
**Figure 3.9** VC[1]~VC[9] vs. $V_{CON}$ DC transfer function

(5) Amplifier for VREF

| Frequency Response | | VDD=10V | VDD=18V |
|---|---|---|---|
| **FF 0℃** | **Gain** | 72dB | 103dB |
| | **PM** | 81° | 72° |
| | **GB** | 4.4KHz | 1.01MHz |
| **TT 30℃** | **Gain** | 66dB | 106dB |
| | **PM** | 82° | 73° |
| | **GB** | 2.1KHz | 0.71MHz |
| **SS 70℃** | **Gain** | 57dB | 65dB |
| | **PM** | 83° | 59° |
| | **GB** | 0.7KHz | 1.7KHz |
| With $C_L$=470pF | | | |

**Table 3-7** The frequency response post-simulation result of the amplifier shown in Fig.2.11

### (6) Conclusions of simulation

Table 3-8 shows that the post simulation result of this work is better than the design specification which is refers to TDA-7496L. Also, Fig.3.10 and 3.11 show the relationship between supply voltage and out power. Compared with TDA-7496L, this chip can drive larger output power under the same supply voltage.

(Testing condition $V_S$ = 14V; $R_L$ = 8Ω, Temp=25℃)

| Symbol | Parameter | Test condition | SPEC. | Post-sim. | Unit |
|--------|-----------|----------------|-------|-----------|------|
| Vs | Supply voltage range | | 10~18 | 10~20 | V |
| Iq | Total quiescent current | | <50 | 20 | mA |
| $P_O$ | Output power | THD=1%, $R_L$=8Ω | >1.3 | 1.84 | W |
| THD | Total harmonic distortion | $P_O$=1W, f=1kHz | <0.4 | 0.073 | % |
| BW | Unit gain bandwidth | | >0.6 | 0.72 | MHz |
| Ipeak | Out peak current | | <1.2 | <1.10 | A |
| PSRR | Power supply rejection ratio | F=1kHz | >50 | 63 | dB |

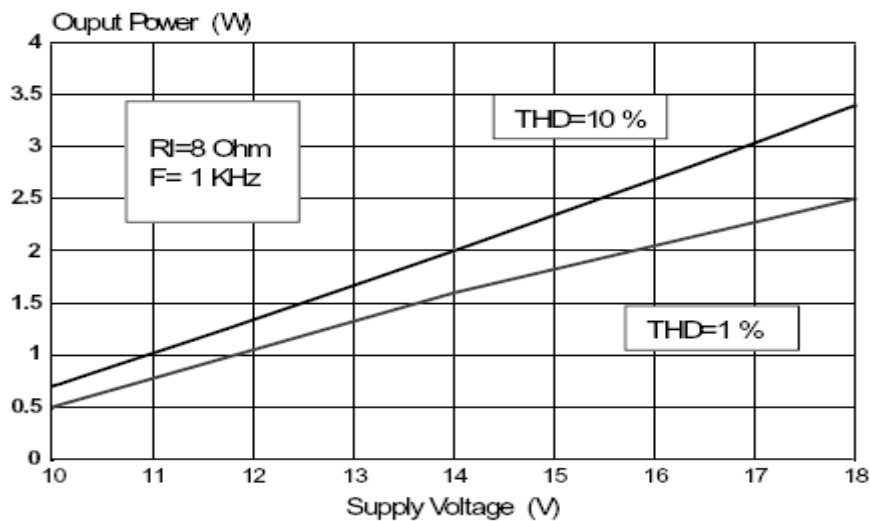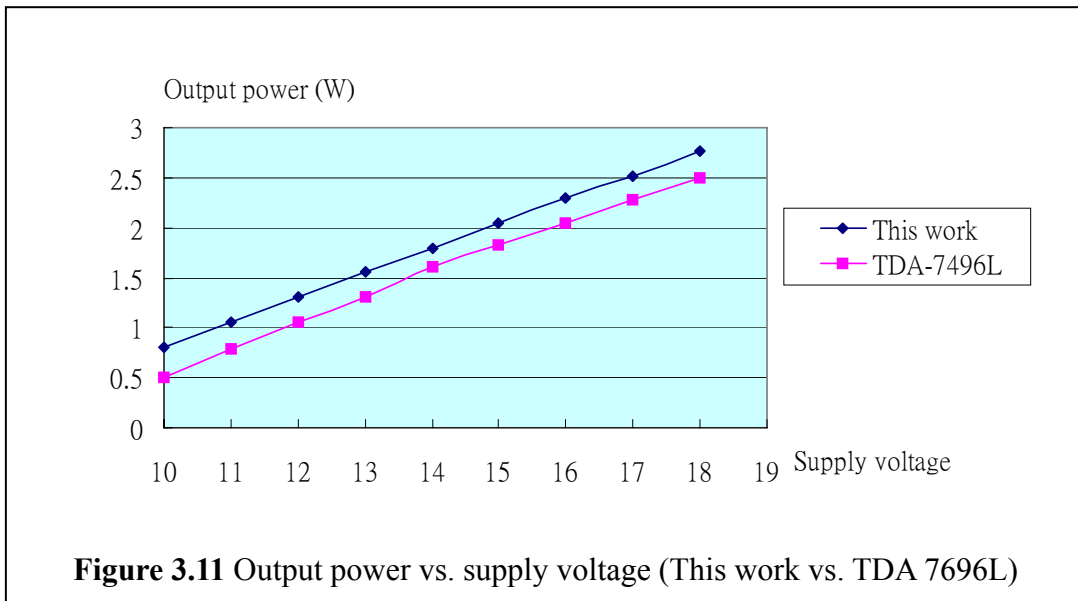**Table 3-8** The comparison of post-simulation result and design spec.



**Figure 3.10** Output power vs. supply voltage (TDA7496L)

Output power (W)

**Figure 3.11** Output power vs. supply voltage (This work vs. TDA 7696L)

## 3.4 Discussion

Under packaging, audio amplifiers with a large output power must deal with the problem of heat radiation; otherwise the chip will be over-heated. Our chip is packaged by SSOP28 process, as shown in Fig.4.4., where several ground pins are used to help with heat radiation. Compared with TDA7496L, our chip makes use of 8 more pins due to the existence of the test amplifier, OP1C. From Fig.3.3., we can see that the output stage power transistors of the buffered amplifier take up quite some space. This is because we only use two layers of metal and, to meet the required current density of the metal layer according to the UMC layout rule, we have to save much space for the metal layer. Meanwhile, it is rather convincing that, with just one more metal layer, we would size down the chip significantly and rearrange the layout of power transistors more efficiently.

# CHAPTER 4

# Conclusions and future work

## 4.1  Conclusions

This thesis, consulting the specifications in business industry, has put forth a high power, high linearity audio amplifier with complete features of volume control, mute mode, standby mode, and earphone output. The newly proposed error amplifiers, when used in Class-AB quasi-complementary output stage, prove to be highly applicable in well defining the quiescent current and saving it from the influence of offset voltage. Moreover, since the gain of error amplifiers increases accordingly with the augmentation of the output swing, we therefore derive better linearity with a high output power. From Table 3-14, it is simple to draw a comparison between our design and TDA7469L that we have a much smaller THD under the same output power. Besides, compared to the structures proposed in some other papers[6][7][8], since the amplifiers in our design have a large output swing, smaller-size power transistors will therefore suffice to reach the desired output power. Compare our structure specifically with that in reference [7], even though the error amplifier we proposed needs a slightly larger bias current, our structure is by far more applicable to the supply voltage of a much wider range.

## 4.2  Future work

Layout of the chip in discussion here has been completed; however, the process provider failed to schedule the fabrication in time. We therefore need to acquire detail measurements to verify whether the actual performance conforms to the post-simulation results. Besides,

although the fabrication process in use here guarantees a maximum supply voltage of 40V, this is done at the expense of certain characteristics of transistors. Restricted by packaging, we only came out with a design of a maximum output power of 2W, and a maximum supply voltage, 18V. It is a shame to underuse a fabrication process as such. Given the opportunity to apply a more suitable fabrication process with a maximum supply voltage of 20V, we are confident to size down the chip significantly and achieve even better performance.

Our structure provides a bandwidth sufficient enough for audio frequency band, though still not large enough for other applications. As discussed in section 2.3.4., the output stage is designed with a dominant pole 10 times larger than the unit gain frequency of the pre-amplifiers. In our design, it is difficult to locate an output stage dominant pole at a higher frequency domain since we have to at the same time take into account both a high output power and high linearity performance. This is not only the reason why the bandwidth of our structure is limited, but also a direction in which we may consider improving our structure in the future.

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