國立交通大學

電機學院微電子奈米科技產業研發碩士班

碩 士 論 文

寬通道側向電流效應之研究
與新穎薄膜電晶體結構之開發

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摘　　要

這篇論文中,第一次討論到寬通道薄膜電晶體的飽和電流和寬通道調變在線性變化區的關係.我們發現當通道寬度大於汲極源極寬度時,寬通道測向電流效應將產生.這個效應將在較寬的通道產生新的電流路徑和較低的總電阻使的飽和電流上升.

當通道的寬度漸漸增加時,飽和電流一開始會跟著通道的寬度增加而增加.然後到達某個定值後就跟通道的寬度增加無關.當通道的寬度大於有效的通道寬度時,飽和電流增加到最大值時.最大的飽和電流和通道長度汲極源極寬度有某種關係.我們發現飽和電流的增加比率和通道長度除以汲極源極寬度的值成正比隨著通道寬度的增加而增加.

The study of the side-channel current effect of wide channel width and the fabrications of the novel Poly-Si thin-film transistor structure

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ABSTRACT

In this paper, it is first time to discuss the ON-state drain current of a special TFT structure with a wider channel width and a narrower source/drain width in the linear region. We found that, when the channel width is wider than that of the source/drain, the side channel current effect (SCCE) would be generated, and this effect would cause the increase of the ON-state drain current due to the additional current flow paths existed in the side channel regions and lower channel resistance. As the side channel width increasing, the ON-state drain current would be initially increased and then gradually independent of the side channel width when the side channel width is larger than the effective side channel. The maximum ON-state drain current will apply to channel length and source/drain width. We also found that the ON-state drain current gain would be directly proportional to the channel length and the channel length to source/drain width ratio, and dependent on the side channel width.

誌　　謝

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Effect of channel width widening on a poly-Si TFT structure with a half side channel region in the linear region

Chapter 1

Introduction

1.1 Overview of Low Temperature Poly-Si TFTs

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have been intensively studied for application to high performance large-area active matrix liquid-crystal display (AMLCD) systems [1], [2]. They are commonly used in active-matrix liquid-crystal displays (AMLCDs) [3], [4] as pixel switches, drivers, and peripheral control circuits. In recent years, a lot of efforts have been put forth to improve the material quality and device structure of poly-Si TFTs to obtain better device performance. poly-Si TFTs have attracted much attention due to the possibility of realizing the integration of driving circuits and pixel elements on one glass substrate, and the potential to accomplish the system-on-panel (SOP) . High-performance poly-Si TFTs are required for this goal. In generally, poly-Si TFTs have two structures: top-gate coplanar structure and bottom-gate structure. The top-gate TFTs are mainly used in AMLCD application because their self-aligned source/drain regions provide low parasitic capacitances and are suitable for device scaling down. On the other hand, Bottom-gate TFTs have better interface and higher plasma hydrogenation rate than top-gate TFTs, but they have lower current and need extra process steps for backside exposure and difficult fabrication

Recrystallization technology is important for low temperature Poly-Si TFTs because of the grain size, grain boundary and intragranular defects [5], which influence the performance of Poly-Si TFTs. To achieve the large grain size, high performance and low temperature process, several recrystallization technologies have been proposed: solid phase crystallization (SPC) [6], eximer laser annealing (ELA) [7]–[9], and metal-induced lateral crystallization (MILC) [10] – [12] etc. In this paper, we use SPC to recrystallize the poly-Si TFTs.

The major advantages of applying poly-Si TFTs on AMLCDs are large carrier mobility and low photocurrent and high reliability. In poly-Si film, carrier mobility larger than 100 cm^2/Vs can be easily achieved [13].

The dominant leakage current mechanism in poly-Si TFTs is the field emission via the grain boundary traps by a high electric field near the drain. Therefore, reducing the lateral electric field near the drain junction is needed. For example, using a lightly doping drain structure can reduced the lateral electric field. The LDD structure certainly not only reduces the electric field but also enhances source/drain series resistance that limits the on-state current.

1.2 Issues in Low Temperature Poly-Si TFTs

Although the poly-Si TFTs were used to instead of the amorphous TFTs for the high mobility, the complex grain structure in poly-Si has a strong influence on device characteristics. Large amount of defects serving as trap states locate in the disordered grain boundary regions. These traps also cause the valence-band carriers to jump to conduction-band via trap-assisted thermionic emission or trap-assisted thermionic field emission, leading to large leakage current. It is well known that there are three kinds of the leakage current mechanisms in poly-Si TFTs . First, when the drain voltage is very low, the leakage current is governed by thermally generated carriers via the trap states. The leakage current therefore is dependent on the drain voltage, but independent of the gate voltage. Second, when the drain voltage is in the intermediate range, the leakage current is generated by the thermionic field emission of electrons indicated. In this case, the electrons in the valence-band are thermally excited to the trap states, and then tunnel to the conduction-band quantum mechanically. The leakage current therefore increases with increasing the gate voltage due to the narrowing of the barrier width. Third, when the gate voltage is high enough, the leakage current is governed by the field enhanced tunneling. Obviously, decreasing the drain electric field is helpful to reduce the leakage current.

Therefore, the poly-Si TFTs suffer from the high leakage current in the OFF-state and the kink effect in the ON-state [14]. The surface roughness of poly-Si film will enhance the local electrical field near the interface between gate oxide and channel, which will also degrade the reliability of TFT under high gate bias operation**.** However, LDD structure indeed reduces the electric field [15] but also causes high source/drain series resistance which limits the on-state current. Besides, an extra mask in LDD structures is a major problem [16], [17].

Besides, under the long-term operation, the stability of the poly-Si TFTs is a major issue. The hot carrier effect is also an important reliability in LTPS TFTs.

1.3 Motivation

Poly-Si TFTs can be used to integrate peripheral driver circuits on glass for system integration. In order to integrate peripheral driving circuits on the same glass substrate, both a large current drive and a high drain breakdown voltage are necessary for poly-Si TFT device characteristics. It has been previously reported that the use of a thinner active channel film is beneficial for obtaining a higher current drive [18], [19]. However, the use of thin active channel layer inevitably results in poor source/drain contact and large parasitic series resistance.

To achieve this ideal TFT structure, we have proposed a novel four-mask step TFT structure with self-aligned raised source/drain (SARSD) [20]. In SARSD TFT structure, a special structure with a wider channel width and a narrow source/drain width is formed. It also reported that a higher ON-state drain current would be obtained due to lower series resistance and additional current flow paths existing in the side-channel regions [20]. To explain the behavior of the ON-state drain currents of the Poly-Si TFT's and to simulate these ON-state drain current values, several models have been proposed [21]-[24]. The relationship of the ON-state drain current of the structure with a wider channel width and a narrower source/drain width on the channel width, the channel length and the source/drain width must be defined clearly. This is the motive of our study on the wider channel width effect in Poly-Si TFTs. We hope that this study would help those skilled in this art to further understand the behavior of the carrier transport in the channel region when the channel width is larger than the source/drain width and would explain the increase of the ON-state current of the wider channel width TFT structure, such as the SARSD TFT structure.

In this paper, we used a test structure with a wider channel width and a narrower source/drain width to study the influences of the channel width, the channel length and the source/drain width on the ON-state drain current. Because the kink effect would cause an anomalous current increase in the saturation region, we only focused on the ON-state drain current in the linear region in this paper.

1.4 Thesis Organization

In chapter 1, a brief overview of LTPS TFT technology and related applications were introduced.

In chapter 2, the effect of channel width widening on a poly-Si TFT structure in the linear

region will be discussed.

In chapter 3, the effect of channel width widening on a poly-Si TFT structure with a half side channel region in the linear region will be discussed.

Chapter 2

Effect of Channel Width Widening on a Poly-Si Thin-Film Transistor Structure in the linear region

2.1 Abstract

In this study, it is first time to discuss the ON-state drain current of a special TFT structure with a wide channel width and narrow source/drain width in the linear region. When the channel width is wider than that of the source/drain width, the ON-state drain current of the special TFT structure with a wide channel width and narrow source/drain width will be increased due to the additional current flow paths existing in the side channel regions and low channel resistance. As the side channel width increased, the ON-state drain current will initially increase and then gradually become independent of the side channel width. The ON-state drain current gain is proportional to the ratio of channel length to source/drain width.

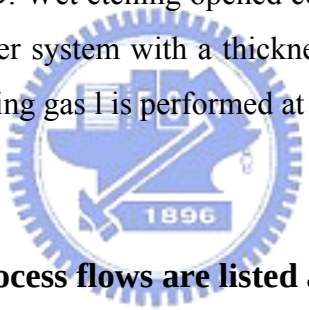
It also has been reported that a higher ON-state drain current would be obtained due to lower series resistance and additional current flow paths existing in the side-channel regions [22]. There are some articles discussed with the case of the narrow channel width [23]-[26], but there are no any articles discussed with the variations of the channel width which is larger than the source/drain width.

Therefore, before new physical models are proposed to explain and simulate the ON-state drain current of the structure with a wider channel width and a narrower source/drain width, the relationship of the ON-state drain current of the structure with a wider channel width and a narrower source/drain width on the channel width, the channel length and the source/drain width must be defined clearly.

In this paper, we used a test structure with a wider channel width and a narrow source/drain width to study the influences of the channel width, the channel length and the source/drain width on the ON-state drain current. Because the kink effect would cause an anomalous current increase in the saturation region, we only focused on the ON-state drain current in the linear region in this paper.

2.2. Device fabrication

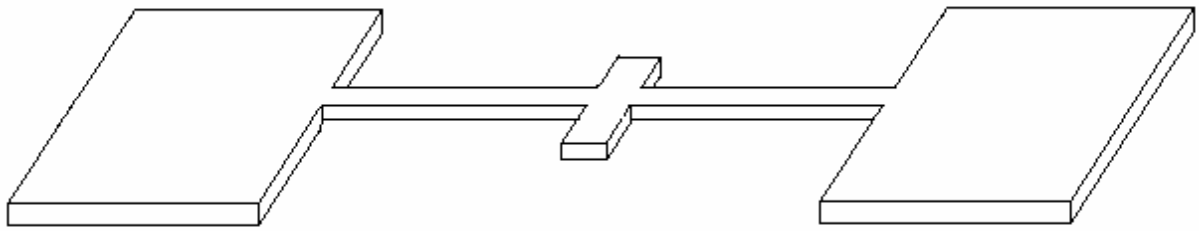
The fabrication processes of the tested n-channel poly-Si TFT with a wider channel width and a narrower source/drain width were as follows: A 50-nm thick α-Si layer for active region was deposited by low pressure chemical vapor deposition (LPCVD) system using SiH_4 at 550°C on 500-nm thermal oxidized silicon wafers, then 600°C 24 hr anneal (SPC). The active region was patterned by G-line stepper and was formed using reactive ion etching (RIE), as shown in Figure 2.1(a). A 50-nm low pressure chemical vapor deposition (LPCVD) TEOS gate oxide layer was deposited, and then a 300-nm LPCVD poly was deposited which was patterned by G-line stepper and was formed using reactive ion etching (RIE). G-line stepper system has a layer-to-layer misalignment, which is less than 0.15 μm, the gate region, as shown in Figure 1(b), having two overlapping regions that lengths are 0.15 μm to ensure that the source/drain width would be narrower than the channel width. After the gate region formation, Gate, Source and Drain regions were formed by ion implantation of Phosphorous (Dose = 5 x 10^{15} cm^{-2} at 30 keV) and then activated in nitrogen ambient at 600 °C for 24 h, as shown in Figure 1(c). After the source, drain and gate activation, the 500-nm passivation oxide was deposited by PECVD. Wet etching opened contact holes. A layer of aluminum was then deposited by thermal coater system with a thickness of 500 nm. After metal patterning, an annealing process with forming gas 1 is performed at 400°C for 30 min.



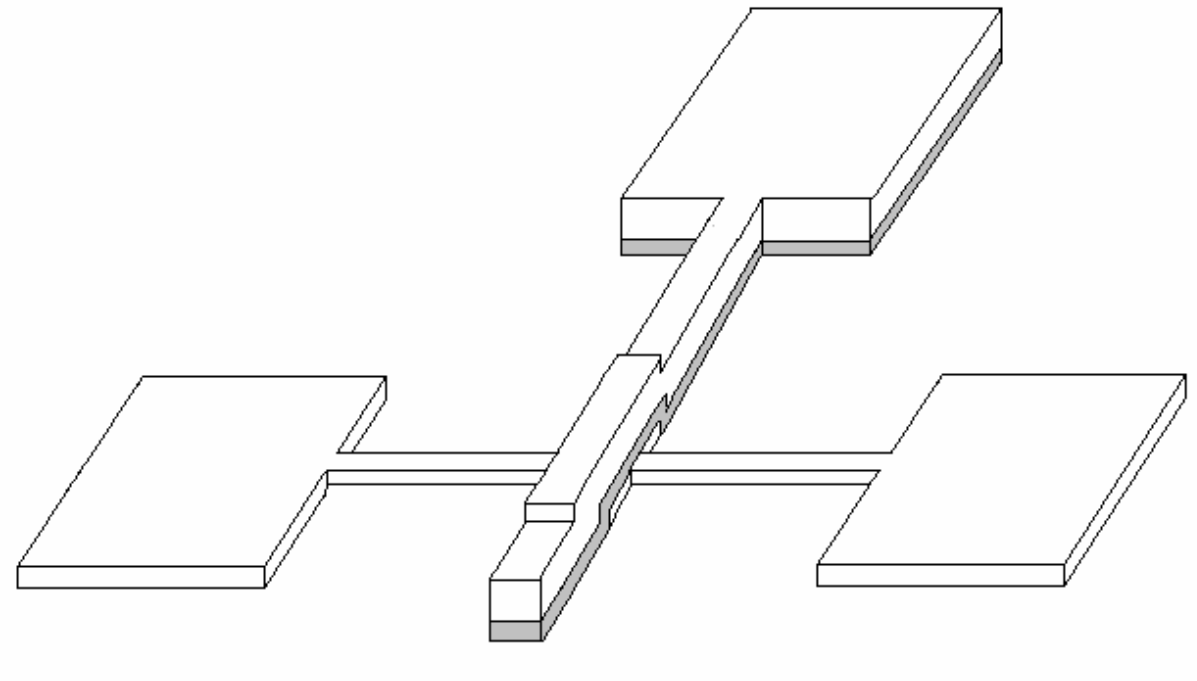
The detailed fabrication process flows are listed as follow：

1. (100) orientation Si wafer
2. Initial cleaning
3. Thermal wet oxidation at 980°C to grow 500nm thermal SiO_2 in furnace
4. 500nm a-Si were deposited by LPCVD at 620°C
5. SPC crystallization for 24 hours
6. pattern # 1: define active regions
7. Poly-Si dry etch by TCP system
8. 50nm TEOS oxide deposition by LPCVD
9. 300nm poly-Si was deposited by LPCVD at 620°C in SiH_4 gas
10. pattern # 2: define poly gate region
11. Poly-Si dry etch by TCP system
12. Ion implantation: P^{31}, 5×10^{15} cm^{-2}, 30 KeV
13. Dopant activation in N_2 ambient at 600°C for 24 hr

14. 400 nm TEOS oxide film was deposited by LPCVD for the passivation
15. pattern # 4: Open contact holes
16. Wet etching by B.O.E
17. 500nm Al thermal evaporation
18. Mask # 4: define metal pad
19. Etching Al and removing photoresist
20. Al sintering at 400°C in N_2 ambient for 30 minutes



(pattern # 1: define active regions)



(pattern # 2: define poly gate region)

In Figure 2.1(c), the channel region is divided into one main channel region (region I)

and two side channel regions (region II). The channel length and width are represented as L_{ch} and W_{ch}, respectively. The channel width (W_{ch}) is wider than the source/drain width (W_{sd}), and the channel width can be written as

$$W_{ch} = W_{mc} + 2W_{sc} = W_{sd} + 2W_{sc} \quad (1)$$

where W_{sc} is the width of the side channel region (Figure 1(c)) in the test structure and W_{mc} is the main channel width that is equal to source/drain width (W_{sd}).

For comparison, the conventional poly-Si TFT's structure which the channel width is identical to the source/drain width was also fabricated at the same time.

2.3 The Simulation Results

We discussed the simulation results of the Test Structure ($W_{ch} > W_{sd}$) and the Conventional Structure ($W_{ch} = W_{sd}$).In order to simulate the current flows of the test and the conventional structures, the 2-D numerical simulator MEDICI was used [27]. Figure 2.2 shows the simulated current flow lines of the conventional structure in ON-state. The channel length and the channel width of the simulated conventional structure are 10 μm and 5 μm, respectively.

Comparing Figures 2.2(b) with 2.2(c), it can be observed that additional current flow generated in the side channel regions and the current flow line in the side channel regions would be increased with increasing the channel length (L_{ch} = 3 μm to L_{ch} = 10 μm). It indicates that the current flow distribution in the side channel regions would be dependent on the channel length.

Then comparing with Figures 2.2(c) and 2.2(d), even increasing the source /drain width (W_{sd} = 5 μm to W_{sd} = 10 μm), the distribution and the effective distribution width of current flow lines of W_{sd} = 10 μm in region II are almost identical to those of W_{sd} = 5 μm. It indicates that an increase of the source/drain width (or main channel width) would not significantly change the distribution of current flow lines in side channel.

2.4. Equivalent Circuit of the Channel Region in the Test Structure($W_{ch} > W_{sd}$) in the linear region

To explain the additional current flow paths of the test structure in the side channel regions, we used the equivalent circuit as shown in Figure 2.3. In the side channel regions of the Figure 2.3, the resistance of path 2 (R_{sc2}) would be larger than that of path 1 (R_{sc1}) due to

the distance of path 2 is longer than path 1. So, the currents flow via the path 2 must be less than the currents flow via the path 1. According to this equivalent circuit, the total channel resistance (R_{tot}) of the test structure could be written as:

$$R_{tot} = \frac{1}{\frac{1}{R_{mc}} + \frac{2}{R_{sc1}} + \frac{2}{R_{sc2}} + ...} < R_{mc} \qquad (2)$$

and

$$R_{mc} = \frac{L_{ch}}{W_{sd}\mu_{eff}C_{ox}(V_{gs}-V_{th})} \qquad (3)$$

where R_{mc} is the resistance of the main channel region in the linear region, and R_{mc} is also the channel resistance of the conventional structure in the linear region. The total channel resistance (R_{tot}) of the test structure should be smaller than that of the main channel region (R_{mc}). Therefore, the ON-state drain current of the test structure would be higher than that of the conventional structure. As discussed above, the ON-state drain current of the test structure would be saturated at a certain value, if W_{sc} were large enough.

2.5 Electrical Characteristics of the Test Structure (W_{ch} > W_{sd})

In order to confirm our observations on the results of Figures 2.2 and 2.3, the experimental data of the test structure were shown in Figures 2.4 - 2.6.

In Figure 2.4(a), the I_{ds}-V_{gs} transfer characteristics of the test structure with different side channel widths. It can be observed that the on-state drain currents of the test structures are higher than conventional structure. The ON-state drain current of the test structure would be initially increased with increasing the side channel width (W_{sc}), and then gradually independent of W_{sc}, even though the W_{sd} / L_{ch} ratio of the test structure was changed from 10 μm /5 μm to 5 μm /15 μm

In Figure 2.5(a). These results are corresponding with our suggestions in the section 2.3. In the Figures 2.4(b) and 2.5(b), the characteristics of the test structure with different side channel widths were shown. In the Figures 2.4(b) and 2.5(b), the ON-state drain currents of the test structure are larger than those of the conventional structure. It can be observed that increasing Wsc will reduce the channel resistance. According to the results of Figure 2.4, Figure 2.5 and the equation (1), it can be observed that the reason of higher ON-state drain

current of the test structure is lower channel resistance.

Figure 2.6 shows the ON-state drain current distributions of the test structure with the varied side channel width for different channel lengths. Ten test TFTs were measured for each condition. In Figure 2.6, it can be observed that the ON-state drain current of the test structure would be initially increased with increasing W_{sc}, and then gradually be saturated in certain W_{sc}. This special side channel width would be called as the effective side channel width ($W_{sc,eff}$). The higher ON-state drain current would be obtained by increasing channel width (W_{sc}). In Figures 2.4 and 2.5, it can be observed that the value of the effective side channel width ($W_{sc,eff}$) would be decreased with decreasing the channel length. It is consistent with the simulated results of Figure 2.2.

In order to analyze the increased ratio of the ON-state drain current caused by increasing channel width (W_{sc}). The average values of the ON-state drain current gain (A_i) with different channel width (W_{sc}) were shown in Figures 2.7(a) and 2.7(b). The ON-state drain current gain (A_i) is defined as

$$A_i \equiv \frac{I_{ds,t} - I_{ds,c}}{I_{ds,c}} \qquad \textbf{(4)}$$

where $I_{ds,c}$ is the ON-state drain current of the conventional structure; $I_{ds,t}$ is the ON-state drain current of the test structure with different side channel widths.

In Figures 2.7(a) ~2.7(f), it can be observed that the average values of the ON-state drain current gain (A_i) of the test structure would be increased as increasing the channel length. In addition, in the same channel length (such as L_{ch} = 15 μm), the effective side channel widths ($W_{sc,eff}$) of W_{sd} = 5 μm and W_{sd} = 10 μm are almost the same. These results are consistent with the simulated results of Figures 2, and the decrease of the W_{sd} from 10 μm to 5 μm would increase the average value of A_i. From the results of Figures 2.5 and 2.6, we can conclude that the effective side channel width ($W_{sc,eff}$) is dependent on the channel length (L_{ch}) and independent of the source/drain width (W_{sd}), and the effective side channel width ($W_{sc,eff}$) would be not only dependent on the side channel width, but also dependent on the channel length and the source/drain width.

2.6 Relationship of the ON-state drain current Gain with the Channel Length, the Side Channel Width and the Source/Drain Width for long source/drain width (W_{sd} = 5 μm and W_{sd} = 10μm)

To investigate the relationship of the ON-state drain current gain (A_i) with the channel length, the side channel width and the source/drain width, the distributions of the ON-state drain current gain (A_i) against L_{ch} and L_{ch}/W_{sd} ratio with different channel widths and side channel width conditions were shown in Figures 2.8(a)-2.8(b) and Figures 2.9(a)-2.9(b). As shown in Figures 2.8(a) and 2.8(b), it can be observed that the ON state current gains A_i were directly proportional to L_{ch} for both W_{sd} = 5 μm and 10 μm. In Figures 2.9(a) and 2.9(b), it can be also observed that the ON state current gains A_i were directly proportional to the L_{ch}/W_{sd} ratio for both W_{sd} = 5 μm and 10 μm. Therefore, we can conclude that the ON state current gain is directly proportional to L_{ch} and the L_{ch}/W_{sd} ratio, and is dependent on W_{sc}.

In Figures 2.8 and 2.9, the relationship of the ON-state drain current gain (A_i) with the channel length L_{ch} and the source/drain width W_{sd} for long the source/drain width can be written as:

$$A_i \cong B\frac{L_{ch}+C}{W_{sd}} \qquad \textbf{(5)}$$

Where B and C are constants.

When $W_{sc} \geq W_{sc,eff}$, B is about 0.48 according to Figures 2.9 ; and C is about -1.55 in Figures 2.8.

Combining the equations (4) and (5), the maximum ON-state drain current gain ($A_{i,max}$) is obtained:

$$A_{i,max} \equiv \frac{I_{ds,t,max} - I_{ds,c}}{I_{ds,c}} \cong 0.48\left(\frac{L_{ch}-1.55}{W_{sd}}\right) \qquad \textbf{(6)}$$

Because Eq. (6) is derived from the experimental data of, $W_{sc} \geq W_{sc,eff}$., the maximum ON-state drain current of the test structure ($I_{ds,t,max}$) can be written as:

$$I_{ds,t,max} \cong \left[1+0.48\left(\frac{L_{ch}-1.55}{W_{sd}}\right)\right]I_{ds,c} \qquad \textbf{(7)}$$

The experimental data and calculated data were all shown in Figure 2.10. As shown in

Figure 2.10, the calculated data almost agreed with the experimental data for different source/drain widths and different applied drain biases (V_{ds} = 5 V or 10 V).

In Figures 2.8(a) and 2.9(a), W_{sc} is 6 μm which is smaller than the effective side channel width ($W_{sc,eff}$) of the test structure of L_{ch} = 15 μm. $W_{sc,eff}$ of the test structure of L_{ch} = 15 μm is about 10 μm as shown in Figure 2.7. Therefore, the experimental data of (L_{ch} = 15 μm ,W_{sc} =6 μm) can not be fitted by Eq. (5) .

In Figures 2.8(b) and 2.9(b), they were not fitted by Eq. (5), even though W_{sc}(= 14 μm) is larger than $W_{sc,eff}$ (~ 10 μm). The channel resistance is directly proportional to the L_{ch}/W_{sd} ratio. Larger L_{ch}/W_{sd} ratio represents larger channel resistance. The main reason of the experimental data of L_{ch}/W_{sd} = 15 μm/ 5 μm were not fitted by equation(5). In Figures 2.8(b) and 2.9(b) is that larger channel resistance is dominant.

When the channel width is wider than the source/drain width, the side channel would cause the increase of the ON-state drain current due to the additional current flow paths existed in the side channel regions and lower channel resistance. As the side channel width (W_{sc}) increasing, the ON-state drain current would be initially increased and then gradually independent of the side channel width when the side channel width is larger than the effective side channel width ($W_{sc,eff}$). We also found that the ON-state drain current gain would be directly proportional to the channel length and the channel length to source/drain width ratio, and dependent on the side channel width. Moreover, once the channel length to source/drain width ratio is too large, higher channel resistance caused by larger channel length to source/drain width ratio would suppress the effect and limit the increase of the ON-state drain current gain.

2.7 Relationship of the ON-state drain current Gain with the Channel Length, the Side Channel Width and the Source/Drain Width for short source/drain width (W_{sd} = 1 μm and W_{sd} = 2 μm)

In Figures 2.11 and 2.12, the relationship of the ON-state drain current gain (A_i) with the channel length L_{ch} and the source/drain width W_{sd} for short source/drain width can be written as:

$$A_i \cong B\frac{L_{ch}+C}{W_{sd}} \qquad (5)$$

Where B and C are constants.

2.7(a) For W_{sd} = 1 μm

When $W_{sc} \geq W_{sc,eff}$, B is about 0.34 according to the slopes of the auxiliary straight lines in Figures 2.11(a) and 2.11(b); and C is about zero in Figures 2.12(a) and 2.12(b).

Combining the equations (4) and (5), the maximum ON-state drain current gain ($A_{i,max}$) is obtained:

$$A_{i,max} \equiv \frac{I_{ds,t,max} - I_{ds,c}}{I_{ds,c}} \cong 0.34\left(\frac{L_{ch}}{W_{sd}}\right) \qquad \textbf{(8)}$$

In the case of $W_{sc} \geq W_{sc.eff}$, if the channel length and the source/drain width are determined, the saturated or maximum ON-state drain current of the test structure ($I_{ds,t,max}$) can be written as:

$$I_{ds,t,max} \cong [1 + 0.34\left(\frac{L_{ch}}{W_{sd}}\right)]I_{ds,c} \qquad \textbf{(9)}$$

In Figure 2.13 presents experimental data and calculated data. The calculated data roughly agreed with experimental data for different source/drain widths and different applied drain biases (V_{ds} = 5 V or 10 V) (Fig. 2.13).

2.7(b) For W_{sd} = 2 μm

When $W_{sc} \geq W_{sc,eff}$, B is about 0.42 according to the slopes of the auxiliary straight lines in Figures 2.11(a) and 2.11(b); and C is about zero in Figures 2.12(a) and 2.12(b).

Combining the equations (2) and (3), the maximum ON-state drain current gain ($A_{i,max}$) is obtained:

For W_{sd} = 2 μm

$$A_{i,max} \equiv \frac{I_{ds,t,max} - I_{ds,c}}{I_{ds,c}} \cong 0.42\left(\frac{L_{ch}}{W_{sd}}\right) \qquad \textbf{(10)}$$

In the case of $W_{sc} \geq W_{sc.eff}$, if the channel length and the source/drain width are

determined, the saturated or maximum ON-state drain current of the test structure ($I_{ds,t,max}$) can be written as:

For W_{sd} = 2 μm

$$I_{ds,t,max} \cong [1 + 0.42(\frac{L_{ch}}{W_{sd}})]I_{ds,c} \qquad \textbf{(11)}$$

In Figure 2.13 presents experimental data and calculated data. The calculated data roughly agreed with experimental data for different source/drain widths and different applied drain biases (V_{ds} = 5 V or 10 V) (Fig. 2.13).

2.8 Conclusion

In this chapter, we discussed the ON-state drain current of a structure with wide channel width and narrow source/drain width. We found that the On-state drain current of this special structure would be larger than which of the conventional structure (the channel width is identical to the source/drain width), due to the additional current flow paths and low channel resistance. We also found that, the ON-state drain current of this special structure would be dependent on not only the channel length and the source/drain width, but also the side channel width. Moreover, a simple relationship of the ON-state drain current between the source/drain width and the channel length were also provided. These results might help people to further understand the carrier transport mechanism in ON-state when the channel width is larger than the source/drain width.

Chapter 3

Effect of channel width widening on a poly-Si TFT structure with a half side channel region in the linear region

3.1 abstract

In the chapter, in order to analyze the effect of channel width widening on a poly-Si TFT structure with a half side channel region in the linear region. We want to discuss the ON-state drain current of a special TFT structure with a half side channel region in the linear region. It also reported that a higher ON-state drain current would be obtained due to lower series resistance and additional current flow paths existing in the half side channel region. The ON-state drain current of the special TFT structure with a half side channel region will has been increased due to the additional current flow paths existed in the half side channel region and lower channel resistance. We want to compare with the results of chapter#2 and try to analyze the increased ratio of the ON-state drain current caused by increasing channel width. We want to discuss the relationship of ON-state drain current gain (A_i) with effect of channel width widening on a poly-Si TFT structure with a half side channel region in the linear region.

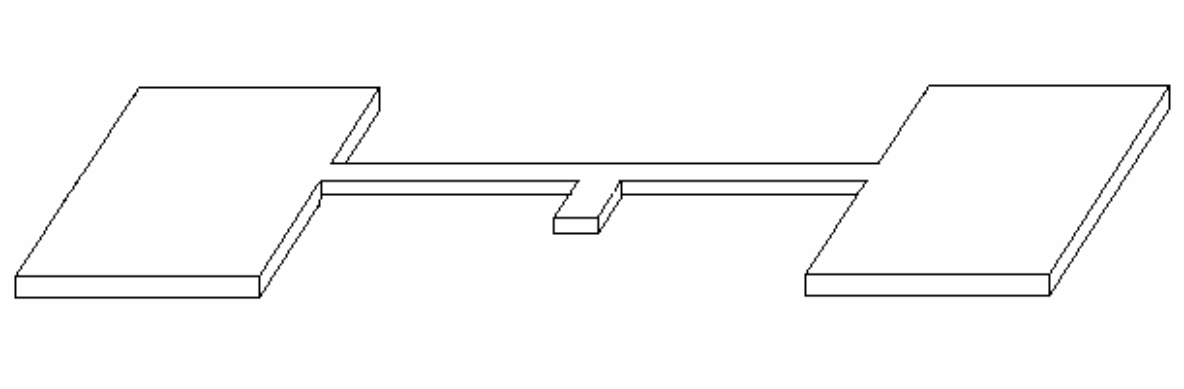
3.2 Device fabrication

The fabrication processes of the tested n-channel poly-Si TFT with a wider channel width and a narrower source/drain width were as follows: A 50-nm thick α-Si layer for active region was deposited by low pressure chemical vapor deposition (LPCVD) system using SiH_4 at 550°C on 500-nm thermal oxidized silicon wafers, then 600°C 24 hr anneal (SPC). The active region was patterned by G-line stepper and was formed using reactive ion etching (RIE), as shown in pattern#1. A 50-nm low pressure chemical vapor deposition (LPCVD) TEOS gate oxide layer was deposited, and then a 300-nm LPCVD poly was deposited which was patterned by G-line stepper and was formed using reactive ion etching (RIE). G-line stepper system has a layer-to-layer misalignment which is less than 0.15 μm, the gate region, as shown in pattern#2, having two overlapping regions which lengths are 0.15 μm to ensure that the source/drain width

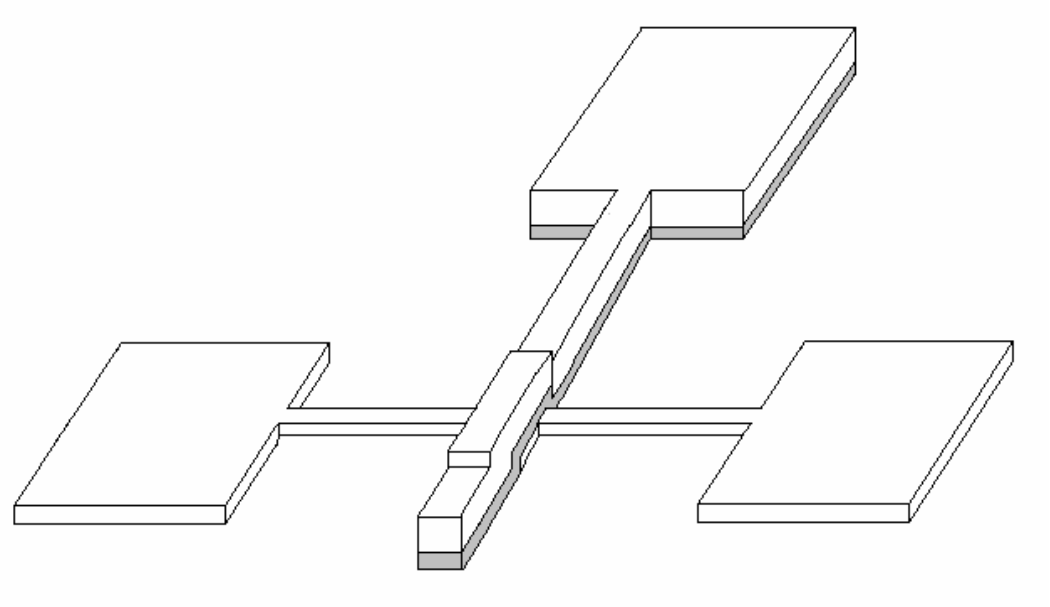
would be narrower than the channel width. After the gate region formation, Gate, Source and Drain regions were formed by ion implantation of Phosphorous (Dose = 5 x 10^{15} cm^{-2} at 30 keV) and then activated in nitrogen ambient at 600 °C for 24 h, as shown in Figure 1(c). After the source, drain and gate activation, the 500-nm passivation oxide was deposited by PECVD. Contact holes were opened by wet etching . A layer of aluminum was then deposited by thermal coater system with a thickness of 500 nm. After metal patterning, an annealing process with forming gas l is performed at 400°C for 30 min.

The detailed fabrication process flows are listed as follow：

1. (100) orientation Si wafer
2. Initial cleaning
3. Thermal wet oxidation at 980°C to grow 500nm thermal SiO_2 in furnace
4. 500nm a-Si were deposited by LPCVD at 620°C
5. SPC crystallization for 24 hours
6. pattern#1: define active regions
7. Poly-Si dry etch by TCP system
8. 50nm TEOS oxide deposition by LPCVD
9. 300nm poly-Si was deposited by LPCVD at 620°C in SiH_4 gas
10. pattern#2: define poly gate region
12. Poly-Si dry etch by TCP system
12. Ion implantation: P^{31}, 5×10^{15} cm^{-2}, 30 KeV
13. Dopant activation in N_2 ambient at 600°C for 24 hr
14 400 nm TEOS oxide film was deposited by LPCVD for the passivation
15 pattern#4: Open contact holes
16 Wet etching by B.O.E
17. 500nm Al thermal evaporation
18. Mask#4: define metal pad
19. Etching Al and removing photoresist
20. Al sintering at 400°C in N_2 ambient for 30 minutes



(pattern#1: define active regions)



(pattern#2: define poly gate region)

3.3 Electrical Characteristics of the Test Structure

Figure 3.2 shows the ON-state drain current distributions of the test structure with a half side channel region with the varied side channel width for different channel lengths. Ten test TFTs were measured for each condition. In Figure 3.2, it can be observed that, for the structure 2, the ON-state drain current is still initially increased with increasing W_{sc}, and then gradually independent of W_{sc}. Moreover, it also can be observed that the value of the effective side channel width ($W_{sc,eff}$) would be decreased with decreasing the channel length.

Figure 3.3 shows the average values of the ON-state drain current gain (A_i) of the structure 2 with different channel width (W_{sc}).

For short source/drain width (W_{sd} = 2 μm), comparing with the experimental results of Figure 3.3(a) and Figure 2.7(c), the ON-state current gain of the structure 2 is smaller than that of the structure 1. It can be observed that the ON-state current gains of the structure 2 for each condition are almost smaller than half of the ON-state current gain of structure 1. A small ON-state current gain is still obtained for the case of the long source/drain width (W_{sd} = 5 μm).

According to Eq (2) of the chapter 2, when the side channel resistance of the structure 2 is twice larger than that of the structure 1, the total channel resistance of the structure 2 does not become twice larger than that of the structure 1. Therefore, the ON-state current of the structure 2 is not half of that of the structure 1.

For the case of short source/drain width (W_{sd} = 2 μm), comparing with the experimental results of Figure 2.12(b) and Figure 3.4, the slopes of the auxiliary straight lines in the Figures 2.12(b) are larger than the slopes of the auxiliary straight lines in the Figures 3.4. The slope of Figure 2.12(b) for source/drain width (W_{sd} = 2 μm) is 0.42. The slope of Figure 3.4 for source/drain width (W_{sd} = 2 μm) is 0.24. Because the side channel resistance of the structure 2 is twice larger than that of the structure 1, the total channel resistance of structure 1 is smaller than that of structure 2.

For the case of short source/drain width (W_{sd} = 5 μm), comparing with the experimental results of Figure 2.9(b) and Figure 3.4, the slopes of the auxiliary straight lines in the Figures 2.9(b) are larger than the slopes of the auxiliary straight lines in the Figures 3.4. The slope of Figure 2.9(b) for source/drain width (W_{sd} = 2 μm) is 0.48. The slope of Figure 3.4 for source/drain width (W_{sd} = 2 μm) is 0.30. Because the side channel resistance of the structure 2 is twice larger than that of the structure 1, the total channel resistance of structure 1 is smaller than that of structure 2.

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Figure Captions

Figure 2.1, Schematic top view of the major fabrication steps of the test TFT's.

Figure 2.2, Current flow lines simulated by MEDICI in

(a) the conventional structure with L_{ch} = 1 0 μm and W_{ch} = W_{sd} = 5 μm;

(b) the test structure with L_{ch} = 3 μm, W_{sd} = 5 μm and W_{ch} = 30 μm;

(c) the test structure with L_{ch} = 10 μm, W_{sd} = 5 μm and W_{ch} = 30 μm;

(d) the test structure with L_{ch} = 10 μm, W_{sd} = 10 μm and W_{ch} = 30 μm.

Figure 2.3, The equivalent circuit of the channel region of the test structure ($R_{m,c}$ is the main channel resistance; $R_{s,c}$ is the side channel resistance)

Figure 2.4, (a) I_{ds}-V_{gs} transfer characteristics; (b) I_{ds}-V_{ds} output characteristics of the test structure of L_{ch} / W_{sd} = 1 0 μm / 5 μm with different side channel widths (Wsc) compared with the conventional structure.

Figure 2.5, (a) I_{ds}-V_{gs} transfer characteristics;

(b) I_{ds}-V_{ds} output characteristics of the test structure of L_{ch} / W_{sd} = 5 μm / 15 μm with different side channel widths (Wsc) compared with the conventional structure.

Figure 2.6, The distributions of the ON-state drain currents of the test structure with

(a) Wsd = 1 um ,Vds = 5V; Vgs = 30 V

(b) Wsd = 1 um ,Vds = 10V; Vgs = 30 V

(c) Wsd = 2 um ,Vds = 5V; Vgs = 30 V

(d) Wsd = 2 um ,Vds = 10V; Vgs = 30 V

(e) Wsd = 5 um ,Vds = 5V; Vgs = 30 V

(f) Wsd = 10 um ,Vds = 5V; Vgs = 30 V

Figure 2.7, The average values of the ON-state drain current gain A_i of the test structure with

(a) Wsd = 1um, Vds = 5 V, Vgs = 30 V

(b) Wsd = 1um, Vds = 10 V, Vgs = 30 V

(c) Wsd = 2um, Vds = 5 V, Vgs = 30 V

(d) Wsd = 2um, Vds = 10 V, Vgs = 30 V

(e) Wsd = 5um, Vds = 5 V, Vgs = 30 V

(f) Wsd = 10um, Vds = 5 V, Vgs = 30 V

as a function of the side channel width W_{sc}.

Figure 2.8, The distributions of the ON-state drain current gain A_i of the test structure with (a) W_{sc} = 6 μm; (b) W_{sc} = 1 4 μm against with the channel length L_{ch} for W_{sd} = 5 μm and W_{sd} = 10μm.

Figure 2.9, The distributions of the ON-state drain current gain A_i of the test structure with (a) W_{sc} = 6 μm; (b) W_{sc} = 1 4 μm against with the channel length to source/drain width ratio L_{ch}/ W_{sd} for W_{sd} = 5 μm and W_{sd} = 10μm.

Figure 2.10, The experimental and calculated maximum ON-state drain current of the test structure with different source/drain widths and different applied drain biases against with the channel length L_{ch}, in which the solid symbols represented the experimental data and the empty symbols represented the calculated data obtained from the equation (5).

Figure 2.11, The distributions of the ON-state drain current gain A_i of the test structure with

(a) W_{sc} = 6 μm

(b) W_{sc} = 1 4 μm

against with the channel length L_{ch} for W_{sd} = 1 μm and W_{sd} = 2μm.

Figure 2.12, The distributions of the ON-state drain current gain A_i of the test structure with

(a) W_{sc} = 6 μm;

(b) W_{sc} = 1 4 μm against with the channel length to source/drain width ratio L_{ch}/ W_{sd} for W_{sd}=1μm and W_{sd}=2μm.

Figure 2.13, The experimental and calculated maximum ON-state drain current of the test structure with different source/drain widths and different applied drain biases against with the channel length L_{ch}, in which the solid symbols represented the experimental data and the empty symbols represented the calculated data obtained from the equation (7) and equation (9).

Figure 3.1, Schematic top view of the major fabrication steps of the test TFT structure with a half side channel region in the linear region.

Figure 3.2, The distributions of the ON-state drain currents of the test structure with a half side channel region in the linear region.

(a) Wsd = 2 um ,Vds = 5V; Vgs = 30 V

(b) Wsd = 2 um ,Vds = 10V; Vgs = 30 V

(c) Wsd = 5 um ,Vds = 5V; Vgs = 30 V

(d) Wsd = 5 um ,Vds = 10V; Vgs = 30 V

Figure 3.3, The average values of the ON-state drain current gain A_i of the test structure with a half side channel region in the linear region.

(a) Wsd = 2um, Vds = 5 V, Vgs = 30 V

(b) Wsd = 2um, Vds = 10 V, Vgs = 30 V

(c) Wsd = 5um, Vds = 5 V, Vgs = 30 V

(c) Wsd = 5um, Vds = 10 V, Vgs = 30 V

Figure 3.4, The distributions of the ON-state drain current gain A_i of the test structure with a half side channel region in the linear region. W_{sc} = 14 μm against with the channel length to source/drain width ratio L_{ch}/ W_{sd} for W_{sd}=2μm and W_{sd}=5μm.

Figure all

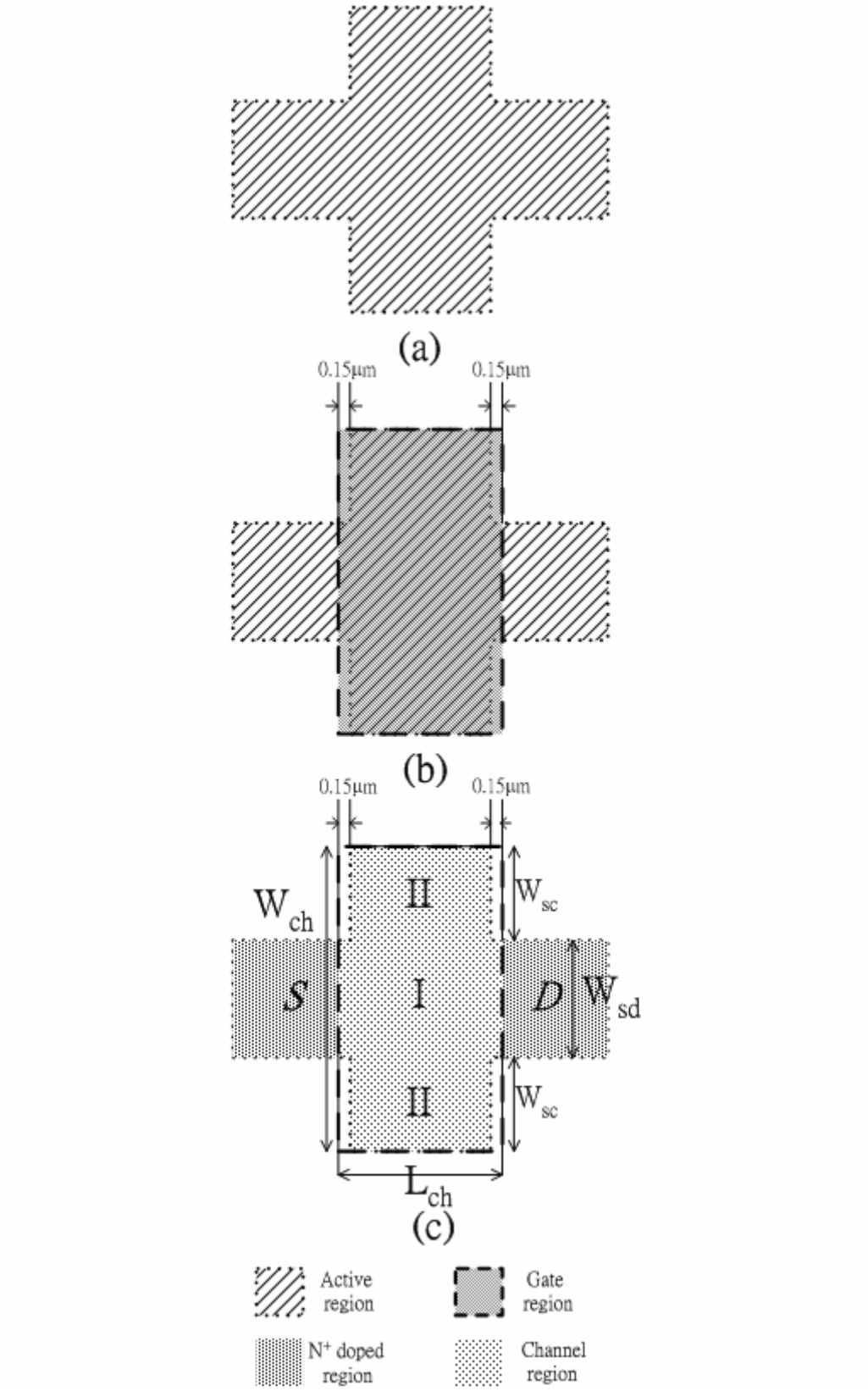
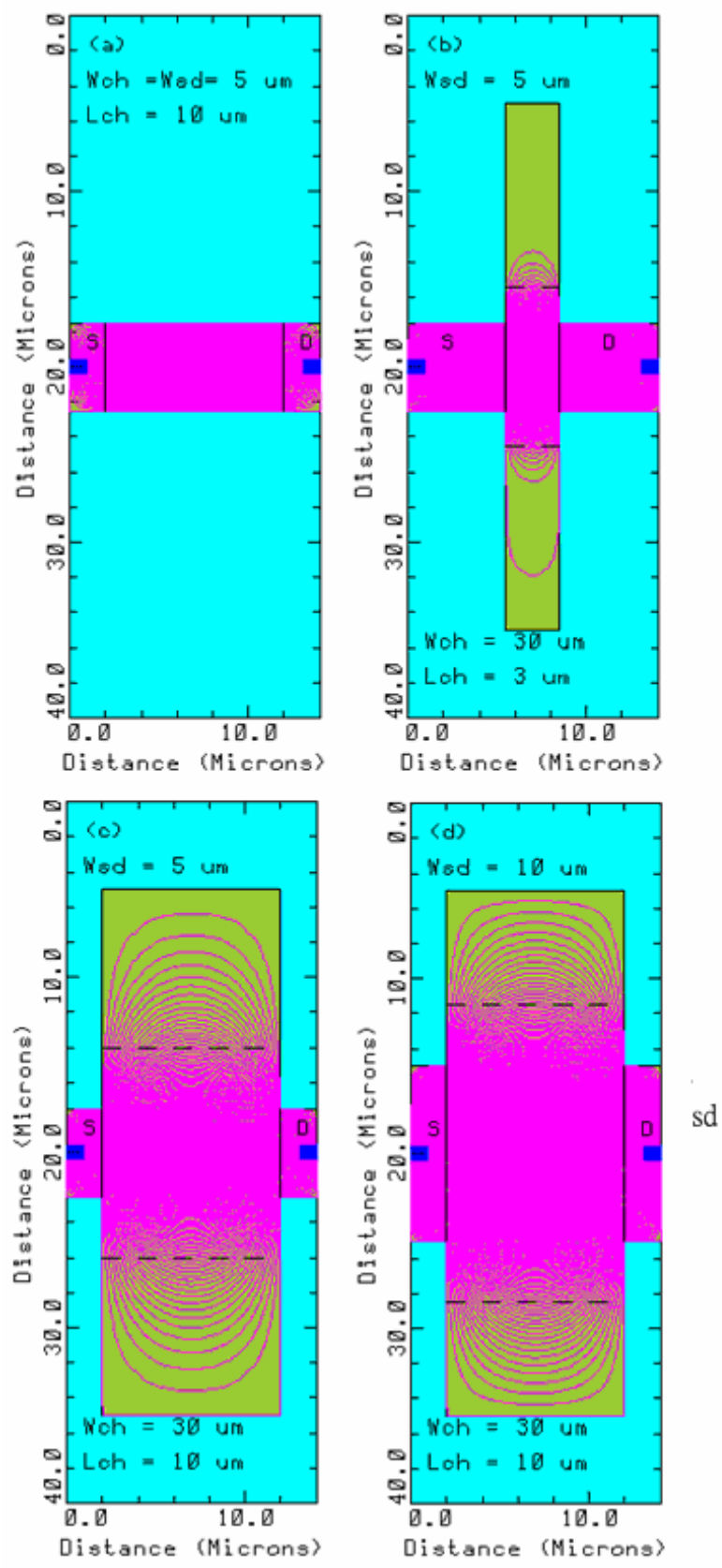


Figure 2.1


(a)
Wch =Wsd= 5 um
Lch = 10 um
(b)
Wsd = 5 um
Wch = 30 um
Lch = 3 um
(c)
Wsd = 5 um
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Lch = 10 um
(d)
Wsd = 10 um
Wch = 30 um
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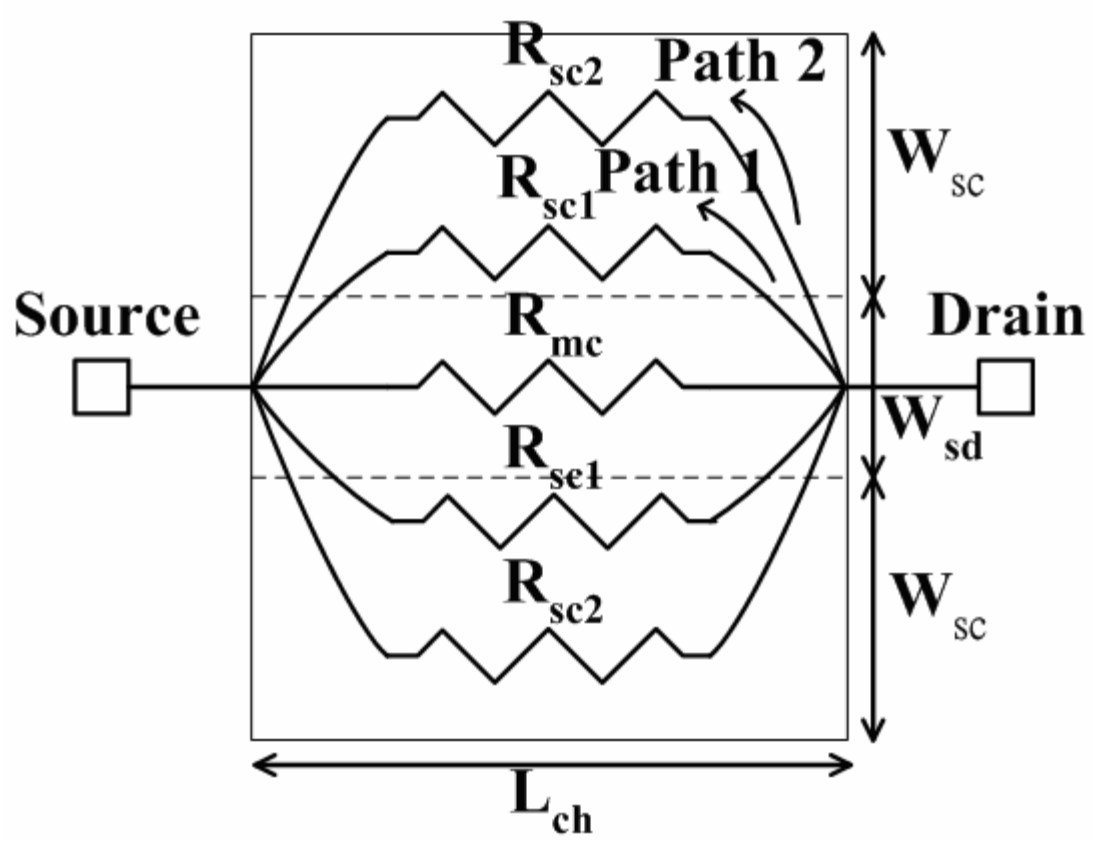
Distance (Microns)
0.0
10.0
20.0
30.0
40.0

sd

Figure 2.2


R sc2
Path 2
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Path 1
W SC
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R mc
Drain
W sd
R se1
R sc2
W SC
L ch

Figure 2.3

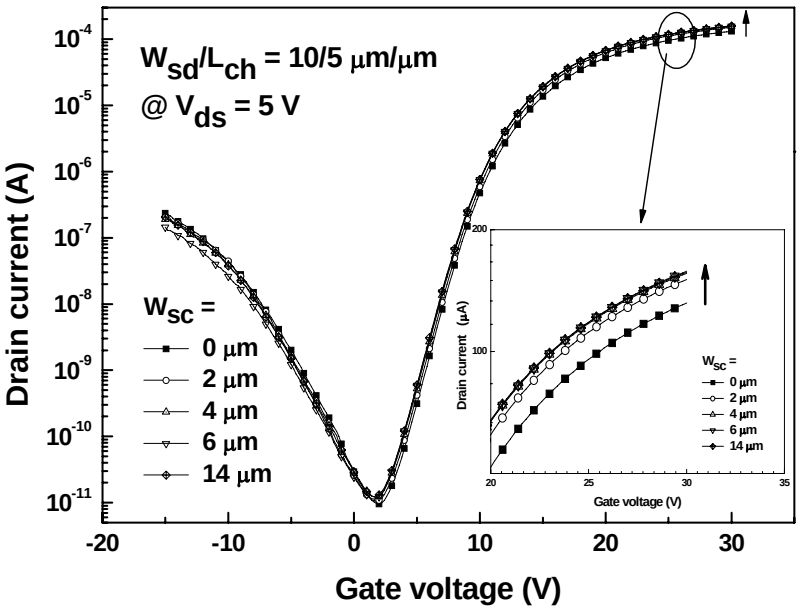

Figure 2.4(a)

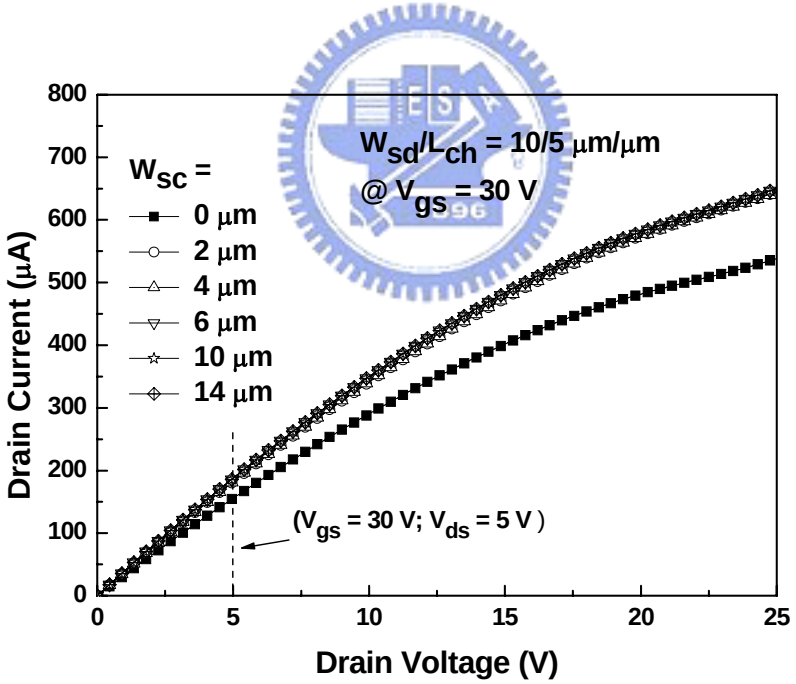

Figure 2.4(b)

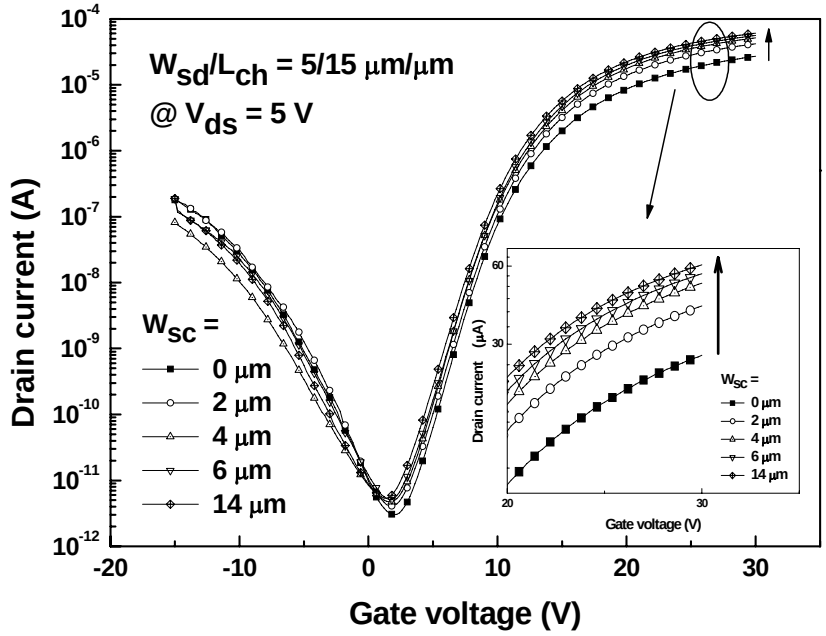

Figure 2.5(a)

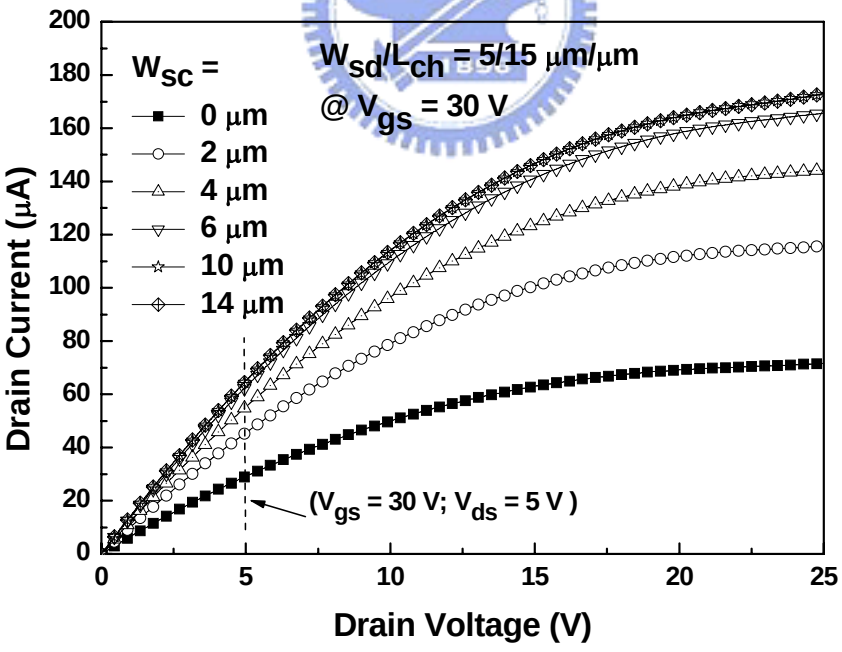

Figure 2.5(b)

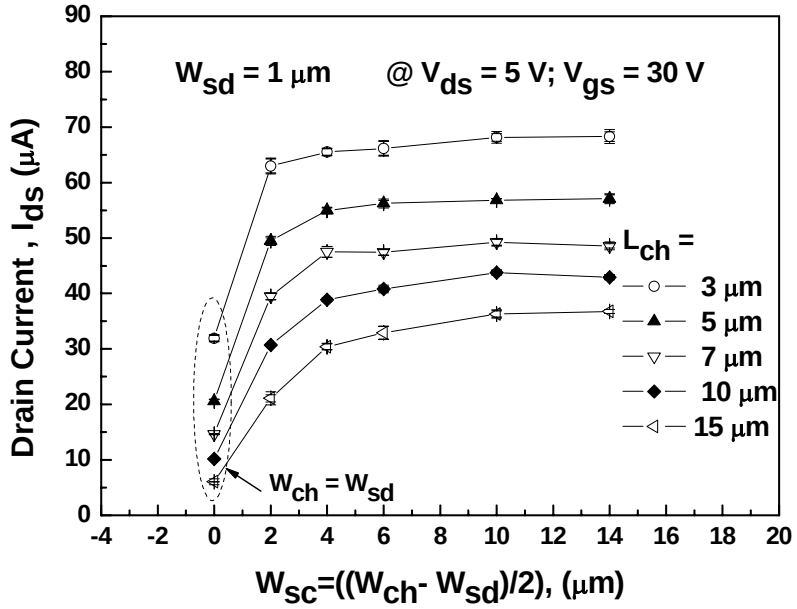

Figure 2.6(a)

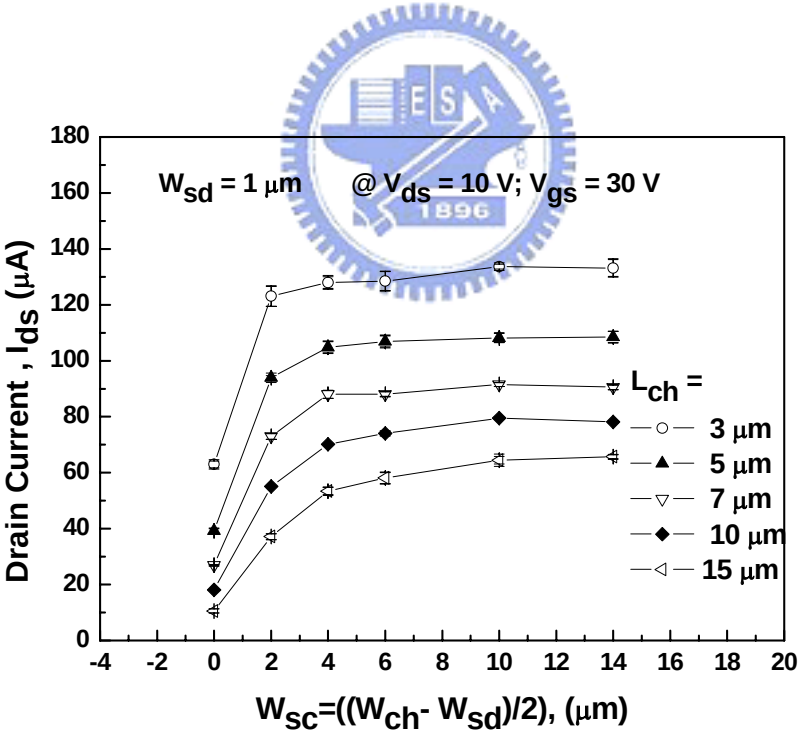

Figure 2.6(b)

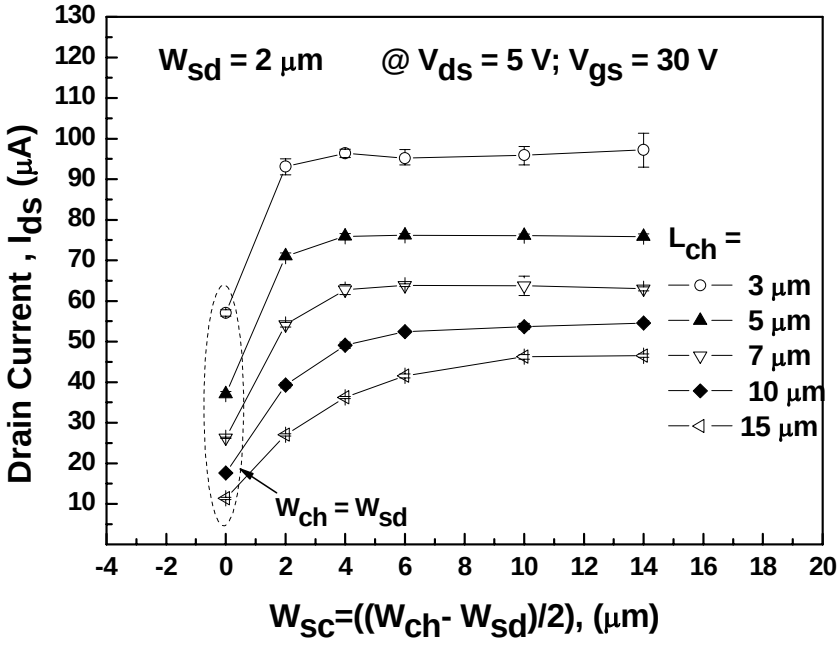

Figure 2.6(c)

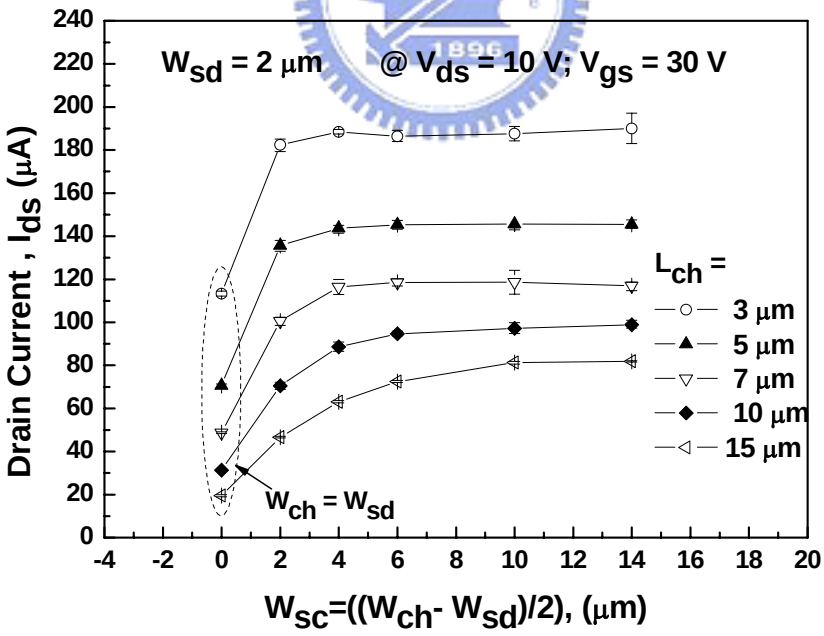

Figure 2.6(d)

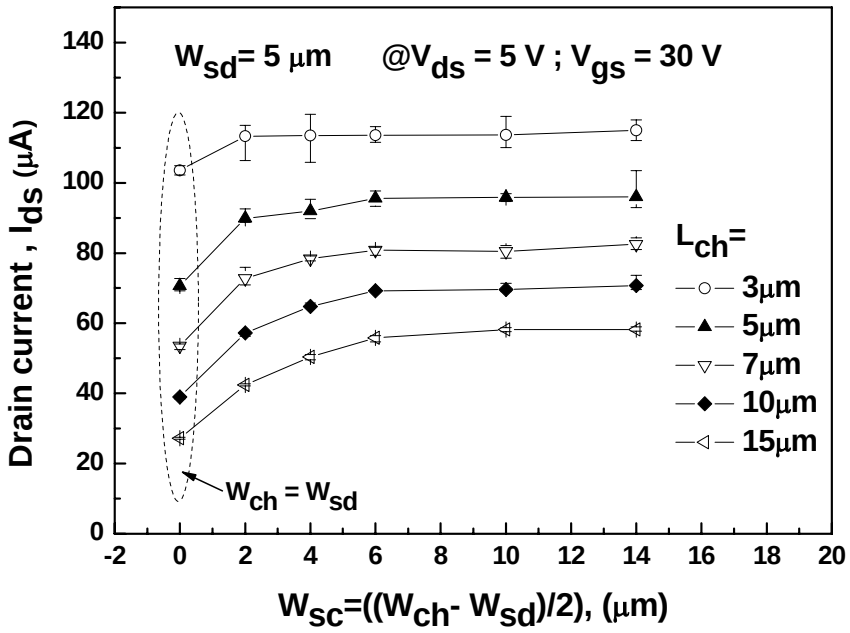

Figure 2.6(e)

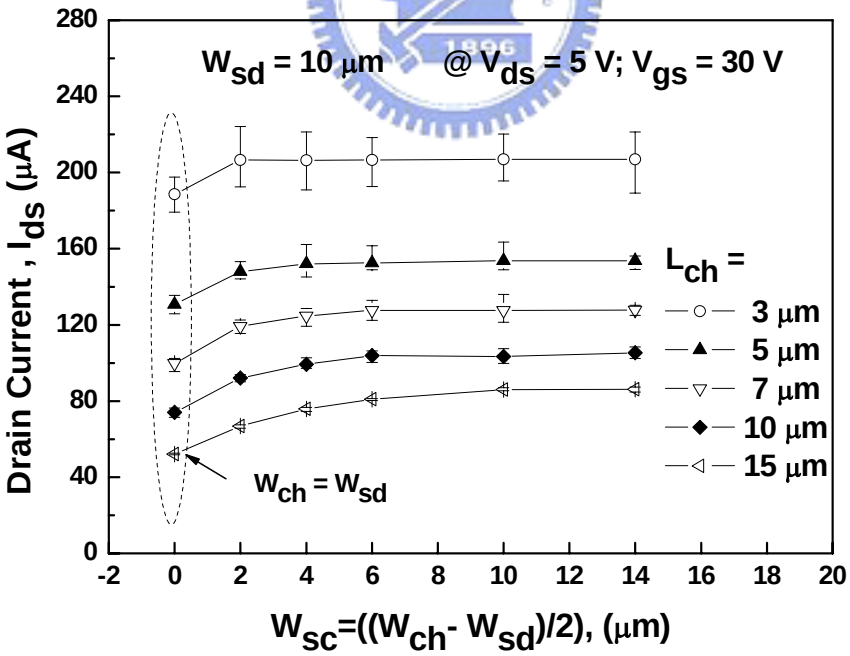

Figure 2.6(f)

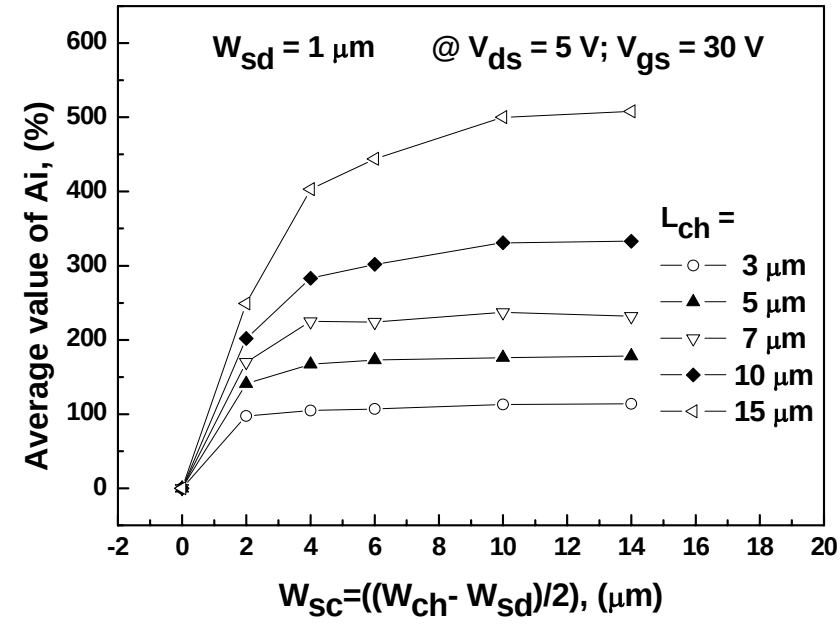

Figure 2.7(a)

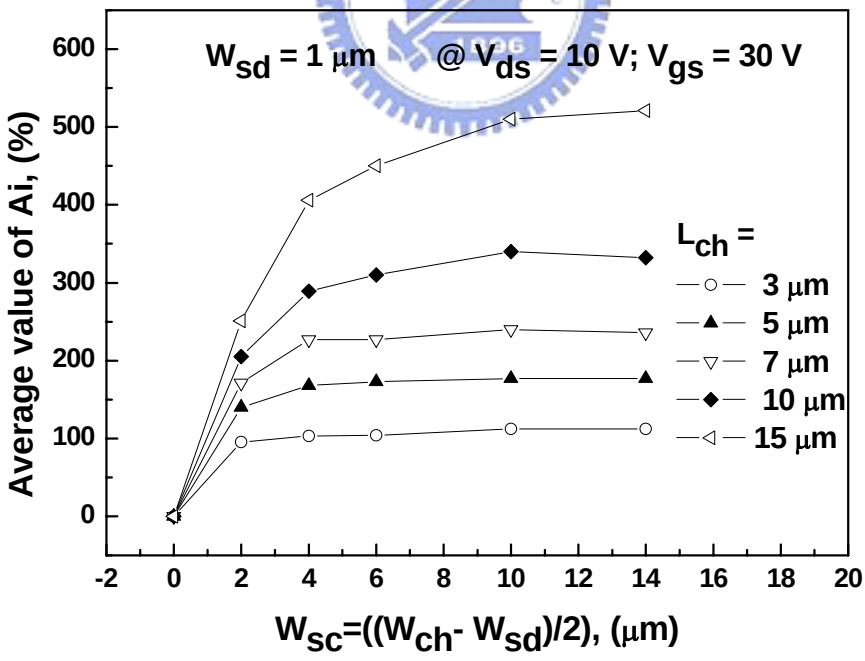

Figure 2.7(b)

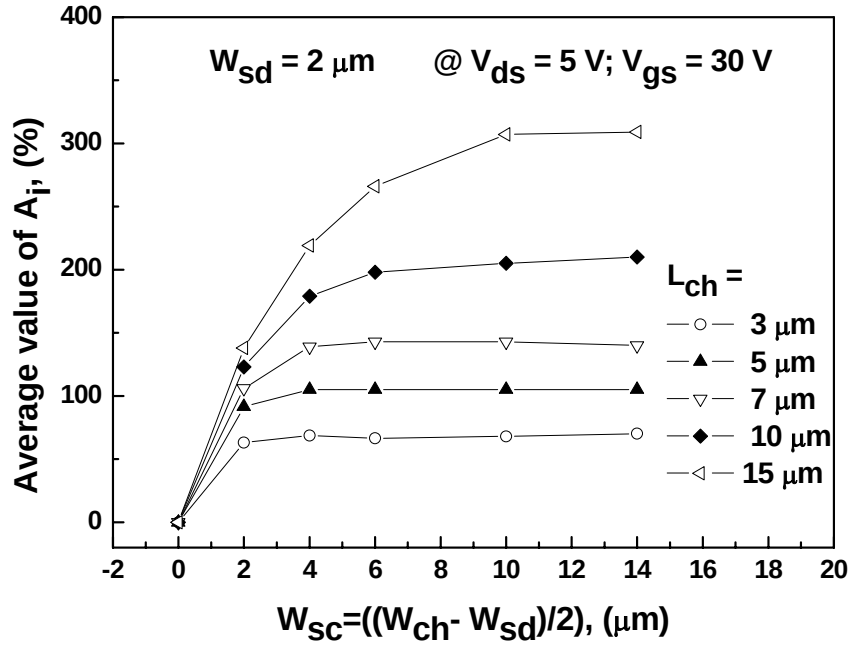

Figure 2.7(c)

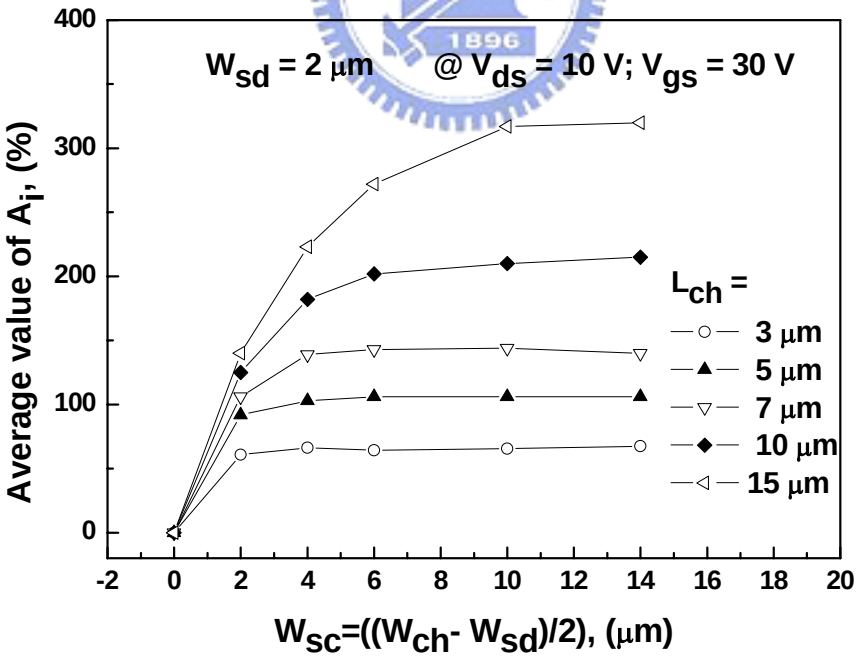

Figure 2.7(d)

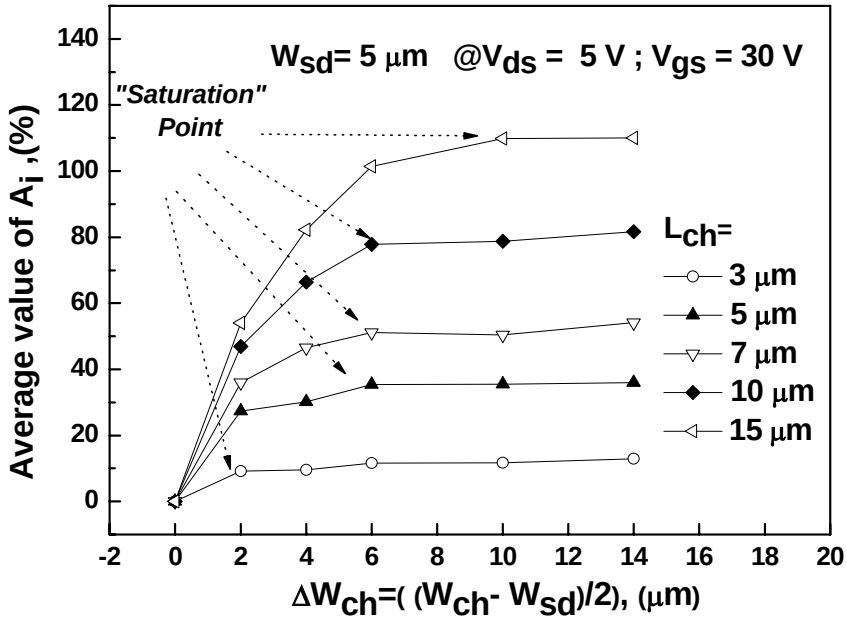

Figure 2.7(e)

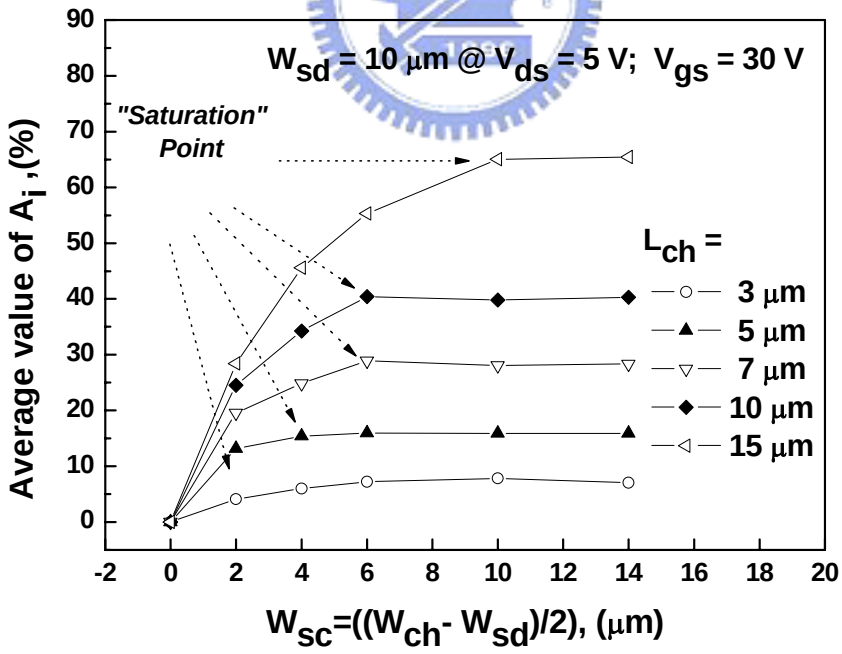

Figure 2.7(f)

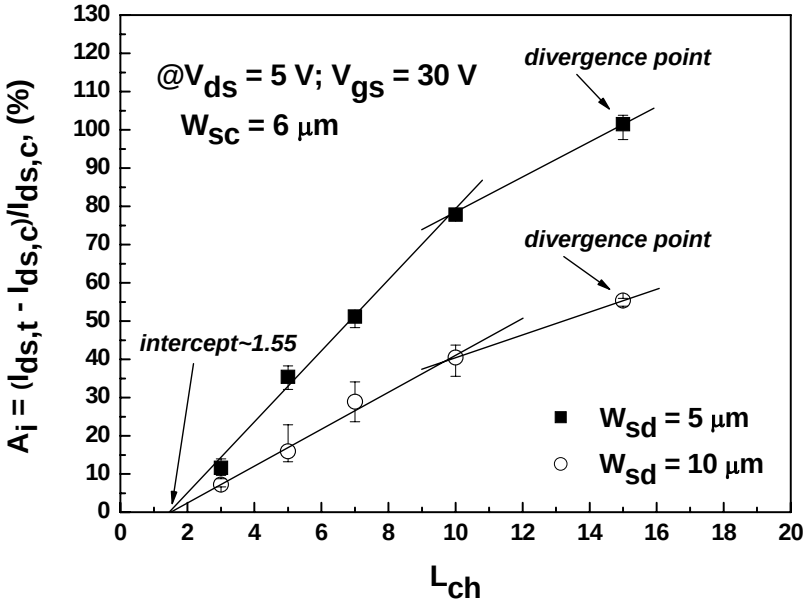

Figure 2.8(a)

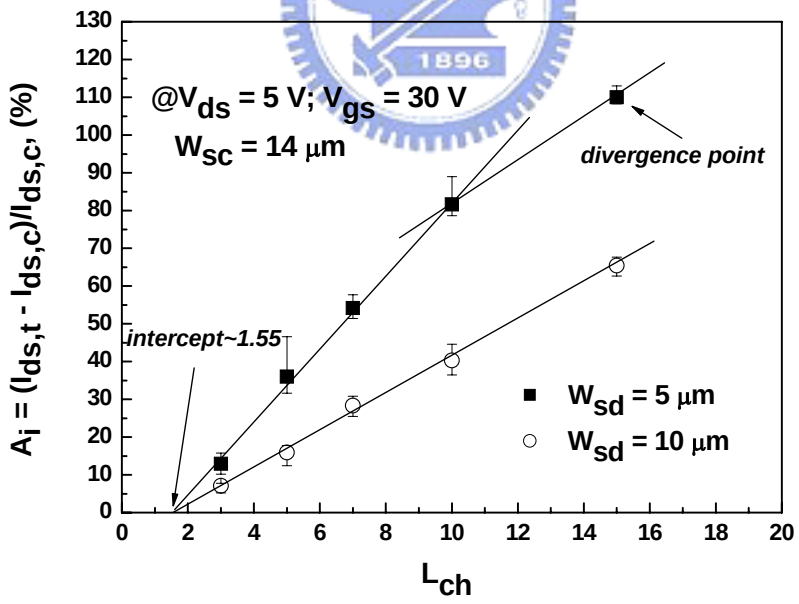

Figure 2.8(b)

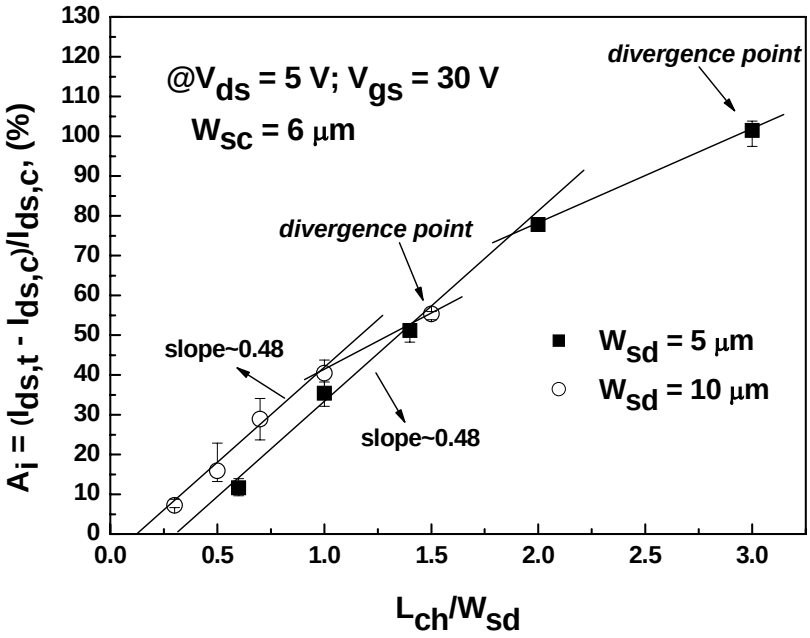

Figure 2.9(a)

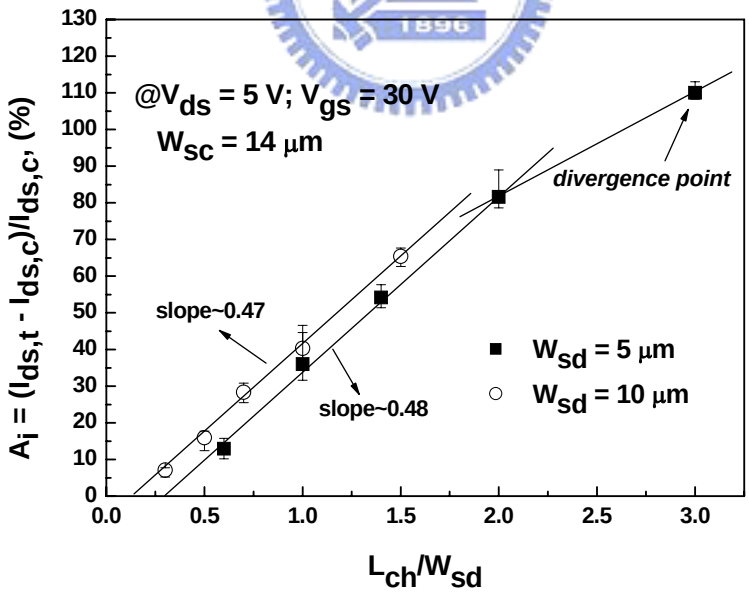

Figure 2.9(b)

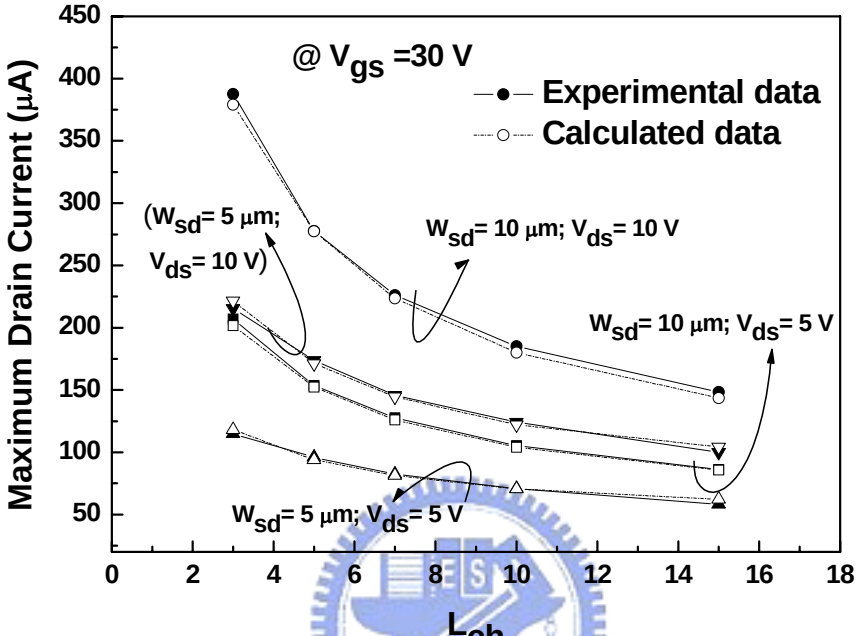
Maximum Drain Current (μA)
450
400
350
300
250
200
150
100
50
0
2
4
6
8
10
12
14
16
18
L_ch
@ V_gs =30 V
Experimental data
Calculated data
(W_sd= 5 μm;
V_ds= 10 V)
W_sd= 10 μm; V_ds= 10 V
W_sd= 10 μm; V_ds= 5 V
W_sd= 5 μm; V_ds= 5 V

Figure 2.10

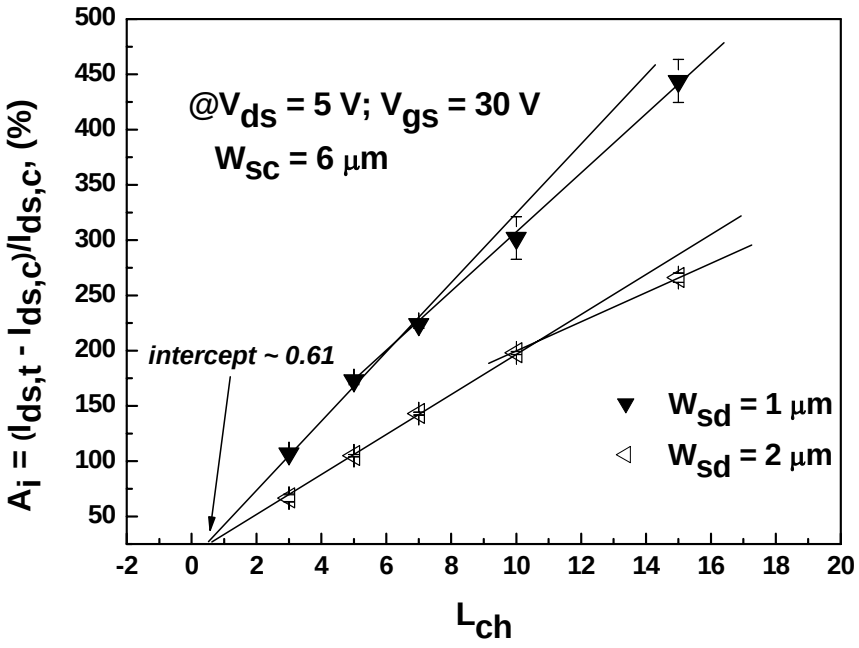

Figure 2.11(a)

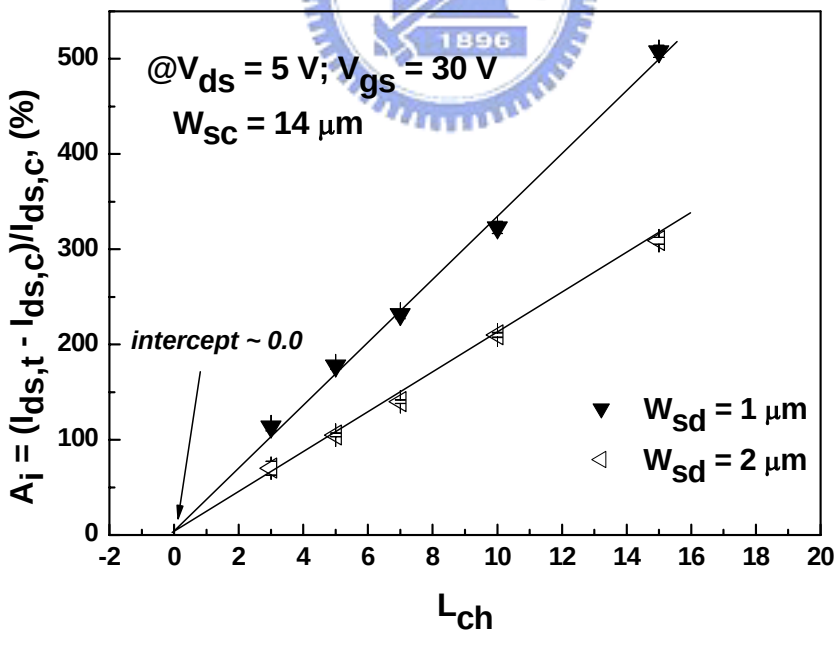

Figure 2.11(b)

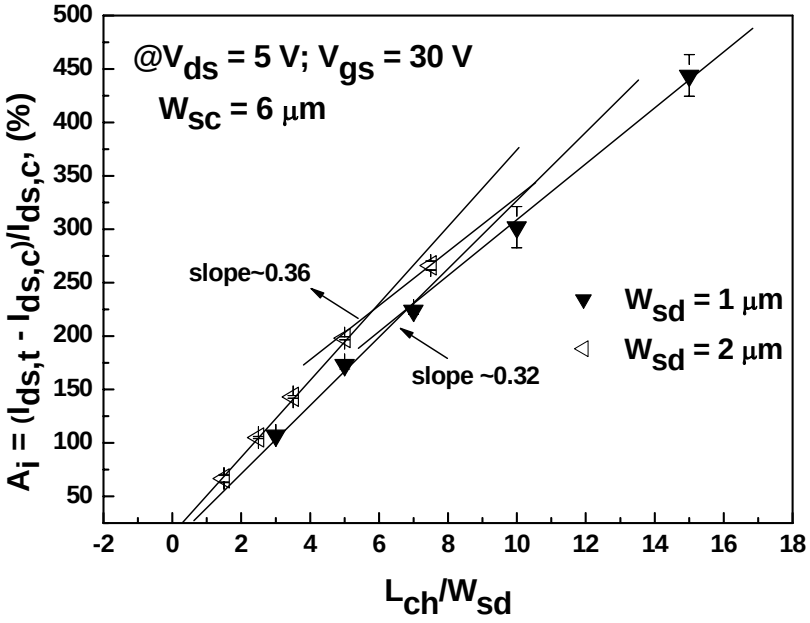

Figure 2.12(a)

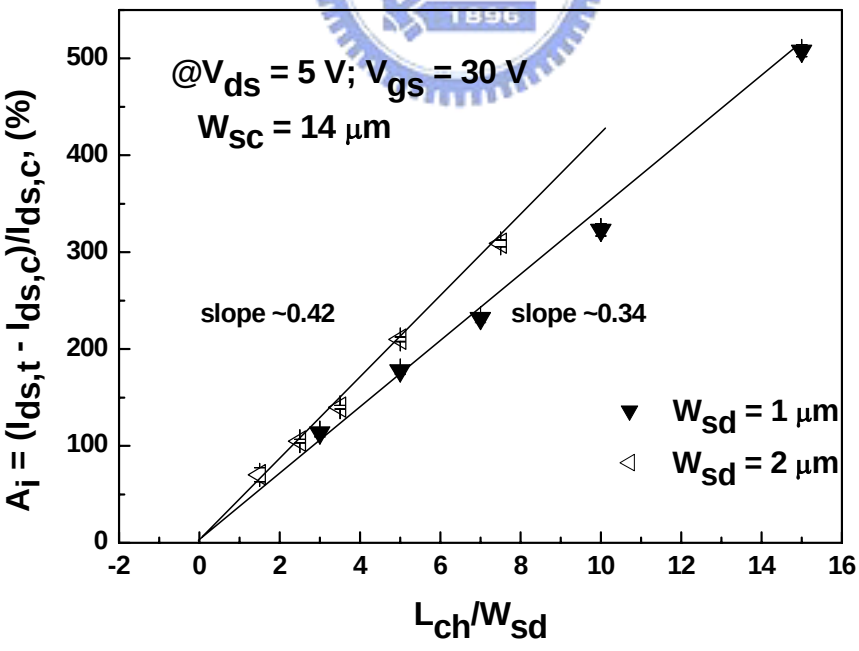

Figure 2.12(b)

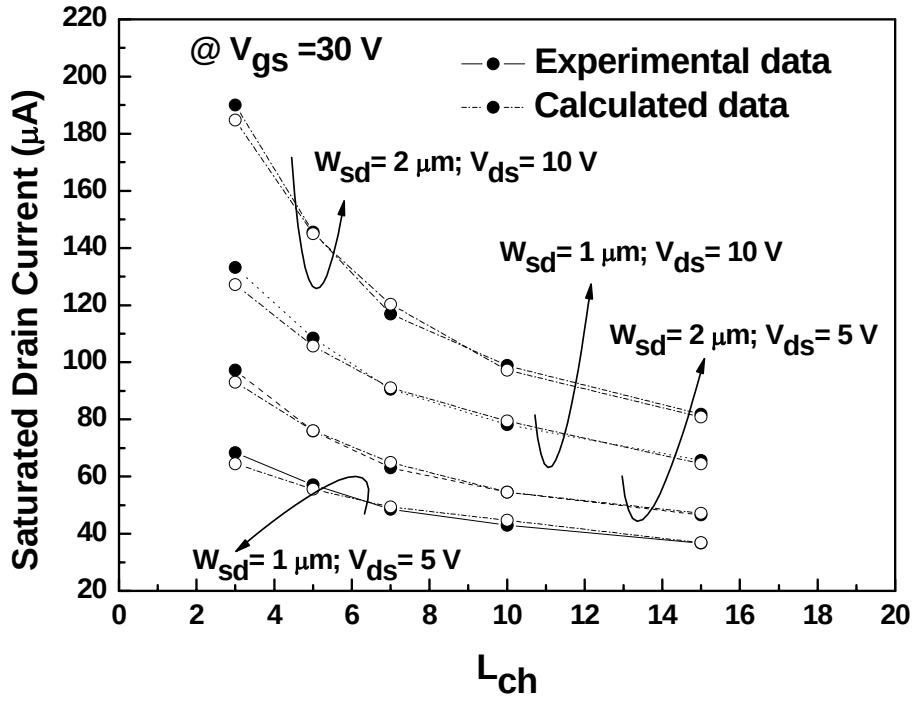
@ V_{gs} =30 V
Experimental data
Calculated data
W_{sd}= 2 μm; V_{ds}= 10 V
W_{sd}= 1 μm; V_{ds}= 10 V
W_{sd}= 2 μm; V_{ds}= 5 V
W_{sd}= 1 μm; V_{ds}= 5 V
Saturated Drain Current (μA)
L_{ch}
220
200
180
160
140
120
100
80
60
40
20
0
2
4
6
8
10
12
14
16
18
20

Figure 2.13

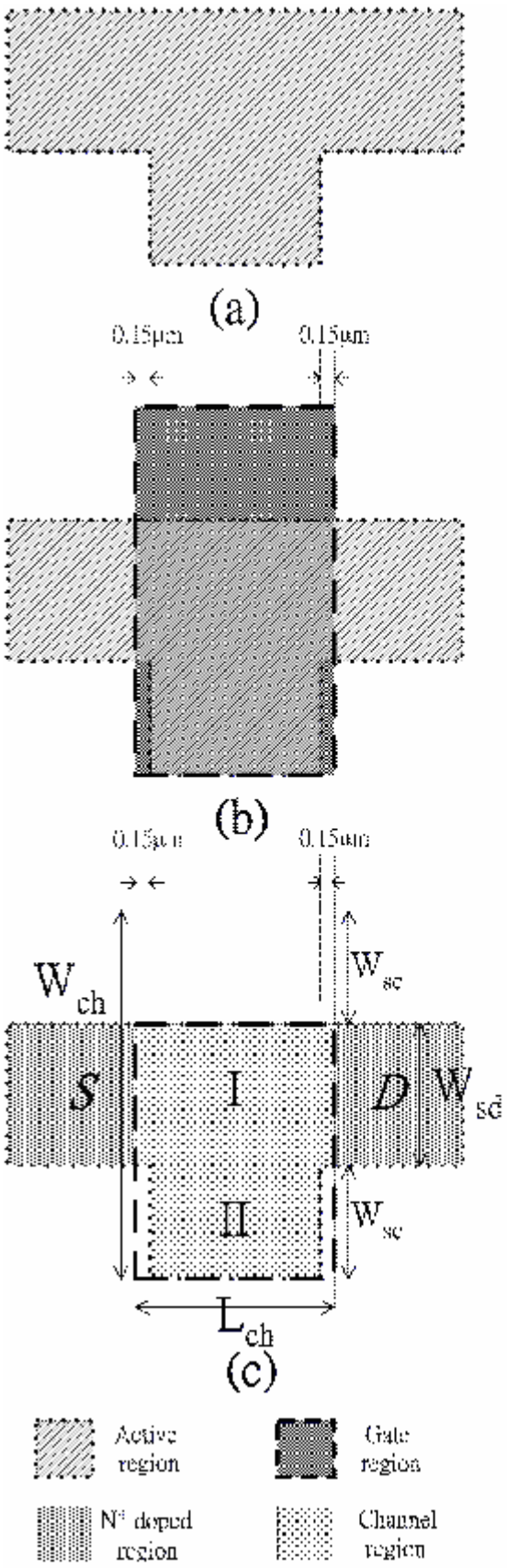
(a)
0.15μm
0.15μm
(b)
0.15μm
0.15μm
W ch
W sc
S
I
D
W sd
II
W sc
L ch
(c)
Active region
Gate region
N+ doped region
Channel region

Figure 3.1

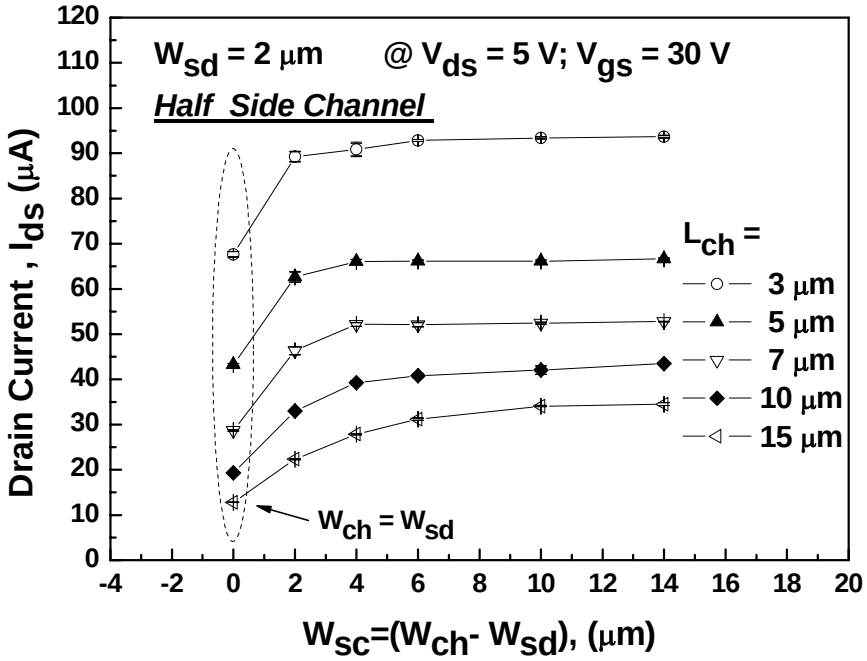

Figure 3.2(a)

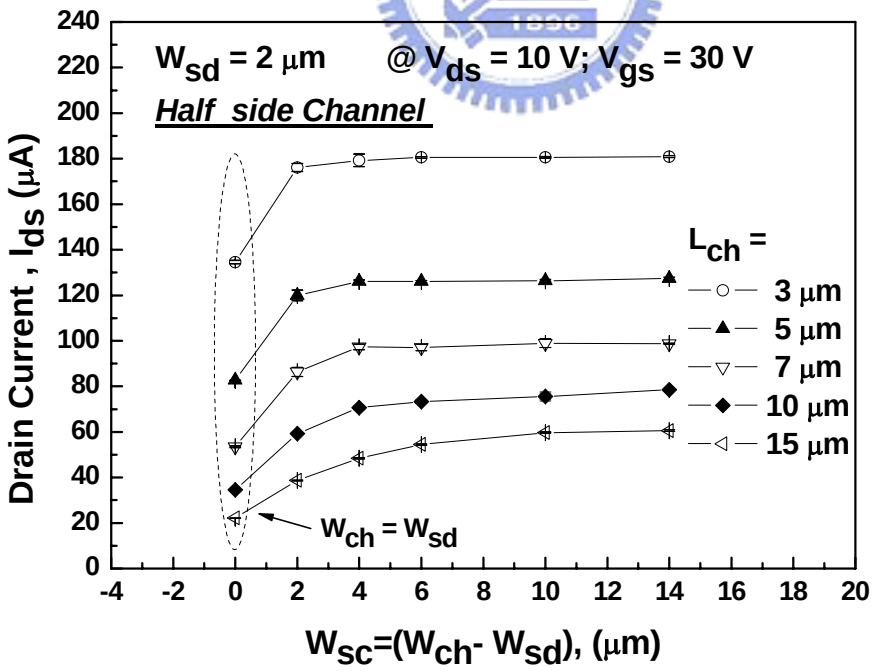

Figure 3.2(b)

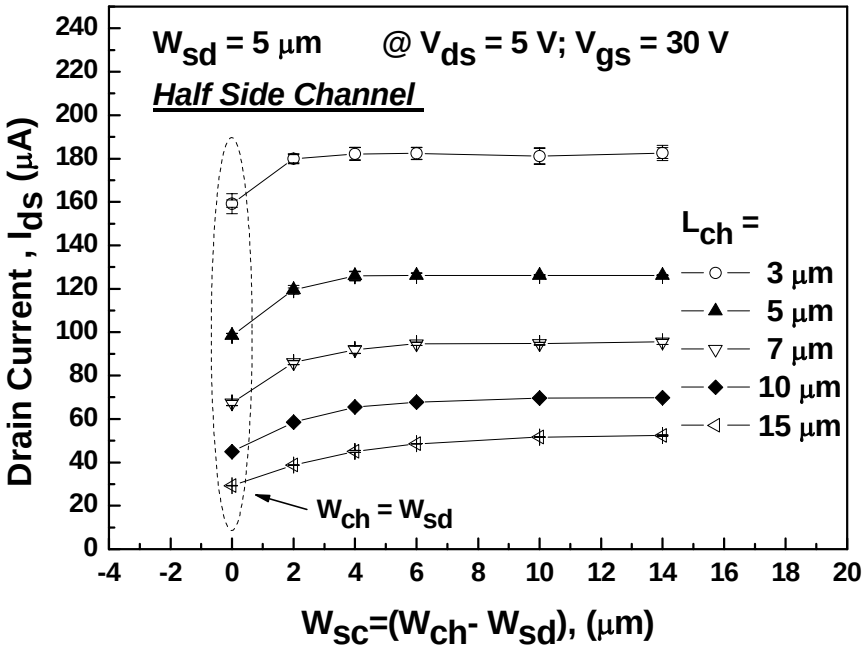

Figure 3.2(c)

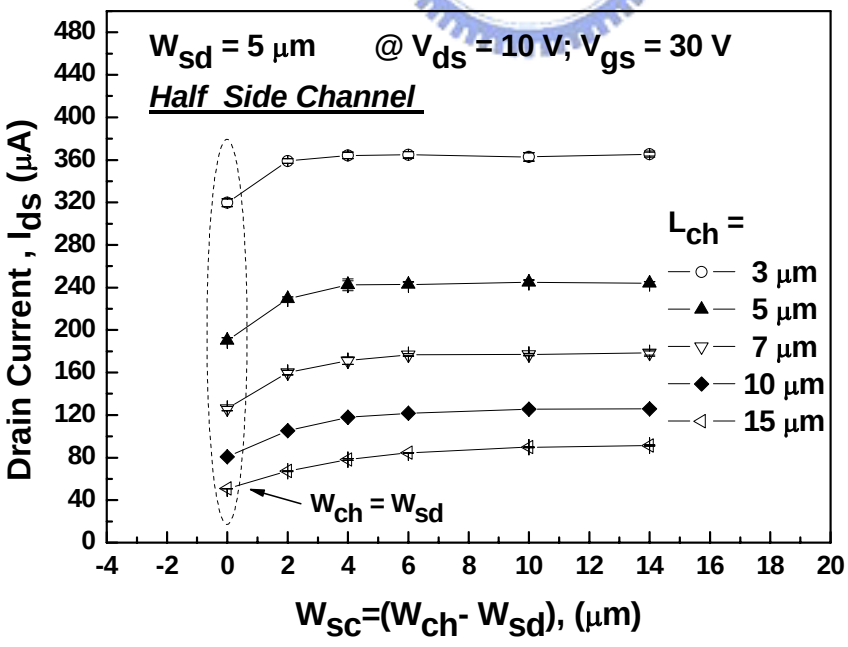

Figure 3.2(d)

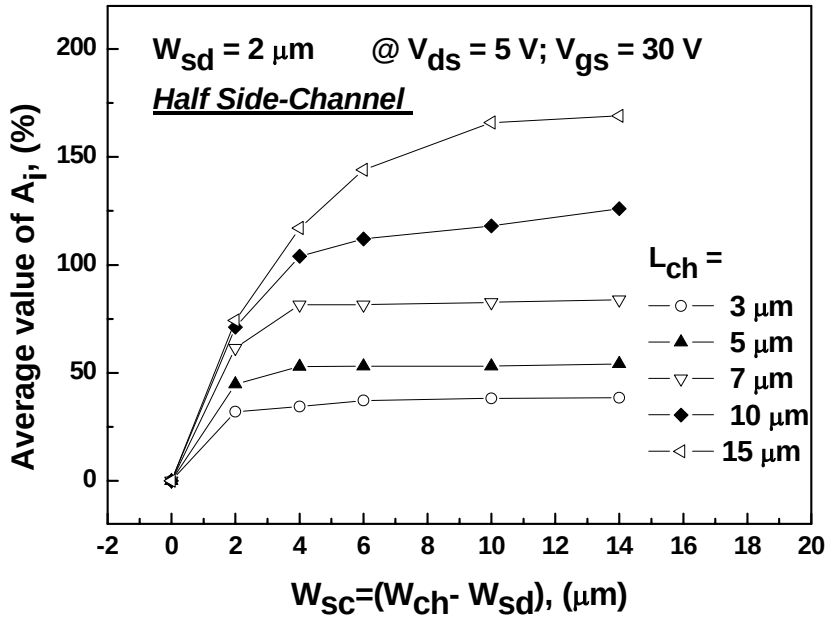

Figure 3.3(a)

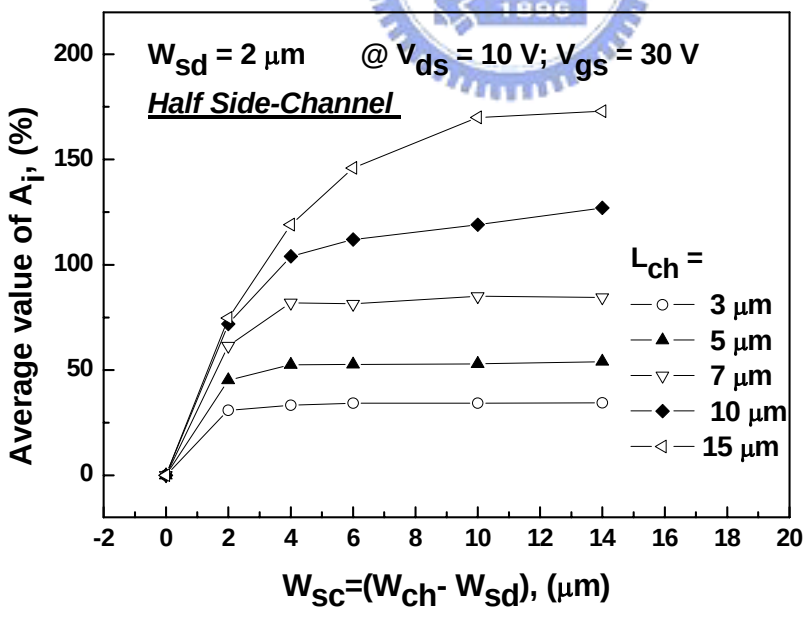

Figure 3.3(b)

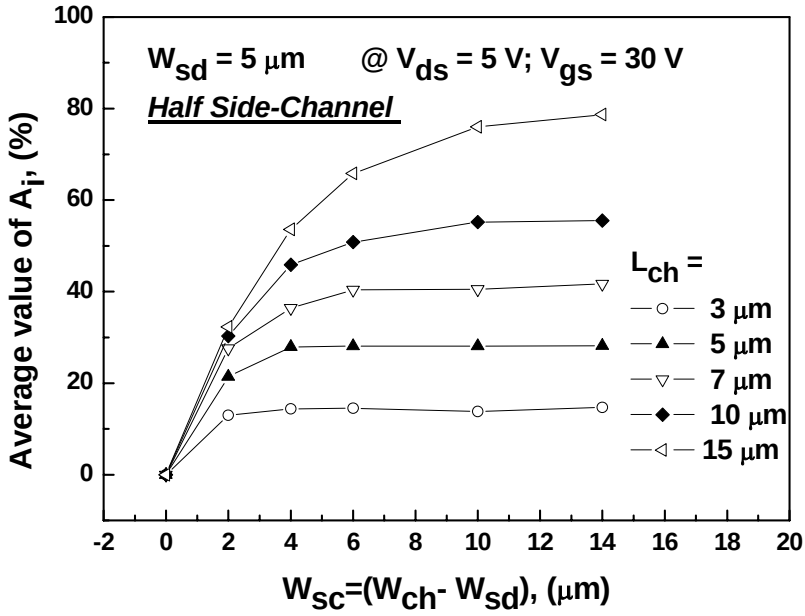

Figure 3.3(c)

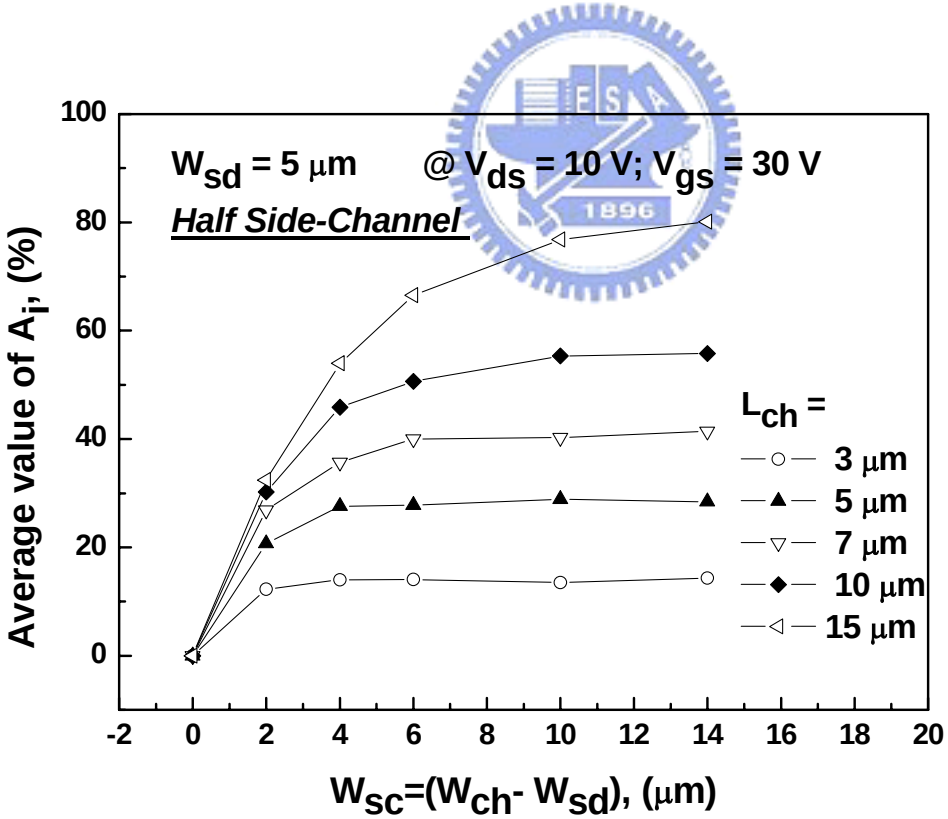

Figure 3.3(d)

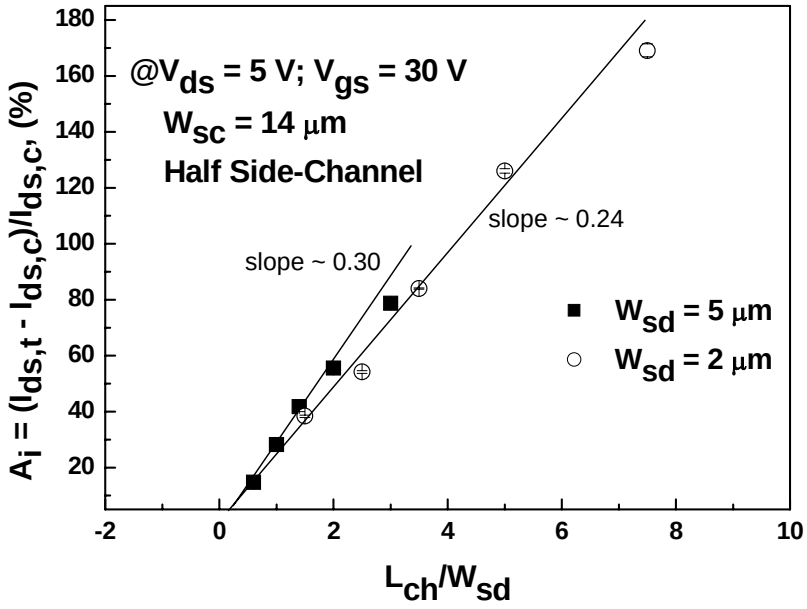
@Vds = 5 V; Vgs = 30 V
Wsc = 14 μm
Half Side-Channel
slope ~ 0.30
slope ~ 0.24
Wsd = 5 μm
Wsd = 2 μm
Ai = (Ids,t - Ids,c)/Ids,c, (%)
Lch/Wsd
180
160
140
120
100
80
60
40
20
-2
0
2
4
6
8
10

Figure 3.4