溶膠凝膠法製備鈦酸鉍薄膜之雙穩態導電率轉換記憶體元件

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摘　　　要

近來由於傳統快閃式記憶體(flash memory)在不斷微縮化下，面臨到許多急欲克服之難題，例如儲存在懸浮閘極(floating gate)中之電荷，因穿遂氧化層(tunneling oxide)過薄而隨著時間漸漸流失，喪失其非揮發記憶效應，另外，在長時間操作之下，易於穿遂氧化層內產生缺陷以及操作電壓過高…等，如此瓶頸，實為下世代非揮發性記憶體研究之首要課題。然而，眾多前瞻性非揮發性記憶體研究中，電阻式記憶體為利用電壓或電流脈衝在極短時間下改變電阻值，並藉由元件內部電阻值之不同作為其相對應之記憶狀態，進而達到資料寫入之動作。

本實驗首先在二氧化矽(200 奈米)/矽基板上鍍製白金下電極(80 奈米)，接著沉積厚度為 100 奈米之鎳酸鑭($LaNiO_3$) 為緩衝層，接著再利用溶膠凝膠法製備鈦酸鉍電阻薄膜(20~60 奈米)，最後鍍上 80 奈米厚之白金上電極，完成$Pt/BiTiO_3/LaNiO_3/Pt$實驗結構。發現此記憶元件具有電阻轉態現象，並討論其電學、物理、化學等性質，分析此材料應用於電阻式記憶體之潛力與特性探討。

Bistable Conductivity Switching Memory Devices Using Sol-Gel Derived BTO Thin Films

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ABSTRACT

A Recently, due to continuously scaling down for the conventional flash memory, there are many issues need to be overcome, such as the charge stored in the floating gate lost due to direct tunneling current or defects formed in the tunneling oxide during long-term operation. Therefore, the investigation of the next-generation nonvolatile memory is going to be the main topics. Among various next-generation nonvolatile memories, resistance random access memory store the data by change the resistance in the memory cell, which can be altered by voltage or current pulse in a short time leading to the write/erase operation.

In this experiment, an 80-nm-thick Pt bottom electrode was deposited on SiO2/Si substrate, and follow by a 100-nm-thick LaNiO3 buffer layer. By sol-gel method, the 20-60nm BiTiO3 thin films were fabricated, and finally, the 80-nm-thick Pt top electrode were deposited to fabricating the Pt/BiTiO3/LaNiO3/Pt structure. The resistive switching behaviors are found in this structure, and the electrical, physical, and chemical properties are also investigated to discuss the possibility for RRAM application.