Chapter 1

Introduction

1.1 Introduction to Memories

Memory can be classified into two main categories, volatile and nonvolatile memory (NVM).

1.1.1 Volatile Memory

Volatile memory loses its stored data as soon as the system is turned off, so it requires constant power to remain its information. Most types of random access memory (RAM) are this category. RAM can be subdivided into two main groups, static RAM (SRAM) and dynamic RAM (DRAM). The difference between them is that the stored information of DRAM memory disappears from the memory within milliseconds, so it has to be refreshed periodically. This makes the operation speed of DRAM much slower than that of SRAM. The speed advantage of SRAM means that it is used in cache memory, which is a small amount of high speed SRAM mounted close to or on the processor itself.

1.1.2 Nonvolatile Memory

NVM does not lose its data when the system or the devices are turned off. A typical NVM device is a MOS-like structure consisting of a source, a drain, an access or a control gate, and a floating gate. It is structurally different from a standard MOSFET due to its floating gate, which is electrically isolated. NVMs are subdivided into two main classes: floating gate and charge-trapping, respectively. Kahng and Sze proposed the first floating gate device in 1967 [1]. In this memory, electrons are transferred from the floating gate to the substrate by tunneling through a 3 nm thin SiO_2 layer. Tunneling is the process by which an NVM can be both erased and programmed, and is usually dominant in thin oxides of thicknesses less than 12 nm. Storage of the charge on the floating gate allows the threshold voltage (V_T) to be electrically altered between a low and a high value to present logic 0 and 1, respectively.

In floating gate memory devices, charges or data are stored in the floating gate and are retained when the power is removed. All floating gate memories have the same generic cell structure. They consist of a stacked gate MOS transistor as shown in Fig. 1-1 [1]. The first gate is the floating gate that is buried within the gate oxide and the inter-polysilicon dielectric (IPD) beneath the control gate. The IPD isolates the floating gate and can be oxide or oxide-nitride-oxide (ONO). The SiO_2 dielectric surrounding the transistor serves as a protective layer from scratches and defects. The second gate is the control gate which is the external gate of the memory transistor. Floating gate devices are typically used in electrically programmable read only memory (EPROM), electrically erasable and programmable read only memory (EEPROM), and Flash memory. The disadvantages of NVM are low operation speed, high operation voltage, poor endurance, and its congenital limit in size due to gate oxide thinning that causing poor retention.

1.2 Resistive Random Access Memory (RRAM)

1.2.1 Introduction to RRAM

RRAM shows superior advantages such as simple device structure, low operation voltage, low power consumption, long retention time, small cell size, high operation speed, low cost, good endurance, and non-destructive readout. As a result, there are high expectations for RRAM to be a next-generation memory. However, it is not yet clearly how the resistance changes in the metal oxide films, the key components of RRAM, and achieving a memory device takes full advantage of the outstanding characteristics of RRAM which has be proven difficultly. RRAM with the properties of the reversible switching between the low (OFF state) and the high leakage (ON state) states, induced by voltage pulse or bias voltage, is not clear. In this study, the sol-gel method is used for the first time to fabricate the $BiTiO_3$-based metal–insulator–metal (MIM) structure, and the conduction mechanisms of the device are investigated. The deposition method, the buffer layer, the electrode materials, and process temperature were adopted for low cost and integration considerations. The resistance transitions between the two leakage states are also changed by voltage pulse. The asymmetric transition times for the switching between the two leakage states are indicated for the first time. The device of RRAM is the MIM structure as shown in Fig. 1-1. It is operated among the two conductivity states by applying either positive or negative voltages on the top electrode. Then, $Bi_4Ti_3O_{12}$ (BTO) thin film is initially insulating will be switched to high conductivity state, and the electric characters can be defined as “0” and “1” in memory device.

1.2.2 Structure and Operation Method of RRAM

In Fig.1-2 [2], the RRAM memory cell is composed of a transistor and a resistor. In order to write the specific resistor to ON state, a dc voltage is applied on the word line which can turn on the access transistor and a positive voltage pulse is applied to the bit line with the source of the transistor grounded as shown in Fig.1-3 [3]. In order to erase the specific resistor to OFF state, a dc voltage is also applied on the word line which can turn on the transistor and a positive voltage pulse is applied to the source of the bit transistor while the bit line is grounded. For the read operation, the word line of the memory cell is selected and a read voltage is applied on the bit line to sense the current value while the source of the bit transistor is grounded. Therefore, the data are determined by comparing the current value with the reference value, and the memory state of the device during the read operation remain unchanged, called non-destructive readout.

The main issue of the cross-point array RRAM is read error. Fig. 1-4(a) and (b) [4] describe how leakage current paths make cell resistance misread. When the resistance is measured with all the unselected lines open, (3,3) cell, for example, has been changed from high to low resistance state after 3 neighboring cells are switched on because of the leakage path described in Fig. 1-4(b). Theoretically, this kind of misreading and misprogrammig issues can be avoided by proper biasing method, but the amount of necessary current becomes unreasonably large as memory density increases [5]. Therefore, it is very important to find suitable rectifying elements to realize an ultra high density cross-point array memory device.

1.2.3 Introduction to Perovskite Materials

Perovskite materials have been investigated for various applications such as superconductors, dynamic random access memory, and gate oxide for complementary metal oxide semiconductor (CMOS). Negative resistance phenomena have been observed in the binary oxides, [6~8] leading to the investigation of various materials such as metal-doped perovskites, $Pr_{1-x}Ca_xMnO_3$ (PCMO), and chalcogenide semiconductors for use in resistive random access memory (ReRAM) applications. Many researchers have reported the resistive switching behavior of various perovskite films and suggested plausible resistive switching mechanisms.

The perovskite structure with the chemical formula ABO3 is shown in Fig. 1-5. The structure is very versatile and is useful in technological applications such as ferroelectrics, catalysts, sensors, and superconductors. The general crystal structure is a primitive cube, with the A-cation in the middle of the cube, the B-cation in the corner and the anion, commonly oxygen, in the centre of the face. The structure is stabilized by the 6 coordination of the B-cation (octahedron) and 12 of the A-cation. The packing of the ions can be thought of the A and O ions together forming a cubic close packed array, where the B ions occupy a quarter of the octahedral holes. Although the primitive cube is the idealized structure, differences in radius between the A and B cations can alter the structure to a number of different distortions of which tilting is the most common one. With perovskite tilt the BO6 octahedron twists along one or more axes to accommodate the difference. Complex perovskite structures contain two different B-site cations. This results in ordered and disordered variants. The perovskite structure shares the property of ferroelectricity with garnet and olivine. Many superconducting ceramic materials have perovskite-like structures.

1.2.4 Crystal Structure of BTO

Novel synthesis methods have been investigated for the preparation of $Bi_4Ti_3O_{12}$ thin film. The Aurivillius family of layered perovskite oxides is a group of ferroelectric materials whose properties have been extensively studied. In Fig. 1-6, their crystallographic structures consist of an integer number ("n") of perovskitelike units interleaved with $(Bi_2O_2)^{2+}$ layers. The possibility to have lead-free compounds with almost fatigue free behavior has attracted the attention of many researchers, especially in the area of thin film technology. $Bi_4Ti_3O_{12}$ is an n=3 member of the Aurivillius family of compounds. These characteristics together with its high piezoelectric coefficients and low permittivity make it a suitable material for high-temperature transducers. The syntheses of the crystalline phases were obtained by annealing of the precursors at different temperatures.

1.3 Resistive Switching Properties of BTO Films

In order to focus on the measurement of electric properties and simplify the experiment process, all the BTO films are produced from the 0.04 M solution. Moreover, the most important parts of a nonvolatile memory are the electrical properties, including the switching voltage, operation voltage, retention time, and fatigue, and those properties are attempted to be improved. The electrical properties of BTO thin film are significantly influenced by changing, even a little, the mole concentration of the contents. In addition, the fabricated process is modified by treating with the different pre-process and post-process. In the pre-process, the various mixing methods of BTO solution had been tried. In the post-process, the various deposition temperatures, thermal treatment temperatures, and different electrodes had been also demonstrated.

1.4 Thin Film Coating by Sol-Gel

We adopted the oriented $LaNiO_3$ film as the buffer layer for the considerations of low cost and low process temperature. The sol–gel method is used to deposited BTO films to investigate the electrical and physical properties. Sol–gel method has the advantages that include low cost, easy stoichiometric control, and high uniformity. The influence of thermal treatment on the physical properties of the films is also investigated during process. The BTO film, synthesized on $LaNiO_3/Pt/SiO_2/Si$ substrate, is found to have the reversible switching behavior and the memory effect. The physical and electrical properties of the memory device are studied. The structure and surface morphology of the BTO films are also characterized by X-ray diffraction and scanning electron microscopy. The resistive switching between high state and low state can also be operated with voltage sweeping. The device with the properties of long retention time and non-destructive readout is expected to be suitable for nonvolatile memory application.

1.5 Resistive Switching Mechanisms

There are many kinds of mechanisms which have been proposed for the RRAM to explain why the switching phenomenon occurs. In 1964, conducting filament was used to interpret the property of the switching phenomenon [9]. The conducting filament will be formed when the external applied voltage is employed on the device. Recently, the rediscovery that the switching phenomenon lies in polycrystalline NiO films has been reported again [10]. In the nickel oxide, it is observed that the bistable phenomenon is not only in the polycrystalline NiO films but also in the epitaxial ones, so the bistable phenomenon is not on the ground of the structural phase transition as remarked in the

phase change memory device. Those characteristics were proposed to be caused by the formation and rupture of the conducting filaments within the NiO films. In an insulator, six conduction mechanisms, Schottky emission, Frenkel-Poole emission, Tunnel (field emission), Space-charge limited, Ohmic and Ionic conduction, are proposed to explain transport of carriers leading current flow. In table 1-1, the conduction processes in the insulators are summarized.

When a metal contacts an insulator, their work function difference forms a barrier in band diagram with a barrier between the interface of metal and the insulator. The current, then, flows in the insulator by means of the fact that carriers with enough high thermal energy to surmount the barrier and to transport either from insulator to metal or from metal to insulator. A plot of lnJ versus $V^{1/2}$ produces a straight line with a slope determined by the permittivity of insulator.

The Frenkel-Poole emission is due to field enhanced thermal excitation of trapped electrons into the conduction band. A plot of ln(J/V) versus $V^{1/2}$ yields a straight. When an enough large field applies on an insulator, trapped electron can escape from a trapped state or electrons can tunnel from the metal Fermi energy into the insulator conduction band. The tunnel emission has the strongest dependence on the applied voltage but is not correlation to temperature. Space-charge-limited results from a carrier injected into the insulator, where no compensating charge is present. The current for the trap-free case is proportional to the square of the applied voltage.

At low voltage and high temperature, current is carrier by thermally excited electrons hopping from one isolated state to the next. This mechanism yields an Ohmic characteristic exponentially dependent on temperature. The ionic conduction is similar to a diffusion process. Generally the dc ionic conductivity decreases during the time the electric field is applied, because ions cannot be readily injected into or extracted from

the insulator. After the external applied voltage is removed, large internal fields remain causing a few ions to flow back toward their equilibrium position and hysteresis effects result.

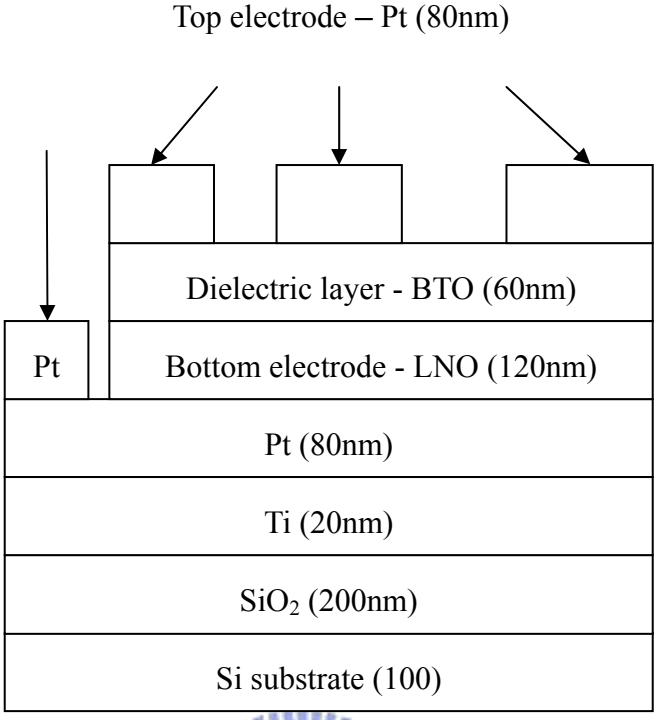

Fig. 1-1 Cross section view of the memory device

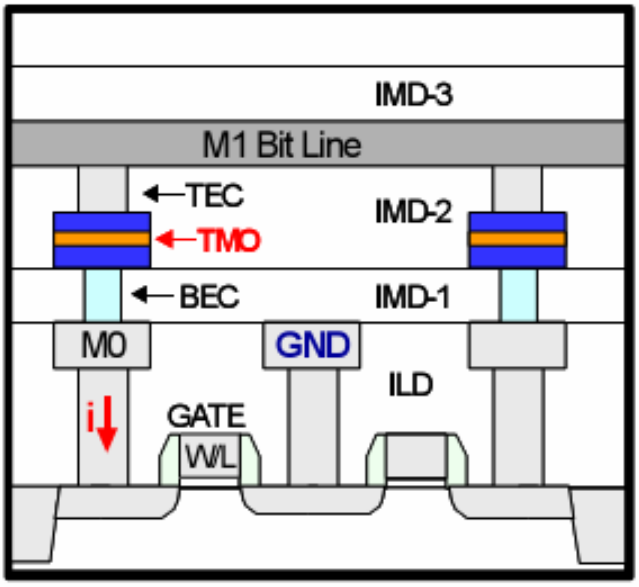

Fig. 1-2 Cross section schematic diagram of the RRAM. The transistor is fabricated in the front and the resistor in the back end [2]

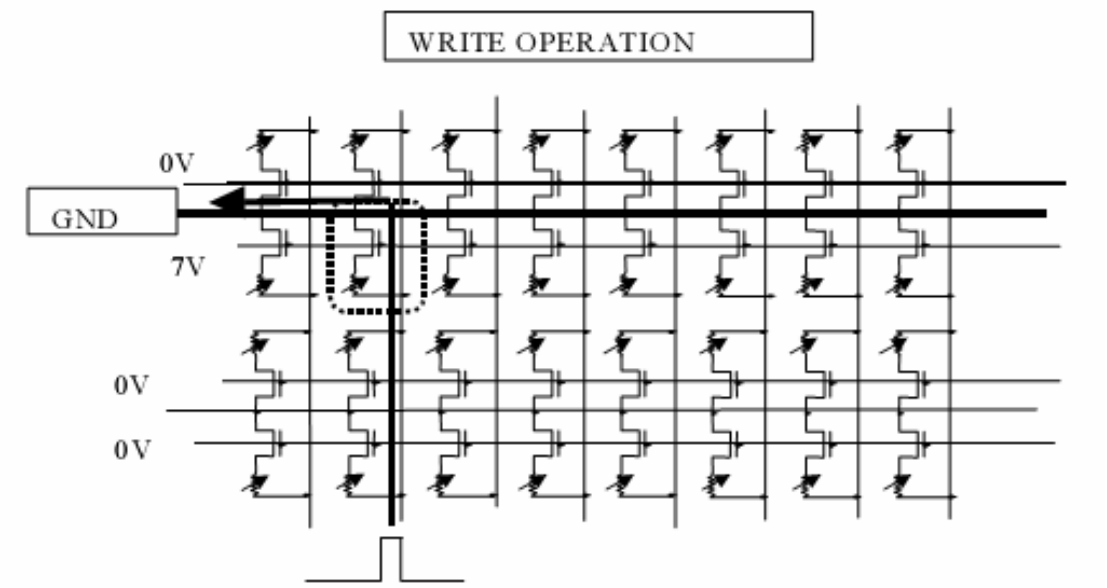

Fig. 1-3 Equivalent circuit of an array for the write operation of a given bit resistor [3]

(a)

W/L \ B/L	1	2	3	4
1	29M	20M	34M	48M
2	67M	25M	21M	46M
3	64M	21M	74M	24M
4	36M	55M	19M	38M
5	23M	46M	47M	39M

W/L \ B/L	1	2	3	4
1	28M	7.4M	7.4M	27M
2	28M	770	1.1K	7.6M
3	34M	690	950	7.6M
4	35M	7.1M	7.2M	19M
5	23M	18M	18M	22M

(b)

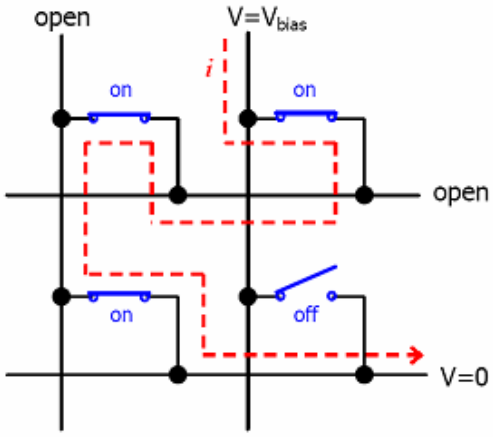

Fig. 1-4 Describing how leakage current paths make cell resistance misread [4]

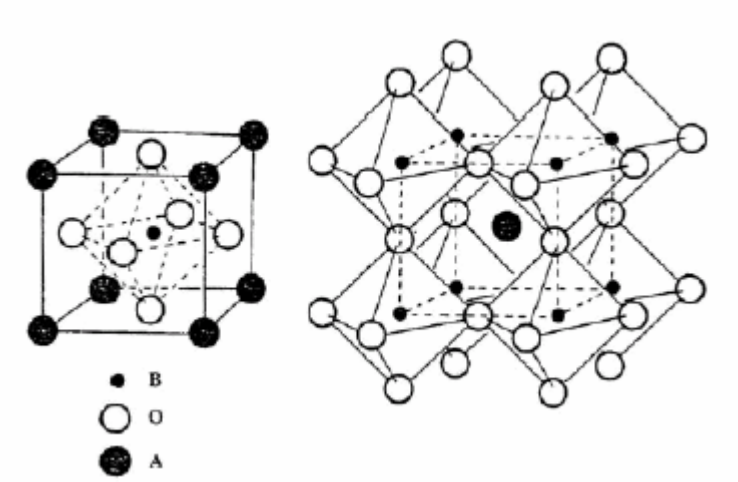

Fig.1-5 Basic structure of perovskite material [12]

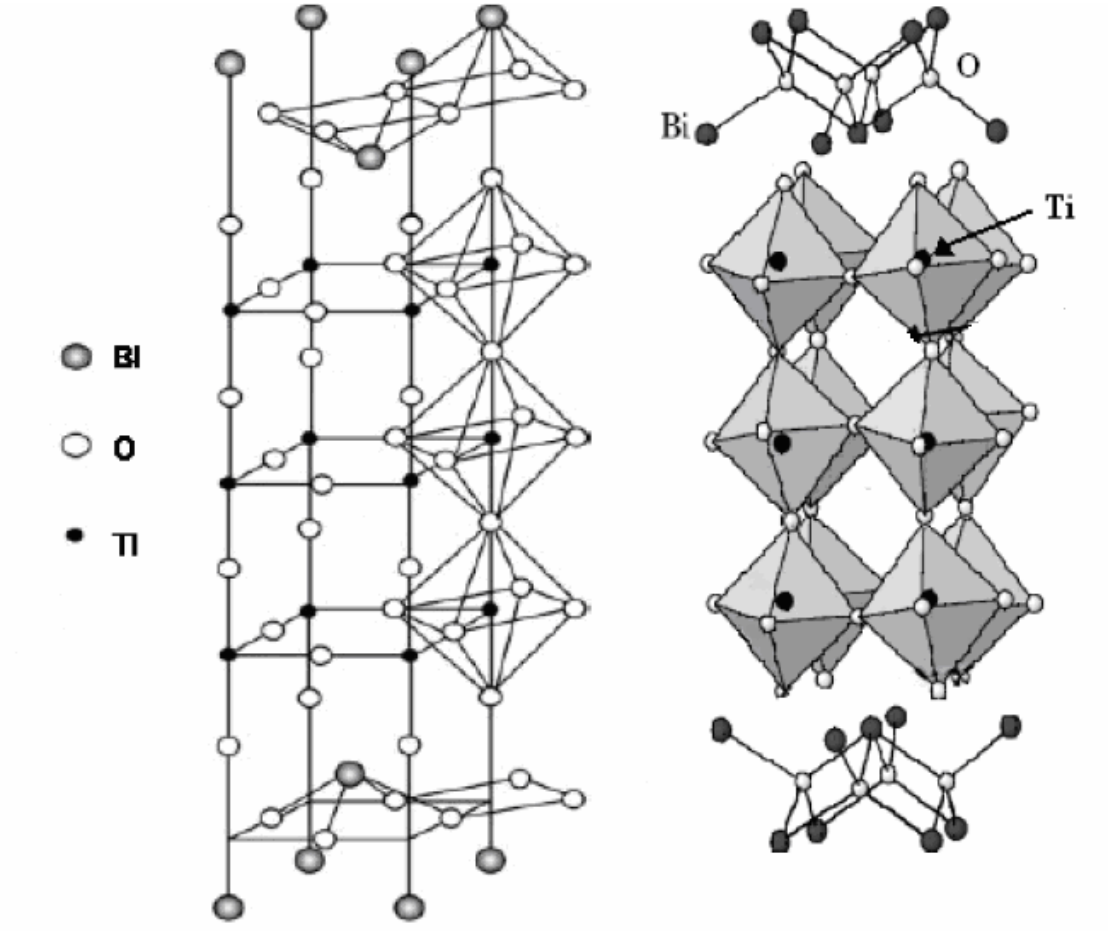

Fig.1-6 $Bi_4Ti_3O_{12}$ crystal structure [13]

Conducting mechanism	Voltage and temperature dependence
Schottky emission	$\sim T^2 \exp(\frac{+a\sqrt{V}}{T} - \frac{q\Phi_B}{kT})$
Frenkel-Poole emission	$\sim V \exp(\frac{+2a\sqrt{V}}{T} - \frac{q\Phi_B}{kT})$
Tunneling (field) emission	$\sim V^2 \exp(\frac{-b}{V})$
Space-charge-limited current	$\sim V^2$
Ohmic conduction	$\sim V \exp(\frac{-c}{T})$
Ionic conduction	$\sim \frac{V}{T} \exp(\frac{-d'}{T})$

Table 1-1 Conduction processes in insulators [14]