國　立　交　通　大　學

電機學院微電子奈米科技產業研發碩士班

碩　士　論　文

在有機薄膜電晶體低溫製程下利用常壓式電漿技術沉積閘極二氧化矽

Low Temperature Processes of Organic Thin-Film Transistor with Gate Dielectric of Silicon Dioxide Deposited by Scanning Atmospheric-Pressure Plasma Technology

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國立交通大學電機學院產業研發碩士班

摘要

我們已經成功地利用大氣壓電漿技術在有機薄膜電晶體低溫製程下沉積閘極矽氧化物，大氣壓電漿技術的優點是可以在一般正常氣壓下沉積矽氧化物，並且也可以應用在低溫製程下適合軟性電子製程條件，在這次研究中，我們的有機薄膜電晶體操作電壓小於-5 伏特，利用 MIM 的結構量出絕緣層在 0.5 MV/cm 的崩潰電場下漏電流大約在 9×10^{-8} A/cm^2，在可携式的電子產品上低的操作電壓與低的漏電流是必要的條件，對於沒有定義有機半導體的主動成區域比有定義有機半導體的主動層區域的漏電流特性大，而且對於有沉積 HMDS 的元件比沒有沉積 HMDS 的元件的漏電流特性大。

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ABSTRACT

We have successfully fabricated pentacene-based organic thin film transistor at a low temperature process with silicon oxide as a gate dielectric deposited by atmospheric-pressure plasma technology (APPT). The major merit of scanning atmospheric-pressure plasma technology was low deposition temperature at one standard atmosphere which was suitable for the application of flexible electrons. The organic thin film transistor demonstrated in this study could operate at the voltage less than -5V and the leakage current of silicon oxide dielectric with MIM structure is about $9\times10^{-8}A/cm^2$ at 0.5 MV/cm. The low operation voltage and low leakage current properties are required in portable applications. Leakage current of not define pentacene region is higher than define pentacene region. And leakage current of have HMDS is higher than not have HMDS.

誌　謝

首先，要感謝的是我的指導老師張國明教授，在這兩年的碩士研究生涯裡給予熱心的指導和教誨，使的我不論在研究上或待人處事上都有很大的收穫，更給我們建立獨立思考解決問題的觀念，也不斷的激勵我，讓我更有信心的完成我的學業，在此衷心的表達感謝之意。

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Chapter 1

Introduction

1.1 Application and Motivation of Organic Thin Film Transistor (OTFT)

In the past decade, organic thin-film transistor (OTFT) has been studied extensively. Now, technical product gradually more and more progress, from large to small and from weight to light, people's life is more and more convenient in emphasizes high efficiency century. Along with the low cost and the massively manufactures technology, the electronic products market starts to emphasis, organic thin film transistors start to become the research the tidal current. No matter industry or academia energetically investment research.

Except conventional technology of display on glass substrate, technology of display on flexible substrate already becomes noticeable technology on next generation. Organic thin film transistors have already manufactured on flexible substrate for low cost and low temperature process. In at present, some many flexible substrates are researched and developed, show figure1-1.

Poly(ethylene terephthalate) (PET) and poly(ethylene naphtha-late) (PEN) were often used for OTFT substrates. Because, they have very little effect on the melting point (Tm), which increases by only a few degrees but a substantial effect on the glass transition temperature (Tg). Moreover, chooses the suitable material of sub-strate is important, view table 1-1. We will set experimental process temperature less than 300℃.

However, organic thin film transistors have more potential than conventional transistors. Organic thin film transistors have been proposed for use in various applications in displays and flexible electronic devices. Such as active-matrix emissive and reflective displays, chemical and mechanical sensors, low-cost flexible

integrated circuits, radio-frequency identification (RFID), light-weight large-screen displays, low power consumption, low temperature manufacturing, liquid-crystal flat panel displays, biochemical sensors and large-area sensor arrays and so on.

The organic material may carry on the large area using the solution to spin-coating, or semiconductor thin film layers were deposited by vacuum evaporation, down to reduces the manufacture process the cost. Therefore, improves the organic thin film transistor the manufacture process to enhance the manufacture process efficiency. Such as dip coating, inkjet printing and contact coating. Nevertheless, these all are suitable on plastic substrate, Organic thin film transistors will develop roll to roll manufacture process regarding the future to have the very large help. Down to achieves manufacture the process simple aspiration and devices of quality frivolous characteristic.

On the other hand, the organic semiconductor material improvement characteristic, the process enhances the technology and the OTFT improvement structure, the OTFT application gradually is realized on integrated circuits. OTFT decides the performance of the transistor by mobility magnitude. However, the high operating voltage remains a limitation on organic transistors. One of the most critical problems with traditional organic TFT is the large operating voltage which is often higher than 10V. Therefore, account for the power consumption of the transistor to increase and the performance of the transistor to reduce.

1.2 Issues for fabrication OTFT structures

However, in order to successfully integrate organic thin-film transistors (OTFTs) technology, construction of organic thin-film transistor view figure 1-2, there are a few important issues to be discussed, as below several terms:

1.2.1 Organic semiconductor material

The semiconducting materials generally divide into the organic materials with the inorganic materials. Inorganic, atoms are bonded by strong covalent bond, result as the higher carrier mobility. Organic, molecules are bonded by weak Van der Waal forces. Lower mobility is due to the localized-states carriers. View table 1-2. The inorganic semiconductor materials usually use have several kinds, such as Ⅳ Kind, Ⅱ-Ⅵ Kind and Ⅲ-Ⅴ Kind. View figure 1-3.

Nevertheless, the organic materials generally divides into three kinds, respectively are Small molecular (molecular weight < 3000) , Polymer (molecular weight > 10000) and Complex (molecular weight > 10000) .

The small molecular material usually uses evaporative process, therefore, it needs the perfect vacuum the environment. Making the manufacture process to be relatively complex moreover the cost also relatively to enhance. N-type of the small molecular material carries transmission characteristic poorly. The material appears extremely does not stabilize in the air environment. But also has one kind of semiconducting organic material to be called a-nT(Oligothiophene). Researches and develops the improvement material the stability to be good and the characteristic nice in the air environment. P-type of the small molecular material most has the representative material is pentacene, view figure1-4. Among all semiconducting organic materials used to fabricate OTFT, pentacene is the most popularly used organic material to serve as the active layer because of its higher carrier mobility in OTFTs. The performance of OTFT is determined by its mobility, which in turn is greatly influenced by the interface properties between the active layer and the dielectric layer. Pentacene (C22H14) is a semiconducting organic material currently attracting much interest among scientists and engineers because pentacene films can be used as a channel layer of OTFTs with exceptional mobility.

Pentacene transistors can be used as a switching device for active-matrix display. The pentacene films are usually polycrystalline when they are deposited by organic vapor phase deposition and thermal evaporation. Other also have some small molecular semiconductor organic materials, such as Linear fused ring compounds, 2-D fused ring compounds, oligomers and 3-D molecules and so on.

The polymer compares to the small molecular has the higher manufacture process superiority, Because of the organic polymer manufacture process can apply the technology of solution coating. Such as spin-coating, dip-coating and printing process and so on. Consequently, manufacture process more is easy to apply in on the large area device. Regioregular Poly(3-alkylthiophene) (P3HT) is P-type of the organic polymer most has the typical material. View figure1-5. At present may utilize on the photoelectric device, and the transistor has superior characteristic of mobility.

Poly(benzobisimidazobenzophenanthroline) (BBL) is N-type of the organic polymer most has the typical material. Hereinto, Poly (9,9-dioctylfluoreneco- bithiophene) (F8T2) is one kind material of Thermotropic liquid crystal. It may apply in printing process achieved largely reduces the production cost.

The complex most have the typical materials such as Phthalocyanine Coordination Compound and Organic-inorganic Hybrid Material. Moreover Phthalocyanine Coordination Compound is most early applied on the semiconductoring organic device.

Organic thin-film transistors (OTFT) based on conjugated polymers, oligomers, or other molecules have been envisioned as a viable alternative to more traditional, mainstream thin-film transistors (TFT) based on inorganic materials. Because of the relatively low mobility of the organic semiconductor layers, OTFT can’t rival the performance of field-effect transistors based on single-crystalline inorganic semiconductors, such as Si, Ge, GaAs, InP, which have charge carrier mobilities about three orders of magnitude higher [21].

1.2.2 Source/Drain contact

The position of the Fermi level is a quite important consideration in the semiconductor. As a result of metallic work function consideration, whether forms barrier or ohmic contact interface between metal and semiconductor. and it is decided to the fermi level position. Therewith judges fermi level the relative position to decide type of conduction condition. If semiconductor fermi level approaches valence band, treats as by the hole carries to convey. Therefore is called the p-type semiconductor. Adversative, if semiconductor fermi level approaches conduction band, treats as by the electron carries to convey. Therefore is called the n-type semiconductor. Consequently, we will improve interface to avoid forming Schottky barrier and creates oversized contact resistance to affect the device characteristics.

1.2.3 High dielectric constant insulator

In recent years, the organic thin film transistor (OTFT) has been studied widely on flexible electronic circuit for the application such as e-books, e-papers, and RF tags [1-3]. The effect of flexible electronic products for human life will grow drastically in the near future. A reliable low temperature process becomes more and more important and urgent for OTFT fabrication since a critical issue in OTFT fabrication is that the flexible substrate cannot suffer high temperature. There are some low temperature methods used to fabricate inorganic gate insulator reported in many studies such like sputter, electron-gun, and anodic oxidation [4-6]. Although the dielectric could be deposited or grown at low temperature, however, in order to reduce gate leakage current for obtaining a good gate dielectric property, a high temperature annealing after dielectric deposited is needed. Besides, a good gate insulator with high dielectric constant at low-temperature process is urgently demanded for the portable application on OTFT now. A low operation voltage for OTFT is required to reduce power consumption from flexible electronic circuits. By adopting some

high dielectric constant materials such as Al_2O_3 [8], TiO_2 [7], HfO_2 [6] and TaO_2 [5] for OTFT are a common way to reduce the operation voltage. Increase dielectric constant with reduce leakage current for OTFT, phenomenon of leakage current involve defect density and charge trap density at low temperature process,

charge trapped in defects causes a shift in the gate threshold voltage of the OTFT, the trapped charge will change with change with time so the threshold voltage will shift with time, leading to instability of operating characteristics, and occur increase scatter carriers so that low mobility for OTFT performance, hence, influence of dielectric quality is important for OTFT research.

1.2.4 Active region pattern

In order to obtains the high efficiency the experiment, develops many conveniences process technology, a variety of strategies have been used to create integrated arrays of transistors including photolithography, stamping, and shadow masking, photolithography has an established infrastructure thanks to its extensive use in silicon fabrication, printing process in which the printing surface is neither raised nor etched into the plate, and printing is affected by means of a chemical process that allows ink to adhere to only the parts of the surface to be reproduced. Photolithographic patterning has several advantages: arbitrary patterns can be used with fine features, a variety of deposition techniques may be used, and photolithography can be applied over large areas in multilayer process.

1.2.5 Passivation

The degradation of electrical characteristics was observed, show figure 1-7. It is supposed, the reason is sheer stress by the viscosity of PVA when it was coated and dried. Because of the reason, we developed a novel encapsulation method for OTFTs. OTFTs were packaged by novel encapsulation method; the Al film adhered onto the pentacene

active layer in a dry nitrogen atmosphere using a proper adhesive. Using this method, we observed no degradation, view figure 1-8. No substantial degeneration occurred. The initial mobility of no passivation device the characterization was degraded after long terms. Their mobility is reduced to 2% of initial mobility value. Hence, a lifetime was defined as the time necessary to reduce mobility to 2% of initial mobility value. Through this result, the performance and the stability were observed by the novel encapsulation effect[15].

1.2.6 Surface treatment

The dielectric polarity is modified by the self-assembled monolayer (SAM) on inorganic dielectrics. Inorganic dielectrics with lower surface energy proffer improved device performance; such surfaces reduce many of interface traps in OTFTs [9,10]. However, controlling gate leakage is an extra difficulty[11]. As well as the increase in capacitance, the surface polarity (hydrophilic or hydrophobic) of the gate dielectric is an important factor[5]. However, the inorganic metal oxide dielectric with higher polarizability leads to the higher O-H group density on the interface and oppositely rough surface morphology. The formed O-H groups and the rough surface further affection the unprofitable quality of device performances. By this reason, the polymer-coating manner appears to be absolutely pervasive and thus could be used to any dielectric surface before organic semiconductor deposition [12-14]. In order to successfully integrate with OTFTs technology, there are a few important issues to be addressed, including degradation in channel mobility, charge trapping, and thermal stability.

1.2.7 Device structure

Usually, test structures of OTFT are usually fabricated in shown figure1-9. Top gate advantages were slef-passivation and fine source

/drain resolution, but disadvantages were poor semiconductor/dielectric interface and high contact resistance.

1.3 Gate dielectric for organic and inorganic materials

Organic dielectrics can be solution-processed, provide smooth films on transparent glass and plastic substrates, are suitable for optic-electronics like photo-responsive OFETs due to their high optical transparency, can be thermally stable up to 200℃ with a relatively small thermal expansion coefficient, and can posses a rather high dielectric constant up to 18.

Required properties for gate dielectrics.

1. Good for pentacene growth (for high mobility).
2. Should have low leakage current (for high on/off ratio).
3. Good chemical resistance (for high resolution).
4. Spin on material (for low cost).
5. High k (for low power).

1.4 Introduction of APPT

The atmospheric-pressure plasma technology (APPT) is useful for treating and modifying the surface properties of organic and inorganic materials. The APPT apparatus does not require any vacuum systems, produces high density plasma, and provides treatment of various substrates at low temperatures while operating open to the atmosphere. The plasma system has used for a wide variety of applications including treatment of polymer films, paper, wood, and foils; plasma grafting and plasma polymerization; ash various materials in the microelectronics industry; barrier layer deposition for the packaging industry; and sterilizing biologically contaminated materials.

For polymer films, the technique offers the following advantages:

- Uniform treatment and No backside treatment.
- Improved surface energy with concomitant improved wet ability, printability, and adhesion.
- No additional vacuum system and low cost.
- Continuous fabrication availably and high speed for production.
- High plasma density.

As shown in Fig.1-10, we exhibited the atmospheric-pressure plasma system which was used in our experiment.

From the viewpoint of processes, deposition method of SAPPT is more efficient than that of E-gun for the OTFT process since SAPPT does not need a vacuum system. This takes advantages of reduced process time and cost of the equipment. The electric properties of OTFT device fabricated at low temperature processes are demonstrated.

1-5 Thesis Organization

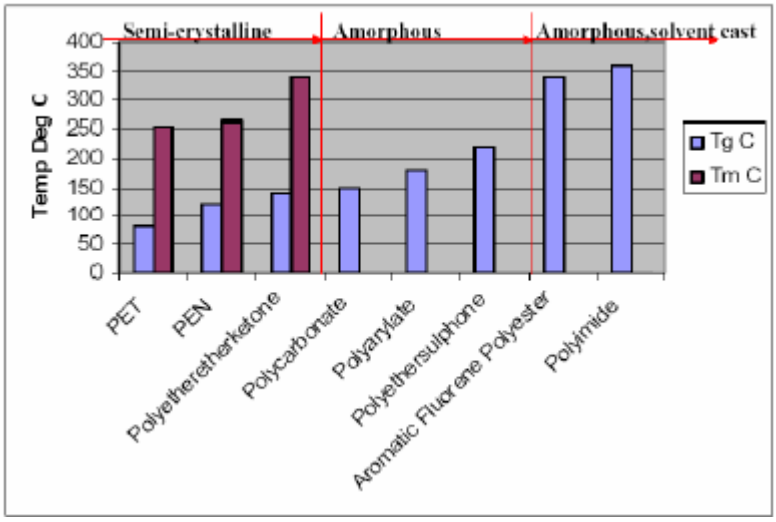
In this study, properties of silicon oxide deposited by SAPPT and E-gun system on silicon substrate are discussed. In addition, a suitable condition for silicon oxide deposited by SAPPT was selected from different temperature biases using MIS and MIM test structures.

In chapter 1, we describe application and Motivation of Organic Thin Film Transistor. Than acquaint with issues for fabrication OTFT structures, and technique of APPT.

In chapter 2, we adopt a new process, APPT, which can be operated under low temperature and atmospheric ambient. And APPT will make use of dielectric layer SiO_2 for our experiment. We use to two different systems deposited silicon oxide as insulator dielectric layer which to test insulator quality of handicapper convenient for metal insulator semiconductor (MIS), metal insulator metal (MIM) and amorphous silicon metal insulator metal (a-Si MIM) structures.

In chapter 3, we use different structures to experiment with silicon oxide dielectric layer quality and leakage current.

In chapter 4, we will describe the conclusions and the future works.



Ref: William A. MacDonald"Advanced Flexible Polymer Substrates"p.165

Figure 1-1: Compare with temperature for a variety of flexible electronic substrates.

Continuous-use Temp.	Material	Characteristics (good, OK, bad)
900°C	Steel	Opaque, moderate CTE, moderate chemical resistance, poor surface finish
275°C	Polyimide (Kapton)	Orange color, high CTE, good chemical resistance, expensive, high moisture absorption
250°C	Polyetheretherketone (PEEK)	Amber color, good chemical resistance, expensive, low moisture absorption
230°C	Polyethersulphone (PES)	Clear, good dimensional stability, poor solvent resistance, expensive, moderate moisture absorption
200°C	Polyetherimide (PEI)	Strong, brittle, hazy/colored, expensive
150°C	Polyethylenenapthalate (PEN)	Clear, moderate CTE, good chemical resistance, inexpensive, moderate moisture absorption
120°C	Polyester (PET)	Clear, moderate CTE, good chemical resistance, inexpensive, moderate moisture absorption

Ref : MRS 2002 FlexICs

Table 1-1: Compare with characterization for a variety of flexible electronic substrates.

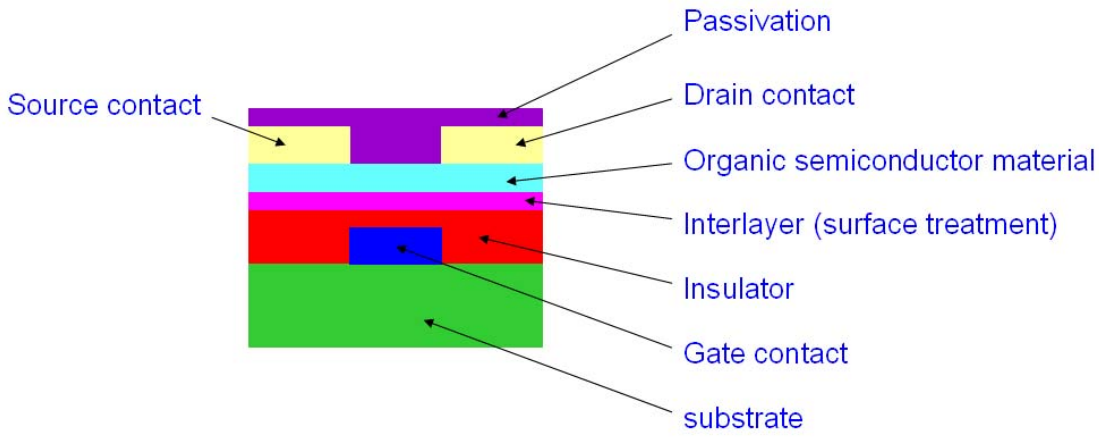


Figure 1-2: Construction of organic thin-film transistor

	Active materials	Mobility (cm^2 / v-s)
Inorganic semiconductor	Ge	1900
	Silicon crystal	300 ~ 900
	Poly silicon	50 ~ 100
	Amorphous silicon	~ 1
	GaAs	400
	InP	150
Organic semiconductor	P3HT poly(3-hexylthiophene)	0.1
	Pentacene	~ 1
	C60	0.3
	α-W-hexathiophene	0.03
	Polyacetylene	0.001
	PTV (pooly(2,5-thienylene vinylene)	

Table 1-2: Characterization of materials for OTFT.

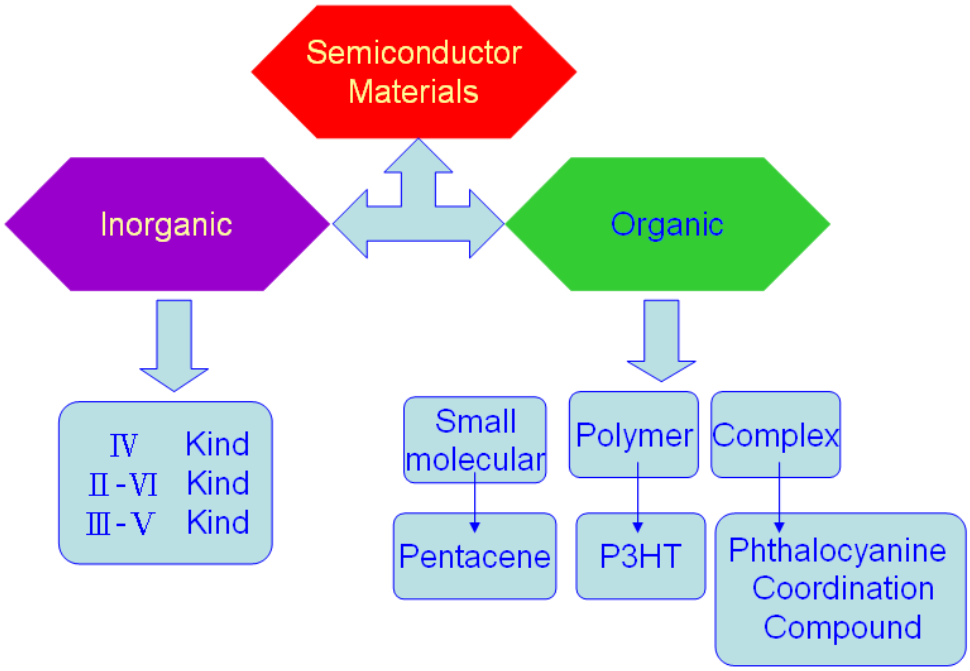
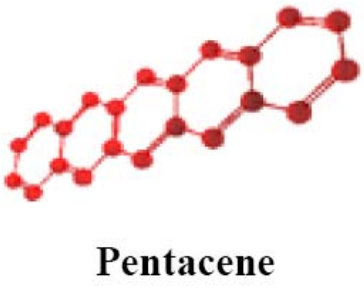


Figure 1-3: Classification of semiconductor materials



Pentacene

Figure 1-4: Molecular structure of pentacene.

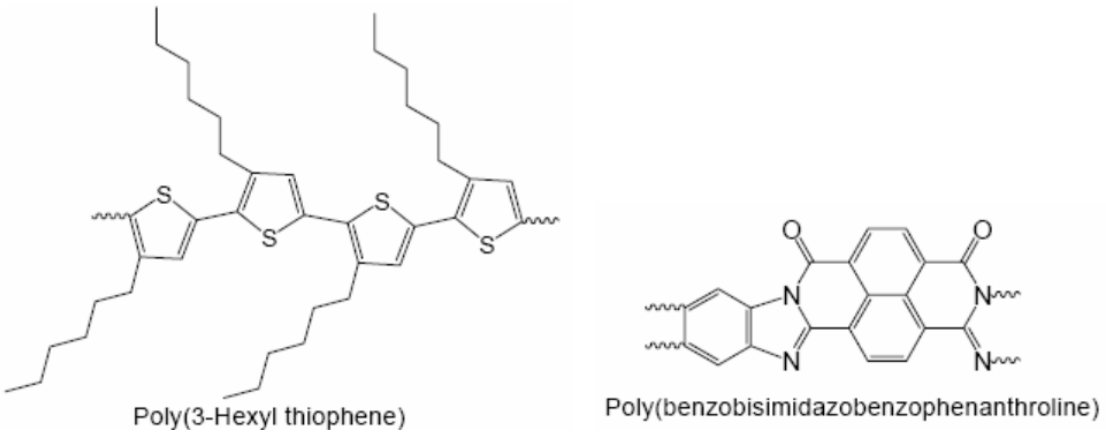
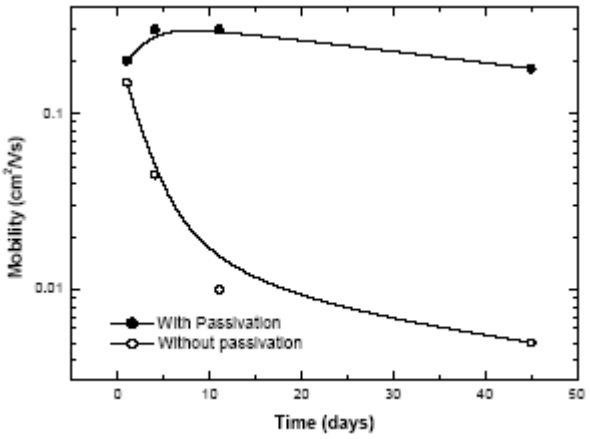
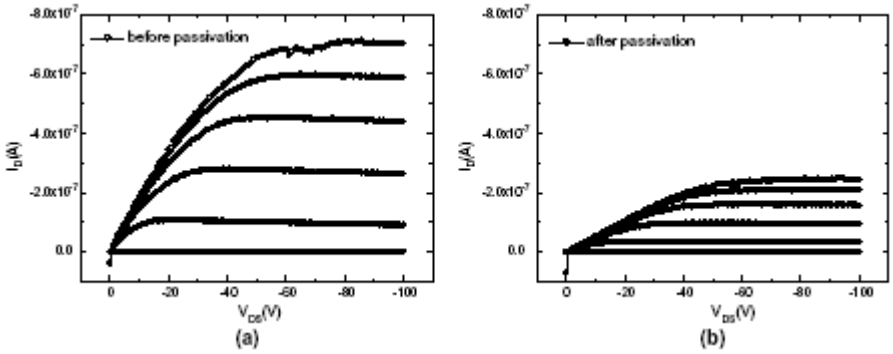


Figure 1-5: Molecular structures of P3HT and BBL.



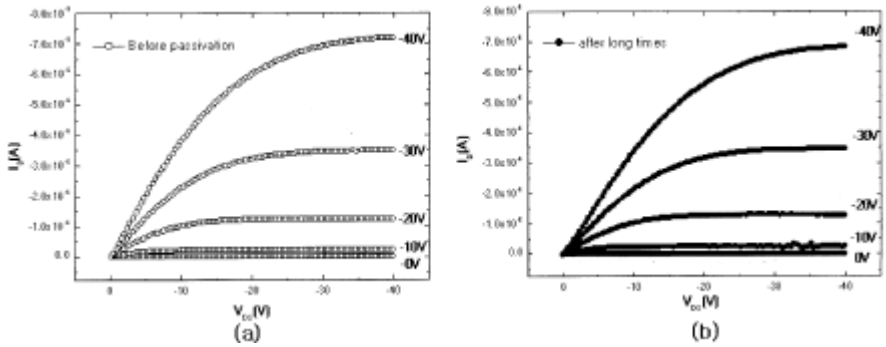
Ref : *Synthetic Metals 143 (2004) 21–23*

Figure 1-6: Influence of mobility for OTFT passivation.



Ref: Current Applied Physics 5 (2005) 348–350

Figure 1-7: The electrical characteristics of OTFT encapsulated by the PVA coating method.



Ref: Current Applied Physics 5 (2005) 348–350

Figure 1-8: The electrical characteristics of OTFT encapsulated by polyacrylate-based adhesive multilayer composed method.

Contact-angle measurements and the corresponding surface free energy of the commonly used dielectrics in the OTFTs fabrication

Substrate	Contact angle between liquid and sample			Surface free energy (mJ/m^2)
	D.I. water	Glycerol	Di-iodo-methane	
Al_2O_3	20–37			68–78
Si_3N_4	20–30			55–60
SiO_2	35.7	22.4	25.1	60
PVA	53.9	54		46.3
HMDs + SiO_2	53.7	53.7	43.9	45.4
PVP-copolymer	50–60			42
Pentacene				38,42–48
AlN	72.9 ± 5	60.7 ± 4	43.8 ± 2	38.3
OTS + SiO_2	78.9	81.8	43.9	34.9

Ref: Organic electronics 8 (2007) 450-454.

Table 1-3: Characterization of contact angle for organic and inorganic materials

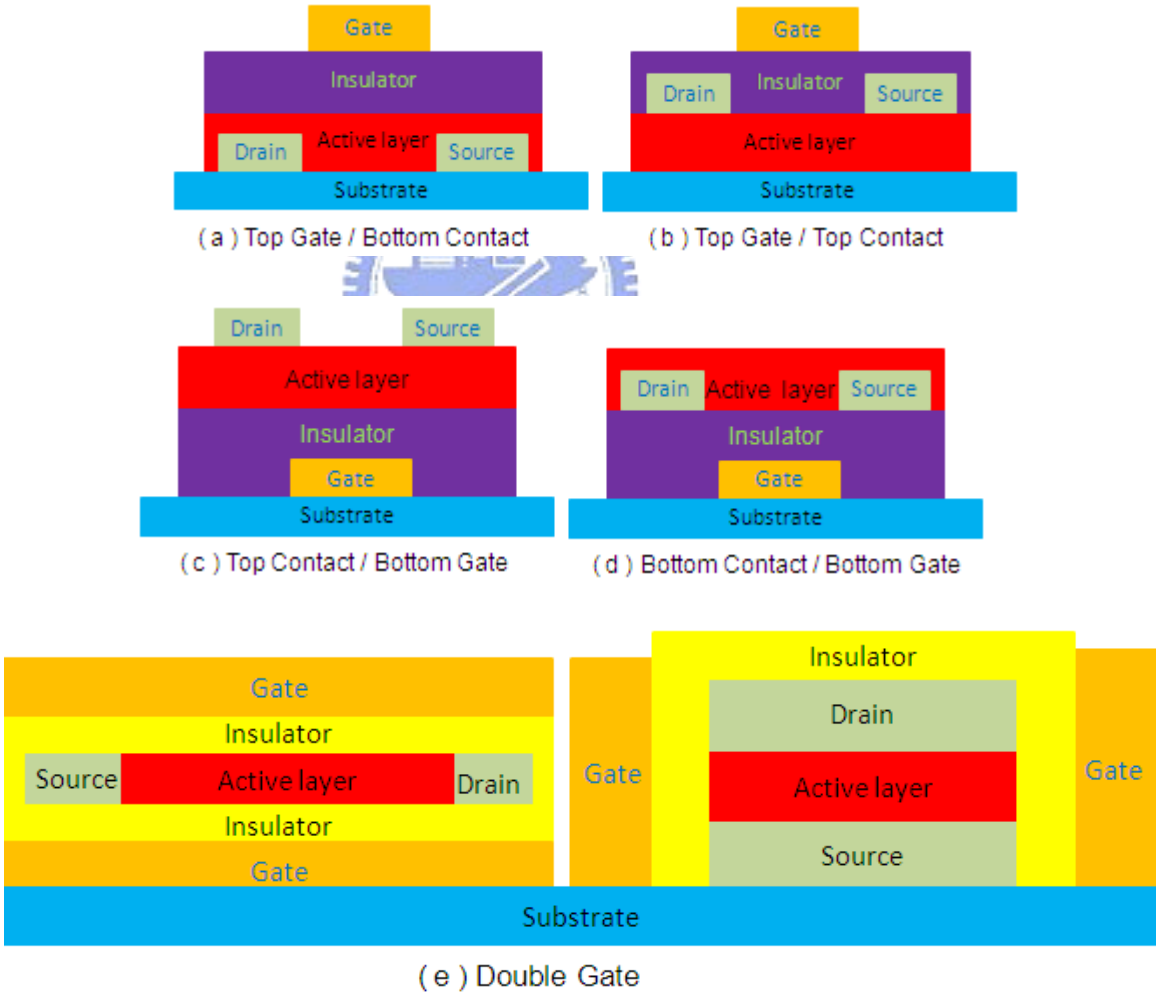


Figure 1-9: Schematic of the organic thin film transistors (OTFTs) with (a) Top gate/Bottom contact structure (b) Top gate/Top contact structure (c) Top contact/Bottom gate structure (d) Bottom contact/Bottom gate structure (e) Double gate structures.

	Dielectric materials	Process methods
Inorganic dielectric	Al_2O_3 Si_3N_4 SiO_2 AlN TiO_2 HfO_2 Ta_2O_5	CVD E-Gun evaporation Sputter Thermal coater evaporation Anodic oxidation
	Siloxane-based SOG	Spin-coater
Organic dielectric	PVA PMMA PVP SAM: MNB, MB, MMB HSQ (low-K)	Roll to roll Spin-coater Inkjet printer Sol-gel

Table 1-4: Characterization of dielectric materials and process methods for OTFT

Figure 1-10: APPT system of ITRI

Chapter 2

Experiment

2.1 Silicon oxide deposited with E-gun and SAPPT equipments on the metal insulator semiconductor (MIS) structure

In this scenario, we use to two different systems deposited silicon oxide as insulator dielectric layer which to test insulator quality of handicapper convenient for metal insulator semiconductor (MIS) structure.

First, the n^+-Si wafer was used as the substrate, and was rinsed in the deionization water (DI water), and was then dipped in dilute HF solution (HF:DI water = 1:100) that to remove the native oxide, the wafer was accomplished the RCA Clean procedure after, deposition of silicon oxide were electron-beam (e-gun) technique and atmospheric-pressure plasma technology (APPT), respectively.

In atmospheric-pressure plasma technology aspect, Heats up the Tetraethoxy silane (TEOS) to 180℃ was injected by nitrogen (50％) and oxygen (50％) as carrier gases which was the deposition source of silicon oxide. The plasma power was established around 50 W with an appropriate scanning rate (sccm /cycle) to deposit silicon oxide on the top of n^+-Si substrate at room temperature under an atmospheric-pressure. The thickness of silicon oxide was increased with the scanning times (cycle/area) , and we adopted 80 times and flow 1 sccm parameters to compare with different silicon oxide dielectrics.

In electron-beam technique aspect, the silicon substrate was deposited 60 nm thick remained at room temperature (25℃) that the deposition rate and vacuum pressure were 0.05 nm/sec and 4×10^{-6} Torr, respectively. Finally, all top contact electrodes were deposited 300 nm thick aluminum layer defined with shadow mask by thermal coater system. The active region pad of all capacitors was diameter 200 μm and all bottom contact electrode were deposited 300 nm thick aluminum layer before the bottom n^+-Si substrate swabs the sponge of dilute HF solution.

2.2 Silicon oxide deposited with effect of substrate temperature by SAPPT on the metal insulator metal (MIM) structure

In this scenario, we purpose to deposit silicon oxide dielectric on the bottom contact electrode metal by atmospheric-pressure plasma technology. But silicon oxide was not deposited on the metal at room temperature. Consequently, we try to find solution to heat up to the n^+-Si substrate that was able to deposit on the metal.

First, the n^+-Si wafer was used as the substrate, and was rinsed in the deionization water (DI water), and was then dipped in dilute HF solution (HF:DI water = 1:100) that to remove the native oxide, the wafer was accomplished the RCA Clean procedure after, deposition of silicon dioxide was thermal kiln grown 500 nm thick on the top of n^+-Si substrate for isolation purpose. And deposited 300 nm aluminum as the bottom electrode. Heats up the Tetraethoxy silane (TEOS) to 180℃ was injected by nitrogen (50％) and oxygen (50％) as carrier gases which was the deposition source of silicon oxide. The plasma power was established around 50 W with an appropriate scanning rate (sccm /cycle) to deposit silicon oxide on the top of n^+-Si substrate at room temperature under an atmospheric-pressure. The thickness of silicon oxide was increased with the scanning times (cycle/area) , silicon oxide was deposited on the aluminum thin film by atmospheric-pressure plasma technology (APPT) with varied substrate temperature (was treated at 100℃ , 150℃, and 200℃ respectively). Than we adopted 60 times and flow 1 sccm parameters to compare with different silicon oxide dielectrics.

Finally, all top contact electrode were deposited 300 nm thick aluminum layer defined with shadow mask by thermal coater system. The active region pad of all capacitors was diameter 200 μm .

2.3 Deposition of silicon oxide dielectric under room temperature on amorphous silicon metal insulator metal (a-Si MIM) structure

In this scenario, we purpose to deposit silicon oxide dielectric on the bottom contact electrode metal by atmospheric-pressure plasma technology. But silicon oxide was not deposited on the metal at room temperature. Consequently, we try to find solution to deposit amorphous silicon on the bottom electrode metal by electron-beam technique that was able to deposit on the metal at room temperature.

First, the n^+-Si wafer was used as the substrate, and was rinsed in the deionization water (DI water), and was then dipped in dilute HF solution (HF:DI water = 1:100)

that to remove the native oxide, the wafer was accomplished the RCA Clean procedure after, deposition of silicon dioxide was thermal kiln grown 500 nm thick on the top of n^+-Si substrate for isolation purpose. And deposited 300 nm aluminum as the bottom electrode.

Then, we deposited amorphous silicon thickness of 2 nm by electron-beam technique that in order to easeful grow silicon oxide by atmospheric-pressure plasma technology at room temperature.

Heats up the Tetraethoxy silane (TEOS) to 180℃ wae injected by nitrogen (50 %) and oxygen (50%) as carrier gases which was the deposition source of silicon oxide. The plasma power was established around 50 W with an appropriate scanning rate (sccm /cycle) to deposit silicon oxide on the top of n^+-Si substrate at room temperature under an atmospheric-pressure. The thickness of silicon oxide was increased with the scanning times (cycle/area) , silicon oxide was deposited on the aluminum thin film by atmospheric-pressure plasma technology (APPT) with varied scanning times (at 60, 80, 100, and 120 times respectively). Than we adopted flow 1 sccm parameter to compare with different silicon oxide dielectrics.

Finally, all top contact electrode were deposited 300 nm thick aluminum layer defined with shadow mask by thermal coater system. The active region pad of all capacitors was diameter 200 μm .

2.4 Fabricated processes of organic thin film transistor (OTFT)

In this scenario, we adopted flow 1 sccm and 60 times parameters to deposit insulator as gate dielectric layer on the organic thin film transistor structure by atmospheric-pressure plasma technology (APPT).

First, the n^+-Si wafer was used as the substrate, and was rinsed in the deionization water (DI water), and was then dipped in dilute HF solution (HF:DI water = 1:100) that to remove the native oxide, the wafer was accomplished the RCA Clean procedure after, deposition of silicon dioxide was thermal kiln grown 500 nm thick on the top of n^+-Si substrate for isolation purpose. The bottom contact structure was adopted to fabricate organic thin film transistor. That the structure of organic thin-film transistor. And deposited 50 nm thick aluminum layer as the gate electrode by lift-off method. The aluminum layer was deposited by thermal coater and silicon oxide deposited by

atmospheric-pressure plasma technology (APPT) at 150℃ under an atmospheric pressure with scanning 60 times was used as gate insulator. Source/ Drain electrodes with 50 nm thick nickel layer were deposited by electron-beam technique. The active layer used in this study was pentacene (obtained from Aldrich Co., Ltd.) which was evaporated by thermal coater. During deposition of pentacene active layer, the substrate was heated to 70℃ at power 17 W in a pressure chamber of around $1x10^{-6}$ Torr.

2.5 Characteristic measurement of devices

Capacitance-Voltage (C-V) characteristic diagrams were analyzed at 1MHz by HP 4284A precision LCR meter parameter and the characteristic curves of Current-Voltage (I-V) were measured with semiconductor parameter analyzer by HP 4156. All measurements were carried out at room temperature in an air atmosphere.

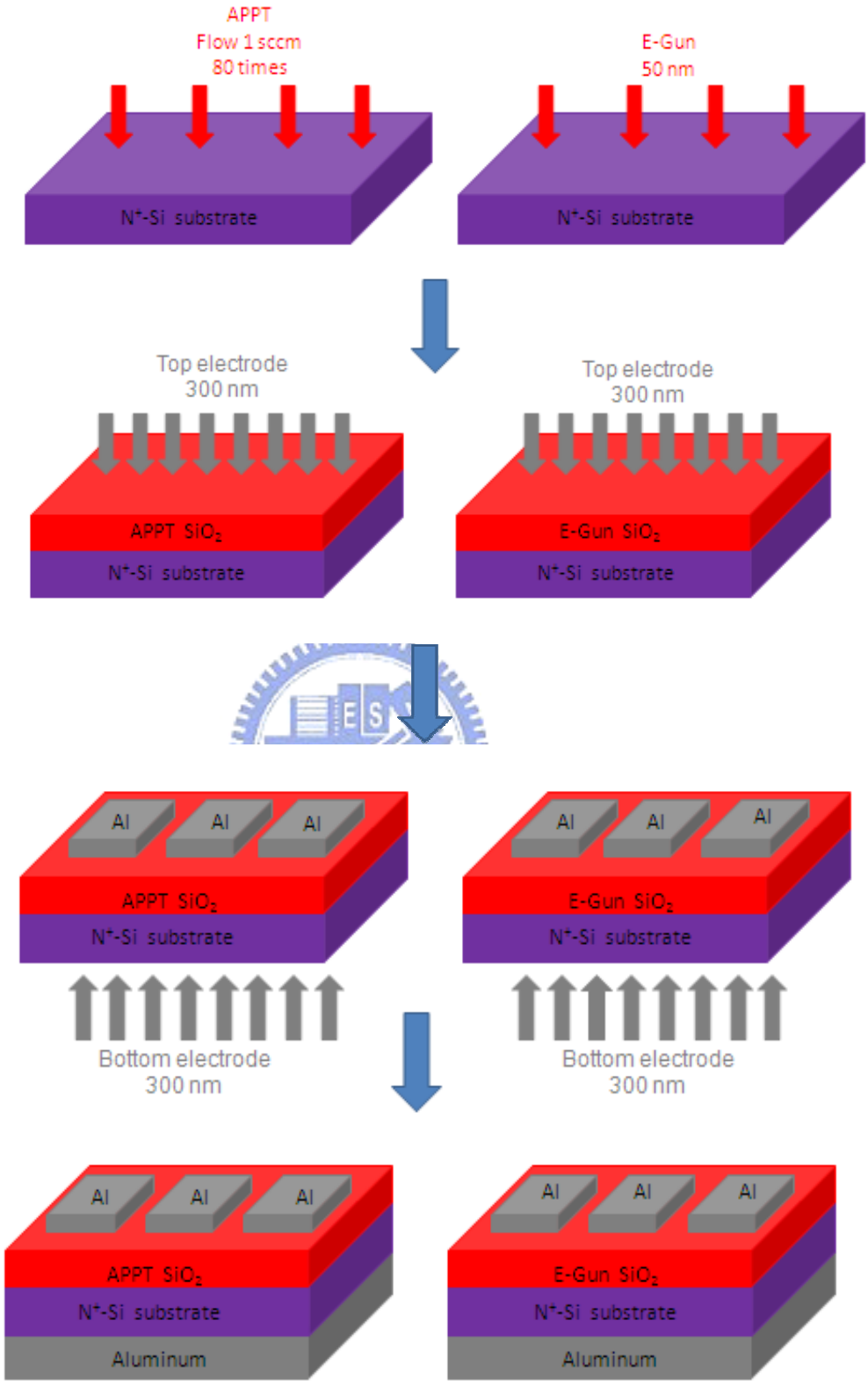
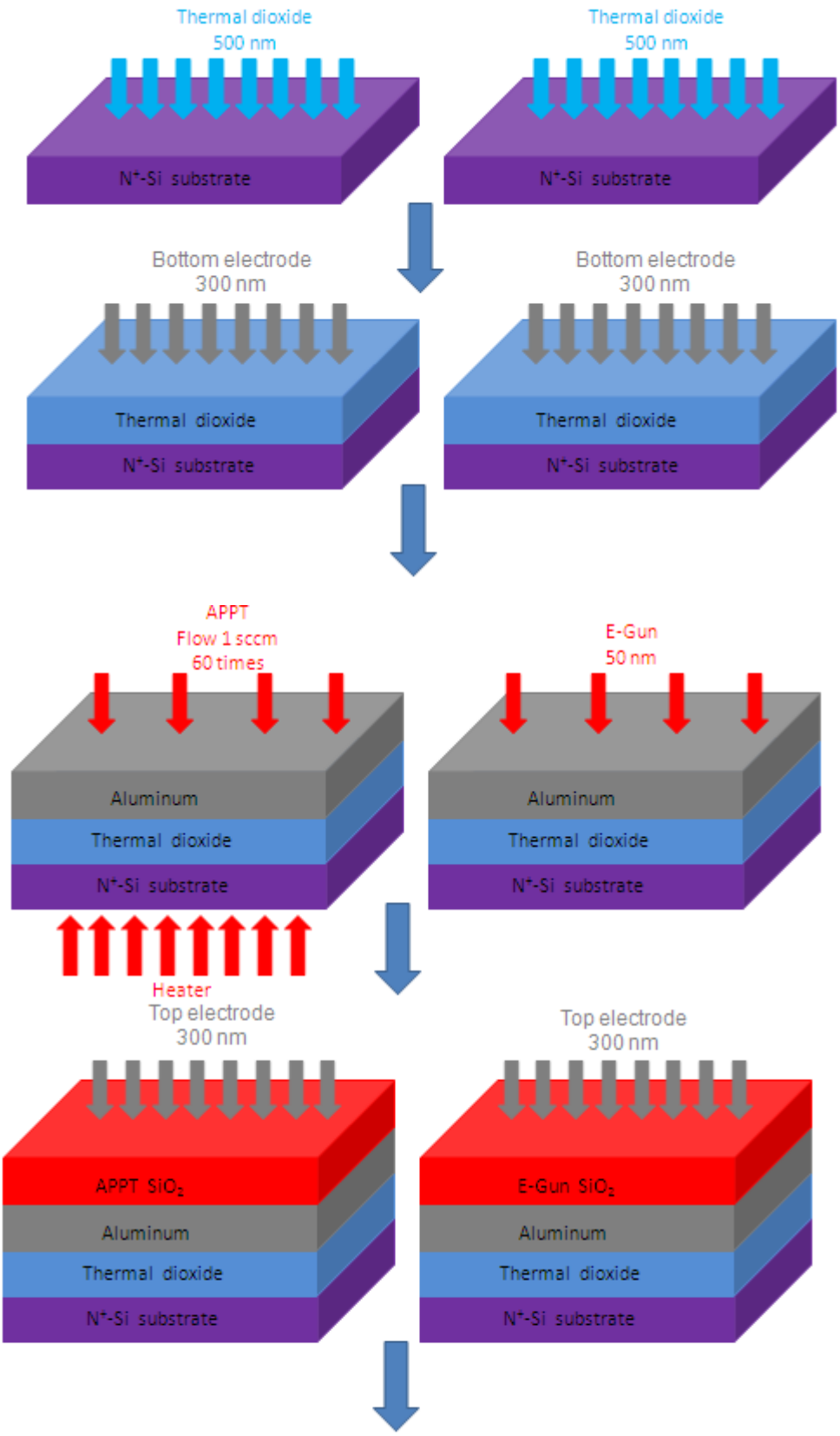


Figure 2-1: Fabrication flow of metal insulator semiconductor (MIS).


Thermal dioxide
500 nm
Thermal dioxide
500 nm
N+-Si substrate
N+-Si substrate
Bottom electrode
300 nm
Bottom electrode
300 nm
Thermal dioxide
N+-Si substrate
Thermal dioxide
N+-Si substrate
APPT
Flow 1 sccm
60 times
E-Gun
50 nm
Aluminum
Thermal dioxide
N+-Si substrate
Aluminum
Thermal dioxide
N+-Si substrate
Heater
Top electrode
300 nm
Top electrode
300 nm
APPT SiO2
Aluminum
Thermal dioxide
N+-Si substrate
E-Gun SiO2
Aluminum
Thermal dioxide
N+-Si substrate

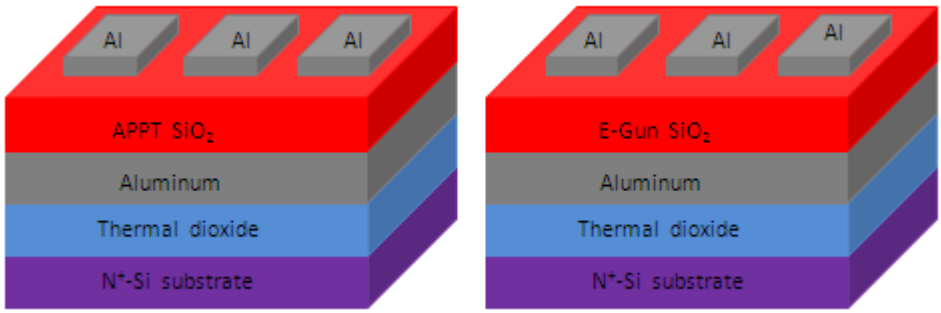


Figure 2-2: Fabrication flow of metal insulator metal (MIM).

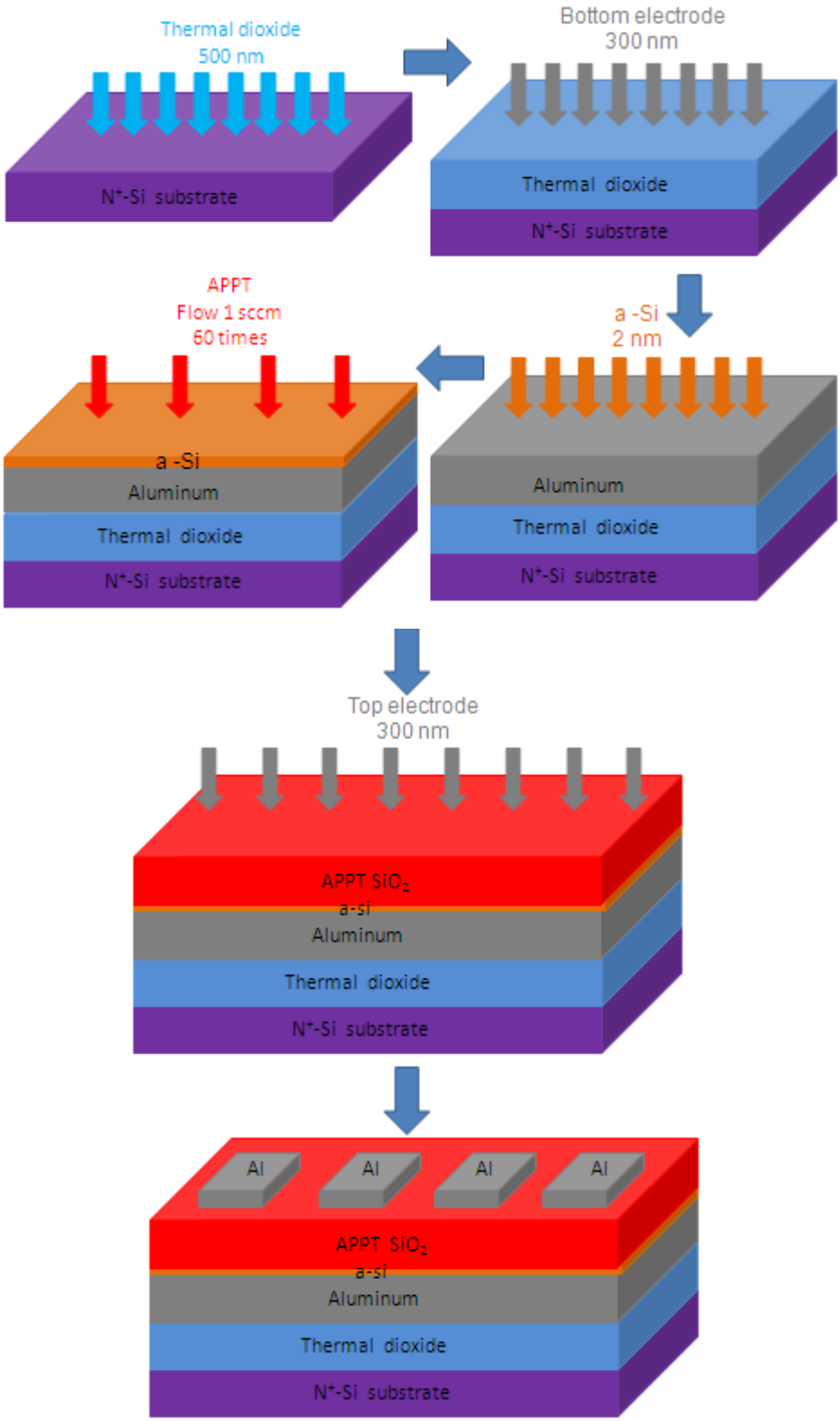
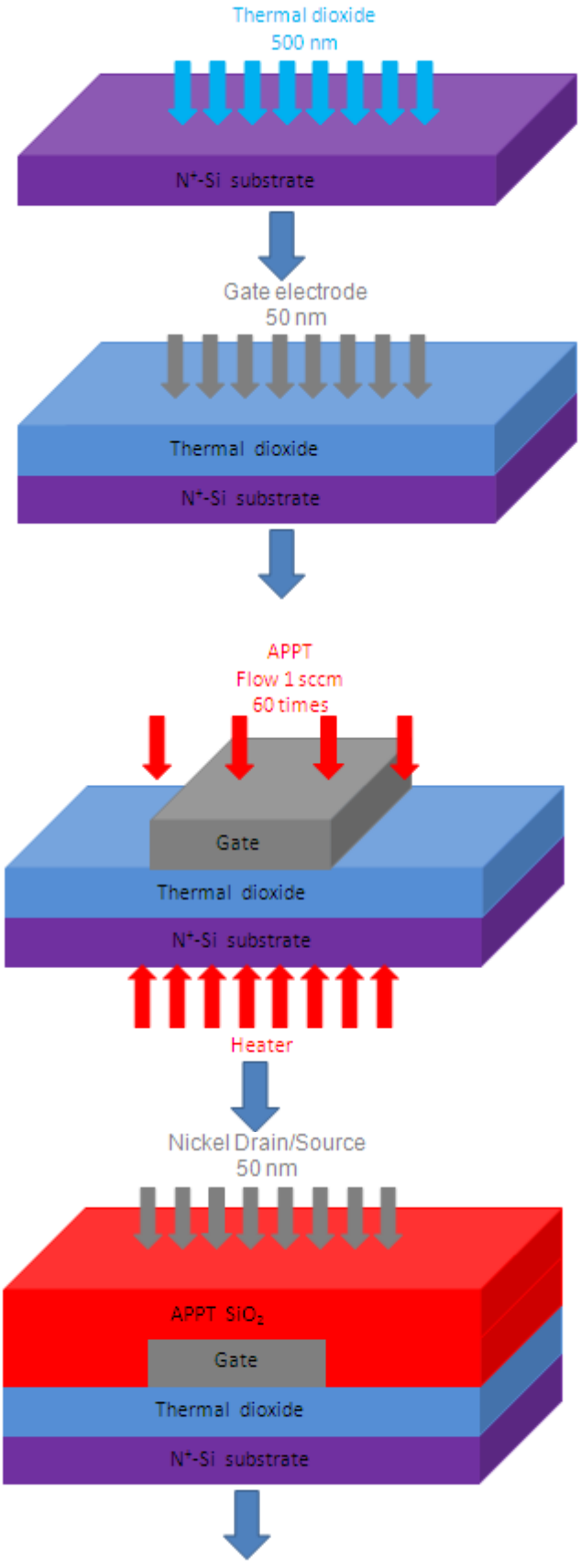


Figure 2-3: Fabrication flow of amorphous silicon metal insulator metal (a-Si MIM).


Thermal dioxide
500 nm
N+-Si substrate
Gate electrode
50 nm
Thermal dioxide
N+-Si substrate
APPT
Flow 1 sccm
60 times
Gate
Thermal dioxide
N+-Si substrate
Heater
Nickel Drain/Source
50 nm
APPT SiO2
Gate
Thermal dioxide
N+-Si substrate

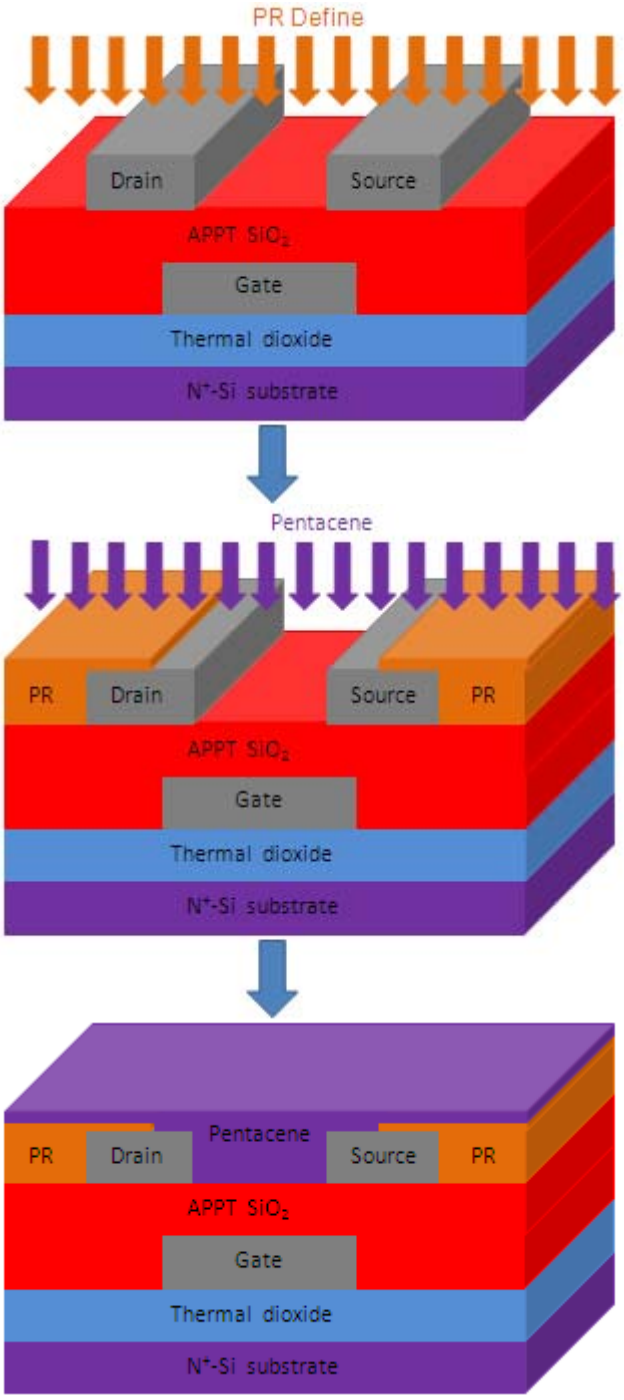


Figure 2-4: Fabrication flow of organic thin film transistor (OTFT).

Chapter 3

Results and Discussion

3.1 Silicon oxide dielectric layer quality analysis and appraisal

3.1.1 MIS

We use to two different systems deposited silicon oxide as insulator dielectric layer which to test insulator quality of handicapper convenient for metal insulator semiconductor (MIS) structure. Sample A and sample B was APPT and E-Gun deposition respectively.

The C-V characterization of sample A and sample B was shown in Figure 3-1. EOT (Equivalent Oxide Thickness) calculated from capacitance of Figure 3-1(a) for sample A and sample B was about 8.277 nm and 10.919 nm respectively. The expression of EOT is very popular for the high dielectric constant gate insulator of CMOS device [16]. Because there are many kinds of insulator materials with different dielectric constants, EOT could be considered as a standard for a comparison of the gate insulator controllability to channel accumulation. The calculation of EOT is presented at equation (3-1). The circular area of top electrode in this study was diameter 200 μm .

$$EOT = \frac{3.9 \times 8.85 \times 10^{-4} \times \text{device area}}{\text{Capacitance}} \qquad (3\text{-}1)$$

The relationship between I-V of sample A and sample B were showed in Figure 3-1(b). The leakage current of sample B is higher than sample A at 1.5V bias voltage. However, because we want to know the effect of silicon oxide deposited by e-gun and SAPPT at different physical thickness, we try to make the comparison under the same electric field obtained from the voltage divided by the EOT (E_{EOT}= Bias Voltage / EOT). When two OTFT devices are biased at the same E_{EOT}, which means the same charges were accumulated at both device's channels. In this case, when the E_{EOT} was 1.5 MV/cm, leakage current of sample B is higher than sample A. Show figure 3-1 (c).

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3.1.2 MIM

We purpose to deposit silicon oxide dielectric on the bottom contact electrode metal by atmospheric-pressure plasma technology. But silicon oxide was not deposited on the metal at room temperature. Consequently, we try to find solution to heat up to the n^+-Si substrate that was able to deposit on the metal. Silicon oxide of sample D ~ F was deposited by SAPPT on the bottom electrode surface at different substrate temperature at 100℃, 150℃, and 200℃. The horizontal axis and vertical axis of Figure 3-2 represent the swept voltage set and the value of capacitance respectively. The values of EOT calculated from Figure 3-2 (a) of sample D, E, and F were about 20.198 nm, 23.836 nm, and 28.496 nm respectively, so we could find that the deposition rate was increased with the substrate temperature. However, the capacitance value of sample C couldn't be measured due to the high leakage current. The I-V characterization of sample C shows almost short circuit current, which implies the deposition rate was almost zero when we deposited silicon oxide on the surface of aluminum at room temperature. This situation is very different to that by deposited on silicon substrate at room temperature. These results revealed that the surface material is a main factor for SAPPT method to deposit silicon oxide at room temperature. The leakage current density versus electric field was shown in Figure 3-3. The leakage current of sample E and sample E-Gun is about 9×10^{-8} A/cm^2 and 2×10^{-7} A/cm^2 at 0.5 MV/cm respectively. The quality of silicon oxide deposited by SAPPT at 150℃ is better than that deposited by e-gun.

3.1.3 a-Si MIM

We purpose to deposit silicon oxide dielectric on the bottom contact electrode metal by atmospheric-pressure plasma technology. But silicon oxide was not deposited on the metal at room temperature. Consequently, we try to find solution to deposit amorphous silicon on the bottom electrode metal by electron-beam technique that was able to deposit on the metal at room temperature. Silicon oxide was deposited on the aluminum thin film by atmospheric-pressure plasma technology (APPT) with varied scanning times at 60, 80, 100, and 120 times respectively. Than we adopted flow 1 sccm parameter to compare with different silicon oxide dielectrics.

The horizontal axis and vertical axis of Figure3-4 represent the swept voltage set and the value of capacitance respectively. The values of EOT calculated from Figure3-4

(a) of sample 60, 80, 100, and 120 times were about 18.072 nm, 19.715 nm, 24.643 nm and 27.108 nm respectively,

The leakage current density versus electric field was shown in Figure 3-5. The leakage current of sample E-Gun is about 2×10^{-7} A/cm^2 at 0.5 MV/cm respectively. The quality of silicon oxide deposited by e-gun is better than that deposited by SAPPT.

3.2 Determination of Threshold voltage and Mobility

The linear regime field effect mobility can be obtained by the calculation described below. At low V_D, I_D increases linearly with V_D (linear regime) and is approximately determined by the following equation:

$$I_D = \frac{W\mu_n C_{ox}}{2L}\left[2(V_G + V_T)V_D - V^2{}_D\right] \qquad \textbf{(3-2)}$$

where L is the channel length, W is the channel width, C_{ox} is the capacitance per unit area of the insulating layer, V_T is the threshold voltage, and μ is the field effect mobility, which can be calculated in the linear regime from the transconductance,

$$G_m = \frac{\partial I_D}{\partial V_G} = \frac{Z}{L}\mu_n C_{ox} V_D \qquad \textbf{(3-3)}$$

by plotting I_D versus V_G at a constant low V_D, with $-V_D$ <<-(V_G - V_T), and equating the value of the slope of this plot to Gm, then find Gm_{max} which can gain the value of threshold voltage (V_T) and linear mobility. For the known values included C_{ox}, V_T, and W/L, the value of saturation mobility can be obtained from equation (3-4)

$$I_D(sat) = \frac{W\mu_n C_{ox}}{2L}(V_G + V_T)^2 \qquad \textbf{(3-4)}$$

3.3 OTFT electric characteristics analysis and discussion

At this part, SAPPT method was adopted to fabricate the gate insulator of OTFT with the parameters of sample E discussed. Process temperature and throughput are the two main considerations for this selection. First, most plastic substrates could not sustain temperature higher than 200℃. The process condition of sample E (150℃) provides a suitable thermal buffer for flexible electronic device fabrication. Secondly, the deposition rate is increased with the raised process temperature and the condition of sample E has a relatively higher deposition rate than sample D. The condition of sample

E is still a low temperature process and can get a better deposition rate for throughput and still maintain good quality. The drain current (I_D) versus drain-source voltage (V_{DS}) at varied gate voltages (V_{GS}) was shown in Figure 3-8(a). The output characteristic of I_D versus V_{GS} was shown in Figure 3-8(b). The carrier mobility was calculated at the saturation region with following equation:

$$I_D = \frac{W}{2L} C_i \mu (V_G - V_T)^2 \quad (3\text{-}5)$$

C*i* is the capacitance per unit area of gate insulator in equation. (3-5). It correspond to a device with channel width W = 200 μm and length L = 50 μm. The saturation mobility and the threshold voltage of the OTFT were about 0.066 cm^2/V-s and - 2 V respectively. The OTFT could be operated at the voltage below -5 V due to the EOT of about 14 nm. However, the mobility of this device was lower than some other reports [17, 18]. We suggested that three possible reasons could explain this phenomenon. First, since we fabricated the OTFT device with bottom contact structure [2], the grain size of the active layer would be affected by the roughness of the electrodes of source and drain. Secondly, the roughness of aluminum gate electrode was about 8.7 nm (the corresponding AFM analysis was shown in Figure 3-14(a)), the roughness of the silicon oxide deposited by SAPPT on the top of aluminum gate electrode was around 10.8 nm (see Figure 3-14(b)). Third, the contact angle of gate insulator with DI water was about 20 degree and figure 3-15 shows hydrophilic characteristic at the surface of the silicon oxide. Roughness and hydrophilic characteristic might be the main factors to influence the deposition of pentacene and then decrease the mobility of OTFT devices. [18-20].

3.4 Leakage current characteristic of OTFT discussion in various structures

We can see leakage current 3×10^{-7} A at drain/source voltage and gate voltage was zero and -7 respectively. In figure 3-8(b). Consequently, we to discuss for leakage current in the different structure. View from figure 3-9 to figure 3-13.

First, we compare with define pentacene region and not define pentacene region in figure 3-9. Result in leakage current of not define pentacene region is higher than define pentacene region. Because of not define pentacene region have large field that account to more leakage current. And we adopt two materials to experiment, we obtain the same result. Hence, define pentacene region is important for OTFT divice that can be

effective reduce leakage current.

We compare with have HMDS and not have HMDS in figure 3-11. Result in leakage current of have HMDS is higher than not have HMDS. Because of HMDS can be increase pentacene grain size and increase pentacene conductivity. Therefore, we found have HMDS not only the increase conductive merit but also increases leakage the current shortcoming. In figure 3-12 and figure 3-13, leakage current of not define pentacene region is higher than define pentacene region and leakage current of have pentacene is higher than not have pentacene.

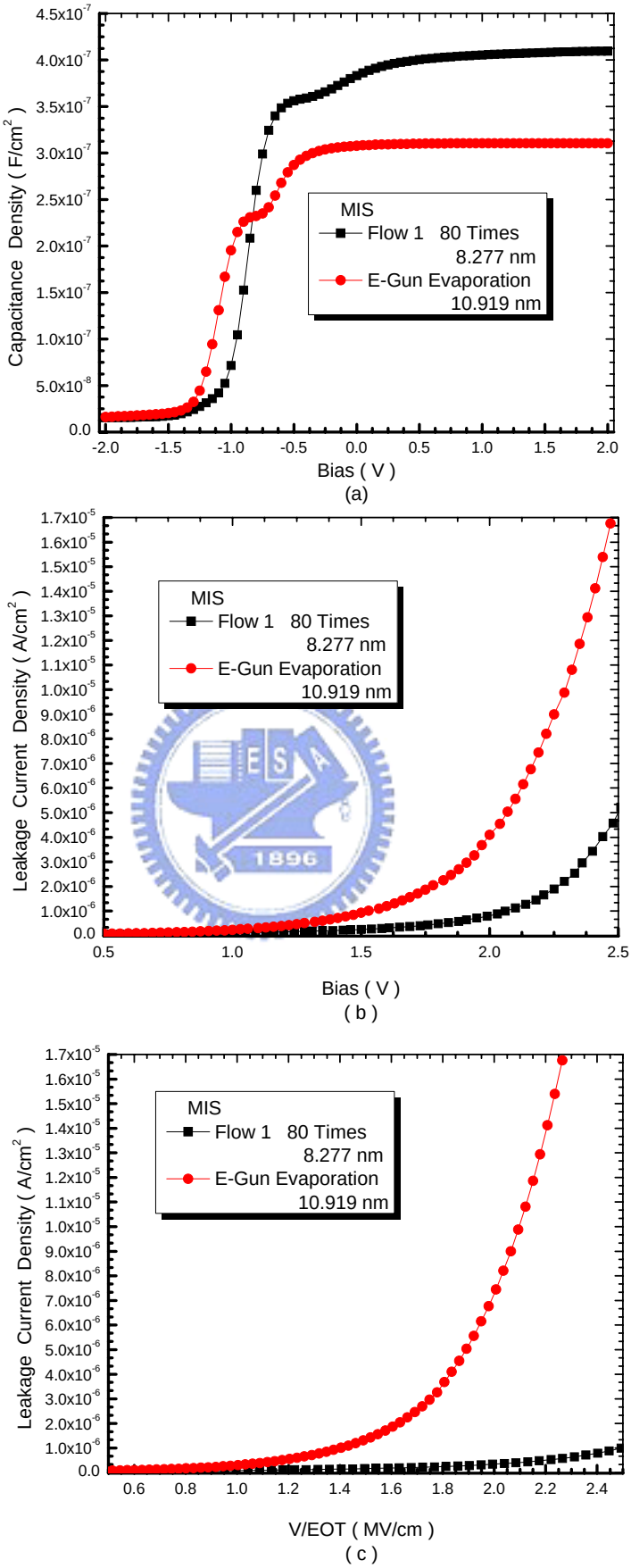
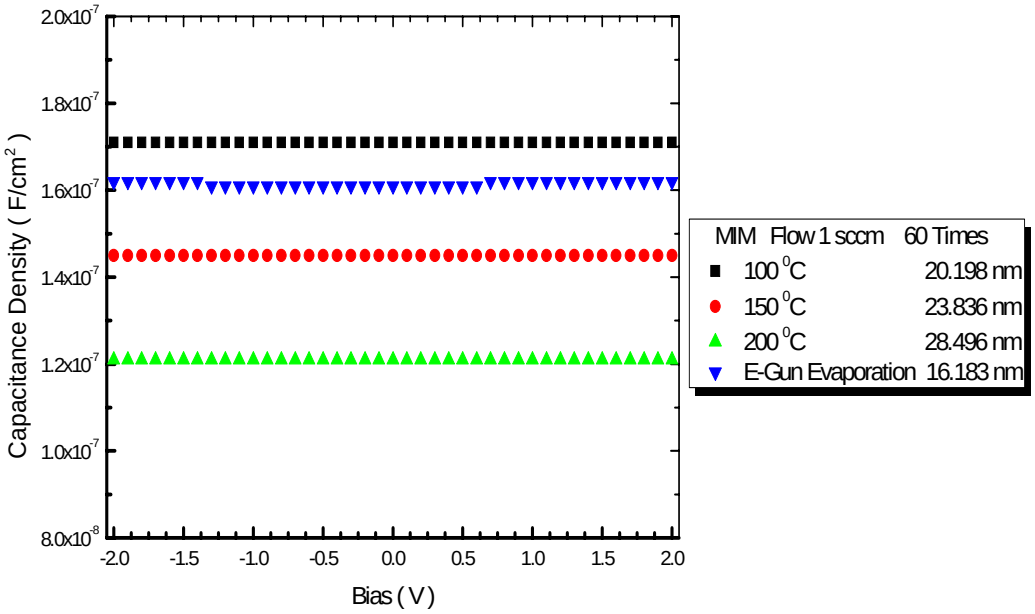
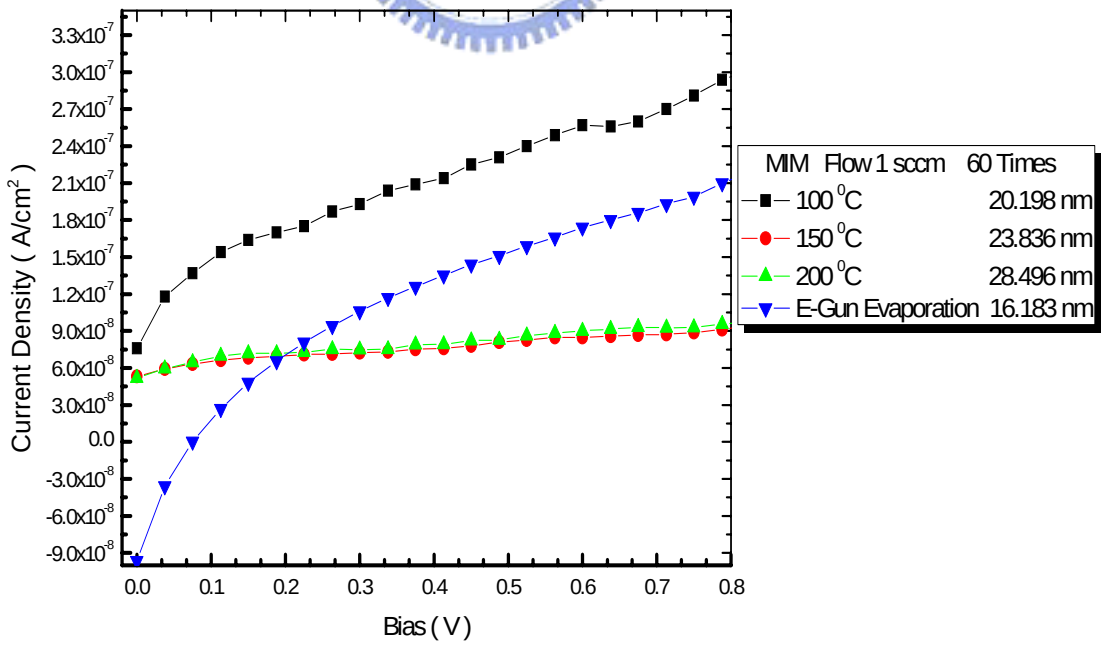


Figure 3-1: The electronic characterization of MIS.



(a)



(b)

Figure 3-2: The electronic characterization of MIM for C-V and I-V.

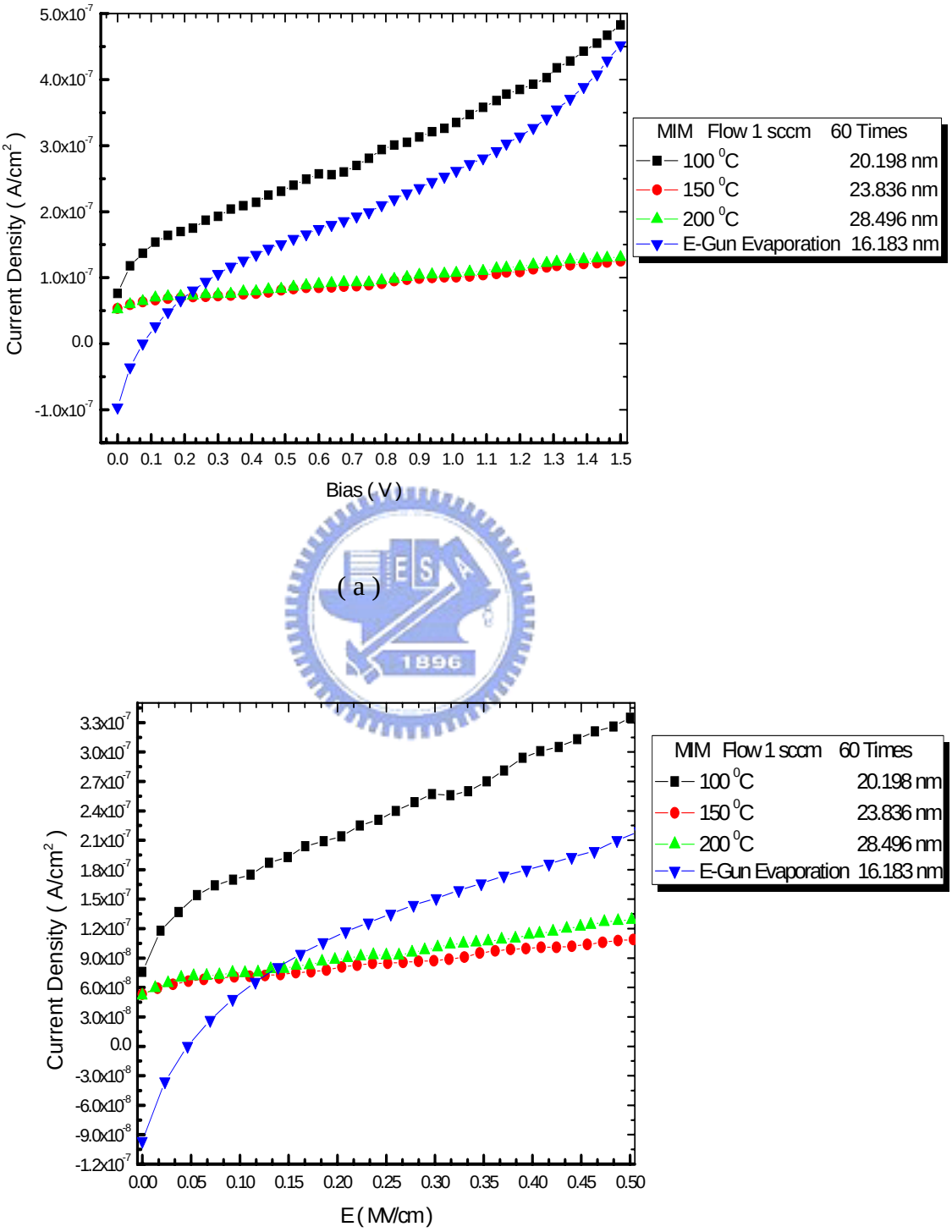
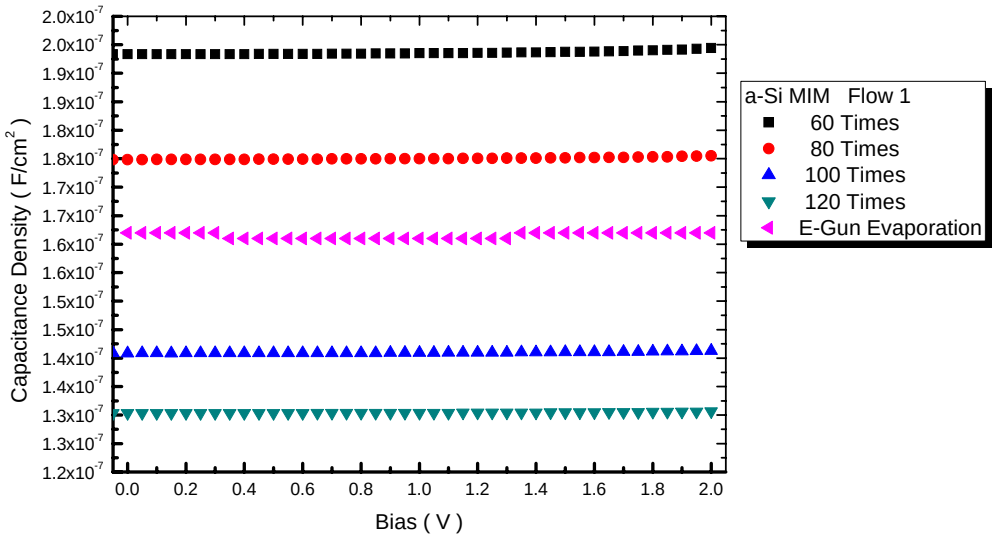
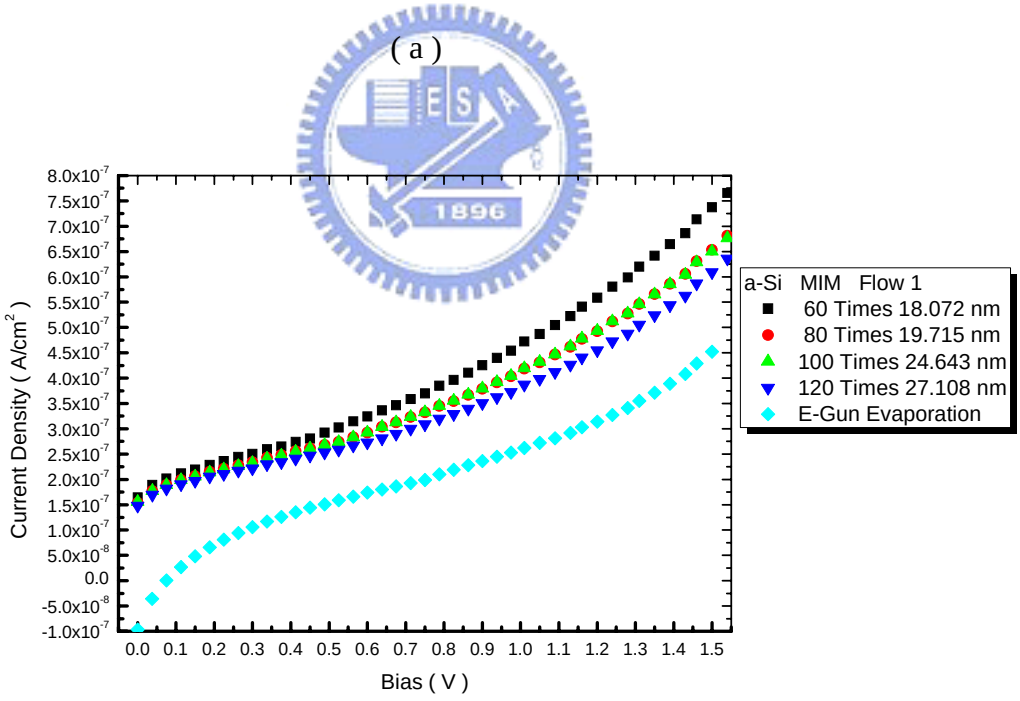


Figure 3-3: The electronic characterization of MIM for I-V and I-E.

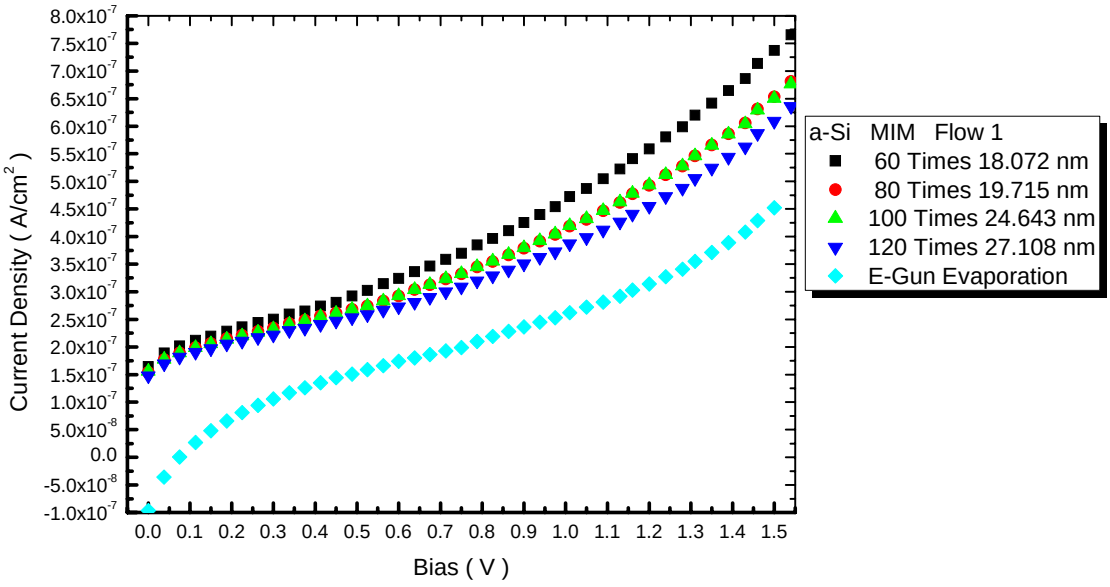


(a)

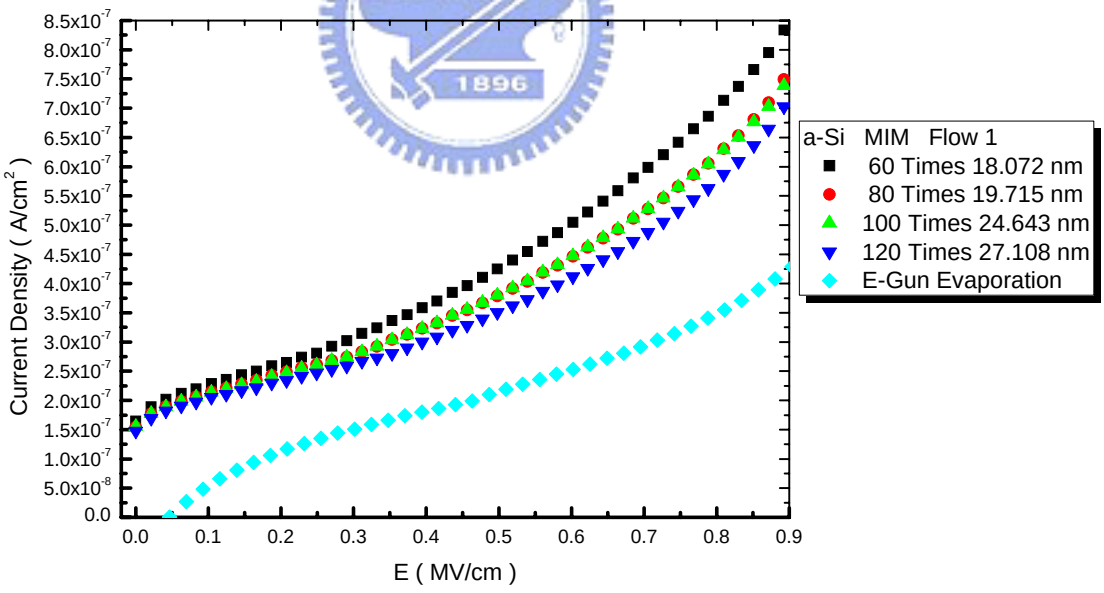


(b)

Figure 3-4: The electronic characterization of a-Si MIM for C-V and I-V.

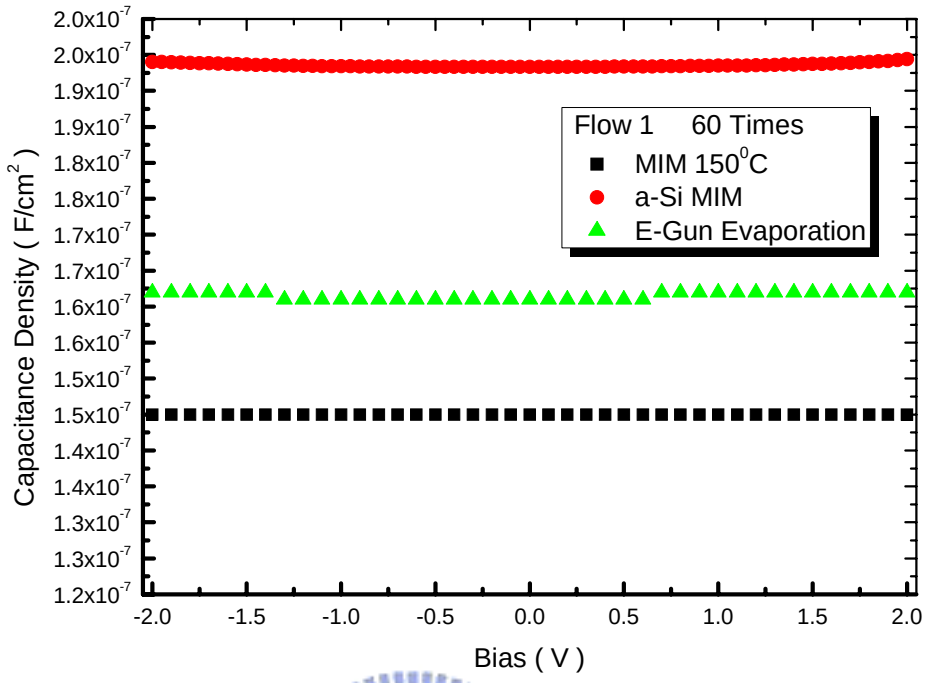


(a)

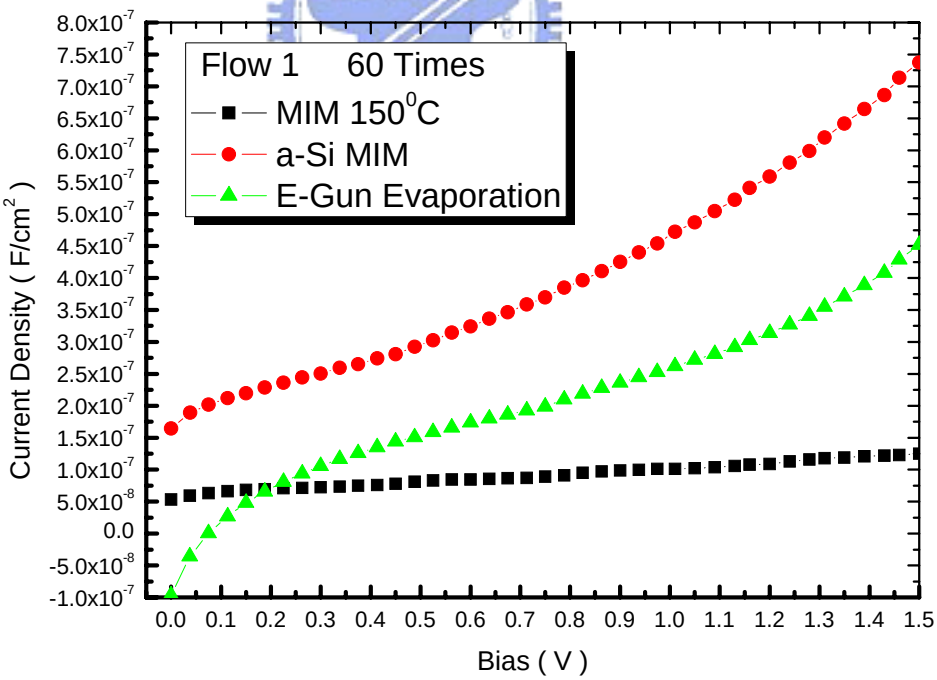


(b)

Figure 3-5: The electronic characterization of a-Si MIM for I-V and I-E.

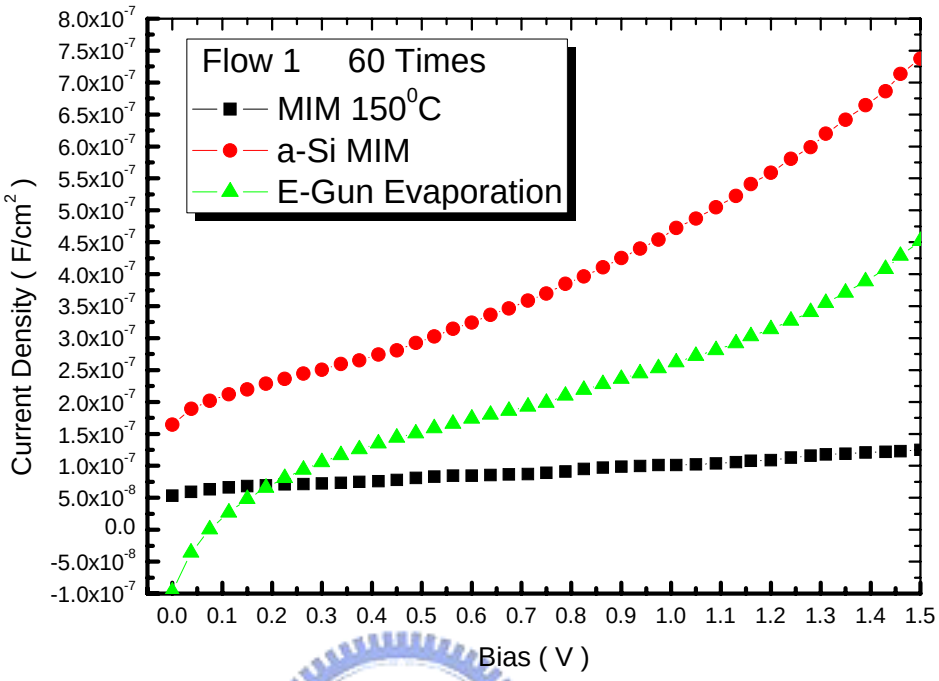


(a)

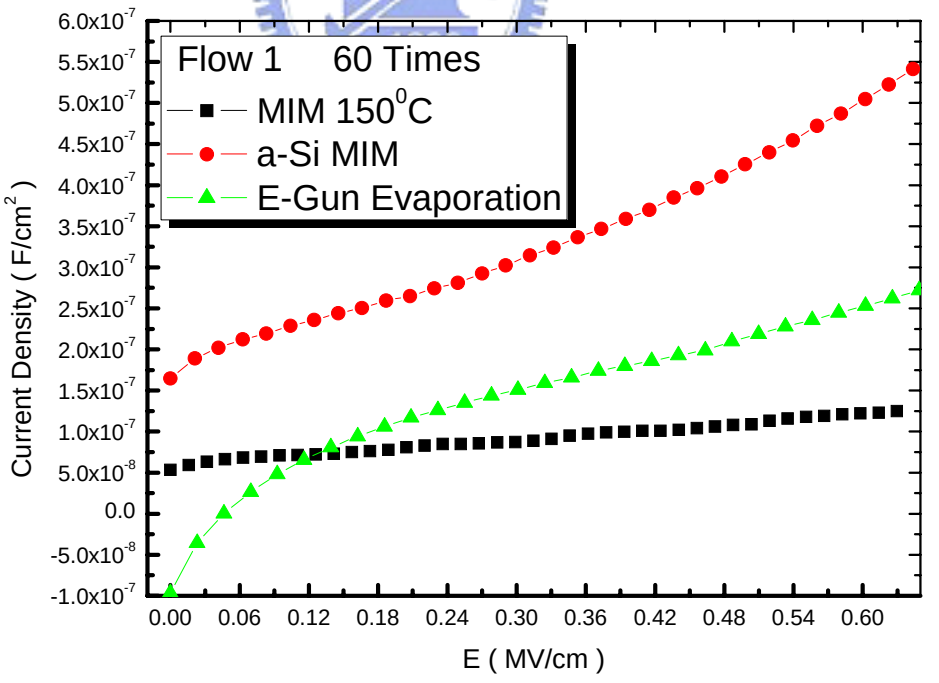


(b)

Figure 3-6: The electronic characterization of MIM, a-Si MIM and E-Gun for C-V and I-V.

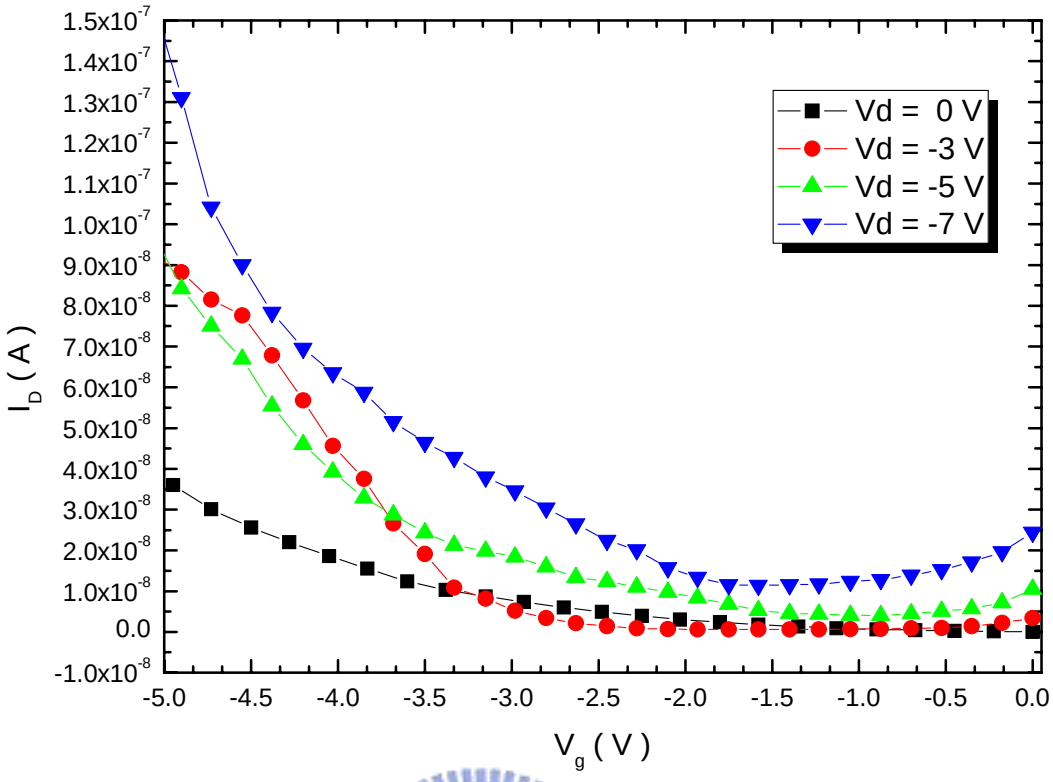


(a)

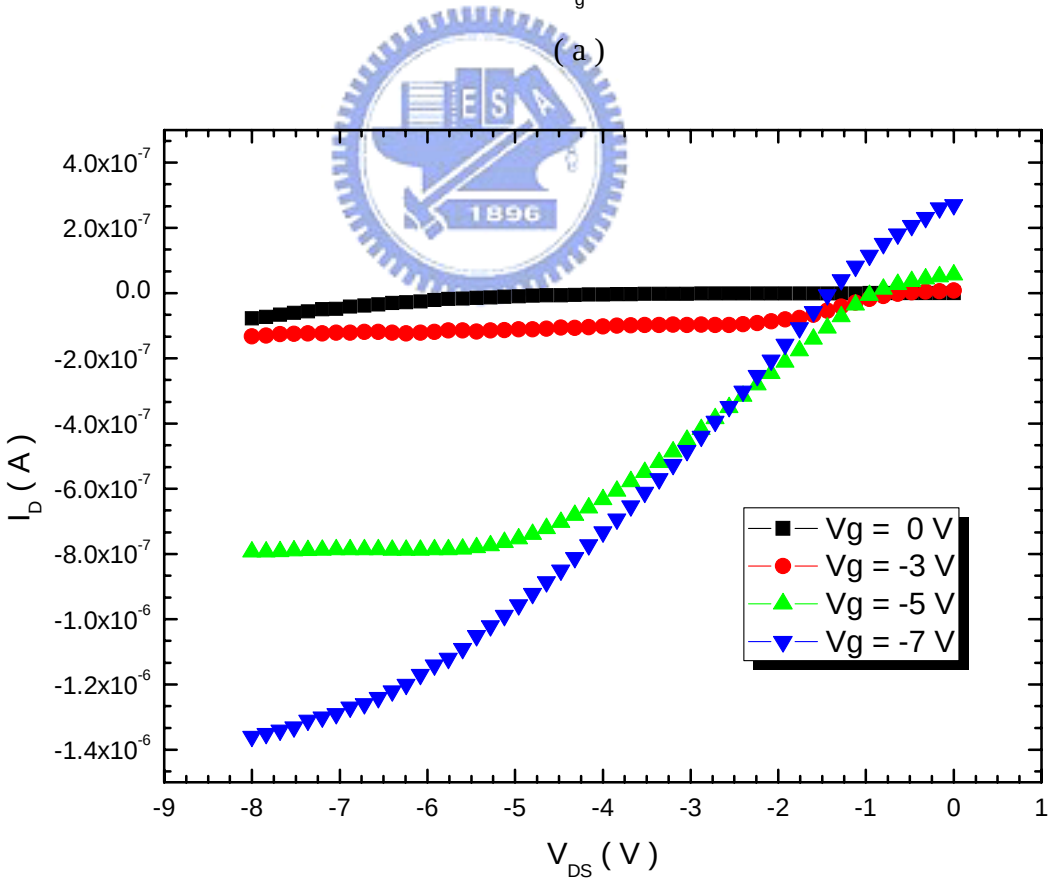


(b)

Figure 3-7: The electronic characterization of MIM, a-Si MIM and E-Gun for I-V and I-E.

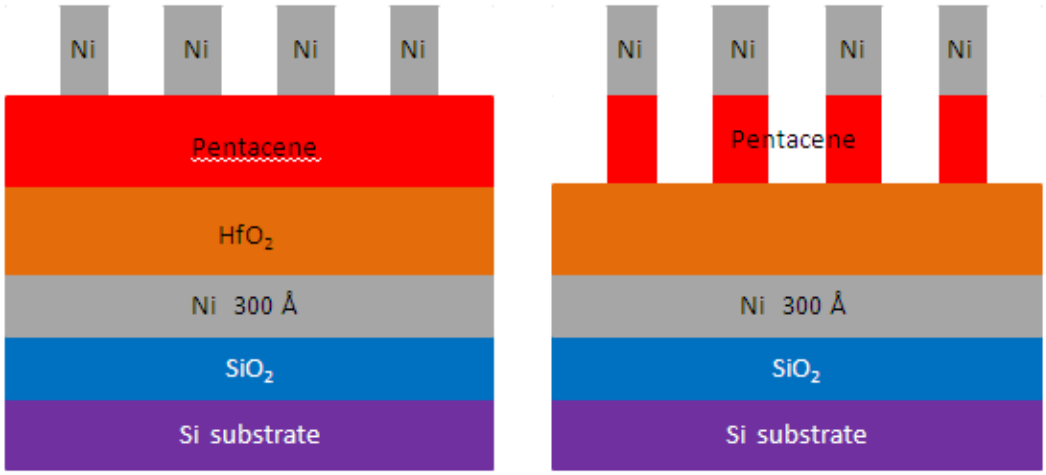


(a)



(b)

Figure 3-8: The electronic characterization of OTFT for I_d-V_g and I_d-V_d.



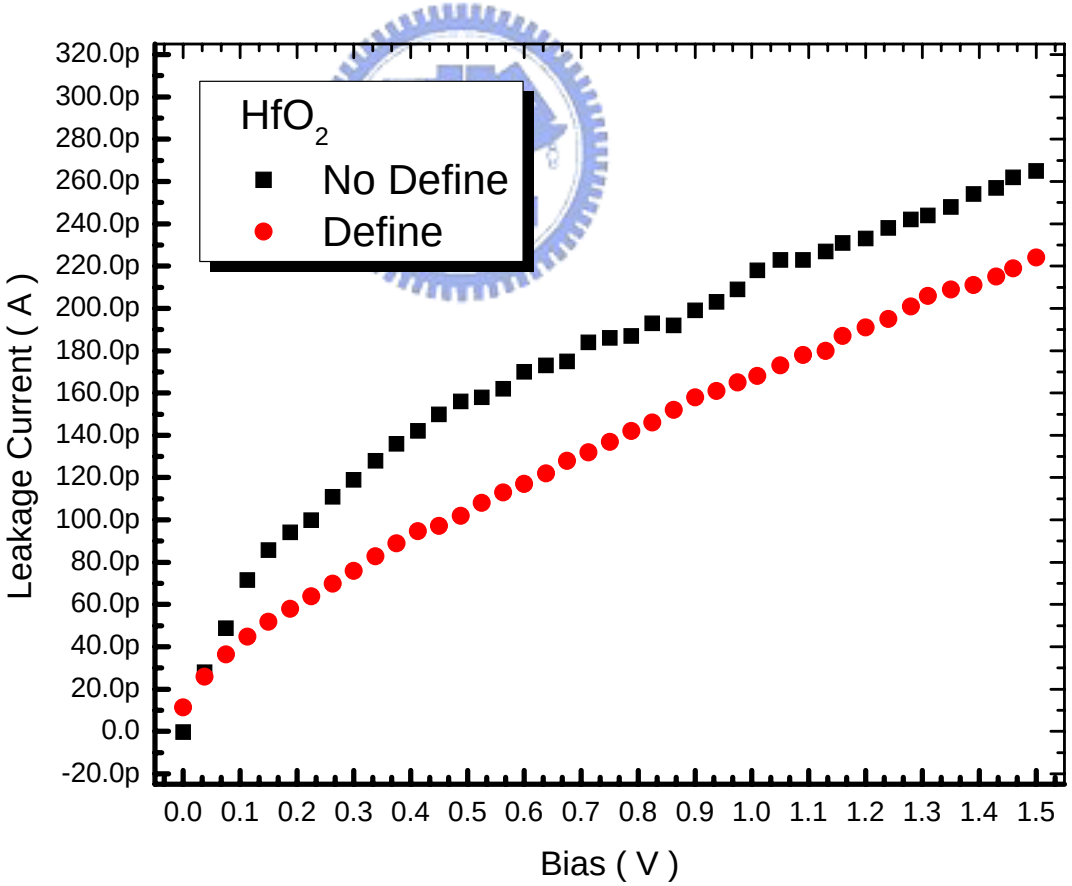
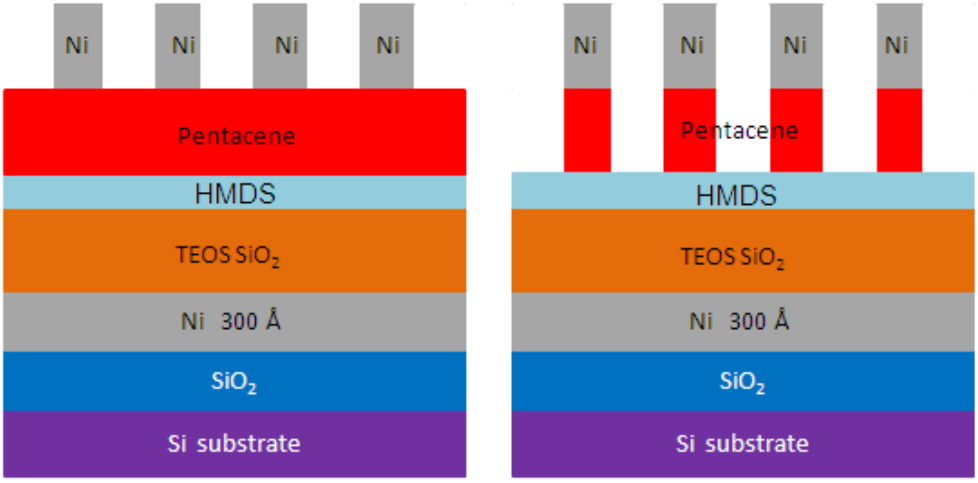


Figure 3-9: The electronic leakage current characterization of pentacene-HfO2 MIM for I-V.



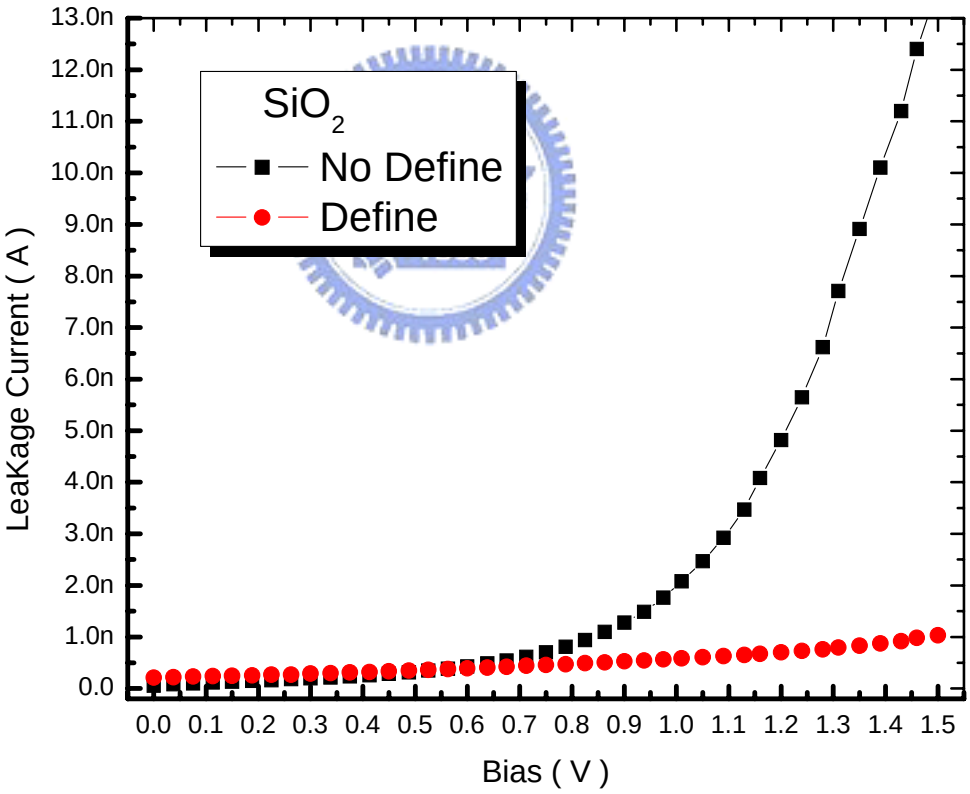
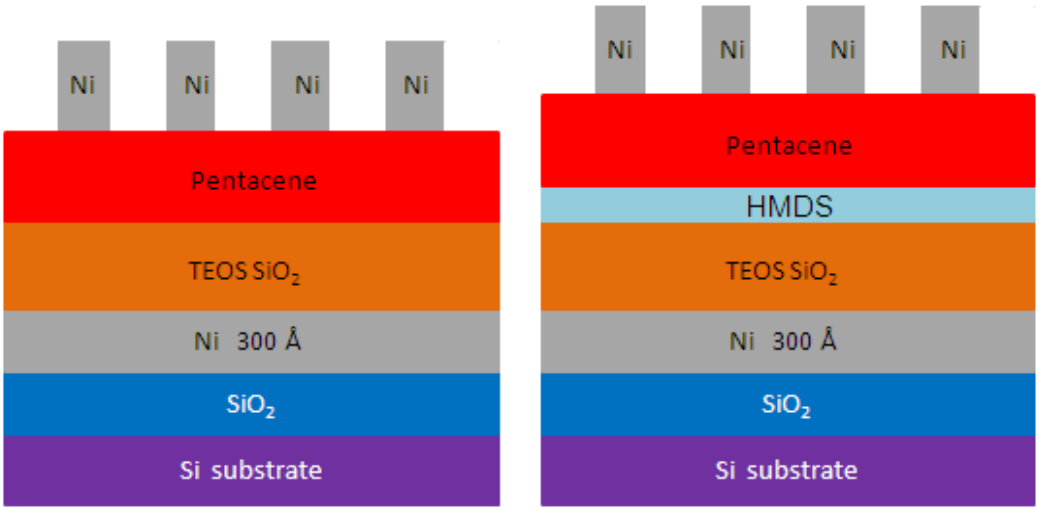


Figure 3-10: The electronic leakage current characterization of pentacene-SiO2 MIM for I-V.



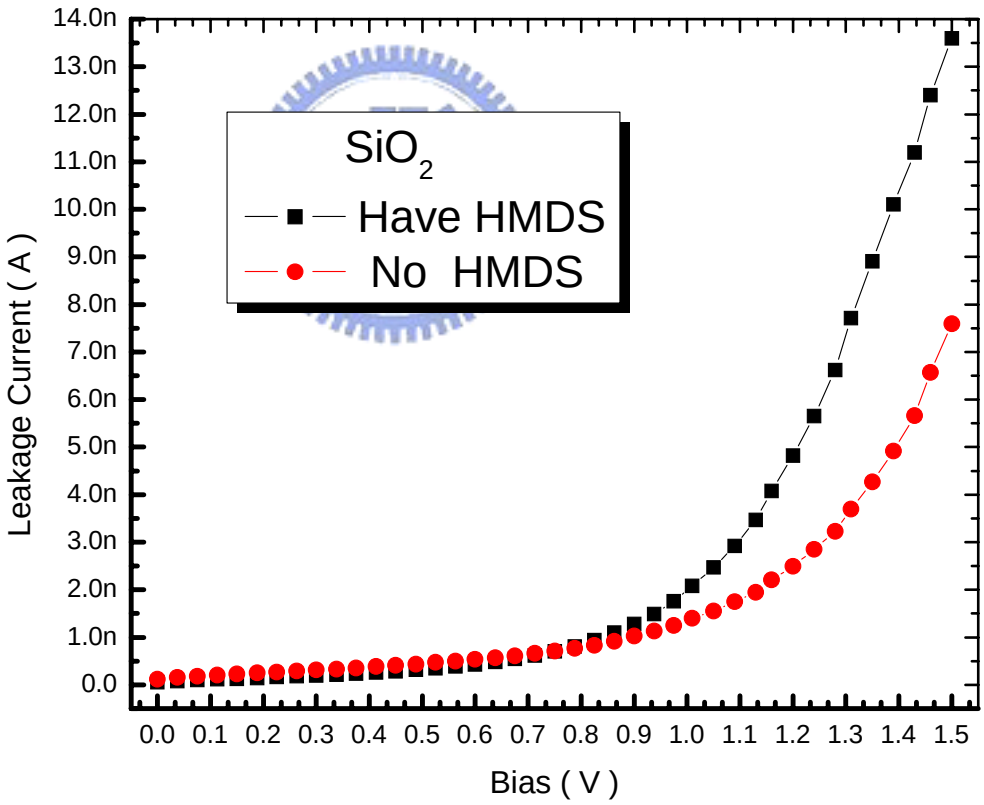
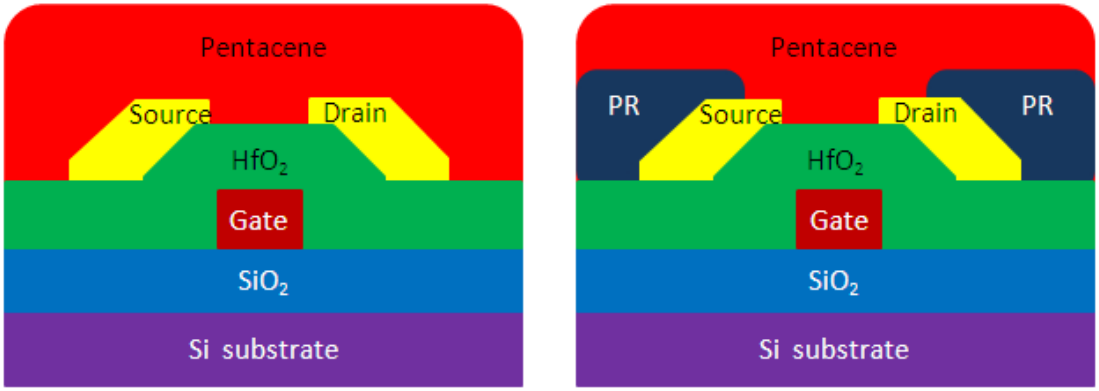


Figure 3-11: The electronic leakage current characterization of pentacene-SiO2 MIM for I-V.



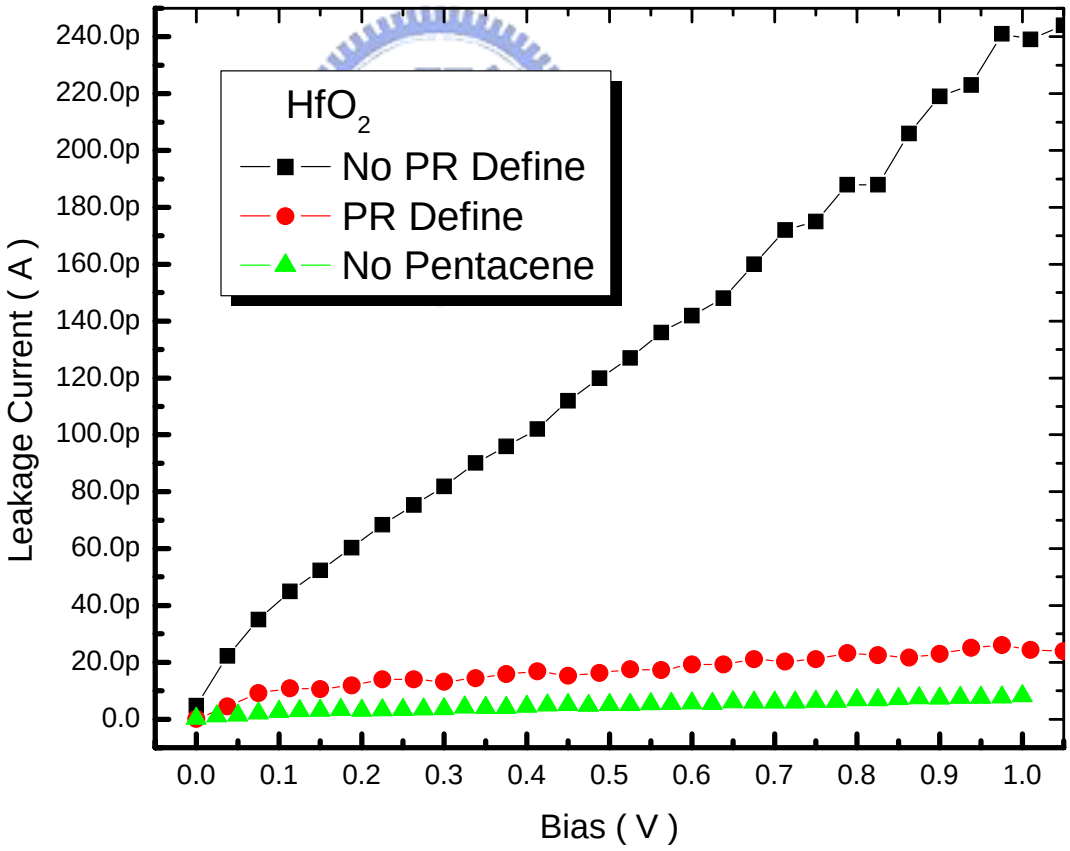
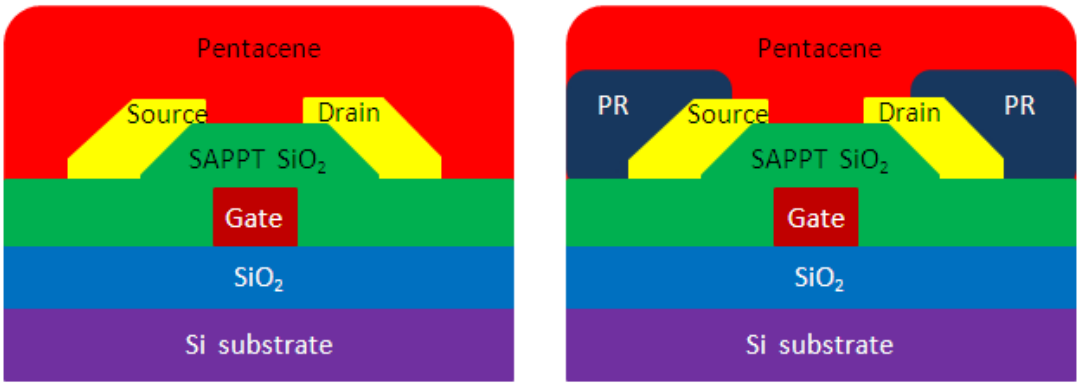


Figure 3-12: The electronic leakage current characterization of OTFT for HfO2.



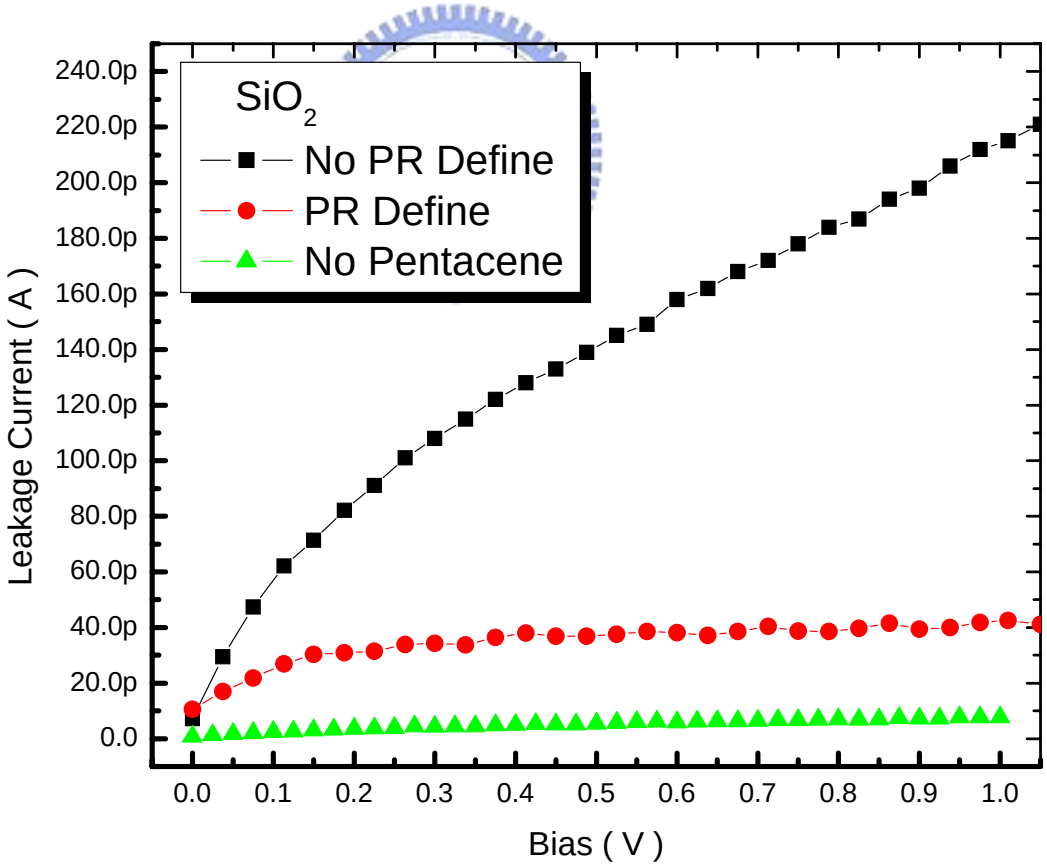


Figure 3-13: The electronic leakage current characterization of OTFT for SiO2.

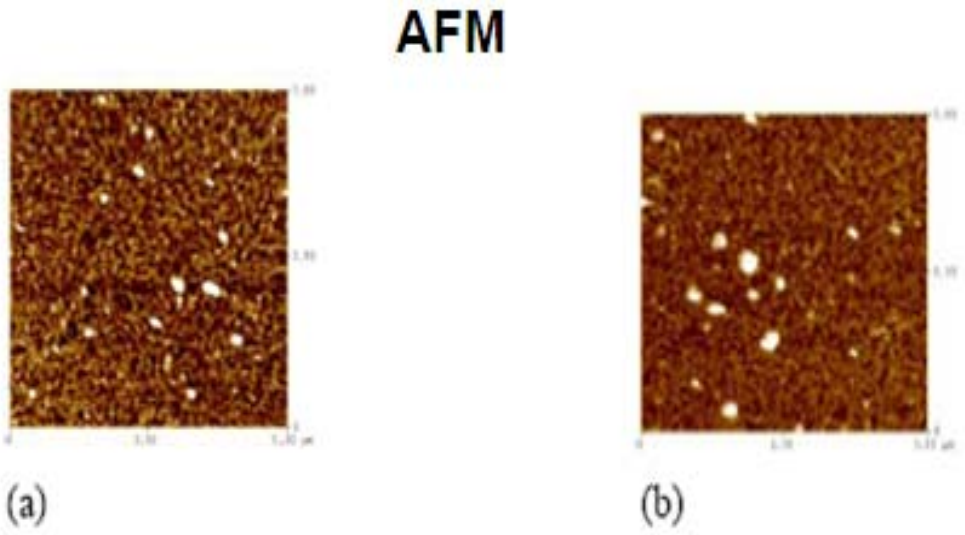


Figure 3-14:

(a) shows the AFM image of aluminum gate insulator with roughness about 8.7 nm.

(b) shows the AFM image silicon oxide deposited at 150℃ on the aluminum with the roughness around 10.8 nm.

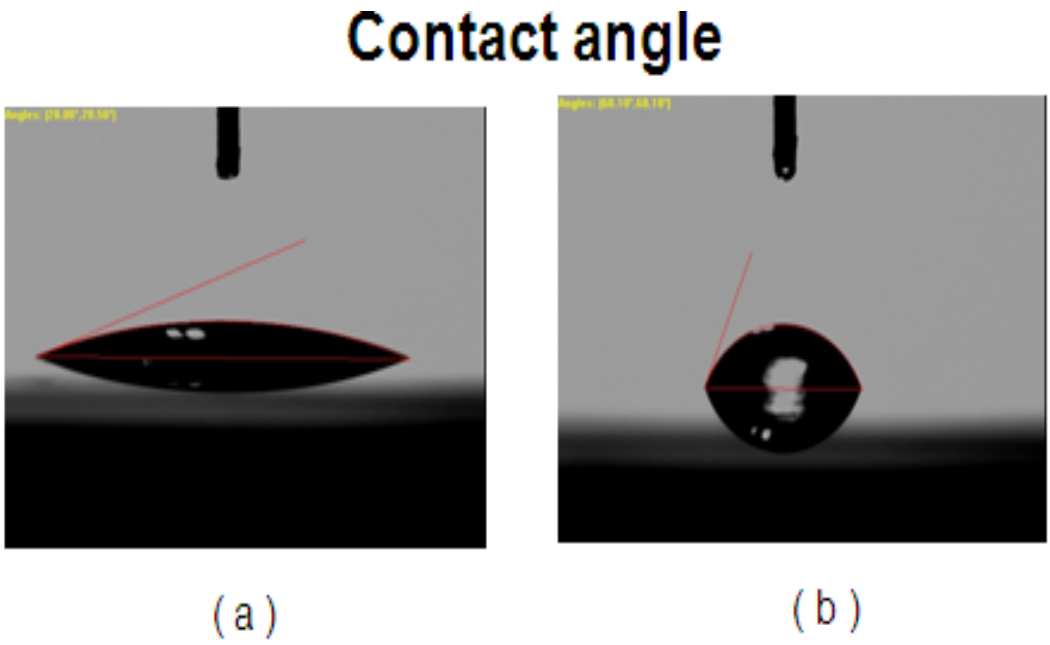


Figure 3-15:

(a) shows the contact angle image silicon oxide deposited at 150℃ on the aluminum with the angle around 20°.

(b) shows the contact angle image with HMDS the angle around 68.1°.

Chapter 4

Conclusion

4.1 Conclusion

From the experiment 3.1.1 and 3.1.2, we can know that the deposition rate of silicon oxide deposited by SAPPT at room temperature depend on the surface material where to deposit on. The leakage current of silicon oxide deposited by SAPPT at 150℃ (sample E) was about 9×10^{-8} A at 0.5 MV/cm which is around one order lower than that of the control sample G (E-gun deposition). Because sample E has better insulator property due to a higher deposition rate and suitable process temperature than other samples deposited by E-gun, its process condition was chosen to fabricate OTFT device. OTFT with the gate insulator deposited by scanning atmospheric-pressure technology was successfully demonstrated in experiment 3.1.3. The highest process temperature in the fabrication of OTFT device was 150℃. The operation voltage of this device is reduced to -5V due to the smaller EOT of 14 nm. Although the mobility of our device is lower than 0.1 cm^2/V-s. The reasons for low mobility may be caused by the surface roughness of gate electrode and the hydrophilic surface in SAPPT process.

In summary, we already fabricated successfully OTFT with good dielectric property by using SAPPT method and demonstrated that SAPPT is a suitable method to fabricate good dielectric for the applications of plastic substrate due to the low temperature process under an atmospheric pressure.

4.2 Future work

- Improves the organic thin film transistor performance on surface treatment by atmospheric pressure plasma technology.
- Change gate electrode metal from aluminum to nickel , tellingly reduce surface roughness enhance organic thin film transistor performance .
- Because Pentacene OTFT are sensitive to ambient conditions. Protection from the environment by encapsulation is critical to the stability of Pentacene OTFT. Therefore, using a suitable material as passivation to protect Pentacene film from environmental effect is another important topic.

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