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碩 士 論 文

高壓製程之靜電放電防護元件設計

HIGH-VOLTAGE ESD PROTECTION DEVICES DESIGN IN BCD PROCESS

研 究 生 ：黃 曄 仁（Yeh-Jen Huang)

指導教授 ：柯 明 道（Ming-Dou Ker)

中華民國九十七年一月

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摘要

在高電壓(High-Voltage)靜電放電(Electrostatic Discharge, ESD)防護元件中[如：橫向擴散金氧半功率電晶體(LDMOS Power Transistor)、金氧半電晶體(MOSFET)、矽控整流器(SCR)、雙載子電晶體(BJT)、二極體(Diode)和場氧化電晶體(Field Oxide Device, FOD)]，BCD(Bipolar CMOS DMOS)製程技術中的橫向擴散金氧半功率電晶體由於其可以同時作為輸出級電流驅動(Output Current Driver)及靜電放電防護元件，故在應用面上相當廣泛，目前使用在薄膜液晶顯示器驅動器(LCD Driver)、電源管理積體電路(Power Management IC)和汽車電子(Motor Electronics)等領域。而金氧半電晶體、矽控整流器、雙載子電晶體、二極體及場氧化電晶體則用作單純的靜電放電防護元件。矽控整流器是由電流驅動而導通的元件，在高壓靜電放電防護上由於其過高的觸發電壓(Trigger Voltage)和過低的持有電壓(Holding Voltage)，不是造成內部電路先損壞就是造成閂鎖效應(Latchup)發生，所以要加上額外的驅動電路或是透過調變佈局參數(Layout Parameter)去使觸發電壓降低和使持有電壓超過元件之工作電壓(Operation Voltage)，如此才可作為高壓靜電放電防護元件。

在本論文中首先會介紹各種已經被驗證的元件觸發方法去快速地將靜

電放電能量排放及有效率地保護內部電路之氧化層，有使用當靜電放電發生時就處於導通狀況(Initial-on)的寄生(Parasitic)元件去觸發的靜電放電防護元件、原生性 N 型金氧半電晶體觸發矽控整流器(Native-NMOS-Triggered SCR, NANSCR)、外加的元件觸發電路、閘極耦合(Gate-Couple)、基體觸發(Substrate-Trigger)技術、假閘極(Dummy-Gate)結構去取代原本的隔離區(Isolation Region)之結構及透過佈局參數的改變達成元件自身基體觸發導通(Self-Substrate-Trigger)去增加元件觸發的速度。

另外會介紹智慧功率積體電路技術(Smart Power Integrated Circuit Technology)的應用領域及各種功率電晶體[包括：V 型槽金氧半電晶體(VMOS)、U 型槽金氧半電晶體(UMOS)、橫向擴散金氧半功率電晶體]在導通電阻(Turn-On Resistance)上和傳統金氧半電晶體有何差異使其可應用於輸出級電流驅動。接著介紹橫向擴散金氧半功率電晶體的元件導通機制(Turn-On Mechanism)和由於其特殊的元件結構造成之雙重驟回崩潰(Double-Snapback)機制。

本論文研究的第一部分是探討在 0.25μm 18V BCD 製程中各種佈局參數下的測試元件(Testkey)，其中包括高壓 N 型橫向擴散金氧半功率電晶體、高壓 P 型橫向擴散金氧半功率電晶體、高壓 N 型場氧化電晶體、高壓雙向矽控整流器及高壓 N 型矽控整流器(NSCR)。分別觀察其直流 I-V 特性及傳輸線觸波脈衝(Transmission Line Pulse) I-V 特性，發現在高壓 N 型橫向擴散金氧半功率電晶體中在調變汲極端之 N 型擴散邊緣至電接觸的距離(N+ edge to contact spacing)由 1μm 至 4μm 時，由於其元件表面上的電阻值提升而使電流路徑由元件表面改變成元件深處，其二次崩潰電流(Secondary Breakdown Current, It2)由原本之 0.4A 上升至 2.5A。在高壓 P 型橫向擴散金氧半功率電晶體方面則是發現 P 型金氧半電晶體的二次崩潰電流值在大幅調變元件的總寬度(Total Width)後只提昇了少許，在調變其他佈局參數並無

法使其二次崩潰電流值能夠有效提升。在高壓 N 型場氧化電晶體及高壓 N 型矽控整流器則也可以透過調變汲極端之 N 型擴散邊緣至電接觸的距離去提升 ESD 耐受度。而在高壓雙向矽控整流器中則是發現雖然在傳輸線觸波產生系統的量測下持有電壓可透過調變參數去超過工作電壓，但是在直流 I-V 上所觀測到的卻是只有約 2V。

本論文研究的第二部分則是介紹由製程(Process)方面去達到高壓靜電放電防護之能力。首先說明 N 型橫向擴散金氧半功率電晶體的詳細失效機制(Failure Mechanism)。在了解其失效機制後針對其失效點去做改善，目前已有方法有效地使寄生於 N 型橫向擴散金氧半功率電晶體的雙載子電晶體延緩進入導通狀態，其方法為分別在汲極端和源極端下方加入 N 型重摻雜和 P 型重摻雜，使汲極端 N/N+接面要達成雪崩崩潰(Avalanche Breakdown)所需的觸發電流上升及使源極端之 β gain 下降造成雙載子電晶體所需觸發電壓上升。而在本 BCD 製程中提供了一道 P 型重摻雜的 PSB(P type Sub Body)光罩於 N 型橫向擴散金氧半功率電晶體的源極和基體端下方，去比較在小型元件(Small Device)和大型元件(Large Device)上在加入此道光罩後對靜電放電防護有何影響。

在小型元件上加入此道光罩可使觸發電壓及持有電壓同時上升，但卻會有部份元件因為過大的持有電壓而使二次崩潰電流些微下降；在大型元件上加入此道光罩可使此元件不進入驟回崩潰狀態而將不均勻導通情況改善，同時將此元件可導通的電流達到了此元件能夠承受的最高值。

HIGH-VOLTAGE ESD PROTECTION DEVICES DESIGN IN BCD PROCESS

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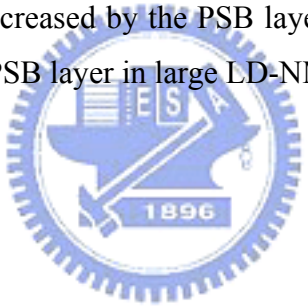
ABSTRACT

The high-voltage (HV) ESD (Electrostatic Discharge, ESD) protection devices including the LDMOS power transistor, MOSFET, SCR (Silicon Controlled Rectifier), BJT (Bipolar Junction Transistor), diode and FOD (Field Oxide Device). The LDMOS in BCD (Bipolar CMOS DMOS) process can be the output current driver and ESD protection device, simultaneously. Therefore, it is applied in the fields of LCD driver, power management IC and motor electronics, etc. The MOSFET, SCR, BJT, diode and FOD are for the ESD protection device only. The SCR is a current-triggered device and it suffers the high trigger voltage and low holding voltage issues in HV ESD protection. It is necessary to add the trigger circuit and modify the layout parameter to reduce the trigger voltage and increase the holding voltage to protect the internal circuits and avoid the latchup effect.

The various trigger methods to reduce the trigger voltage will be introduced first. The methods are parasitic initial-on PMOS-triggered device, native-NMOS-triggered SCR, dual-direction SCR trigger circuit, gate-couple, substrate trigger, dummy-gate structure and self-substrate-trigger. In addition, the application fields and turn-on resistance of smart power integrated circuit technology will be also introduced to discuss the reason of the VMOS, UMOS and LDMOS can be the output current driver. Then, to investigate the turn-on mechanism and the double-snapback characteristic of the LD-NMOS.

The first research of this thesis is to discuss the ESD performance of HV LD-NMOS, HV LD-PMOS, HV NFOD, HV dual-direction SCR and HV NSCR by layout modification in 0.25μm 18V BCD process. In TLP (Transmission Line Pulse) measurement, the ESD performance of LD-NMOS, NFOD and NSCR can be improved by increasing the N+ edge to contact spacing of the drain side due to the current path change. Unfortunately, the It2 (Secondary Breakdown Current) value can be improved a little by larger device total width of LD-PMOS. By layout modification, the holding voltage of dual-direction SCR can be controlled to over the operation voltage. But, the holding voltage of dual-direction SCR measured by 370A is different from the data measured by the TLP system is found.

The second research of this thesis is to discuss the ESD performance of the small and large LD-NMOS devices with the PSB (P type Sub Body) layer. Due to the failure mechanism of the LD-NMOS is due to the snapback characteristic. The PSB layer is added to reduce the base resistance of the parasitic BJT and increase the trigger voltage of the LD-NMOS. Once the β gain decreased, the turn-on uniformity can be improved. The holding and trigger voltage can be both increased by the PSB layer in small LD-NMOS device; The It2 value can be increased by the PSB layer in large LD-NMOS device substantially.



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而在老師開明的指導及豐沛的研究資源下，我獲得不易取得的高壓製程下線機會去驗證所研究的高壓 ESD 元件，也獲得老師提供充裕的研究經費使我這兩年中不至於生活匱乏而更努力於我的研究主題。畢業之後到業界工作更將謹記老師的名言：R＆D≠Repeat＆Delay 而使自己做事更有效率及水準。

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97 年 春

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CHAPTER 1

INTRODUCTION

1.1 Background

Electrostatic discharge (ESD) plays a major role in the reliability issue on the semiconductor industry, which originates from the transfer of electrostatic charges between two objects with different electrical potentials and damage to integrated circuits (ICs) by large energy dissipation in an extremely short time. ESD failures become more and more serious in nanoscale CMOS processes. Common ESD failures of IC chips caused by either thermal breakdown in silicon and/or metal interconnects due to high-current transient, or dielectric breakdown in gate oxide due to high voltage overstress. The ESD specifications of commercial IC products are generally required to be higher than 2kV in human-body-model (HBM) [1] ESD stress and 200 V in machine-model (MM) ESD stress. There are several on-chip ESD protection devices that have been used for a long time, such as gate-grounded NMOS (GGNMOS), gate-VDD PMOS (GDPMOS), parasitic silicon controlled rectifier (SCR) and diode, as shown in Figs. 1.1(a) ~ 1.1(d). During normal circuit operation, these ESD protection devices are in off-state. While ESD happens, these devices will be triggered into on-state and discharge the ESD current by the low-impedance characteristic. The first point after the device snapback is named the holding point. The holding point includes two useful messages about the holding voltage and the holding current. In high-voltage (HV) ESD protection, in order to provide efficient ESD protection, the trigger voltage of the protection device should be larger than the normal circuit operation voltage and smaller than the internal circuit's gate oxide breakdown voltage [2]-[3]. The on-chip ESD protection circuits have to be added between the input/output (I/O) pad and VDD/VSS to provide the desired ESD robustness in CMOS ICs [4]-[5]. There are four pin-combination modes on an I/O pad while ESD stressing: positive-to-VSS (PS-mode), negative-to-VSS (NS-mode), positive-to-VDD (PD-mode), and negative-to-VDD (ND-mode), as shown in Figs. 1.2(a) ~ 1.2(d), respectively. For example, the PS-mode means a positive stress at the I/O pad to discharge through the grounded VSS, while the VDD and other pins are floating. The locations of the ESD

protection circuits to achieve whole-chip ESD protection for CMOS ICs are illustrated in Fig. 1.3. To avoid the unexpected ESD damage in the internal circuits of CMOS ICs, the turn-on-efficient power-rail ESD clamp circuit was placed between VDD and VSS power lines [6]. ESD current at the I/O pad under the PS-mode ESD stress can be discharged through the parasitic diode of PMOS from I/O pad to VDD, and then through the VDD-to-VSS ESD clamp circuit to ground.

1.2 The Latchup Issue in High-Voltage ESD Protection

With the special application in HV operation, latchup [7]-[8] is more serious than in low-voltage operation. In HV operation, the holding voltage is always smaller than the operation voltage, the parasitic SCR in CMOS technology will be triggered and cannot be off. The reason is the positive feedback generated by the large enough substrate or well current as shown in Figs. 1.4(a) ~ 1.4(c). The parasitic circuit includes two BJTs (one is NPN, the other is PNP) and two resistors. The SCR is a two-terminals and four-layers PNPN (P+/N Sub/P Well/N+) structure. The trigger voltage is determined by the avalanche breakdown voltage of N Sub/P Well junction. When a positive voltage applied on the anode of SCR is larger than the breakdown voltage and its cathode is relatively grounded. Through the avalanche breakdown, the generation of hole and electron is launched. If the voltage drop across the resistor is larger than 0.7 V, the parasitic BJT will be turn on and initiates the SCR into latching state. Once the SCR is triggered on, the required holding current to keep the NPN and PNP transistors on is no longer involving the avalanche breakdown mechanism. Due to this reason, the holding voltage of SCR is always at low voltage level around 5 V. However, if the resistor is large enough, the latchup happens more easily. Once latchup happens, the current will conduct through a low-impedance path from the power supply to ground. If the current is not limited, irreversible damage will happen by the latchup-generated high power. Even though the current is limited, the CMOS ICs may be malfunction. In order to avoid the latchup effect, there are several methods that have be developed, such as well-designed SCR structure, epitaxial layer, silicon on insulator (SOI), trench isolation and layout parameter with modified anode-to-cathode spacing, guard ring width. The well-designed SCR structure means the SCR is latchup-free by itself through the product of the β_{npn} and β_{pnp} is smaller than 1, as shown in Fig. 1.5. The guard ring types are shown in Fig. 1.6, including the single guard ring and the double guard ring.

1.2.1 The Device Structures with Latchup Immunity

The HV ESD protection device with sufficient latchup immunity is necessary. The device with isolated and asymmetric structure has been verified that has the better latchup immunity than the non-isolated and symmetry structure. The isolated structure means that there is an additional N+ burier layer (NBL) beneath the N Well or P Well combine with its peripheral N Well regions and the non-isolated structure is without the NBL layer [9], as shown in Figs. 1.7(a) and 1.7(b), respectively. The isolated structure can prevent the possible leakage current path between outside and inside device. The asymmetric structure means that not both the drain and source sides enclosed with N Well region. The N Well region is a lightly doped layer and it is used to sustain high breakdown voltage. On the other hand, the symmetry structure means both the drain and source sides can sustain high voltage as shown in Fig. 1.7(c), but the turn-on resistance is large than asymmetric structure.

To investigate the latchup characteristic in HV CMOS process, the transmission line pulsing (TLP) generator is used to measure the latchup I-V curves. The TLP system was invented by T. J. Maloney and N. Khurana (Intel) in 1985, it generates a short width (rise time) of 100ns (10ns) and high current square pulse [10]. Since then, TLP has allowed tremendous insight into the electrical characteristics of ESD protection circuits and devices. The main value of TLP is to reduce the design cycle time for the ESD protection circuits. The TLP system is to simulate the real ESD current discharge event and it's the most accurate facility to measure the trigger voltage, holding voltage and secondary breakdown current (It2) of the device under test (DUT). On the other hand, the TLP will not damage the HV devices so easier than continuous-type curve tracer Tektronix 370A due to its shorter pulse width and limited energy [11].

Compared with the non-isolated and symmetry structure, the device with isolated and asymmetric structure has better latchup immunity due to its higher trigger and holding voltage, as shown in Fig. 1.7(d). By the way, to raise the layout parameter of anode-to-cathode spacing will improve the latchup immunity due to the holding voltage increasing by the increased SCR current path. However, increasing guard ring width only has a little improvement on latchup immunity of isolated structure, because the dominant factor is the isolation region of NBL/P well junction, not the guard ring structure.

1.2.2 The Latchup-Free Power-Rail ESD Clamp Circuit

While using the HV ESD protection device on the power-rail ESD clamp, the holding voltage must be smaller than the power supply voltage, the ESD device may be triggered on by the system-level electromagnetic compatibility (EMC)/ESD transient pulses to cause a very serious latchup or latchup-like failure in CMOS ICs [12]. The increasing of the holding voltage method is developed by the stacked device technique. On the stacked Field Oxide Device (FOD), the total trigger voltage and holding voltage are the sum of the single device. For example, if the trigger voltage and holding voltage of single device are 30 V and 15 V. With two stacked devices, the total trigger voltage and holding voltage are 60 V and 30 V.

Through this technique, the holding voltage is doubled, but the drawback is that the trigger voltage is also doubled, as shown in Figs. 1.8(a) and 1.8(b). In order to get a turn-on-efficient power-rail ESD clamp, the extra ESD detection circuit is added to detect the ESD pulse on the power line and let the trigger voltage be smaller. The power-rail ESD detection circuit is composed of a resistor, a capacitor and an inverter. This detection circuit is also called RC-inverter. Due to the ESD pulse happens on nanosecond order duration. The product of the resistor and capacitor is always set to microsecond order to distinguish the normal circuit operation and the ESD stress event. The inverter is used to push the NMOS in the next stage. To match the value of the resistor and capacitor is another issue. Although the product of the resistor and capacitor is the same, it may cause the turn-on efficiency something different. Moreover, another drawback of the stacked technique is the turn-on resistance is also increased, because the connection of the stacked devices is in series type.

1.3 The Trigger Techniques of ESD Protection Device

Because of the total power dissipation of one certain device is fixed at the product of the It2 and holding voltage (power = It2 x V_{hold}), the SCR device can sustain a much higher It2 than other devices in a smaller layout due to its low holding voltage characteristic. So, it had been used to protect the internal circuits against ESD damage for a long time. But, the trigger voltage of the HV SCR is too large to protect the internal circuit. Therefore, how to decrease the trigger voltage in HV operation is another issue.

There are several SCR-based structure had been verified. The application method is to integrate two kinds of devices into one device by using the low holding voltage characteristic of SCR and the low trigger voltage of other devices. The integration method can be one device with parasitic SCR path or SCR device with parasitic trigger device.

1.3.1 The Initial-On Parasitic Structure Technique

In the past, the traditional ESD protection devices are use the parasitic BJT to turn on the GGNMOS and use the avalanche breakdown to turn on the SCR. But, with the device scaling, the internal circuits are fabricated on thinner oxide, the traditional ESD protection design cannot be able to effectively protect it. The initial-on technique means the ESD device is turned on when the IC is floating without any power bias, when the I/O pad is zapped by ESD, the ESD device is already standby to discharge the ESD current from pad to ground as shown in Figs. 1.9(a) ~ 1.9(e).

The design window of the ESD protection device is between the power supply (VDD) and the internal circuit's gate oxide breakdown voltage as shown in Fig. 1.10. The holding voltage should be higher than the VDD to avoid the latchup effect and the trigger voltage should be lower than the gate oxide breakdown voltage to discharge the ESD current efficiently. One device with lower trigger voltage by initial-on technique is verified by the SCR device with PMOS-triggered and RC-based ESD transient detection circuit as shown in Fig. 1.11 [13]. The source and drain terminals of the PMOS transistor are connected to the additional N+ diffusion and P+ diffusion of the SCR structure. The additional N+ and P+ diffusions are used to trigger the N Well and P Substrate. The gate terminal of the parasitic PMOS is controlled by the RC-based ESD transient detection circuit.

Under PS-mode stress, the gate voltage of embedded PMOS is initially kept at zero in the power-rail ESD clamp circuit. The PMOS will turn on by the zero bias and conduct the ESD current from the N Well and inject into P Substrate of the SCR device. With these two trigger nodes, the SCR can be launched quickly. The initial-on PMOS transistor provides another path to make the voltage bias and induce base current between the emitter and base in the two BJTs to turn on the SCR device as shown in Fig. 1.12.

Due to the holding voltage, turn-on resistance and ESD robustness of SCR are influenced by its anode-to-cathode spacing, the layout structure can be changed to merge the n trigger node into the source terminal of PMOS transistor as shown in Fig. 1.13. Through this method, the trigger voltage, holding voltage can be reduced and the It2 will be increased.

1.3.2 The Dual-Direction SCR with Extra Trigger Circuit

Traditional SCR device provides only one direction ESD protection path. The dual-direction SCR device can protect each I/O pad against ESD stress in the PS-mode,

PD-mode, NS-mode and ND-mode [14]. This dual-direction SCR device is composed of a symmetrical five-layers NPNPN structure with one lateral PNP (Q1) and two vertical NPN (Q2 and Q3), as shown in Fig. 1.14(a). The extra trigger circuit comprises two pairs of Zener diodes (D1~D4) with back-to-back connection, as shown in Fig. 1.14(b). When a positive ESD pulse is stress at the anode of dual-direction SCR and its cathode is relatively grounded, the Zener diode D1 will be reverse breakdown and let the ESD current to trigger on the Q3 and Q1 transistor. The positive ESD current can be discharged through the current path1 and the negative ESD current through the current path2. The TLP I-V curve of dual-direction SCR is shown in Fig. 1.14(c). The dual-direction SCR provides low holding voltage and low impedance path to discharge the huge ESD current under every stress mode.

Although the SCR device is more area efficiency than other ESD protection devices. To improve the area efficiency in SCR device is an important challenge of manufacture. The layout structure divide into three kinds of square-shaped cells, named a corner cell, a center cell and an edge cell, respectively. As their names imply, they disposed in the corner location, center location and edge location. Figs. 1.15(a) ~ 1.15(g) shows three kinds of cells, each cell provides current flow either to or from P+ region. The center cell can discharge in four directions; the edge cell can discharge in two directions; the corner cell can discharge in one direction. Compared with traditional structure, the cell based structure can improve the current capability substantially.

1.3.3 The Gate-Coupled Technique

Except the SCR device provides good ESD robustness. The GGNMOS and GDPMOS are also used in ESD protection devices. Generally, according to the lower β gain of GDPMOS, the GDPMOS will have very unapparent snapback characteristic than the GGNMOS as shown in Figs. 1.1(b) and 1.1(c). Due to the snapback mechanism, the multiple finger type layout of GGNMOS will suffer the non-uniform turn on issue. Once the one of the multiple fingers turns on, the current will conduct through this path soon, while the other fingers are not turn on yet. The more current flow through the finger, the more heat generates. It may cause the device failure on the most heat accumulation location as shown in Figs. 1.16(a) and 1.16(b).

Due to the snapback mechanism, the GGNMOS have lower holding voltage than the GDPMOS and the GGNMOS have higher It2 than the GDPMOS. The symbol of the ESD robustness is the It2 value, so the GGNMOS is preferred to be the ESD protection device. If

the non-uniform turn on effect can be delayed or decreased, the ESD level must be increased. To improve the turn on uniformity, the gate-coupled and substrate-triggered designs have been reported.

The gate-coupled technique is used to lower the trigger voltage and to ensure uniform ESD current distribution [15]-[16]. The couple capacitor can be made by a poly layer under the wire-bonding metal pad or the parasitic capacitance without increasing extra layout area; the resistor can also be made by poly layer, the product of the capacitor and the resistor is set to micron second order to distinguish the ESD stress as the previous RC-based circuit. Fig. 1.17 shows the gate-coupled structure, while the positive ESD stress occurs on the pad with relatively grounded VSS, the gate voltage of the GGNMOS is logic high. Thus, the ESD device can use the ESD voltage to trigger itself and not to work by the avalanche breakdown of the parasitic BJT. Furthermore, this coupled gate voltage can lowered the energy band of the channel surface and concentrate the ESD current at a smaller turn-on region in the channel surface of the GGNMOS. It also means there is a high electric field across the gate oxide. From the semiconductor physics, the gate-coupled technique can uniformly turn the channel current but it cannot enhance the turn-on uniformity of parasitic lateral BJT in the GGNMOS.

If the rising time of the ESD pulse be smaller, the trigger voltage could be also reduced. This is why a faster rising time of pulse can trigger a transient latchup event during normal operation. In order to build a wide safety ESD margin, it is necessary to consider different rising time of pulse as shown in Fig. 1.18.

Moreover, in order to make sure the gate-coupled effect, there are three kinds of HV devices to be tested as the NPN BJT, NPN-SCR and the NSCR. The HV NPN BJT device is designed on the N+ Buried Layer (NBL) and there are two current paths as shown in Fig. 1.19(a) without using the sinker layer to gain more chipper cost. The sinker layer is a high doping optional layer to let the current flow deeper to prevent the hot-spots on the surface, non-uniform current flow and early failure. So, how to avoid such disadvantages on the HV NPN device without sinker layer is a cost down issue. The HV NPN-SCR device is to insert a P+ diffusion in the collector region of the NPN BJT, then there is a SCR path (P/N/P/N) be established, as shown in Fig. 1.19(b). The HV NSCR is to insert a P+ diffusion in the drain region of the NLDMOS and there is a SCR path from the drain to source, as shown in Fig. 1.19(c). In these test devices, the gate-coupled technique can reduce the trigger voltage more by larger gate-grounded resistor.

1.3.4 The Substrate-Triggered Technique

The substrate-triggered technique is to draw an electric connection from the P+ of substrate or N+ of N Well [17]. The current flows into the substrate or well can change the turn-on resistance of the ESD protection device during ESD stress. It means the substrate current can change the turn-on area or the turn-on path as parasitic lateral BJT in the NMOS to sustain higher ESD stress. Comparing to the gate-coupled, there is no gate bias to lower the energy bands on the surface channel of the substrate-triggered NMOS. But, the substrate bias can lower the energy bands in the substrate region and extend the current distribution. The turn-on behavior of the substrate-triggered GGNMOS device is the parasitic lateral BJT of all fingers can be uniformly turned on. With the increasing of the substrate current, the trigger voltage and the turn-on resistance of the device can be reduced as shown in Fig. 1.20.

The substrate-triggered circuit structure is also use the RC-based detection circuit to trigger the ESD protection device as shown in Fig. 1.21. During the positive ESD stress, the voltage of point A is logic low to trigger the PMOS (Mp1) and let the voltage of point B be logic high. Then, the NMOS (Mn2) is triggered and let the voltage of point C be logic low. The turn on of the Mp1 can conduct the current from VDD to trigger the P+ diffusion of P Substrate; the turn on of the Mn2 can draw the current from the N+ diffusion of N Well to VSS and it means the N Well has been triggered.

These two types of substrate-triggered methods can be used in any device to reduce its trigger voltage. For example, the trigger voltage of HV SCR is too high to protect the internal circuit. Moreover, in order to avoid the latchup effect of HV SCR, the stacked-device technique can be adapted to raise the holding voltage, but the trigger voltage is also rise up. The trigger node can be set on the N+ of N Well and P+ of P Substrate to trigger the parasitic NPN and PNP BJTs synchronously. Then, the HV SCR can be triggered on without junction avalanche breakdown mechanism.

When the trigger current is applied in p-trigger node, the NPN BJT in the SCR device is active, and the collector current of NPN is generated to bias the PNP transistor. Then, the PNP is turned on, the collector current of PNP is also generated to further bias the NPN transistor. The positive-feedback regenerative mechanism of latchup is initiated by the substrate-triggered current in SCR structure instead of avalanche breakdown mechanism. On the other hand, when the trigger current is drawn from the n-trigger node, the positive-feedback mechanism is also generated.

On the whole-chip ESD protection, the double-triggered SCR (including the n-trigger

and p-trigger) is set between the power-rail, I/O pad to VDD and VSS, respectively. In order to save the layout area, the RC-based ESD detection circuit can be shared and connect to each double-triggered SCR, as shown in Fig. 1.22.

1.3.5 The Native-NMOS-Triggered Technique

Using the parasitic PMOS structure to trigger the SCR ESD protection device is introduced as above. There is another trigger method by using the native-NMOS with very low threshold voltage about 0.1 V to trigger the SCR device [18]. Compared with the traditional low-voltage-triggered SCR (LVTSCR), the drain of native NMOS in native-NMOS-triggered SCR (NANSCR) is directly coupled to the anode of SCR, but the drain of NMOS in LVTSCR is set across the N Well/P Substrate junction of the SCR device, as shown in Figs. 1.23(a) and 1.23(b), respectively.

The gate of native NMOS is connected to a negative bias circuit (NBC) to keep off the NANSCR during normal circuit operation. The NBC is composed of clock generator, capacitors and diodes. The output negative voltage of NBC can be tuned to fulfill various applications. During the ESD event, the NBC is relatively floating, the native NMOS is an initial-on device as the PMOS-triggered SCR. Then, the trigger current flows into the base of NPN and the base voltage of NPN will be raised up by the substrate resistor (Rsub). Once the voltage across the base and emitter of NPN exceeds 0.7 V, the NPN in SCR structure is turned on. After the NPN turns on, the PNP is also turned on by the collector current of NPN. Therefore, the positive-feedback mechanism of the NANSCR is initiated by the trigger current of the initial-on native NMOS in the NANSCR device. Finally, the NANSCR will be triggered on to discharge the ESD current. In addition, comparing with the TLP I-V curve of the LVTSCR and NANSCR, the turn-on resistance and holding voltage of NANSCR are smaller than those of LVTSCR on the same device width.

1.3.6 The Dummy-Gate Structure Technique

The dummy-gate structure is used to block the shallow trench isolation (STI) and silicide between the diffusion regions as shown in Figs. 1.24(a) and 1.24(b) [19], the ESD current discharge path can be changed to enhance the turn on speed of the ESD protection device. For example, to merge the dummy-gate structure with the substrate-triggered SCR

(STSCR) device. Due to the deeper STI region causes a longer current path from the anode to cathode, the dummy-gate structure can block the STI region to smaller the current path. This STSCR with dummy-gate structure can be used in input, output and power-rail ESD protection device. In order to prevent the device suffering latchup, the voltage drop elements (such as diodes) can be stacked with the dummy-gate structure STSCR to raise the total holding voltage.

Comparing on the STSCR device with STI and dummy-gate structure, the trigger voltage can be further reduced by the dummy-gate structure than STI structure under the same trigger current. The reason is the current gain (β) of parasitic BJT in dummy-gate structure is higher than in STI structure by the shorter current path.

1.3.7 The Self-Substrate-Triggered Technique

The self-substrate-triggered technique is to conduct the ESD current to the desired finger location and use the ESD current to trigger other fingers [20]. This trigger method will improve the turn-on uniformity and the HBM and It2 level of the GGNMOS substantially, but the trigger voltage and holding voltage will not change.

Due to the base resistance in parasitic NPN of the center-finger GGNMOS is higher than other fingers, the center-finger of GGNMOS is always triggered first. Once the center-finger of NMOS has been triggered, the ESD voltage will let the device into snapback status. Therefore, the ESD current will be only discharged through few part of device to cause the non-uniform turn on issue.

In order to guarantee the center-finger of the GGNMOS will turn on first, let the channel length of the center-finger be the minimum rule and other fingers with larger channel length. The cross-sectional view of the self-substrate-triggered GGNMOS is shown in Fig. 1.25, the source of the center-finger is connected to the substrate-triggered node.

1.4 Thesis Organization

In order to reach the desired ESD performance in 0.25μm 18V BCD process, there are various layout splits have been verified in this thesis.

This thesis is composed of five chapters. Chapter 1 presents the fundamental concept of ESD protection design by device layout modification and extra trigger circuit. In order to get the appropriate trigger voltage and holding voltage in high voltage operation to protect the

internal circuit and suppress the latchup effect, there are several methods to reduce the trigger voltage and the suitable device structure to avoid the latchup happens

In chapter 2, presents an overview on several power MOS transistors and their advantages and disadvantages in current path and reliability. To research one kind of power MOS transistors, the DMOS is the main topic of this thesis. Then, discuss the turn-on mechanism and double-snapback characteristic in HV LD-NMOS and HV NMOS. Such turn-on mechanism is very important on designing the trigger and holding voltage.

In chapter 3, presents the HV BJT with controllable trigger and holding voltage, the HV NMOS with Embedded SCR structure and HV BJT with Embedded SCR Structure those have been reported first. Then, the experimental results show the ESD performance of HV LD-NMOS, HV LD-PMOS, HV NFOD, HV dual-direction SCR and HV NSCR by layout modification. The ESD performance of LD-NMOS, NFOD and NSCR can be improved to 2A by increasing the N+ edge to contact spacing of the drain side. The dual-direction SCR can be used in discharging the ESD current while the operation voltage is from negative to positive. With increasing the layout parameters of dual-direction SCR, the It2 value, HBM and MM level can be improved to about 4A, 6KV and 300V, respectively.

In chapter 4, presents the failure mechanism of the LD-NMOS and introduce the methods of no turn-on parasitic BJT and no snapback characteristic in LD-NMOS. To make sure the no snapback characteristic can be made correctly, the PSB (P type Sub Body) layer of 0.25μm 18V BCD process is added to let the ESD protection device not to snapback. The PSB layer is verified in small device (total width <5k μm) and large device (total width > 5k μm) to investigate the influence on ESD performance of LD-NMOS. In larger device, the PSB layer can reach the no snapback characteristic and have the best turn-on uniformity.

Finally, the main results of this thesis are summarized in chapter 5, the future work is to research the holding voltage is different by TLP and 370A measuring. In addition, the trigger elements have to be added in the dual-direction SCR to reduce the trigger voltage without extra layout area.

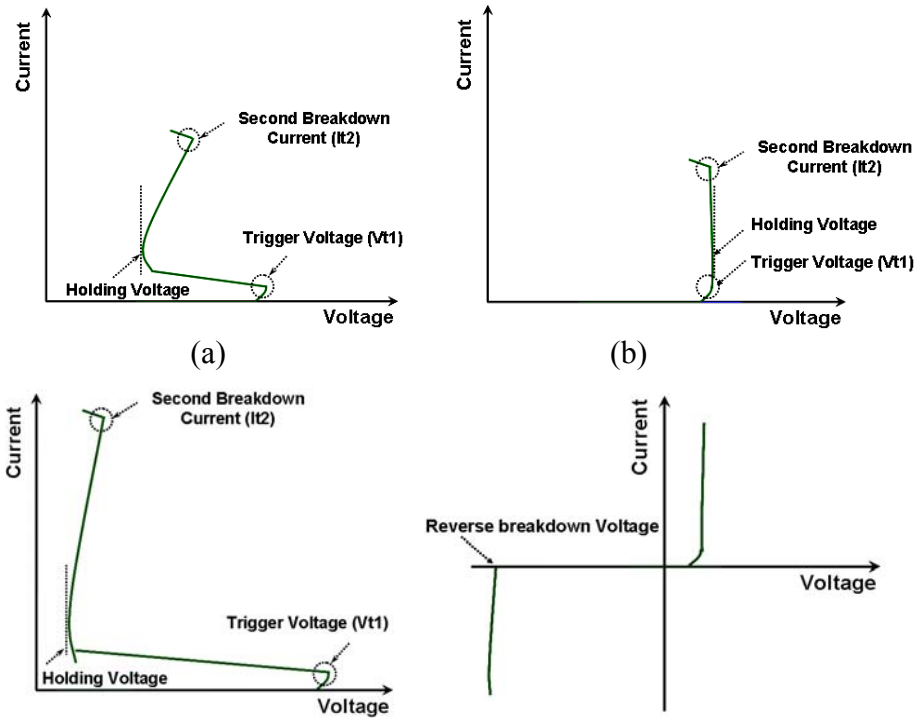


Fig. 1.1 The I-V curve of the four common ESD protection devices: (a) gate-grounded NMOS (GGNMOS), (b) gate-VDD PMOS (GDPMOS), (c) parasitic silicon controlled rectifier (SCR), and (d) diode.

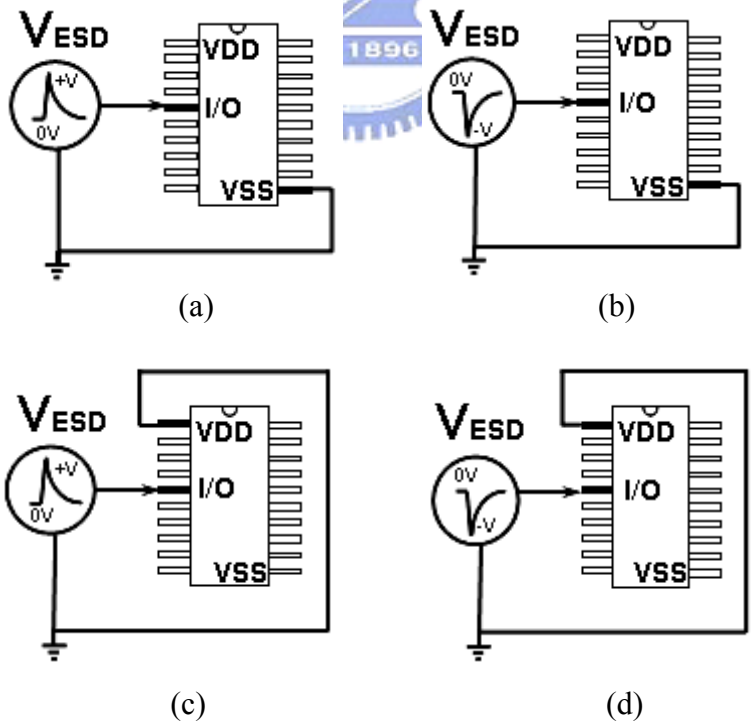


Fig. 1.2 The four pin-combination modes for ESD test: (a) positive-to-VSS (PS-mode), (b) negative-to-VSS (NS-mode), (c) positive-to-VDD (PD-mode), and (d) negative-to-VDD (ND-mode).

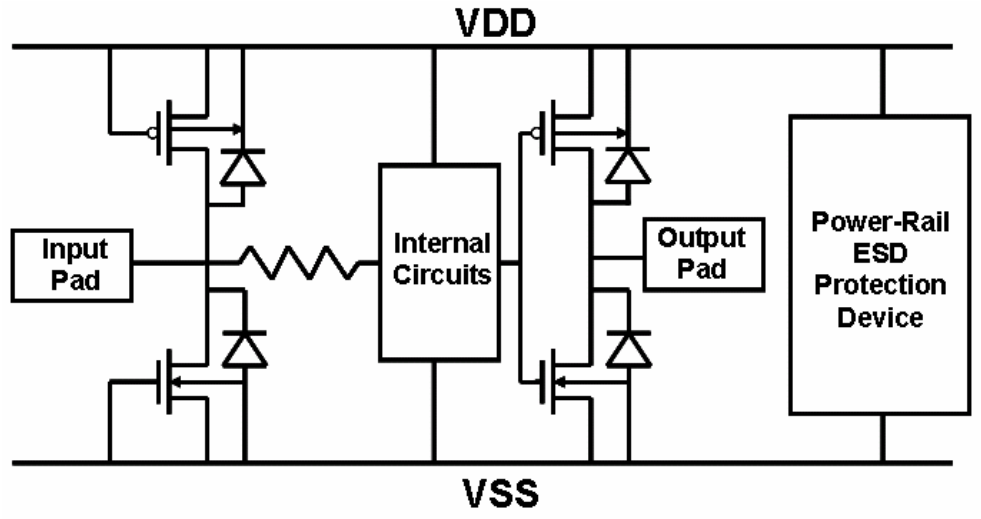
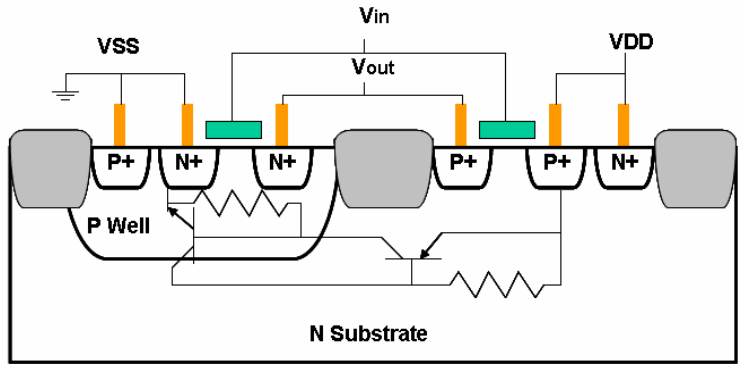
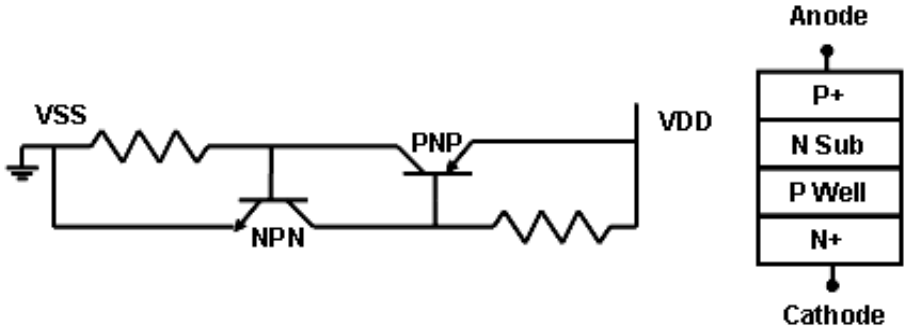


Fig. 1.3 The whole-chip ESD protection circuits in CMOS IC.



(a)



(b) (c)

Fig. 1.4 (a) The parasitic SCR path in CMOS ICs. (b) The equivalent circuit of SCR. (c) The two terminals and four layers P-N-P-N of SCR.

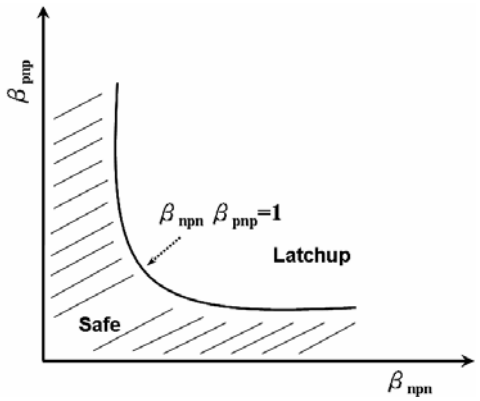


Fig. 1.5 The latchup-free current gain (β) product parabola curve.

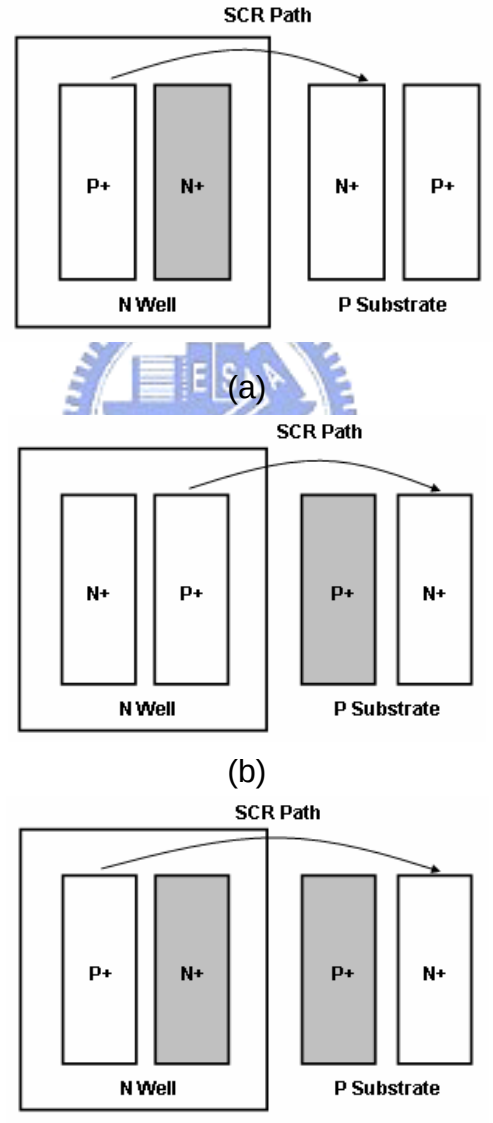
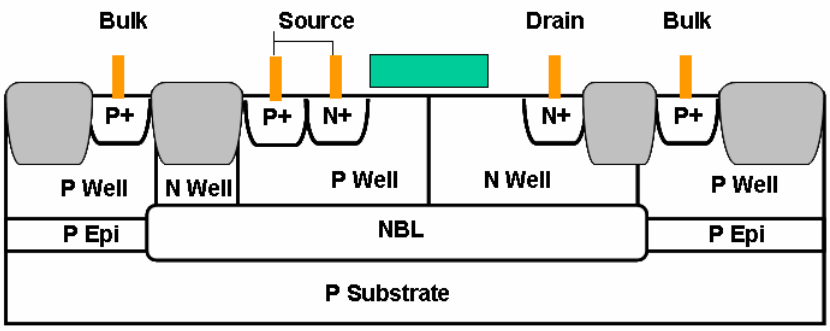
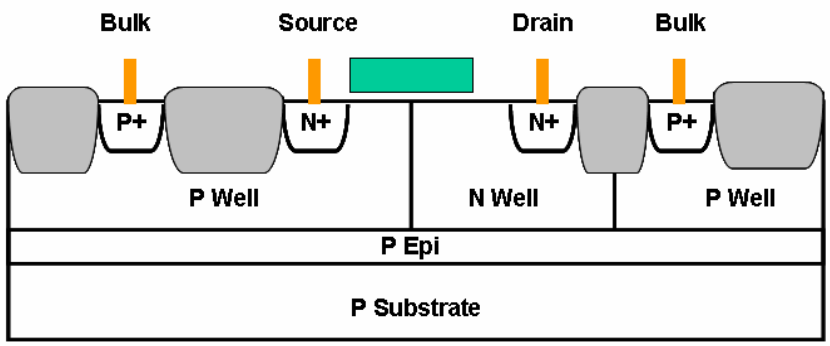


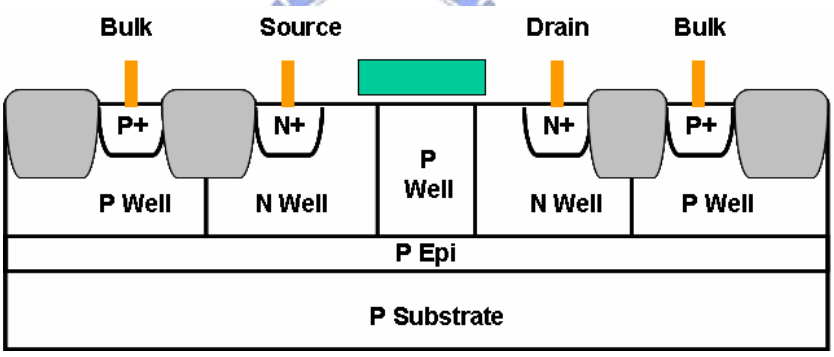
Fig. 1.6 (a) The N+/N Well guard ring, (b) The P+/P Substrate guard ring, (c) The double guard ring.



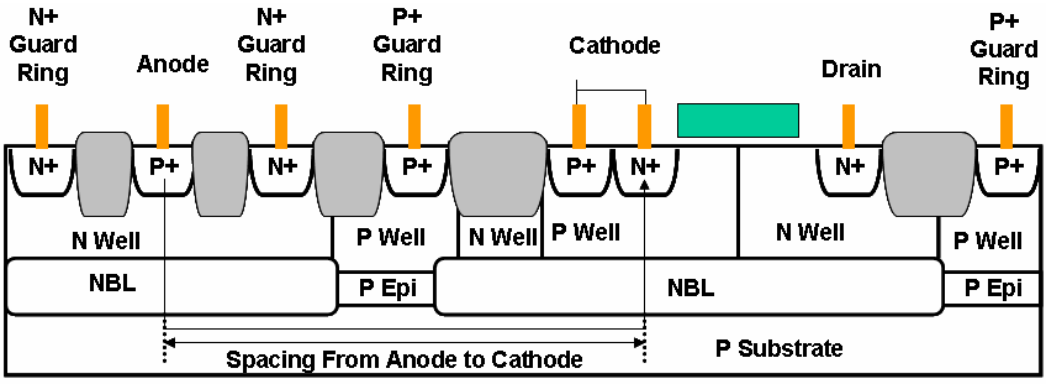
(a)



(b)

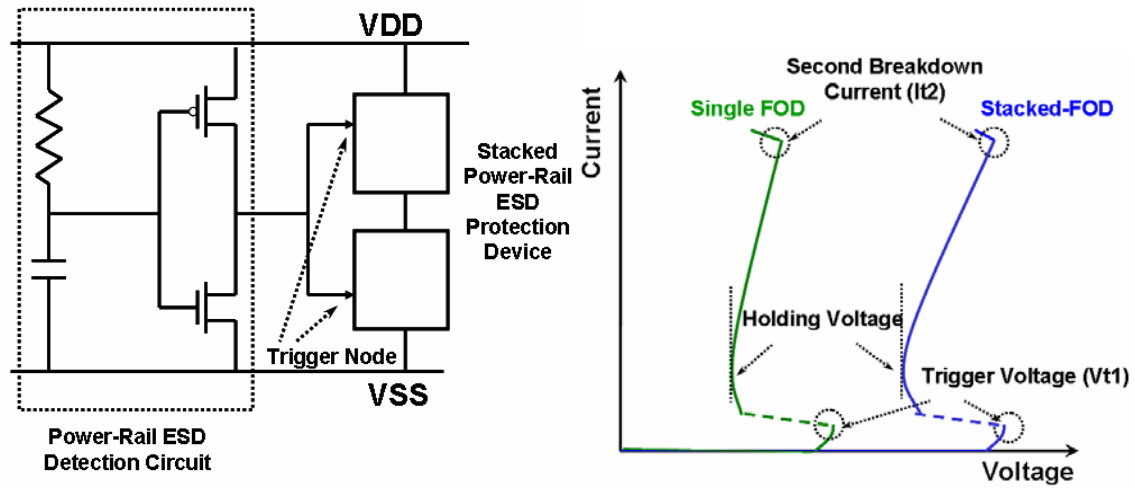


(c)



(d)

Fig. 1.7 The device cross-sectional views of (a) isolated HV NMOS, (b) non-isolated HV NMOS, (c) non-isolated symmetric HV NMOS, (d) isolated asymmetric HV NMOS and HV PMOS.



(a) (b)

Fig. 1.8 (a) The stacked power rail ESD protection device and its RC-based detection circuit. (b) The TLP I-V curves of single FOD and stacked-FOD.

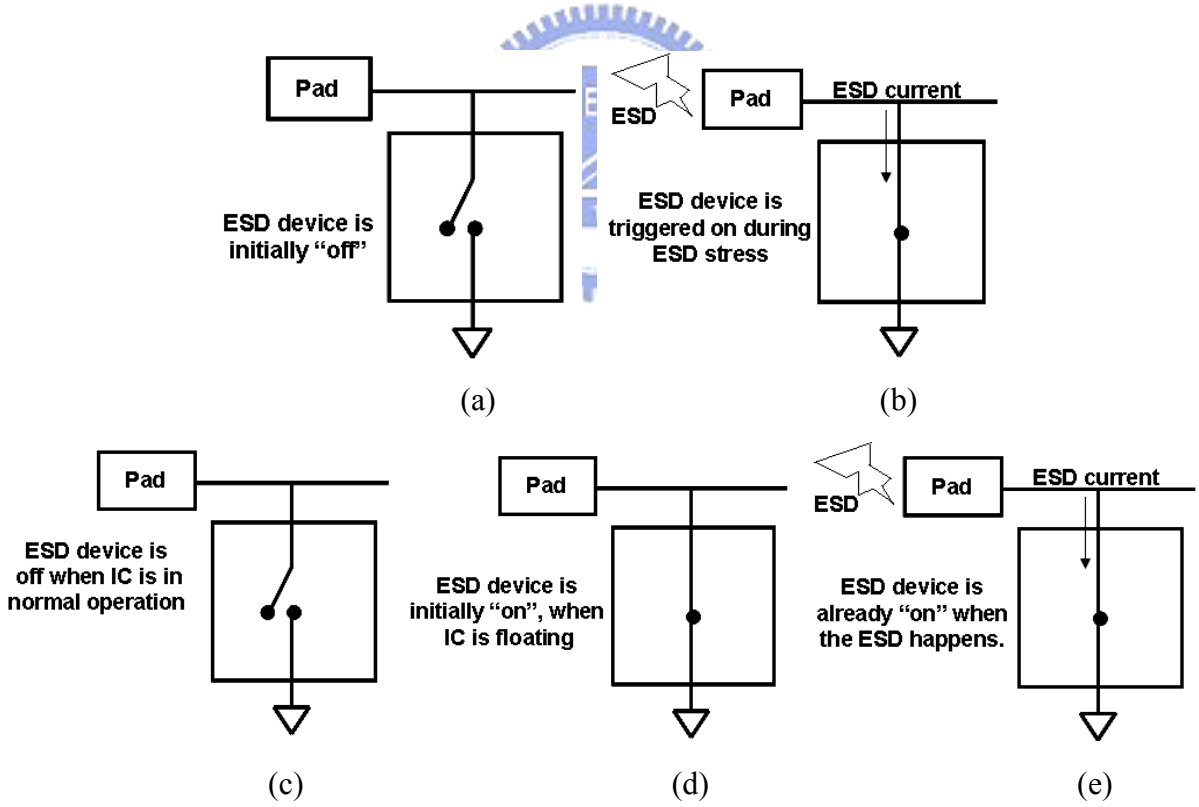


Fig. 1.9 (a) ~ (b) The traditional ESD protection device with the initial-off characteristic. (c) ~ (e) The ESD protection device with the initial-on characteristic.

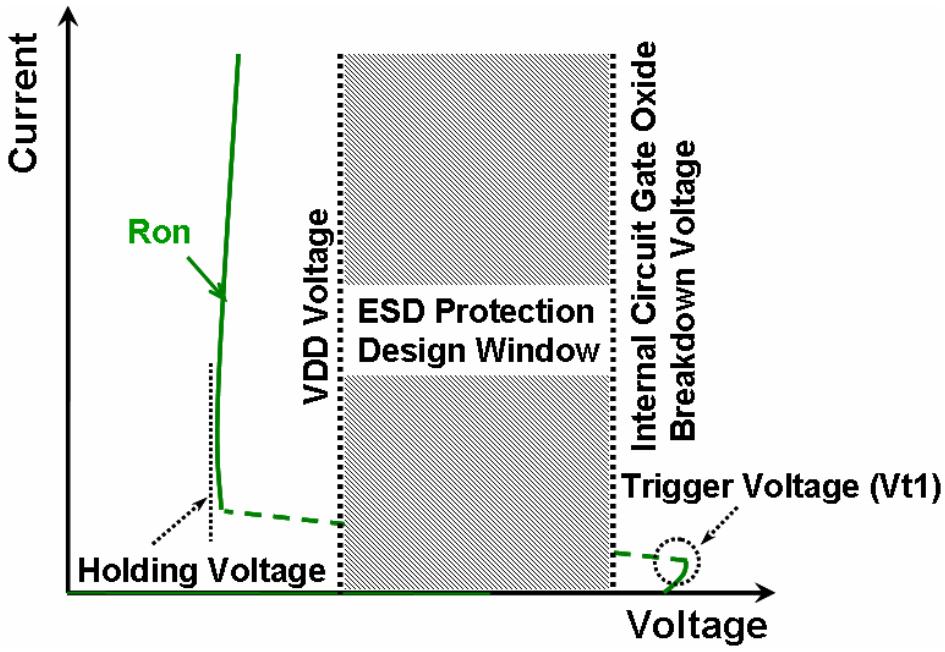


Fig. 1.10 The ESD protection design window in traditional SCR device.

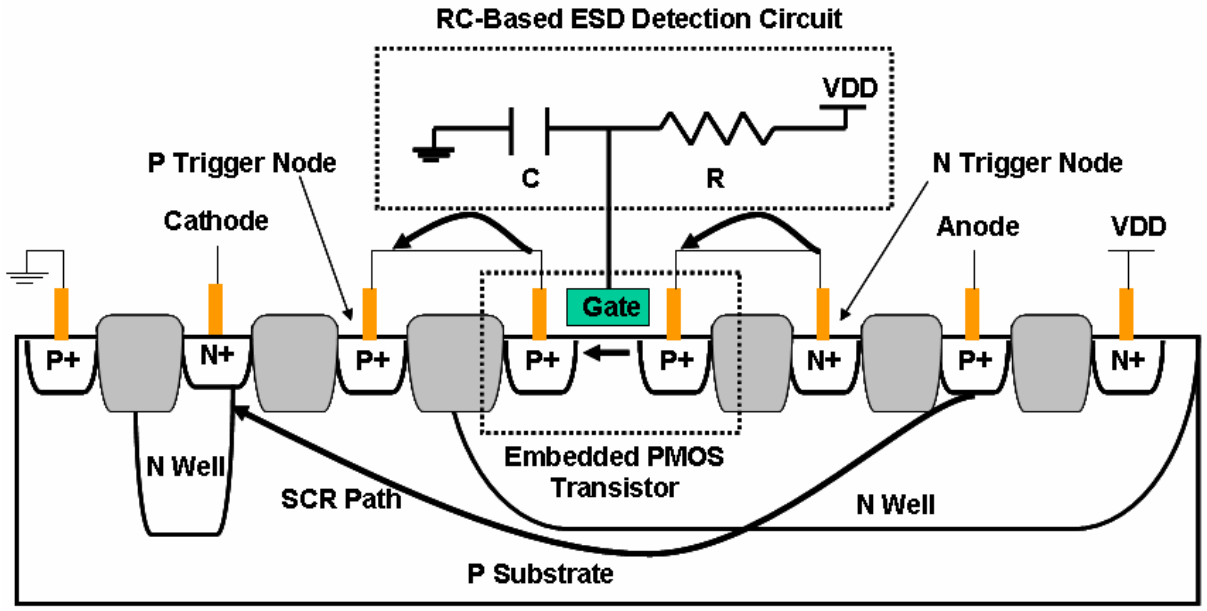


Fig. 1.11 The cross-sectional view of the initial-on SCR with PMOS trigger technique.

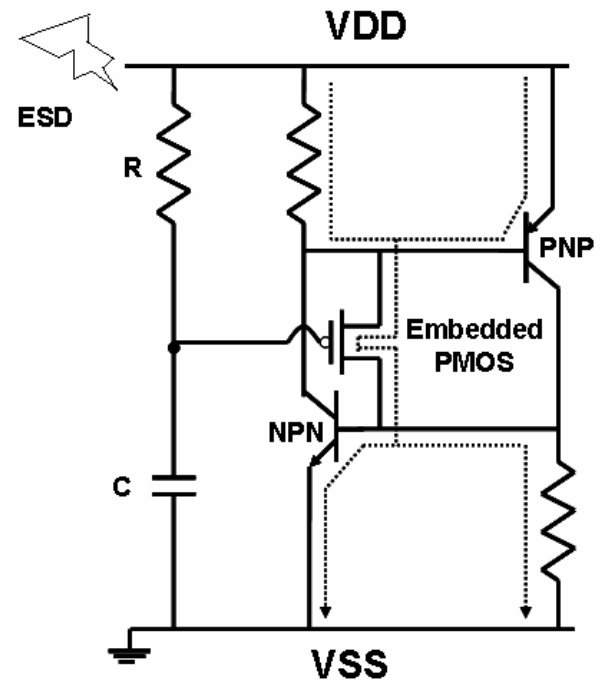


Fig. 1.12 The equivalent circuit of the initial-on SCR with PMOS trigger.

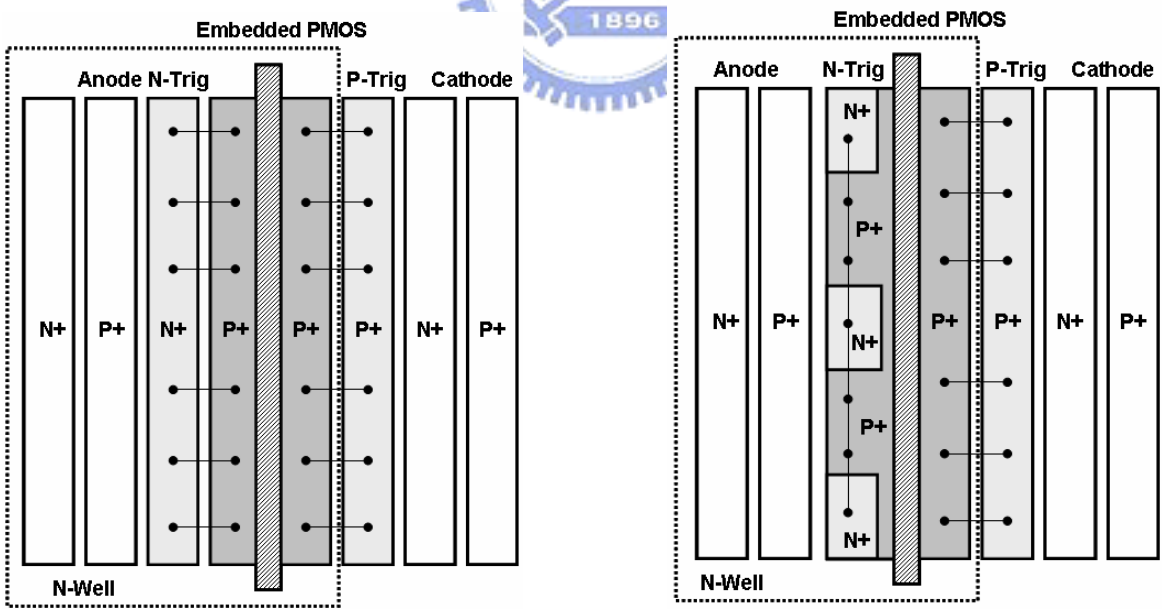
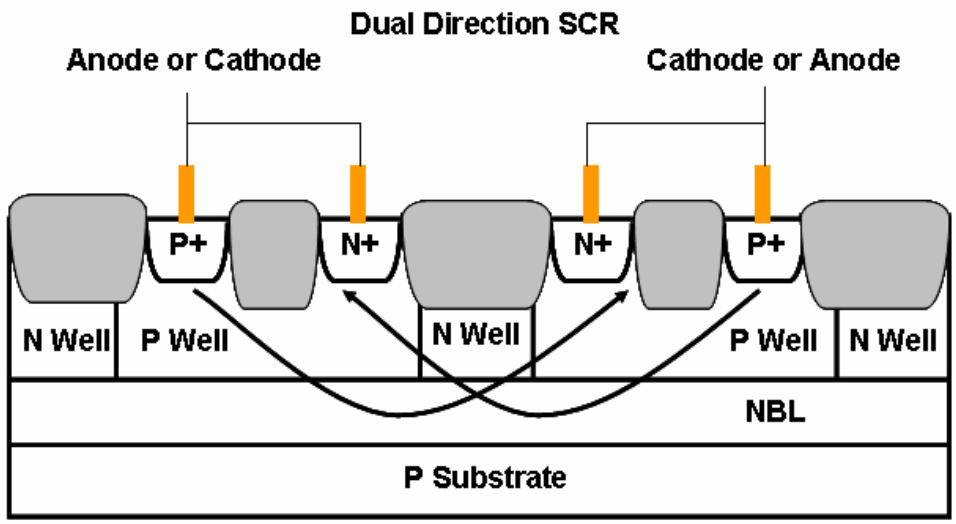
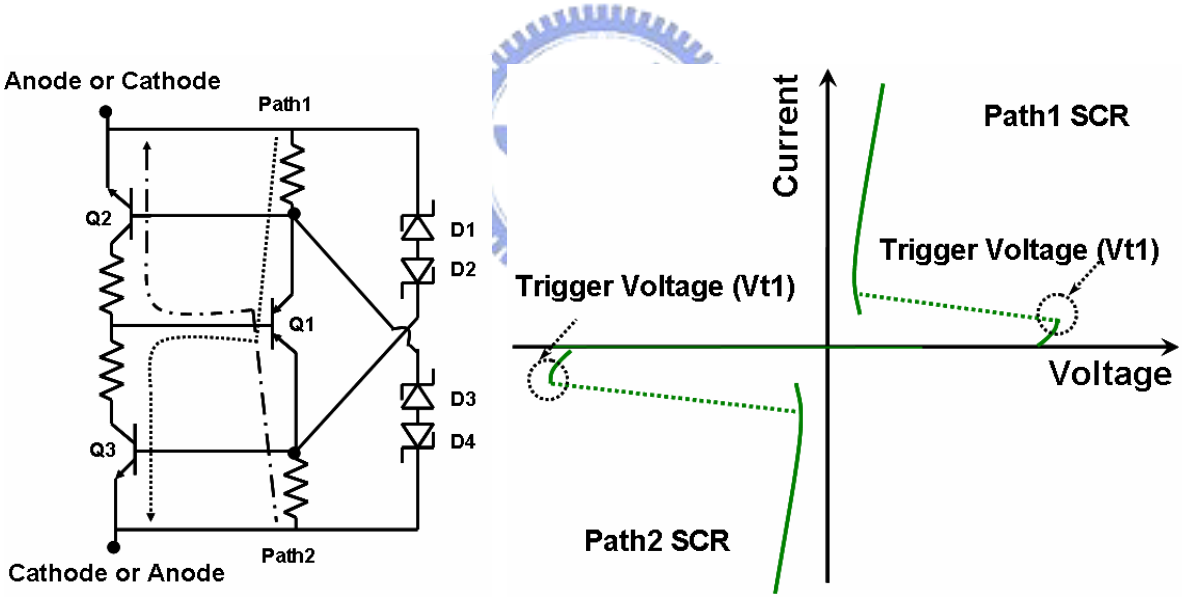


Fig. 1.13 The layout view of the initial-on SCR with PMOS trigger (a) The common layout pattern, (b) The n-trig node merged into the source side of the embedded PMOS structure.



(a)



(b) (c)

Fig. 1.14 (a) The cross-sectional view of the dual-direction SCR structure, (b) The trigger node and the trigger method with two pair back-to-back Zener diode, (c) The TLP I-V characteristic of the dual-direction SCR.

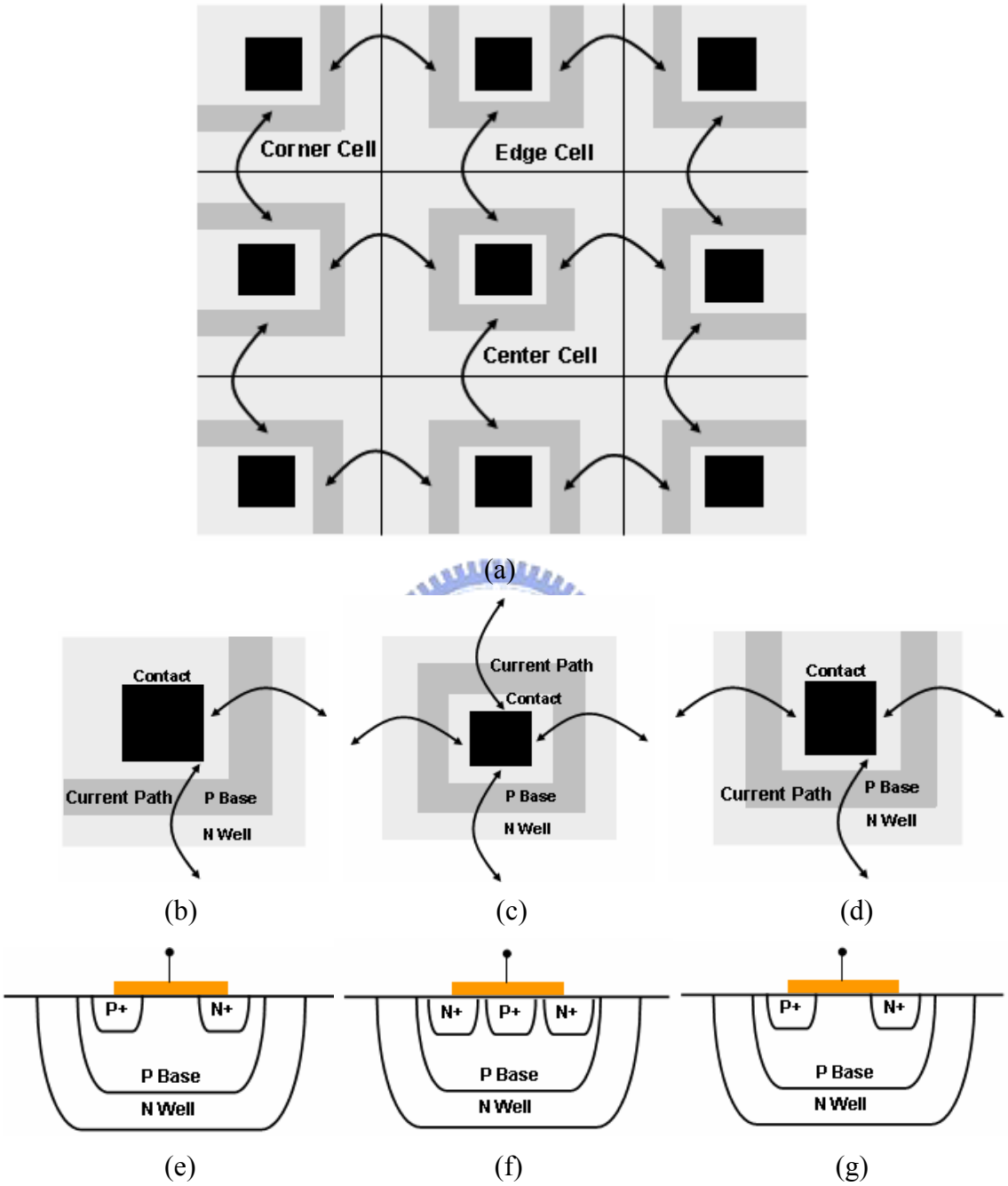


Fig. 1.15 (a) The layout cell structure of the dual-direction SCR, (b) The layout view of corner cell, (c) The layout view of edge cell, (d) The layout view of center cell, (e) The cross-sectional view of corner cell, (f) The cross-sectional view of edge cell, (g) The cross-sectional view of center cell.

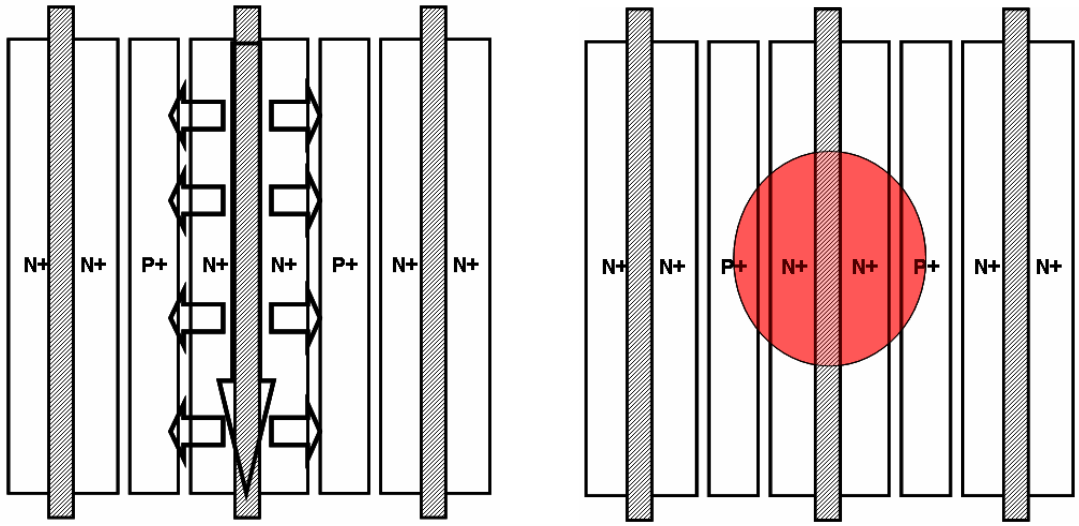


Fig. 1.16 (a) The ESD current always flow through the center-finger of GGNMOS first, (b) The center-finger will burn out by the joule heating.

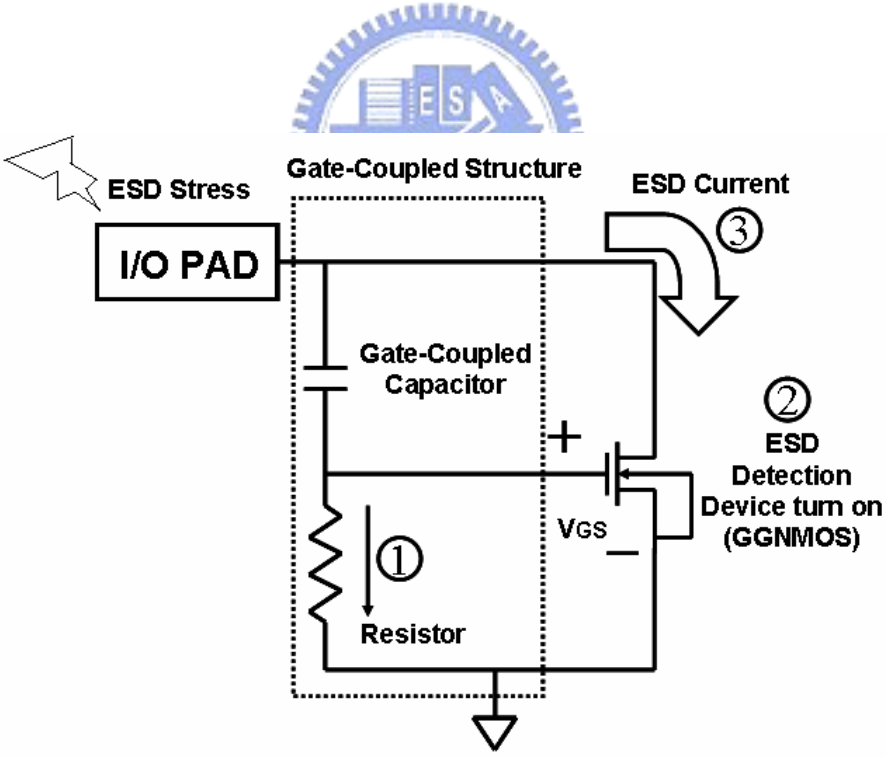


Fig. 1.17 The gate-coupled structure and the turn-on sequence of the gate-coupled technique.

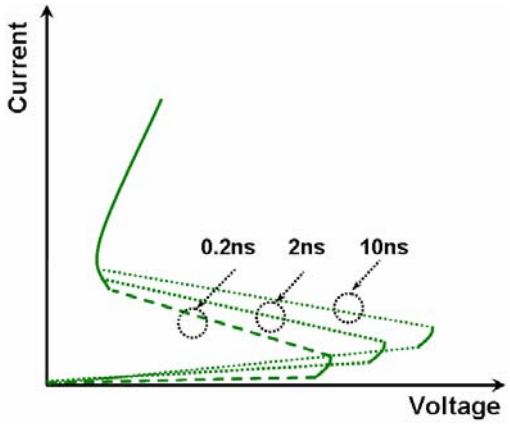


Fig. 1.18 The TLP I-V curves of various rising time of the ESD pulse.

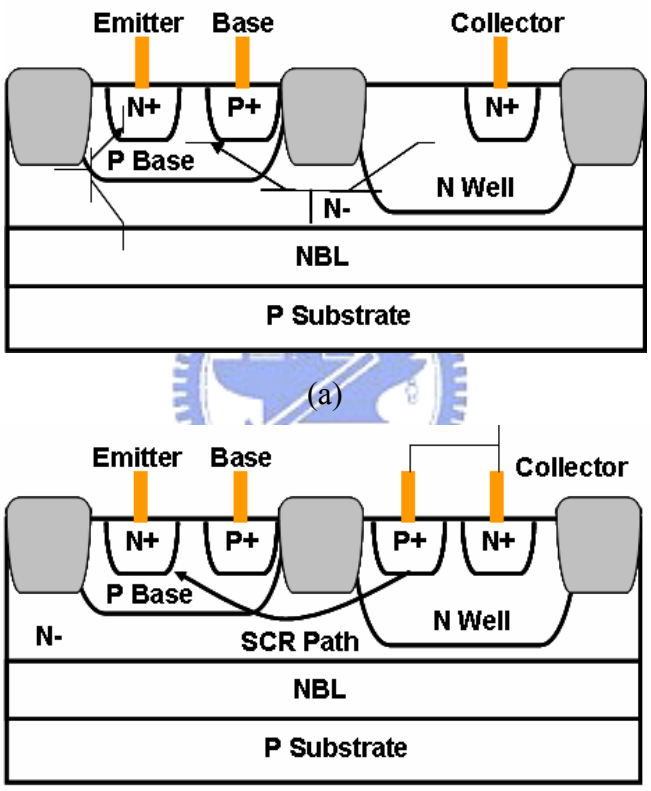


Fig. 1.19 (a) The HV NPN BJT, (b) The HV NPN-SCR, (c) The HV NSCR.

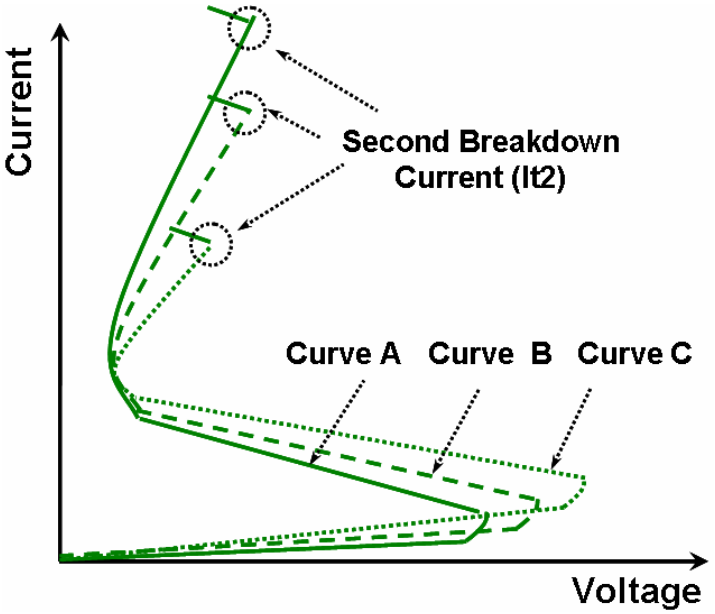


Fig. 1.20 The TLP I-V curves and turn-on resistances of the different substrate trigger current on GGNMOS (added trigger current：curve A > curve B > curve C).

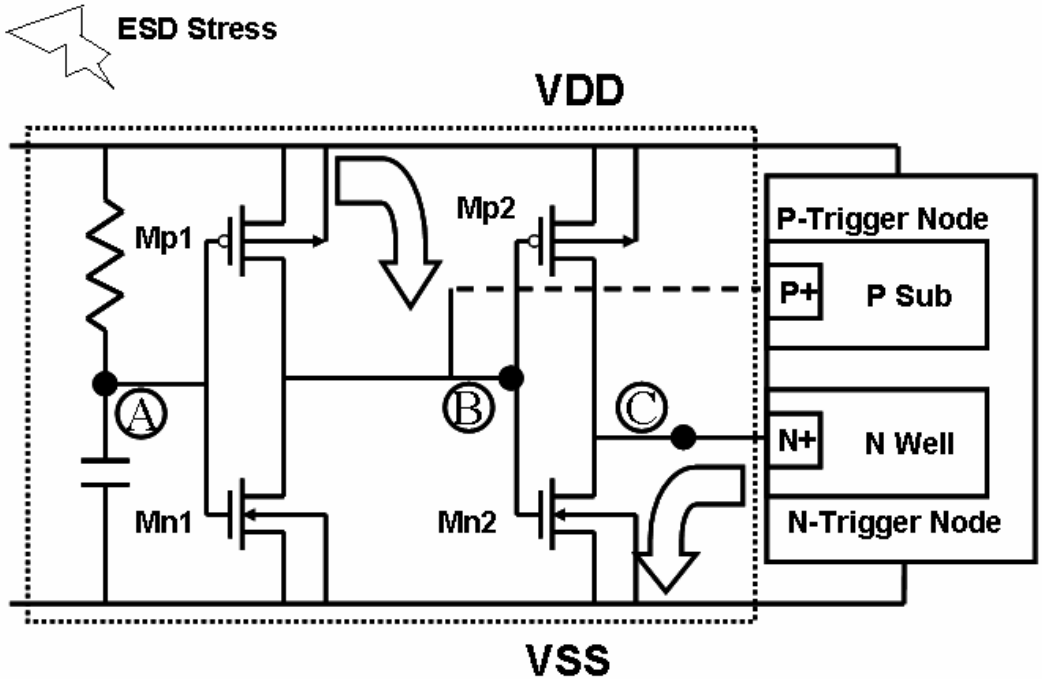


Fig. 1.21 The double-substrate-triggered structure (including the P-trigger node and N-trigger node).

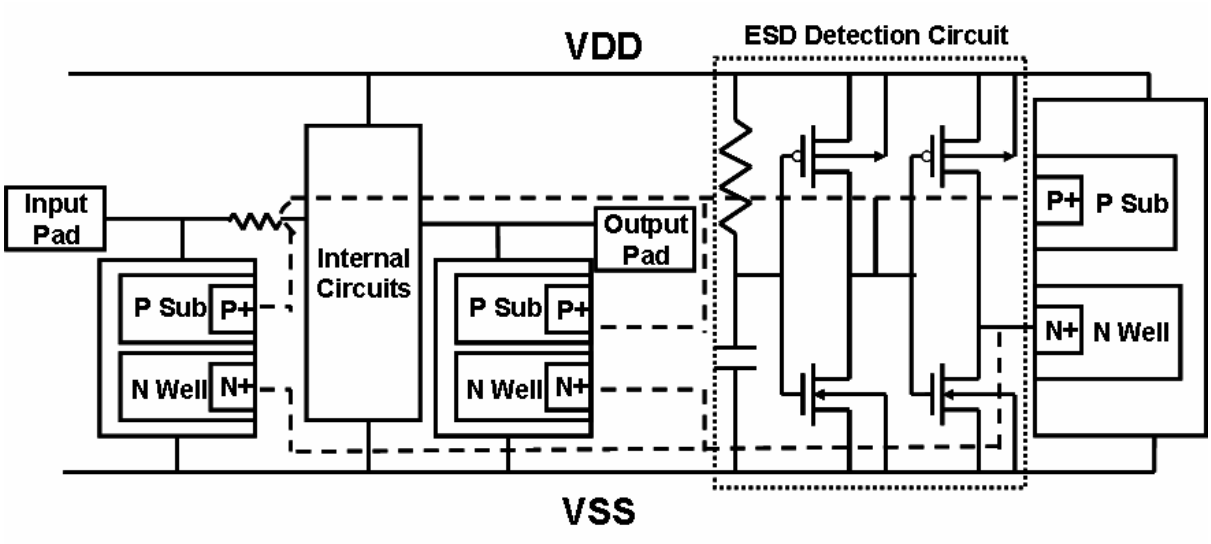


Fig. 1.22 The whole-chip ESD protection with shared ESD detection circuit for input, output and power-rail ESD clamp devices.

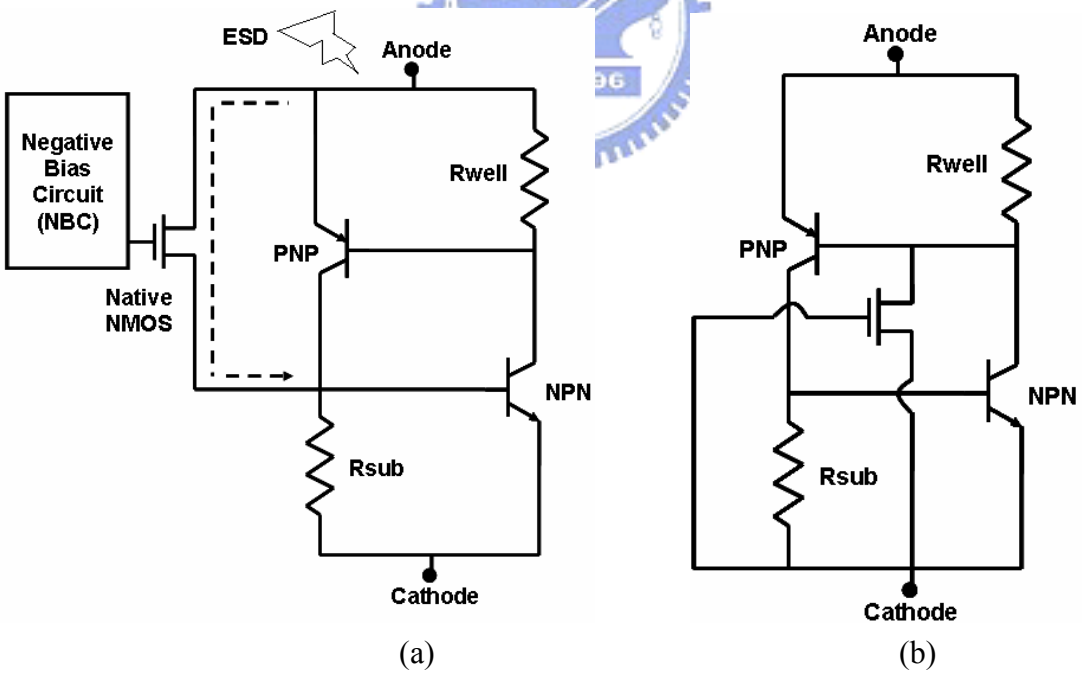
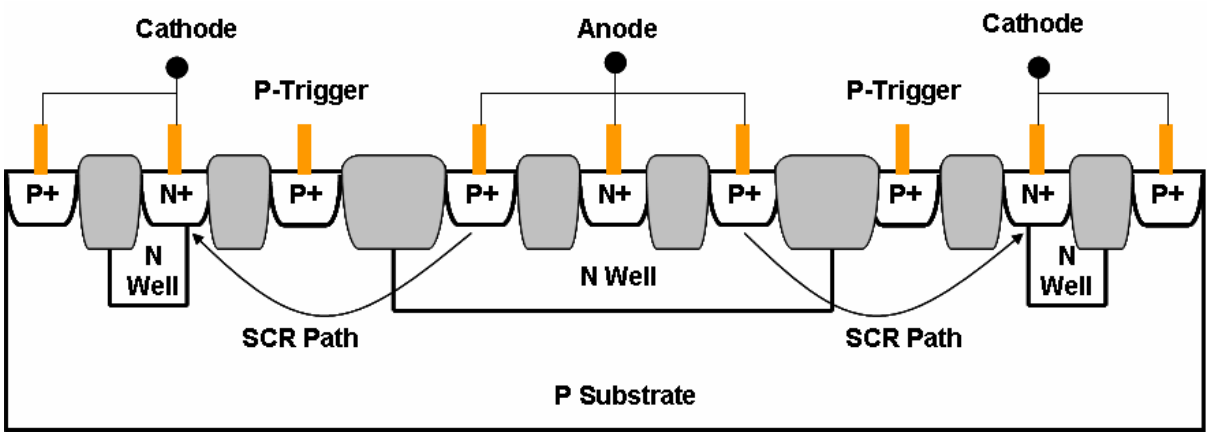
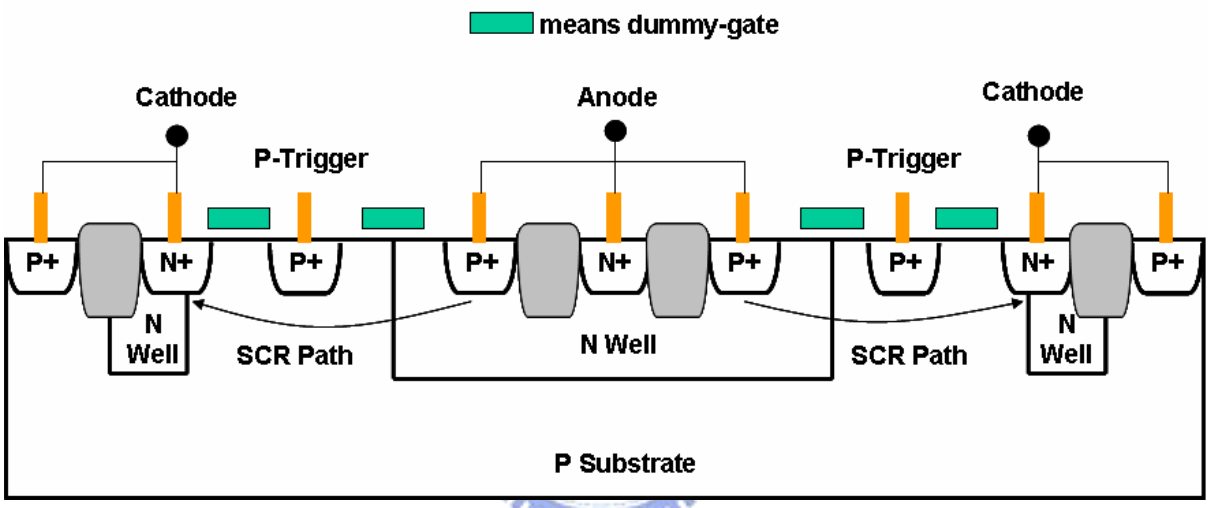


Fig. 1.23 The circuit schematics of (a) the native-NMOS-triggered SCR (NANSCR), (b) the traditional LVTSCR.



(a)



(b)

Fig. 1.24 The circuit schematics of (a) the native-NMOS-triggered SCR (NANSCR), (b) the traditional LVTSCR.

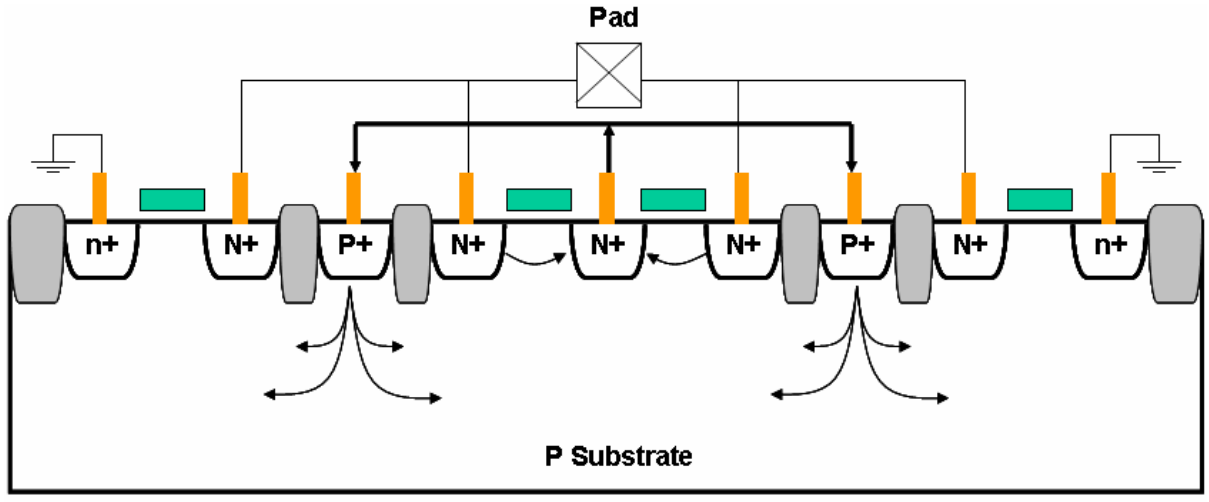


Fig. 1.25 The cross-sectional view of the self-substrate-triggered GGNMOS. The P+ trigger node connects to the source terminal of the center-finger.

CHAPTER 2

OVERVIER ON POWER MOSFETs FOR HIGH-VOLTAGE ESD PROTECTION DESIGN

2.1 Power MOS Transistors

MOS transistors can drive large amounts of power are called power transistors to distinguish them from low-power or small-signal devices. The power MOS can conduct large currents at low drain-to-source voltage by the low impendence characteristic. At low drain-to-source voltage ($V_{DS}<<V_{GS}-V_t$), the Shichman-Hodges equation in the linear region will be derived from $I_d=k(V_{GS}-V_t)V_{DS}+kV_{DS}^2/2$ to $I_d=k(V_{GS}-V_t)V_{DS}$. The on resistance $R_{DS}(on)$ varies inversely with the product of the transconductance and the effective gate voltage ($V_{GS}-V_t$), it will be $R_{DS}(on)=1/k(V_{GS}-V_t)$. The $R_{DS}(on)$ of the power MOS transistors are usually measured at a specified gate voltage V_{GS} and junction temperature. The $R_{DS}(on)$ of a power MOS transistor typically increases 50% when the junction temperature rises from 25℃ to 125℃.

The metallization resistance becomes significant for on resistance of less than an Ohm order, and the equation for $R_{DS}(on)$ then becomes $R_{DS}(on) =1/k(V_{GS}-V_t)+R_M$. Where the R_M is the sum of the resistance of the source and drain metallization. This metallization resistance is difficult to calculate because it depends on transistor geometry. There are several metal line layout patterns have been published as shown in Figs. 2.1(a) ~ 2.1(c). Fig. 2.1(a) shows a common arrangement in which both terminations lie on the same side of the transistor. The paired terminations may be more adjacent to the bond pads, but they produce excessive voltage drop and an uneven distribution of current in the device. Fig. 2.1(b) shows a better arrangement where the source and drain terminations lie on the opposite sides of the transistor. This arrangement delivers a more even distribution of current and exhibiting a lower total resistance than the pattern in Fig. 2.1(a). Fig. 2.1(c) shows the method to minimize the metallization resistance. The termination points lie on the middle of both buses, so the current does not have to flow through the full length of the buses.

The smart power integrated circuit technology is composed of VLSI digital/analog signal processing and high power output current driver on the same chip. The percentage split in chip area is uncommonly by 50% to 50% each. The signal processing part is consist of low voltage (LV) circuits；The power output current driver usually operates in high voltage (HV) and/or high current supply.

The smart power integrated circuit technology applies in Automotive Electronics, Telecommunications, Power management, LCD (Liquid Crystal Display) or EL (Electro Luminescence) industry, etc [21]. Especially the large number of column and row drivers of the LCD industry, the driving speed in dependent on the frame rate and scan rate of the display. For a refresh frame rate of 60 frames per second on the VGA definition (640 x 480), a minimum scan rate of 30 kHz is needed. For these reasons, MOS technology is preferred to approach these performances. How to improve the density and switching speed of the high voltage output transistors is the main challenge in the next generation of high-definition (HD) performance.

Power devices in smart power integrated circuit technology are usually required to perform switching functions. The gate drive characteristic of the MOSFETs is more favorable than the bipolar junction transistors (BJTs) with large base current to turn on/off. One of the main advantages of power MOSFETs is that the gate only requires a bias voltage with no steady-state current to switch between the on and off states. Due to above reasons, the inherent switching speed of MOSFETs is faster than for power BJTs.

Most high voltage devices are used as switches operating between the on and off states and designed to operate in the 1st quadrant, occasionally in the 3rd quadrant as shown in Fig. 2.2. The I-V curve is similar to the conventional MOSFETs except that the power devices usually switch between fully on and fully off – cutoff or triode region. The power devices rarely operate in the saturation region (except as amplifiers) because of power dissipation limits.

Power MOSFETs can be categorized into V-MOS, VDMOS, UMOS, IGBT and LDMOS. The V-MOS have a V-groove etch from the top side of the wafer using a preferential etch and the channel is formed along the wall of the V-groove as shown in Fig. 2.3(a). The V-MOS was the first commercial power MOSFET structure, however it is quickly replaced by the VDMOS due to manufacturing problems and the concentration of high electric field at the tip of the V-groove. The VDMOS has a conventional surface channel while still relying on double diffusion to produce the short channel length as shown in Fig.

2.3(b). The UMOS uses a trench etching technique to turn the channel into a vertical direction as shown in Fig. 2.3(c). In the V-MOS, VDMOS and UMOS, the forward blocking capability is provided by the P Well to N Epi junction. Due to higher doping concentration of the P Well region, the depletion region extends mostly into the N Epi region. Therefore, the choice of N Epi doping concentration can directly affects the breakdown voltage and on-resistance of the power MOSFETs. The IGBT (Insulated Gate Bipolar Transistor) is use the P+ substrate to replace the N+ substrate and then a merged MOS-Bipolar device can be made as shown in Fig. 2.3(d). The IGBT offers enough amounts of current handling capability, but with slower switching speed. The IGBT is a dominant power device in high current application. The V-MOS, VDMOS, UMOS, IGBT as above are vertical devices, the drawback of the vertical devices is that it is difficult to include multiple power devices on the same chip. But the lateral structure allows all terminals to be accessed from the top surface of the chip.

The current flows from the drain, laterally along the surface through the MOS channel and up into the source, hence the name Lateral Double-Diffused MOSFETs (LDMOS) as shown in Fig. 2.4(a) [22]-[25]. LDMOS generally has a higher on-resistance due to the longer current path than vertical devices. Furthermore, the breakdown voltage of the LDMOS depends critically on the curvature of the P Well to N Drift region junction. In order to obtain high breakdown voltage, it is necessary to use a low doping concentration in the N Drift region. However, this will cause a high turn-on resistance.

To provide a device with high breakdown voltage and low turn-on resistance, an advanced technique called REduced SURface Field (RESURF) was developed as shown in Fig. 2.4(b) [26]-[27]. The RESURF device structure is the same as the LDMOS, except the much thinner N Epi layer is added for the N Drift region. Through a well-tuning doping concentration in the N Drift region, a much lower turn-on resistance can be produced without decreasing in breakdown voltage.

The breakdown voltage of LDMOS is mainly between 20 V to 100 V and is more suitable for automotive applications. The remaining issue is to reduce the series resistance of the metal interconnection and bonding wires. Due to the specific lower on-resistance and high breakdown voltage, the LDMOS can as for output current driver and self high-voltage ESD protection device simultaneously.

This chapter will discuss the whole mechanisms of the LDMOS including the turn-on mechanism, the double-snapback characteristic and the isolation method to implement the high breakdown voltage.

2.2 The Turn-On Mechanism and Double-Snapback Characteristic of the High-Voltage LD-NMOS and High-Voltage NMOS Devices

The turn-on mechanism of the LD-NMOS device is caused by the positive feedback between the turn-on BJT of the source side and the N/N+ junction avalanche breakdown of the drain side and it's called the double snapback characteristic. Although the N/N+ junction is the most basic parasitic structure in the device, which plays a major role in the snapback characteristic.

In order to analyze the I-V curve of the LD-NMOS structure, there are three points that have been sampled as shown in Fig. 2.5(a). Point A denotes the turn-on BJT of the source side and the point C denotes the N/N+ junction avalanche breakdown of the drain side. With increasing the applied voltage in the drain side, the more excess electrons from the N+ source induce the more excess holes from N+ drain in the HV N Well/P Body junction. These space charges will become denser at the junction and raise the electric field. Moreover, one part region of the HV N Well with excess holes become an extension of the P Body layer. In other words, this effect is the same as the "Kirk effect [28]-[29]" of the BJT and the extension region will reach the N+ drain region until the excess electrons concentration is less than the N+ drain doping concentration. As a result, the electrical field peak moves from the HV N Well/P Body junction to the N/N+ junction of the drain side, as shown in Fig. 2.5(b). This electric field peak leads the N/N+ junction avalanche breakdown and feedbacks additional hole current to the P Body.

The electric field of point A is large enough to trigger the impact ionization effect and the electric field of point B will enhance the ionization. Due to the avalanche multiplication occurred in the HV N Well/P Body junction, the voltage to sustain the junction breakdown is reduced, and then it snapbacks to low voltage and causes a negative slope after point A. Point C denotes the electric field peak reaches the N/N+ junction to cause the junction avalanche breakdown. Then, the feedback hole current will improve the multiplication effect in the HV N Well/P Body junction and snapback to low voltage again.

Compared to other structure of HV device, the HV NMOS with deeper N Well and N+ Buried Layer (NBL) can also have the double snapback characteristic, as shown in Fig. 2.6(a). Due to the doping concentration of the NBL is higher than the N Well region, the breakdown

voltage is determined by the NBL/P Well junction and the first snapback is caused by the turn-on of BJT. After turn-on the BJT, the current flows vertically into the NBL region will result in a longer current path and the turn-on resistance will become larger. When the current further increases, the “Kirk effect” happens and the electric field peak moves from NBL/P Well junction to N Well/N+ junction. Then, the N Well/N+ junction will go into avalanche breakdown and increase the multiplication rate to snapback to lower holding voltage, as shown in Fig. 2.6(b). The current path of this HV structure will be changed from vertical path to lateral path and get a smaller turn-on resistance after the second snapback.

But not all HV devices have the double snapback characteristic [30], if the current path will not change, the second snapback characteristic will be not obvious or be no longer exist. Figs. 2.7(a) and 2.7(b) show the HV device structure without the double snapback characteristic and its TLP I-V curve. The shallow N Grade region is to sustain the high breakdown voltage, before and after the N Grade/P Well junction breakdown, the current path is always in the lateral direction.

2.3 The Isolation Technique of High-Voltage Devices

There are two isolation techniques have been reported to reach the high breakdown voltage. The first isolation method is called the self isolation. It is mostly used in MOS technology and the source and drain junction isolate by itself under reverse bias, as shown in Fig. 2.8(a). In addition, the potential of source will be always grounded. The second isolation method is called the junction isolation, the device will be enclosed by the PN junction and the potential of source may be above ground potential, as shown in Fig. 2.8(b). With such kinds of isolation technique, the trigger voltage of the ESD protection device can be increased and resist the external noises.

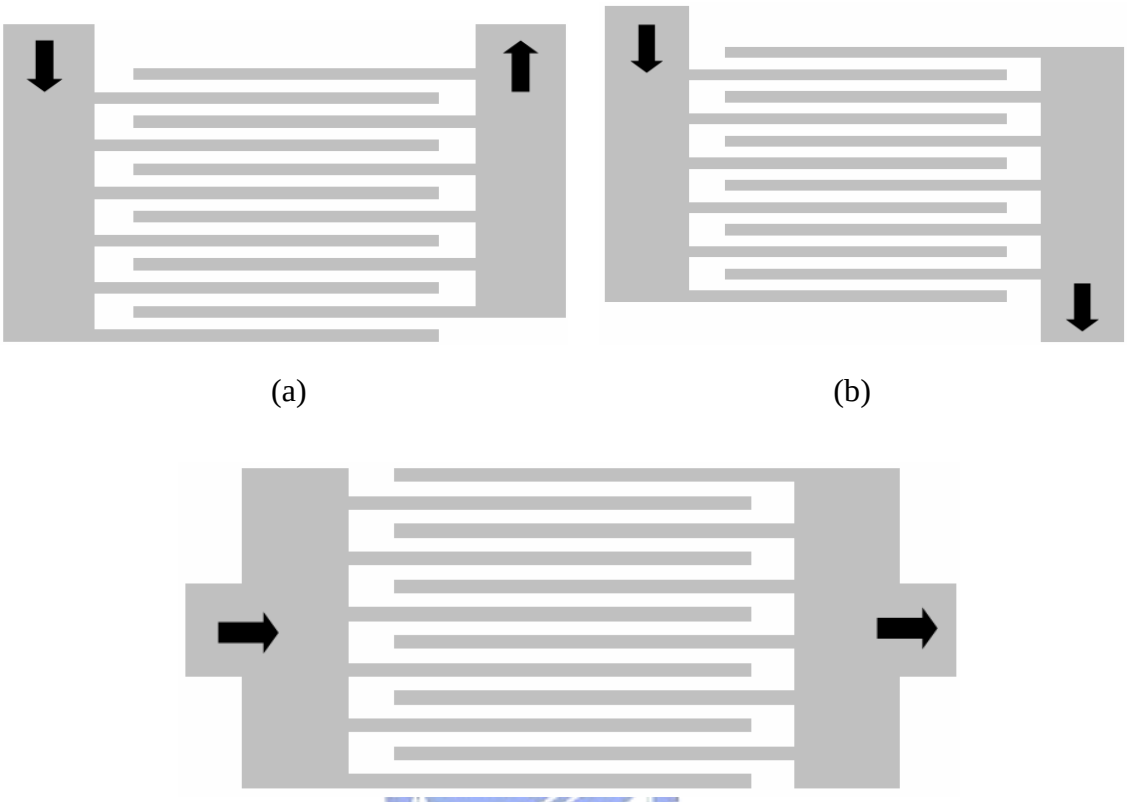


Fig. 2.1 Three kinds of layout patterns and its current flow path (a) The layout structure of the same side current flow, (b) The layout structure of the opposite side current flow, (b) The layout structure of the minimum metallization.

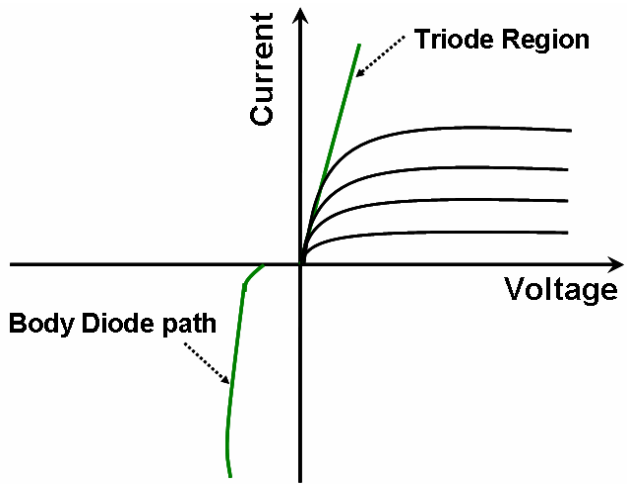


Fig. 2.2 The operation region of the power transistors.

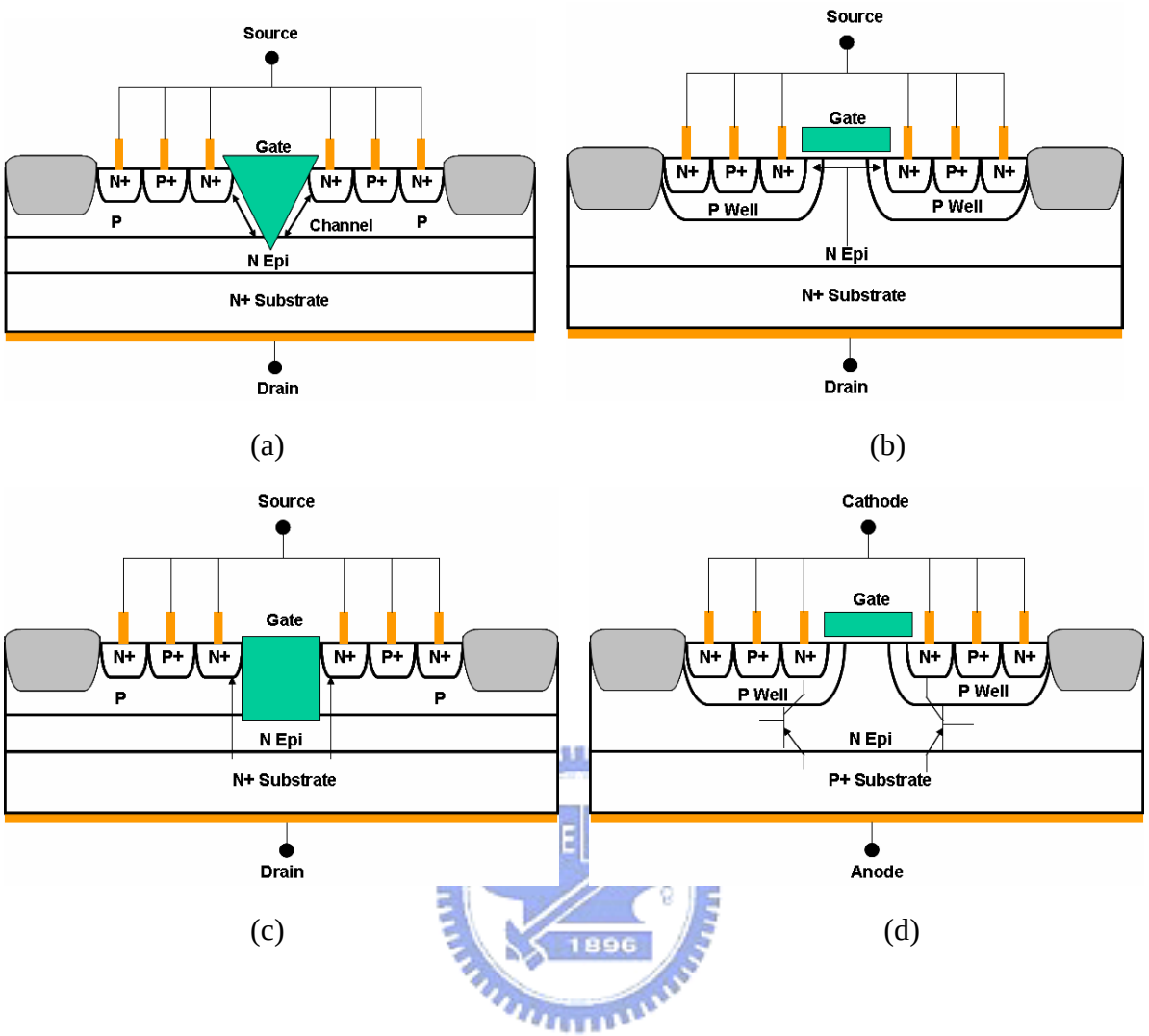


Fig. 2.3 Four kinds cross-sectional views of power devices: (a) The VMOS device, (b) The VDMOS device, (c) The UMOS device, (d) The IGBT device.

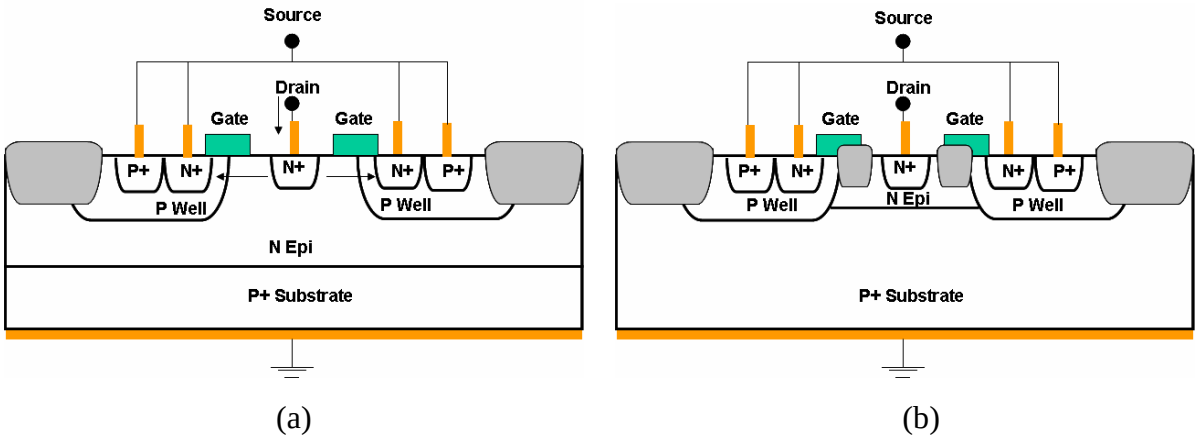
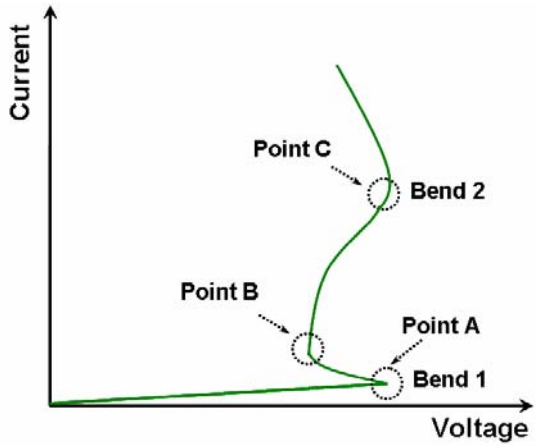
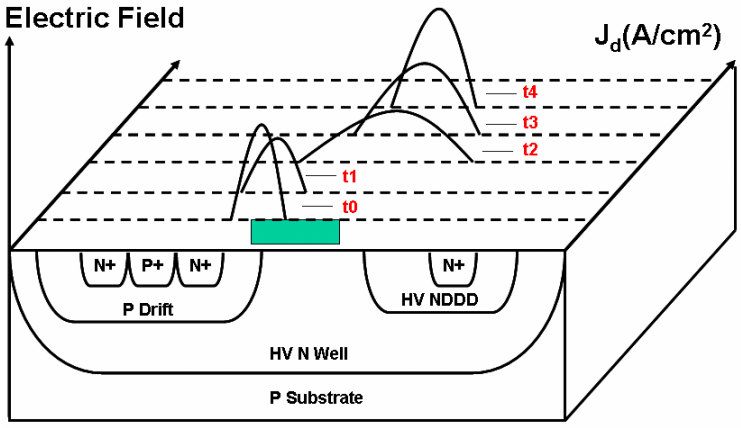


Fig. 2.4 (a) The LDMOS device, (b) The RESURF device.

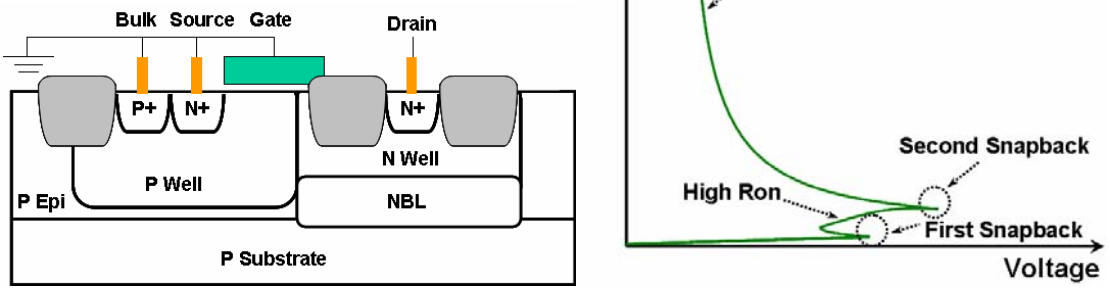


(a)



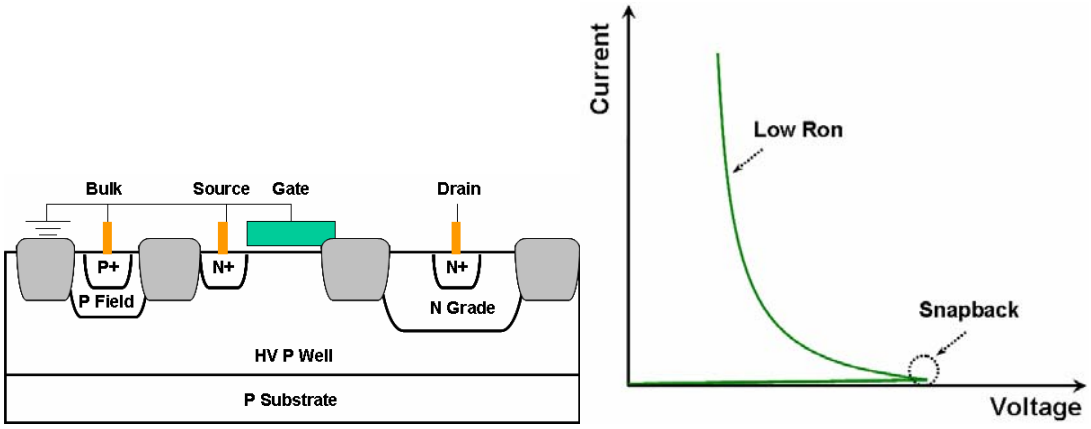
(b)

Fig. 2.5 (a) The three TLP I-V sampled points of LD-NMOS, (b) The electric field distribution versus the applied current.



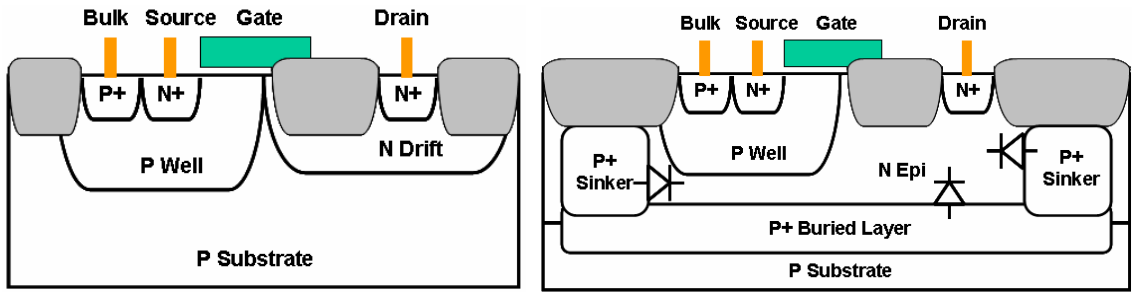
(a) (b)

Fig. 2.6 (a) The device structure with double snapback characteristic of HV NMOS, (b) The TLP I-V curve of device structure with double snapback characteristic of HV NMOS.



(a) (b)

Fig. 2.7 (a) The device structure without double snapback characteristic of HV NMOS, (b) The TLP I-V curve of device structure without double snapback characteristic of HV NMOS.



(a) (b)

Fig. 2.8 (a) The self isolation structure, (b) The junction isolation structure.

CHAPTER 3

DEVICE PARAMETERS MODIFICATION FOR HIGH-VOLTAGE ESD PROTECTION DESIGN

The high-voltage (HV) ESD protection devices should be provided with a higher breakdown voltage than operation voltage to guarantee they won't be triggered in normal circuit operation. The method of providing a higher breakdown voltage is usually through a low doped layer under the drain side. This chapter will introduce some HV devices that have been reported and present the experimental results of HV LD-NMOS, HV LD-PMOS, HV N-type Field Oxide Device (NFOD), HV Dual-Direction Silicon Controlled Rectifier (DD-SCR) and HV NMOS with embedded SCR (NSCR) in a 0.25μm 18V BCD technology.

3.1 The High-Voltage ESD Protection Devices

There are several high-voltage ESD protection devices that have been developed in different two processes. In the high-voltage (HV) process, a low doping layer is added in the drain and source sides named DDD-structure to increase the breakdown voltage. The ESD robustness of the asymmetric structure is better than symmetric structure in the HV process as described in chapter 1. The asymmetric structure means the DDD layer is added in the drain side. In the Bipolar-CMOS-DMOS (BCD) process [31]-[35], there are BJT, CMOS and DMOS to use in the high-voltage operation. In addition, the diode with high reverse breakdown voltage and high-voltage SCR are also available in these two processes.

3.1.1 The High-Voltage Bipolar Junction Transistor with Controllable Trigger and Holding Voltage

To provide effective whole-chip ESD protection, on-chip ESD protection devices are added in different parts of ICs. The required ESD specification of breakdown voltage, trigger

voltage and holding voltage in each part are different. So, this requires devices with high electrical flexibility to meet the different ESD specifications.

In the BCD process, the high-voltage bipolar junction transistor (HV BJT) with controllable trigger and holding voltage has been developed by well-adjusted layout parameter, as shown in Fig. 3.1 [36]. The holding voltage can be controlled by changing the "d" spacing (the clearance between P Body edge and N+ emitter); the trigger voltage can be controlled by changing the "t" spacing (the distance between P Body and N Well), respectively.

In order to understand the physical mechanism of the influence on changing each layout parameter, to investigate the current flow, electrical field and the impact ionization in the device is necessary. Due to the junction breakdown is happened at P Body/N- junction, with the increasing of the "t" spacing, the breakdown and the trigger voltage can be both increased as shown in Fig. 3.2(a) [36].

Moreover, there are two current paths can trigger the HV BJT device, a lateral one and a vertical one via the N+ Buried Layer (NBL). To find out the effect on different "d" spacing, the TLP I-V curve shows the current path can be changed from lateral bipolar path to vertical bipolar path, as shown in Fig. 3.2(b) [36]. If the applied voltage exceeds the breakdown voltage of P Body/N- junction in small "d" spacing, the device enters the first snapback state and the impact ionization happens on the surface of P Body/N- junction. When the current further increases, the Kirk effect happens and push the maximum electric field peak from the P Body/N- junction to the collector N Well/N+ junction. In this higher doped region (N Well/N+), due to the higher multiplication rate, a lower electric field can reach the same avalanche current to bring the device into second snapback state resulting in the low holding voltage.

With the larger "d" spacing, the device behavior is completely different due to the carrier recombination of the electron. The larger base width can let more electron current be recombined by the base hole current. Therefore, the bipolar current gain (β) degrades with increasing the base width. By the decreased current gain of the lateral NPN BJT, the lateral NPN will be turned off. The NBL is a high doping N-type layer, which constructs a low impedance current path to shunt the ESD current through the vertical NPN BJT. The impact ionization and the base-widening effect will reach the NBL layer, and then the second snapback occurs. Due to the doping profile of NBL is lower than the N+/N Well region, the multiplication rate is also lower than the N Well/N+ region and the holding voltage may be much higher than the lateral NPN.

In summary, by tuning the “t” spacing, the breakdown and trigger voltage can be increased; by tuning the “d” spacing, the turn-on type of the bipolar junction transistor and the holding voltage can be selected.

3.1.2 The High-Voltage NMOS with Embedded SCR Structure (NSCR)

The HV NMOS has poor ESD robustness compared to LV NMOS. To increase the ESD robustness, the conventional method is to use the large device structure, but it suffers non-uniform turn-on issue. This non-uniform turn-on phenomenon in HV NMOS is caused by the strong snapback characteristic during ESD stress. The gate-coupled technique can alleviate this issue, but the added gate-grounded resistor sacrifices a large layout area.

In order to increase the breakdown voltage, the N Grade region below the N+ diffusion [37]-[38] and the field oxide between the drain side and the polygate can be used. The P Field under the bulk is for device isolation. The higher breakdown voltage causes higher electrical field and more interface trap in the field oxide. An optional low doped N-type layer named N Drift implant below the field oxide can minimize the peak electric field and let the device avoid the hot-carrier effect, but it also cause a longer current path from drain to source, as shown in Fig. 3.3(a) [38]. Due to the drift layer and the grade region are of the same type, the current will flow into the drift layer first and then to the source side. This current flow causes current-crowding in the N Drift region. On the contrary, the device without the drift layer has more uniform current distribution from drain to source. With the increasing of the “d” spacing, the trigger voltage of device with drift implant will be increased by the longer current path. The trigger voltage of device without Drift implant is kept the same because the trigger voltage is determined by the N Grade/ HV P Well junction. Therefore, the HV NMOS without the drift implant can switch quickly and have better It2 level. In addition, the HV PMOS also has the same effect.

The HV N-type SCR (HV NSCR) is to insert a P+ diffusion in the drain side of the HV NMOS to form a SCR path, as shown in Fig. 3.3(b) [38]. The HV NSCR is a NMOS triggered SCR, due to the trigger voltage of SCR is always higher than NMOS, and the NMOS will be triggered first during ESD stress. Then, the SCR will be triggered and snapback to its low holding voltage and high It2 characteristic. In fact, a part of current can flow from P+ diffusion to HV P Well to trigger on the parasitic vertical PNP BJT earlier and the turn-on parasitic PNP BJT can also provide current to trigger the other parasitic NPN BJT. To compare with the trigger voltage of HV NMOS and HV NSCR, the trigger voltage of HV

NSCR is smaller than the HV NMOS. With the increasing of "d" spacing, the trigger voltage and the holding voltage of HV NSCR with N Drift implant will be increased. So, the It2 value of HV NSCR without the N Drift implant is higher than the HV NSCR with the N Drift implant.

3.1.3 The High-Voltage BJT with Embedded SCR Structure (B-SCR)

The bipolar-triggered SCR (B-SCR) device consists of a added P+ diffusion in the collector of the NPN transistor, this device can conduct much higher current than NPN transistor, as shown in Fig. 3.4 [39]. Both the trigger voltage and the ESD protection capability of NPN-triggered B-SCR depend on the P+ spacing. Under small P+ spacing about 5μm, the trigger voltage is similar to that of NPN BJT. With increasing the P+ spacing from 5μm to 10μm, the trigger voltage can be decreased substantially, as shown in Fig. 3.5 [39]. On the other hand, the larger P+ spacing decreases the It2 value.

3.2 Experimental Results

Five kinds of HV ESD protection devices have been investigated : LD-NMOS, LD-PMOS, NFOD, dual-direction SCR and NSCR. They are manufactured in a 0.25μm 18V BCD technology, the additional mask layers are HV N Well, HV NDDD, HV PDDD and P Drift. All of them are lightly doped layers and they are used to increase the breakdown voltage. The doping concentration of Drift layer is higher than DDD layer.

3.2.1 The High-Voltage LD-NMOS

The device cross-sectional view and layout view of HV LD-NMOS in the given 0.25μm 18V BCD process are shown in Figs. 3.6(a) and 3.6(b), respectively. The HV LD-NMOS is fabricated in the HV N Well and the source and bulk regions are inside it. The effective channel length is the overlap region of the P Drift and the polygate; the HV NDDD layer in the drain region is used to increase the breakdown voltage; the HV RPO (Resistor Protect Oxide) layer is used to block the silicide region and increase the surface resistance between the drain side and polygate. The breakdown voltage is determined by the HV N Well/P Drift junction while the LD-NMOS is gate-grounded and the ESD pulse is zapped at drain side. In

addition, the β gain of the parasitic NPN transistor is large enough to cause strong snapback characteristic after the device enters trigger state.

The split layout parameters are the N+ edge to contact spacing of the drain side named N_C, the OD region beyond N+ edge of the drain side named D_O, the HV NDDD spacing of the drain side named H_N, the P+ edge to polygate spacing of the source side named P_P and the device total width named W.

To measure the TLP I-V curve, the failure criterion is determined by the leakage current over 1μA when the drain bias is 18V. With increasing the device total width from 400μm to 800μm (one finger width is 50μm), the trigger voltage, holding voltage and the It2 value can be increased a little due to the non-uniform turn-on characteristic of the LD-NMOS is more serious than traditional NMOS, as shown in Figs. 3.7(a) and 3.7(b). With increasing the D_O and P_P spacing of the drain side and source side, the holding voltage will be raised and the It2 value will be decreased due to the total power dissipation is kept the same, as shown in Figs.3.8 and 3.9, respectively. With increasing the N_C spacing of the drain side, the ballast resistance of the surface will be increased and the ESD current can flow deeper to protect the gate oxide. Therefore, the holding voltage can be increased due to the longer current path from drain to source and the It2 value can be increased due to the deeper current path have higher current conduction area. With increasing the N_C spacing from 1μm to 4μm, the holding voltage can be doubled and the It2 value can be increased from 0.2A to 2.5A, as shown in Figs. 3.10(a) and 3.10(b). With increasing the N_C spacing from 1μm to 3μm and H_N spacing from 9μm to 18μm on the same time, the holding voltage and It2 value seem to not change substantially, as shown in Figs. 3.11 ~ 3.13. But, when the N_C spacing is 4μm, the holding voltage and It2 value are decreased with the H_N spacing increasing. The maximum holding voltage and It2 value can be implemented by N_C spacing with 4μm and H_N spacing with 9μm, as shown in Figs. 3.14(a) and 3.14(b). Moreover, the leakage will be improved to 0.1 nano ampere order while the N_C spacing is above 1μm, as shown in Figs. 3.7 ~ 3.14.

The HBM and MM robustness are measured by HANWA ESD simulator HED W5100D, the failure criterion is determined by the I-V curve shifts over 30%. Table 3.1 ~ 3.4 show the HBM and MM ESD levels in different layout parameters of LD-NMOS as above, the HBM level will pass 2kV and the MM level will pass 200V when the N_C spacing is 3μm or above. Therefore, the N_C spacing is the critical ESD design parameter.

In addition, to investigate the influence on separating the source and bulk regions, there

are four layout parameters to discuss with the source to bulk spacing (S_B). The four layout parameters are device total width, polygate length and channel length, as shown in Fig. 3.15. Theoretically, with increasing the S_B spacing, the breakdown voltage will not change, but the current should flow through an added resistor built by the separation of the source and bulk region. Then, the trigger voltage will be increased to turn-on the device.

With increasing the total width from 100 and 200μm and S_B spacing from 0 and 2μm, the measurement shows that the larger total width can obtain larger It2 level and the no butted structure is suitable for the larger total width uniform turn-on, as shown in Figs. 3.16(a) ~ 3.16(c). With increasing channel length from 0.35 and 0.5μm and S_B spacing from 0 and 2μm, the better It2 level can be obtained by smaller channel length and butted structure, as shown in Figs. 3.17(a) ~ 3.17(c). With increasing the polygate length from 1 and 1.5μm and S_B spacing from 0 and 2μm, the trigger voltage will be increased by larger polygate length substantially due to the current flow through an added path in HV N Well region and the better It2 level can be obtained by smaller polygate length and butted structure, as shown in Figs. 3.18(a) ~ 3.18(c). Therefore, the butted structure, relative small channel length and polygate length are suitable for LD-NMOS to be a ESD protection device.

3.2.2 The High-Voltage LD-PMOS

Figs. 3.19(a) and 3.19(b) shows the cross-sectional and layout view of the LD-PMOS, the LD-PMOS is fabricated in the HV N Well as the LD-NMOS. The effective channel length is the polygate length subtracts its overlap region of the HV PDDD layer. The HV PDDD layer is used to increase the breakdown voltage. Due to the β gain of PNP transistor is smaller than NPN transistor, the snapback characteristic will be reduced to very unapparent. The breakdown voltage is determined by the HV N Well/HV PDDD junction while the LD-PMOS is gate-VDD and the ESD pulse is zapped at source side.

The split layout parameters are the P+ edge to contact spacing of the drain side named P_C, the HV PDDD spacing of the drain side named H_P, the N+ edge to polygate spacing of the source side named N_P and the device total width named W.

To measure the TLP I-V curve, the failure criterion is also determined by the leakage current over 1μA when the gate bias is 18V. With increasing the device total width from 400μm to 800μm, the trigger voltage is almost the same, but holding voltage will be decreased and It2 value will be increased, as shown in Figs. 3.20(a) and 3.20(b). With

increasing the H_P spacing from 6μm to 15μm, the trigger and holding voltage are almost the same, but the It2 value will be decreased, as shown in Figs. 3.21(a) and 3.21(b). With increasing the P_C spacing from 1μm to 3μm, the trigger and holding voltage are almost the same, but the It2 value will be increased, as shown in Figs. 3.22(a) and 3.22(b). With increasing the N_P spacing from 1μm to 4μm, the trigger voltage is almost the same, but the holding voltage will be decreased and the It2 value will be increased, as shown in Figs. 3.23(a) and 3.23(b). Moreover, the It2 value of LD-PMOS is too low in different layout splits.

Table 3.5 ~ 3.8 show the HBM and MM ESD levels of different layout parameters of LD-PMOS as above, the HBM and MM level are too low to pass the specification 2kV and 200V, respectively. Therefore, the LD-PMOS is not suitable to be a ESD protection device.

3.2.3 The High-Voltage NFOD

The N-type Field Oxide Device (NFOD) is fabricated through replacing the gate oxide by the Shallow Trench Isolation (STI), as shown in Fig. 3.24. The NFOD will be turned on by the parasitic NPN transistor turn-on due to the channel is no longer exist. To investigate the influence on ESD performance, there are four layout parameters have to be discuss, the device total width named W, STI spacing named S, N+ edge to contact spacing of drain side named N_C and source to bulk spacing named S_B. In addition, the C spacing means the P Drift edge to STI edge spacing and it is fixed at 0.5μm.

With increasing the total width from 100μm to 200μm (one finger width is 50μm) and S_B spacing from 0 and 2μm, the trigger and holding voltage are almost the same no matter what the S_B spacing is. But the larger S_B spacing reduces the It2 value apparently when the width is 200μm, as shown in Figs. 3.25(a) ~ 3.25(c). With increasing the S spacing from 1 and 1.5μm and S_B spacing from 0 and 2μm, the trigger voltage will be increased substantially due to the added path in the HV N Well region and the holding will be increased a little. The It2 value will be higher when the S_B spacing is 2μm, as shown in Figs. 3.26(a) ~ 3.26(c). With increasing the N_C spacing from 2 and 4μm and S_B spacing from 0 and 2μm, the trigger and holding voltage are almost the same no matter what the S_B spacing is, but the It2 value will be increased apparently. Moreover, when the S_B spacing is 2μm, the It2 value can be increased a little, as shown in Figs. 3.27(a) ~ 3.27(c).

Therefore, the better ESD performance in NFOD can be obtained by larger device total width, larger N_C spacing and butted structure. In addition, the leakage current of the

different NFOD as above are all in 0.1 nano ampere order before the device is destroyed.

3.2.4 The High-Voltage Dual-Direction SCR

There are three kinds of dual-direction SCR have been tested, the dual-direction structure is used when the power supply is operate between negative to positive voltage. Figs. 3.28 (a) and 3.28(b) show cross-sectional view and the layout diagram of the type I SCR, it is fabricated in the HV N Well and the HV N Well is floating. The parasitic diode is no longer exist than traditional SCR device. There are two SCR path in this structure, the path 1 (P+ (P Drift) /HV N Well/P Drift/N+) from left to right side is a short path when node 1 is zapped and node 2 is grounded, the path 2 (P+ (P Drift) /HV N Well/P Drift/N+) from right to left side is a long path when node 2 is zapped and node 1 is grounded. In addition, the width of this dual-direction SCR is 50μm.

There are two layout parameters to be tested in the type I SCR, the P+ edge to STI edge spacing named C and the STI spacing named S. With increasing the C spacing from 1 and 4μm and fix the S spacing at 2 and 3μm, the holding voltage can be increased substantially in path 2 and the holding voltage can be increased a little in path 1, as shown in Figs. 3.29(a) and 3.29(b), 3.30(a) and 3.30(b). The reason why the holding voltage of path 2 is higher than path 1 is the longer current path. With increasing the S spacing from 2 and 4μm and fix the C spacing at 3μm, the holding will be also increased in path 1 and path 2 but not obvious than tuning the C spacing, as shown in Figs. 3.31(a) and 3.31(b). Therefore, the C spacing is the dominant factor to improve the holding voltage in type I SCR

Fig. 3.32 shows the type II SCR structure, this dual-direction SCR is fabricated in the P Substrate and the P Substrate is floating. The low doping concentration layers of HV PDDD and HV NDDD are used to increase the breakdown voltage and the type III SCR is to replace the HV PDDD layer by the P Drift layer, as shown in Fig. 3.34. The modified layout parameter of type II and III SCR is the STI spacing named S. With increasing the S spacing from 8 and 14μm, the holding voltage can be both increased about 5V and the holding voltage of path 2 is over the operation voltage 18V to avoid the latchup issue in type II and III SCR, as shown in Figs. 3.33(a) and 3.33 (b), 3.35(a) and 3.35(b).

The It2 value of these three kinds of SCR are all passed 5A in path 1 and 4A in path 2 The HBM and MM level of them are all passed 8kV and 400V in path 1, respectively. With increasing the modified parameter spacing, the HBM and MM level can be increased about 6kV and 300V, respectively, as shown in Figs. 3.29(c) and 3.29 (d), 3.30(c) and 3.30(d),

3.31(c) and 3.31(d), 3.33(c) and 3.33(d), 3.35(c) and 3.35(d). In addition, the leakage current of these three types SCR are all in pico ampere order before the device is destroyed. Therefore, the SCR devices have the best ESD performance in It2 value, HBM level and MM level than other devices.

3.2.5 The High-Voltage NSCR

The NSCR is made by inserting a P+ diffusion in the drain side of the LD-NMOS to establish a SCR path from drain to source [40]. Due to the doping concentration of the N Well is higher than the HV NDDD, by adding the N Well beneath the P+ diffusion of the drain side can be used to conduct currents into the HV N Well and hence increase the turn-on speed of the NSCR, as shown in Fig. 3.36. The NSCR is a LD-NMOS triggered SCR, where the LD-NMOS is used to triggered the SCR. Therefore, the trigger voltage is almost the same as LD-NMOS. Some variation still exists due to the injection hole currents from the anode of the SCR.

There are three layout parameters be modified to find the ESD rule, the device total width named W, the N+ edge to contact spacing of the drain side named N_C, the polygate length and the channel length. With increasing the total width from 100μm to 200μm (one finger width is 50μm) and S_B spacing from 0 and 2μm, the holding voltage are almost the same no matter what the S_B spacing is and the larger It2 value can be obtained by larger total width and butted structure, as shown in Figs. 3.37(a) ~ 3.37(c). With increasing the N_C spacing from 2μm to 4μm and S_B spacing from 0 and 2μm, the higher holding voltage and It2 value can be obtained by larger N_C spacing, as shown in Figs. 3.38(a) ~ 3.38(c). With increasing the polygate length from 1μm to 1.5μm and S_B spacing from 0 and 2μm, the trigger voltage can be increased substantially by the added current path in the HV N Well region. The higher It2 value can be obtained by larger S_B spacing when the polygate length is relative small, as shown in Figs. 3.39(a) ~ 3.39(c). With increasing the channel length from 0.35μm to 0.5μm and S_B spacing from 0 and 2μm, the higher It2 value can be obtained by larger channel length and S_B spacing, as shown in Figs. 3.40(a) ~ 3.40(c).

The It2 value as above NSCR devices are almost 2A and the holding voltage is higher than that of the traditional SCR. Moreover, the leakage current of the NSCR is in 0.1 nano ampere order before the device is destroyed. Therefore, the better ESD performance of the NSCR can be obtained by larger total width, N_C spacing and channel length.

3.3 Summary

In 0.25μm 18V BCD process, to increase the N_C spacing of drain side in LD-NMOS can improve the holding voltage, It2 value, HBM and MM ESD levels. The larger N_C spacing can also improve the It2 value in both NFOD and NSCR devices. Moreover, with increasing the polygate length and S spacing in LD-NMOS, NSCR and NFOD, respectively, the trigger voltage is increased substantially. In LD-PMOS, no matter how to modify the layout parameters, the ESD robustness is not improved. So, the LD-PMOS is not a good ESD protection device. In dual-direction SCR, a holding voltage higher than the operation voltage can be obtained by designing proper longitude spacing. The It2 value, HBM and MM ESD levels are higher than the standard ESD specification.

Table 3.1

Various ESD Characteristics of LD-NMOS in different device total width (W).

N_C Spacing (μm)	0.3		
D_O Spacing (μm)	1		
P_P Spacing (μm)	1		
H_N Spacing (μm)	6		
W (μm)	400	600	800
Trigger Voltage (V)	25.71	26.3	26.8
Holding Voltage By TLP (V)	4.2	4.377	4.54
Holding Voltage By 370 (V)	2.2	2.3	2.3
It2 (A)	0.407	0.41	0.418
HBM Level (kV)	0.5	0.5	0.5
MM Level (V)	50	50	50

Table 3.2

Various ESD Characteristics of LD-NMOS in different OD region beyond N+ region of drain side (D_O).

W (μm)	400		
P_P Spacing (μm)	1		
N_C Spacing (μm)	0.3		
H_N Spacing (μm)	6		
D_O Spacing (μm)	1	2	3
Trigger Voltage (V)	25.9	26.1	25.9
Holding Voltage By TLP (V)	5.036	5.216	5.513
Holding Voltage By 370 (V)	2.1	2.2	2.2
It2 (A)	0.444	0.4	0.383
HBM Level (kV)	0.5	0.5	0.5
MM Level (V)	50	50	50

Table 3.3

Various ESD Characteristics of LD-NMOS in different P+ edge to polygate spacing of source side (P_P).

W (μm)	400		
D_O Spacing (μm)	1		
N_C Spacing (μm)	0.3		
H_N Spacing (μm)	6		
P_P Spacing (μm)	1	2	3
Trigger Voltage (V)	25.7	26.2	26.7
Holding Voltage By TLP (V)	5.436	5.558	6.182
Holding Voltage By 370 (V)	2.1	2.2	2.4
It2 (A)	0.392	0.375	0.372
HBM Level (kV)	0.5	0.5	0.5
MM Level (V)	50	50	50

Table 3.4

Various ESD Characteristics of LD-NMOS in different HV NDDD spacing (H_N) and N+ edge to contact spacing (N_C) of drain side.

(a)

W (μm)	400								
D_O Spacing (μm)	1								
P_P Spacing (μm)	1								
H_N Spacing (μm)	9				12				
N_C Spacing (μm)	1	2	3	4	1	2	3	4	5
Trigger Voltage (V)	25.7	26.3	26.2	26.3	26.6	25.3	26	25.8	25.6
Holding Voltage By TLP (V)	7.06	10.2	11.4	12.8	7.6	10.4	10.8	11.9	11.9
Holding Voltage By 370 (V)	3	5.5	5.7	5.8	3.1	5.6	5.8	5.8	5.8
It2 (A)	0.2	0.667	1.45	2.52	0.182	0.676	1.6	1.65	1.63
HBM Level (kV)	0.5	2	2.5	3	0.5	1.5	2.5	2.5	2.5
MM Level (V)	50	200	250	300	50	250	250	250	400

(b)

W (μm)	400									
D_O Spacing (μm)	1									
P_P Spacing (μm)	1									
H_N Spacing (μm)	15					18				
N_C Spacing (μm)	1	2	3	4	5	1	2	3	4	5
Trigger Voltage (V)	25.6	26.9	27.1	25.8	25.9	26.3	26.3	26.1	26.1	25.6
Holding Voltage By TLP (V)	6.37	10.9	11.7	11.4	11.4	7.46	10.5	11.1	11.9	11.9
Holding Voltage By 370 (V)	2.9	5.5	5.6	5.66	5.7	3.2	5.4	5.7	5.65	5.8
It2 (A)	0.204	0.717	1.42	1.6	1.62	0.188	0.725	1.46	1.54	1.63
HBM Level (kV)	0.5	2	2.5	3	3.5	0.5	1.5	2.5	2.5	2.5
MM Level (V)	50	200	250	300	400	50	250	250	250	400

Table 3.5

Various ESD Characteristics of LD-PMOS in different device total width (W).

N_C Spacing (μm)	0.3		
D_O Spacing (μm)	1		
P_P Spacing (μm)	1		
H_N Spacing (μm)	6		
W (μm)	400	600	800
Trigger Voltage (V)	37.8	39	39.2
Holding Voltage By TLP (V)	37.4	38.6	38.8
Holding Voltage BY 370 (V)	38	38.3	38.4
It2 (A)	0.279	0.44	0.593
HBM Level (kV)	0.5	0.5	0.5
MM Level (V)	50	50	50

Table 3.6

Various ESD Characteristics of LD-PMOS in different HV PDDD spacing of drain side (H_P).

W (μm)	400			
P_C Spacing (μm)	0.3			
N_P Spacing (μm)	1			
H_P Spacing (μm)	6	9	12	15
Trigger Voltage (V)	38	37.7	37.7	37.9
Holding Voltage By TLP (V)	37.2	37.2	37	37.1
Holding Voltage BY 370 (V)	38.1	38.1	38.4	38.2
It2 (A)	0.349	0.347	0.316	0.29
HBM Level (KV)	0.5	0.5	0.5	0.5
MM Level (V)	50	50	50	50

Table 3.7

Various ESD Characteristics of LD-PMOS in different P+ edge to contact spacing of drain side (P_C).

W (μm)	400		
N_P Spacing (μm)	1		
H_P Spacing (μm)	6		
P_C Spacing (μm)	1	2	3
Trigger Voltage (V)	37.9	37.9	37.9
Holding Voltage By TLP (V)	37	37	37.1
Holding Voltage BY 370 (V)	38	38	38.1
It2 (A)	0.353	0.35	0.382
HBM Level (KV)	0.5	0.5	0.5
MM Level (V)	50	50	50

Table 3.8

Various ESD Characteristics of LD-PMOS in different N+ edge to polygate spacing of source side (N_P).

W (μm)	400			
P_C Spacing (μm)	0.3			
H_P Spacing (μm)	6			
N_P Spacing (μm)	1	2	3	4
Trigger Voltage (V)	39.6	38	37.9	37.9
Holding Voltage By TLP (V)	37.2	37	36.8	36.8
Holding Voltage BY 370 (V)	37.7	38.1	38	38
It2 (A)	0.349	0.347	0.36	0.356
HBM Level (KV)	0.5	0.5	0.5	0.5
MM Level (V)	50	50	50	50

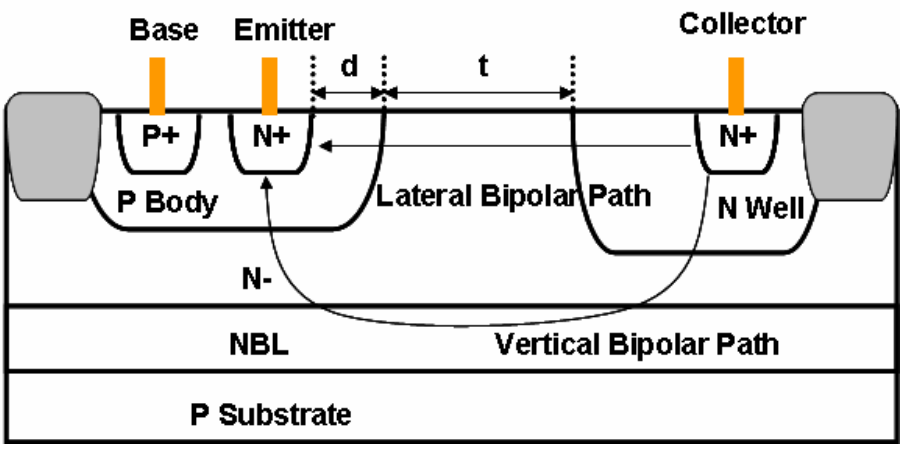
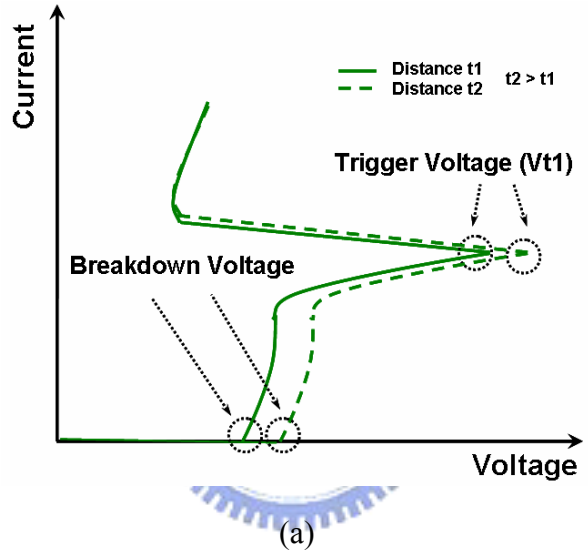
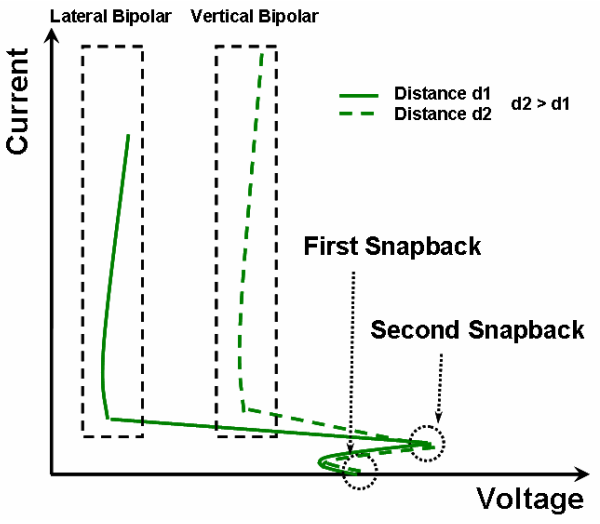


Fig. 3.1 The HV BJT structure with controllable trigger and holding voltage.

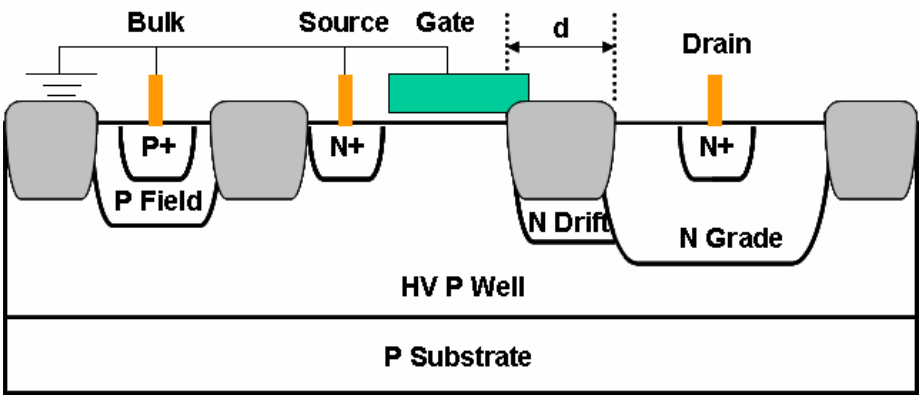


(a)

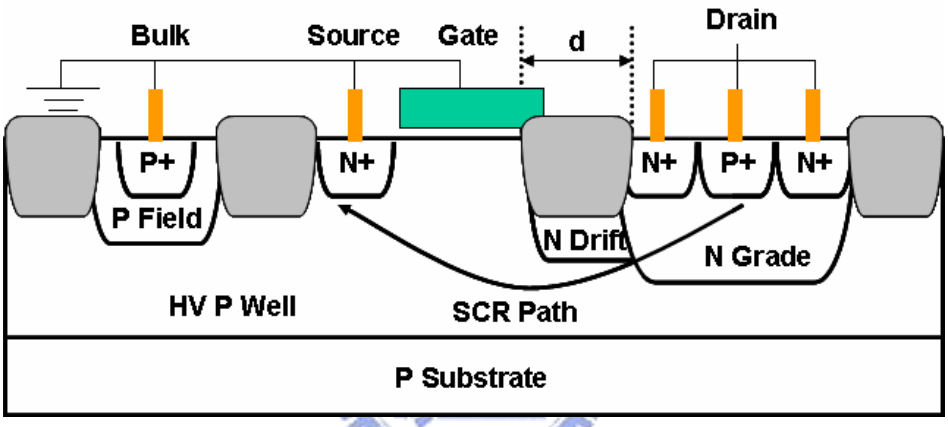


(b)

Fig. 3.2 The TLP I-V curves of HV BJT structure with different (a) "t" spacing, (b) "d" spacing.



(a)



(b)

Fig. 3.3 The cross-sectional views of (a) HV NMOS with N-drift implant and (b) HV NSCR with N-drift implant.

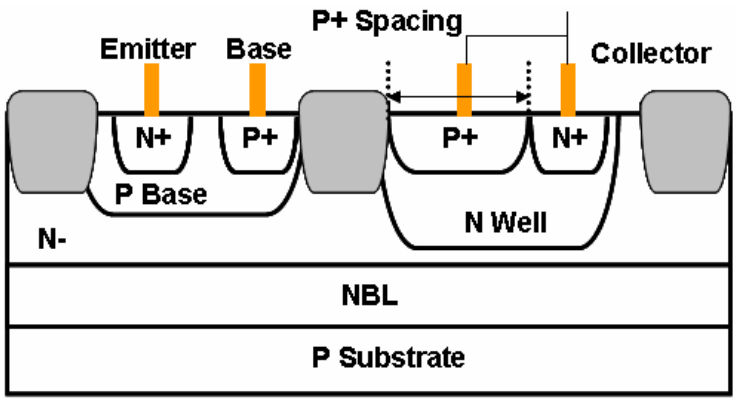


Fig. 3.4 The cross-sectional view of bipolar-triggered SCR (B-SCR).

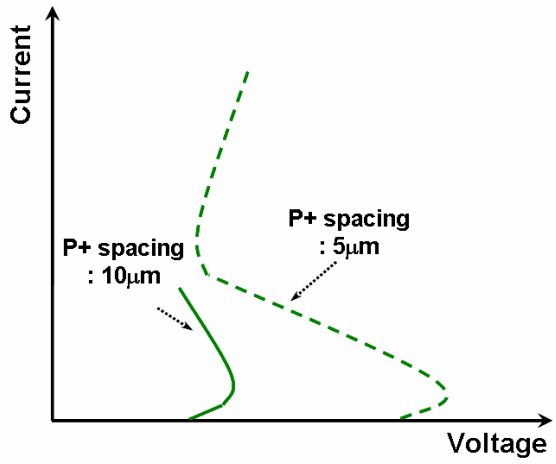
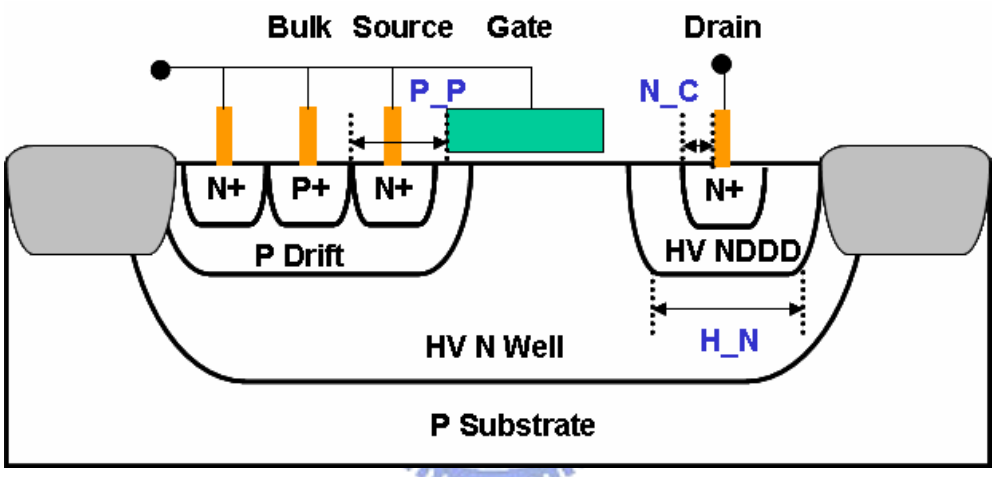
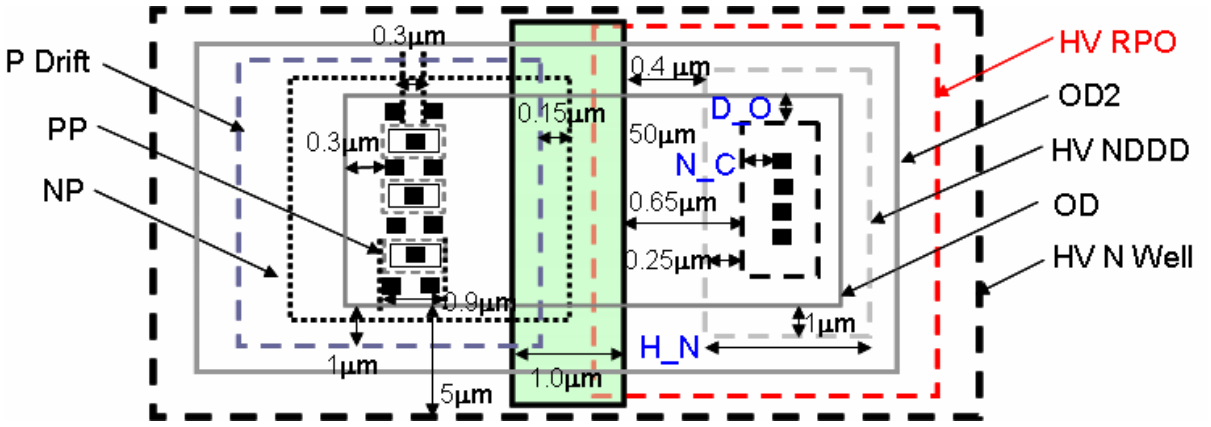


Fig. 3.5 The TLP I-V curves of bipolar-triggered SCR (B-SCR) with different P+ spacing.

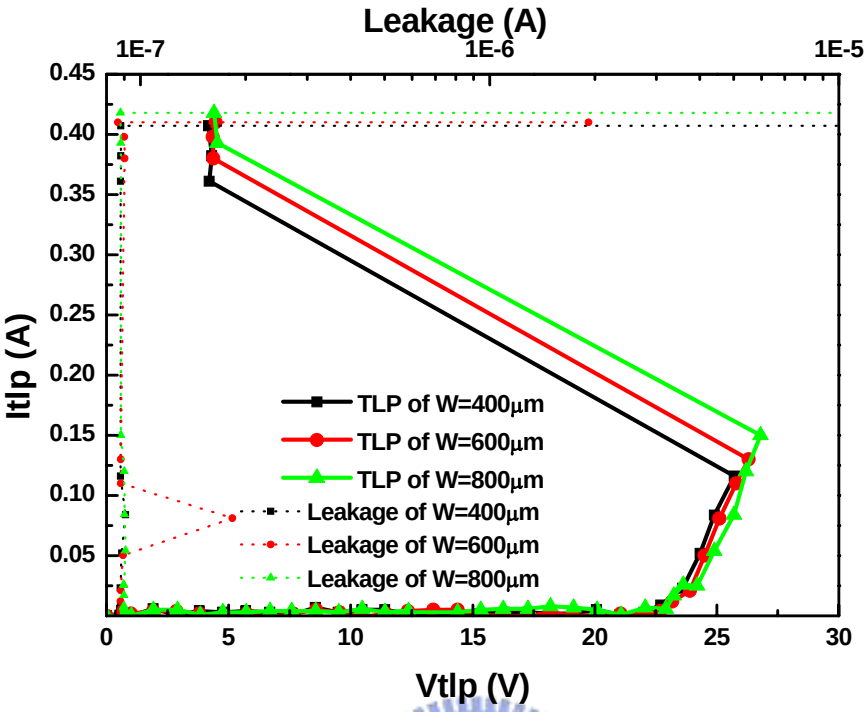


(a)

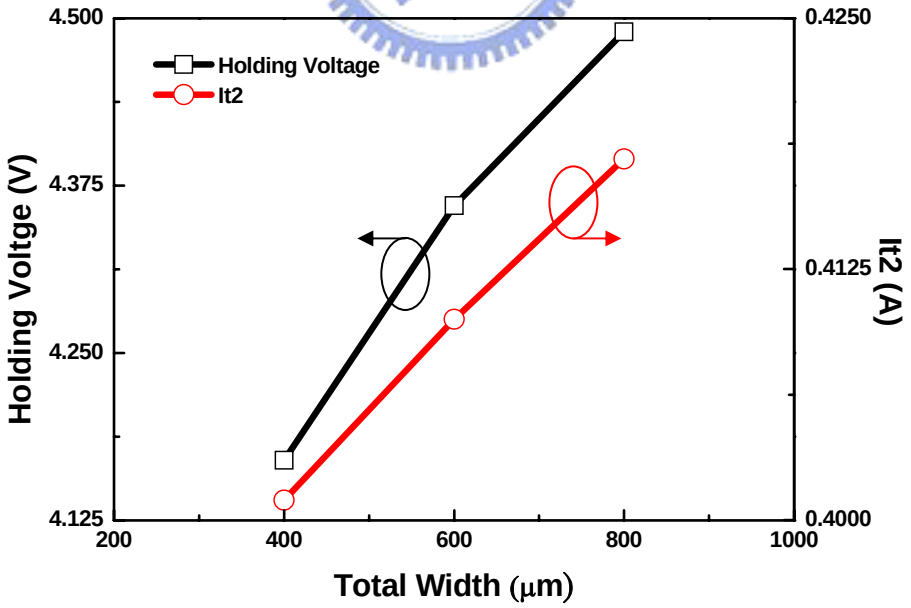


(b)

Fig. 3.6 (a) The cross-sectional view of LD-NMOS and the modified parameters, (b) The layout view of LD-NMOS and the modified parameters.

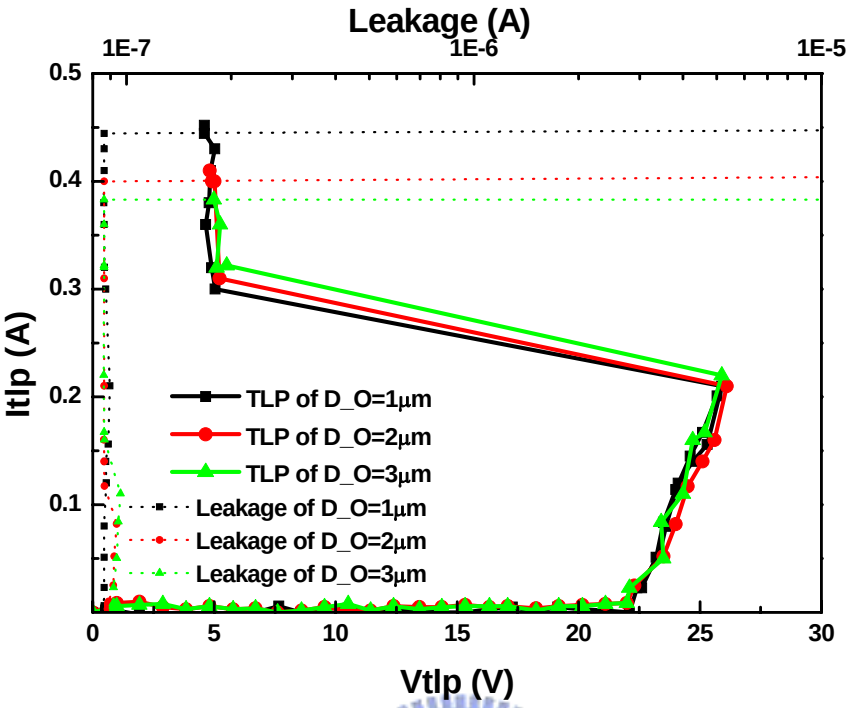


(a)

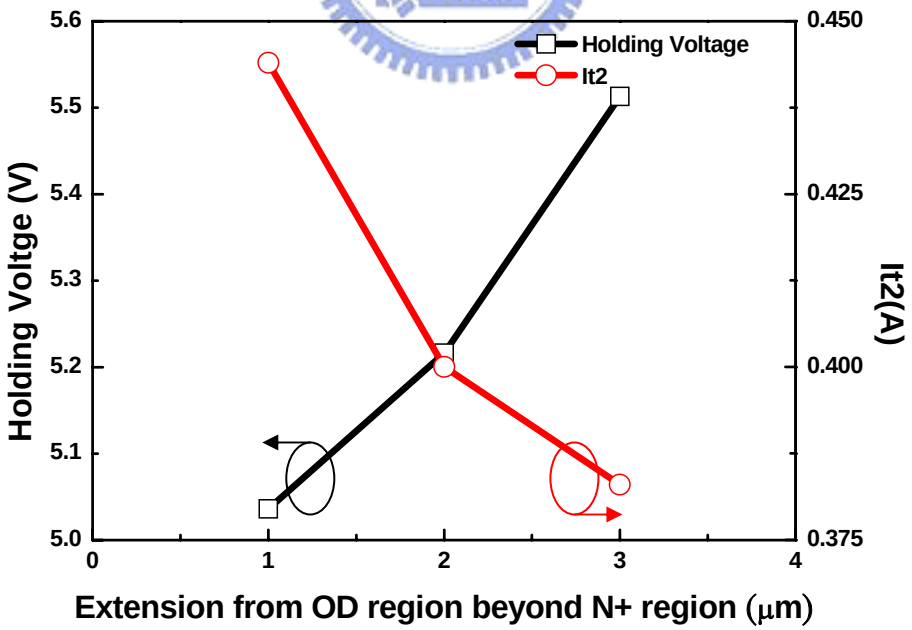


(b)

Fig. 3.7 (a) The TLP I-V curves of LD-NMOS with different total width, (b) The diagram of the holding voltage and It2 value versus the total width.

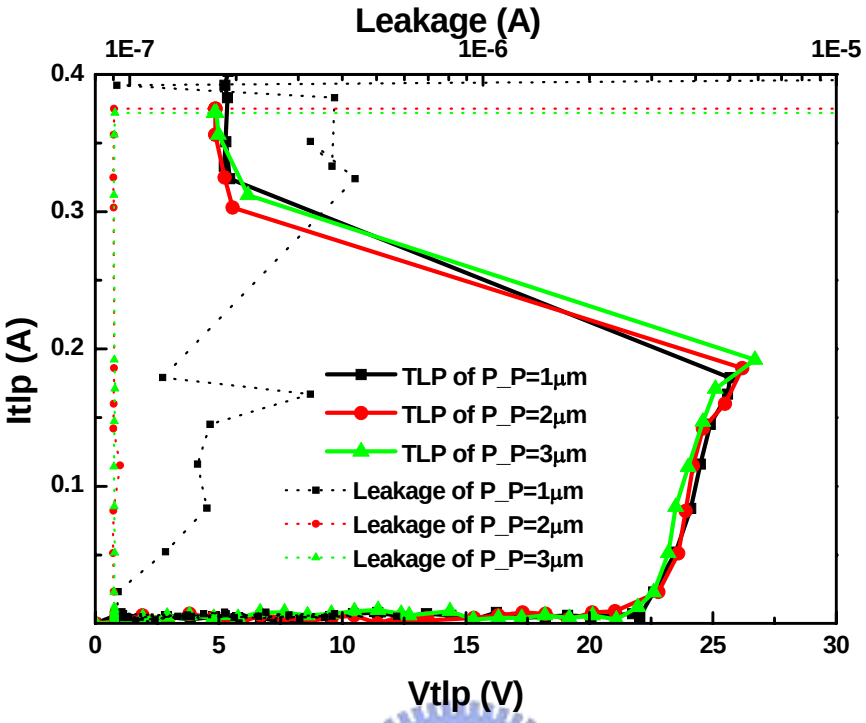


(a)

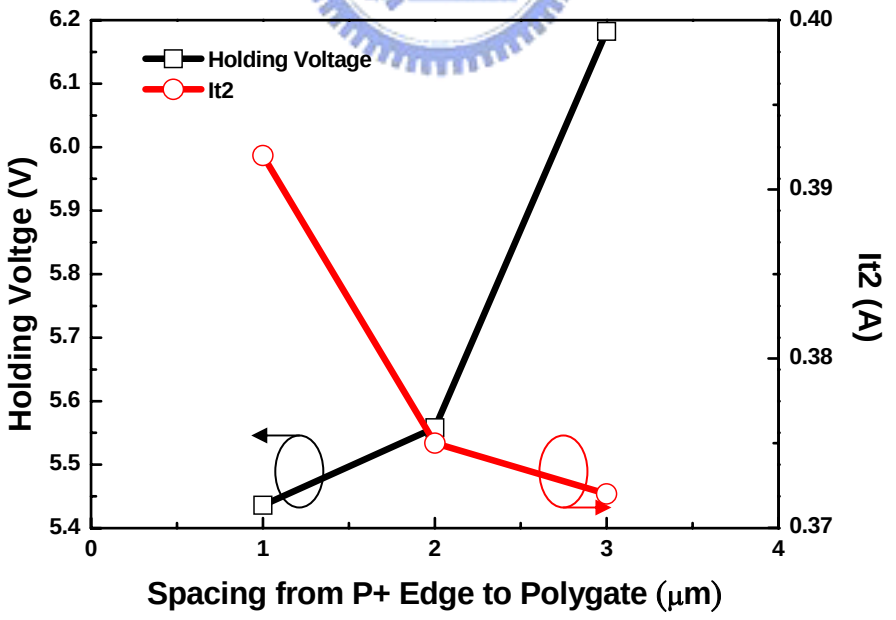


(b)

Fig. 3.8 (a) The TLP I-V curves of LD-NMOS with different D_O spacing, (b) The diagram of the holding voltage and It2 value versus the D_O spacing.

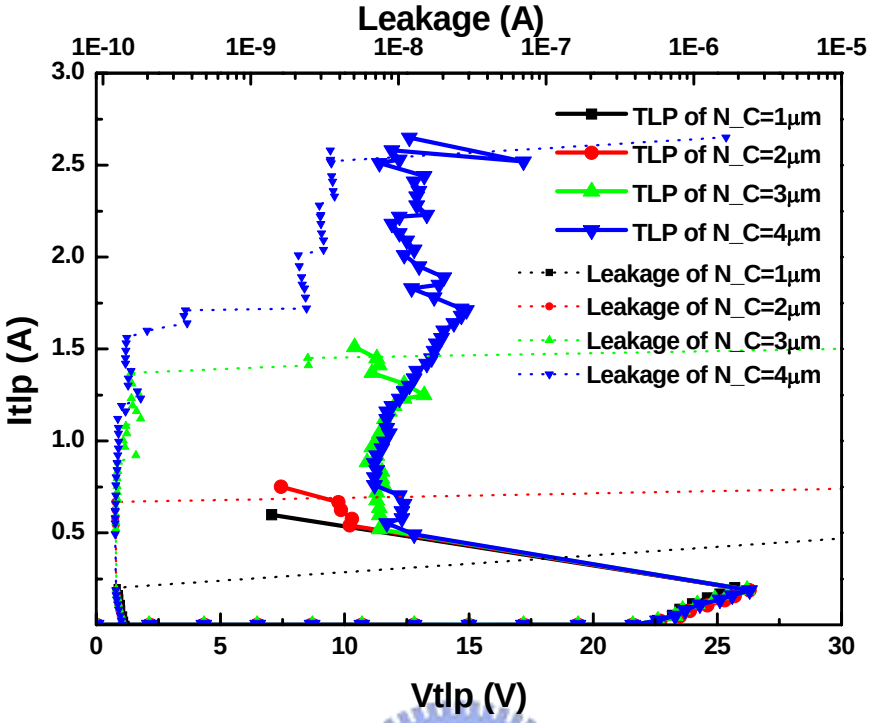


(a)

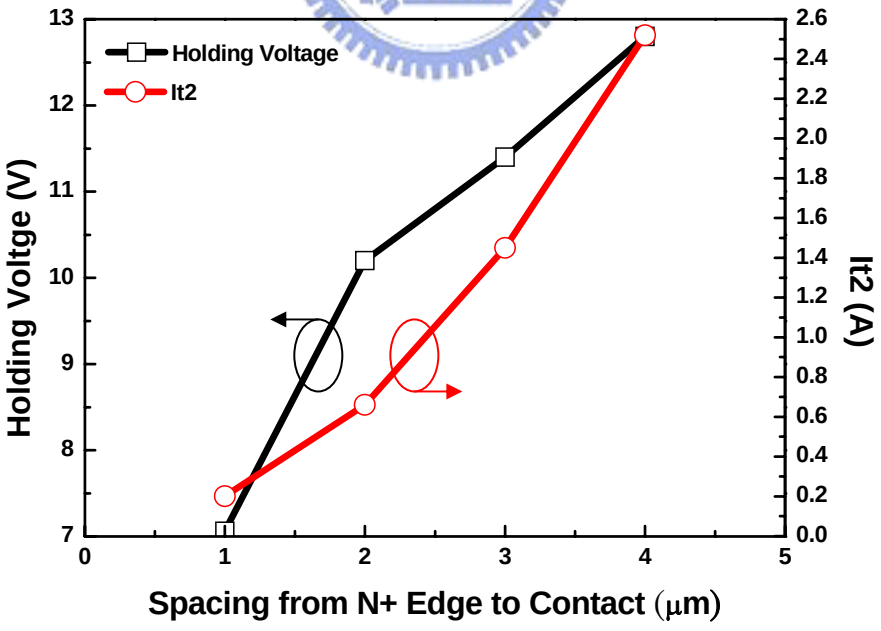


(b)

Fig. 3.9 (a) The TLP I-V curves of LD-NMOS with different P_P spacing, (b) The diagram of the holding voltage and It2 value versus the P_P spacing.

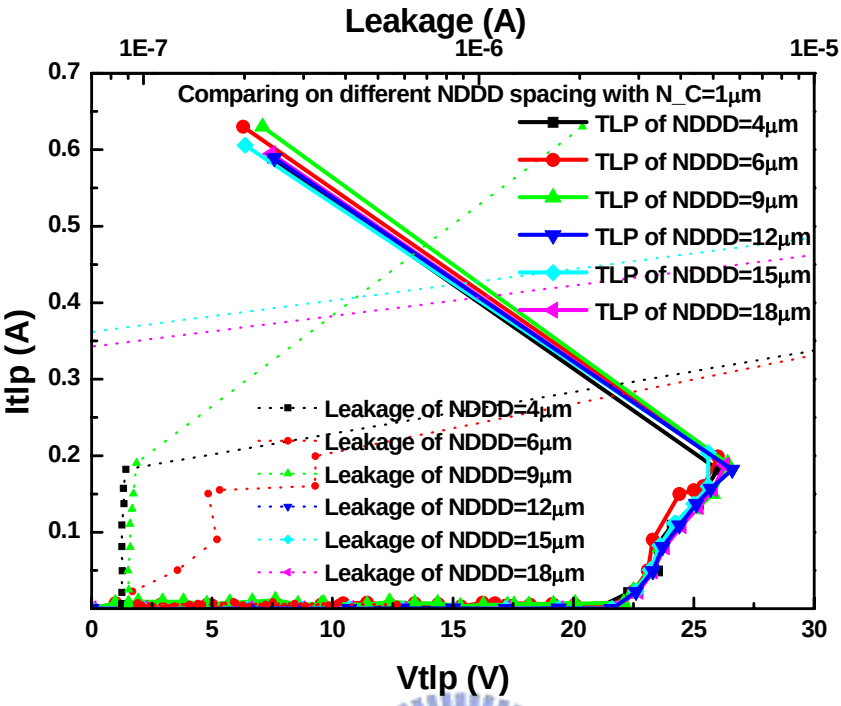


(a)

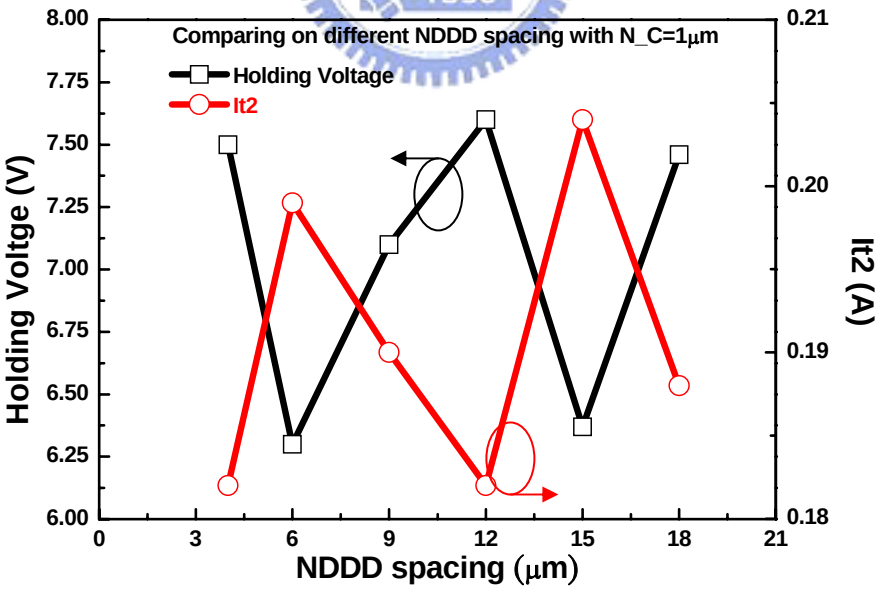


(b)

Fig. 3.10 (a) The TLP I-V curves of LD-NMOS with different N_C spacing, (b) The diagram of the holding voltage and It2 value versus the N_C spacing.

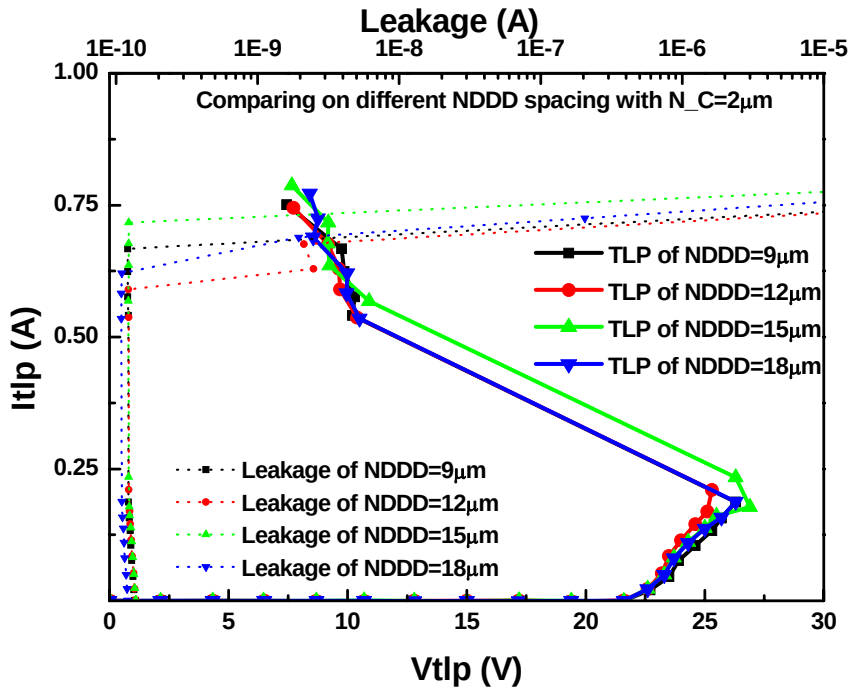


(a)

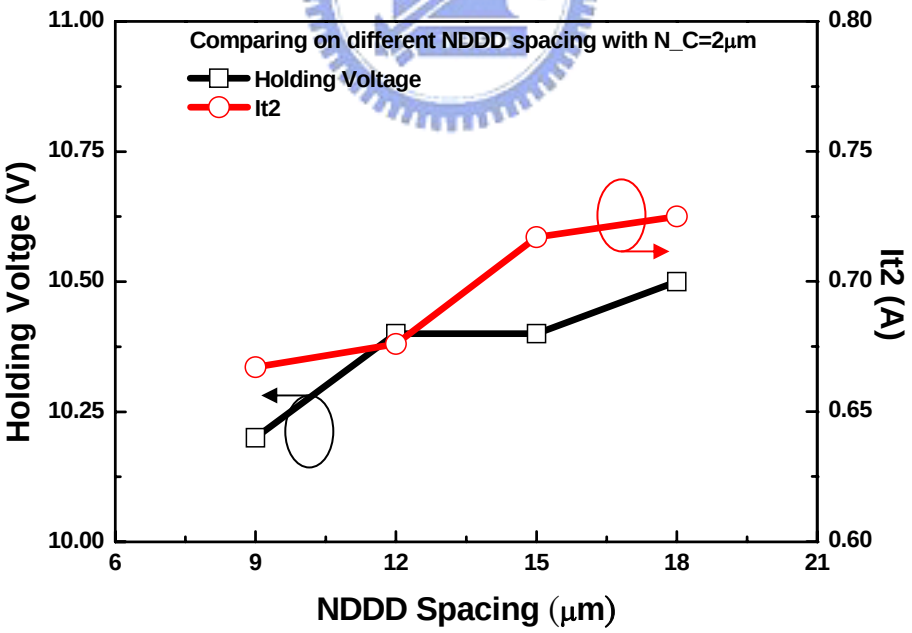


(b)

Fig. 3.11 (a) The TLP I-V curves of LD-NMOS with different H_N spacing on N_C = 1μm, (b) The diagram of the holding voltage and It2 value versus the H_N spacing.

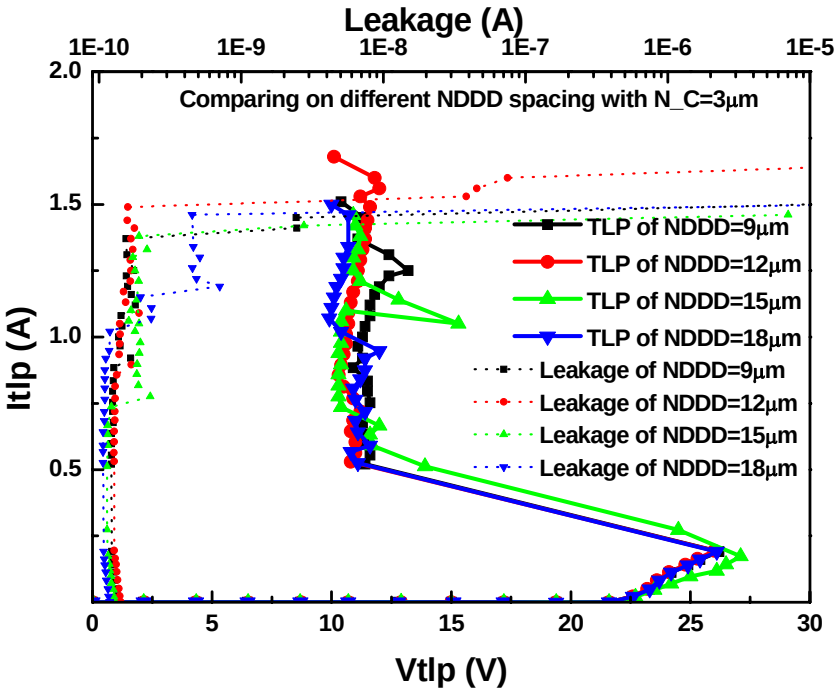


(a)

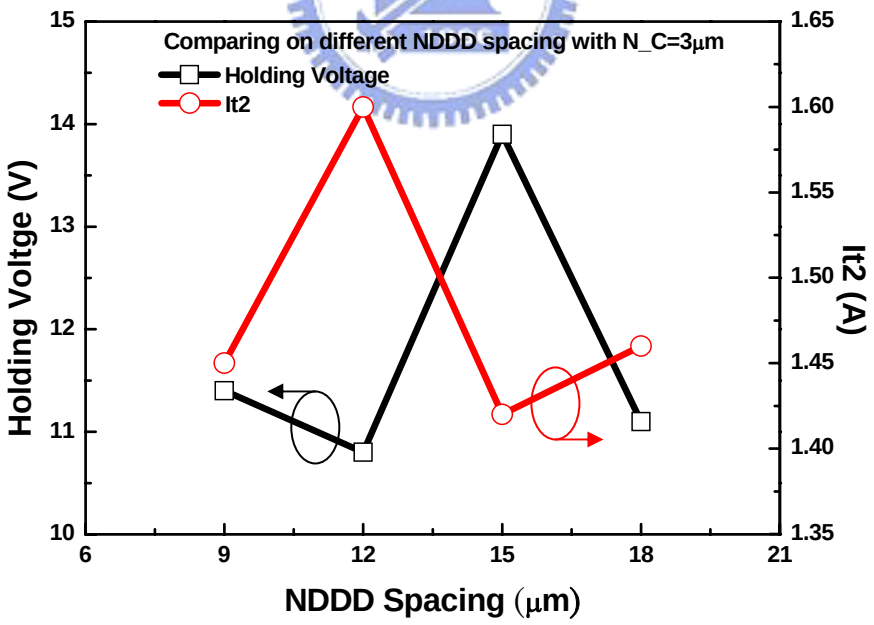


(b)

Fig. 3.12 (a) The TLP I-V curves of LD-NMOS with different H_N spacing on N_C = 2μm, (b) The diagram of the holding voltage and It2 value versus the H_N spacing.

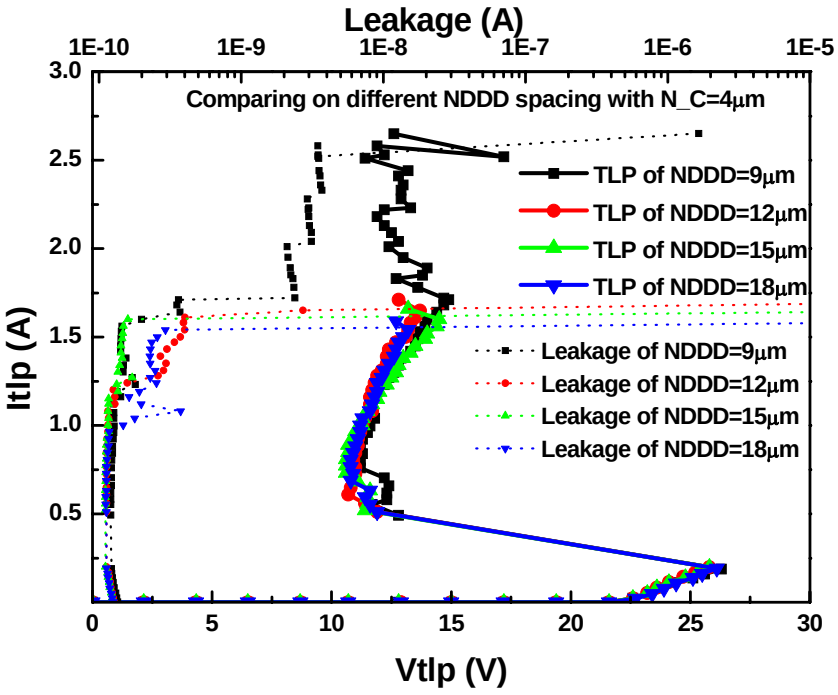


(a)

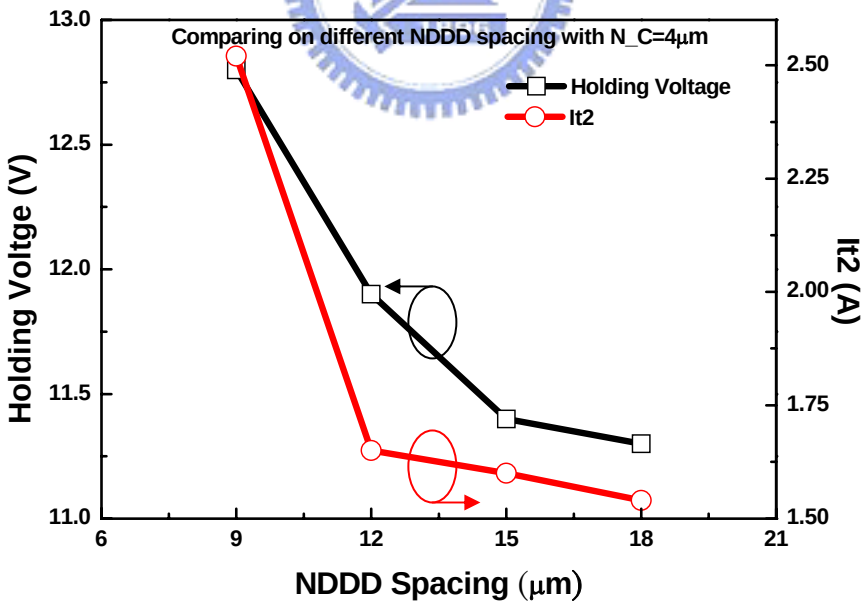


(b)

Fig. 3.13 (a) The TLP I-V curves of LD-NMOS with different H_N spacing on N_C = 3μm, (b) The diagram of the holding voltage and It2 value versus the H_N spacing.



(a)



(b)

Fig. 3.14 (a) The TLP I-V curves of LD-NMOS with different H_N spacing on N_C = 4μm, (b) The diagram of the holding voltage and It2 value versus the H_N spacing.

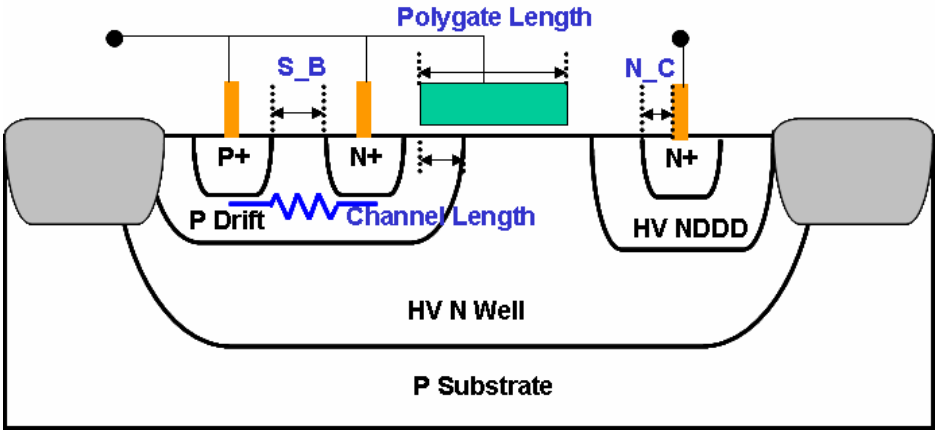
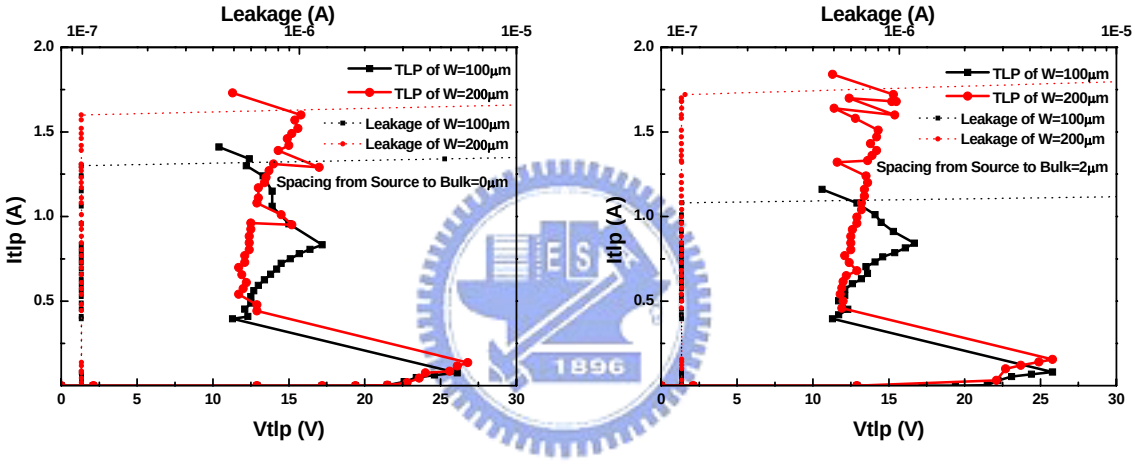
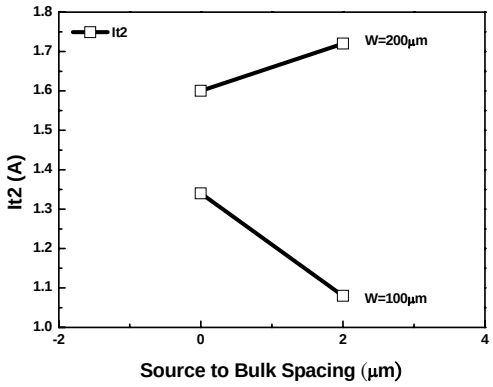


Fig. 3.15 The cross-sectional view of the LD-NMOS with separation source and bulk regions.



(a) (b)



(c)

Fig. 3.16 LD-NMOS : (a) The TLP I-V curves of different total width with S_B spacing=0μm, (b) The TLP I-V curves of different total width with S_B spacing=2μm, (c) The It2 value versus S_B spacing on different total width.

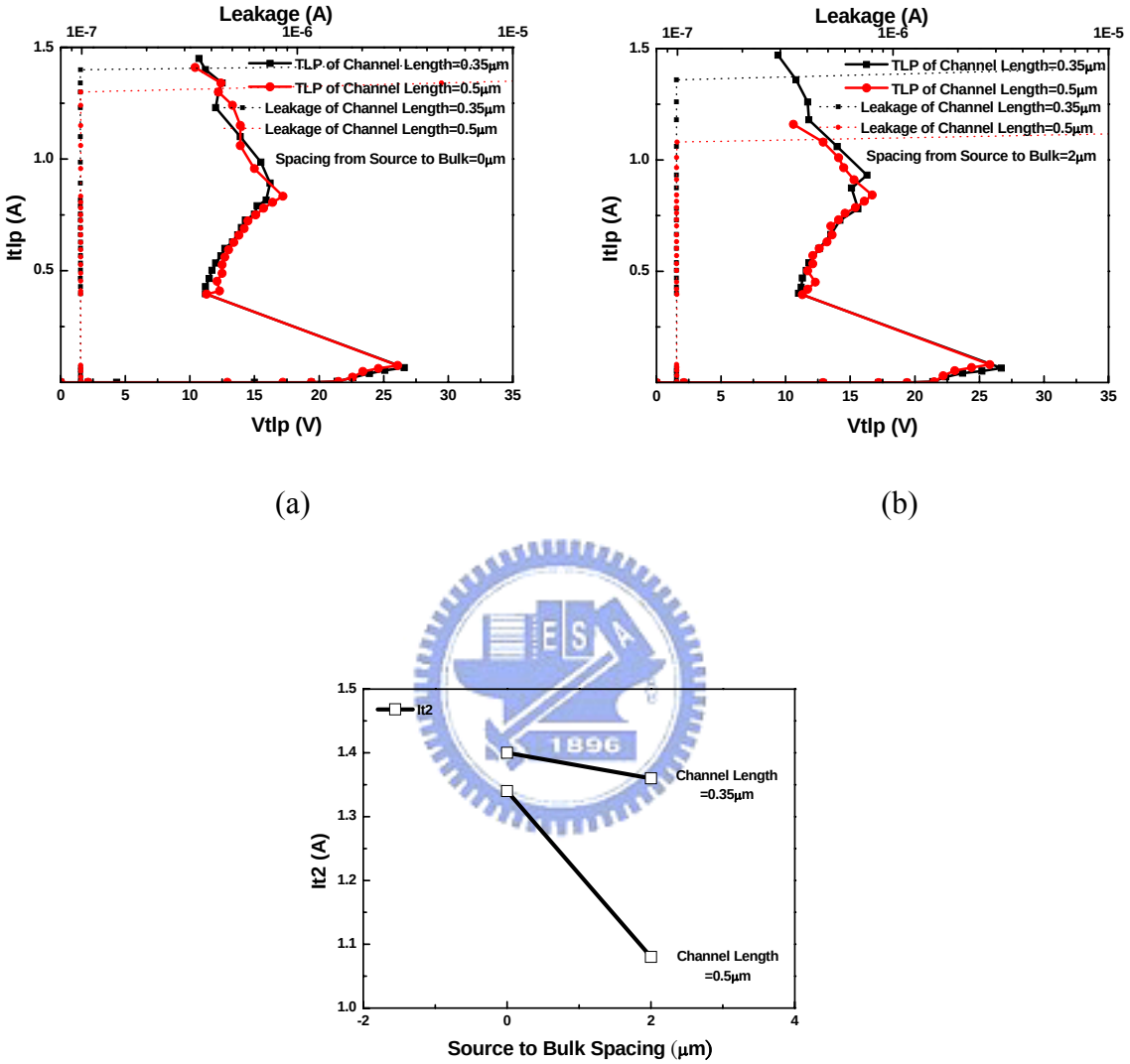


Fig. 3.17 LD-NMOS : (a) The TLP I-V curves of different channel length with S_B spacing=0μm, (b) The TLP I-V curves of different channel length with S_B spacing=2μm, (c) The It2 value versus S_B spacing on different channel length.

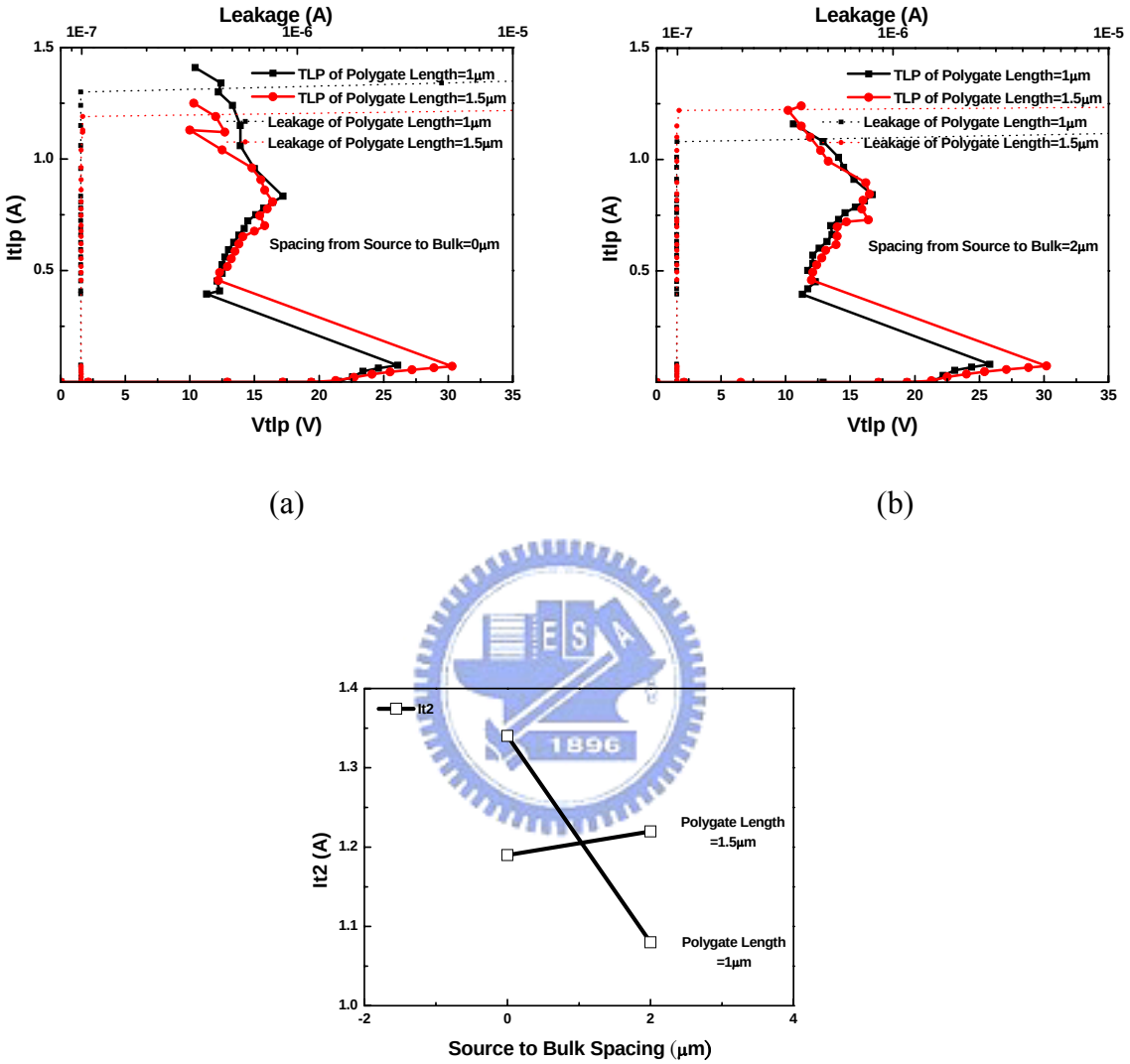
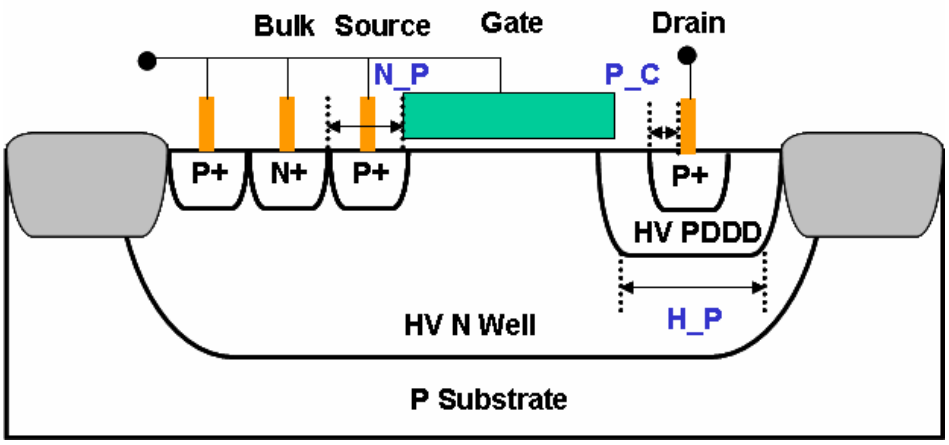
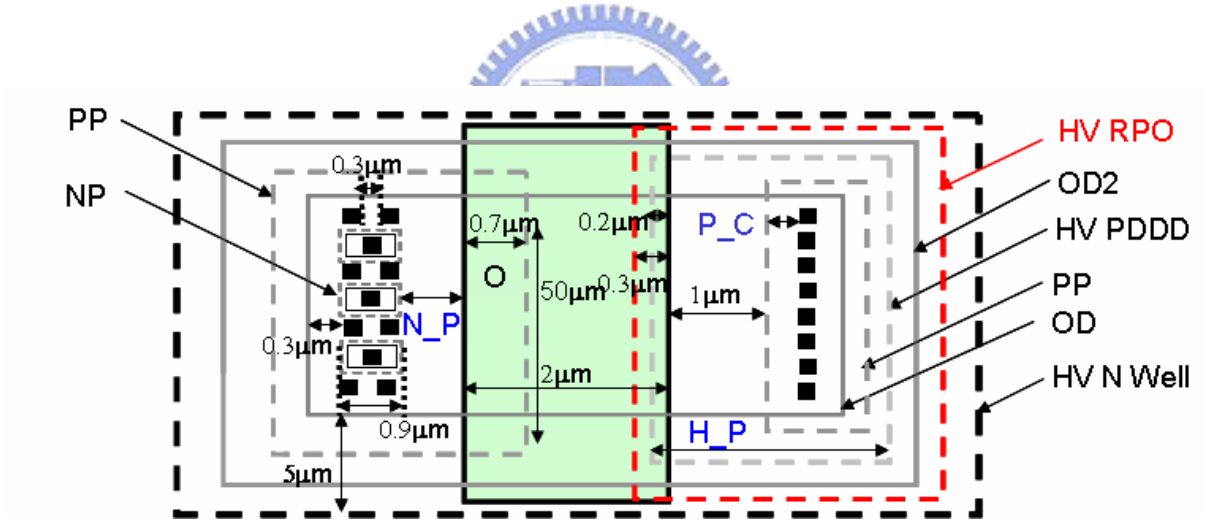


Fig. 3.18 LD-NMOS : (a) The TLP I-V curves of different polygate length with S_B spacing=0μm, (b) The TLP I-V curves of different polygate length with S_B spacing=2μm, (c) The It2 value versus S_B spacing on different polygate length.

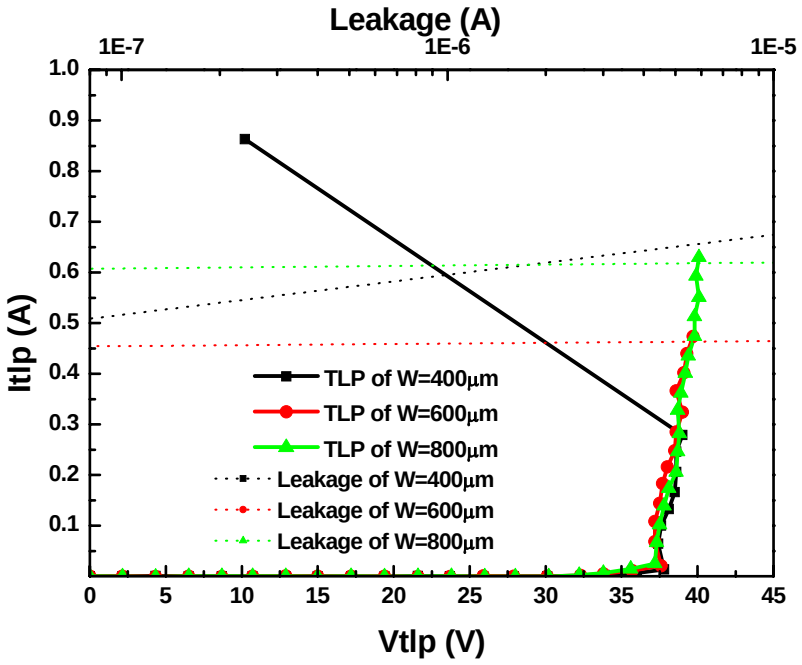


(a)

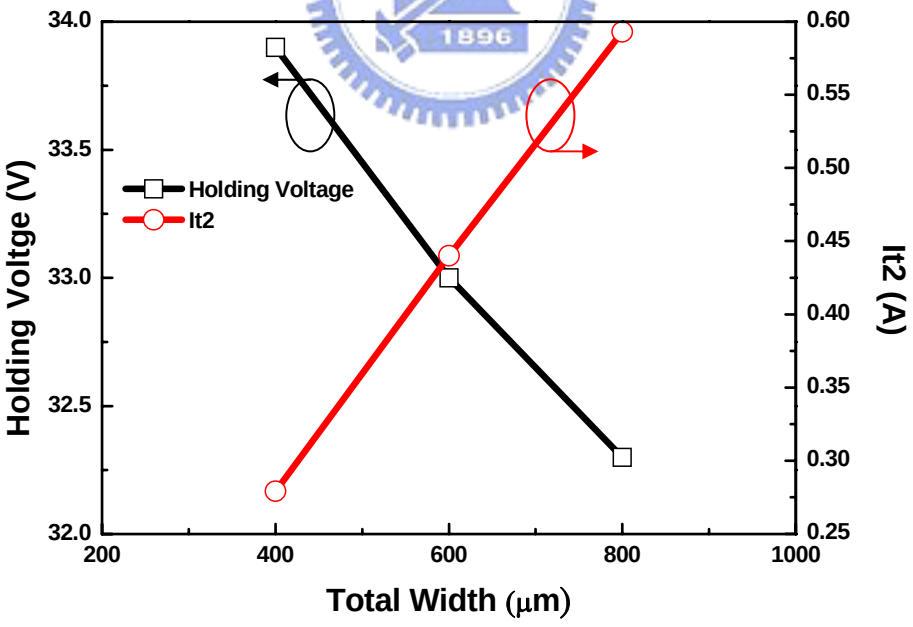


(b)

Fig. 3.19 (a) The cross-sectional view of LD-PMOS and the modified parameters, (b) The layout view of LD-PMOS and the modified parameters.

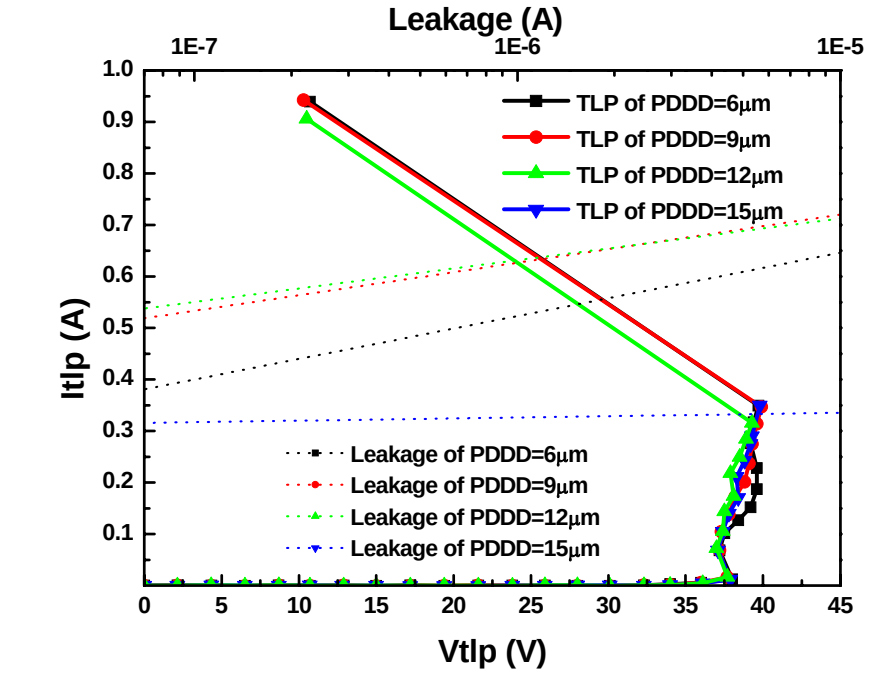


(a)

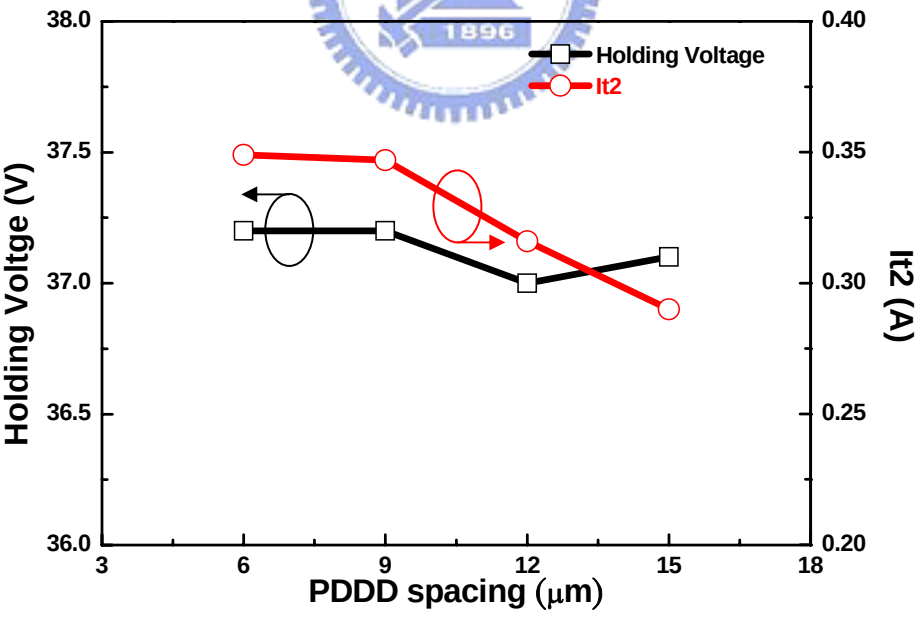


(b)

Fig. 3.20 (a) The TLP I-V curves of LD-PMOS with different total width, (b) The diagram of the holding voltage and It2 value versus the total width.

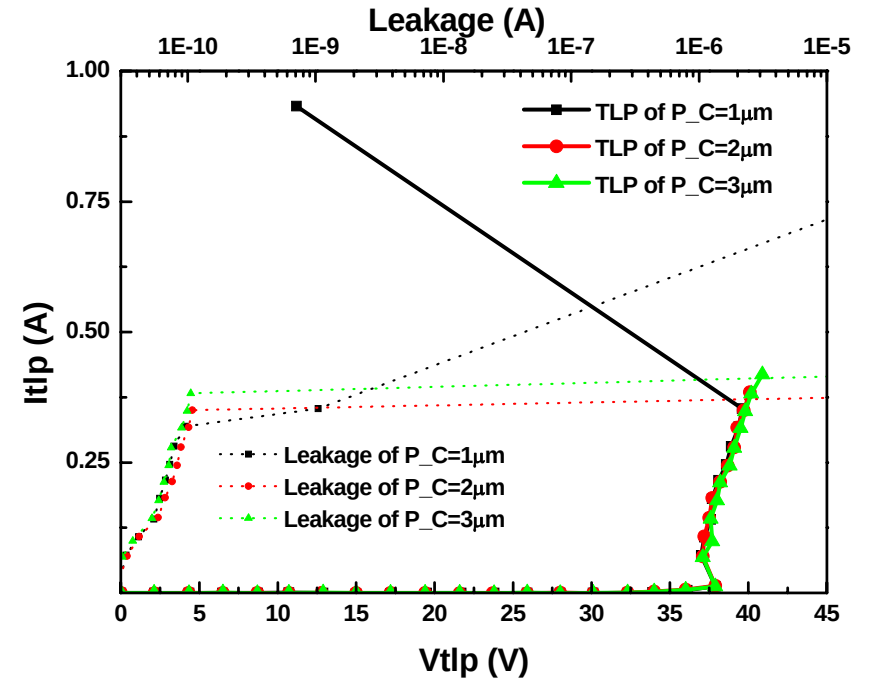


(a)

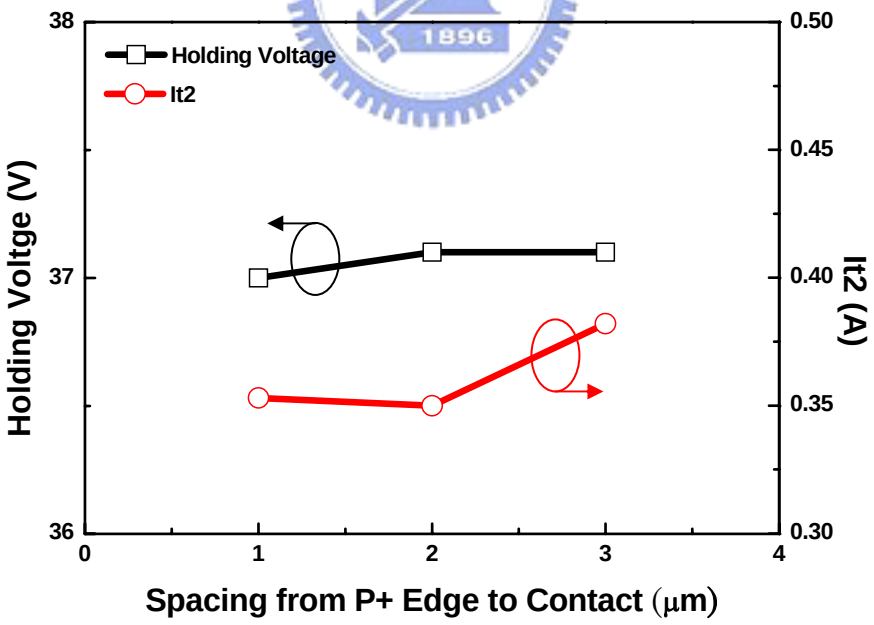


(b)

Fig. 3.21 (a) The TLP I-V curves of LD-PMOS with different H_P spacing, (b) The diagram of the holding voltage and It2 value versus the H_P spacing.

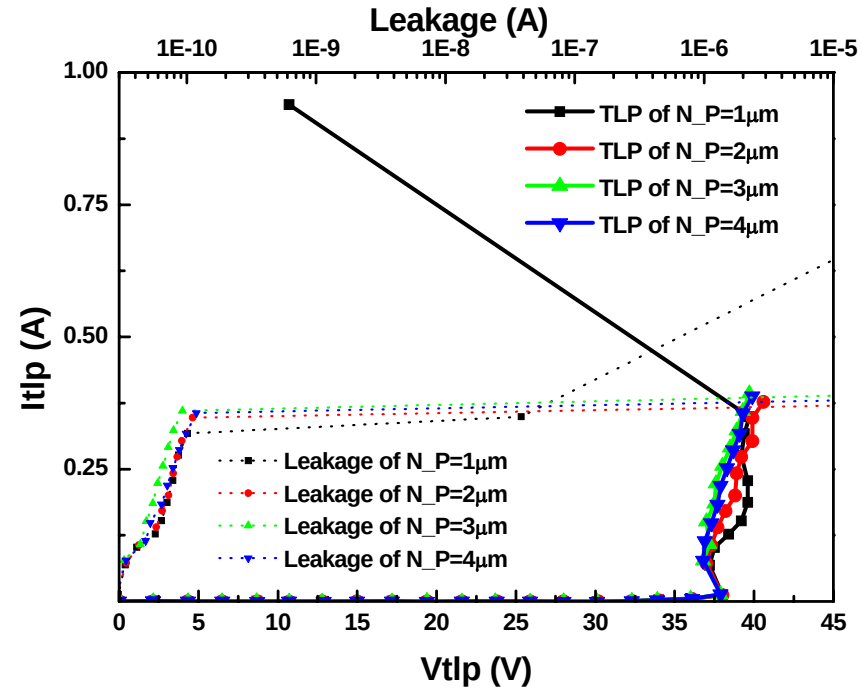


(a)

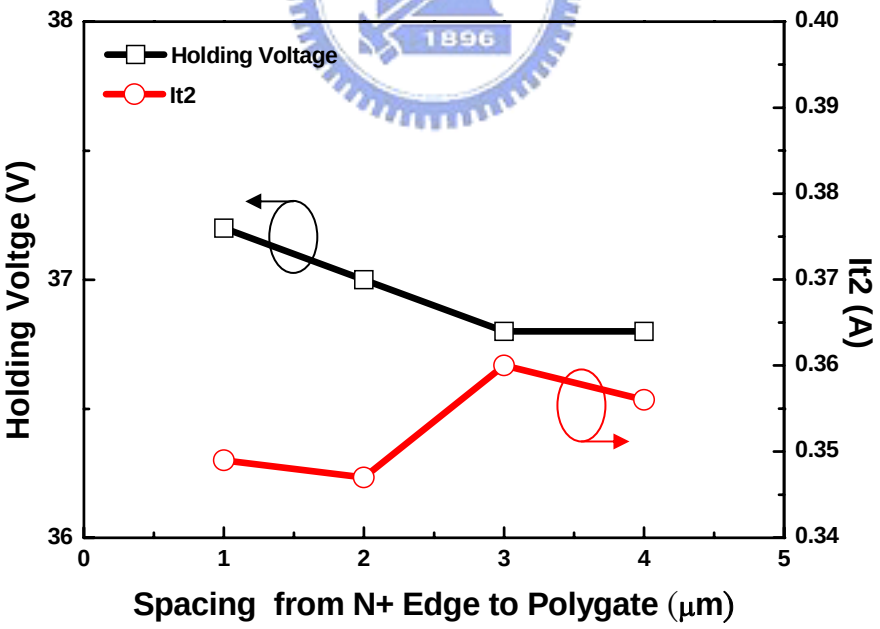


(b)

Fig. 3.22 (a) The TLP I-V curves of LD-PMOS with different P_C spacing, (b) The diagram of the holding voltage and It2 value versus the P_C spacing.



(a)



(b)

Fig. 3.23 (a) The TLP I-V curves of LD-PMOS with different N_P spacing, (b) The diagram of the holding voltage and It2 value versus the N_P spacing.

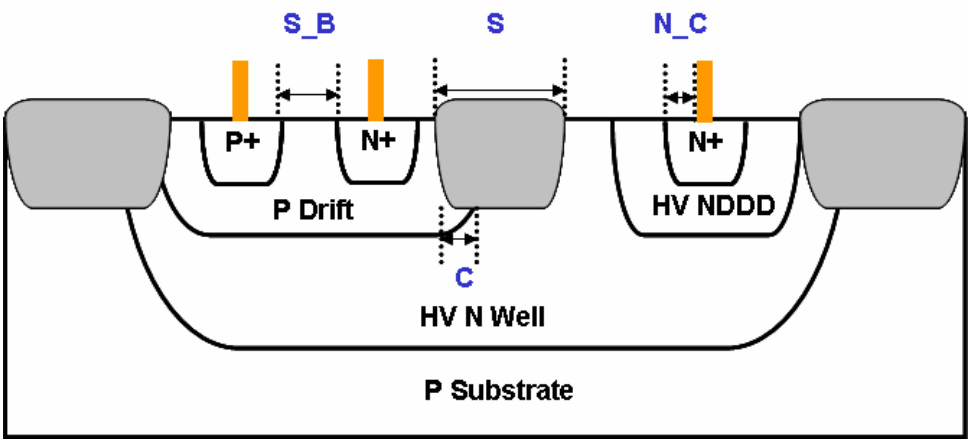


Fig. 3.24 The cross-sectional view of NFOD and the modified parameters.

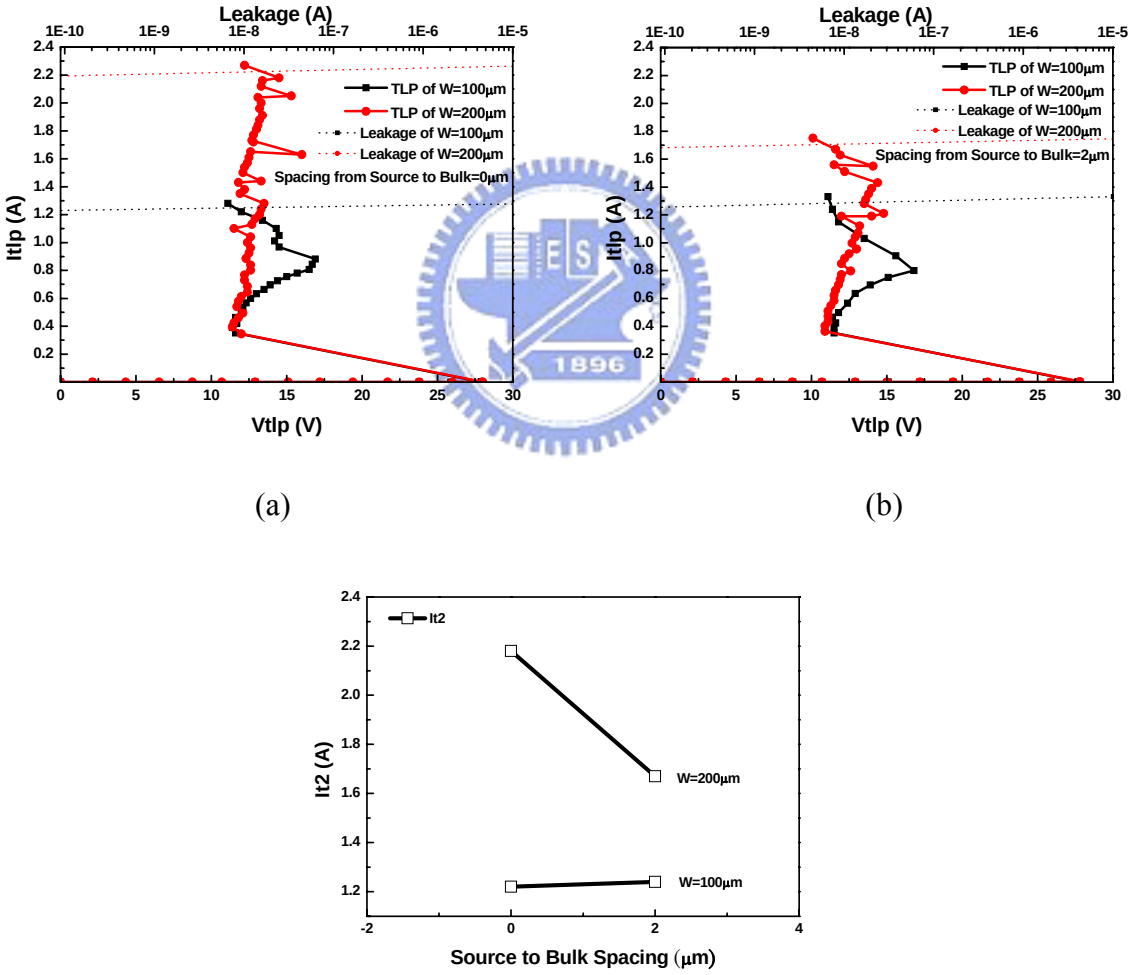
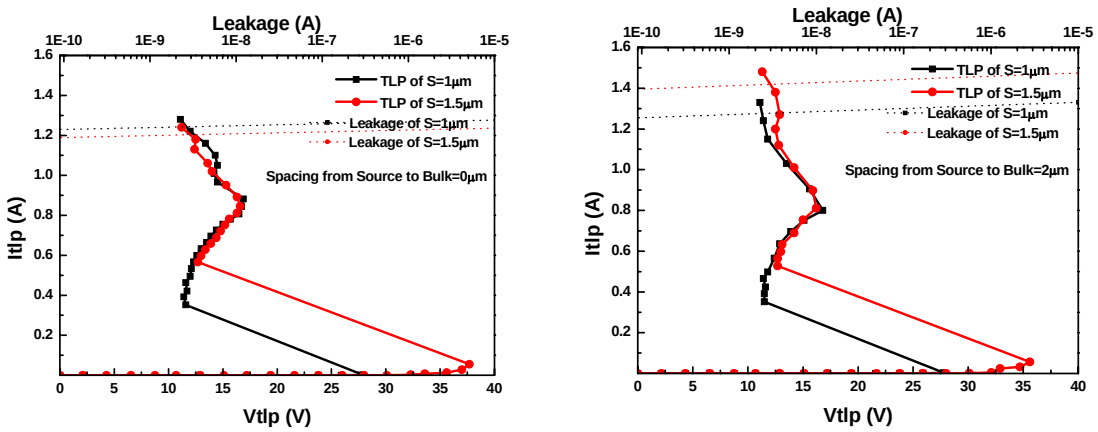
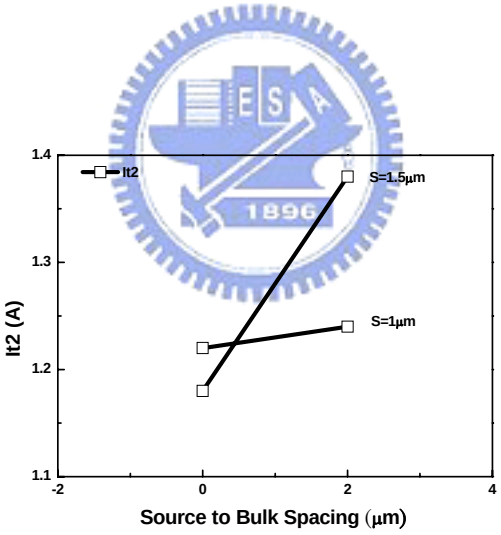


Fig. 3.25 NFOD : (a) The TLP I-V curves of different total width with S_B spacing=0μm, (b) The TLP I-V curves of different total width with S_B spacing=2μm, (c) The It2 value versus S_B spacing on different total width.



(a) (b)



(c)

Fig. 3.26 NFOD : (a) The TLP I-V curves of different S spacing with S_B spacing=0μm, (b) The TLP I-V curves of different S spacing with S_B spacing=2μm, (c) The It2 value versus S_B spacing on different S spacing.

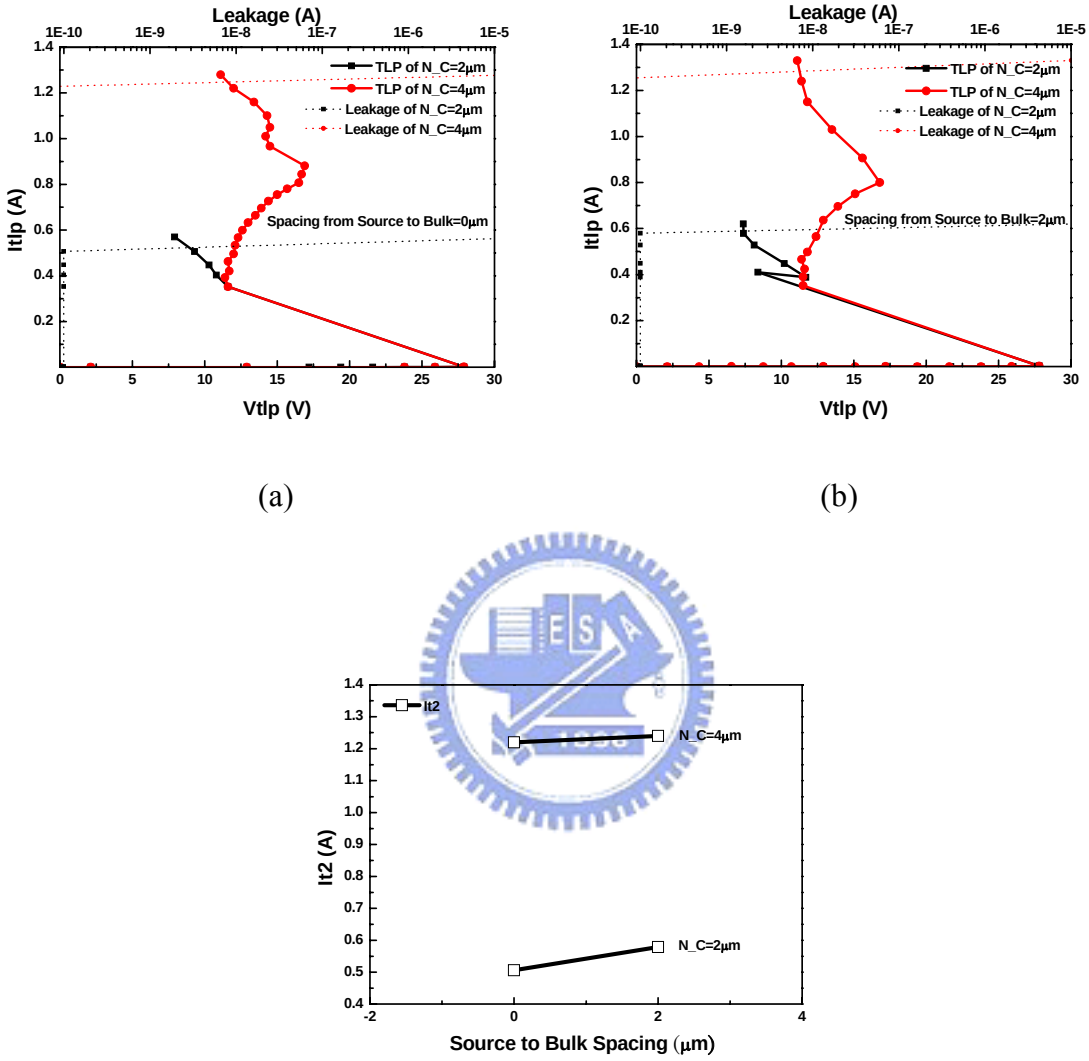


Fig. 3.27 NFOD : (a) The TLP I-V curves of different N_C spacing with S_B spacing=0μm, (b) The TLP I-V curves of different N_C spacing with S_B spacing=2μm, (c) The It2 value versus S_B spacing on different N_C spacing.

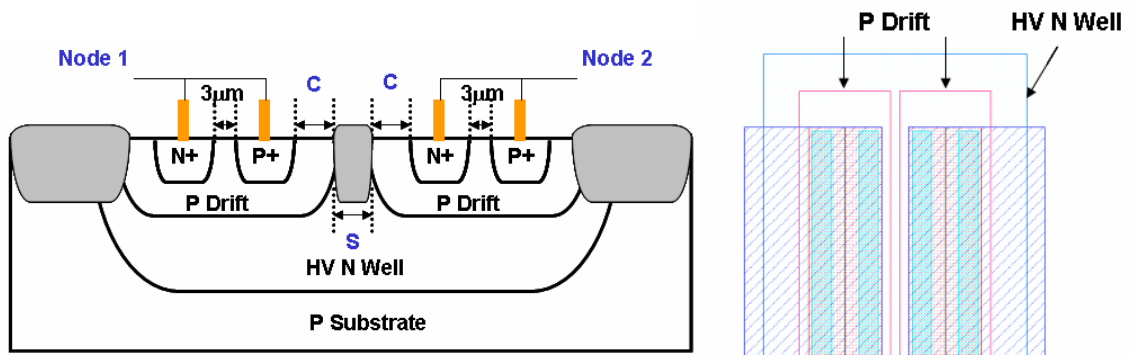


Fig. 3.28 (a) The cross-sectional view of dual-direction SCR type I and the modified parameters, (b) The layout diagram of dual-direction SCR type I.

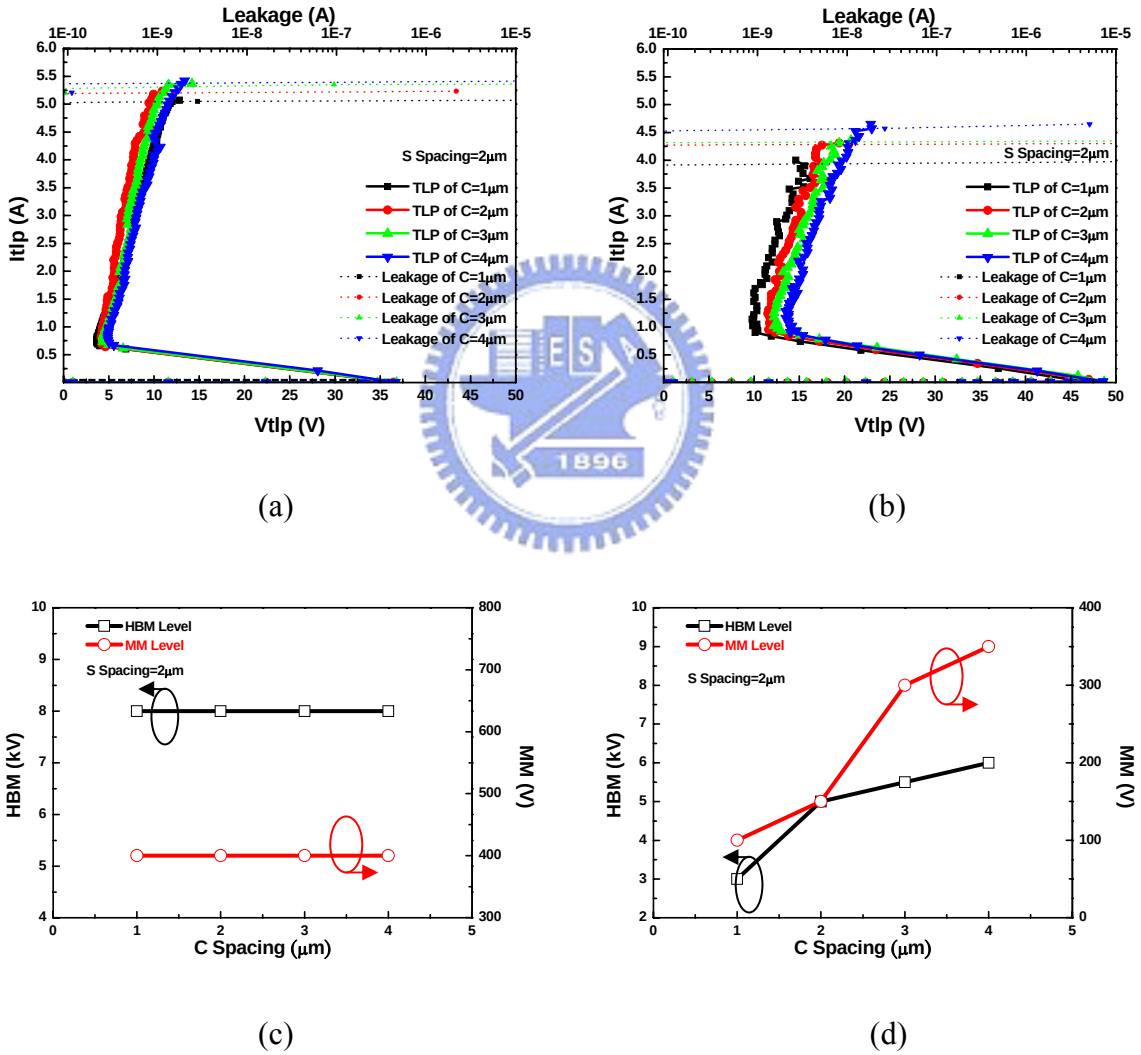


Fig. 3.29 The S spacing is fixed at 2μm of dual-direction SCR type I : (a) The TLP I-V curves of different C spacing with ESD zap at node 1, (b) The TLP I-V curves of different C spacing with ESD zap at node 2, (c) The HBM and MM levels versus C spacing with ESD zap at node 1, (d) The HBM and MM levels versus C spacing with ESD zap at node 2.

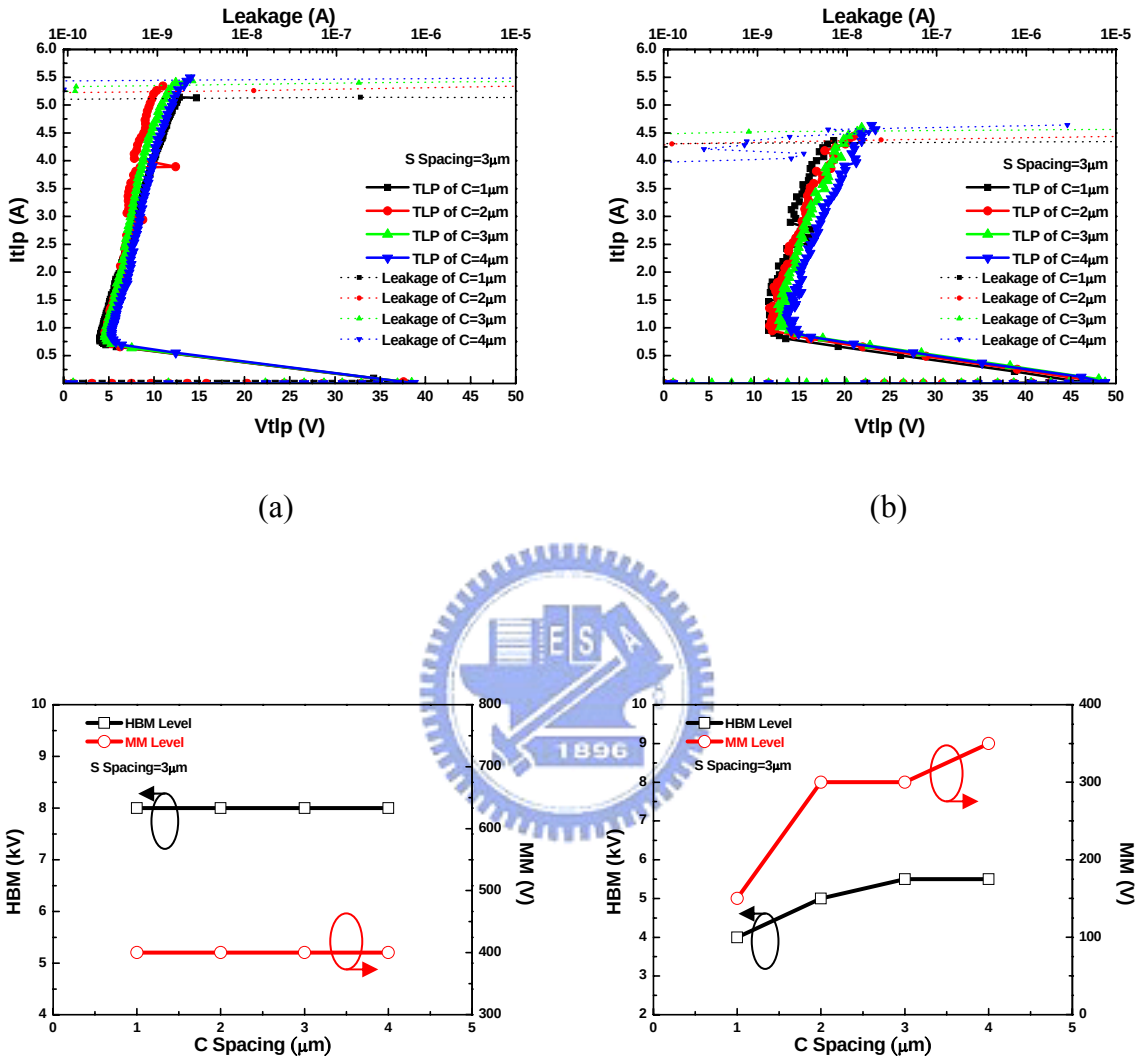


Fig. 3.30 The S spacing is fixed at 3μm of dual-direction SCR type I : (a) The TLP I-V curves of different C spacing with ESD zap at node 1, (b) The TLP I-V curves of different C spacing with ESD zap at node 2, (c) The HBM and MM levels versus C spacing with ESD zap at node 1, (d) The HBM and MM levels versus C spacing with ESD zap at node 2.

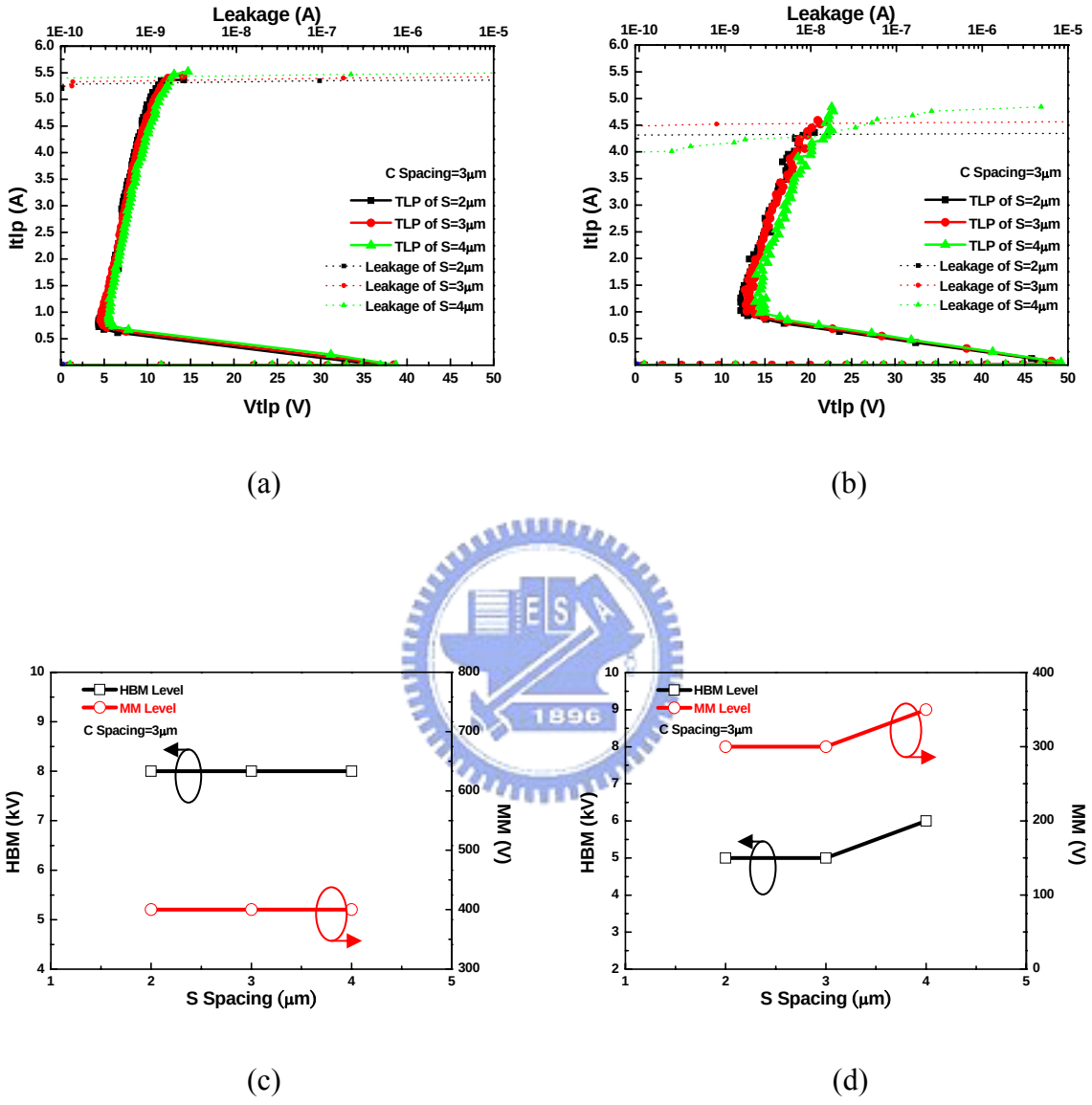


Fig. 3.31 The C spacing is fixed at 3μm of dual-direction SCR type I (a) The TLP I-V curves of different S spacing with ESD zap at node 1, (b) The TLP I-V curves of different S spacing with ESD zap at node 2, (c) The HBM and MM levels versus S spacing with ESD zap at node 1, (d) The HBM and MM levels versus S spacing with ESD zap at node 2.

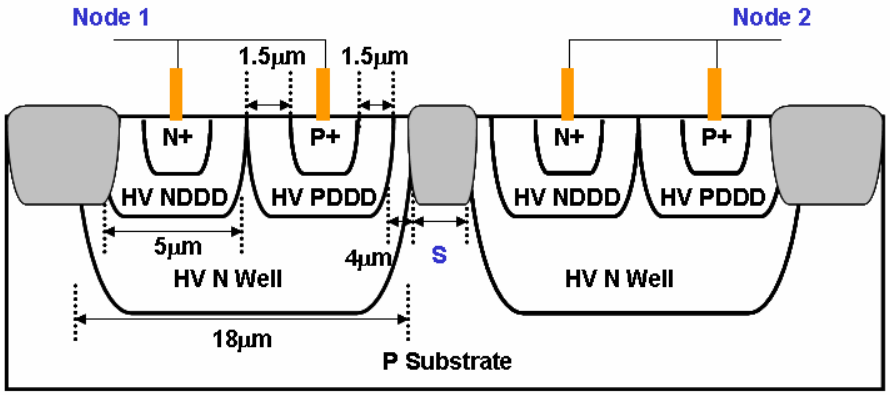
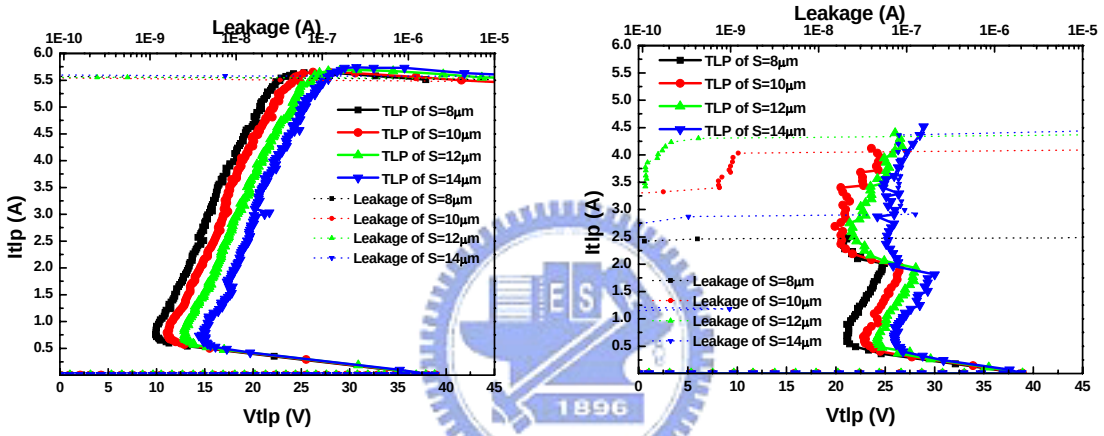
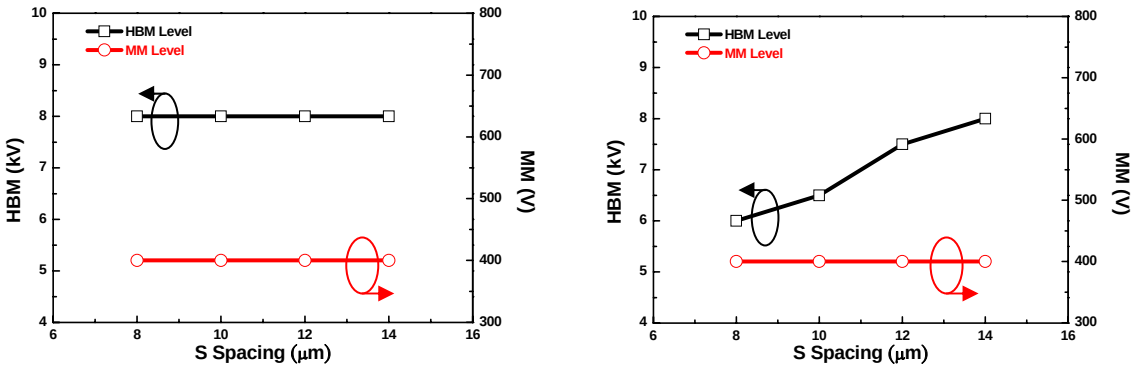


Fig. 3.32 The cross-sectional view of dual-direction SCR type II and the modified parameter.



(a) (b)



(c) (d)

Fig. 3.33 Dual-direction SCR type II : (a) The TLP I-V curves of different S spacing with ESD zap at node 1, (b) The TLP I-V curves of different S spacing with ESD zap at node 2, (c) The HBM and MM levels versus S spacing with ESD zap at node 1, (d) The HBM and MM levels versus S spacing with ESD zap at node 2.

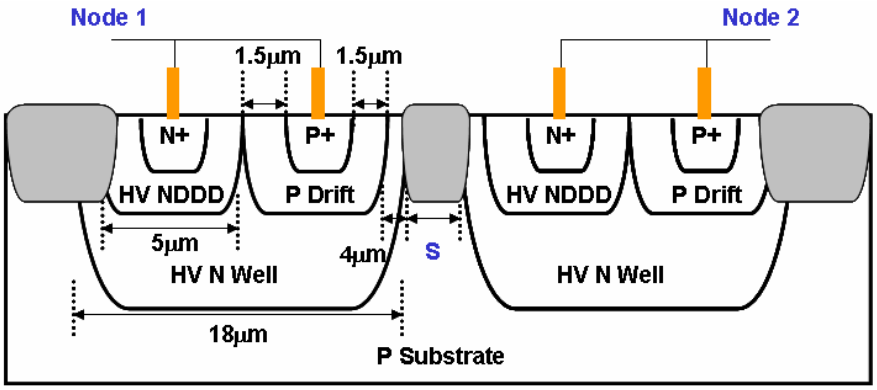


Fig. 3.34 The cross-sectional view of dual-direction SCR type III and the modified parameter.

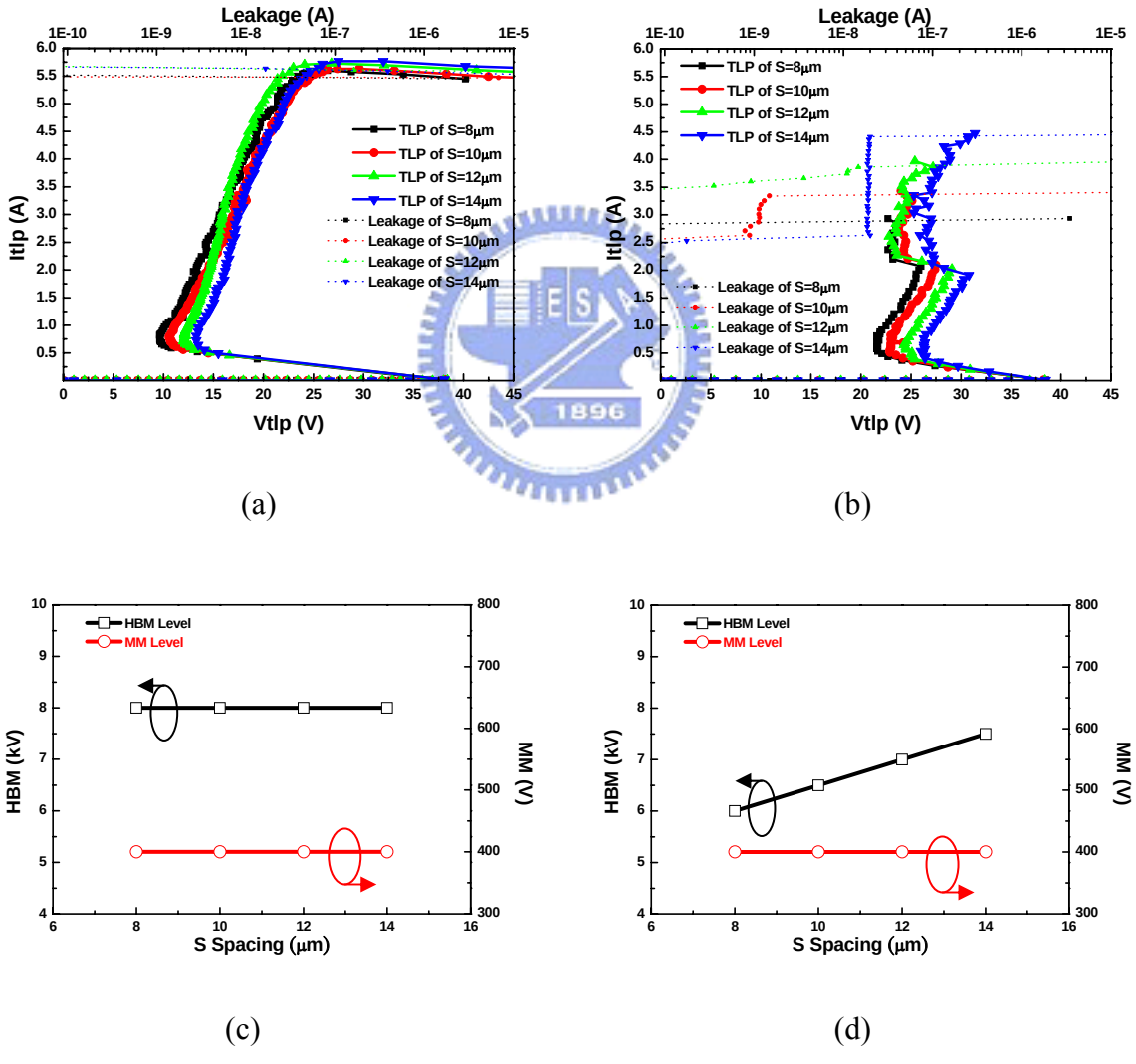


Fig. 3.35 Dual-direction SCR type III : (a) The TLP I-V curves of different S spacing with ESD zap at node 1, (b) The TLP I-V curves of different S spacing with ESD zap at node 2, (c) The HBM and MM levels versus S spacing with ESD zap at node 1, (d) The HBM and MM levels versus S spacing with ESD zap at node 2.

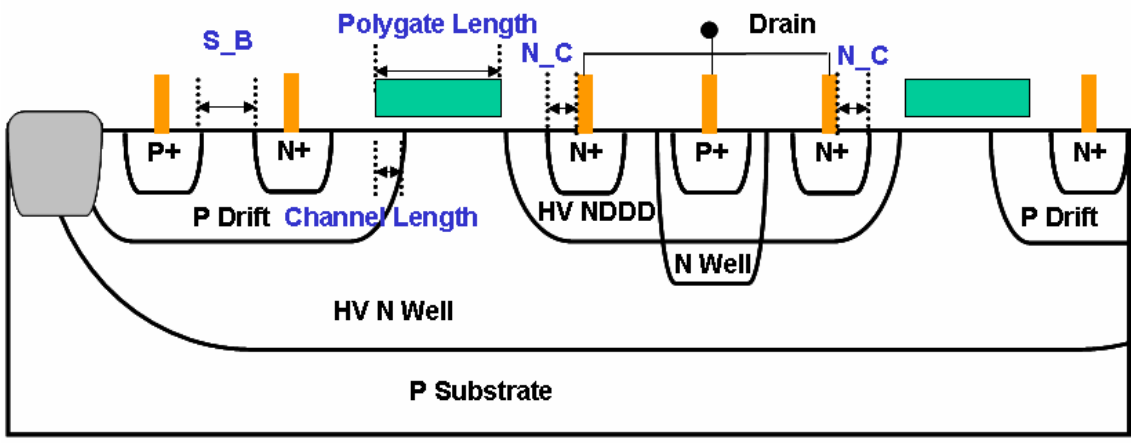
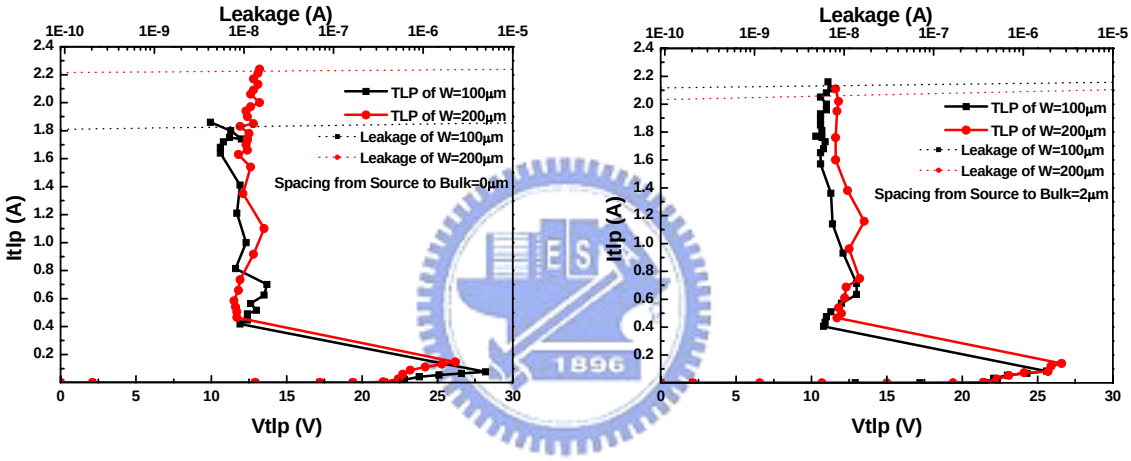
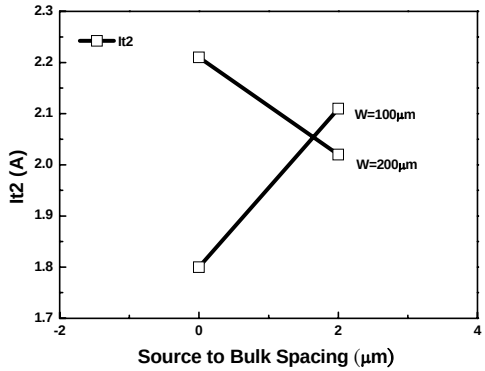


Fig. 3.36 The cross-sectional view of NSCR and the modified parameters.

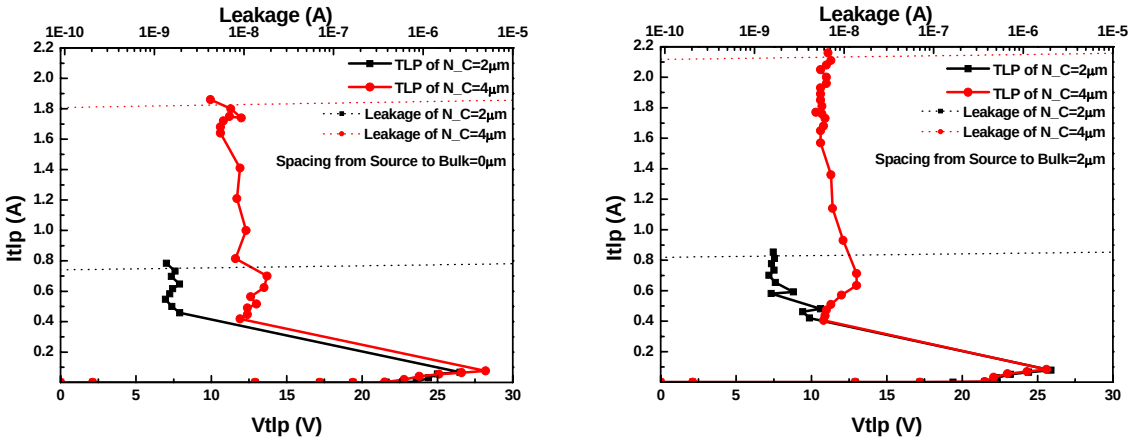


(a) (b)

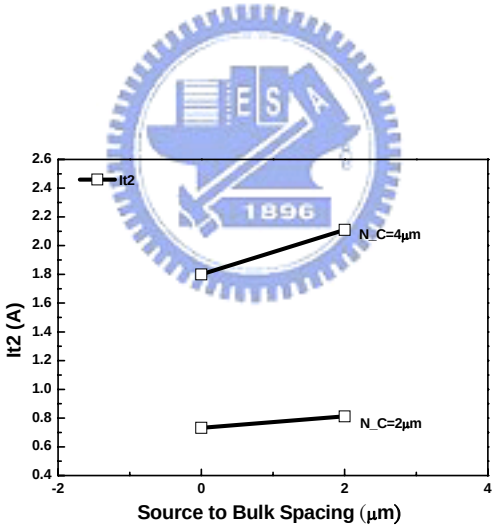


(c)

Fig. 3.37 NSCR : (a) The TLP I-V curves of different total width with S_B spacing=0μm, (b) The TLP I-V curves of different total width with S_B spacing=2μm, (c) The It2 value versus S_B spacing on different total width.

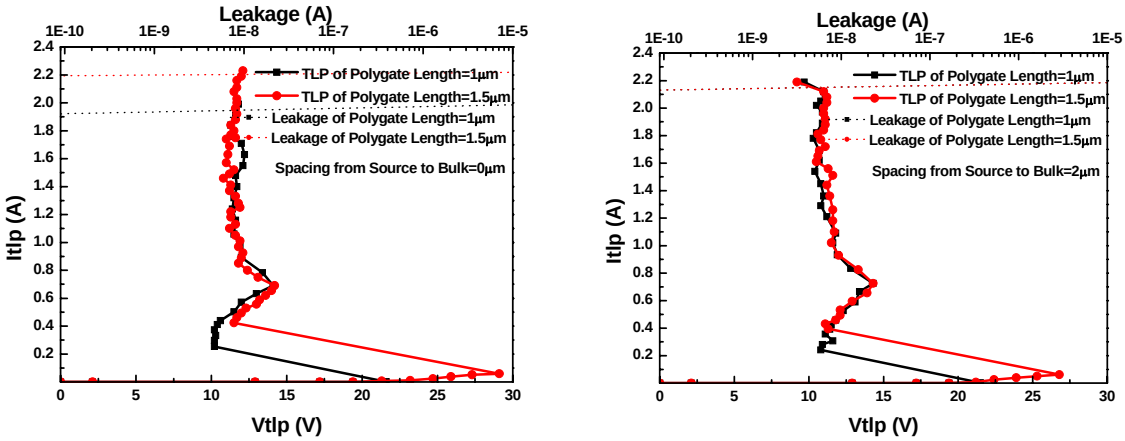


(a) (b)

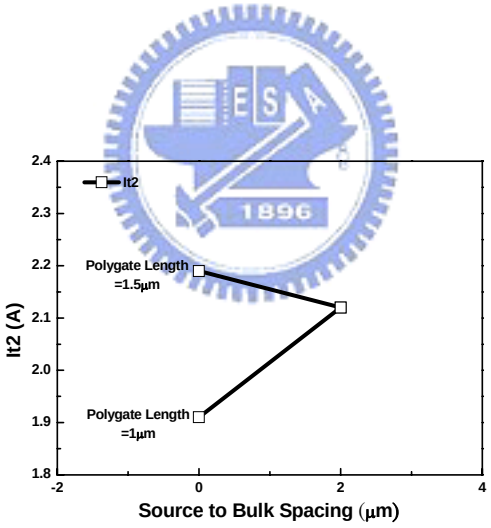


(c)

Fig. 3.38 NSCR : (a) The TLP I-V curves of different N_C spacing with S_B spacing=0μm, (b) The TLP I-V curves of different N_C spacing with S_B spacing=2μm, (c) The It2 value versus S_B spacing on different N_C spacing.

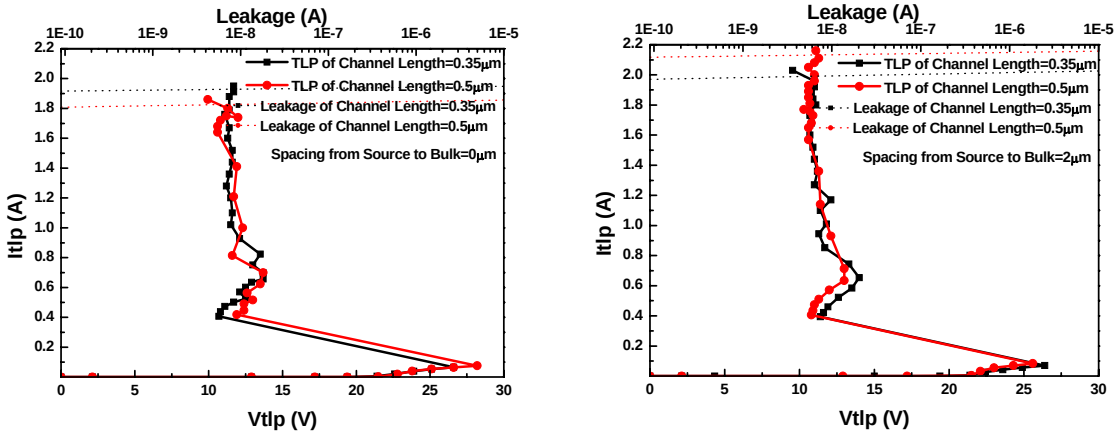


(a) (b)

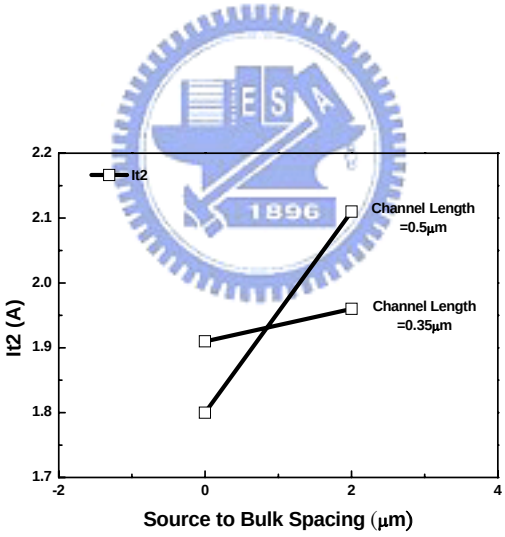


(c)

Fig. 3.39 NSCR : (a) The TLP I-V curves of different polygate length with S_B spacing=0μm, (b) The TLP I-V curves of different polygate length with S_B spacing=2μm, (c) The It2 value versus S_B spacing on different polygate length.



(a) (b)



(c)

Fig. 3.40 NSCR : (a) The TLP I-V curves of different channel length with S_B spacing=0μm, (b) The TLP I-V curves of different channel length with S_B spacing=2μm, (c) The It2 value versus S_B spacing on different channel length.

CHAPTER 4

PROCESS MODIFICATION FOR HIGH-VOLTAGE ESD PROTECTION DESIGN

4.1 The ESD Failure Mechanism of LD-NMOS

According to the chapter 2.2, the turn-on of the BJT and the avalanche breakdown of the N/N+ junction of the LD-NMOS result in the double snapback characteristic. During each snapback period, the voltage of the device will be decreased and the current of the device will be increased substantially. This phenomenon can cause current crowding in the drain area and raise the temperature to the silicon melting point to fuse the drain contact. So, the ESD failure mechanism of the LD-NMOS is due to the double snapback characteristic. If the snapback characteristic can be delayed or be diminished, the device can have longer and large ESD current can be discharged [41]. The turn-on of the BJT can be delayed or diminished by changing the base resistance. The avalanche breakdown of the N/N+ junction can be delayed and diminished by controlling the electric field peak not to approach the N/N+ junction. This chapter will introduce some reported HV devices with additional process layer to have better ESD performance that have been reported and discuss the ESD performance of the small device (total width < 5k μm), the large device (total width > 5k μm) with the PSB (P type Sub Body) layer in a 0.25μm 18V BCD process.

4.2 The High-Voltage BJT with ESD Implantation

The gate-grounded NMOS transistor (GGNMOS), diode strings and SCR with trigger circuit are used in traditional ESD protection. If there are only low-voltage devices available, the high-voltage and high-current characteristics of the lateral bipolar device can be adjusted by changing ESD implant dose and layout modification. The BJT does not require gate oxide and therefore does not need to follow gate oxide constraints. Fig. 4.1(a) shows the lateral bipolar device, the three terminals are separated by STI, the "a_c" denotes the collector-to-STI

distance and the "d_{ESD}" denotes the ESD mask-to-STI distance [42]. During the ESD stresses on the collector, the device breaks down at the N+/P well junction where the ESD implant is located. Then, the bipolar will turn on and go into snapback state. In TCAD simulation, a hot spot develops at S2 location, which finally causes the device damage and the current path will change from S1 path to S2 path during high currents condition.

The breakdown voltage can be modified by tuning the concentration of the ESD implantation. With the increasing of the ESD implant boron dosage, the trigger voltage can be decreased and the holding voltage can be increased by increasing both the a_c and d_{ESD} spacing. Moreover, the turn-on resistance can be decreased by decreasing the "a_c-d_{ESD} spacing" with fixed a_c due to the entering electrons still flow through the high-ohmic diffusion to reach the collector contact, as shown in Fig. 4.1(b) [42]. The parasitic resistance of current path S2 is smaller than S1 due to the deeper current path. In the formula of resistance ($R=\rho L/A$), bigger cross-sectional area causes the smaller resistance.

4.3 The Methods to Enhance ESD Performance in LD-NMOS

The ESD performance in typical LD-NMOS is very awful. Therefore, various LD-NMOS structures have been reported to improve the current capability without changing the breakdown voltage. The failure mechanism of LD-NMOS is attributed to current crowding by the snapback characteristic of parasitic BJT turn-on and the avalanche breakdown characteristic of the N/N+ junction as described in chapter 4.1. So, reduce the strong snapback effect of turned-on BJT or keep the parasitic BJT off are the methods to enhance the ESD performance of LD-NMOS, as described below.

4.3.1 No Turn-On Parasitic BJT by Drain and Gate Clamp Technique

The only practical method to allow the LD-NMOS conduct higher current without parasitic BJT turning on is to use various gate and drain clamp circuits [24]. Through this method, the channel heating effects can be minimum and the ESD level can be optimized by the more uniform turn-on of the LD-NMOS.

If the gate bias gets higher, the driving current will be saturated by the mobility degradation of the channel heating. For power devices, the effective thermal impedance is proportional to pulse width. The pulse width range of non-ESD condition is from tens of μs

to a few ms, whereas the ESD pulse duration is about 100ns. Therefore, the effective thermal impedance for ESD pulse is a fraction of the thermal impedance under normal operating conditions and the channel heating effect can be minimized to gain higher secondary breakdown current (It2). Fig. 4.2(a) compares the I-V measurement of LD-NMOS under ESD pulse and under normal operation. It can be observed that under ESD stress, the only limiting effects are the vertical and lateral fields [24].

To add the zener diodes to clamp drain voltage and gate voltage, respectively, as shown in Fig. 4.2(b) [24]. These clamp circuits are used to prevent the device entering bipolar breakdown. When the transient voltage at the pad exceeds the drain zener clamp voltage, the sufficient gate bias voltage will trigger the LDMOS. When more current flows into the device, the gate potential rises and the LD-NMOS starts to conduct. If a larger gate clamp is used, the It2 value and the HBM level of the LD-NMOS can be increased, but the gate oxide reliability is another important issue needed to concern. The It2 value is determined by the gate zener clamp breakdown voltage or the leakage current of the LD-NMOS.

On the other hand, the drain clamp can increase the power dissipation, so the smaller drain clamp can enhance ESD performance. For larger device total width with multiple fingers, the device can be turned on more uniformly by adding the resistor between the gate and source terminal, then the ESD level can also be enhanced. In summary, the optimized ESD performance of the LD-NMOS can be obtained by using the adequate gate clamp, smaller drain clamp with satisfied operating voltage range, larger device total width to discharge ESD currents and the added resistor between the gate and source sides to enhance the uniform turn-on characteristic..

4.3.2 No-Snapback Characteristic by Adaptive Layer Technique

Because the snapback mechanism is caused by the positive feedback between the parasitic BJT turn-on in the source side and the avalanche breakdown of the N/N+ junction in the drain side. The no-snapback LD-NMOS can be implemented by adding the adaptive layer beneath the drain and source side, respectively. Fig. 4.3(a) shows the added adaptive layer in the LD-NMOS to suppress the snapback effect [43]-[44].

During ESD stress condition and after the BJT turns on, the drain N/N+ junction is reverse biased by the voltage ($V = R_d \times I_d$), where the R_d denotes the drain resistance and the I_d denotes the drain current. In order to prevent the snapback effect happening, it is necessary to reduce the V below the N/N+ junction avalanche breakdown voltage. The method is to

reduce the R_d by inserting a N-type high doping concentration drain adaptive layer beneath the N+ diffusion. Through this method, the more I_d is needed to cause junction breakdown. Therefore the trigger current of N/N+ junction should be increased. Fig. 4.3(b) shows the device with different N-type doping concentration adaptive layer, the bend 1 is the turn-on point of the BJT and the bend 2 is the drain avalanche point [43]-[44]. With increasing the doping concentration, the bend 2 moves upward and the snapback effect can be reduced effectively.

On the other hand, to avoid the BJT in the source side turn-on is another issue. The BJT can be turned on easily by increasing base resistance. So, to reduce the base resistance can prevent the BJT turning on. The added adaptive layer in the source side is a P-type high doping concentration layer, it can reduce the base resistance substantially. Through this method, the more current is needed to turn on the BJT. With increasing the doping concentration of the body adaptive layer, the base resistance can be reduced and the bend 1 moves to higher current, as shown in Fig. 4.3(c) [43]-[44]. In addition, curve A of Fig. 4.3(c) shows the base resistance is converged.

The adaptive layer in both sides can suppress the snapback effect by adjusting on/off condition of the BJT turns in the source side and N/N+ junction avalanche breakdown in the drain side. Therefore, the failure mechanisms can be avoided and the ESD performance of LD-NMOS can be enhanced.

4.4 Experimental Results and Failure Analysis

The additional layer in this experiment is similar to the adaptive layer as above. This layer is named PSB (P type Sub Body) layer and it is also a high doping P type layer. The original concept to design this layer is to decrease the base resistance of the parasitic BJT and increase the holding voltage after snapback condition. On the other hand, to decrease the base resistance of the parasitic BJT can also enhance the turn-on uniformity. By appropriate modifying the doping concentration, the snapback characteristic of the parasitic BJT can be avoided in 0.25μm 18V BCD process. There are small device (total width < 5k μm) and large device (total width > 5k μm) with and without the PSB layer had been experimented and discussed the influence on ESD performance. In addition, the failure analysis is presented in large device (total width = 20k and 80k μm) with the guardring floating and grounded.

4.4.1 *The Small Device with and without PSB Layer*

To investigate the influence on ESD performance, the small device (total width = 200μm and one finger width = 50μm) with and without the PSB layer had been experimented, as shown in Fig. 4.4. The N+ edge to contact spacing of the drain side is fixed at 10μm to enhance the ESD performance and to avoid the device destroying so early. The modified parameters are the source to bulk spacing of the source side named S_B and the channel length.

Table 4.1 shows the various ESD data when the small LD-NMOS device without the PSB layer. To find out the ESD performance of device without the PSB layer, with increasing the channel length from 15μm to 30μm, the holding voltage can be increased from 22V to 26V. With increasing the channel length from 15μm to 30μm and S_B spacing from 0 to 10μm, the trigger voltage will be increased a little, the holding voltage and the It2 value will be increased about 3V and 2A when the S_B spacing is 0μm, respectively, as shown in Figs. 4.5(a) and 4.5(b). Therefore, the large channel length can enhance the holding voltage and It2 value substantially.

Table 4.2 shows the various ESD data when the small LD-NMOS device with the PSB layer. To find out the ESD performance of device with the PSB layer, with increasing the channel length from 15μm to 30μm, the holding voltage can be increased from 23V to 27V. With increasing the channel length from 15μm to 30μm and S_B spacing from 0 to 10μm, the trigger voltage and the holding voltage can be increased from 35V to 43V and 27V to 35V when the S_B spacing is 0μm, respectively, as shown in Figs. 4.6(a) and 4.6(b). The It2 can be also increased by the increasing channel length.

Comparing with the Table 4.1 and 4.2, the PSB layer can enhance the trigger voltage and holding voltage substantially when the S_B spacing is 0μm, but the It2 value may be decreased a little due to the larger holding voltage

4.4.2 *The Large Device with and without PSB Layer*

The large device of LD-NMOS had been fabricated by minimum design rule and had been designed as ESD protection device and output current driver, simultaneously. The cross-sectional and layout diagram of large device with the PSB layer and guardring are shown in Figs. 4.7(a) and 4.7(b). Figs. 4.8(a) and 4.8(b) show the TLP I-V curve of large device (total width = 5k, 20k and 80k μm and guardring floating) without and with PSB layer,

respectively. Figs. 4.9(a) and 4.9(b) show the TLP I-V curve of large device (total width = 5k, 20k and 80k μm and guardring grounded) without and with PSB layer, respectively. The It2 value and the turn-on uniformity can be further increased by the PSB layer substantially. Comparing the leakage current of Fig. 4.8(a) and Fig. 4.8(b), the device with the PSB layer can decrease the leakage current. Therefore, by adding the PSB layer, the LD-NMOS with no snapback characteristic can be implemented successfully.

4.4.3 The Failure Analysis of Large Device

Figs. 4.10(a) and 4.10(b) show the SEM images of the large LD-NMOS device with PSB layer (total width = 80K) with guardring floating and with guardring grounded, respectively. The failure locates at center finger while the guarding is floating and the failure locates at corner while the guarding is grounded. Figs. 4.11(a) and 4.11(b) show the SEM images of the large LD-NMOS device with PSB layer (total width = 20k) with guardring floating and with guardring grounded, respectively. The failure location of the device total width = 20k is similar to the device total width = 80k. Therefore, the guardring grounded type will conduct the ESD current to the corner and damage the corner fingers. The guardring floating type can have better ESD performance than the guardring grounded type..

4.5 Summary

The failure mechanism of LD-NMOS is the snapback characteristic. To suppress the parasitic BJT turn-on of source side and the N/N+ junction avalanche breakdown of drain side can both improve the turn-on uniformity and ESD performance. The PSB layer can increase the trigger voltage and holding voltage in small LD-NMOS device, but decrease the It2 value a little while the source and bulk regions are butted. Moreover, The PSB layer can increase the It2 value in large LD-NMOS device substantially and improve the leakage current while the guardring is floating.

Table 4.1

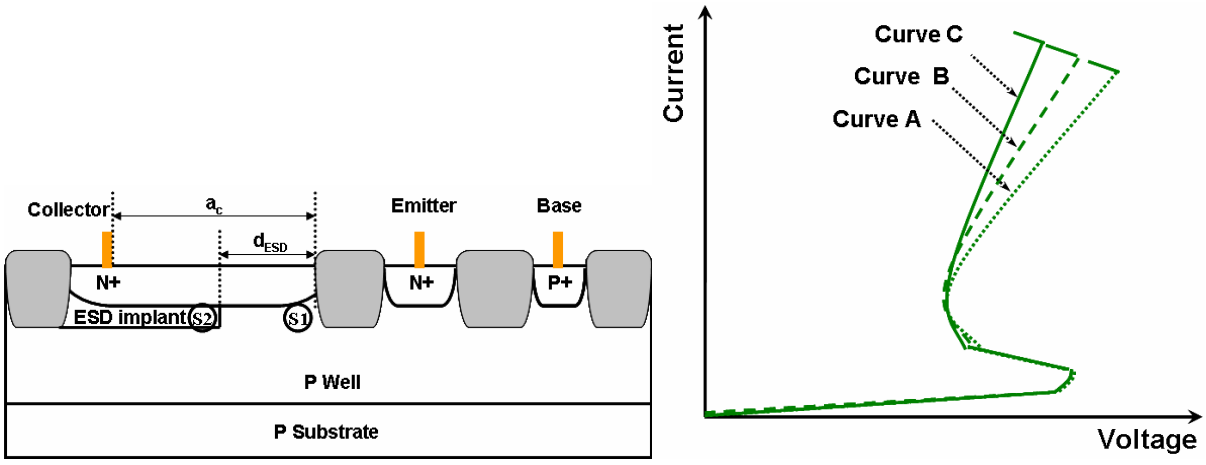
The ESD characteristics of the small LD-NMOS device without the PSB layer.

Channel Length (μm)	S_B Spacing (μm)	Trigger Voltage (V)	Holding Voltage (V)	It2 (A)
15	0	30.8	24.1	1.46
15	5	30.2	22.4	1.97
15	10	29.7	22.4	2.7
30	0	31.3	27.2	3.97
30	5	31.2	26.8	3.64
30	10	31.2	26.4	2.69

Table 4.2

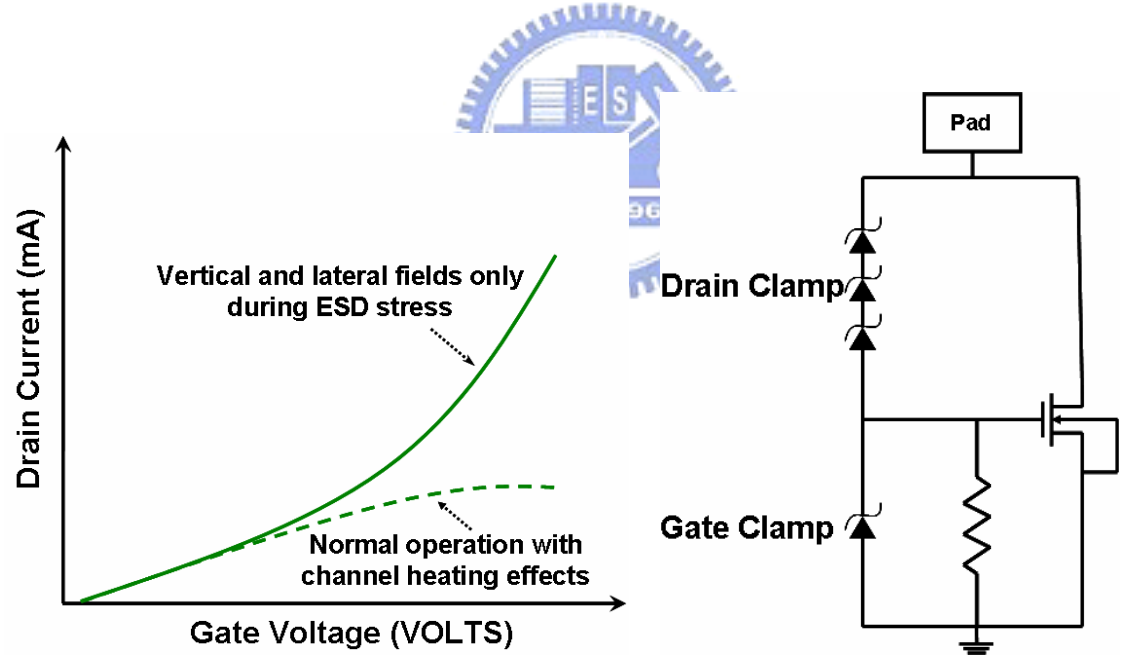
The ESD characteristics of the small LD-NMOS device with the PSB layer.

Channel Length (μm)	S_B Spacing (μm)	Trigger Voltage (V)	Holding Voltage (V)	It2 (A)
15	0	35	26.7	2.85
15	5	30.2	23.3	3.6
15	10	29.5	23.1	2.62
30	0	42.9	34.8	3.16
30	5	32.4	27.7	3.8
30	10	31.3	27.5	4.28



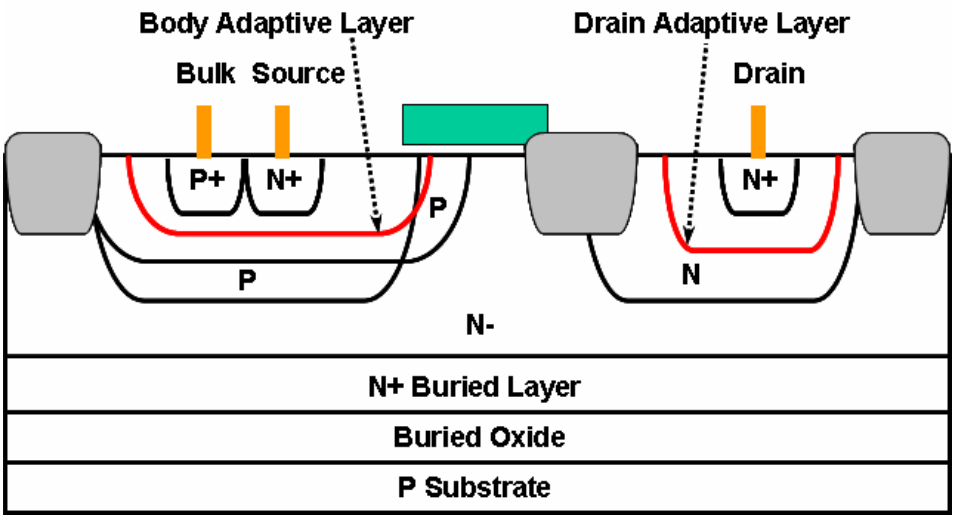
(a) (b)

Fig. 4.1 (a) The cross-sectional of lateral NPN device with ESD implant, (b) Measured I-V curve for different d_{ESD} but fixed a_c, with increasing the a_c-d_{ESD} spacing, the current will flow through the collector diffusion and the resistance will increased. The a_c-d_{ESD} spacing is curve A > curve B > curve C.

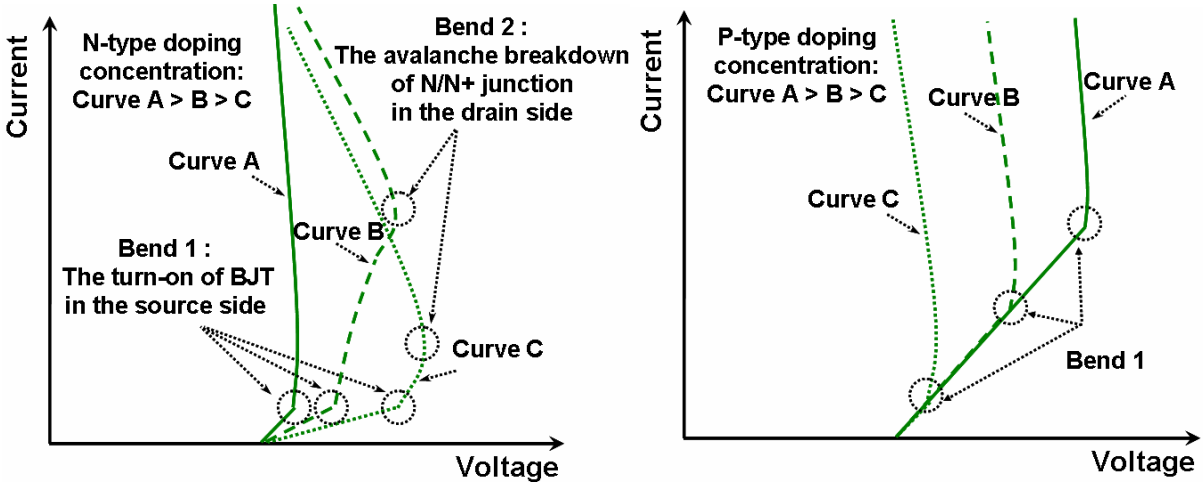


(a) (b)

Fig. 4.2 (a) The I-V curve of normal operation and ESD stress by curve tracer, (b) The drain and gate clamp structure with a gate-grounded resistor.



(a)



(b) (c)

Fig. 4.3 (a) The adaptive layer structure of LD-MOS on both drain and source sides, (b) The influence on snapback effect by drain adaptive layer, (c) The influence on snapback effect by body adaptive layer.

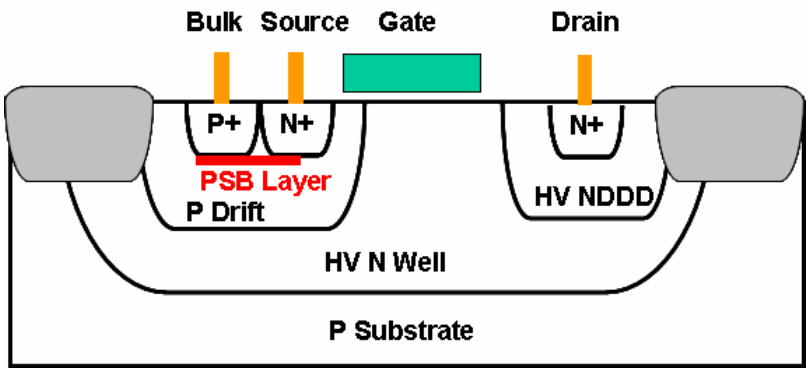
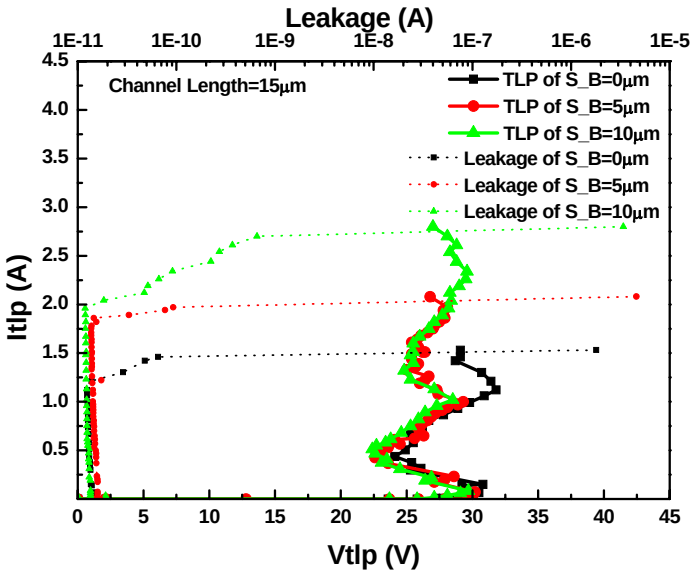
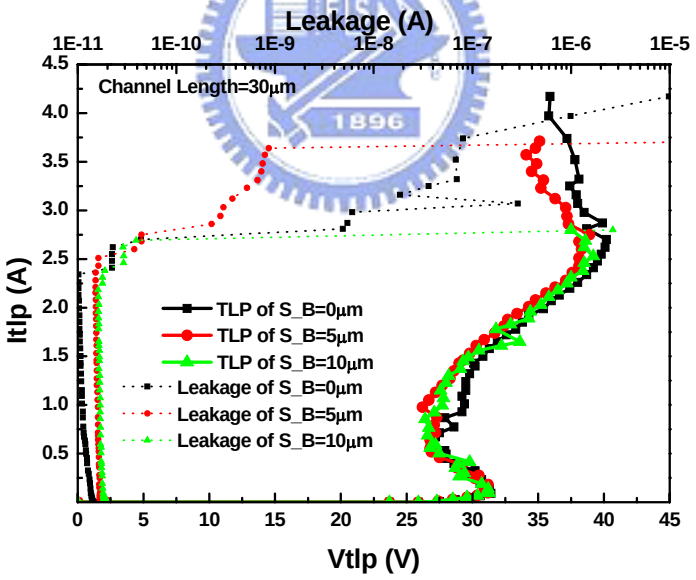


Fig. 4.4 The cross-sectional view of small LD-MOS device with the PSB layer.

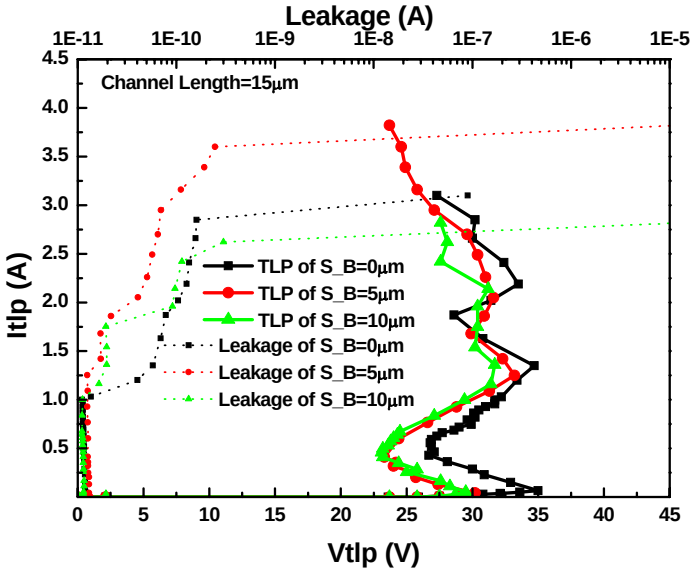


(a)

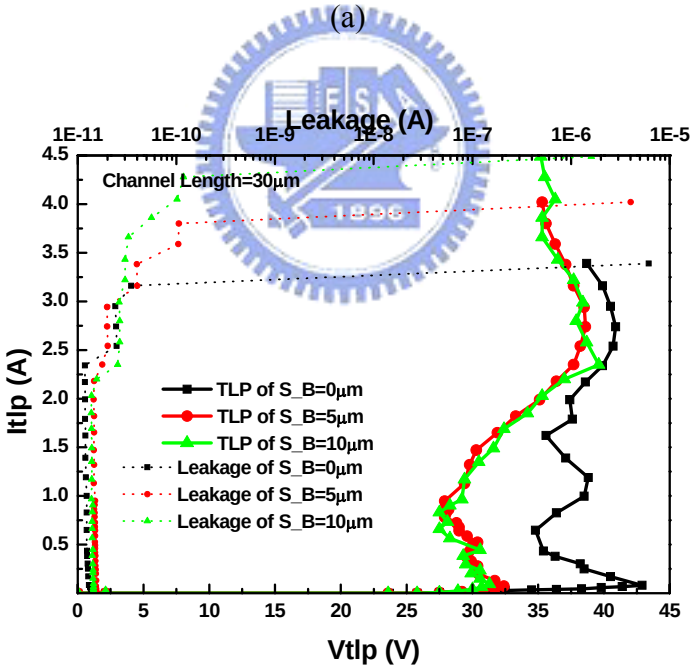


(b)

Fig. 4.5 (a) The TLP I-V curves of different S_B spacing in small LD-NMOS device without PSB layer (channel length = 15μm), (b) The TLP I-V curves of different S_B spacing in small LD-NMOS device without PSB layer (channel length = 30μm).

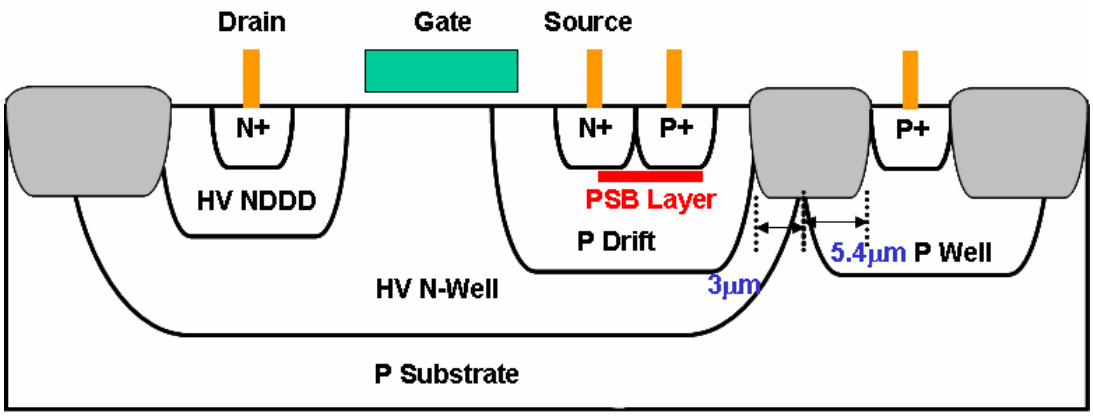


(a)

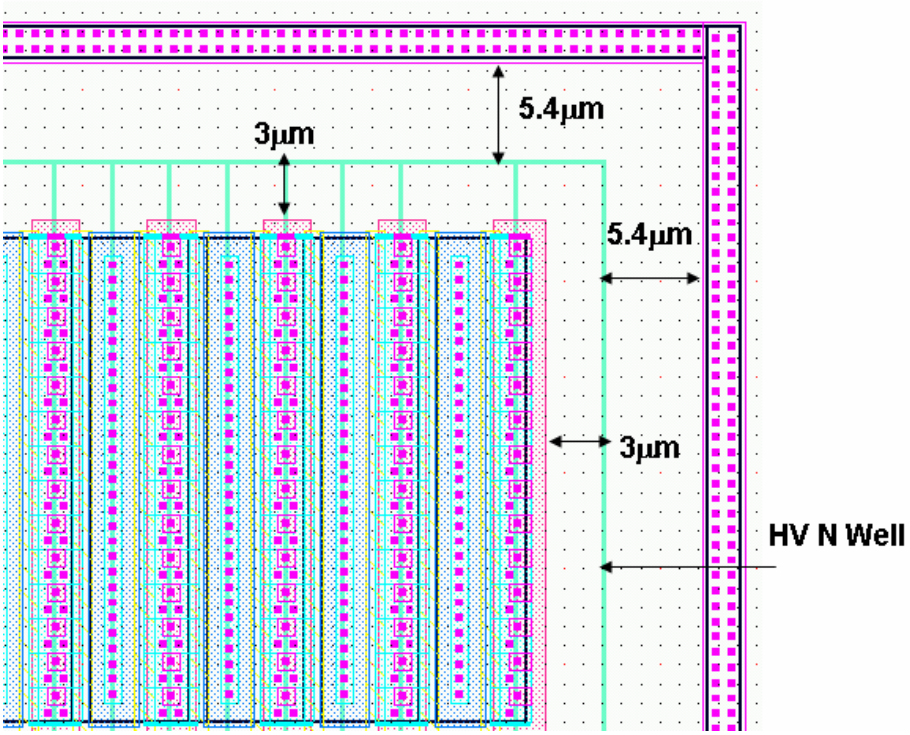


(b)

Fig. 4.6 (a) The TLP I-V curves of different S_B spacing in small LD-NMOS device with PSB layer (channel length = 15μm), (b) The TLP I-V curves of different S_B spacing in small LD-NMOS device with PSB layer (channel length = 30μm).

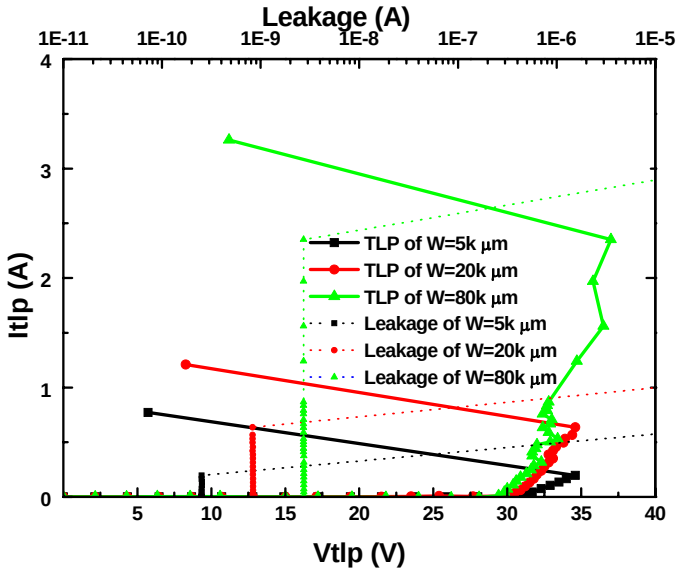


(a)

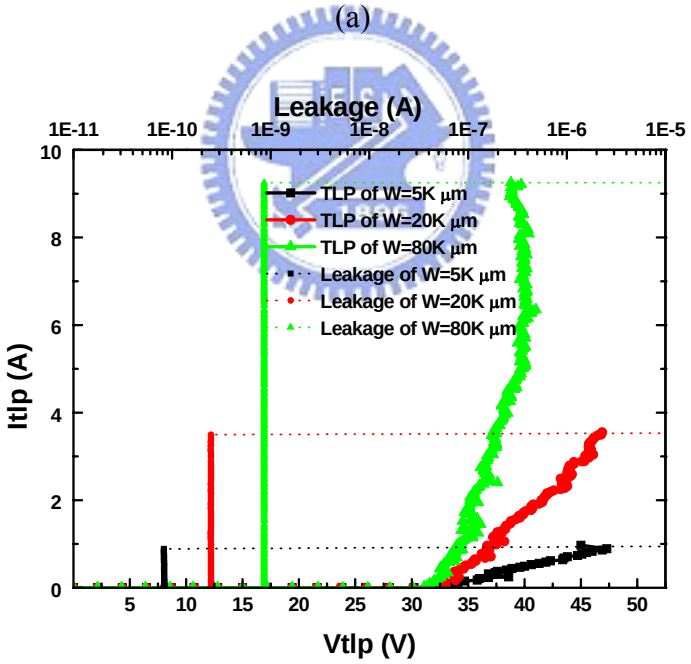


(b)

Fig. 4.7 (a) The cross-sectional view of large LD-MOS device with the PSB layer and guarding, (b) The layout diagram of the large device.

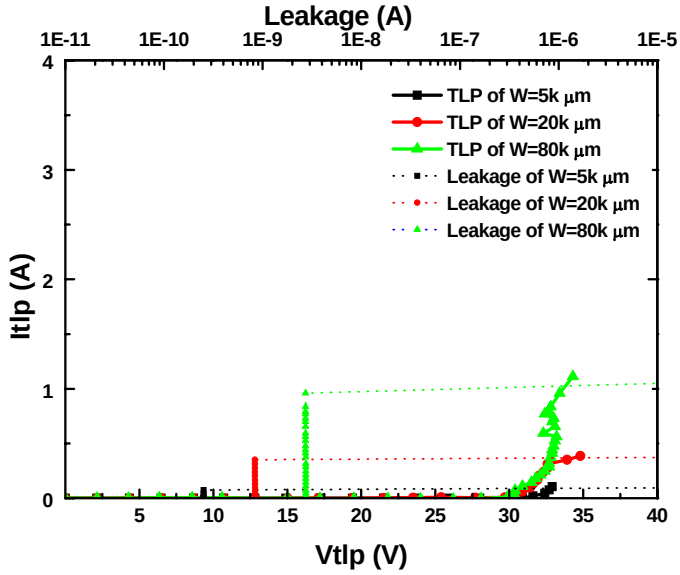


(a)

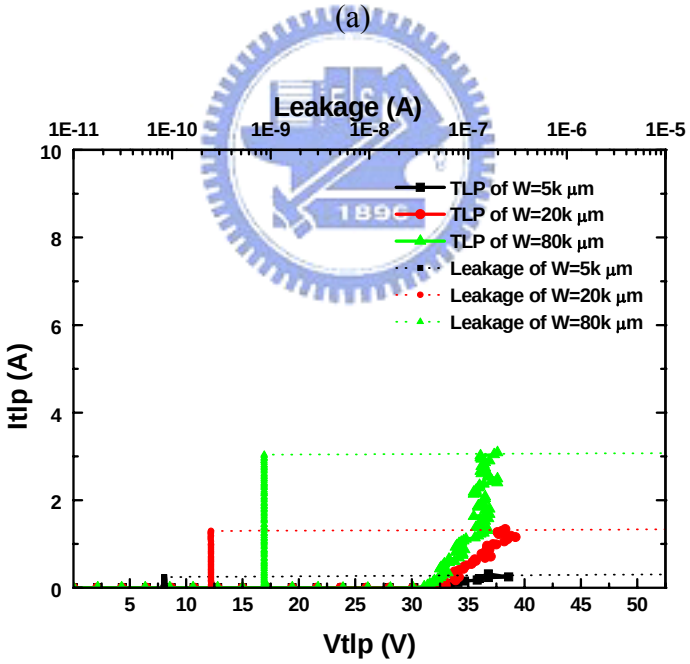


(b)

Fig. 4.8 (a) The TLP I-V curves of large LD-NMOS device without PSB layer and guardring floating, (b) The TLP I-V curves of large LD-NMOS device with PSB layer and guardring floating.

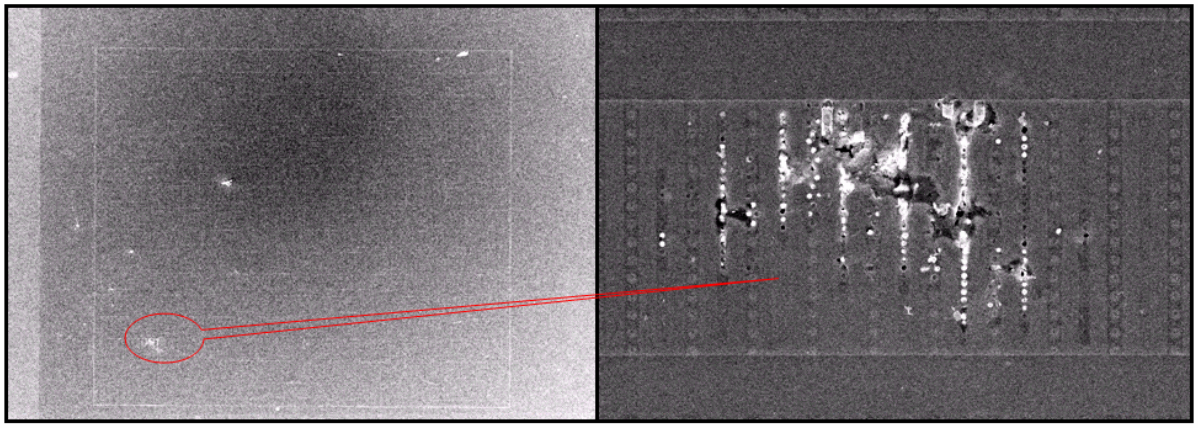


(a)

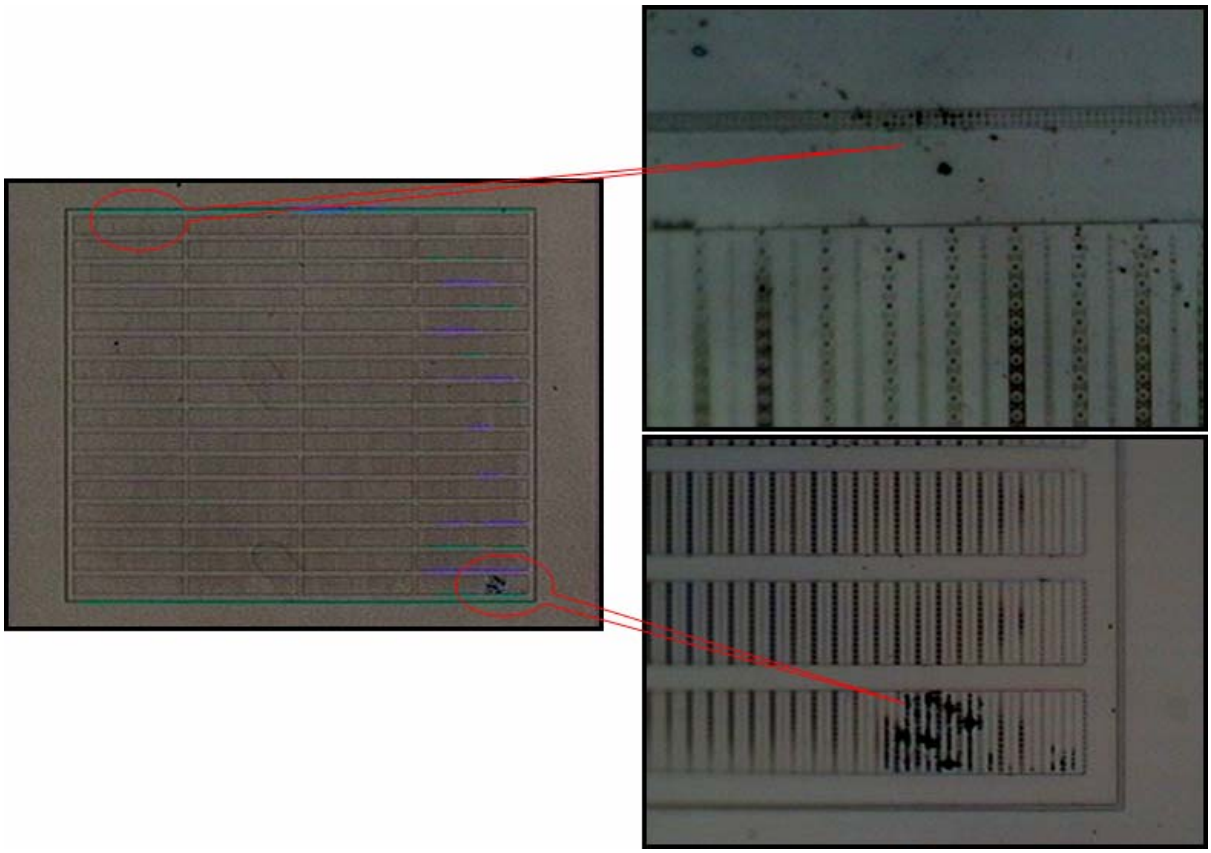


(b)

Fig. 4.9 (a) The TLP I-V curves of large LD-NMOS device without PSB layer and guardring grounded, (b) The TLP I-V curves of large LD-NMOS device with PSB layer and guardring grounded.

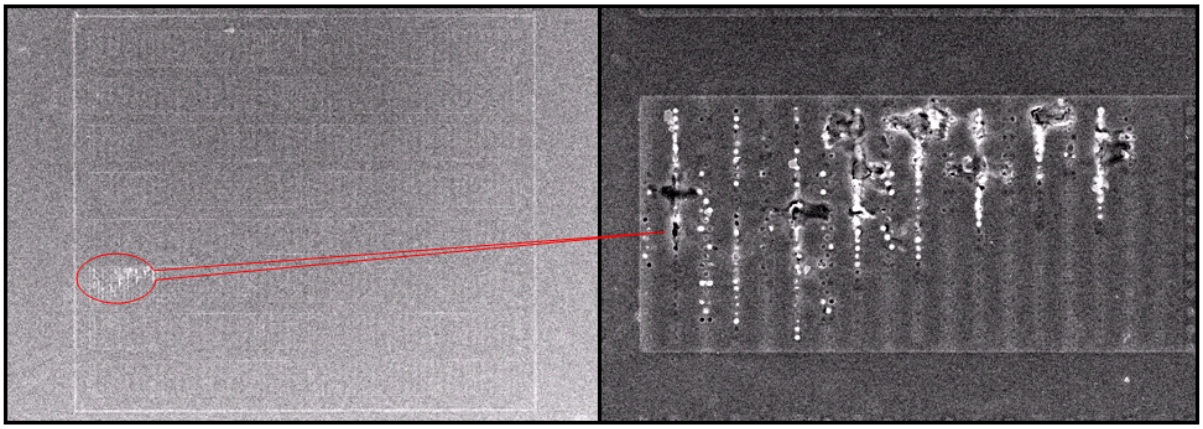


(a)

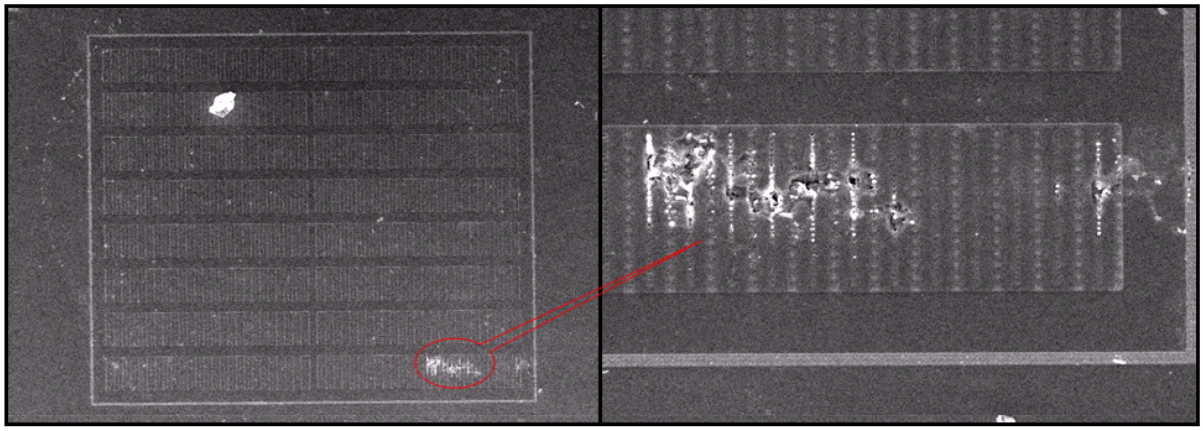


(b)

Fig. 4.10 (a) The SEM image of large LD-NMOS device (total width = 80k μm) with PSB layer and guarding floating, (b) The SEM image of large LD-NMOS device (total width = 80k μm) with PSB layer and guarding grounded.



(a)



(b)

Fig. 4.11 (a) The SEM image of large LD-NMOS device (total width = 20k μm) with PSB layer and guarding floating, (b) The SEM image of large LD-NMOS device (total width = 20k μm) with PSB layer and guarding grounded.

CHAPTER 5

CONCLUSIONS AND FUTURE WORKS

5.1 Main Results of This Thesis

In this thesis, the various ESD protection devices have been developed for BCD process with high ESD robustness. Each of the ESD protection devices has been successfully verified in the testchips.

In chapter 2, the turn-on mechanism and double-snapback characteristic of HV LD-NMOS and HV NMOS has been discussed. The turn-on mechanism of LD-NMOS is composed of the turn-on parasitic BJT and the N/N+ junction avalanche breakdown. After the BJT turns on, the electric field peak will move toward the drain side and cause the N/N+ junction breakdown. The feedback between the BJT and N/N+ junction will improve the snapback characteristic. The double-snapback characteristic of the HV NMOS depends on the device structure. If the current path won't change after the device go into first snapback, the device will not have the second snapback chance.

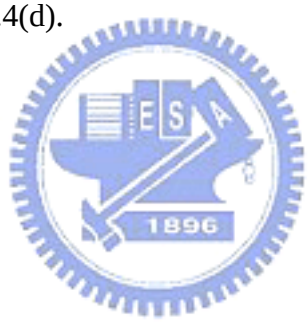
In chapter 3, there are several splits on HV LD-NMOS, HV LD-PMOS, HV NFOD, HV NSCR and HV dual-direction SCR. The dominant factor to improve the ESD performance of LD-NMOS, NFOD and NSCR is the N+ edge to contact spacing of the drain side. Unfortunately, the ESD performance of the LD-PMOS in several testkeys is very insufficient to pass the standard ESD specification. In dual-direction SCR, the holding voltage can be modified to over than the operation voltage and to avoid the latchup effect. The It2 value, HBM and MM level of the dual-direction SCR are about 4A, 6KV and 300V, respectively.

In chapter 4, the PSB layer is added to small device and large device of LD-NMOS to investigate the ESD performance. The holding and trigger voltage of small LD-NMOS device can be increased by the PSB layer substantially while the source and bulk regions are butted. The PSB layer can decrease the base resistance of the parasitic BJT and improve the turn-on uniformity of the large LD-NMOS device with the minimum rule. Therefore, the It2 value of the large LD-NMOS device with the PSB layer can be increased.

5.2 Future Works

The trigger voltage of the dual-direction SCR is relative high to protect the internal circuit. The extra trigger element is added to reduce the trigger voltage, as shown in Fig. 5.1 [45]. By using the spacing between the HV N Wells, the additional layout area is not needed. Through this trigger method, the dual-direction SCR will have the same trigger voltage on both sides.

The difference holding voltage of TLP and 370A has been found in dual-direction SCR. Even though the holding voltage of TLP is more than the operation voltage, the holding voltage measured by 370A will be only 2V, as shown in Figs 5.2 and 5.3(a) ~ 5.3(d). To investigate the reason and try to improve the holding voltage in DC domain is the next research topic. In addition, the holding voltage and trigger voltage of DC I-V curve in LD-NMOS are also different from TLP I-V curve, as shown in Figs 5.4(a) ~ 5.4(b), but the holding voltage and trigger voltage of DC I-V curve in LD-PMOS are the same as TLP I-V curve, as shown in Figs 5.4(c) ~ 5.4(d).



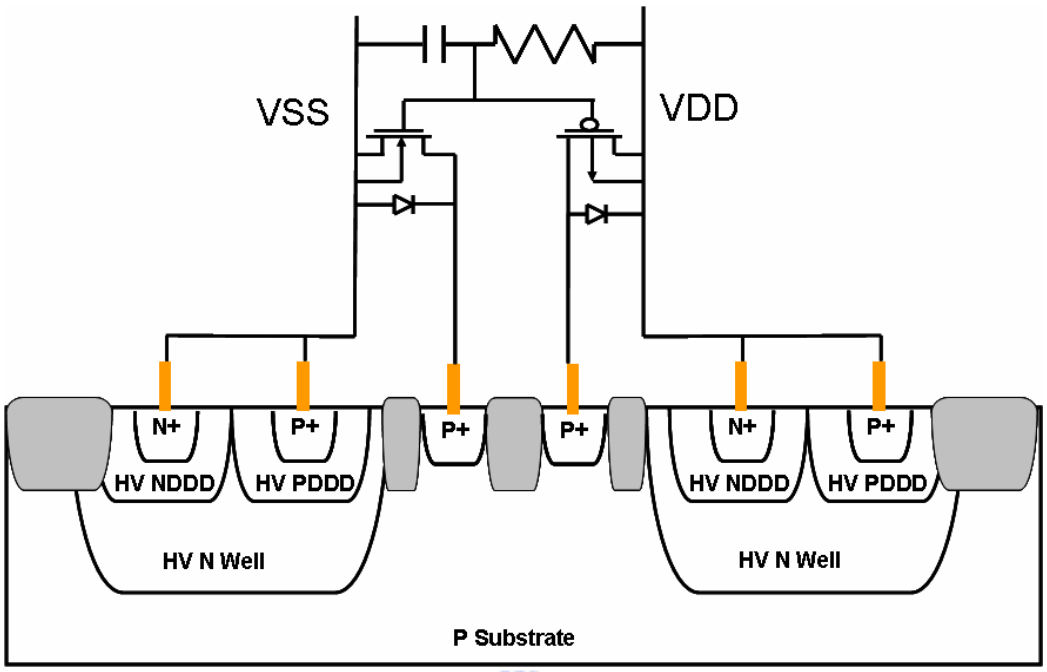


Fig. 5.1 The added trigger element to trigger the dual-direction SCR on both sides.

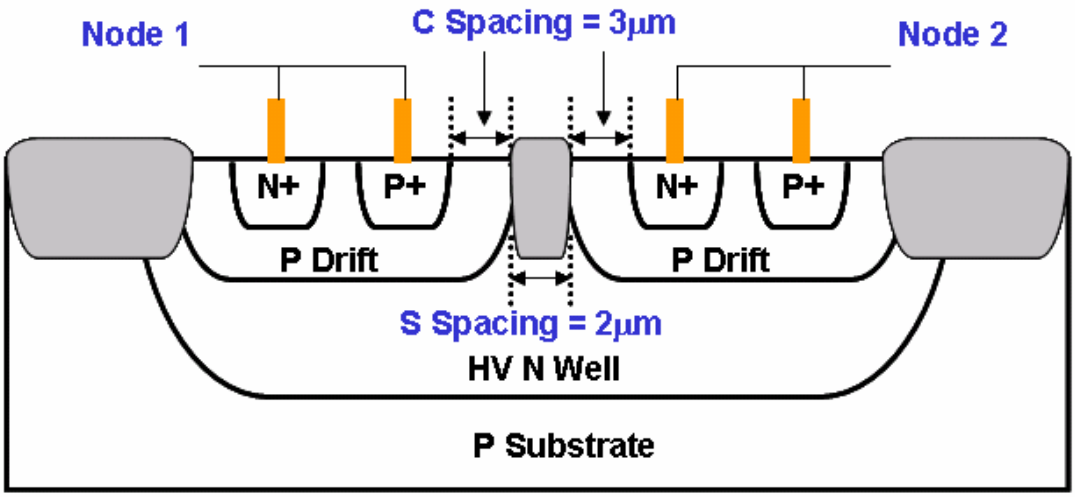


Fig. 5.2 The dual-direction SCR measured by TLP and 370A.

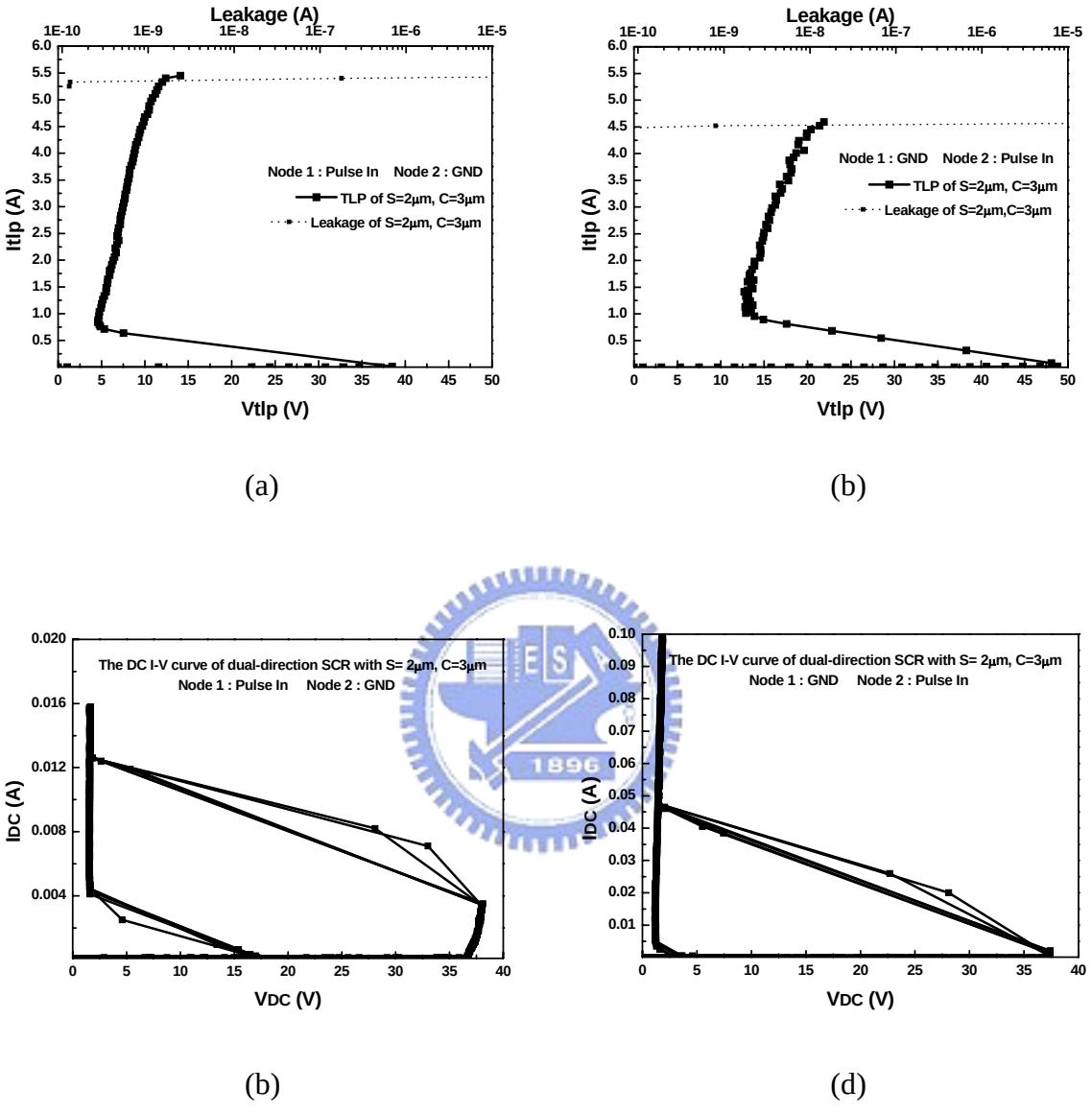


Fig. 5.3 (a) The TLP I-V curve of dual-direction SCR with node 1 pulse in and node 2 GND, (b) The TLP I-V curve of dual-direction SCR with node 2 pulse in and node 1 GND, (c) The DC I-V curve of dual-direction SCR with node 1 pulse in and node 2 GND, (d) The DC I-V curve of dual-direction SCR with node 2 pulse in and node 1 GND.

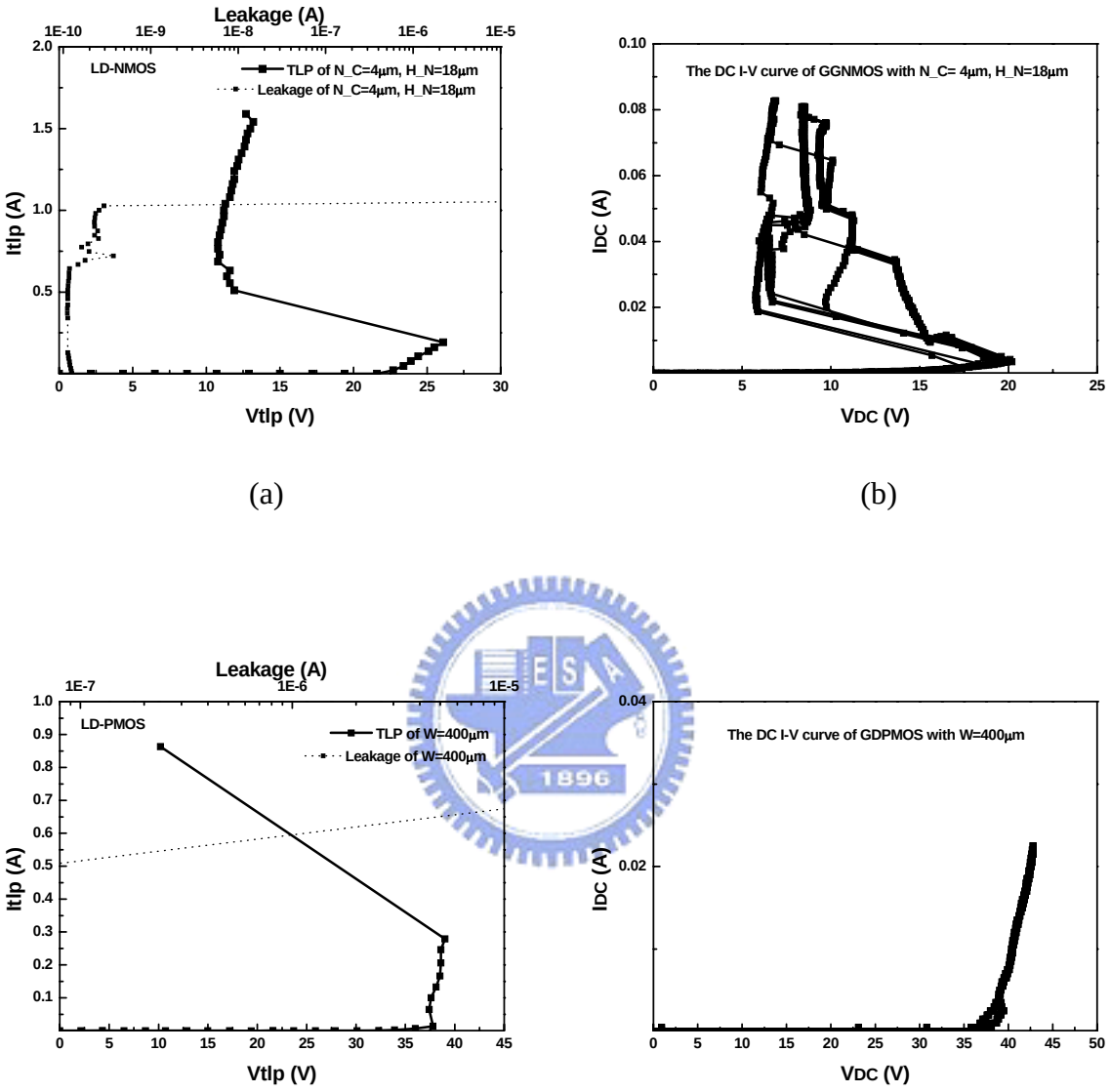


Fig. 5.4 (a) The TLP I-V curve of LD-NMOS with N_C=4μm, H_N=18 μm, (b) The DC I-V curve of LD-NMOS with N_C=4μm, H_N=18 μm, (c) The TLP I-V curve of LD-PMOS with W=400μm, (d) The DC I-V curve of LD-PMOS with W=400μm.

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