國立交通大學

電機學院微電子奈米科技產業研發碩士班

碩 士 論 文

可寫入抹除高介電常數氮氧化鉿金屬–絕緣層–矽 電容

A Program-Erasable High-κ $Hf_3N_2O_5$ Metal-Insulator-Silicon Capacitor

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摘　　要

記憶體電容是決定檢測訊號電壓、速度、資料保存時間、耐久性以及防止軟性誤差的重要參數。然而隨著超大型積體電路技術不斷的微縮，電容面積勢必隨之遞減，以期達到減少元件尺寸及降低成本的需求，但此舉將減低電容厚度造成不必要的漏電流，為了解決此問題，傳統的二氧化矽將被高介電常數材料所取代，以達高電容密度及降低漏電流，此外記憶體電容也渴望具有可寫入抹除和良好資料保存等特性。

本文將探討使用高介電常數氮氧化鉿為介電層的 可寫入抹除 金屬-絕緣層-矽 結構電容，其可應用在記憶體上例如:動態隨取記憶體(DRAM)與快閃記憶體(Flash)。此元件具有高電容密度約 6.5 fF/μm^2、低寫入-抹除電壓 ±5V、大記憶體視窗 1.5V 以及優異資料保存特性。此外經由漏電流特性分析計算出其蕭基能障與電子捕捉能階，發現氮氧化鉿蕭基能障為 0.69~0.7 eV 且具有較深的電子捕捉能階約 1.01~1.05 eV。

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ABSTRACT

Memory cell capacitance is the crucial parameter which determines the sensing signal voltage, speed, data retention times, endurance and against the soft error event. However, the very large scale integration (VLSI) technology is continues down-scaling of the size of capacitors to reduce chip size and the cost. It will decrease dielectric thickness and result in the undesired leakage current. To solve this problem, the conventional silicon dioxide will be replaced with high dielectric constant (high-κ) materials to increase the capacitance density and degrade the leakage current. Besides, capacitors also desire both good data retention and program-erasable capability for memory applications.

In this study, we demonstrate a programmable-erasable MIS capacitor with a single high-κ $Hf_3N_2O_5$ dielectric layer for many applications such as volatile DRAM and non-volatile MONOS type memories. This device showed a capacitance density of ~ 6.5 fF/μm^2, low program and erase voltages of +5 and -5 V, and a large ΔV_{th} memory window of 1.5V. In addition the 25^{o}C data retention was good, as in program and erase decay rates of only 2 and 6.2 mV/dec. In addition, we found a deep trapping level of 1.01~1.05 eV from measured *J-V* characteristics. The electrodes displayed a Schottky barrier height of 0.69~0.7 eV.

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Chapter 1

Introduction

1.1 Motivation to study high-κ dielectrics

The industry's demand for greater integrated circuit functionality and performance at lower cost requires an increased circuit density, which has translated into a higher density of transistors on a wafer. This rapid shrinking of the transistor feature size has forced the channel length and gate dielectric thickness to also decrease rapidly. However, the scaling trend of MOSFETs devices will produce the large leakage current due to thinner gate oxide [1.1]. To reduce the leakage current related higher power consumption in highly integrated circuit and overcome the physical thickness limitation of silicon dioxide, the conventional SiO_2 will be replace with high dielectric constant (high-κ) materials as the gate dielectrics beyond the 65nm technology mode [1.2]-[1.7]. Therefore, the engineering of high-κ gate dielectrics have attracted great attention and played an important role in technology pull for VLSI. Although high-κ materials often exhibit smaller band gap and higher defect density than conventional silicon dioxide, using the high-κ gate dielectric can increase efficiently the physical thickness in the same effective oxide thickness (EOT) that shows lower leakage characteristics than silicon dioxide by several orders without the reduction of capacitance density [1.3]-[1.6].

According to the ITRS (International Technology Roadmap for Semiconductor) [1.8], the thickness of gate oxide has to be below 10Å after 2008. Besides, the suitable gate dielectrics must have κ value more than 8 for 50-70 nm technology nodes and that must be more than 15 when the technology dimensions less than 50 nm. Fig. 1-1 shows the evolution of MOSFET technology requirement.

As an alternative to oxide/nitride systems, much work has been done on high-κ metal oxides as a means to provide a substantially thicker (physical thickness) dielectric for reduced leakage and improved gate capacitance. In the search of finding suitable high-κ gate dielectrics for use beyond oxynitride systems, several approaches have been used in fabricating potential materials candidates. To find out the suitable high-κ dielectrics are significant task to the next VLSI generation.

1.2 Overview of high-κ dielectrics

Many of the materials initially chosen as potential alternative gate dielectric candidates were inspired by memory capacitor applications and the resultant semiconductor manufacturing tool development infrastructure. The most commonly studied high-κ gate dielectric candidates such as Ta_2O_5, SrTiO3, and Al_2O_3 which have dielectric constants ranging from 10 to 80, and have been employed mainly due to their maturity in memory capacitor applications. With the exception of Al_2O_3, however, these materials are not thermodynamically stable in direct contact with Si [1.1]. Moreover, the oxides should preferably be amorphous and able to withstand processing at high temperatures of up to 1000 °C. The leading contenders are the Hf, Zr, and La oxides. However, these oxides are not good glass formers like SiO_2 and they tend to crystallize well below 800 °C. Silicates or aluminates can be used instead of oxides as they crystallize much less easily, but at the expense of a lower κ [1.9].

The gate electrode in CMOS devices is traditional made of polysilicon. However, as the technology down-scaling, device performance and reliability can be seriously degraded by the intolerably high direct-tunneling leakage current, increased gate resistance, worsened polysilicon gate depletion, and boron penetration [1.12]-[1.13]. To alleviate these problems, a high dielectric constant (high-κ) gate insulator and metal gate have been proposed to meet the stringent performance requirement. For the high-κ dielectrics, replacing the conventional

polysilicon gate electrode with metal gate has been proposed because of the interface instability between the high-κ dielectrics and polysilicon gate [1.10]. The work function (Φ_m) of metal (in Fig. 1-2) play an important role for metal-gate/high-κ MOSFET. The preferred work function of the metals are ~5.1 eV for p-MOSFETs and ~4.2 eV for n-MOSFETs. Refractory metal nitrides such as tantalum nitride (TaN) and titanium nitride (TiN) have been extensively investigated as the potential solutions to replace poly-Si [1.11]. Tantalum (Ta) has a work-function close to n^+ poly-Si. Tantalum nitride (TaN) is quite stable (to maintain thermal stability up to a 1000^{o}C RTA) because the activation energy of metal and nitrogen is relatively low. Tantalum is bonded tightly within nitride and no diffuse was observed in fabricated devices.

In conclusion, a systematic consideration of the required properties of gate dielectrics indicates that the key guidelines for selecting an alternative gate dielectric are (a) permittivity, band gap, and band alignment to silicon, (b) thermodynamic stability, (c) film morphology, (c) interface quality, (e) compatibility with the current or expected materials to be used in processing for CMOS devices, (f) process compatibility, and (g) reliability. Many dielectrics appear favorable in some of these areas, but very few materials are promising with respect to all of these guidelines. Fig. 1-3 summarizes the properties for high-κ candidates.

1.3 Hafnium-based dielectrics

Hafnium-based dielectrics, including HfO_2 [1.14]-[1.15], HfON [1.16]-[1.17], HfSiO [1.18], HfSiON [1.19], HfAlO, and HfAlON [1.20]-[1.22] have gained significant attention in recent years as a replacement for SiO_2 in complementary-metal-oxide semiconductor (CMOS) devices. Among them, HfO_2 is very promising for the next-generation gate dielectric of MOSFETs, because of its high dielectric constant, excellent thermal stability, wide band gap, and large band offsets. However, the high oxygen and impurities penetration and boron diffusion into the gate dielectric should be suppressed to maintain low equivalent oxide thickness (EOT), reduce flatband voltage fluctuation; and further it demonstrated a well crystallized structure after annealing at low temperature around 500℃ [1.23].

Several studies have focused on the improvement of the thermal stability of high-κ gate dielectric to overcome the insufficient immunity to oxygen or impurity diffusion during the subsequent thermal process. Those studies incorporated Al, Si, and N into Hafnium oxide to form HfON, HfSiO, HfSiON, HfAlO, and HfAlON respectively. Among them, HfSiON, hafnium silicon oxynitride which was found to improve thermal stability further compared to HfON. However, dielectric constants are reduced in HfSiON due to the presence of silicon oxide bonds with much lower dielectric constant than HfO_2. HfSiON with optimized composition remained amorphous state up to 1100 ^{0}C whereas dielectric constant decreased down to ~10. In terms of application, the HfSiON appears to be very promising materials for

the low power devices rather than high speed device requiring further scaling-down of EOTs <10Å in the near future. In conclusion, the addition of Al and Si has been known to retard crystallization of HfO_2, but the dielectric constant is degraded as the Al or Si content increases [1.23]-[1.31].

$Hf_{1-x-y}N_xO_y$ appears to be promising for further scaling-down of EOT since incorporated nitrogen does not degrade dielectric constant of the film. $Hf_{1-x-y}N_xO_y$ showed a lower leakage current than HfO_2. Fig. 1-4 shows the leakage current of Hafnium oxynitride with different N_2 flow rate conditions as depositing. It shows $Hf_{1-x-y}N_xO_y$ for N_2 flow rate at 50% almost 2 order lower leakage current than HfO_2 at -2V. The lower leakage current of $Hf_{1-x-y}N_xO_y$ can be attributed to its thicker physical thickness to achieve a given EOT due to the higher dielectric constants of bulk and interface layer compared to HfO_2. (Dielectric constant of bulk for HfO_2 and $Hf_{1-x-y}N_xO_y$ are 19 and 22, and the dielectric constant of interfacial layer in $Hf_{1-x-y}N_xO_y$ ~14 is larger than that of HfO_2 ~7.8) [1.23]-[1.31].

Nitrided films show improved thermal stability, inhibited crystallization, improved electrical and dielectric properties, and decreased dopant, oxygen, and silicon interlayer diffusion when compared to hafnium silicates. It was due to the atomic [N] could passivate [O] vacancies in the gate dielectrics during nitridation process and remove electron leakage path mediated by [O] vacancies. Thin film XRD with a glancing angle of 3^0 was used to investigate crystalline of HfO_2 and $Hf_{1-x-y}N_xO_y$ on Si substrates. Fig.1-5 depicts XRD spectra

of HfO_2 and $Hf_{1-x-y}N_xO_y$ films which were annealed under N for 1 min at various temperatures ranging from500℃ to 950℃. $Hf_{1-x-y}N_xO_y$ showed an increase of 300℃ in crystallization temperature compared to HfO_2. It was due to Hf-N bond has higher thermal stability than Hf-O bond. Although, recent reports have indicated that the nitrogen introduces energy levels in the band gap of HfO_2, thereby reducing the valence-band offset of the dielectric on silicon. It concludes that both band gap and band offset of hafnium oxynitrides are reduced by a fixed amount regardless of nitrogen concentration. However, these offsets result in barrier heights that are still sufficient to make $Hf_{1-x-y}N_xO_y$ a viable high-κ for gate dielectric applications while taking advantage of the improved physical and electrical properties [1.23]-[1.31].

Although $Hf_{1-x-y}N_xO_y$ crystallizes around ~800^oC not high enough to remain amorphous phase in the conventional self-aligned source/drain process, and reduce the band offset ,but it provide higher scalability than HfSiON due to its higher dielectric constant ~22.Therefore, it is worth further studying on the electrical and material characterization of $Hf_{1-x-y}N_xO_y$ film [1.23]-[1.31].

1.4 Scotty Emission and Pool-Frenkel Emission

Schottky Barrier:

The ideal energy band diagram for a particular metal and n-type semiconductor before making contact is shown in Fig.1-6. The vacuum level is used as a reference level. The parameter ϕ_m is the metal work function (measured in volts), ϕ_s is the semiconductor work function, and χ is known as the electron affinity. Now, we have assumed that $\phi_m > \phi_s$. The ideal thermal-equilibrium metal-semiconductor energy-band diagram can be observed, for this situation. Before contact, the Fermi level to become a constant through the system in thermal equilibrium, electrons from the semiconductor flow into the lower energy states in the metal. Positively charged donor atoms remain in the semiconductor, creating a space charge region.

The parameter ϕ_{B0} is the ideal barrier height of the semiconductor contact, the potential barrier seen by electrons in the metal trying to move into the semiconductor. This barrier is known as the *Schottky barrier* and is given, ideally by

$$\phi_{B0} = (\phi_m - \chi) \tag{1.1}$$

On the semiconductor side, V_{bi} is the built-in potential barrier, similar to the case of the pn junction, is the barrier seen by electrons in the conduction band trying to move into the metal. The built-in potential barrier is given by

$$V_{bi} = \phi_{B0} - \phi_n \tag{1.2}$$

which makes V_{bi} a slight function of the semiconductor doping, as was the case in a pn junction. Fig. 1-6 shows Schottky barrier formed by contacting an n-type semiconductor with a metal having a larger work function and Fig. 1-7 shows Schottky barrier between a p-type semiconductor and a metal having a smaller work function [1.36].

If we apply a positive voltage to the semiconductor with respect to the metal, the semiconductor-to-barrier height increases, while ϕ_{B0} remains constant in this idealized case. This bias condition is the reverse bias. If a positive voltage is applied to the metal with respect to the semiconductor, the semiconductor-to-metal barrier V_{bi} is reduced while ϕ_{B0} again remains essentially constant. In this situation, electrons can more easily flow from the semiconductor into the metal since the barrier has been reduced. This bias condition is the forward bias. We expect the current-voltage characteristics of the Schottky barrier junction to be similar to the exponential behavior of the pn junction diode. The current mechanism here, however, is due to the flow of majority carrier electrons. In forward bias, the barrier seen by the electrons in the semiconductor is reduced, so majority carrier electrons flow more easily from the semiconductor into the metal. The forward-bias current is in the direction from metal to semiconductor; it is an exponential function of the forward-bias voltage [1.32] .

Schottky Effect:

The *Schottky effect* or *image force induced barrier lowering effect* is due to an electron in a dielectric at a distance x from the metal will create an electric field. The field lines must be perpendicular to the metal surface and will be the same as if an image charge $+e$ is located at the same distance from the metal surface, but inside the metal. This image effects is shown in Fig. 1-8. The force on the electron due to the coulomb attraction with the image charge is

$$F = \frac{-e^2}{4\pi\varepsilon_s (2x)^2} = -eE \tag{1.3}$$

The potential can then be found as

$$-\phi(x) = +\int_x^\infty E dx' = +\int_x^\infty \frac{e}{a\pi\varepsilon_s \cdot 4(x')^2} dx' = \frac{-e}{16\pi\varepsilon_x x} \tag{1.4}$$

Where x' is the integration variable and where we have assumed that the potential is zero at $x=\infty$.

The potential energy of the electron is $-e\phi(x)$; Fig.1-9 (a) is a plot of the potential energy assuming that no other electric fields exist. With an electric field present in the dielectric, the potential is modified and can be written as

$$-\phi(x)=\frac{-e}{16\pi\varepsilon_s x}-E_x \tag{1.5}$$

The potential energy of the electron, including the effect of a constant electric field, is plotted in Fig. 1-9(b). The peak potential barrier is now lowered. This lowering of the potential barrier is the Schottky effect, or image-force-induced lowering.

We can find the Schottky barrier lowering, $\Delta\phi$, and the position of the maximum barrier, x_m, from the condition that

$$\frac{d(e\phi(x))}{dx}=0 \tag{1.6}$$

We find that

$$x_m=\sqrt{\frac{e}{16\pi\varepsilon_s E}} \tag{1.7}$$

And

$$\Delta\phi=\sqrt{\frac{e}{4\pi\varepsilon_s}} \tag{1.8}$$

This is so called *Schottky effect* or *image force induced barrier lowering effect.* The actual

energy barrier to emission is $\phi_{ox} - \Delta\phi$ [1.32].

Schottky Emission:

The current transport in a metal-semiconductor junction is due to mainly to majority carries as opposed to minority carriers in a pn junction. The basic process in the rectifying contact with an n-type semiconductor is by transport of electrons over the potential barrier, which can be described by the thermionic emission theory [1.32].

The thermionic emission characteristics are derived by using the assumptions that the barrier height is much larger than κT, so that the Maxwell-Boltzmann approximation applies and that thermal equilibrium is not affected by this process. The current $J_{s\to m}$ is the electron current density due to the flow of electrons from semiconductor into the metal, and the current $J_{m\to s}$ is the electron current density due to the flow of electrons from the metal into the semiconductor. The subscripts of the currents indicate the direction of electron flow. The conventional current direction is opposite to electron flow.

The current density $J_{s\to m}$ is a function of the concentration of electrons which have x-directed velocities sufficient to overcome the barrier. We may write

$$J_{m\to s} = e\int_{E'}^{\infty} v_x dn \qquad (1.9)$$

Where E' is minimum energy required for thermionic emission into the metal, υ_x is the carrier velocity in the direction of transport, and e is the magnitude of the electronic charge.

The incremental electron concentration is given by

$$dn = g_c(E) f_F(E) dE \tag{1.10}$$

Where $g_c(E)$ is the density of states in the conduction band and $f_F(E)$ is the Fermi-Dirac probability function. Assuming that the Maxwell-Boltzmann approximation applies, we may write

$$dn = \frac{4\pi\left(2m_n^*\right)^{3/2}}{h^3}\sqrt{E - E_C}\exp\left[\frac{-(E - E_F)}{\kappa T}\right]dE \tag{1.11}$$

If all of the electron energy above E_c is assumed to be kinetic energy, then we have

$$\frac{1}{2}m_n^* v^2 = E - E_c \tag{1.12}$$

The net current density in the metal-to-semiconductor junction can be written as

$$J = J_{s\to m} - J_{m\to s} \tag{1.13}$$

which is defined to be positive in the direction from the metal to the semiconductor. We find that

$$J = \left[A^* T^2 \exp\left(\frac{-e\phi_{B0}}{\kappa T}\right)\right]\left[\exp\left(\frac{eV_a}{\kappa T}\right) - 1\right] \tag{1.14}$$

where

$$A^* \equiv \frac{4\pi e m_n^* k^2}{h^3} \tag{1.15}$$

$$= 120\left(\frac{m_{ox}^*}{m_0}\right) \tag{1.16}$$

The parameter A^* (A/cm^2K^2) is called the *effective Richardson constant* for thermionic

emission. We can although change the expression in another form

$$J_{SE} = A^* T^2 \exp\left[\frac{-q\left(\phi_{B0} - \sqrt{\frac{qE}{4\pi\varepsilon_r\varepsilon_0}}\right)}{\kappa T}\right] \qquad (1.17)$$

Pool-Frenkel Emission:

Pool-Frenkel effect is also possible conduction mechanism and in fact it is observed very often in all high-κ materials. This mechanism is appearing with field enhanced electron emission from Columbic centers, i.e. it is bulk-limited [1.33].

The Pool-Frenkel emission is due to field-enhanced thermal excitation of trapped electrons into the conduction band. For trap states with coulomb potentials, ignoring the effect of finite temperature and image-force-induced barrier lowering [1.34], the expression is virtually identical to that of the Schottky emission. The barrier height, however, is the depth of the trap potential well, and the quantity $\sqrt{\frac{q}{\pi\varepsilon_i}}$ is larger than in the case of Schottky emission by a factor of 2, since the barrier lowering is twice as large due to the immobility of the positive charge. Fig.1-10 illustrates the Pool-Frenkel emission.

$$J_{PF} = B^* E \exp\left[\frac{-q\left(\phi_t - \sqrt{\frac{qE}{\pi\varepsilon_r\varepsilon_0}}\right)}{kT}\right] \qquad (1.18)$$

where

$$B^* = qN_C u \tag{1.19}$$

ϕ_t is the energy level of trapping center.

Pool-Frenkel emission occurs more often than not while depositing oxide by PVD or CVD methods because of the more defects in the insulator [1.35].

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
	L_g: Physical L_{gate} for High Performance logic (nm) [1]	32	28	25	22	20	18	16	14	13
	EOT: Equivalent Oxide Thickness [2]									
IS	Extended planar bulk (Å)	12	11	11	10	9	6.5	5	5	
Delete	UTB FD (Å)				~~9~~	~~8~~	7	6	5	5
	DG (Å)							8	7	6
	Gate Poly Depletion and Inversion-Layer Thickness [3]									
IS	Extended Planar Bulk (Å)	7.3	7.4	7.4	7.0	7.0	2.7	2.5	2.5	
Delete	UTB FD (Å)				~~4~~	~~4~~	4	4	4	4
	DG (Å)							4	4	4
	EOT_{elec}: Electrical Equivalent Oxide Thickness in inversion [4]									
IS	Extended Planar Bulk (Å)	19.3	18.4	18.4	17.0	16.0	9.2	7.5	7.5	
Delete	UTB FD (Å)				~~13~~	~~12~~	11	10	9	9
	DG (Å)							12	11	10
	$J_{g,limit}$: Maximum gate leakage current density [5]									
IS	Extended Planar Bulk (A/cm^2)	1.88E+02	5.36E+02	8.00E+02	1.18E+03	1.10E+03	1.56E+03	2.00E+03	2.43E+03	
Delete	UTB FD (A/cm^2)				~~7.73E+02~~	~~9.50E+02~~	1.22E+03	1.38E+03	2.07E+03	2.23E+03
	DG (A/cm^2)							6.25E+02	7.86E+02	8.46E+02
	V_{dd}: Power Supply Voltage (V) [6]	1.1	1.1	1.1	1	1	1	1	0.9	0.9
	$V_{t,sat}$: Saturation Threshold Voltage [7]									
IS	Extended Planar Bulk (mV)	195	168	165	164	237	151	146	148	
Delete	UTB FD (mV)				~~169~~	~~168~~	167	170	166	167
	DG (mV)							181	184	185
	$I_{sd,leak}$: Source/Drain Subthreshold Off-State Leakage Current [8]									
IS	Extended Planar Bulk (µA/µm)	0.06	0.15	0.2	0.26	0.22	0.28	0.32	0.34	
Delete	UTB FD (µA/µm)				~~0.17~~	~~0.19~~	0.22	0.22	0.29	0.29
	DG (µA/µm)							0.1	0.11	0.11
	$I_{d,sat}$: effective NMOS Drive Current [9]									
IS	Extended Planar Bulk (µA/µm)	1.02E+03	1.13E+03	1.20E+03	1.21E+03	1.18E+03	2.05E+03	2.49E+03	2.30E+03	
Delete	UTB FD (µA/µm)				~~1486~~	~~1625~~	1815	2015	2037	2198
	DG (µA/µm)							1899	1932	2220
	Mobility Enhancement Factor for $I_{d,sat}$ [10]									
	Extended Planar Bulk	1.09	1.09	1.08	1.09	1.1	1.1	1.12	1.11	
Delete	UTB FD				~~1.06~~	~~1.06~~	1.06	1.06	1.05	1.05
	DG							1.05	1.04	1.05

Fig.1-1 The International Technology Roadmap for semiconductor 2006.

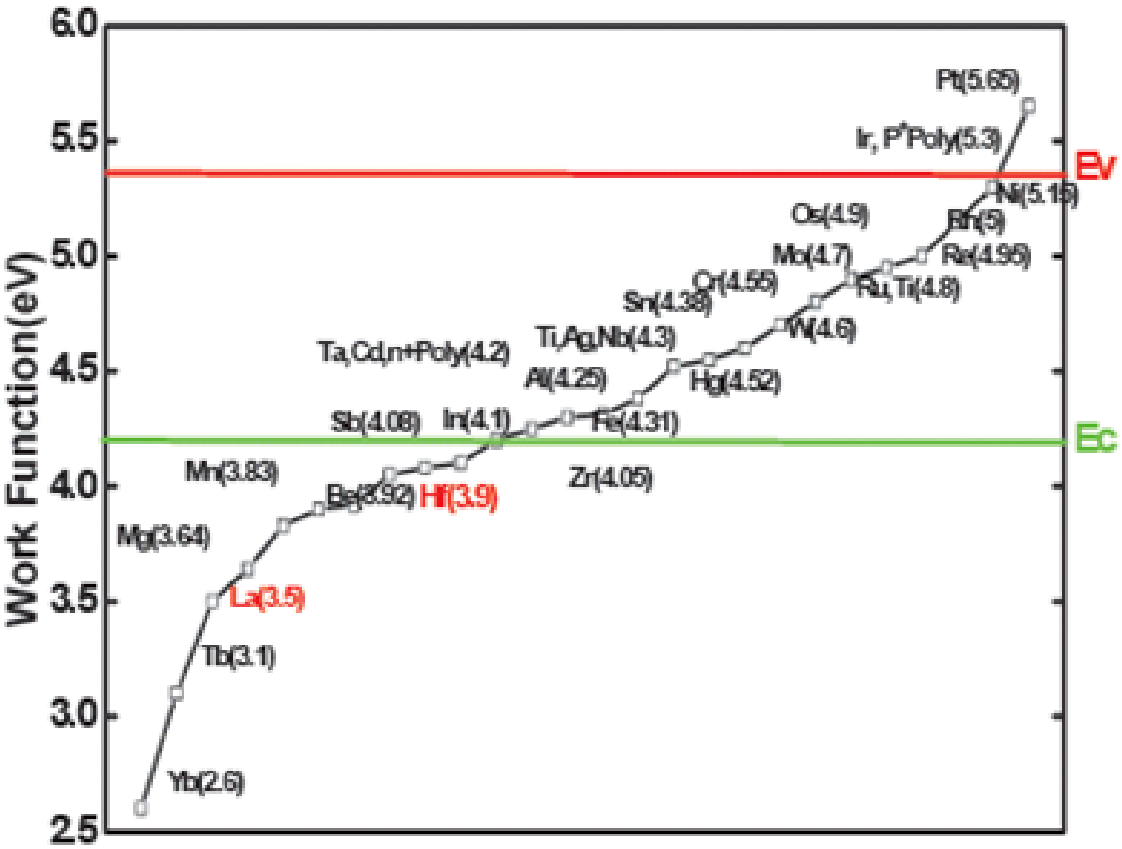


Fig.1-2 The values of work function for different metal materials.

Material	Dielectric constant (κ)	Band gap E_G (eV)	ΔE_C (eV) to Si	Crystal structure(s)
SiO_2	3.9	8.9	3.2	Amorphous
Si_3N_4	7	5.1	2	Amorphous
Al_2O_3	9	8.7	2.8[a]	Amorphous
Y_2O_3	15	5.6	2.3[a]	Cubic
La_2O_3	30	4.3	2.3[a]	Hexagonal, cubic
Ta_2O_5	26	4.5	1–1.5	Orthorhombic
TiO_2	80	3.5	1.2	Tetrag.[c] (rutile, anatase)
HfO_2	25	5.7	1.5[a]	Mono.[b], tetrag.[c], cubic
ZrO_2	25	7.8	1.4[a]	Mono.[b], tetrag.[c], cubic

Fig.1-3 Comparison of relevant properties for high-κ candidates.

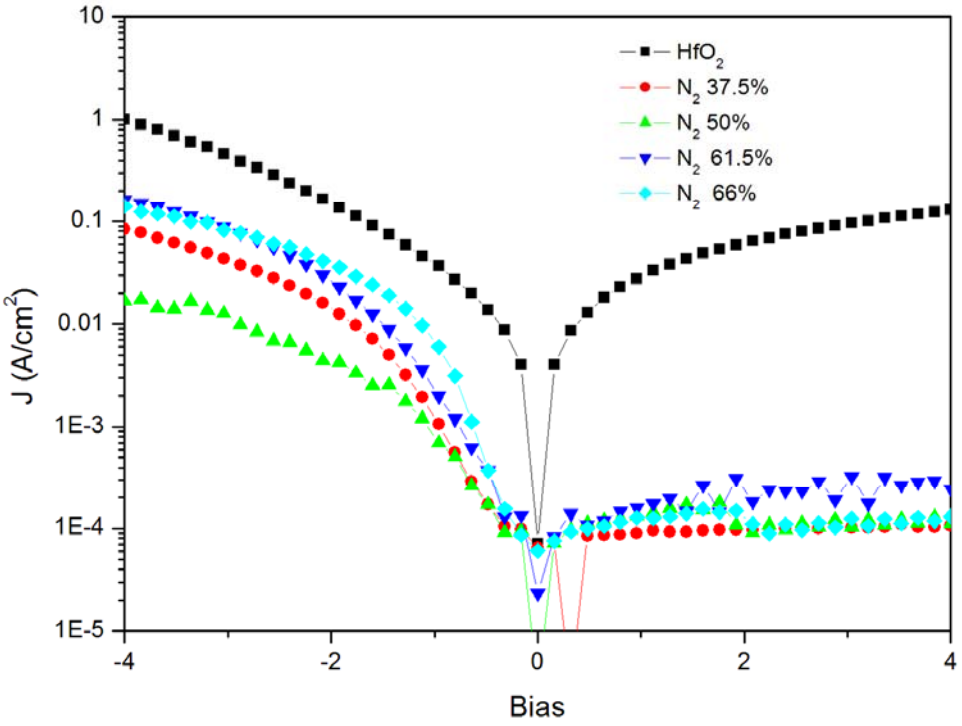


Fig.1-4 The leakage current of Hafnium oxynitride with different N_2 flow rate conditions as depositing.

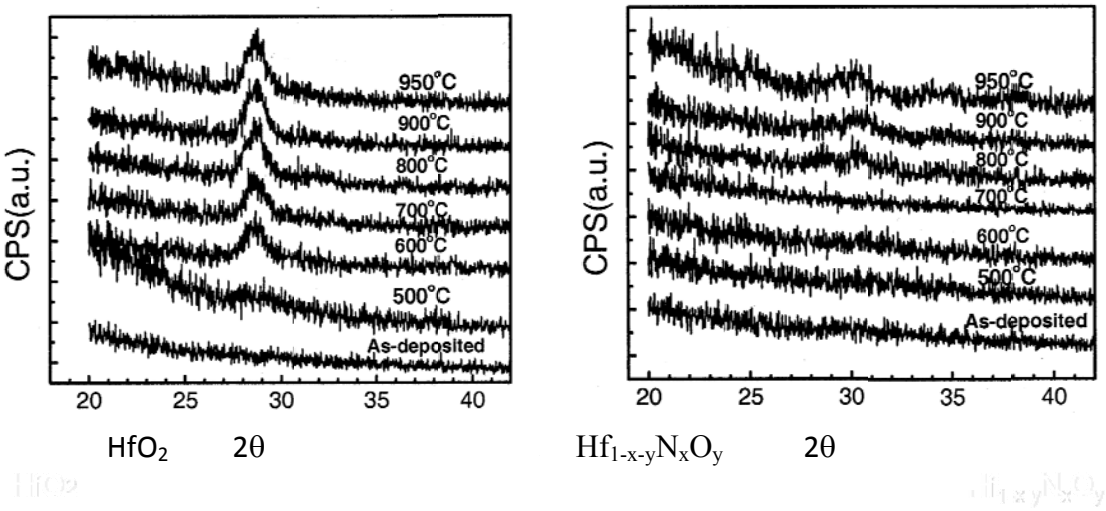
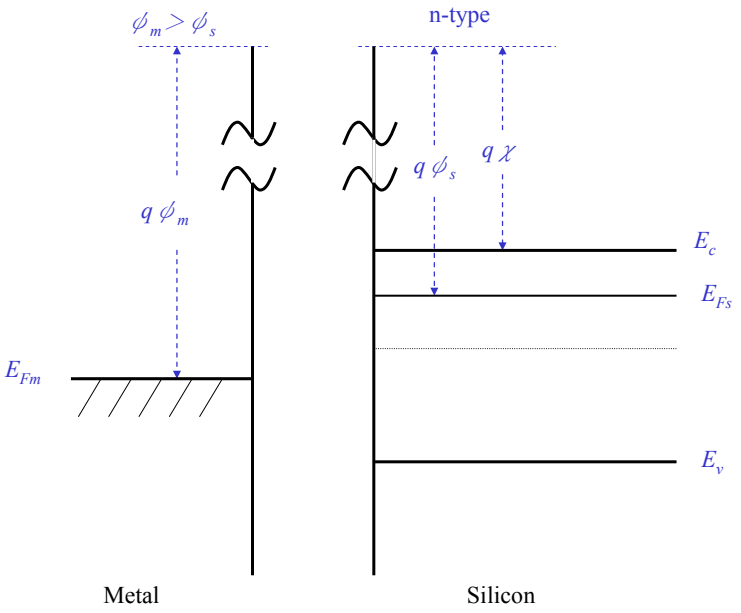
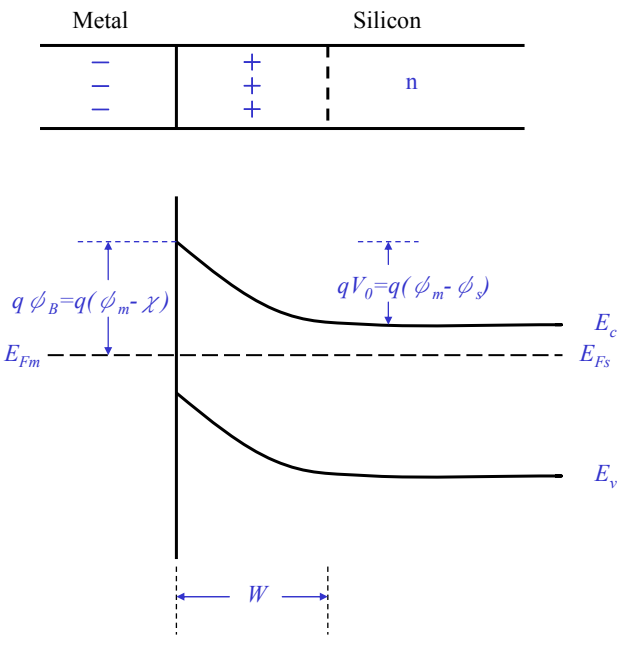


Fig.1-5 Thin film XRD spectra with a glancing angle of 3^0 as a function of PDA temperature for HfO_2 and $Hf_{1-x-y}N_xO_y$ films on Si substrates[1.23].

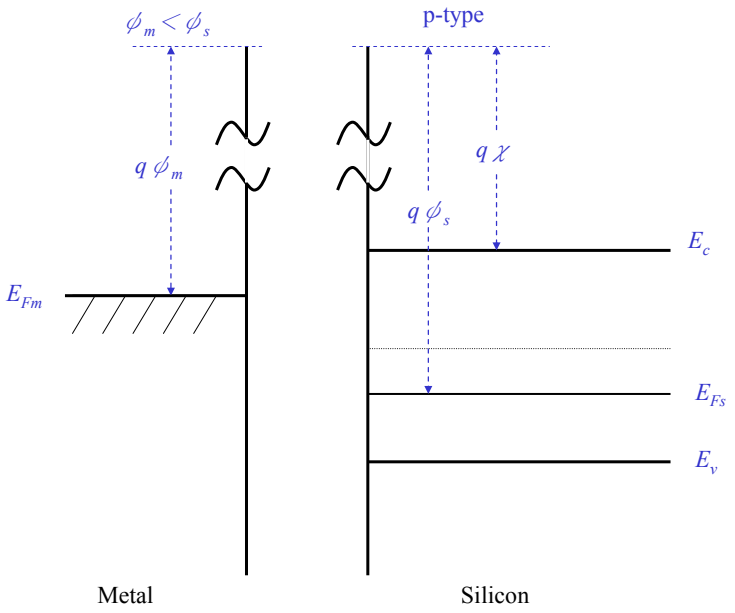


(a)

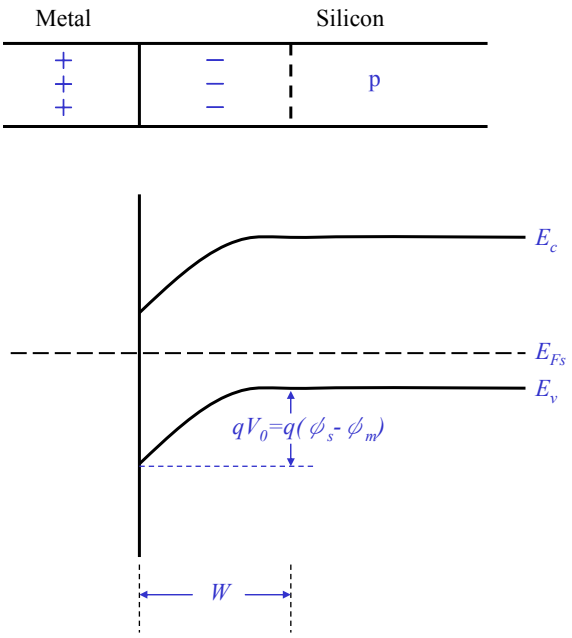


(b)

Fig.1-6 A Schottky barrier formed by contacting an n-type semiconductor with a metal having a larger work function: (a) band diagrams for the metal and the semiconductor before joining; (b) equilibrium band diagram for the junction.



(a)



(b)

Fig.1-7 Schottky barrier between a p-type semiconductor and a metal having a smaller work function: (a) band diagram before joining; (b) band diagram for the junction at equilibrium.

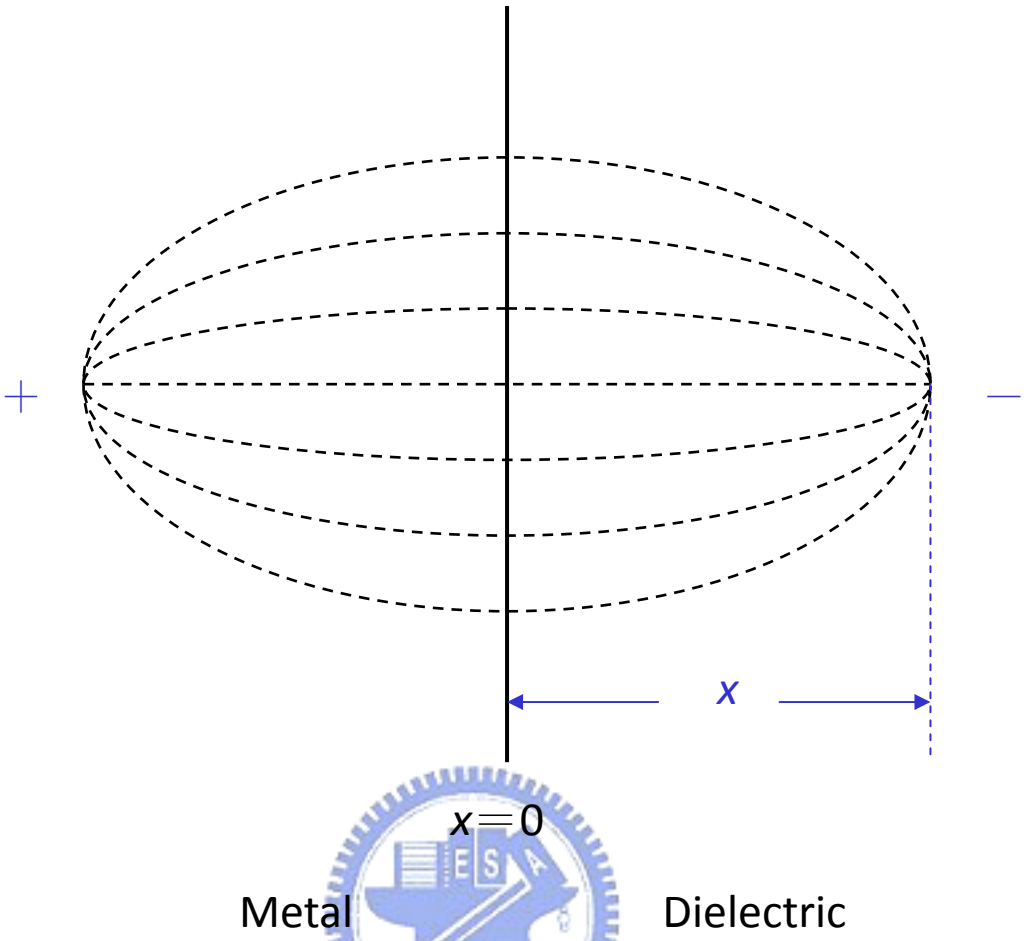
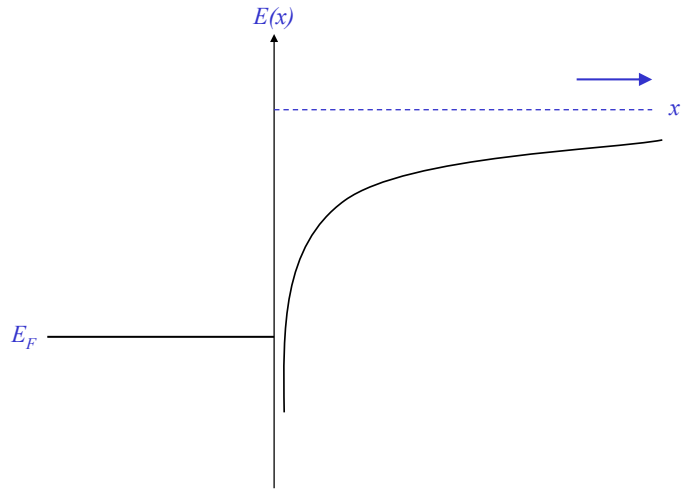
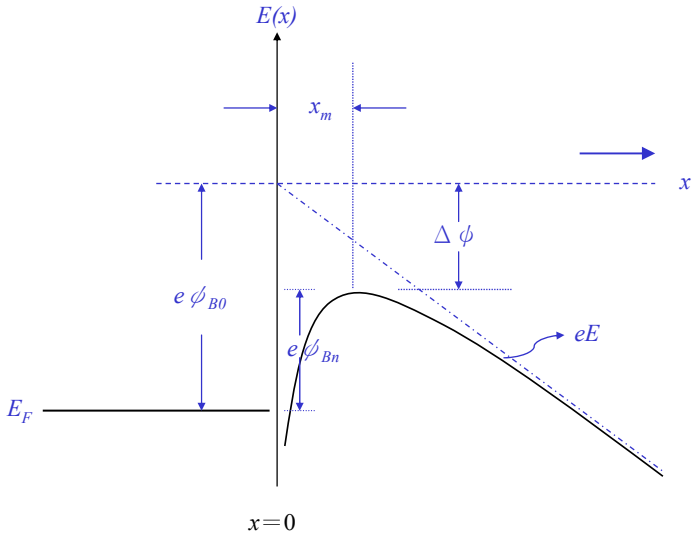


Fig.1-8 Image charge and electric field lines at a metal-dielectric interface



(a)



(b)

Fig.1-9 (a) Distortion of the potential barrier due to image forces with zero electric field; (b) with a constant electric field.

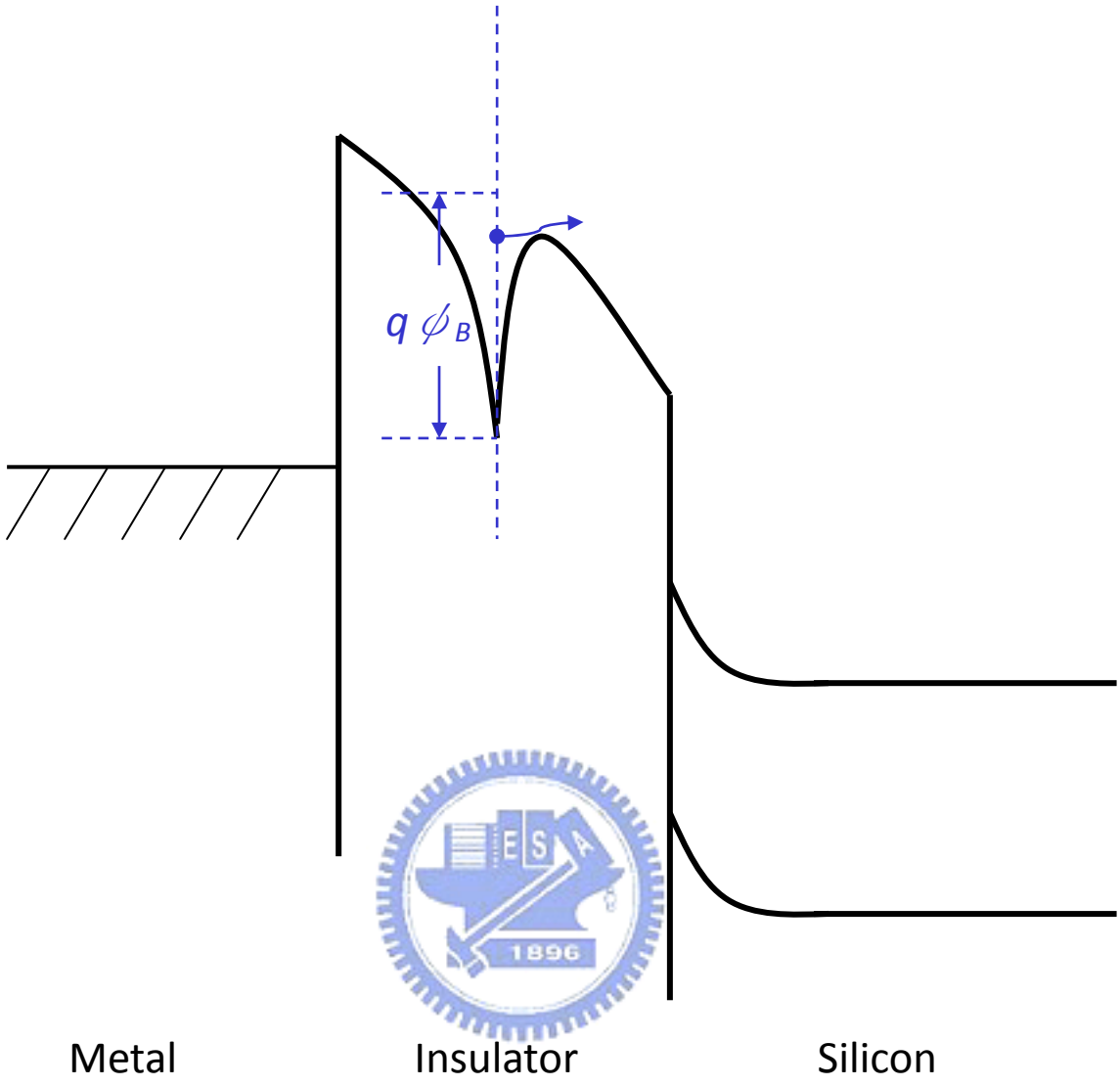


Fig.1-10 Pool -Frenkel emission from trapped electrons.

Chapter 2

The Experimental Steps and Measurement

2.1 Fabrication of MIS capacitors

The MIS capacitor used a standard 4-in P-type silicon wafer (100) as the substrate, and following RCA clean processes. Fig. 2-1 shows the steps of RCA clean in detail. After standard pre-gate clean, an 30nm $Hf_{1-x-y}N_xO_y$ dielectric was deposited with high N_2 flows by DC sputtering of Hf target in Ar + N_2 +O_2 mixed gas ambient at a sputtering power of 150W. The total gas pressure was kept as 7.6 mTorr during the sputtering process. The dielectric was then Post Deposition Anneal (PDA) at 650℃ for 30s under N_2 ambient to reduce defects. A TaN layer was deposited by PVD and then gate patterned by photo lithography to form top electrode with capacitor area of 100μm × 100 μm. Finally, TaN/ $Hf_{1-x-y}N_xO_y$/silicon stacked metal-insulator-silicon (MIS) capacitors were fabricated. The processes of MIS capacitors is shown in Fig. 2-2 ~ Fig. 2-10. For comparison, we also fabricated Al_2O_3 and Si_3N_4 capacitors.

2.2 The measurement of MIS capacitors

To investigate the electrical characteristics of devices, we measured the *Ig-Vg* curves for gate leakage current by using HP 4156C semiconductor parameter analyzer. Besides, HP4284A precision LCR meter was used to evaluate the gate capacitance and the conductance ranging from 100 kHz to 1 MHz. For memory measurement, the fabricated MIS devices were characterized by program and erase measurements, as well as retention tests at 25℃ and 100℃ using an HP4156C Semiconductor Parameter Analyzer and HP8110A 150 MHz Pulse Pattern Generator.

A. DI water rinse, 5 min.
B. H_2SO_4 : H_2O_2 = 3:1, (10 min, 75~85℃)
C. DI water rinse, 5 min.
D. HF : H_2O = 1:100
E. DI water rinse, 5 min.
F. NH_4OH : H_2O_2 : H_2O = 1:4:20 (SC1), (10 min,75~85℃)
G. DI water rinse, 5 min.
H. HCl : H_2O_2: H_2O = 1:1:6 (SC2), (10min, 75~85℃)
I. DI water rinse, 5 min.
J. HF : H_2O = 1:100
K. DI water rinse.
L. Spinner

Fig.2-1 The RCA clean steps.

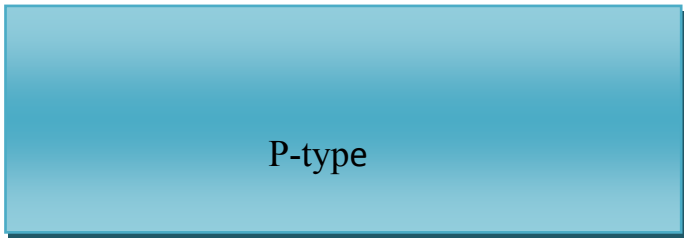


Fig.2-2 Silicon substrate.

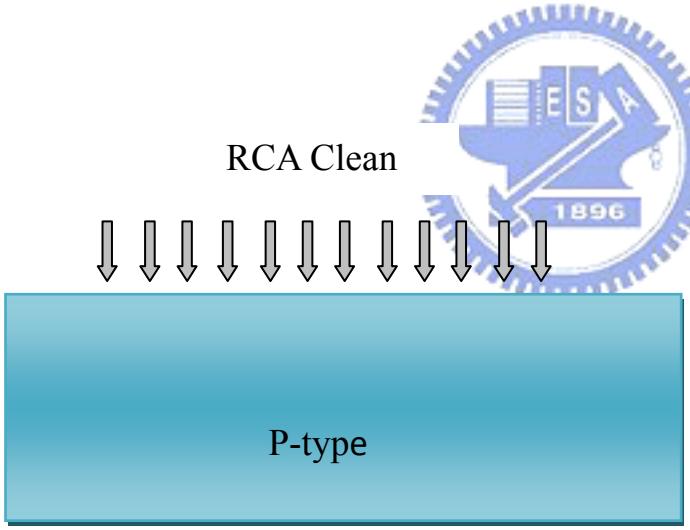


Fig.2-3 RCA Clean.

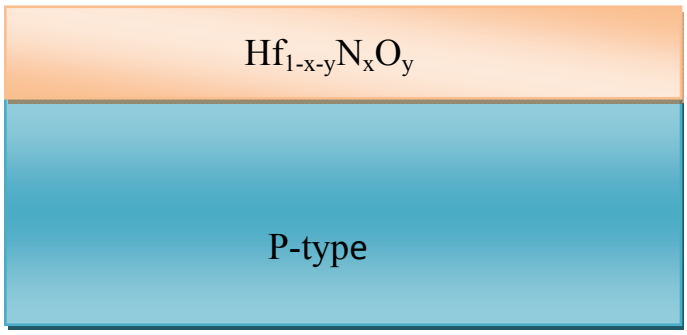


Fig.2-4 Deposited $Hf_{1-x-y}N_xO_y$ dielectric.

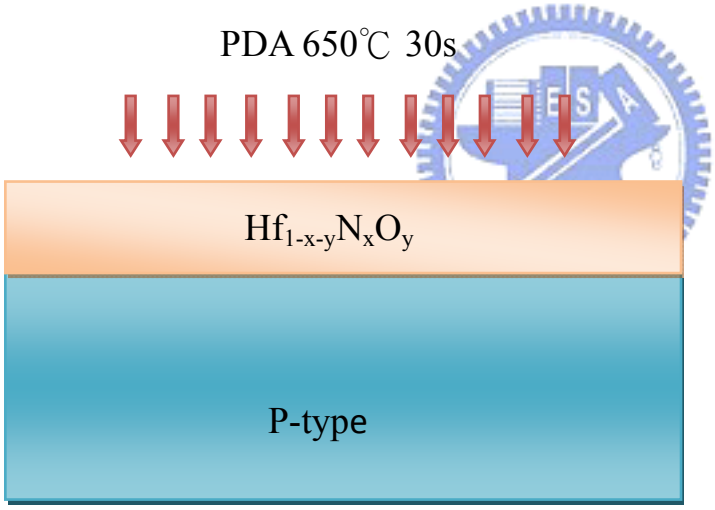


Fig.2-5 Post Deposition Annealing.

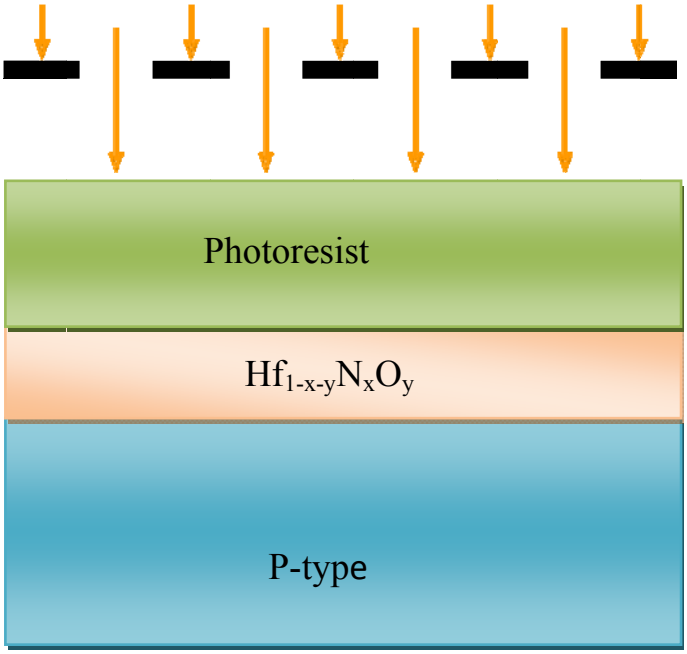


Fig.2-6 Photoresist and Lithography.

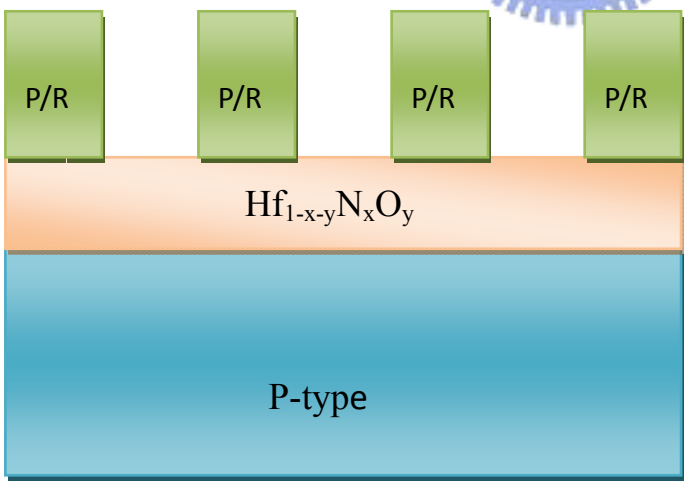


Fig.2-7 Lithography Patterned.

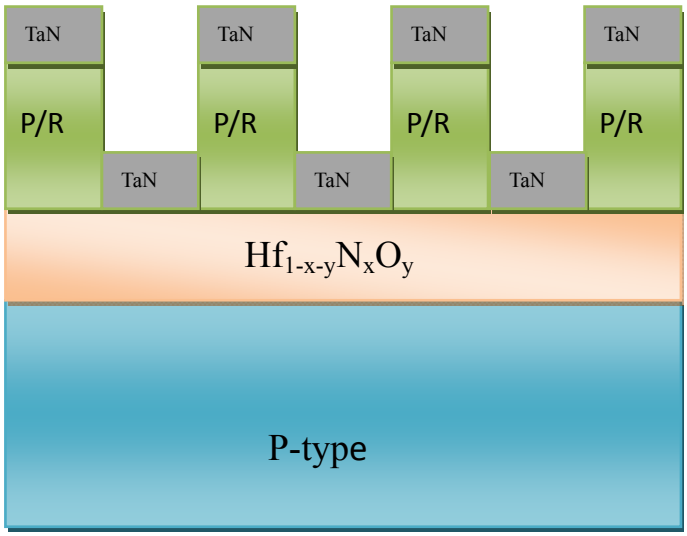


Fig.2-8 Deposited TaN by PVD.

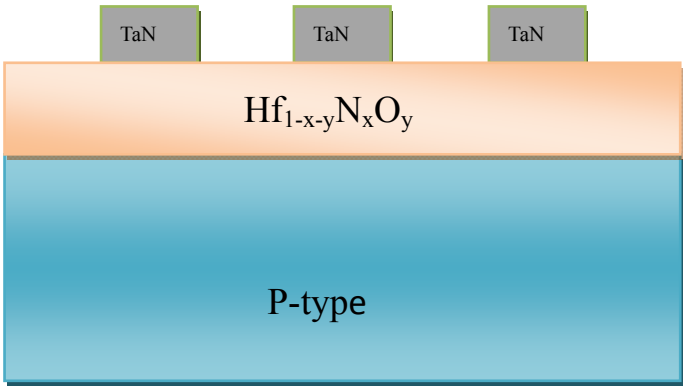


Fig.2-9 Fabricated MIS capacitors.

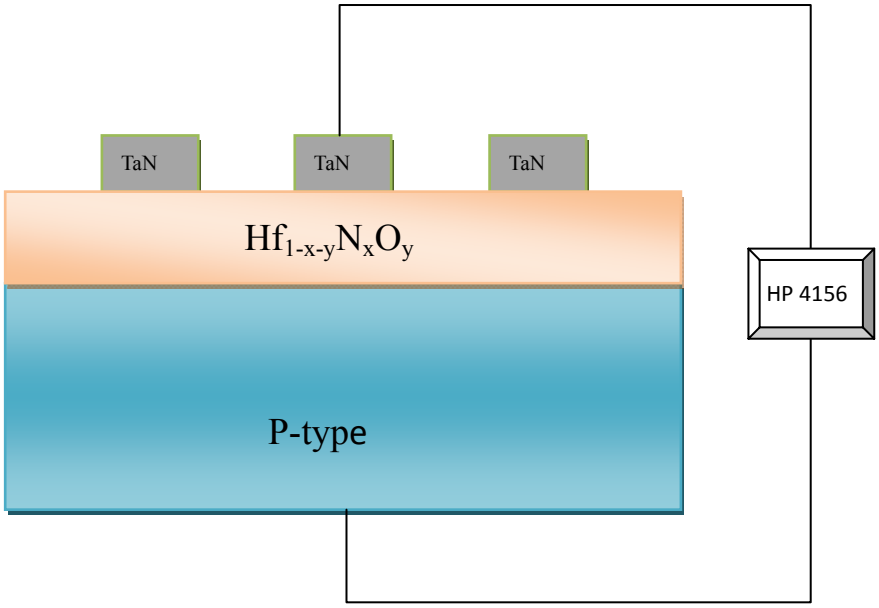


Fig.2-10 *IV* and *CV* measurement.

Chapter 3

Result and Discussion

3.1 Memory characteristics of Hafnium oxynitride capacitors

We first determined the N composition in the $Hf_{1-x-y}N_xO_y$. Fig. 3-1 shows the XPS spectra of $Hf_{1-x-y}N_xO_y$. The existence of Hf, N and O are clear in the XPS spectra, where the composition was determined to be $Hf_3N_2O_5$. Fig. 3-2 shows the measured *C-V* characteristics of a high-κ $Hf_3N_2O_5$ MIS capacitor. We found a large *C-V* hysteresis of 1.9 to 2.4 V as the sweep voltage was increased from ±3 to ±5 V. This suggests that the charge trapping characteristics of the $Hf_3N_2O_5$ dielectric are better than those reported for AlN [3.5], and it is likely due to a higher trap density and/or a deeper energy of those traps.

Fig. 3-3 shows the characteristics of a high-κ $Hf_3N_2O_5$ capacitor after applying +5 or -5V voltage for 0.1 to 100ms. The positive or negative shift of the threshold voltage (V_{th}), corresponding to a +5 or -5V applied voltage, indicates that the device can be programmed or erased, respectively. These phenomena are similar to non-volatile Flash or SONOS memory[3.1]-[3.4]. The devices showed a capacitance density of 6.5 fF/μm^2, which indicate a κ value of ~22 for the $Hf_3N_2O_5$. The high capacitor density is important for backend capacitor due to the very thick equivalent oxide thickness (EOT). The capacitor density of

TaN/$Hf_3N_2O_5$/Si device is also higher than those SONOS capacitors [3.2]-[3.4]. Fig. 3-4 displays the V_{th} shift as a function of the program/erase time. The $|V_{th}|$ increases with P/E time, as does ΔV_{th} with increasing P/E voltage. This suggests that the V_{th} shift mechanism is caused by charge trapping and indicated the good charge storage. We found a switching speed of ~ 1 ms, due to the rapid increase of V_{th} between 0.1 to 1 ms and the approximate saturation for times from 1 to 100 ms. From the V_{th} shift for P/E conditions of ± 5 V for 1ms, a memory window of 1.5 V was measured which is larger than that of an AlN device [3.5] and is comparable with certain SONOS NVM [3.6] data. In addition, the feature of nearly symmetrical positive and negative V_{th} for program and erase function is important for low voltage applications.

For comparison, we also measured the C-V characteristics of high-κ Si_3N_4 and Al_2O_3 capacitors, shown in Fig. 3-5 and Fig. 3-6. For Si_3N_4 capacitor, only a few mV V_{th} shift is shown after applying voltages of ± 4 V, which suggests shallower trap energy or lower trap density in the Si_3N_4. The larger hysteresis of C-V curve indicates the stronger carrier trapping (high density and/or deeper energy of traps) in the $Hf_3N_2O_5$ device than that of Si_3N_4 capacitor. For Al_2O_3 capacitor, V_{th} increases continuously after applying a negative voltage as high as -8V. Therefore, no erase function is shown, even after applying a higher negative voltage close to device breakdown. It may be due to increasing trapping negative charges in the high-κ dielectrics. The V_{th} change of Al_2O_3 capacitors after applying +4V is similar to the

hysteresis found in high-κ dielectrics, which is due to dielectric traps. A higher trap density is needed to achieve a higher V_{th} change, and the C-V shift values are much larger than Si_3N_4. This result suggests a higher trap density inside the Al_2O_3 dielectrics compared with Si_3N_4. This is also the motivation to replace Si_3N_4 by Al_2O_3 in MONOS or SONOS memories [3.2] [3.3] [3.7].

Data retention is one of the most important characteristics for memory applications. Fig. 3-7 shows the retention characteristics of an $Hf_3N_2O_5$ MIS capacitor at 25 and 100^oC, measured after ± 5 V and 1 ms P/E, for periods from 1 to 10000 s. The data of an AlN MIS capacitor are included for comparison. The retention data indicates Program and Erase decay rates of only 2 and 6.2 mV/dec, at 25^oC. At 100^oC, the decay rates increased to 104 and 116 mV/dec. Such decay rates are still comparable with the 85^oC data of advanced SONOS or MONOS NVM [3.2] [3.6] devices. Moreover, the retention of this $Hf_3N_2O_5$ device is significantly better than that of an AlN MIS capacitor which had a closed memory window at 10000 s at 100^oC. Further improvement is required to extend the high temperature retention, although these results are already useful for DRAM improvement.

3.2 Energy barrier and trap energy level

In order to investigate the trap energy, we measured the *J-V* characteristics. Fig. 3-8 showing measured *J-V* curves from 25 to 85°C. The *J-V* characteristics fit theoretical models for Schottky emission (SE) at low electric field and Frankel-Pool (FP) conduction at high voltages [3.8]. The model expression is simply [3.8]:

$$J \propto \exp[(\gamma E^{1/2} - q\varphi_{b,t})/kT] , \qquad (3.1)$$

where φ_b or φ_t are the Schottky barrier of the metal-electrode/dielectric or the FP trap energy level in the dielectric, respectively. The slope γ can be expressed as:

$$\gamma = (q^3/\eta\pi\varepsilon_0\kappa_\infty) \qquad (3.2)$$

The constant η has a value 1 or 4 for the FP and SE cases respectively. In (3.2) ε_0 is the vacuum permittivity, and κ_∞ is the high-frequency dielectric constant (= n^2; n being the refractive index).

To extract the Schottky barrier φ_b, we have plotted the $ln(J/T^2)$-$E^{1/2}$ relation [3.8] in Fig. 3-9. A φ_b of 0.70 eV was obtained for the lower $Hf_3N_2O_5$/Si interface from a fit of eq. (3.1) to the measured $ln(J/T^2)$-$E^{1/2}$ data. This value is, coincidently, close to the 0.69 eV value extracted for the upper TaN/$Hf_3N_2O_5$ interface.

To extract the trap energy, we have plotted the *ln(J/E)-1/kT* relationship [3.8]in Fig. 3-10. This gives extracted trap energy of 1.05 eV for current injection from the lower $Hf_3N_2O_5$/Si interface. This value reduces to 1.01 eV for current injection from the top TaN/$Hf_3N_2O_5$

interface, as shown in Fig. 3-11. The slight energy difference may be due to the background moisture and pressure transients at the beginning of reactive sputtering which could result in slightly higher oxygen content in the HfNO.

In Fig. 3-12 we summarize the band diagram of the TaN/$Hf_3N_2O_5$/Si MIS structure. The barrier height of 0.7 eV is significantly less than that of HfO_2 due to the high content nitrogen in the HfNO [3.9]. It is important to notice that the trap energy of $Hf_3N_2O_5$ is 1.01~1.05 eV below the conduction band of $Hf_3N_2O_5$. Such a deep trap energy (within the Si forbidden gap) is vitally important for good data retention due to a lack of allowed states within the Si bandgap – this also explains the large *C-V* hysteresis shown in Fig. 3-2.

In conclusion, we have fabricated the TaN/$Hf_3N_2O_5$/Si MIS capacitors which displayed a high capacitance density of ~6.5 fF/μm^2 and a large *C-V* hysteresis necessary for charge storage. Measured *J-V* characteristics indicated a deep trapping level of 1.01~1.05 eV.

3.3 The applications of MIS capacitors

For analog and RF [3.10]–[3.15] ICs and memory applications, capacitors with a high capacitance density are preferred. It is also desirable to have a program-erasable capability. This is especially important for RF ICs where process variations can shift the resonance frequency of LC tank away from designed values, creating impedance mismatches and bandpass frequency differences [3.16]. In addition, the high-κ $Hf_3N_2O_5$ capacitor has the high capacitance density of ~6.5fF/μm^2. Such a high capacitance density is importance for analog and RF applications [3.17]-[3.20] to reduce the chip size. This capacitance density is 5~6 times larger than capacitors currently provided by IC foundries, and would yield a 5~6 times smaller capacitor area in the circuit of a die.

For one-transistor-one-capacitor (1T1C) volatile memory like DRAM, this high density (6.5fF/μm^2) $Hf_3N_2O_5$ capacitor can be programmed and erased with voltage of +5V and -5V for $\leqq$ 1m sec. The mechanism for this may be charge trapping or de-trapping in the high-trap-density $Hf_3N_2O_5$. The retention data decay rates were only 2 and 6.2 mV/dec of program and erase at 25^oC. This is already better than volatile DRAM. The charge loss in a DRAM capacitor is a serious issue, where high capacitance density and frequency refreshing is needed around each 1ms, but due to the limited availability of high-k dielectrics this becomes difficult as devices are scale down. As a result, program and erasable capacitors can extend the data retention for DRAM leading to less refreshing cycles.

The $Hf_3N_2O_5$ capacitor has the large *C-V* hysteresis of 1.9 to 2.4 V as the sweep voltage was increased from ±3 to ±5 V (shown in Fig. 3-2), which is similar to SONOS or MONOS memories. It is already larger than other dielectrics in flash memories due to its deep trapping level of 1.01~1.05 eV. Besides, it also has large dielectric constant κ ~22. So, it is suitable to use $Hf_3N_2O_5$ as trapping layer in SONOS or MONOS type flash memories.

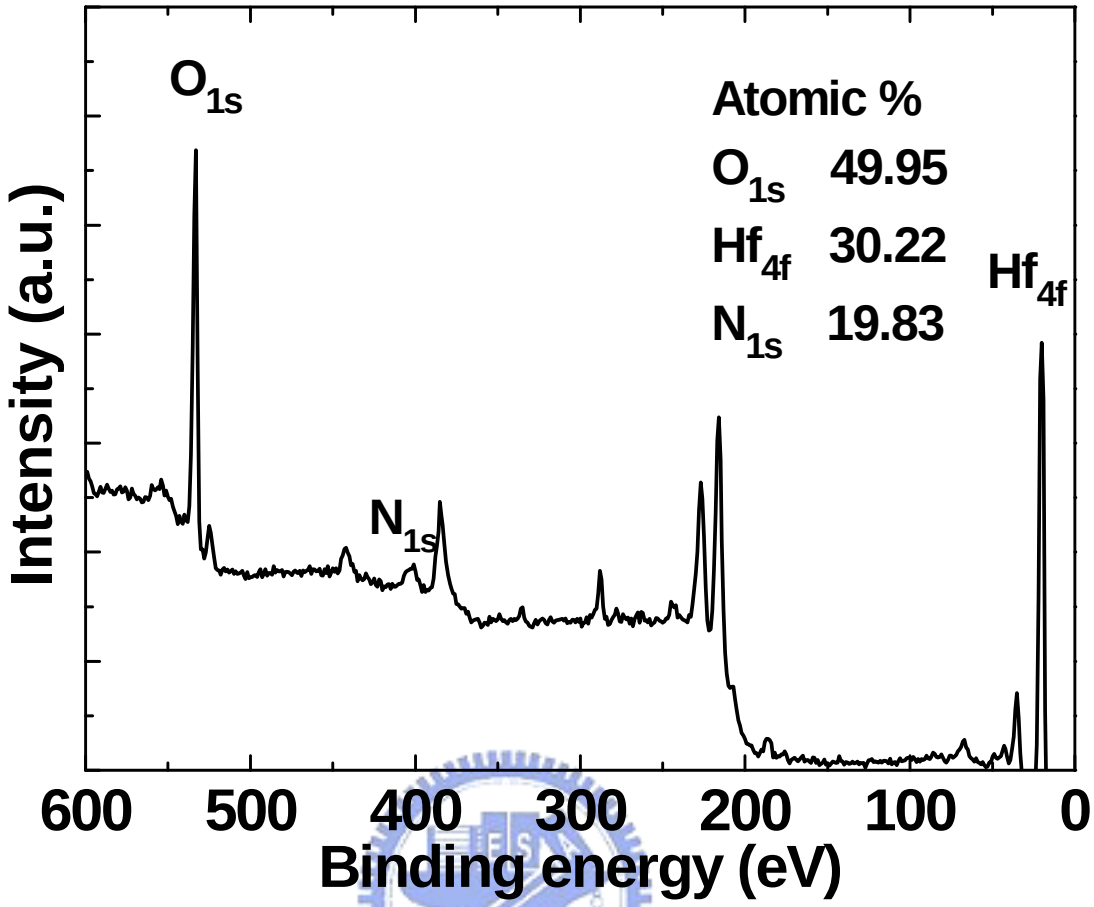


Fig. 3-1 XPS spectra of $Hf_{1-x-y}N_xO_y$, where composition of $Hf_3N_2O_5$ was determined from measurement.

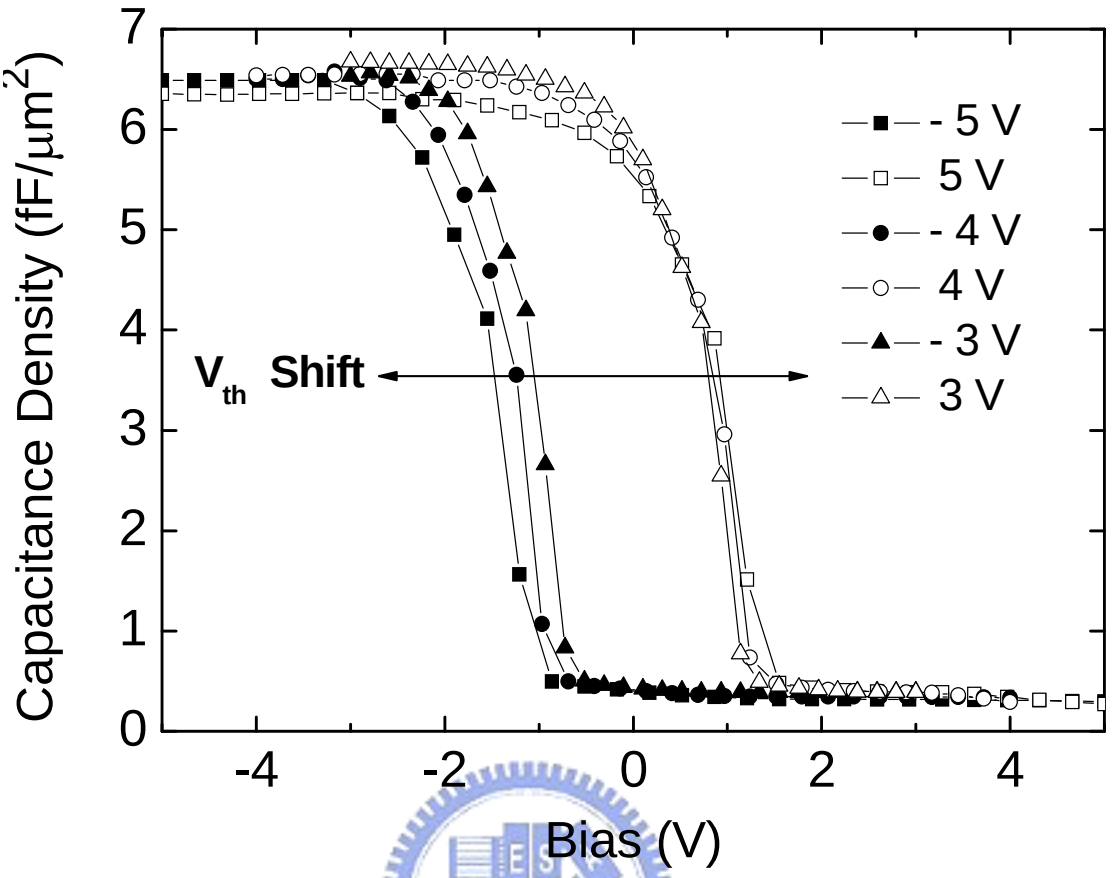


Fig. 3-2 The *C-V* characteristics of a TaN/$Hf_3N_2O_5$/Si MIS device which shows large hysteresis.

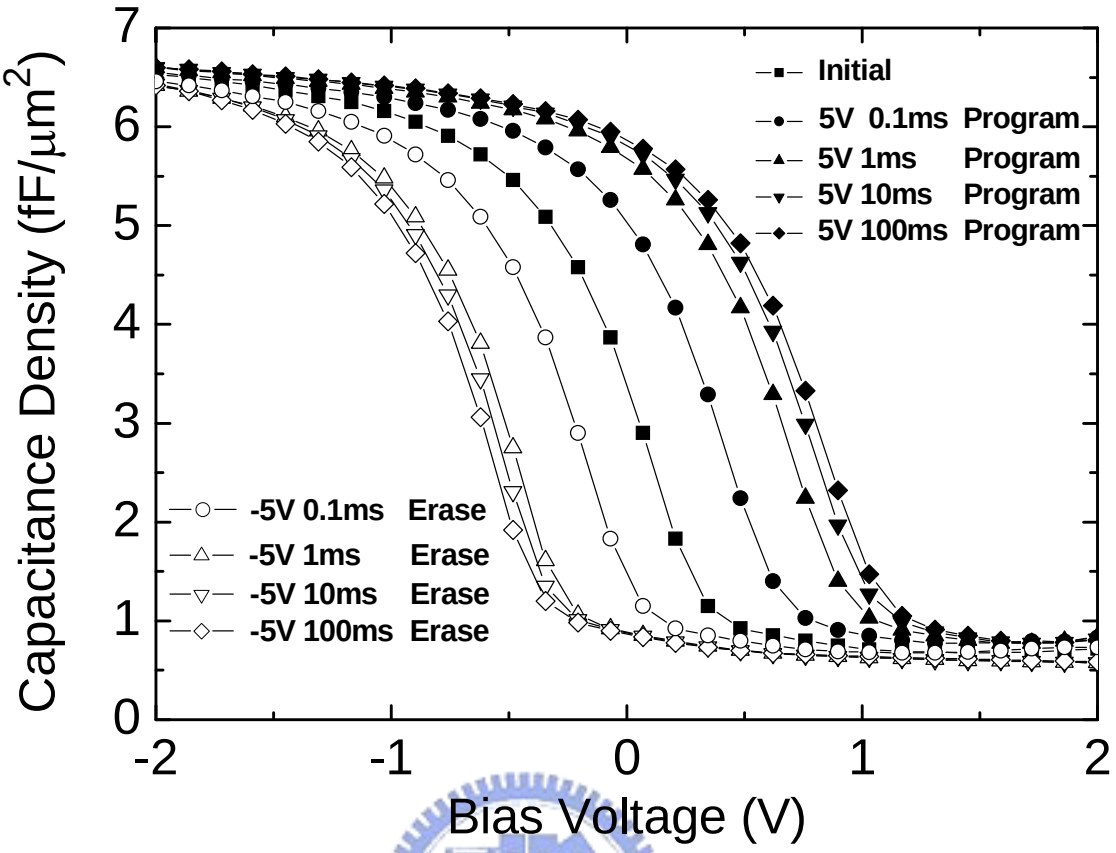


Fig. 3-3 The *C-V* characteristics of an $Hf_3N_2O_5$ MIS capacitor after applying a ± 5 V program/erase (P/E) voltage for various periods from 0.1 to 100 ms.

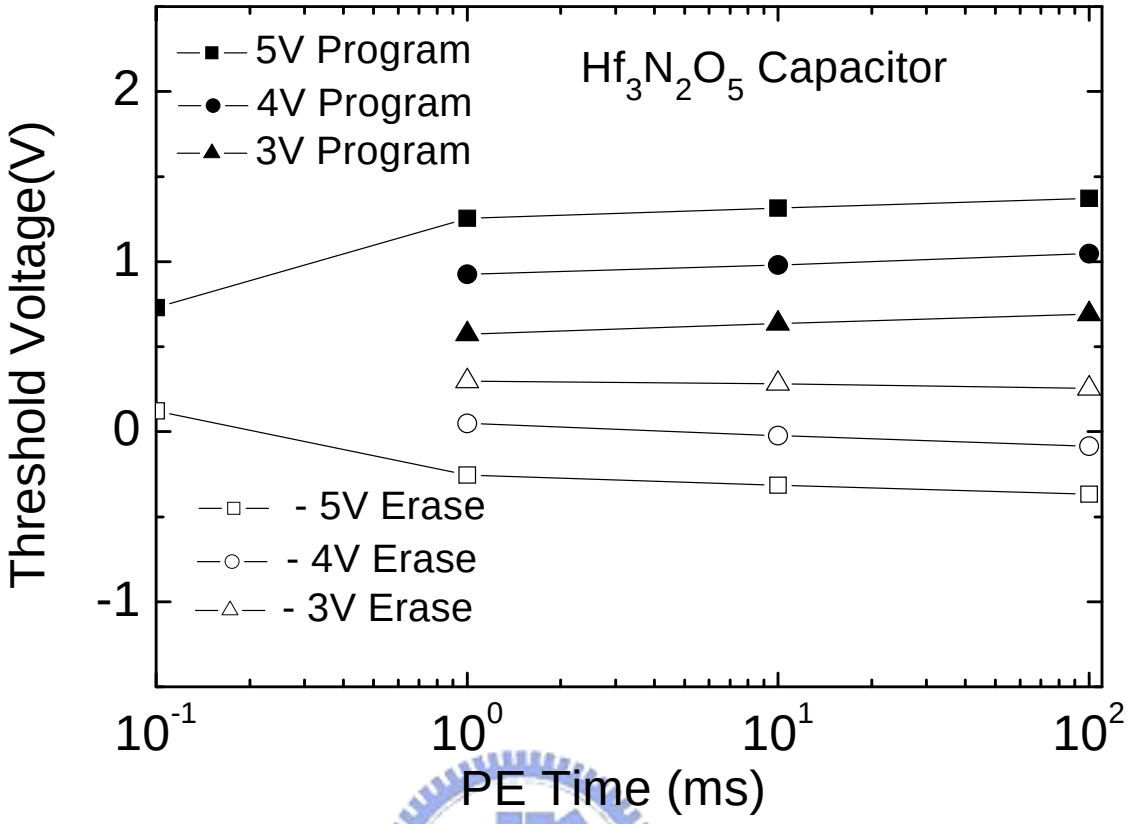


Fig. 3-4 The threshold voltage (V_{th}) for various P/E voltages from ± 3 to ± 5 V, as a function of the P/E time.

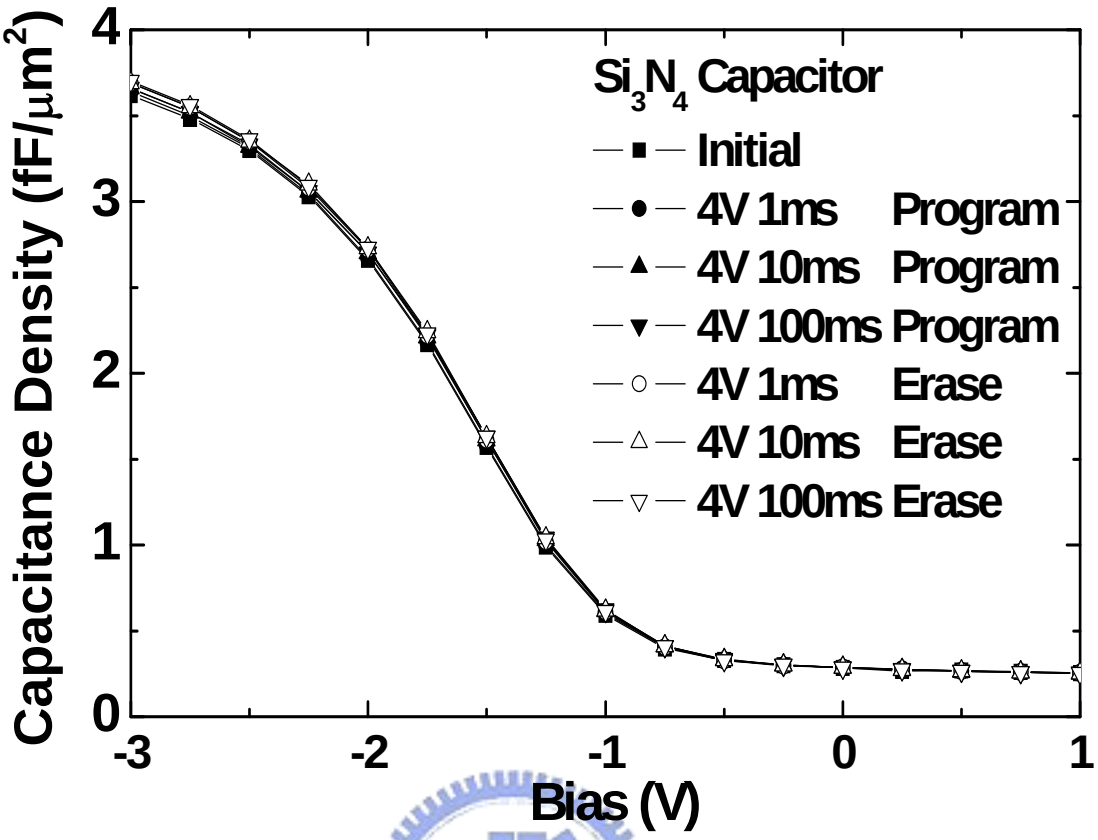


Fig. 3-5 C-V characteristics of a high-κ Si_3N_4 capacitor. A small C-V shift was shown after applying of +4V and -4V.

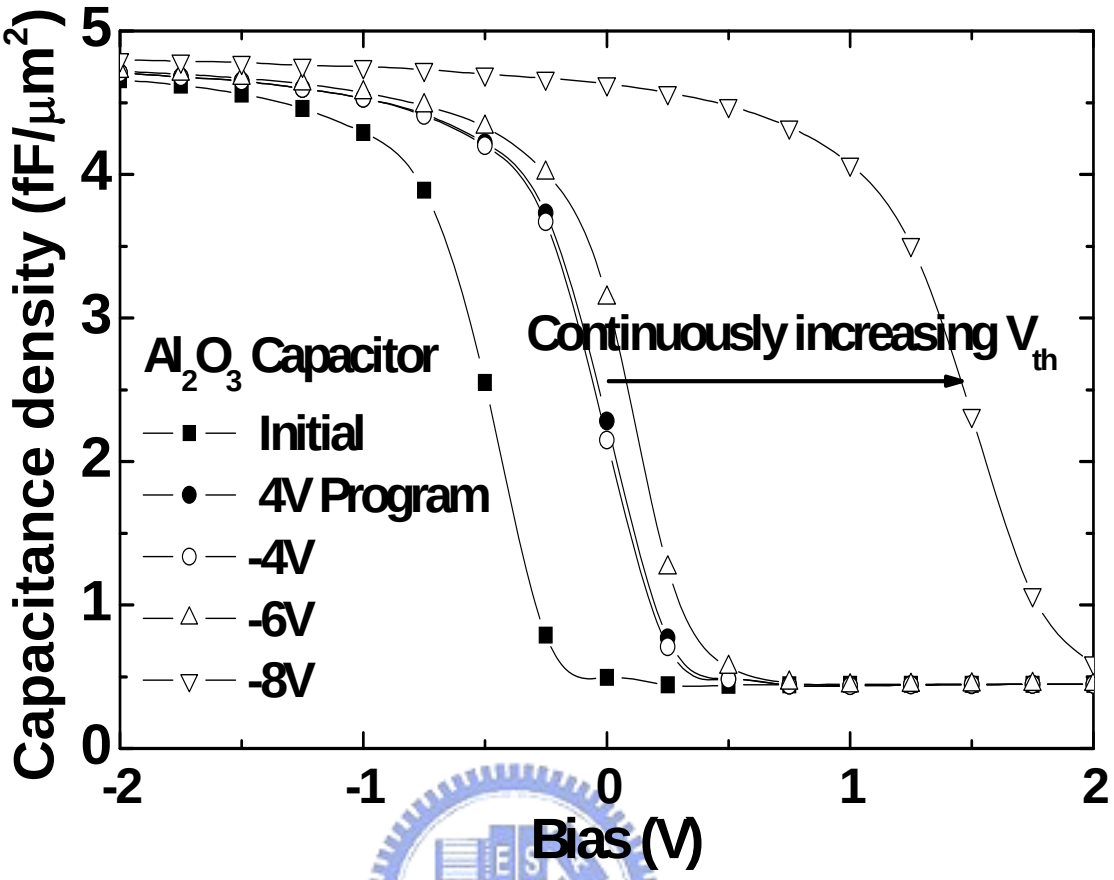


Fig. 3-6 Measured C-V characteristics of a high-κ Al_2O_3 capacitor. Continuously increasing V_{th} is measured even at high negative voltage of -8V but still without erase function.

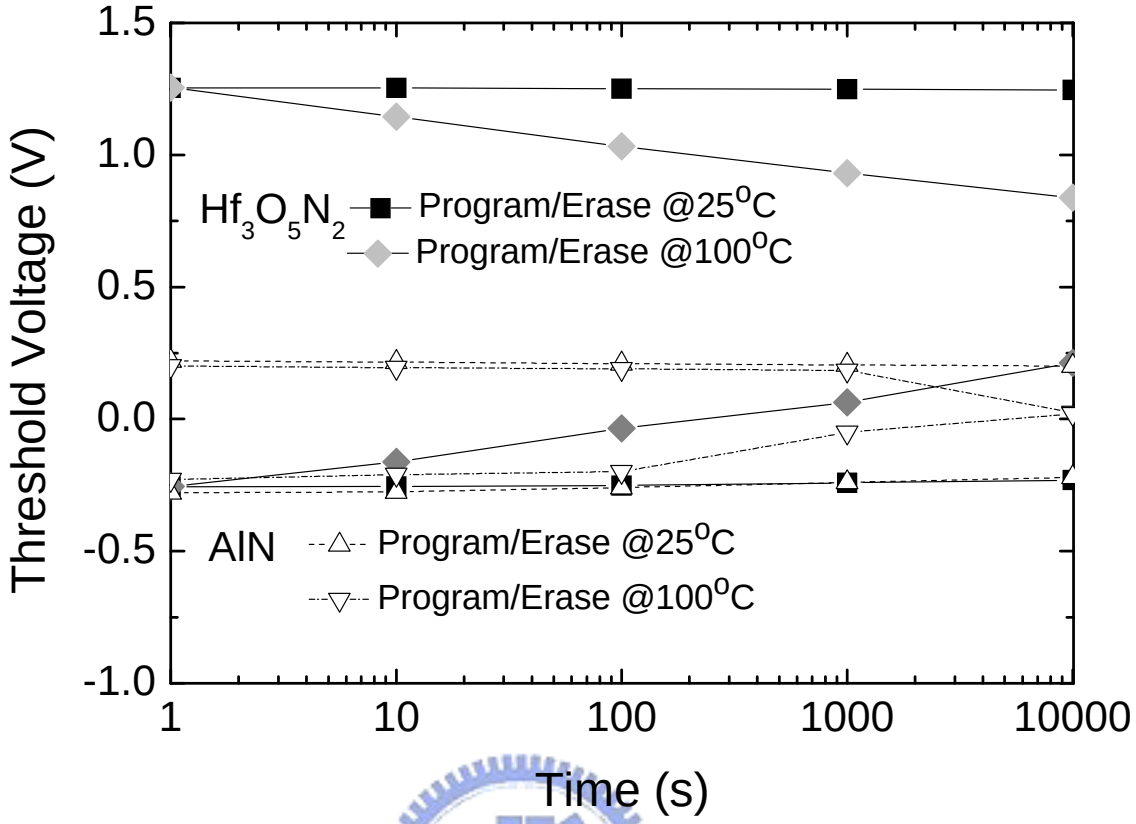


Fig. 3-7 Retention characteristics at 25 and 100°C of an $Hf_3N_2O_5$ MIS capacitor, measured to 10000 s, after the 1 ms, ± 5 V P/E writing pulse. The data for an AlN MIS capacitor are shown for comparison.

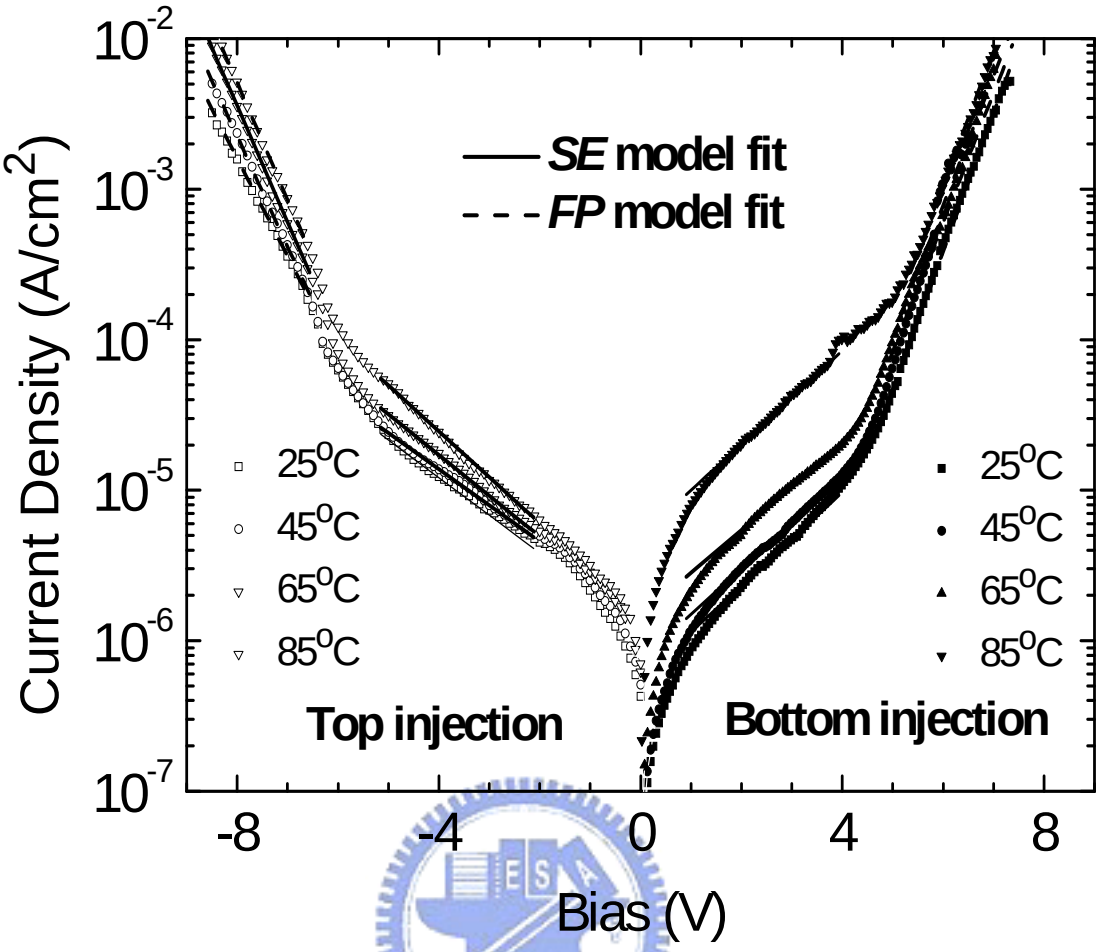


Fig. 3-8 The *J-V* characteristics of a TaN/$Hf_3N_2O_5$/Si MIS device. The lines are fits to *SE* or *FP* models using eq. (3.1).

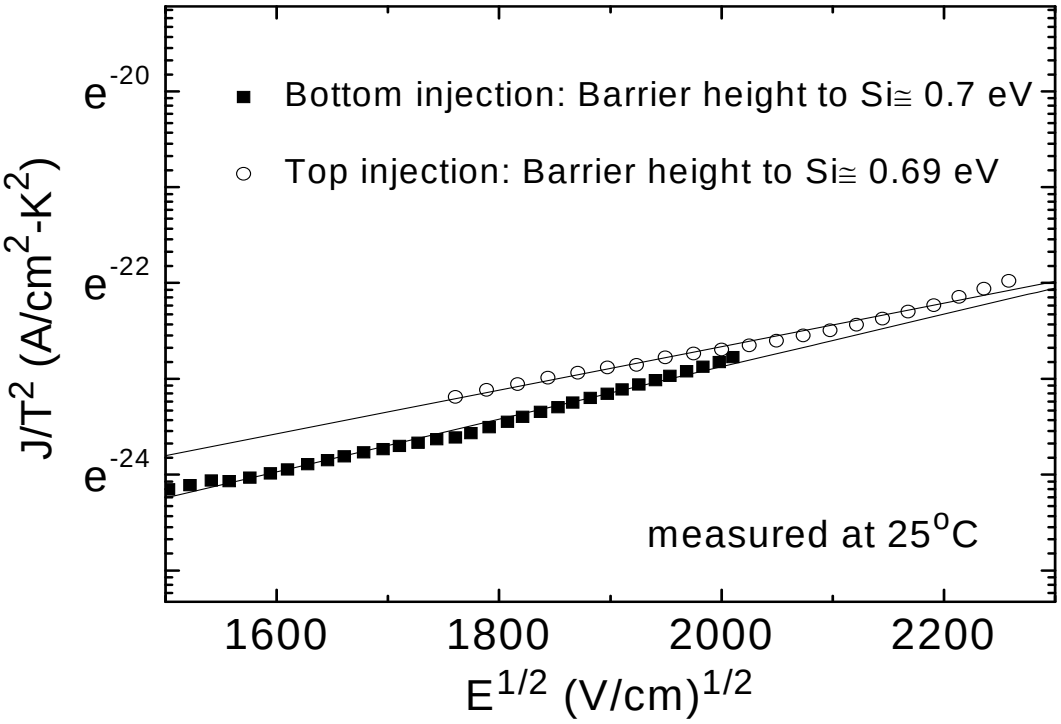


Fig. 3-9 A $ln(J/T^2)$-$E^{1/2}$ plot and *SE* calculations for TaN/$Hf_3N_2O_5$/Si capacitor data at low electric field with electron injection from either lower Si or upper TaN electrodes.

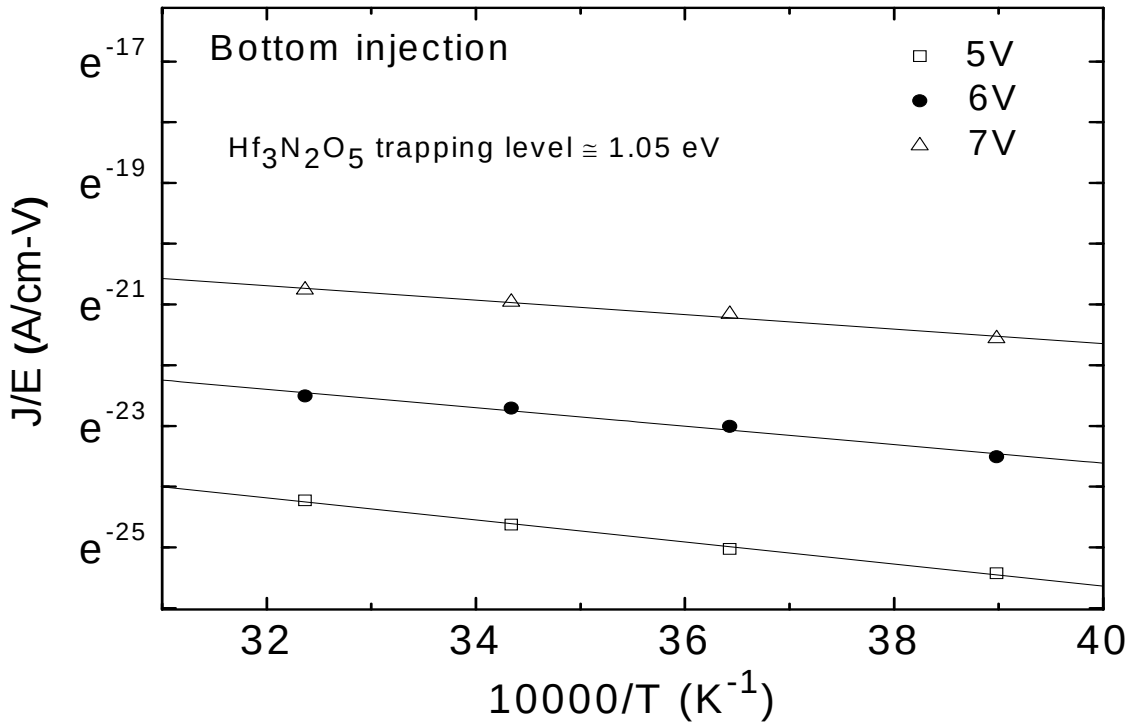


Fig. 3-10 The *ln*(*J/E*)-*1/kT* plots and *FP* calculations of bottom injection forTaN/$Hf_3N_2O_5$/Si device data at high field.

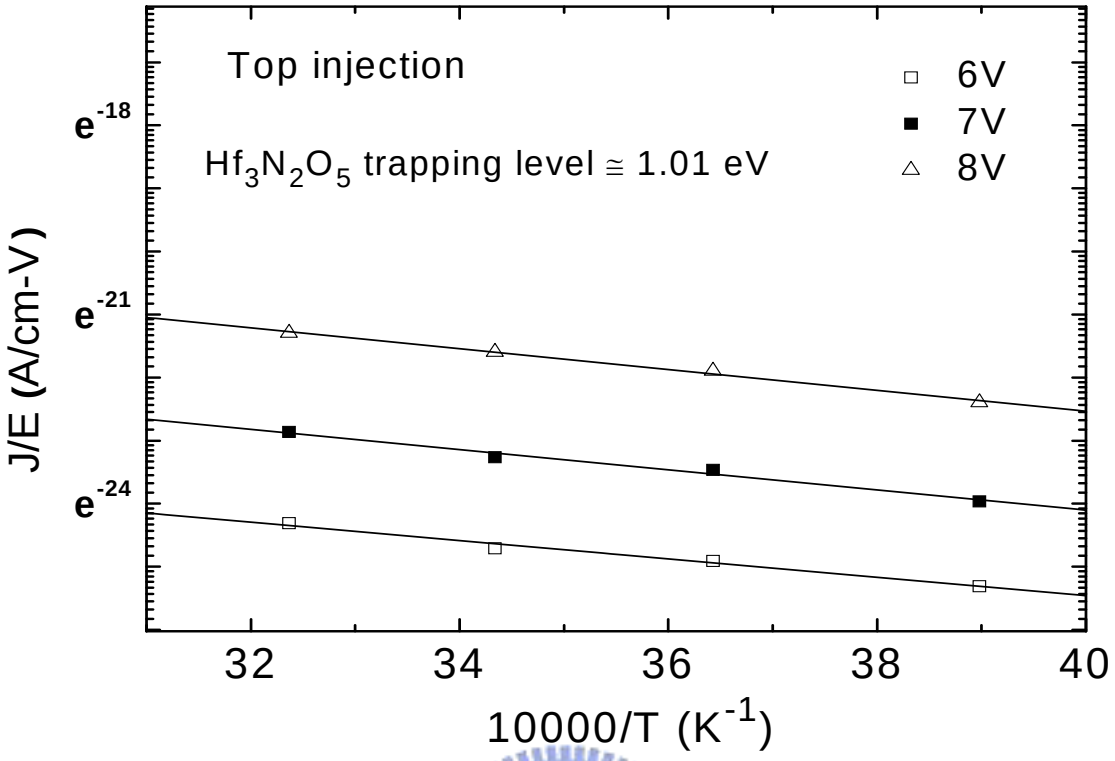


Fig. 3-11 The *ln*(*J*/*E*)-*1*/*kT* plots and *FP* calculations of top injection for TaN/$Hf_3N_2O_5$/Si device data at high field.

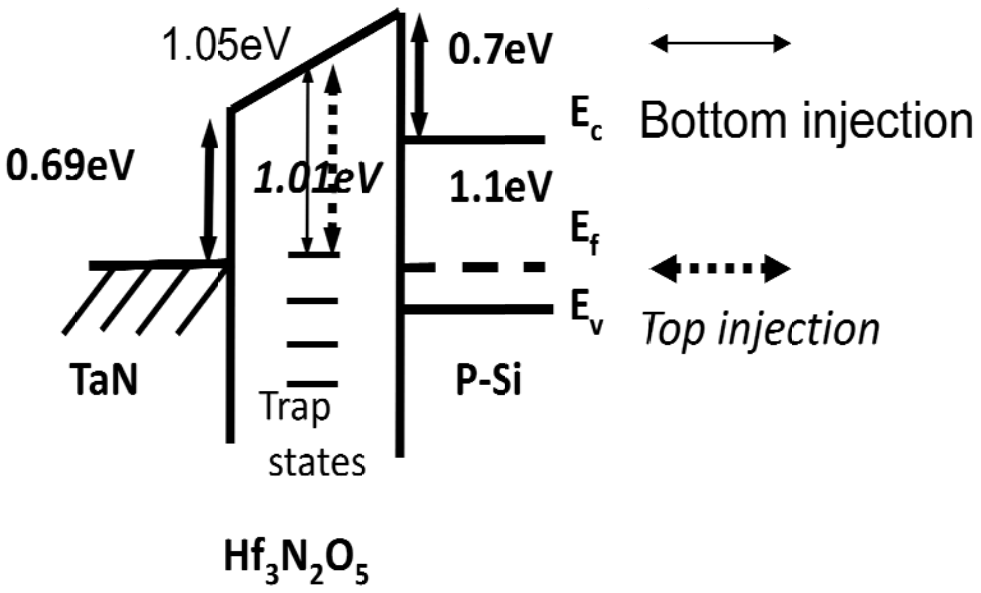


Fig. 3-12 Band diagram of $Hf_3N_2O_5$ MIS devices. The barrier height and trap energy were obtained from *SE* and *FP* model calculations to the measured $ln(J/T^2)$-$E^{1/2}$ and $ln(J/E)$-$1/kT$ data.

Chapter 4

Conclusion

We have demonstrated a program-erasable high-κ $Hf_3N_2O_5$ MIS capacitor for many applications such as DRAM and Flash memories. The programmed charges can be erased by a low operation voltage of -5V for 1ms. The other merits of this capacitors includes good data retention for 10^4 sec which can extend long memory time, a high capacitance density of ~6.5 $fF/\mu m^2$ can reduce the chip size, and a large C-V hysteresis necessary for charge storage. So, this program-erasable high-κ $Hf_3N_2O_5$ capacitor with good data retention would provide an alternative solution to volatile and nonvolatile memories.

We also compared the trapping capability with Si_3N_4 and Al_2O_3. Only a small C-V shift was shown in the Si_3N_4 capacitors which suggest shallower trap energy or lower trap density in that. The measured C-V characteristics of Al_2O_3 capacitors was observed continuously increasing V_{th} and could not be erased by negative voltage. It may be due to increasing trapping negative charges in the high-κ dielectrics. At the end of the discussion, we measured J-V characteristics and found a deep trapping level of 1.01~1.05 eV by theoretical models for Schottky emission (SE) at low electric field and Frankel-Pool (FP) conduction at high voltages.

In conclusion, we have fabricated the TaN/$Hf_3N_2O_5$/Si MIS capacitors which displayed a

high capacitance density of ~6.5 fF/μm^2, a large *C-V* hysteresis, a good data retention property and a deep trapping level of 1.01~1.05 eV.

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（民國 95 年 2 月~民國 97 年 1 月）

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