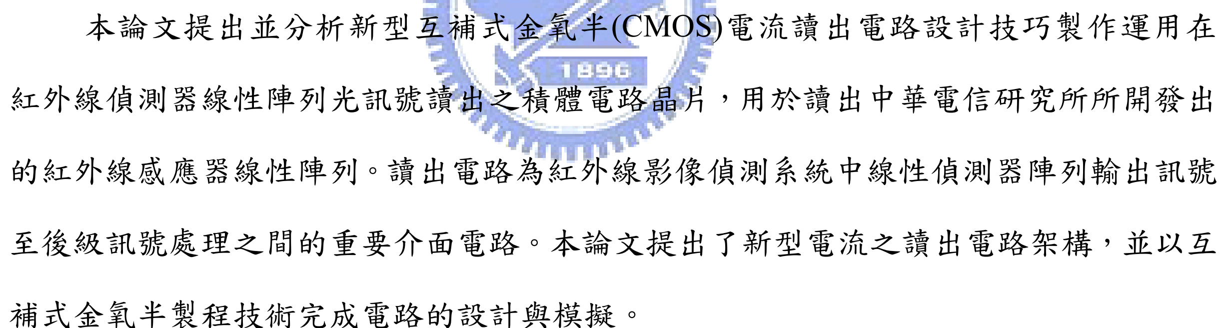
# 1 x 128 紅外線偵測器線性陣列之互補式金氧半讀出積體電路設計與分析

學生：鄭人文　　　　　　　　　　指導教授：吳 重 雨 博士

國立交通大學電機學院產業研發碩士班

## 摘要



本論文提出並分析新型互補式金氧半(CMOS)電流讀出電路設計技巧製作運用在紅外線偵測器線性陣列光訊號讀出之積體電路晶片，用於讀出中華電信研究所所開發出的紅外線感應器線性陣列。讀出電路為紅外線影像偵測系統中線性偵測器陣列輸出訊號至後級訊號處理之間的重要介面電路。本論文提出了新型電流之讀出電路架構，並以互補式金氧半製程技術完成電路的設計與模擬。

利用『緩衝式直接輸入』(Buffered Direct Injection)讀出架構，可以改進傳統『直接輸入』(Direct Injection)的問題與缺點。此前級訊號處理功能(on-FPA signal processing)可以提高讀出電路的效能並降低後級電路雜訊之影響。四種可選擇的積分電容和可獨立控制積分時間的功能更可增加光電流範圍。改良後的雙重三角取樣(Double Delta Sampling)電路除了可以減少固定樣式雜訊(fixed pattern noise)、時脈回饋雜訊、通道電荷注入和共模雜訊，還可以改善線性度和增加輸出電壓的擺幅。1 x 128 讀出晶片使用 0.35 µm 2P4M N-well 互補式金氧半技術設計並完成晶片研製，在 298K 溫度下及 3.3 V 工作電壓，其量測結果成功驗證了讀出晶片的效能。晶片尺寸 7.4mmx1.6mm、輸出線性度

為 99.73%、最大輸出擺幅為 1.6V、最大讀出速度為 10MHz、最大畫面速率為 30k frames/sec(4MHz 讀出速率)、可調積分 37.42us 到 0.935us (畫面速率為 26k frames/sec)、功率消耗為 14.5 mW。此高效能讀出電路具有高注入效率(injection efficiency)、高電荷容量(storage capacity)、高可調積分範圍、低雜訊等優點，可適用於大範圍亮度與高對比影像讀出的運用。

我們深信，吾人所提出之互補式金氧半讀出電路架構以及其設計技術已為紅外線影像系統之讀出處理電路設計提供一個新方向。爾後，相關的研究發展與實際應用於不同影像系統包括可見光與紅外線將持續進行。

# THE DESIGN AND ANALYSIS OF CMOS READOUT INTEGRATED CIRCUIT FOR 1x128 LINEAR INFRARED PHOTODETECTOR ARRAY

**Student : Ren-Wen Cheng** **Advisor : Chung-Yu Wu**

**Industrial Technology R & D Master Program of**
**Electrical and Computer Engineering College**
**National Chiao Tung University**

## ABSTRACT

In this thesis, a CMOS readout structure is proposed, developed, and applied to the implementation of photon signal readout integrated circuit for 1x128 linear InGaAs infrared photodetector array. The silicon readout circuit is an important interface circuit of detector array and signal processing stage in the IR image system. To achieve high performance readout and fit the working characteristic of IR detector material, a CMOS readout structure has been developed and fabricated. The functions and superior readout performance of the proposed CMOS readout structure have been verified by experimental measurement under 298K environment or simulations.

By using the buffered direct injection (BDI) circuit, it can improve the performance and

problem of the conventional Direct Injection (DI). The on-FPA signal processing capability of BDI circuit at front stage can reduce the noise effect of downstream circuit and improve the readout performance. The selectable integration capacitors and independent integration time control can enhance the optical current range. Moreover, the improved double delta sampling (DDS) circuit is used to not only suppress fixed pattern noise, clock feedthrough noise, channel charge injection but also common mode noise. An experimental 1 x 128 readout chip has been designed and fabricated by using 0.35 μm 2P4M N-well CMOS technology. The measurement results of the fabricated readout chip under 298K and 3.3 V supply voltage have successfully verified both readout function and performance. The size of the chip is 7.4mmx1.6mm. The linearity performance of the readout chip is better than 99.73% and the maximum output swing is 1.6V. The maximum readout speed is 10 MHz. The maximum frame rate at 4 MHz readout speed is 30k frames/sec. The integration time tunable range at 26k/s frame rate is from 37.42us to 0.935us. The total active chip power is below 14.5 mW at 298K. It is shown that a high-performance readout interface circuit for linear IR FPA with high injection efficiency, high charge sensitivity, large storage capacity, wide integration time tunable range and low noise is realized. These advantageous traits make the readout circuit suitable for the various applications.

It is believed that the proposed CMOS readout circuit and the associated design methodology offer new design scope and future feasibility for new-generation readout ICs of infrared detector array. Further improvement on circuit performance and practical applications in various image system including visible and thermal image readout will be explored and developed in the future.

# 致　　謝

首先感謝我的指導老師吳重雨教授耐心的指導與鼓勵，使我能順利完成碩士學位。在吳教授循序漸進的諄諄教誨下，讓我不僅獲得許多積體電路設計的專業知識，更學習到做研究時應有的挑戰困難及解決問題的態度與方法，面對問題時如何著手構思和勇於嘗試，雖然在過程倍感艱辛，但卻獲益良多。

其次要感謝口試委員闕河鳴教授、謝志成教授、施育全博士提供許多寶貴的意見與指導，使本論文可以更加完備。

再來要感謝中華電信研究所的洪朝耆博士在晶片規格上的協助與建議。感謝實驗室助理卓慧貞小姐在各項行政事務上的協助。

感謝林俐如、王文傑、虞繼堯、陳旻玹、陳勝豪、楊文嘉、蔡夙勇、林韋霆、陳煒明等諸位 307 實驗室學長姊在各項研究上的指導。感謝實驗室同學黃必超、謝仲朋、陳柏宏、許順維、許宴維、廖廷偉、黃世豪、張巧玲、楊松諭、賴忠裕等，陪我一起度過難忘的研究生活，營造互相激盪的討論風氣，不同觀點的知識分享。

最後，我要致上最深的感謝給我的父母親，謝謝你們一直以來的支持與鼓勵，讓我能順利完成學業。還有我的女友碧珠，謝謝妳總是能在我忙碌的時候，給予溫柔的體諒與溫馨的支持。期望將這份喜悅與你們共享。

**鄭 人 文**

**誌於 風城交大**

**九十七年 1 月**

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# CHAPTER 1

# INTORDUCTION

## 1.1 BACKGROUND

From 1950's, the infrared (IR) imaging system technology has been developed for various applications including IR search and tracking, medical examination [1], astronomy [2], forward-looking infrared (FLIR) systems, missile guidance, and other strategic equipment [3]. Among the infrared (IR) imaging system, linear Infrared (IR) imaging technology has recently been finding a growing range of applications including spectrocopy, foodinspection, moisture measurement, medical science, biology, WDM channel monitor, remote sensing and so on. These days, the design of linear IR image system with multi-function is more and more valuable. This concept has led to the increasing research and developments efforts in applying the commercial CMOS VLSI technologies in the design of IR imaging systems. Incorporating the rapid advancement in CMOS VLSI with the progress in linear infrared photo detector array technologies like detector material, sensing structure, optics, coolers, readout electronics, image enhancement, and intelligent signal processing results in the revolution of linear IR image systems to a new generation with significant performance improvement.

Generally speaking, the linear IR FPA system including two major parts which are: 1.Detector array 2.Readout electronics. Comparing with the conventional structures, the linear IR FPA has many natural advantages such as high packing density, low cost, high feasibility, on-chip signal processing, and high flexibility for system integration. For high sensitivity application, the linear IR FPAs are generally combined with narrow bandgap semiconductor

detectors, like InGaAs photodiode, and silicon multiplexer.

InGaAs, which is alloy of gallium arsenide and indium arsenide, is a popular material in infrared detectors, as shown in Fig. 1.1. In a more general sense, it belongs to the InGaAsP quaternary system that consists of alloys of indium arsenide (InAs), gallium arsenide (GaAs). indium phosphide (InP), and gallium phosphide (GaP). The InAs/GaAs alloy is referred to as $In_xGa_{1-x}As$ where x is the proportion of InAs and 1-x is the proportion of GaAs. The relationship between lattice constant and long wavelength cutoff of 4 ternary alloys in the InGaAsP family are shown in Fig. 1.2. The lattice constants and long wavelength cutoffs of these alloys are depicted as the red line in Fig. 1.2. For lots reasons, the most convenient substrate for $In_xGa_{1-x}As$ is InP. High quality and cheap InP substrate are available with diameters as large as 100mm. $In_xGa_{1-x}As$ with 53% InAs is often called “standard InGaAs”. It has the same lattice constants as InP, as shown in Fig. 1.2, and therefore the combination leads to very high quality thin films. Standard InGaAs with InP substrate forms heterojunction photodiode. Since the bandgap of InP is 1.35eV, InP is transparent for light whose wavelength exceeds 0.92um. The bandgap of $In_{53\%}Ga_{47\%}As$ is about 0.75eV, a value corresponds to a cutoff wavelength of 1.65um. Therefore, the waveband of standard InGaAs with InP substrate ranges from 0.9um to 1.7um.

The property of the detector array developed by Chunghwa Telecom Lab is illustrated by Fig 1.3, Fig 1.4 and Fig 1.5. In Fig 1.3, it is shown that when the detector is biased at -3V, the photo excited current is very stable and the detector shunt resistance is very large. Fig 1.4 shows the dark current of this detector, and Fig 1.5 shows the responsitivity of the InGaAs detector developed by Chunghwa Telecom laboratory. The detector array and the readout circuit array will be combined with the bonding wire.

## 1.2 MOTIVATION

The readout circuit of linear infrared (IR) photo detector array is a very important interface in the overall IR detection system. Thus, many technologies of designing readout circuit are still under development. There are various design requirements and constraints on the readout interface circuit such as charge storage capacity, noise, dynamic range, power dissipation, detector bias control, array size, and pixel pitch. As the cell number in the linear FPA becomes larger, the pixel size and pitch should be scaled down to accommodate more detector cells. The small pixel size limits the complexity of the input stage in the readout circuit and the storage capacitance, which may degrade the readout performance. Thus many efforts have been devoted to the developments of new techniques and circuits to improve readout performance under various constraints. By using selectable integration capacitors and independent integration time control techniques, the effective storage capacity, dynamic range, and noise performance are improved.

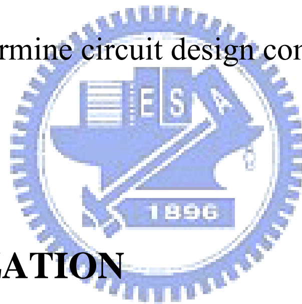
In this thesis, a current readout structure for linear IR FPA, called the buffered direct injection (BDI) circuit, is used to improve the readout performance. Moreover, the dynamic charging output stage with the double delta sampling (DDS) is included to eliminate noise. It has been shown from both simulation and experimental results that the readout circuit can achieve good readout performance through the use of BDI technique.

In this thesis, the proposed BDI readout circuit array will be combined with the 1 x 128 linear InGaAs IR detector array which developed by Chunghwa Telecom Lab to compose a complete IR image system. The function of snapshot is added to the chip to capture the image data of each pixel at the same time instant.

The system specifications are listed below:

1. Bias voltage 0 ~ 3.3V
2. Power consumption < 37.5mW
3. Optical dynamic range > 60dB
4. Snapshot
5. Non-linearity < 2%
6. Integration time adjustable
7. Output signal swing > 1V
8. Frame rate > 30k frame/s

According to bias voltage and output swing, the process can be determined. The frame rate can determine power consumption. The optical dynamic range, snapshot, non-linearity and integration time adjustable determine circuit design complexity and area.



## 1.3 THESIS ORGANIZATION

This thesis contain five chapters which include introduction, review of the techniques of developing the readout circuit, the architecture and circuit design, the both simulation results and experimental results of the fabricated readout chip, and the conclusions and future work.

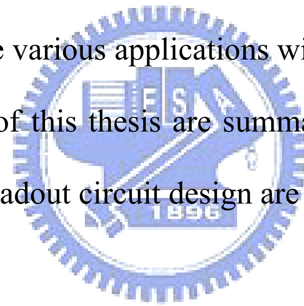
Chapter 1 introduces the background and explains the main topics of this thesis.

In Chapter 2, the architectures and operational requirements of IR FPA, and the CMOS readout techniques for IR detectors including the state-of-the-art structure are given. In this chapter, the analysis of advantages and drawbacks of the conventional direct injection (DI) input and buffered direct injection (BDI) input are given.

In Chapter 3, the circuit structure, readout strategy, and simulation results are presented. By applying BDI technique, this readout circuit can achieve good readout performance.

Moreover, the readout dynamic and application range is dramatically increased by using selectable integration capacitors and independent integration time control. The improved double delta sampling (DDS) circuit is used to reduce fixed pattern noise, clock feedthrough noise, and the noise from the effect of channel charge injection. Then the chip operation and simulation results are described.

In Chapter 4, an experimental 1 x 128 readout chip has been designed and fabricated in TSMC 0.35 μm 2P4M N-well CMOS technology. The measurement results of the fabricated readout chip under temperature 298K and 3.3V supply voltage have successfully verified both readout function and performance. It has been shown that a high-performance readout interface circuit for linear IR FPA with high injection efficiency, high charge sensitivity, high linearity, and low noise is realized within the pixel pitch of 100 um. These advantageous traits make the circuit suitable for the various applications with a wide range of input current.



Finally, the main results of this thesis are summarized in Chapter 5. Some suggestions for the future work about the readout circuit design are also discussed.

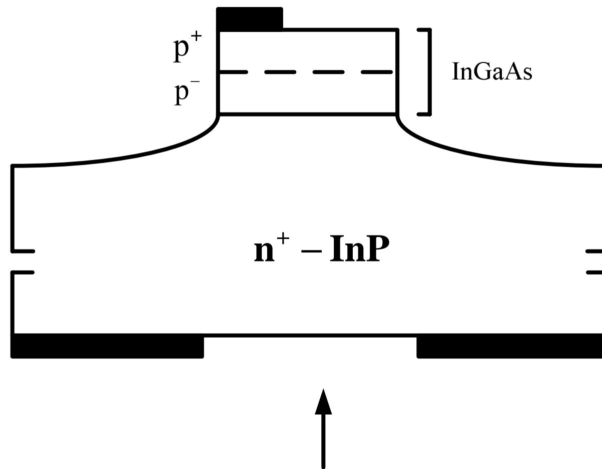



Fig 1.1 The structure of InAsAs photodiode.

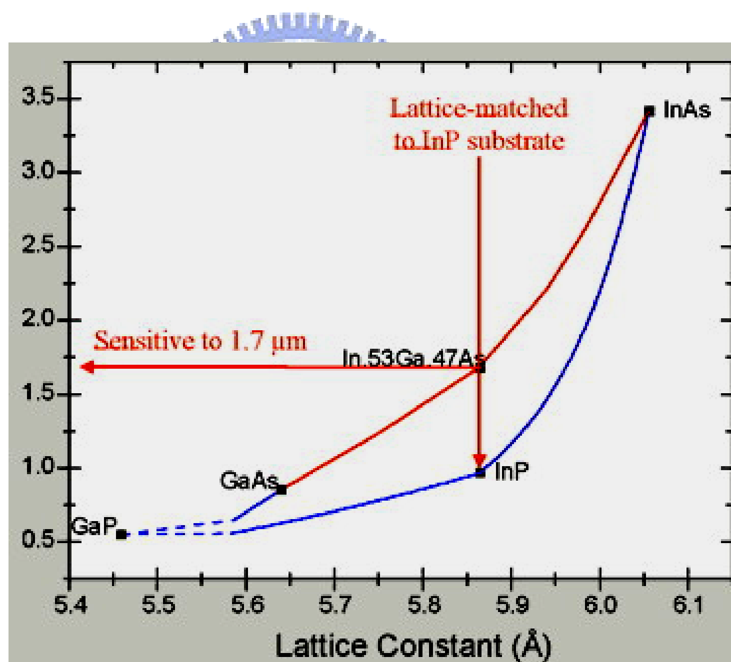



Fig 1.2 The relationship between the lattice constant and the long wavelength cutoff of the 4 ternary alloys in the InGaAsP family.

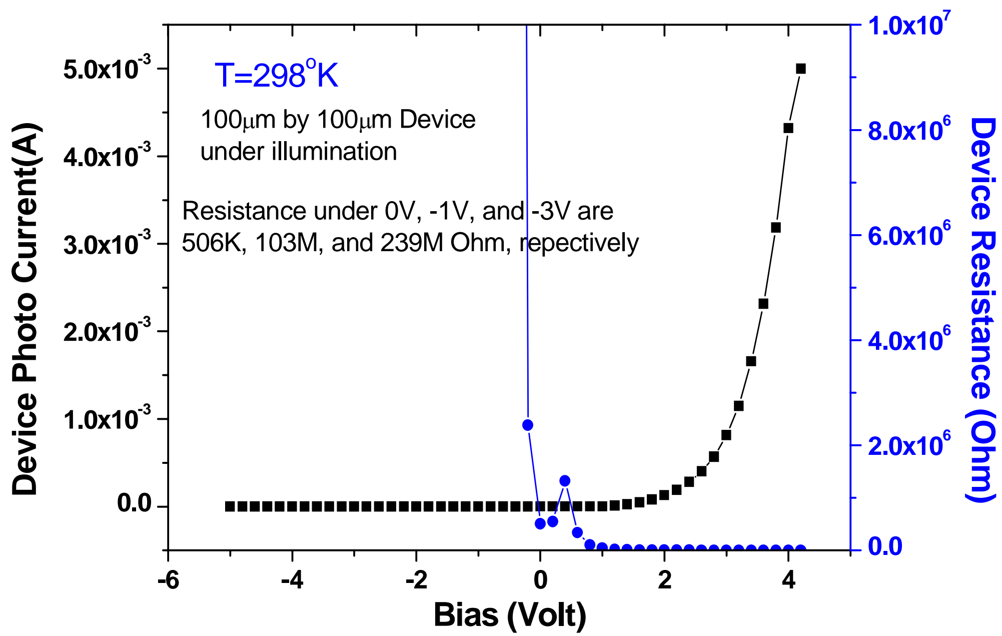



Fig 1.3 The characteristic of the InGaAs detector developed by Chunghwa Telecom laboratory.

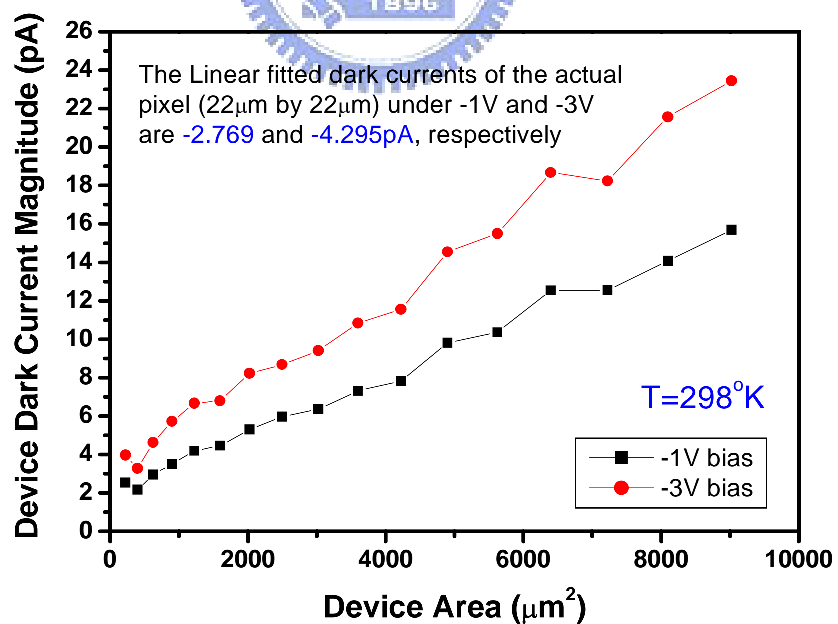



Fig 1.4 The device dark current of the InGaAs detector developed by Chunghwa Telecom laboratory.

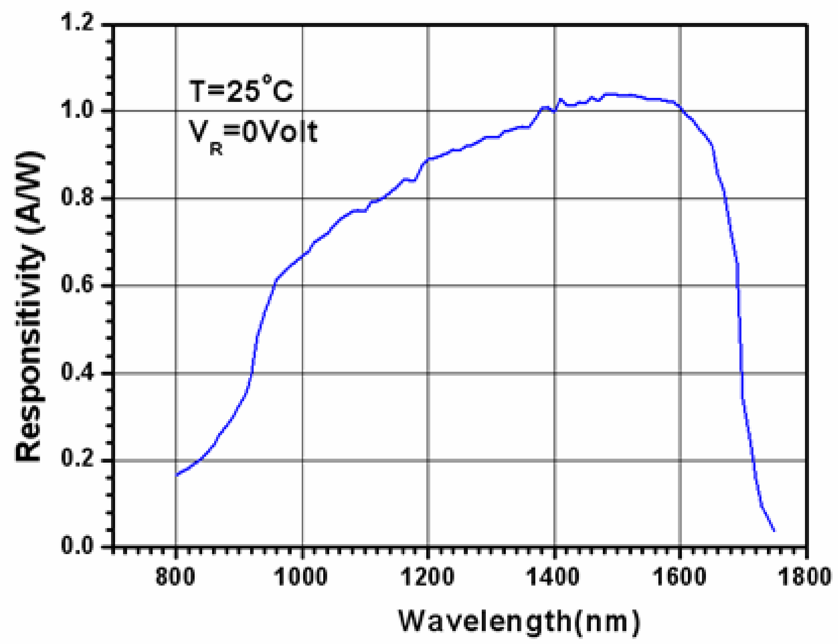
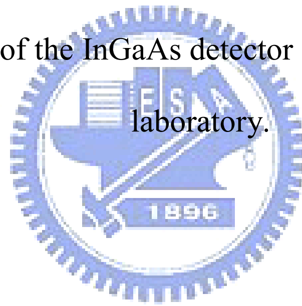



Fig 1.5 The responsitivity of the InGaAs detector developed by Chunghwa Telecom laboratory.



# CHAPTER 2

# REVIEW ON OPERATION REQUIREMENT AND CMOS READOUT TECHNIQUIES FOR IR PHOTODIODE SENSORS

## 2.1 OPERATION REQUIREMENT[4]

In different applications of IR image systems, there exist certain specific requirements for the design of IR FPAs. In general, the requirements involve a broad range of electrical circuit and detector array parameters like detector bias control, injection efficiency, charge storage capacity, integration time, noise, dynamic range, readout rate, array size and pixel pitch, power consumption, and operating temperature. Some general discussions of these requirements are summarized below.

1) Detector Bias Control :

The dark current, injection efficiency, detector 1/f noise, and responsibility are affected by the detector bias. Moreover, operation ability and linearity of spectral response are also affected directly by the bias. Therefore, a strict and stable detector bias control is necessary in IR FPAs.

2) Injection Efficiency and Bandwidth :

The injection efficiency is defined as the ratio of the current flowing into the readout circuit to the detector current. High injection efficiency and wide input bandwidth leads to good responsibility and readout performance. To achieve high injection efficiency and wide bandwidth, the input impedance of the interface circuit should be lower than the shunt resistance of IR detectors.

3) Charge Storage Capacity :

In most readout structures of IR FPAs, the photon excited carriers are accumulated on the integrating capacitor and transferred to voltage output. Therefore, the charge storage capacity is determined by both background and dark current levels of IR detectors as well as the value of integrating capacitor. Maximum charge storage capacity can be achieved by keeping background and dark currents small and using a large integrating capacitor. However, the capacitance value is limited by pixel size and the chip area of readout circuit.

4) Noise :

Noise in the IR FPAs can be separated typically into two categories, random noise and pattern noise. Random noise varied temporally and is not constant from frame to frame in the imager. Pattern noise is divided into two components, one is fixed pattern noise (FPN) and the other is the photo-response nonuniformity (PRNU). The FPN comes from dimensions, doping concentration, and contamination of photo-detectors and the characteristics of threshold voltage, width, and length in MOSFETS. The PRNU noise comes from the thickness of layers on the top of photo-detectors and wavelength of illumination. These noises in the CMOS in the IR FPAs are briefly discussed below.

(i) Random Noise :

An imager with a constant scene should produce identical output from frame to frame. In practice, the output from a given pixel will vary over time due to thermal noise, charge trapping, and 1/f noise in the devices which comprise the imager. Photonic shot noise is usually not included in this quantity, although this also contributes to noise at the output. Random noise is typically stated in terms of input-referred equivalent electrons, i.e., the root mean square (rms) output voltage noise divided by the conversion gain.

(ii) Fixed-Pattern Noise :

Fixed-pattern noise (FPN) is the fixed (constant in time) variation between pixel outputs

under spatially uniform illumination. Fixed-pattern noise is typically due to random or mask-induced mismatches in device parameters such as threshold voltage, trap density, and parasitic capacitance. FPN is usually a function of illumination, and can be written as the sum of a gain term and an offset term for an imager with a linear response characteristic. Offset FPN is constant over illumination, and gain FPN is proportional to illumination.

FPN consists of components that describe variation between columns, and variation between pixels in a single column. Column FPN is the standard deviation of the column-average pixel output values in a time-average, uniformly illuminated frame. The column FPN is expressed as :

$$\text{FPN (column)} = \sqrt{\frac{\sum_j (\overline{P_j} - \overline{P})^2}{j-1}} \tag{2.1}$$

Where $\overline{P_j}$ is the average pixel value in column j and $\overline{P}$ is the average pixel value in the frame. Since a column FPN calculation requires multiple columns, j > 1. Pixel FPN is the standard deviation of pixel output values after column FPN has been removed. In order to calculate pixel FPN, multiple pixels are required. The pixel FPN is expressed as

$$\text{FPN (pixel)} = \sqrt{\frac{\sum_{i,j} (\overline{P}_{i,j} - \overline{P}_j)^2}{i \cdot j - 1}} \tag{2.2}$$

where i • j > 1.

(iii) Reset Noise :

If the diffusion of the photodiode is reset through a MOSFET, this is equivalent to a capacitance being charged through the resistance of the MOSFET channel. The rms (root-mean-square) noise voltage can be expressed as

$$\langle V_{rms} \rangle = \sqrt{\frac{kT}{C}} \tag{2.3}$$

where k is the Boltzmann constant, T is temperature, and C is the capacitance of photodiode. The reset noise is generally called "KTC" noise.

(iv) Thermal Noise :

Thermal noise is due to the random thermal motion of the electrons and is unaffected by the presence or absence of direct current. It is a white noise which means the noise power is constant over all frequencies. For a resistor, the thermal noise rms voltage can be expressed as

$$\langle V_{rms} \rangle = \sqrt{4kTBR} \quad (2.4)$$

where B is the noise bandwidth and R is the resistor. Since the thermal noise covers the entire frequency range, the bandwidth determines the actual amount measured.

(v) Shot Noise :

Shot noise is another white noise that arises from the discrete nature of the electrons, for example, the random arrival of particles of charge. This is the result of the random generation of carriers such as thermal generation within a depletion region (i.e. shot noise of dark current) or the random generation of photon-electrons, and always associated with the direct-current flow through the device.

(vi) Flicker (1/f) Noise :

The flicker noise occurs at any junction, including metal-to-metal, metal-to-semiconductor, semiconductor-to-semiconductor, and conductivity fluctuation. The flicker noise arises mainly in amplifier circuits where there are numerous such contacts. At low frequency, flicker noise can be the dominant component, but it drops below thermal noise at higher frequency.

5) Dynamic Range :

The dynamic range is defined as the ratio of maximum charge capacity to noise floor. The required dynamic range of IR FPAs is determined by the ratio of the brightest signal level

to the weakest. Larger dynamic range is preferred but limited by storage capacitance, linearity, and noise level.

6) Readout Rate :

The readout rate is chosen according to the specific IR system requirement and limited by the allowable chip power dissipation as well as the circuit operation speed. Usually a higher readout rate is needed for multiple sampling applications in image compensation function. Higher readout rate is also needed to avoid the saturation of the signal after integration.

7) Integration Time :

Like the readout rate, the integration time is chosen according to the application consideration. Generally, the saturation frequency of the integrating capacitor and the detector sensitivity determine the proper length of integration time.

8) Array Size and Pixel Pitch :

The array size and pixel pitch are usually determined by the IR FPA technology. Higher image resolution requires larger array size and smaller pixel pitch. However, a larger pixel size is needed to increase the integration capacitance and improve the performance of charge capacity and dynamic range. Thus optimal design trade-off should be made between the application flexibility and resolution performance.

9) Power Dissipation :

This is a typical requirement in the applications of the IR FPA using photon detector instead of thermal detector. Power dissipation is limited by the heat loading of the cryogenic cooling system which determines the system cost.

10) Operating Temperature :

The operating temperature is determined by the detected wavelength range and the material of IR detectors. For each detector, there is a unique operating temperature.

It is important to determine the operational requirements in the design of an IR FPA for specific applications. A complete analysis of operational parameters like IR background radiation level, spectral response band, operating temperature, detector structure, signal contrast ratio, sensitivity, and resolution should be set before the design trade-off. Therefore, all the operational requirements discussed above have unique optimized orientations for IR image systems in different applications.

## 2.2 CMOS READOUT TECHNIQUES

In the development of IR FPAs, the readout circuit electronics is the second major part next to the IR detector array. Readout electronics is deigned to support a good interface between IR detector and the following signal processing stage. Different circuit techniques have been developed for IR FPAs with different materials and structures. The readout circuit techniques based on silicon CMOS VLSI technology are addressed in the following discussion.

Generally, the pixel pitch of IR FPAs is reduced with the increasing array size and resolution. Moreover, the total power dissipation of IR FPAs is limited by the image system. These two major factors often put constraints on circuit design space and complexity. Thus the design of IR FPA readout electronics requires a trade-off between circuit performance and complexity.

Some simple readout structures like source-follower per detector (SFD), direct injection (DI), and gate-modulation input (GMI) are still commonly used in large staring IR FPAs because of the small pixel area and power consumption. In addition, more complex circuit techniques like buffered direct injection (BDI), capacitive transimpedance amplifier (CTIA),

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and buffered gate modulation input (BGMI) have been developed to provide excellent bias control, high injection efficiency, linearity, and noise performance. Simple and high-performance circuit techniques have been a challenging work in the design of readout circuits for IR FPAs.

In the following, some of the commonly used CMOS readout techniques as well as the state-of-the-art structures will be reviewed. The noise reduction strategies used to improve IR image performance are also discussed.

### 2.2.1 Pixel Readout Circuits

1) Source-follower per Detector [5] :

A simple readout circuit called the source-follower per detector (SFD) is shown in Fig. 2.1 where a NMOS source-follower MNI and MNL, a reset PMOS gate M-Rst, and a multiplexing NMOS device M-Sel are used in each cell. The integration capacitance is the summation of detector shunt capacitance $C_{detector}$ and input node capacitance of the SFD. The integration capacitor is reset to high and then discharged by the photocurrent $I_{detector}$. After an integration period, the cell voltage signal is sampled to the output stage serially through the device M-Sel controlled by the clock *Select*. The simple structure of the SFD makes it suitable for the applications of high density, large format, and low power IR FPA. However, since the photon excited carrier charges are integrated on the input node capacitance of the detector directly, the detector bias voltage changes through integration. It can result in variations of detector characteristics and non-linearity of readout current, which limit the application of SFD. Moreover, the SFD is susceptible to KTC noise induced by the integration-and-reset function and fixed pattern noise (FPN) caused by the process-dependent threshold voltage variations. Usually, a correlated double sampling (CDS) stage is used to reduce the KTC

noise of the SFD readout circuit.

2) Direct Injection [6] :

Another simple readout circuit called the direct injection (DI) is shown in Fig. 2.2. In the DI circuit, a common-gate PMOS device $M_{DI}$ is used to bias and sense the current of the IR detector. The detector current $I_{detector}$ passing through the gate $M_{DI}$ is further integrated on the integration capacitor $C_{int}$ which can be reset by the NMOS device M-Rst. The integrated voltage is readout through the PMOS source follower MPI and the multiplexing device M-Sel. In the DI circuit, a better bias control than the SFD during integration is supported by the common gate device $M_{DI}$. Like the SFD circuit, the DI circuit has a simple structure and no active power dissipation. This makes it suitable for high-density IR FPA applications. The injection efficiency of a readout circuit is defined as the ratio of the current flowing into the readout circuit to the detector photocurrent $I_{detector}$. The injection efficiency of the DI is determined by the ratio of detector shunt resistance to input resistance of $M_{DI}$. Thus a lower input resistance means a higher injection efficiency and better detectivity. Since the input resistance of the PMOS device $M_{DI}$ is proportional to its overall current including the background current level. Thus, the DI is not suitable for the applications of low-background IR image readout. Moreover, a stable and low noise dc bias $V_{DI}$ is needed in the DI circuit. Both threshold voltage non-uniformity and KTC noise are still problems of the DI readout circuit.

3) Buffered Direct Injection [7], [8] :

A complex readout circuit called the buffered direct injection (BDI) circuit is shown in Fig. 1.8 where the circuit structure is similar to the DI except that an additional inverted gain stage with the gain -*A* is connected between the gate node of the common-gate input device $M_{BDI}$ and detector node. The input impedance can be decreased by a factor of *A* due to the negative feedback structure. Thus, the injection efficiency is increased to near unity. Usually, the inverted gain stage can be implemented by differential pair or inverter. The detector bias

control of the BDI is more stable than those of SFD and DI due to the virtual-short property of the gain stage. Besides, the source voltage of $M_{BDI}$ can be tuned by adjusting $V_{com}$, thus the bias of the IR detector can be turned to get a stable photo current. Moreover, both equivalent input referred noise and operational bandwidth can also be improved as compared to the DI circuit by this inverted gain stage. Since the detector bias is controlled by the input voltage $V_{com}$ of the differential pair instead of $V_{DI}$ and gate-to-source voltage of $M_{DI}$ in the DI circuit, both threshold voltage non-uniformity problem and strict low-noise bias requirement of the DI are immune. However, the additional gain stage consumes active power during integration. This additional power loading can be reduced by proper design of the gain stage with low bias current. Generally, the BDI is suitable for those applications which require high readout performance and can afford additional circuit complexity, chip area, and power dissipation.

4) Capacitive Transimpedance Amplifier [9] :

The schematic of the capacitive transimpedance amplifier (CTIA) is shown in Fig. 2.4. Where the integration capacitor $C_{int}$ is placed on the feedback loop of the amplifier with a reset device M-Rst to discharge the integration capacitor and reset the amplifier output to the reference voltage $V_{com}$. The detector bias is also controlled by $V_{com}$ through the virtual-short feature of the amplifier. Thus a good detector-bias control can be obtained in the CTIA as the BDI. Due to the Miller effect on the integration capacitor, its capacitance can be made extremely small to obtain low-noise and high-sensitivity performance. Unlike DI and BDI, the input impedance of the CTIA is independent of detector current. However, the feedthrough effect of the reset clock can be coupled to the detector node and affect the stability of both detector bias and amplifier operational point. Moreover, additional area and power consumption of the inverted gain stage are needed in the CTIA. Usually, the inverted gain stage is implemented by a differential amplifier to provide low detector bias offset and a CDS stage is used to eliminate the KTC noise.

4) Gate Modulation Input [10] :

The gate modulation input (GMI) readout circuit has a current-mirror configuration with the tunable source bias $V_{source}$ to control the current gain as shown in Fig. 2.5. The injection current flowing into the master device $M_{load}$ is mirrored and amplified by the slave device $M_{input}$ and integrated on the integration capacitor $C_{int}$. The current gain of the current mirror $M_{load}$ and $M_{input}$ is tunable by the adjustable bias $V_{source}$. Similar to that in the DI circuit, the injection efficiency of the GMI is dependent on the ratio of detector shunt resistance to input resistance of $M_{load}$. However, the inherent current gain of the GMI leads to higher detection sensitivity and reduced input referred noise as compared to the DI. Moreover, the adaptive current gain in the GMI can be controlled by the background level and thus the realizable background suppression leads to a higher dynamic range. However, both injection efficiency and current gain of the GMI are sensitive to the variations of $V_{source}$ and threshold voltages.

The effective injection efficiency (or current gain) $A_{I.\mathrm{GMI}}$ which is the current ratio between $\Delta I_{\mathrm{input}}$ and $\Delta I_{\mathrm{photo}}$, the injection efficiency $\eta_{inj.\mathrm{DI}}$ of the direct injection (DI) readout structure, and the detector bias $V_D$ can be expressed as

$$A_{I.\mathrm{GMI}} = \frac{\Delta I_{\mathrm{input}}}{\Delta I_{\mathrm{photo}}} = \frac{g_{m.\mathrm{input}}}{g_{m.\mathrm{load}}} \eta_{inj.\mathrm{DI}} \tag{2.5}$$

$$\eta_{inj.\mathrm{DI}} = \frac{g_{m.\mathrm{load}} \mathrm{R_D}}{1 + g_{m.\mathrm{load}} \mathrm{R_D}} \tag{2.6}$$

$$\mathrm{V_D} = \mathrm{V_{sub}} - \mathrm{V_{GS.Mload}} - \mathrm{V_{source}} \tag{2.7}$$

where $g_{m.\mathrm{input}}$ ($g_{m\cdot\mathrm{load}}$) is the transconductance of the input (load) MOSFET $M_{input}$ ($M_{load}$) under input background current bias, $R_D$ is the detector shunt resistance, $V_{sub}$ is the detector N-node bias (N-on-P type PV detector), $V_{GS.Mload}$ is the gate-to-source voltage under input background current bias, and $V_{source}$ is the external adjustable source node voltage. The current $I_{load}$ and the gate-to-source voltage $V_{GS.Mload}$ of the load device $M_{load}$ can be expressed as

$$I_{\mathrm{load}} = K_{\mathrm{load}} \left( \mathrm{V_{GS.Mload}} - \mathrm{V_T} \right)^2 \tag{2.8}$$

$$V_{GS.Mload} = \sqrt{\frac{I_{load}}{K_{load}}} + V_T \tag{2.9}$$

where $K_{load}$ is the transconductance parameter of the MOS device and $V_T$ is the threshold voltage. From Eqs. (2.7) and (2.9), the detector bias $V_D$ can be expressed as

$$V_D = V_{sub} - \sqrt{\frac{I_{load}}{K_{load}}} + V_T - V_{source} \tag{2.10}$$

It is shown from Eq. (2.10) that the detector bias is sensitive to the adjustable source voltage $V_{source}$ noise and threshold-voltage variations. Since the detector shunt resistance $R_D$ is sensitive to the detector bias $V_D$, the injection efficiency is also sensitive to $V_{source}$ and threshold voltage variations as may be seen from Eqs. (2.6) and (2.10). To obtain a stable injection efficiency, a strict control on both $V_{source}$ and threshold voltage uniformity is required.

Using Eqs. (2.8) and (2.9) and the relation $V_{G.Minput} = V_{GS.Mload} + V_{source}$, the mirrored current $I_{input}$ can be represented as

$$\begin{aligned} I_{input} &= K_{input}\left(V_{GS.Mload} + V_{source} - V_T\right)^2 \\ &= K_{input}\left(\sqrt{\frac{I_{load}}{K_{load}}} + V_{source} + V_T - V_T\right)^2 \end{aligned} \tag{2.11}$$

Thus we have

$$\sqrt{I_{input}} = \sqrt{K_{input}}\left(\sqrt{\frac{I_{load}}{K_{load}}} + V_{source}\right) \tag{2.12}$$

Since the transimpedance $g_m = 2\sqrt{KI}$, the transimpedance ratio between $M_{input}$ and $M_{load}$ is

$$\begin{aligned} \frac{g_{m.input}}{g_{m.load}} &= \sqrt{\frac{K_{input}}{K_{load}}}\frac{\sqrt{I_{input}}}{\sqrt{I_{load}}} \\ &= \sqrt{\frac{K_{input}}{K_{load}}}\sqrt{K_{input}}\left(\frac{1}{\sqrt{K_{load}}} + \frac{V_{source}}{\sqrt{I_{load}}}\right) \end{aligned} \tag{2.13}$$

As may be seen from Eqs. (2.13) and (2.5), the value of the current gain $A_{I.GMI}$ has a wide

range of several orders of magnitude depending on the IR detector background current. The smaller the current, the higher the current gain. This means an adaptively controlled current gain. Moreover, the current gain also depends on $\eta_{inj.\mathrm{DI}}$ and $V_{source}$. Thus the current gain can be additionally adjusted by $V_{source}$.

However, it is shown in Eq. (2.5) that the GMI circuit, like the DI readout structure, needs a large detector shunt resistance to achieve high injection efficiency and thus a high current gain. Since the injection efficiency is sensitive to $V_{source}$ and threshold voltage variations, so is the current gain. From Eqs. (2.5) and (2.13), it can be shown that the GMI circuit is susceptible to fixed-pattern-noise due to threshold-voltage variations in the transistors $M_{load}$ and $M_{input}$ causing the current gain to vary from one cell to another. To obtain a large total dynamic range in the GMI circuit, the current gain should be kept high and uniform. This leads to strict requirements on MOSFET threshold-voltage uniformity and extremely low noise of the dc bias $V_{source}$ which are difficult to control.

From the discussion above, the properties of the GMI structure are obtained. The advantages are :

i) The current mirror amplifies the photo excited current, therefore the GMI can achieve high injection efficiency.

ii) Due to the simple structure, the pixel pitch can be very small to extend the array size larger.

iii) The current gain can be adjusted to suitable value according to the current level by the external adjustable $V_{source}$.

And the drawbacks of the GMI are :

i) The injection efficiency (or current gain) is affected by the threshold voltage variation and the noise of the adjustable $V_{source,}$ and the linearity is affected at the same time.

ii) From Eq. (2.7), it is shown that the bias of the detector varies with the level of the excited

photo current and the noise of the adjustable $V_{source}$. Therefore, the linearity will be affected by this factor.

5) Buffered Gate Modulation Input (BGMI) [11] :

The buffered gate modulation input (BGMI) structure is improved from GMI structure as shown in Fig. 2.6. The circuit structure is similar to the GMI except that an additional inverted gain stage is connected between the gate node of the common-gate input device and detector node. By applying $V_{com}$ to the amplifier, the detector bias will keep stable to improve the linearity. Besides, the current mirror with adaptive gain control is not sensitivity to source noise.

The effective current gain $A_{I.\mathrm{BGMI}}$ of the BGMI circuit, the injection efficiency $\eta_{inj.\mathrm{SBDI}}$ of the SBDI readout structure [12], and $V_D$ are

$$A_{I.\mathrm{BGMI}} = \frac{\Delta I_{\mathrm{input}}}{\Delta I_{\mathrm{photo}}} = \frac{g_{m.\mathrm{input}}}{g_{m.\mathrm{load}}} \eta_{inj.\mathrm{SBDI}} \quad (2.14)$$

$$\eta_{inj.\mathrm{SBDI}} = \frac{(1+A) g_{m.\mathrm{load}} R_{\mathrm{D}}}{1 + (1+A) g_{m.\mathrm{load}} R_{\mathrm{D}}} \quad (2.15)$$

$$\mathrm{V_D} = \mathrm{V_{sub}} - \mathrm{V_{com}} \quad (2.16)$$

where $A$ is the gain of the amplifier and $V_{com}$ is the common input bias. As may be seen from Eq. (2.15), high injection efficiency can be achieved with a smaller $R_D$ requirement as compared to that in the GMI circuit. Moreover, the injection efficiency is not sensitive to threshold voltage variations and noise of the source bias voltage. The detector bias $V_D$ is independent of the MOS threshold voltage and any source bias voltage as in Eq. (2.16). Thus, unlike the GMI circuit, the threshold non-uniformity and source-bias-voltage noise have no effect on the detector bias.

As seen from Eq. (2.14), the current gain is equal to the transconductance ratio between $M_{input}$ and $M_{load}$. To increase the current gain, $g_{m.\mathrm{input}}$ should be larger than $g_{m.\mathrm{load}}$. To achieve

this without any external bias voltage, shorter channel length is used in $M_{input}$ whereas narrower channel width is used in $M_{load}$. Due to short-channel and narrow width effects, the threshold voltage of $M_{load}$ is greater than that of $M_{input}$. With the threshold diffrence $\Delta V_T$, the transconductance ratio in Eq. (2.14) can be similarly derived as

$$\begin{aligned}\frac{g_{m.\text{input}}}{g_{m.\text{load}}} &= \sqrt{\frac{K_{\text{input}}}{K_{\text{load}}}}\frac{\sqrt{I_{\text{input}}}}{\sqrt{I_{\text{load}}}} \\ &= \sqrt{\frac{K_{\text{input}}}{K_{\text{load}}}}\sqrt{K_{\text{input}}}\left(\frac{1}{\sqrt{K_{\text{load}}}}+\frac{\Delta V_T}{\sqrt{I_{\text{load}}}}\right)\end{aligned} \tag{2.17}$$

In Eq. (2.17), the threshold voltage difference $\Delta V_T$ is geometry dependent and thus is very stable. Unlike the GMI circuit, no strict source bias voltage control is required in the BGMI circuit. The current gain of BGMI circuit is immune to threshold non-uniformity and noise of the source bias voltage. It can also be adaptively controlled by different IR background input flux. This high front-stage current gain makes the downstream circuit and system noise contribution extremely low. It results in a low input referred noise. Moreover, BGMI circuit can operate with a larger integration capacitance compared to DI and BDI and still obtain low noise performance and high charge detection sensitivity.

The integration capacitance is connected to the input MOSFET $M_{input}$ through a row select device. In the integration period, the drain voltage of $M_{input}$ will not be identical. Therefore, the current gain of the current mirror will not keep constant, thus the linearity decrease. Besides, the integration capacitance is shared for each column, the value of the capacitance should be chosen large to eliminate all the parasitic capacitance of the connecting node of the integration capacitance and all the row select switches. With the larger value of integration capacitance, the readout rate decreases.

From the discussion above, the characteristics of BGMI are obtained. The BGMI not only keeps the advantages of GMI such as high injection efficiency, low noise, but also has more benefits like fixed detector bias control and adaptive gain control.

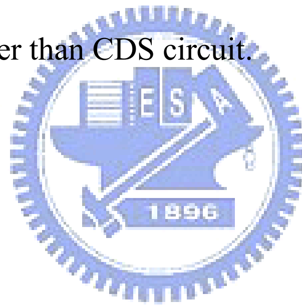
### 2.2.2 Noise Reduction of IR Image

Temporal noise and pattern noise are two main noise types of IR image systems. The temporal noise sources include shot, thermal, 1/f (flicker), generation-recombination, KTC, and photon noise which are contributed by detectors and readout circuits. The pattern noise is caused by the process dependent variations which produce offset drifts among detector channels. Usually, the temporal noise can be reduced by detector technology, operational condition, circuit techniques, and system arrangement, whereas the fixed pattern noise can be reduced by calibration techniques [13]. The two-point and multipoint calibrations are commonly used to reduce the FPN [14]. The required number of calibration points is dependent on the infrared radiation determined by the range of object temperature variations. A larger radiation means a larger output voltage swing and more nonuniformity of response. For the same range of temperature variations, the infrared radiation of medium-wavelength IR (MWIR) detector is larger than that of long-wavelength IR (LWIR) detector. Thus, the number of calibration points of MWIR readout is usually more than that of LWIR readout. The noise sources contributed by readout circuits should be carefully reduced to achieve a background limited performance (BLIP). Some general strategies of noise reduction for readout circuits like correlated double sampling (CDS) [15], modified CDS [16], multiple correlated sample read (MCS) [17], chopper-stabilized input circuit (CSI) [18], double delta sampling (DDS) [18] have been proposed.

### 2.2.3 Double Delta Sampling (DDS) Circuit

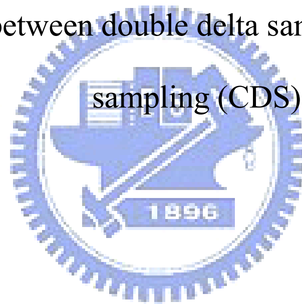
The most commonly used readout circuit in CMOS imagers is double delta sampling (DDS) circuit [19] as shown in Fig. 2.6. The DDS circuit is composed of column sampling

circuit and output correlated double sampling circuit. The two branches in column sampling circuit are used to store the reset and signal voltage. Each branch consists of a sample and hold capacitor (CS or CR) with a sampling switch (SHS or SHR) and the first source follower with a column-selection switch (Csel). The clamp switches, the coupling capacitors (COS and COR), and the output drivers are common to an entire column of pixels. The load transistors of the first set of source follower and the subsequent clamp circuits and output source followers are common to the entire array. The DDS circuit can be used to suppress fixed pattern noise (FPN) and clock feedthrough noise. The disadvantage of DDS circuit is the high noise due to channel charge injection. Table 2.1 shows that the difference between double delta sampling (DDS) and correlated double sampling (CDS). Although DDS circuit has larger circuit area and consumes higher power than CDS circuit, the capability of noise reduction in DDS circuit is better than CDS circuit.



| | CDS | DDS |
|---|---|---|
| Reduced fixed pattern noise | yes | yes |
| Clock feedthrough | higher | lower |
| Charge injection | lower | medium |
| Remove low frequency noise (common mode) | yes | yes |
| Remove high frequency noise (common mode) | no | yes |
| Circuit area | smaller | larger |
| Power | lower | higher |
| Off-chip offset voltage | no | yes |

Table 2.1 The difference between double delta sampling (DDS) and correlated double sampling (CDS).



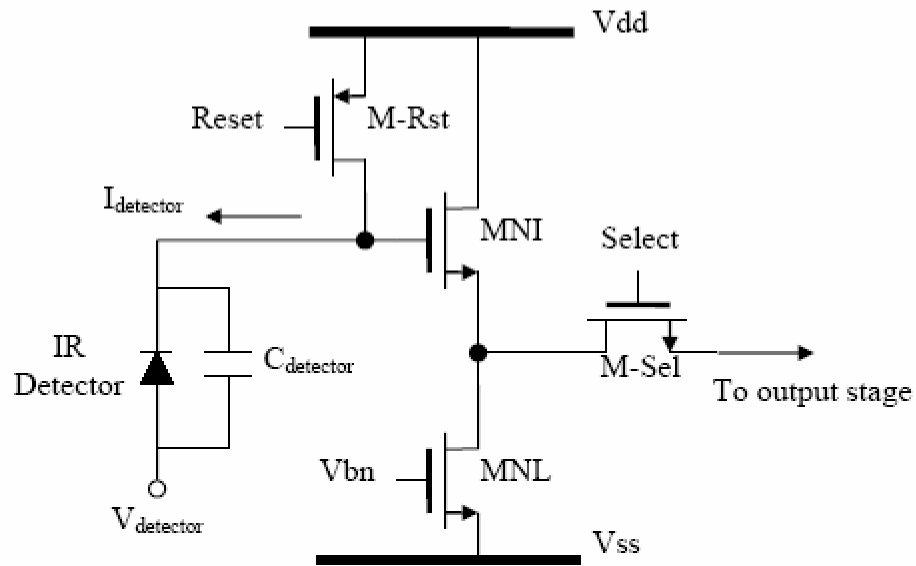
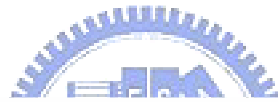



Fig. 2.1 The source follower per detector (SFD) readout circuit.



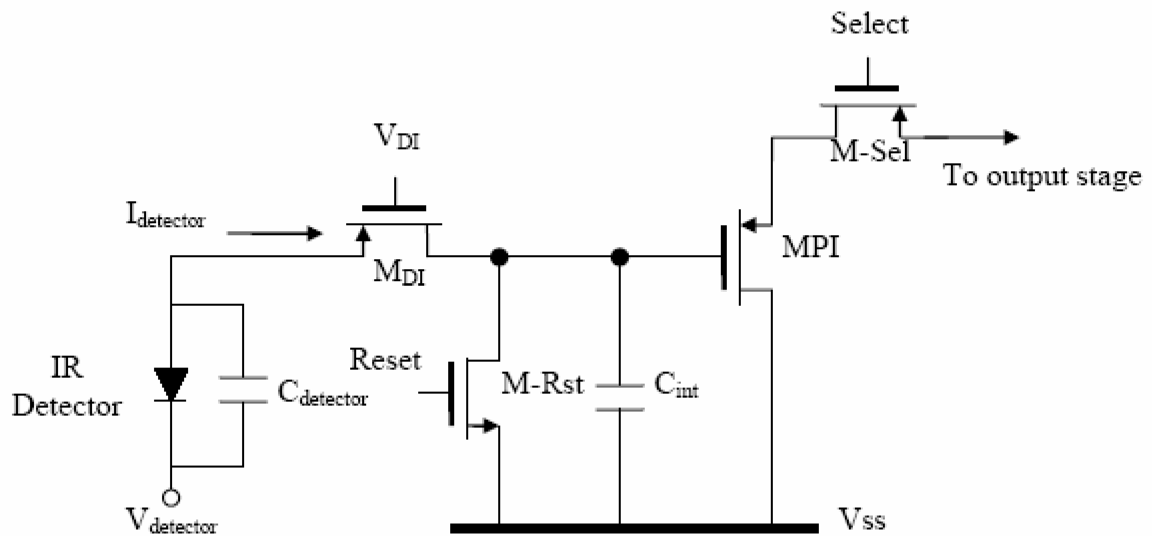



Fig. 2.2 The direct injection (DI) readout circuit.

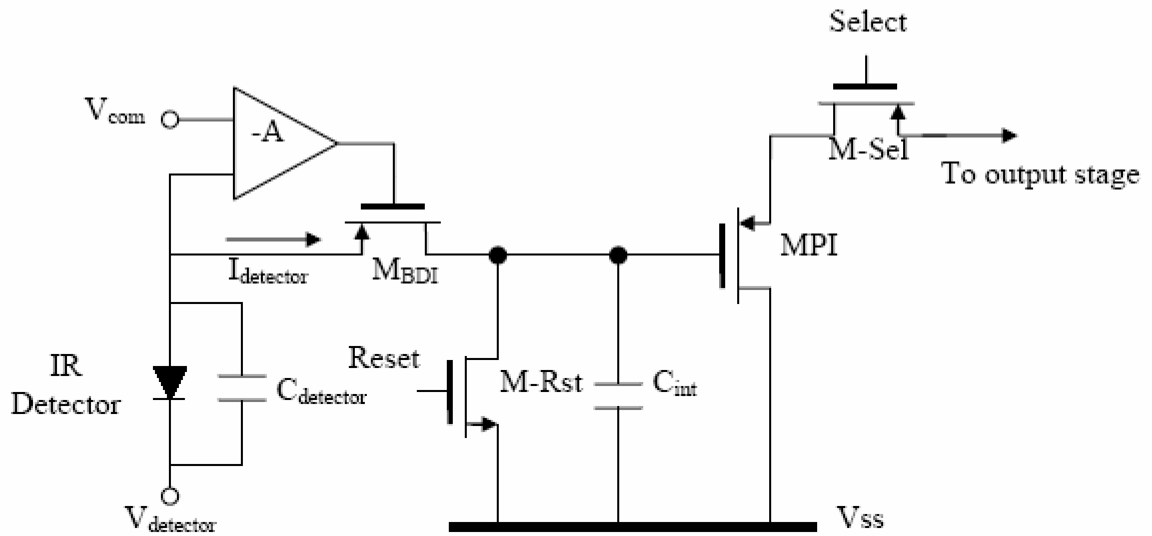



Fig. 2.3 The buffered direct injection (BDI) readout circuit.

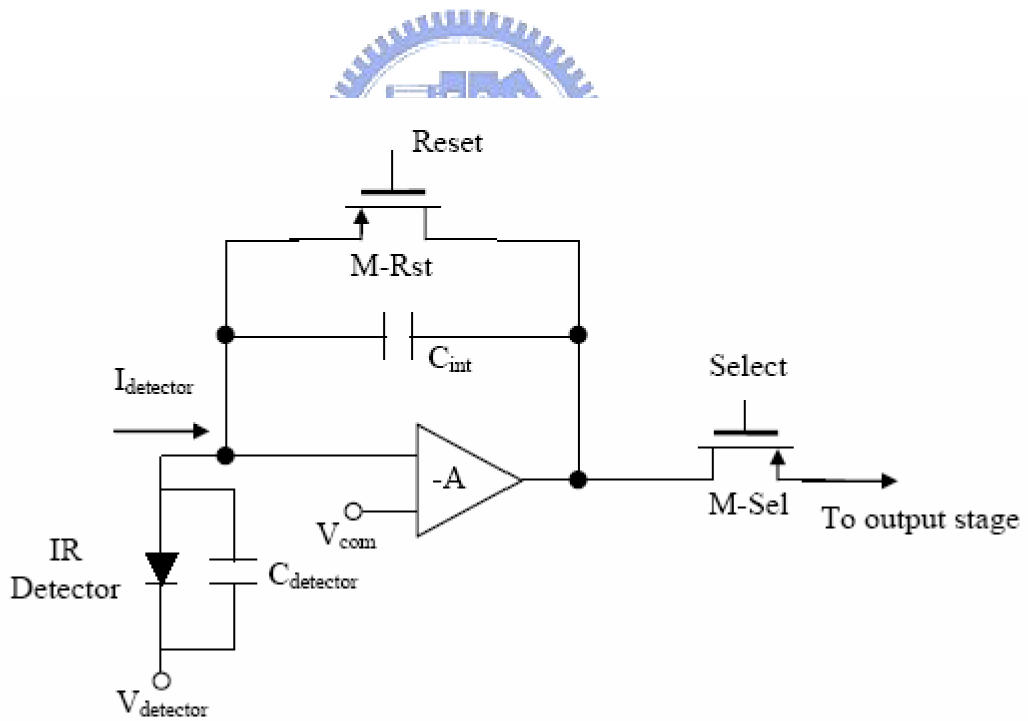



Fig. 2.4 The capacitive transimpedance amplifier (CTIA) readout circuit.

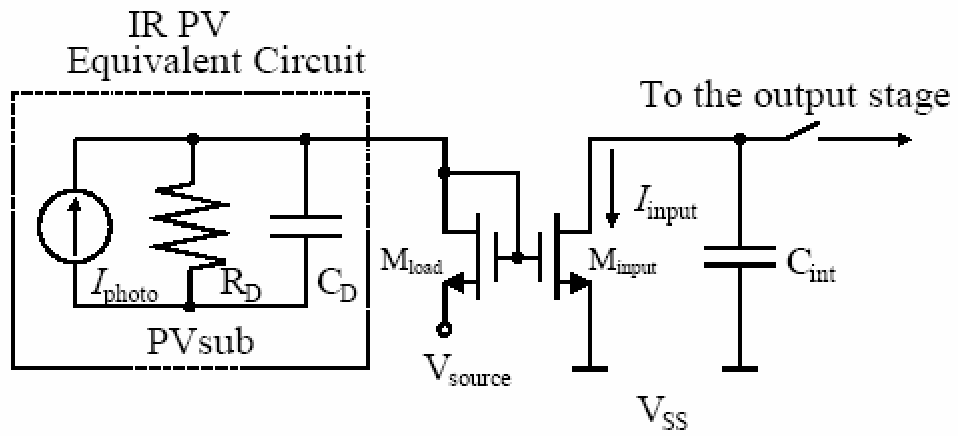



Fig. 2.5 The gate modulation input (GMI) readout circuit.

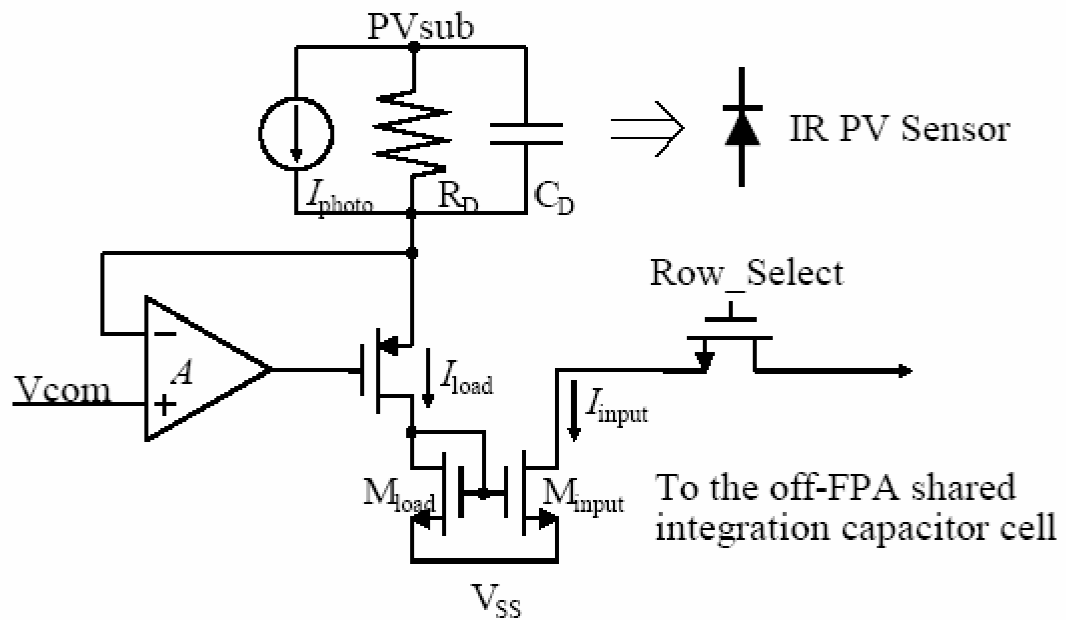



Fig. 2.6 The buffered gate modulation input (BGMI) readout circuit.

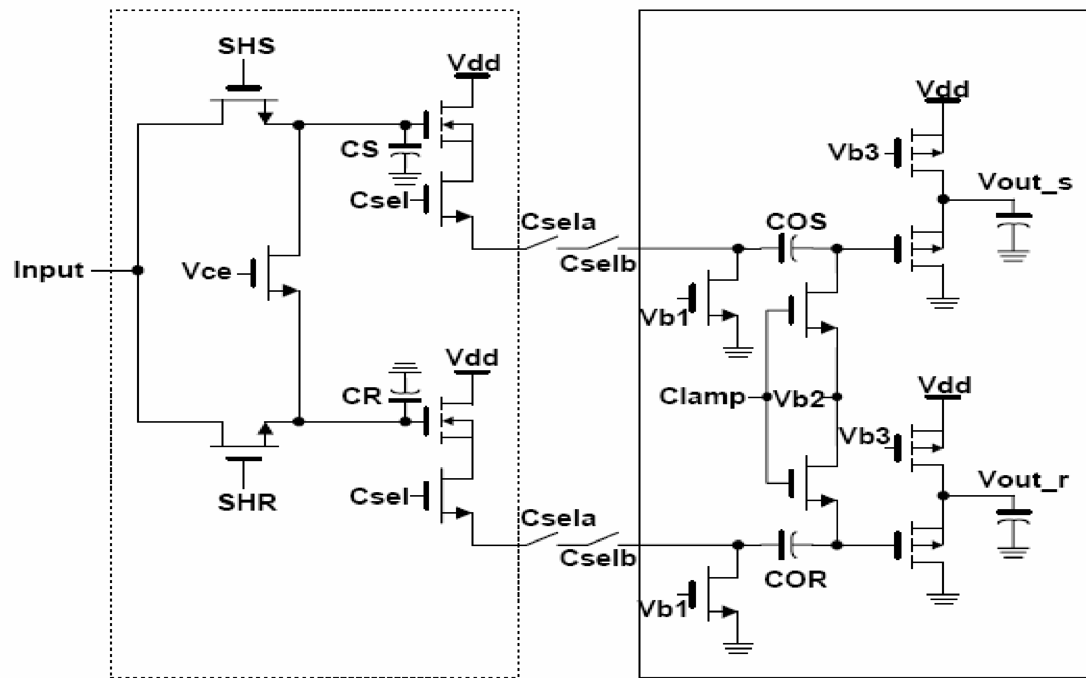
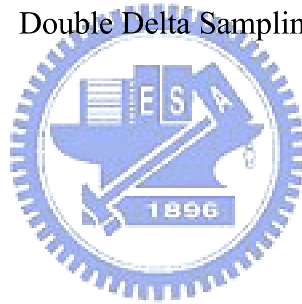



Fig. 2.7 Double Delta Sampling (DDS) circuit.



# CHAPTER 3

# ARCHITECTURE AND CIRCUIT DESIGN

## 3.1 CHIP ARCHITECTURE

Fig. 3.1 shows 1 x 128 array configuration. Two ROIC chips are bonded on the two sides of 1 x 128 infrared photo sensor array, one for even pixels and the other for odd pixels, to read out the detected image data. Two chips are used to read out the image data of detector with the smaller pixel pitch. EVEN ROIC accepts the output data of ODD ROIC and serially reads out the entire image data of the detector. Additionally, the readout data rate is the same with system clock rate. Fig. 3.2 is the block diagram of the architecture of the IR readout chip, including digital control circuit, column readout circuit (Unit-cell BDI input stage and Column sampling circuit) and output CDS circuit. This chip receives photo currents from the IR sensor and transforms the intensity of photo current into voltage scale by a sequence of processing in each unit cell. Then, the processed voltage signals in column readout circuit are one by one sent to the output CDS circuit and make further processing. Digital control circuit accepts the signals (vdir, Fsyn and clk) outside the chip to decide the function of the chip and generate the signals inside the chip to control the actions of analog circuit (column readout circuit and output CDS circuit). Column readout circuit has 64 unit-cell circuits. Each unit-cell circuit receives photo current from 1x128 sensor array (odd or even pixels) and transform photo current signal into voltage signal by using the integration capacitor to store the charge, which is injected from the input photo current. The column readout circuit generates two analog output voltages. One is the signal proportional to the gray scale intensity

of the image, and the other is the reset voltage signal at the integration capacitor. The transformed voltage signals (integration and reset) are held simultaneously in 64 unit-cell circuits and wait for further processes. Then, the reset and integrated signals are serially sent to Output CDS circuit and the CDS operation is performed. When the CDS operation is performed, the processed results are differentially sent to the outputs.

## 3.2 CHIP OPERATION

In Fig. 3.1, two RIOC chips are put on different sides of 1-D sensor array and the chip receiving the photo current of the even pixels accept output results of the other chip receiving the photo current of the odd pixels. To serially read out the detected image data of 1x128 infrared sensor array from pixel 0 to pixel 127 in one chip, the processed results of the detected image data in different chip must be sent out in different output priority and be serial interlace. The output data rate is the same with system clock. In addition to the functions of different output priority and serial interlace, the capability of independent integration time control is also added in the chip. The detailed description of these three functions is depicted as the follows:

1) **Control of Output Priority and Serial Interlace Output:** The chip can be set to two different output priority modes by setting the off-chip signal, vdir, to vdd or gnd. When vdir is set to vdd, the chip is in positive output priority mode and the sequence of the processed data in output CDS circuit is read out from unit-cell 0 to unit-cell 63. When vdir is set to gnd, the chip is in negative output priority mode and the sequence of the processed data in output CDS circuit is read out in reverse order. To serially read out the detected image data of 1x128 infrared sensor array in the shared channels in one chip, the processed results of the two chips can’t not simultaneously appear in the shared

channels. The processed results of the chip in negative output priority mode must be delayed one unit time and sent out to the shared channel. As shown in Fig. 3.3, the sequence of output data is from cell00 to cell63 when the chip is operated in positive mode. The sequence of output data is from cell63 to cell00 when the chip is operated in negative mode. The outputs of the two chips in different output priority mode are serial interlaced and then the transformed results of 1 x 128 infrared photo sensor array are serially sent out from pixel0 to pixel127. The readout rate is the same with system clock. The off-chip pulse signal Lsyn in Fig. 3.3 is used for output synchronization. It is high on the later half period, half clock cycle, of every output data and can help integrate with system for acquisition of effective data.

2) **Independent Integration Time Control:** The one-bit digital signal Fsyn is given outside the chip not only to trigger the occurrence of data output but also to control the integration time without any change of clock frequency. In Fig. 3.4, when Fsyn signal is from low to high, the processed results of all cells begin to serially send to the output. The period and the duty cycle of the signal Fsyn can also decide the integration time. When the signal, Fsyn, is from high to low, all the integration capacitors in Column Readout circuit begin to integrate.

## 3.3 CIRCUIT DESIGN

### 3.3.1 Analog Circuit

Fig. 3.5 shows the schematic of the analog circuit. The analog circuit is composed of unit-cell BDI input stage and DDS circuit. The combination of column readout circuit and output CDS circuit are called double delta sampling (DDS) circuit. The analog circuit of the

readout chip uses the source follower, which provides fixed voltage drop vgs, to pass on the signal from the stage to the next stage for processing. As shown in Fig. 3.6, the equation of the NMOS source follower is :

$$V_{gs} = \sqrt{\frac{I_d}{k}} + V_t = \sqrt{\frac{I_d}{k}} + V_{th0} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi}) \tag{3.1}$$

When the voltage at the gate of Mn1 is at high value, the rise of $I_d$ and $V_{SB}$ causes the increase of $V_{gs}$ and reduce the dynamic range of the output swing. The root of $I_d$ and $V_{SB}$ also cause the nonlinearity of the output of the readout circuit. Therefore, the cascoded current source is used to fix the value of $I_d$. For the PMOS source follower, the source can be connected with the N-well substrate, $V_{SB} = 0$, to avoid the influence of body effect. In the following, the BDI and improved DDS structure will be described in details.

#### 3.3.1.1 Buffered Direct Injection (BDI) Input Stage

Fig. 3.7 shows the input stage structure with the InGaAs photodiode. The input stage circuit is composed of the buffer-direct-injection (BDI) readout structure, the NMOS transistor Mrst as the reset switch, the PMOS source follower Mp1, Mp2 and Mp3, and three optional integration capacitors Cint1, Cint2 and Cint3 with three transistor switches Mrs1, Mrs2 and Mrs3. In the BDI readout structure, the inverting input of a gain stage with gain A is connected to the node “in” and the noninverting input is connected to the bias voltage Vcom. The output of the gain stage is connected to the gate of Min as a common-gate input stage. The gain stage is implemented by a CMOS differential pair to reduce the chip area. The circuit diagram of the gain stage is shown in Fig. 3.8. The device parameters in the circuit diagram of the gain stage are given in Table 3.2. Through the BDI circuit, the bias of the node “in” is controlled by the input voltage Vcom of the differential pair. The value of Vcom is set to be 2 V by a low-noise constant voltage source to maintain the voltage of the node “in” at or

near 2 V. The additional power consumption of the differential pair in each column readout circuit can be reduced by proper design of gain stage with low bias current. The BDI readout structure is used to obtain stable zero detector bias.

In Fig 3.7, the amplifier is connected as negative feedback type. Therefore the bias voltage of the IR detector is fixed and is adjustable by adjusting Vcom. The difference between common voltage Vcom and IR detector substrate bias PVsub deference determines the bias condition of detector. Every unit-cell will combine with the detector by a bonding wire. When the detector absorbs infrared flux, the photo-generated current flows into the integration capacitor and is transformed to voltage by integrating the capacitor in each unit-cell.

In the following, the injection efficiency, noise performance of BDI structure, and the reduction of dark current, shot noise and thermal noise will be describe in details.

1) **Input Impedance and Injection Efficiency:**

The main design goal of the current readout input stage of IR detectors is to achieve a high injection efficiency and low noise. The input impedance in the BDI readout structure is decreased by a factor of A due to the negative-feedback structure. The injection current from the pixel is mainly drained toward the due to the low input impedance. The injection efficiency $\eta(s)$ and the bandwidth $f_{BW}$ of a direct-injection (DI) structure can be expressed as [20], [21]

$$\eta(s) = \frac{g_m R_d}{1 + g_m R_d}\left(\frac{1}{1 + s/2\pi f_{BW}}\right) \tag{3.2}$$

$$f_{BW} = \frac{1 + g_m R_D}{2\pi R_D C_T} \tag{3.3}$$

The injection efficiency and the bandwidth of a buffered direct-injection (BDI) are

$$\eta(s)=\frac{(1+A)g_m R_d}{1+(1+A)g_m R_d}\left(\frac{1}{1+ {s}/{2\pi f_{BW}}}\right) \tag{3.4}$$

$$f_{BW}=\frac{1+(1+A)g_m R_D}{2\pi R_D C_T} \tag{3.5}$$

In the above equations, $A$ is the gain of the buffer, $g_m$ is the transconductance of the input gate, and $R_D(C_T)$ is the total input shunt resistance (shunt capacitance) of the IR detector. The current injection efficiency is increased by the gain of the buffer, which makes the injection efficiency close to 1. From Eqs. (3.4) and (3.5), it can be clearly seen that the injection efficiency $\eta(s)$ and the bandwidth $f_{BW}$ are much improved in the BDI structure because the inputimpedience of the input gate MPi is ${1}/{(1+A)g_m}$ by using an actively compensated input structure.

**2) Noise Performance of BDI Input Stage:**

The noise of the readout input stage should be significantly smaller than the noise produced by the IR detector and the radiation shot noise. An IR PV sensor can be modeled as a current source $I_s$ with the shunt capacitor $C_D$ and the shunt resistance $R_D$. The input referred noise of the BDI input stage as shown in Fig. 3.9 is given by the superposition of the OP input gate referred noise voltages $e_{n1}^2$ and the noise voltages of the input MOS devices $e_{n2}^2$. The input referred noise current generated by $e_{n1}^2$ is

$$i_{n1}^2 = \frac{e_{n1}^2}{R_D^2} \tag{3.6}$$

The input referred noise current generated by $e_{n2}^2$ is

$$i_{n2}^2 = g_{mi}^2 e_{n2}^2 \left( \frac{1/(1+A)g_{mi}}{R_D + 1/(1+A)g_{mi}} \right)^2 \simeq \frac{e_{n2}^2/(1+A)^2}{R_D} = \frac{e_{n2}^2}{(1+A)^2 R_D^2} \tag{3.7}$$

Because $R_D \gg 1/(1+A)g_{mi}$, the total input referred noise current of the input stage is given by summing Eqs. (3.6) and (3.7) as :

$$i_{n,total}{}^2 = i_{n1}{}^2 + i_{n2}{}^2 = \frac{e_{n1}{}^2}{R_D{}^2} + \frac{e_{n2}{}^2}{(1+A)^2 R_D{}^2} \approx \frac{e_{n1}{}^2}{R_D{}^2} \tag{3.8}$$

The gate referred noise voltage source of a MOSFET can be represented as [22]

$$e_n{}^2 \approx \frac{8}{3}\frac{kT}{g_m}\Delta f \tag{3.9}$$

Thus $i_{n,BDI}^2$ is inversely proportional to the gate transconductiance $g_m$.

**3) The Reduction of Dark Current, Shot Noise and Thermal Noise:**

The dark current is increased with the reverse-biased voltage Vr because higher electric field is generated in the pn junction depletion region when the reverse-biased voltage is higher. For the same reasons, the photocurrent is also increased with the reverse-biased voltage.

Thus, biasing the photodiode at or near zero voltage can achieve lower dark current and at the same time largely increase the shunt resistance, $R_D$ of the photodiode. Larger resistance of $R_D$ can reduce the thermal noise of the photodiode and input referred noise current caused by OP input gate and the input MOS devices. The thermal noise current of the photodiode is caused by shunt resistance, $R_D$ and the power spectral density of the thermal noise current is

$$I_T^2 = \frac{4kT}{R_D} \tag{3.10}$$

From the equation 3.9 and 3.10, larger resistance of $R_D$ also reduces the thermal noise current of the photodiode and the input referred noise current caused by OP input gate referred noise voltages $e_{n1}^2$ and the noise voltages of the input MOS devices $e_{n2}^2$.

The noise current of shot noise of the photodiode can be determined empirically and is give by

$$I_{shot}^2 = 2q(I_{ph} + I_{dark}) \tag{3.11}$$

When the radiation of the light is in very low intensity, the dark current $I_{dark}$ contributes to the total shot noise and gives rise to random fluctuations of the output current. The reduction of the dark current can also reduce the shot noise in very low intensity of the radiation of the light. Thus, biasing the photodiode at or near voltage can achieve lower dark current, lower shot noise [23] and higher signal-to noise ratio (SNR) as compared with that at higher reverse-biased voltage.

In addition to high injection efficiency, good noise performance of BDI input stage, the reduction of dark current, shot noise and thermal noise, low good bias stability is inherent in the BDI structure. The detectors should be kept near zero bias to prevent the generation of $1/f$ noise and maintain linear and uniform response. The virtual short-circuit property

between the two differential-pair OP input nodes in the BDI structure makes the detectors biased at near zero bias.

The integration capacitance is composed of the capacitance of Cint1 and the optional capacitance of Cint2, Cint3 and Cint4 with three transistors switch Mrs1, Mrs2 and Mrs3. The optional capacitors is used to achieve the required integration capacitor charge capacity and to prevent saturation when the incident light is strong and the integration time is long such as the application of still imager in the environment of strong light. This leads to increase the dynamic range of the incident light. The capacitance of the integration capacitors with the corresponding integration capacitor charge capacities given in Table 3.3.

The photocurrent generated from the selected pixel is integrated on the integration capacitor after the reset operation when Mrst is open. After the integration, the integrated voltage is transferred through the source follower composed of Mp1, Mp2 and Mp3. At the end of the integration, the reset switch Mrst is turned on and the voltage at the integrating capacitor is also transferred through the source follower to perform the operation of double delta sampling (DDS).

The source follower is composed of the two PMOSFETs of Mp1 and Mp2 with their N-well substrates connected to the sources. Thus the gain of the source follower can be designed to be nearly 1 without the gain loss due to the body effect. The output of the source follower is connected to column sampling circuits in the next stage of the improved double delta sampling (DDS) operation circuit.

### 3.3.1.2 Improved Double Delta Sampling (DDS) Circuit

The improved DDS operation circuit is shown in Fig. 3.10. The device parameters in the circuit diagram of the improved DDS circuit are given in Table 3.4. The improved DDS circuit is composed of column sampling circuit and output CDS circuit. The column sampling

circuit is used in each column whereas the output CDS circuit is shared by all the columns. In the column sampling circuit as shown in Fig. 3.10, the NMOS (PMOS) devices of MSn (MSp) and MRn (MRp) controlled by the signals of SHSn (SHSp) and SHRn (SHRp), respectively, are sampling switches whereas Mvcen (Mvcep) controlled by Vcen (Vcep) is the equalization switch. The signals generated by the integration of photocurrent and the reset signal transferred through the source follower Mp1/Mp2/MP3 are sampled by the two CMOS switches devices, MSn/MSp and MRn/MRp, respectively. Both the effects of clock feedthrough and channel charge injection resulted from the sampling operation of MS and MR in the original DDS circuit [24] will degrade the performance of signal readout. In the improved DDS circuit of Fig. 3.10, the effect of signal-dependent channel charge injection caused by MS and MR during the falling edges of SHS and SHR is reduced by using the CMOS transmission gate switch. The size of MSn (MRn) and MSp (MRp) is designed to be the same unit size because only the channel charges injected to the source regions of MS and MR are to be compensated by those to both drain and source regions of Ma and Mb, respectively.

The signals after the sampling are held at the nodes of A and B until they are readout to the output CDS circuit when the column switches Mn15 and Mn16 are on. Since the column readout sampling is performed simultaneously in each column and the sampled column signals are readout to the output CDS circuit successively, the signal from the last column is held for the longest time that is almost equal to the integration time of the photocurrent. The held signal voltages at the last column will be decreased by the leakage current $I_{leak}$ at the nodes of A and B, the gain $G_{PGA}$ of the programmable gain amplifier (PGA) before the A/D converter with the resolution of 8 bits, the node capacitances at the nodes of A and B $C_{hold}$, and the integration time of photocurrent $T_{int}$. The equation can be represented as

$$(C_{gate} + 0.31pF)V_{1LSB} = G_{PGA}(I_{leak} \times T_{read}) \tag{3.10}$$

The value of $V_{1LSB}$ and $G_{PGA}$ are $1.5V/2^8 = 5.9mV$ and 1. The values of $C_{gate}$ and $I_{leak}$ are determined from the process parameter.

The photosignal (reset) voltage is sampled to the gate of Mn1 (Mn2) of the second source follower composed of Mn3, Mn4, Mn7and Mn8(Mn5, Mn6, Mn9 and Mn10) and sent out to the output CDS circuit through the column select switches Mn15 (Mn16), as shown on Fig. 3.11. The second source follower is composed of NMOS devices because PMOS devices are used in the first source follower. Thus the voltage dynamic range at the output of the second source follower is not reduced by the level shifting of threshold voltage. In the conventional N-well CMOS process, the substrates of all NMOS devices must be connected to the ground together due to the use of a single P-well. Under this circumstance, the source follower composed of NMOS devices suffers from the gain attenuation due to the body effect. If the advanced process, like the 0.25 μm 1P5M CMOS technology, can be used in the design of the chip, the use of the mask of deep N-well, which is beneath the P-well, can solve this problem. In other words, the potential of the P-well at the top of deep N-well can be set to any value. Thus the substrates of Mn1 and Mn2 can be connected to their source and the gain in the NMOS source follower is not attenuated by the body effect. The dynamic range of the output voltage is almost equal to that of the voltage at the integrating capacitor although two types of the source follower are used in the design of column readout circuit.

The cascoded current source of the NMOS source follower is used in each column of the column sampling circuit instead of being shared by all columns in column sampling circuit and divided into two subordinate current sources. Therefore, no voltage drop on NMOS column switch and the linearity can be improved. One current source, Mn3 and Mn4 (Mn5 and Mn6), sink small current and the other, Mn7 and Mn8 (Mn9 and Mn10), sink large current for quickly charging the loading capacitor. When the column is selected, the current source composed of Mn7 and Mn8 (Mn9 and Mn10) start to work. The device Mn7 (Mn9) is

biased by vnb2 by turning on the switch Mn13 (Mn14) and turning off the switch Mn11 (Mn12). When the column is deselected, the current source composed of Mn7 and Mn8 (Mn9 and Mn10) is shut off by turning off the switch Mn13 (Mn14) and turning on the switch Mn11 (Mn12). The equalization of both photosignal path and reset signal path controlled by Vce is performed after the readout of the held voltage. The equalized voltage at the two nodes of A and B is then readout to the output CDS circuit.

In the output CDS circuit, the NMOS devices Mn17 (Mn18) controlled by the signal Clamp is to clamp the voltage at the gate of Mp7 (Mp8) in the output source follower Mp7, Mp9 and Mp10 (Mp8, Mp11 and Mp12) to Vb5. The capacitors of 2.9 pF are used to perform the operation of correlated double sampling (CDS). The detailed discussion in CDS operation and capacitor is shown in Fig. 3.12. The equivalent circuit and the operation theorem are shown in the left side of Fig. 3.12. C1 and C2 are the parasitical capacitance of the two sides of the Ccds capacitor. Cgd and Cgs are the gate capacitance of Mp7 (Mp8). Ceq is the equivalent capacitance of C2, Cgd and Cgs. The equation of CDS operation can be represented as

$$\Delta V_3 = \Delta V_2 \times \frac{C_{cds}}{C_{cds} + C_{eq}} \tag{3.11}$$

The double poly structure is used as Ccds capacitor and the cross-sectional view of layout is shown in the right side of Fig. 3.12. C2 is parasitical capacitance from top poly to metal 3 and C1 is parasitical capacitance from bottom poly to p substrate. However, the capacitance of C1 is too large to degrade the performance of CDS operation. The ratio of the capacitance of Ccds to C1 is about 1:0.4. If C1 is connected with the input the source follower, the value of $\Delta V_3$ will be largely reduced. Therefore, the top poly of Ccds capacitor is connected with the input of the source follower.

### 3.3.2 Digital Control Circuit

The control signals of the readout circuit come from the digital control circuits. Fig 3.6 shows the schematic of the digital control circuit. The digital circuit is mainly composed of flip-flops. The flip-flops are triggered by positive-edge clock signal. When the voltage level of Fsyn signal is from low to high, the startup pulse is generated and passed on through serial flip-flops. And then all the control signals are generated. When the last pulse signal, oi64, is at high voltage level, it turns off the digital and waits for the next startup pulse to be triggered by Fsyn signal.

The major timing diagram of control signals is shown in Fig. 3.7. The Fsyn signal is inputed outside the board. And the Lsyn signal used for synchronization with output data is generated by digital circuit and sends out to the board. Firstly, the SHS signal is high to sample the integrated signals VS to the Chold1 capacitor from all pixels and then the Reset signal is high to reset the voltage at the integrating capacitor to 0V. After that, the control signal of SHR is on to sample the reset signal VR to the Chold2 capacitor. Two clock periods later, the reset signal is on to wait for Fsyn signal to turn it off to integrate the capacitor. The duration of reset time is kept long enough to eliminate the amount of residual charges due to incomplete reset. That is, the amount of KTC noise generated by the trapping of the switch thermal noise in the integration-reset function on the integration capacitor is the same in VS and VR if the settling time of the voltage on the integration capacitor during the reset operation is shorter than the reset time [24]. The clamp signal in the output CDS circuit is then turned on to clamp the gate voltages of Mp7 and Mp8 to Vb5. Then, oixx signal is on to transfer the signal from the column sampling circuit to the output CDS circuit. Finally, Clamp is off and Vce is on, the voltage at both capacitors, Chold1 and Chold2, becomes (VS+VR)/2. If no loss in the stored charges of the capacitor, then the voltage change at the Ccds capacitor is transferred to the output node of the output source follower composed of Mp7 and Mp9 and Mp10(Mp8, Mp11 and Mp12) as shown in Fig. 3.5. Thus we have [19]

$$\text{Vout_s} \cong \frac{\text{VR1} - \text{VS1}}{2} + \text{Vb5} + V_{\text{cf,Mvce}} + V_{\text{SG,Mp7}} \quad (3.12)$$

$$\text{Vout_r} \cong \frac{\text{VS1} - \text{VR1}}{2} + \text{Vb5} + V_{\text{cf,Mvce}} + V_{\text{SG,Mp8}} \quad (3.13)$$

where $V_{\text{cf,Mvce}}$ is the effect of clock feedthrough on the voltage held by capacitors Chold1 and Chold2 in Fig. 3.5 when the MOSFET of Mvce is on and $V_{\text{SG,Mp7}}$ ( $V_{\text{SG,Mp8}}$ ) is the voltage drop between source and gate of Mp7(Mp8). As may be seen from (3.12) and (3.13), the CDS operation is realized in the output CDS circuit. The fixed pattern noise in the NMOS source follower of column sampling circuit can be reduced by this CDS operation. The two output signals are sent out and subtracted each other by the subtraction circuit in the off-chip data acquisition (DAQ) card. Thus the complete operation of the double delta sampling circuit is realized. The fixed pattern noise caused in the PMOS source follower composed of Mp5, Mp6 and Mp7 in Fig. 3.5 can be reduced by the subtraction in DAQ card. The effect of clock feedthrough by switching the signal of Vce to equalize the voltages at the two gates of Mn1 and Mn2 can also be reduced from the subtraction. The final result after the subtraction of DAQ card can be written as [19]

$$\text{Vout_r} - \text{Vout_s} \cong \text{VS1} - \text{VR1} + V_{\text{SG,Mp8}} - V_{\text{SG,Mp7}} \quad (3.14)$$

By enlarging the size of the output source follower, the mismatch of $V_{\text{SG}}$ can be reduced.

## 3.4 SIMULATION RESULTS

The simulations are performed at 298K based on the SPICE device parameters of TSMC 0.35 $\mu$m 2P4M N-well CMOS process. The simulation result of the integration voltage Vint waveforms on integration capacitor with different input current is shown in Fig. 3.15. The input current signals are from 3.5nA to 350nA, the integration capacitance is 20pF, and the integration time is 80us. As shown in Fig. 3.15, the charging rate is proportional to the input

current. The simulation results of the voltage difference between Vout_r and Vout_s of the output CDS circuit with different input current are shown in Fig. 3.16. The linearity of the voltage difference between Vout_r and Vout_s is shown in Fig. 3.17. The small current simulation with four input currents from 10nA to 100pA, 0.3125pF integration capacitor, integration tome 90us and 4MHz clock frequency is shown in Fig. 3.18. Fig. 3.19 shows the simulation waveforms of two chips combined with 5pF integration capacitor, integration time 18us and 4MHz clock frequency. Six test currents are respectively inputted from cell00 to cell05 and from cell58 to cell63 in chip2. The output data of chip2 are sent out to chip1. The simulation readout speed can reach 4 MHz under 14.5 mW power dissipation at a 30 pF output loading and 3.3 V power supply with 1x128 format. The integration time of the readout chip is tunable. It can be controlled by the clock frequency of the digital control signal. When the integration time is different, the detecting photo current range will be changed at the same time. The linearity of the readout circuit is greater than 99.99% and the maximum output swing is about 1.6 V. The frame rate of the maximum 1 x 128 readout circuit is 30k frames/sec. The tunable integration time range is from 36.92us to 0.385us when the frame rate is at 26k/s. The post simulated performances and operation conditions of the readout chip are summarized in Table 3.5.

| Device | W/L (um/um) |
|---|---|
| Mbu | 0.5/0.35 |
| Mrs1 | 0.4/0.35 |
| Mrs2 | 0.8/0.35 |
| Mrs3 | 1.6/0.35 |
| Mr3 | 2.4/0.35 |
| Mp5 | 3/1.2 |
| Mp6 | 5/0.35 (m=2) |
| Mp7 | 5/0.35 |
| Cint1 | 0.31 pF |
| Cint2 | 0.93 pF |
| Cint3 | 3.75 pF |
| Cint4 | 15 pF |
| PVsub | 2.5V |
| Vpb1 | 2.4V |
| Vpb2 | 2.3V |

Table 3.1 The device parameters of the unit-cell BDI input stage.

| Device | W/L (um/um) |
|---|---|
| Mp1 | 1.5/0.5 (m=2) |
| Mp2 | 1/0.5 |
| Mp3 | 1/0.5 |
| Mn1 | 0.8/1 |
| Mn2 | 0.8/1 |
| Vb1 | 2.5V |

Table 3.2 The device parameters in the circuit diagram of the gain stage.

| Integration Capacitor Charge Capacity | Typ. | unit |
| --- | --- | --- |
| 0.31pF | 4 million | e |
| 1.2pF | 16 million | e |
| 5pF | 64 million | e |
| 20pF | 256 million | e |

Table 3.3 The integration capacitor charge capacity.

| Device | W/L (um/um) |
| --- | --- |
| MSn | 0.4/0.35 |
| MSp | 0.4/0.35 |
| Mvcen | 0.4/0.35 |
| Mvcep | 0.4/0.35 |
| Mn1 | 16/0.35 (m=2) |
| Mn3 | 1.6/1.1 |
| Mn4 | 0.8/1.1 |
| Mn7 | 10/0.35 (m=3) |
| Mn8 | 5/0.35 (m=3) |
| Mn11 | 0.8/0.35 |
| Mn13 | 0.8/0.35 |
| Mnp10 | 8/0.35 (m=30) |
| Mp9 | 16/0.35 (m=30) |
| Mp7 | 16/0.35 (m=16) |
| Mn17 | 1.2/0.35 |
| Vnb2 | 0.9 V |
| Vnb1 | 0.7 V |
| Vpb2 | 2.3 V |
| Vpb1 | 2.4 V |
| C1 C2 | 0.12 pF |
| C3 C4 | 0.5 pF |

Table 3.4 The device parameters of improved double delta sampling (DDS) circuit.

| Technology | 0.35μm 2P4M N-well CMOS |
|---|---|
| Power Supply | 3.3 V |
| Operating Temperature | 298 K |
| Input Current | 100 pA ~ 350 nA |
| Array Size | 1 x 64 x 2 |
| Pixel Pitch | 100 μm |
| Maximum Output Swing | 1.6 V |
| Maximum Readout Speed | 10 MHz |
| Maximum Frame Rate (@readout speed 4 MHz) | 30k frames / sec |
| Integration time tunable range (@frame rate 26k/s) | 38.92us ~ 0.935us |
| Linearity | 99.99% |
| Chip Area | 1.63 mm x 7.4 mm |
| Total Power Dissipation | 14.5 mW |

Table 3.5 The post simulated performances and operation conditions of the readout chip.

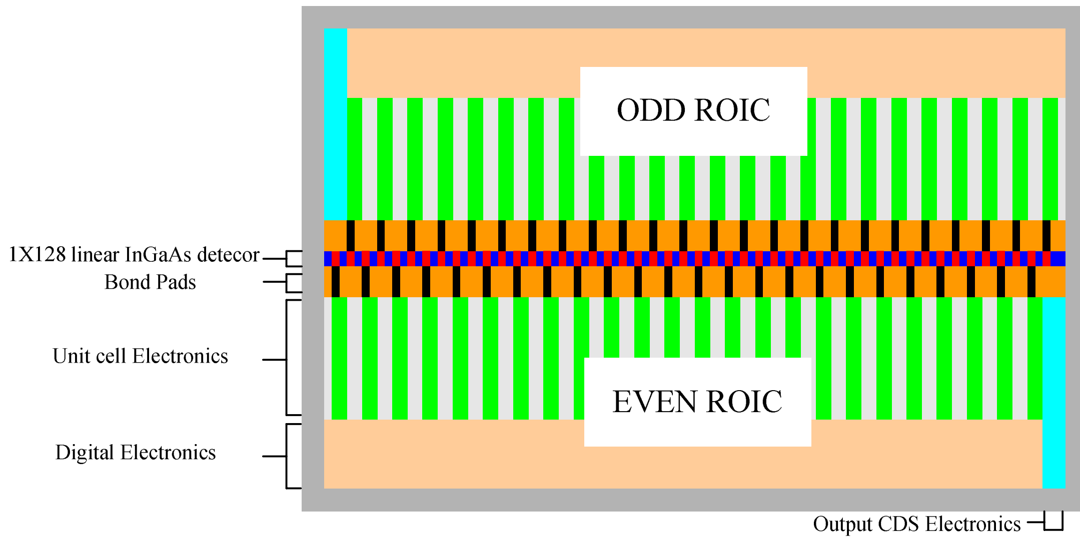



Fig. 3.1 1x128 array configuration.

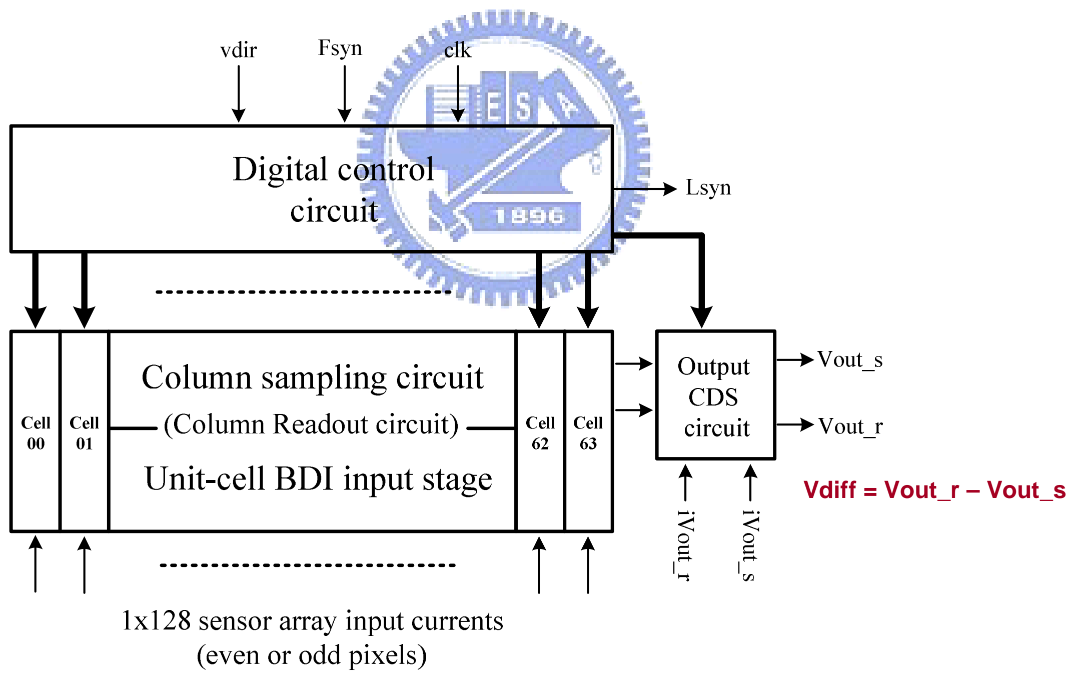



Fig. 3.2 The block diagram of the architecture of the IR readout chip.

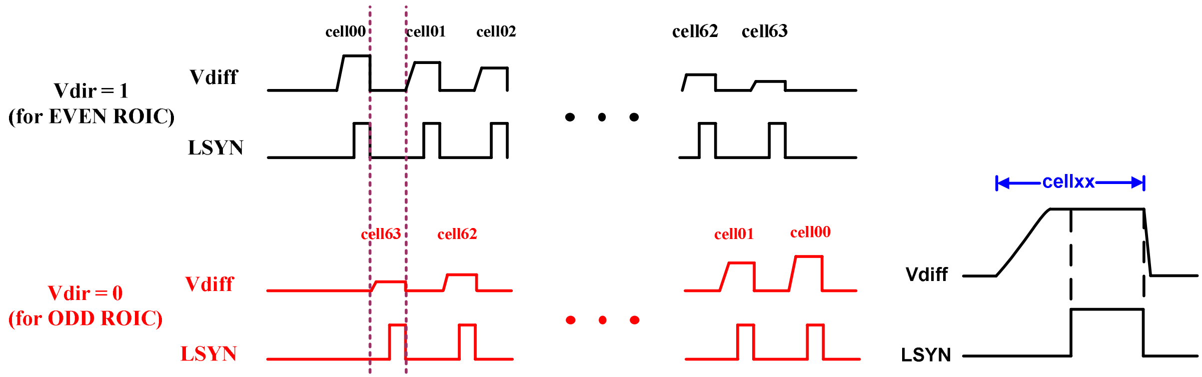



Fig. 3.3 Control of output priority and serial interlace output.

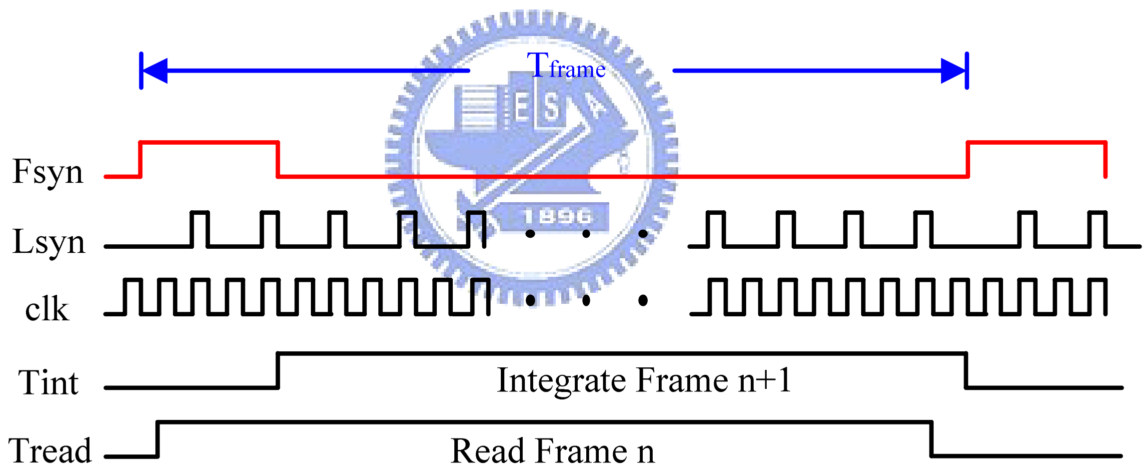



Fig. 3.4 Independent integration time control.

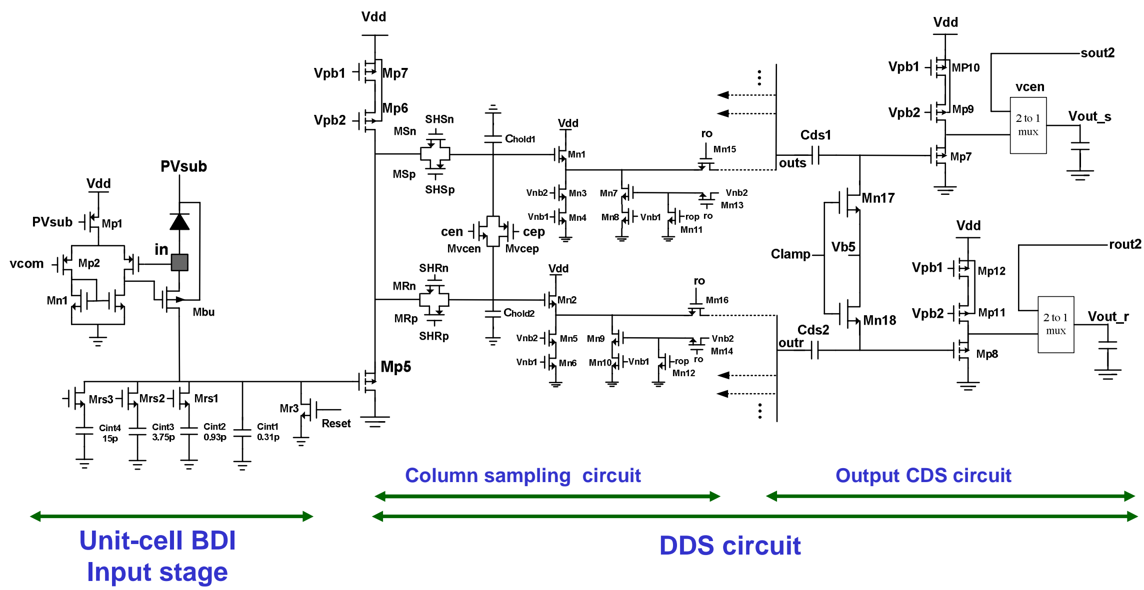
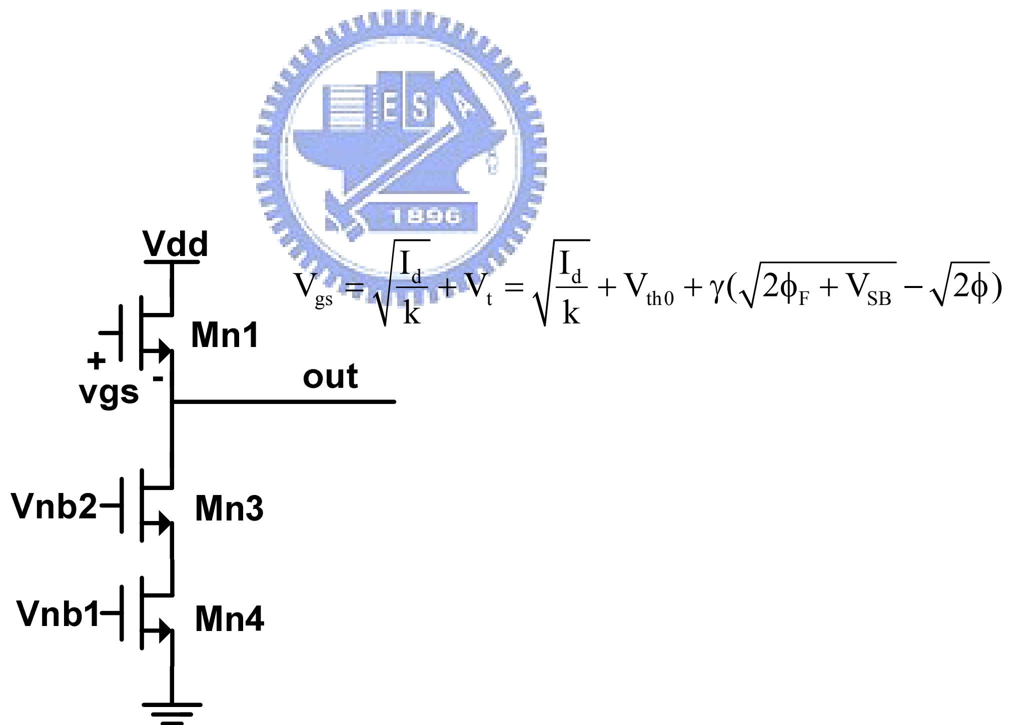



Fig. 3.5 The schematic of the analog circuit.




$$V_{gs} = \sqrt{\frac{I_d}{k}} + V_t = \sqrt{\frac{I_d}{k}} + V_{th0} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi})$$

Fig. 3.6 The NMOS source follower.

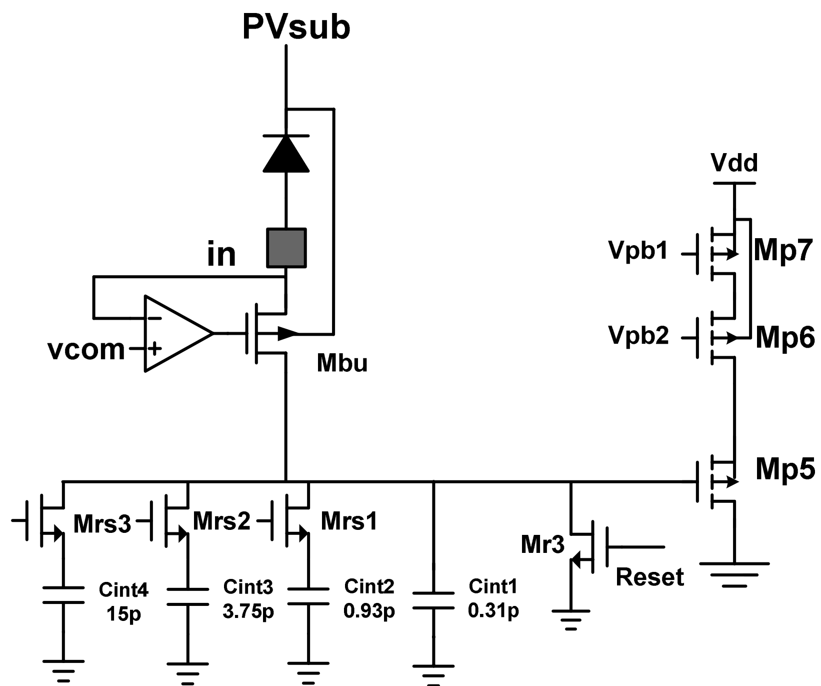



Fig. 3.7 The unit-cell BDI input stage.

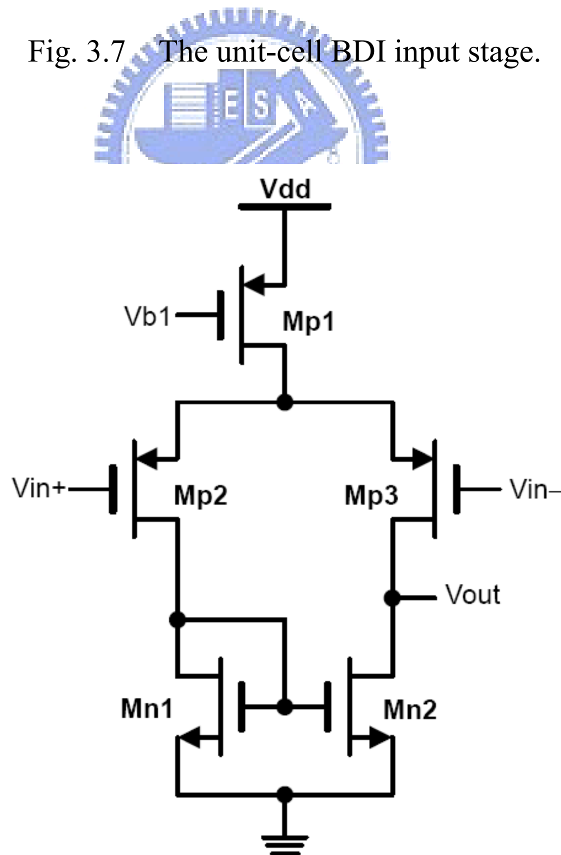



Fig. 3.8 The circuit diagram of the gain stage.

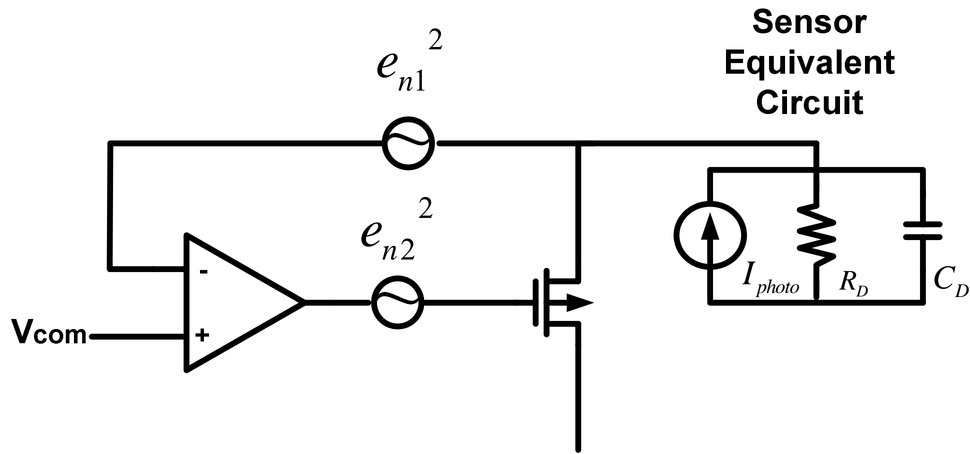



Fig. 3.9 The noise model and equivalent circuit of buffer direct-injection (BDI) input stage.

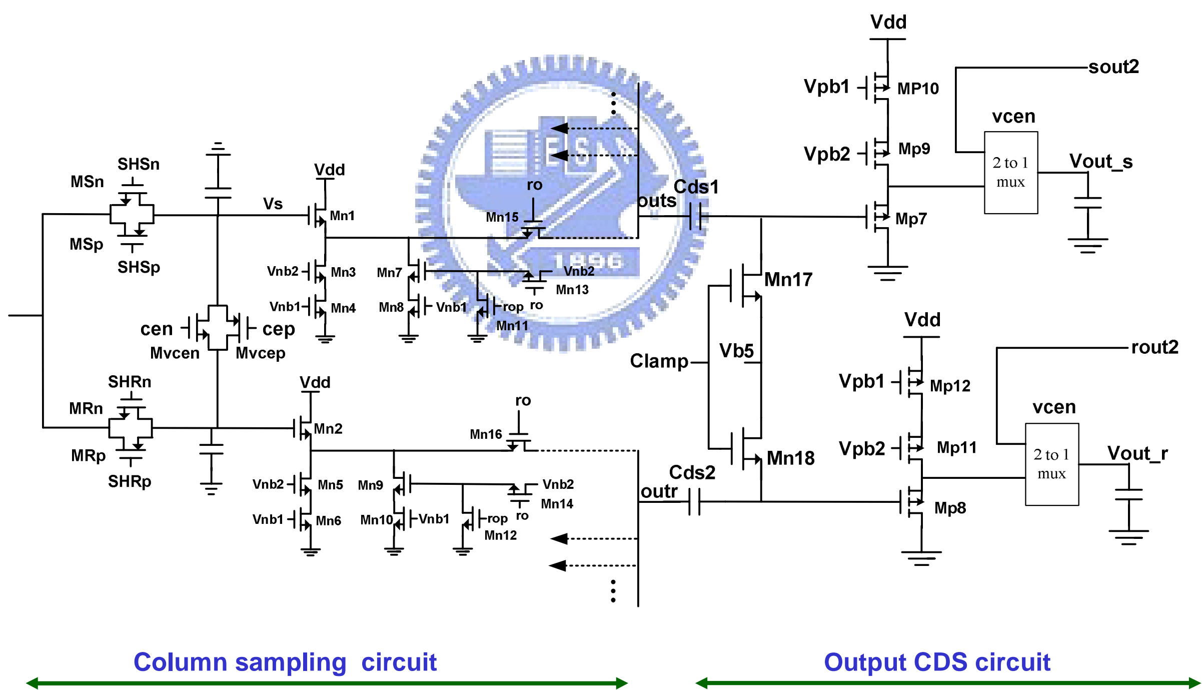



Fig. 3.10 The improved double delta sampling (DDS) circuit.

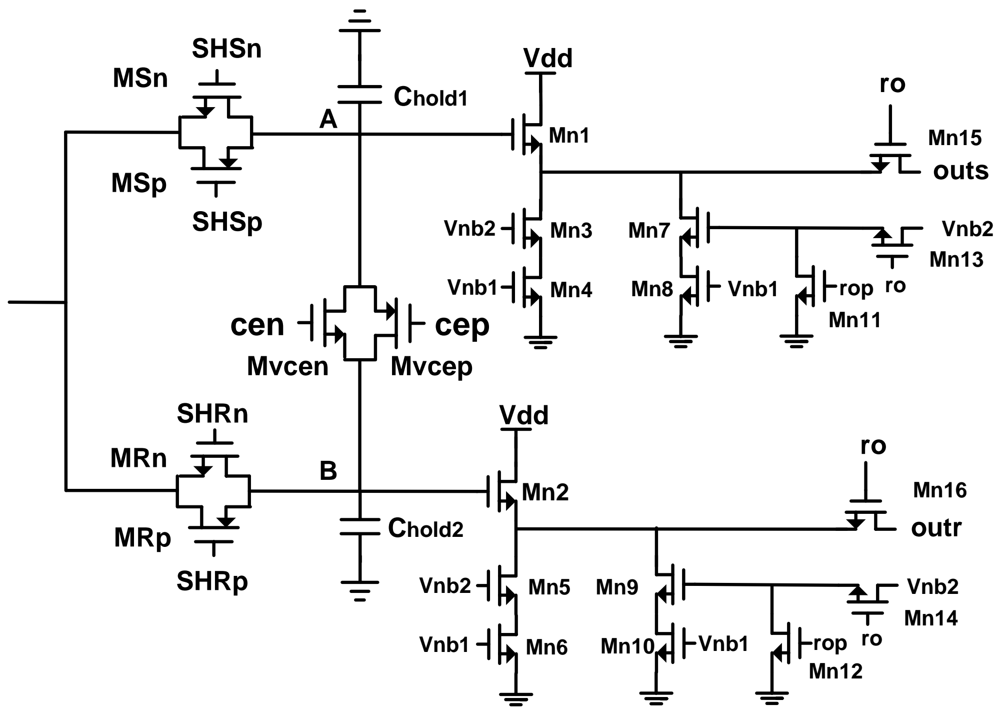
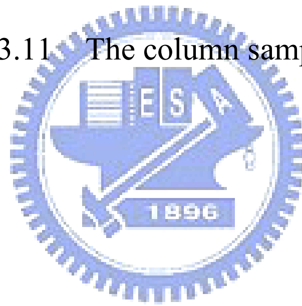
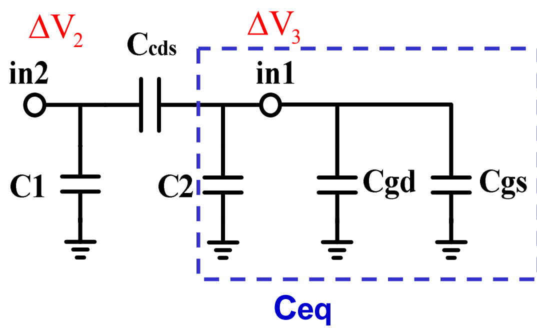



Fig. 3.11 The column sampling circuit.






$$\Delta V_3 = \Delta V_2 \times \frac{C_{cds}}{C_{cds} + C_{eq}}$$

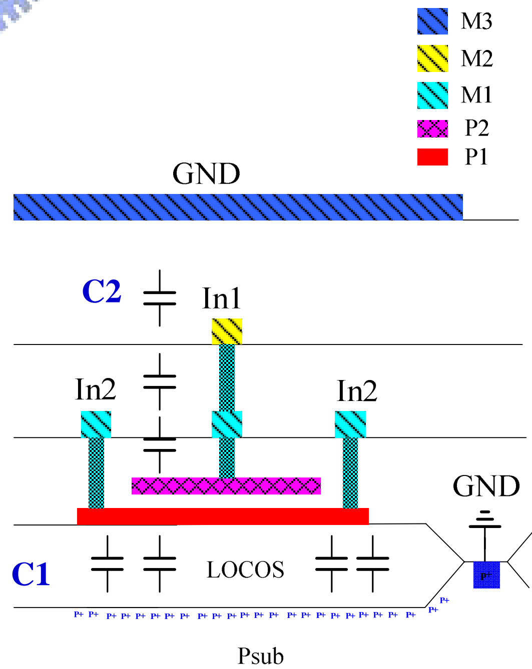



Fig. 3.12 The DDS operation and cross-sectional view of double poly capacitor.

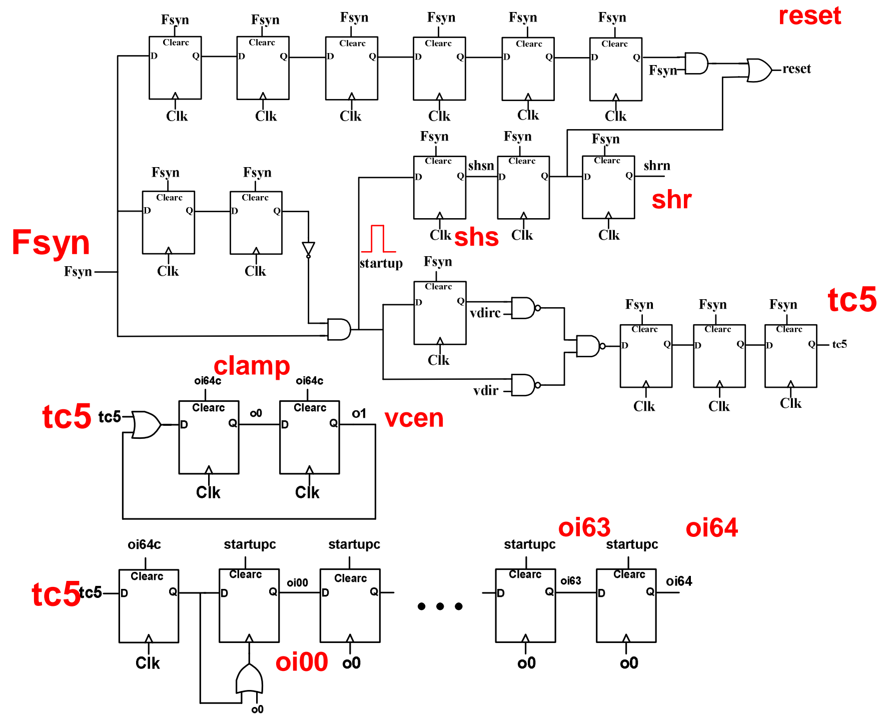



Fig. 3.13 The block diagram of the digital control circuit.

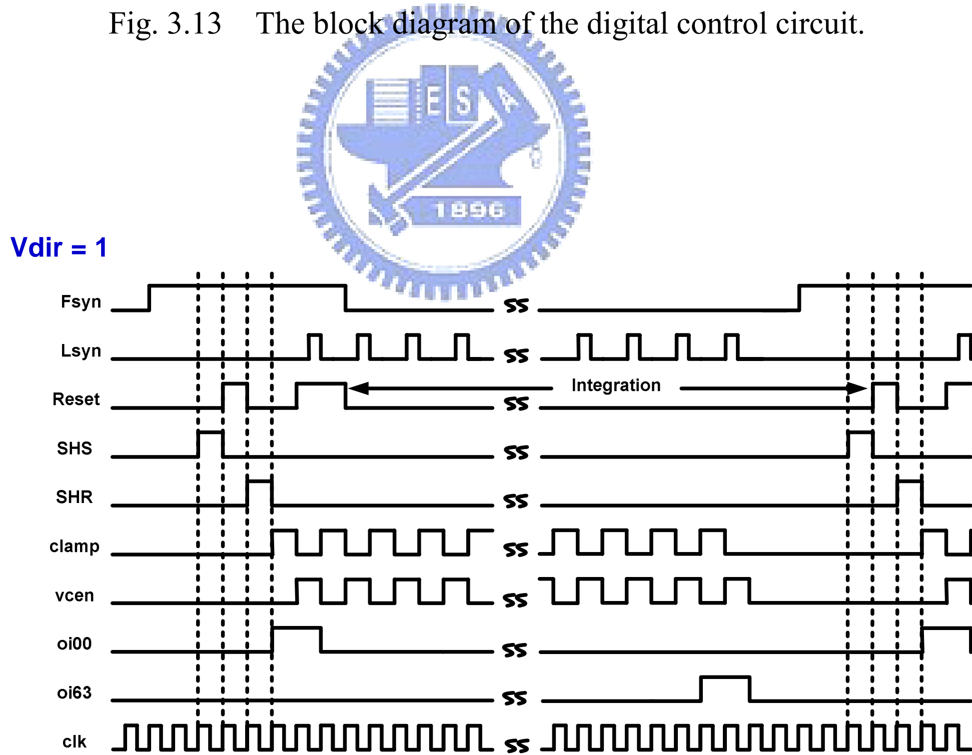



Fig. 3.14 The major timing diagram of the digital control circuit.

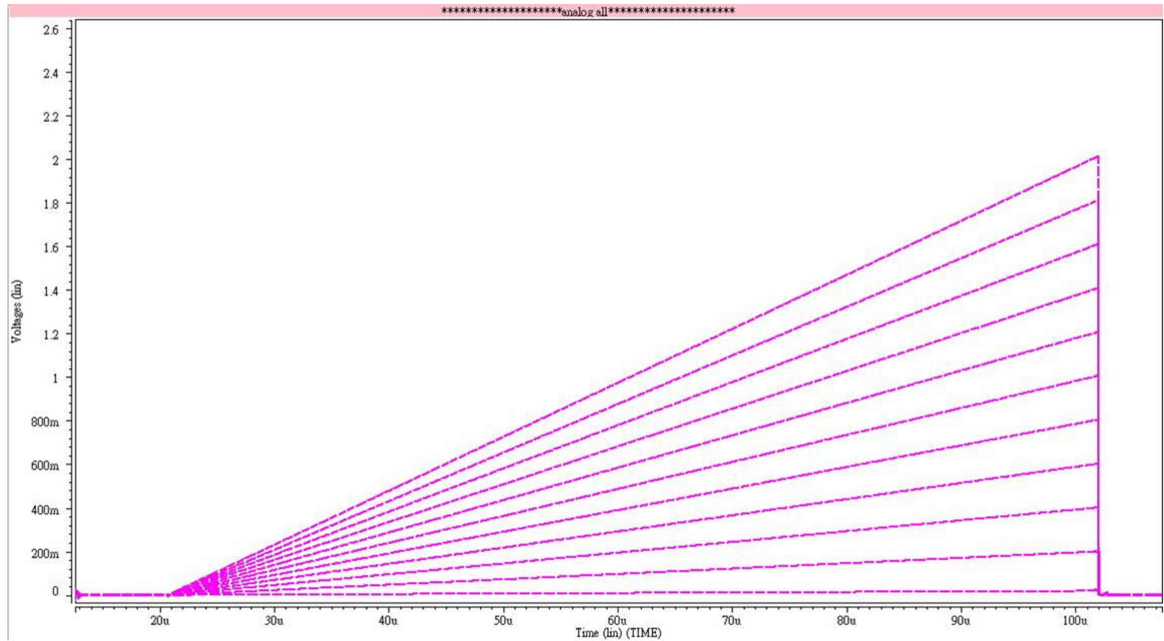
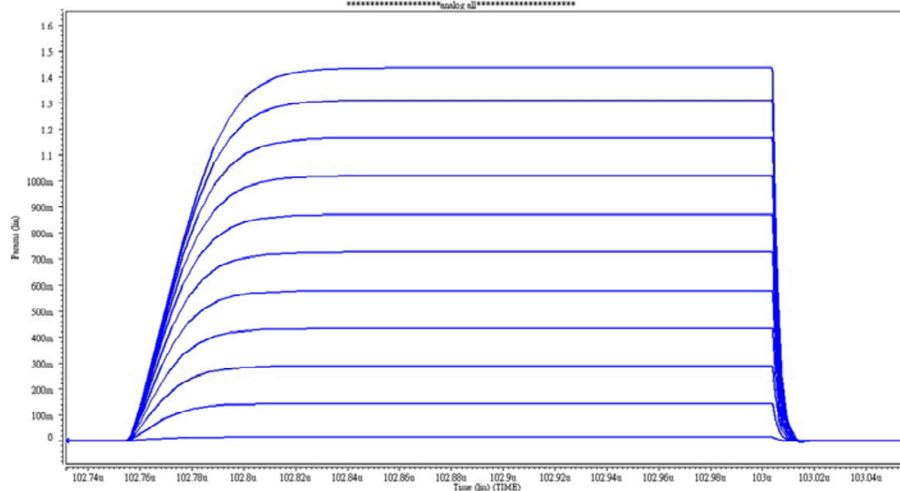



Fig. 3.15 The post-simulated waveforms of Vint on 20pF integration capacitor with input currents from 3.5nA to 350nA, integration time 80us and 4MHz clock frequency.



| Ip(nA) | Out(volt) |
|---|---|
| 350 | 1.44 |
| 315 | 1.31 |
| 280 | 1.17 |
| 245 | 1.02 |
| 210 | 0.871 |
| 175 | 0.724 |
| 140 | 0.578 |
| 105 | 0.431 |
| 70 | 0.287 |
| 35 | 0.142 |
| 3.5 | 0.0142 |

Fig. 3.16 The post-simulated waveforms of the voltage difference between Vout_r and Vout_s with input currents from 3.5nA to 350nA, integration time 80us and 4MHz clock frequency.

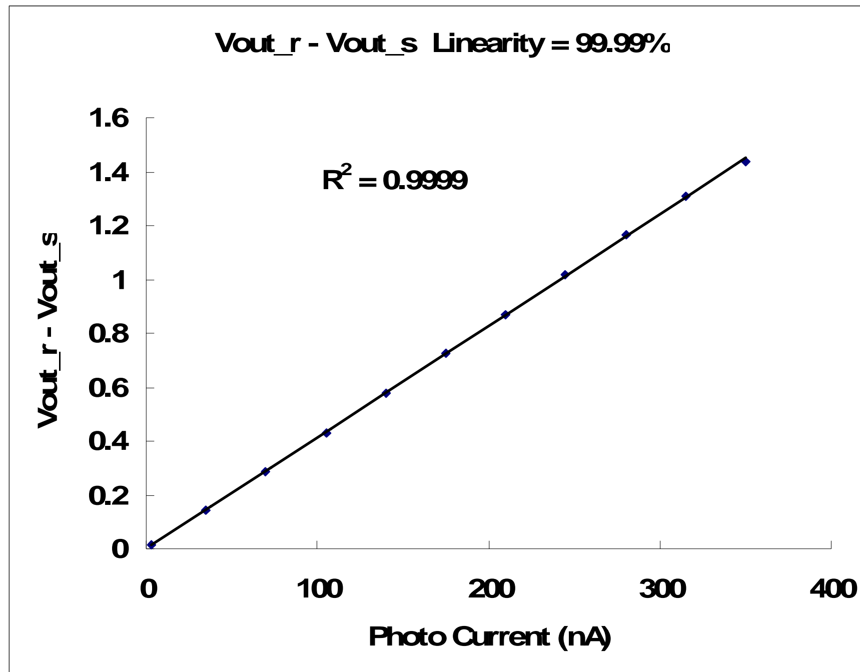



Fig. 3.17 Vout_r－Vout_s linearity with 20pF integration capacitor, integration time 80us and 4MHz clock frequency.

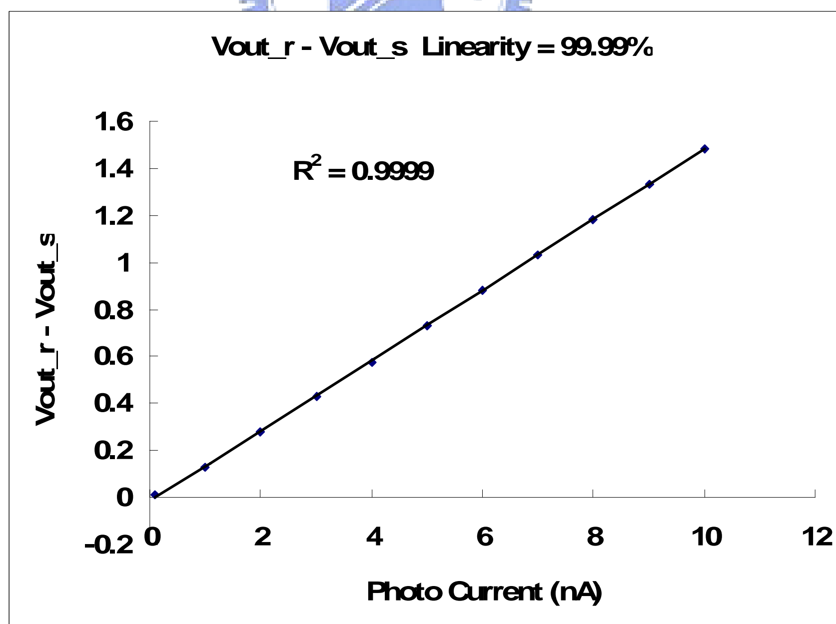



Fig. 3.18 Vout_r－Vout_s linearity (post simulation) with input currents from 10nA to 100pA, 0.3pF integration capacitor, integration time 90us and 4MHz clock frequency.

**Chip1 In00~In05: 300n, 200n, 100n, 50n, 25n, 5n (A)**
**Chip2 In58~In63: 300n, 200n, 100n, 50n, 25n, 5n (A)**

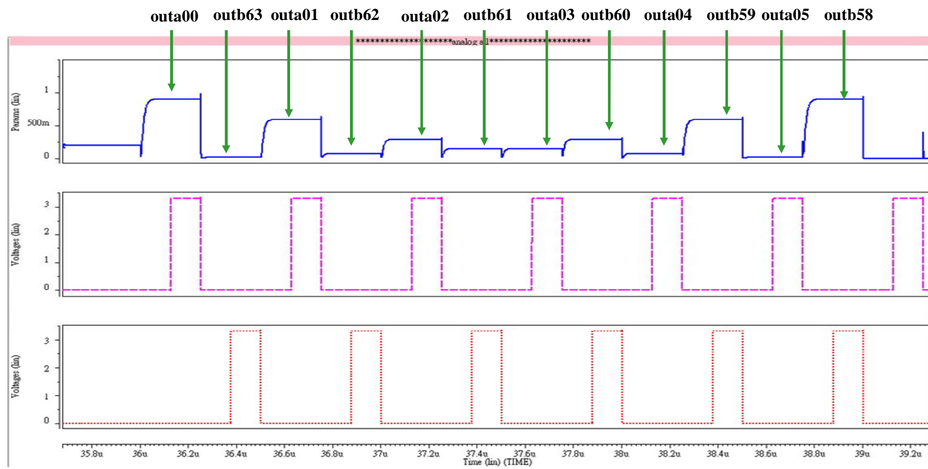



Fig. 3.19 Two chips combined together with 5pF integration capacitor, integration time 18us and 4MHz clock frequency.

# CHAPTER 4

# EXPERIMENTAL RESULTS

## 4.1 LAYOUT DESCRIPTIONS

An experimental chip has been designed and fabricated to verify the function and performance of the 1 x 64 readout circuit by using TSMC 0.35μm 2P4M N-well CMOS technology. The total chip size is 1.63 mm x 7.4 mm. The layout and the photograph of the 1x64 readout chip are shown in Fig 4.1 and Fig 4.2. It is composed of Column Sampling Circuit, Signal Bus, Digital Circuit and Output CDS Circuit. Column Sampling Circuit has 64 unit cells. Each cell circuit contains BDI input stage and column sampling circuit. The odd or even pixels of IR detectors are connected to the input pads of the Column Sampling Circuit by bonding wires. And the pitch of each cell is 100um. The Signal Bus is place between Column Sampling Circuit and Digital Circuit. All signals generated from Digital Circuit are sent to Signal Bus and accepted by Column Sampling Circuit. Finally, the processed signals in each cell of Column Sampling Circuit are one by one sent to Output CDS Circuit through differential paths for further process and outputting.

Because of the mixed mode property of this readout chip, some layout techniques are used. A good shielding between digital part and analog part is required to avoid substrate noise coupling. The isolated substrate biases are used to avoid the noise coupling effect from the digital power supply to the substrate. Separated substrate biased DVsub and AVsub for digital and analog part are used to avoid the substrate coupling through the bias metal line. In addition to this, analog power supply AVdd and digital power supply Dvdd should be

separated to avoid the digital noise of DVdd due to the dynamic switching current of logic gates from coupling to the analog part.

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## 4.2 MEASUREMENT ENVIRONMENT

The measurement setup of the fabricated infrared readout chip is shown in Fig. 4.3. The 10MΩ resistor with power supply is used to generate nA test current. The voltage of input node of BDI structure is at fixed value. Adjust the voltage of power supply to the value of fixed voltage at input node of BDI structure and then the test current can be available by adjusting the voltage drop on the 10MΩ resistor. The function generator provides the clock signal to the digital control circuit of the readout chip. The oscilloscope is used to record the output waveforms of the readout chip. The photograph of measurement boards is shown in Fig. 4.4 (a) and (b). In Fig. 4.4 (a), the Power and Bias board use regulators and resistors to generate the powers and the bias voltages to ROIC test board. Fig. 4.4 (b) is the closer view of the photograph of ROIC test board. Two ROIC chips are bonded on PCBs and the outputs of the PCBs are inset to the ROIC test board.

## 4.3 EXPERIMENTAL RESULTS AND DISCUSSIONS

The infrared readout chip is designed to work at 3.3 V power supply. Off-chip testing current sources are used to simulate the photo-current of IR detectors and the experimental results is shown in Figs. 4.5 - 4.9. Fig. 4.5 (a) and (b) are the measured results of different integration time with Cint=5pF and Iin=90nA. The Fsyn signal with different frequency and duty cycle is used to control integration time. In Fig. 4.5 (a), the duty cycle of Fsyn is 10%. When the frequency of Fsyn is changed from 10k/s to 30k/s, the measured differential output, Vout_r – Vout_s, is change from 1.34V to 0.44V. In Fig. 4.5 (b), the frequency of Fsyn is

10k/s. When the duty cycle of Fsyn is changed from 10% to 80%, the measured differential output, Vout_r – Vout_s, is change from 1.38V4 to 0.32V. Fig. 4.6 shows the measured results of pixel47 and pixel55 in the two different output priorities. When the chip is set in different output priority, the sequence of output is in the reverse order, as shown in Fig. 4.6. Fig. 4.7 shows that the outputs in different output priority are interlaced. Lsyn and RLsyn signals in Fig. 4.7 are used for synchronization with output data when the chip is operated in positive and negative outprioty modes. In Fig. 4.7, the red, gray and green lines respectively mean the measured waveforms of Fsyn, Lsyn and RLsyn. When the chip is operated in negative priority, the output data will be delayed one unit time, as compared with the chip in the positive output priority. Fig. 4.8 shows the measured results that two chips are combined together. Two test currents, 50nA and 100nA, are respectively inputted to pixel31 and pixel 32 of the chip in positive priority mode. One test current, 100nA, is inputted to pixel 32 of the chip in negative priority mode. The output data of the chip in negative priority mode is sent to the chip in positive priority and use the shared channel to be outputted. In left side of Fig. 4.8, the red line of the measured waveform is the measured results of differential outputs of the chip in positive priority mode and three input signals are serially outputted. In the right side of Fig. 4.8, Lsyn signal is added to show the synchronization with the output data. Table 4.1 (a), (b) and (c) show the measured results of different gain operation. The same integration time and input current are given to calculate the gain of the differential voltages for the two capacitors. The measured results of Table 4.1 (a), (b) and (c) show that the gain is about 4. Fig. 4.9 (a) and (b) show the measured differential voltage, vout_r - vout_s, versus input current. Fig. 4.9 (a) shows the measured output voltage Vout_r – Vout_s of pixel 15 and pixel 47 versus input test current from 18nA to 360nA. It is shown that the linearity performance of the readout chip is better than 99.9%. Fig. 4.9 (b) shows the measured output voltage Vout_r – Vout_s of pixel 23 versus input test current with different integration capacitor and input current range. In left side of Fig. 4.9 (b), the integration capacitance is 5pF and the input

test current is from 80nA to 4nA. The linearity performance is 99.93%. In the right side of Fig. 4.9 (b), the integration capacitance is 0.3125pF and the input test current is from 10nA to 500pA. The linearity performance is 99.71%. The integration capacitance corresponding to current range is shown in Table 2. The waveform of maximum output swing is shown in Fig. 4.10. The uniformity of ROCI chip with different input currents from 50nA to 100nA is shown in Fig. 4.11. The difference of output value between 1$^{st}$ cell and 64$^{th}$ cell with 100nA input current is 20mV. The reasons of such large difference may be caused by the variations of oxide thickness gradient of integration capacitor and current source of NMOS source follower. Through the verification of simulation, the difference of output value between different cells, 10% variation of current source of NMOS source follower, is less than 0.5mV. So, the variations is mainly caused by the oxide thickness gradient of integration capacitor.

The measured performances and operation conditions of the fabricated readout chip are summarized in Table 4.3. The maximum output swing is 1.6V. The readout speed is 4 MHz and the maximum frame rate is 30k frames/sec. The tunable integration time range is from 36.92us to 0.385us when the frame rate is at 26k/s. The total active chip power consumption is below 14.45mW.

The measured results of the chip are compared with previous design [25], as shown in Table 4.4. It is shown that the linear ROIC has the advantages of larger output swing and higher linearity than previous design [25]. But the disadvantages are higher area and power consumption.

Fsyn = 1kHz  Duty = 10%

| Cint(F) | Iin(nA) | Vdiff(V) |
|---|---|---|
| 20p | 7.5 | 0.28 |
| 5p | 7.5 | 1.12 |

(a)

Fsyn = 4kHz  Duty = 10%

| Cint(F) | Iin(nA) | Vdiff(V) |
|---|---|---|
| 5p | 7.5 | 0.28 |
| 1.2p | 7.5 | 1.12 |

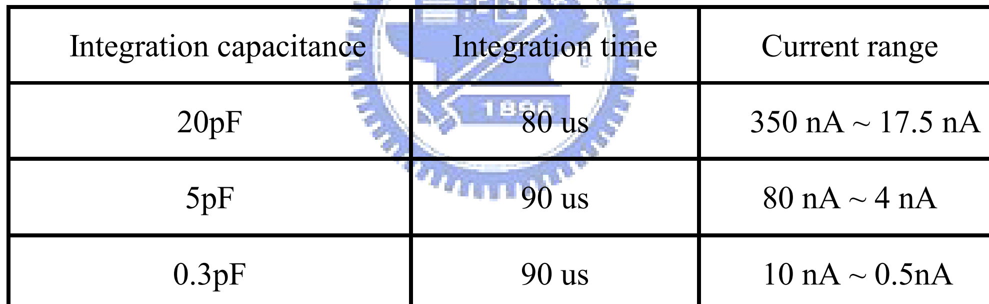
(b)

Fsyn = 4kHz  Duty = 60%

| Cint(F) | Iin(nA) | Vdiff(V) |
|---|---|---|
| 1.2p | 5 | 0.4 |
| 0.3p | 5 | 1.4 |

(c)

Table 4.1  Selectable integration capacitor for different gain operation.



| Integration capacitance | Integration time | Current range |
|---|---|---|
| 20pF | 80 us | 350 nA ~ 17.5 nA |
| 5pF | 90 us | 80 nA ~ 4 nA |
| 0.3pF | 90 us | 10 nA ~ 0.5nA |

Table 4.2  Integration capacitance corresponds to current range.

| | Post Simulated Results | Measured results |
|---|---|---|
| Technology | 0.35μm 2P4M N-well CMOS | |
| Power Supply | 3.3 V | |
| Array Size | 1 x 64 x 2 | |
| Pixel Pitch | 100 μm | |
| Integration capacitance | 0.30fF, 1.2pF, 5pF, 20pF | |
| Input Current | 100 pA ~ 350 nA | 0.5 nA ~ 350 nA |
| Maximum Output Swing | 1.6 V | 1.6 V |
| Maximum Readout Speed | 10 MHz | 10 MHz |
| Maximum Frame Rate (@readout speed 4 MHz) | 30k frames / sec | 30k frames / sec |
| Integration time tunable range (@frame rate 26k/s) | 38.92us ~ 0.935us | 37.42us ~ 0.935us |
| Linearity | 99.99% | 99.73% |
| Total Power Dissipation | 14.5 mW | 14.45 mW |

Table 4.3 The measured performances and operation conditions of the readout chip.

| Input Current | Measured Results | [25] |
|---|---|---|
| Technology | 0.35um | 0.25um |
| Power supply | 3.3 V | 3.3V |
| Temperature | 298k | 298k |
| Array size | 1 x 64 x 2 | 352 x 288 |
| Maximum output swing | 1.6 V | 1.2 V |
| Readout speed | 4 MHz | 3 MHz |
| Linearity | 99.78% | 92% |

Table 4.4 Comparison with previous design.

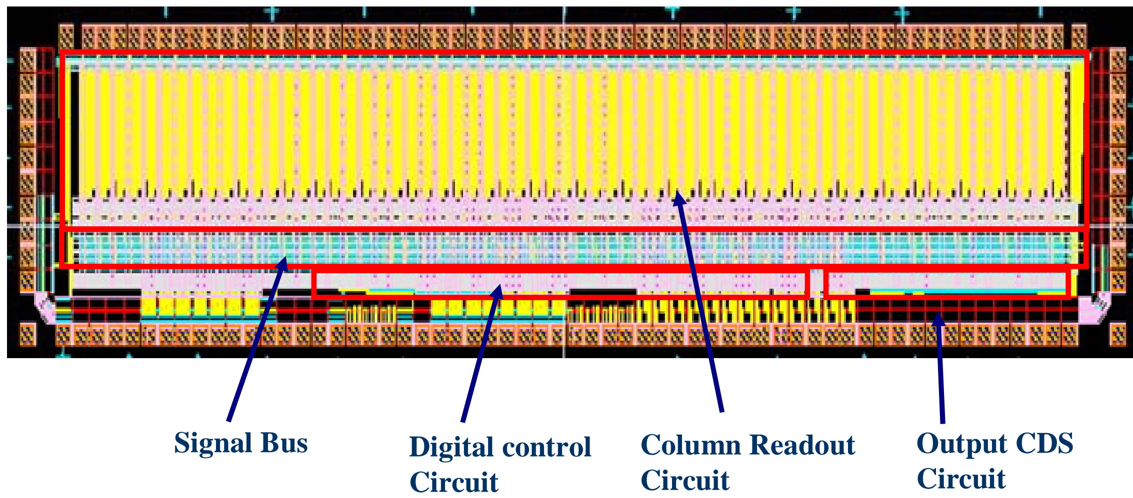



Fig. 4.1 The layout of the 1x64 readout chip.

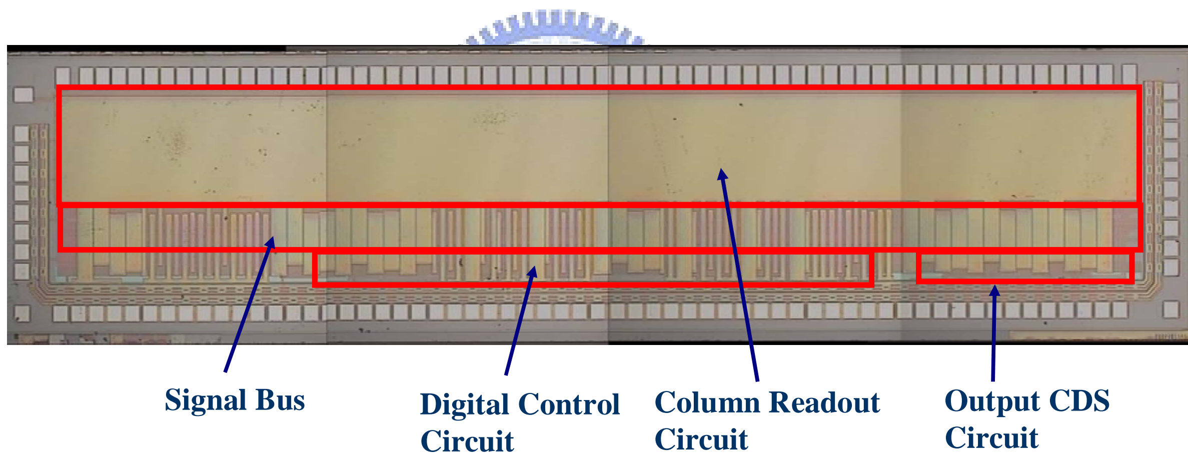



Fig. 4.2 The photograph of the fabricated 1 x 64 readout chip.

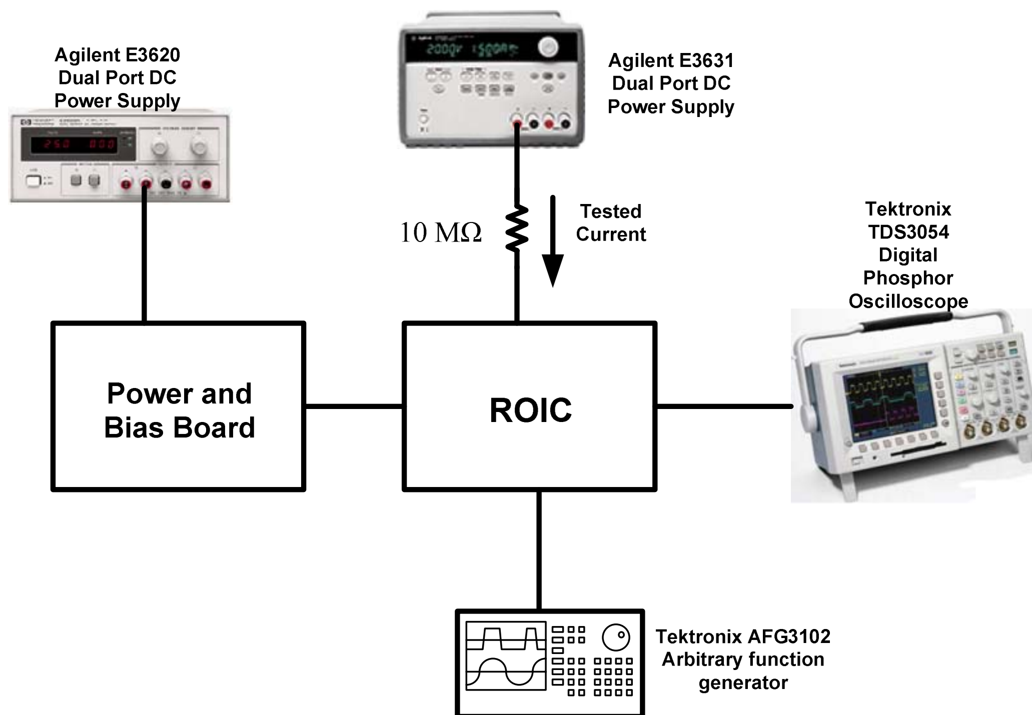
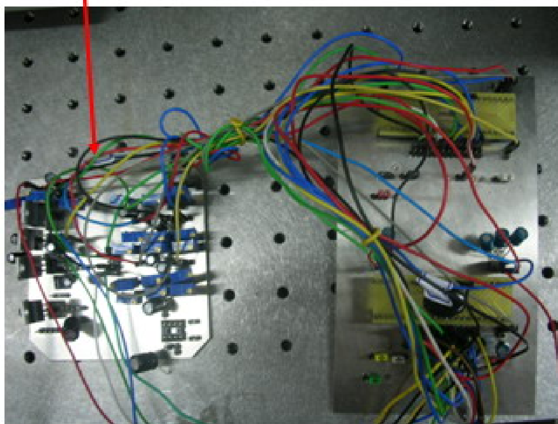
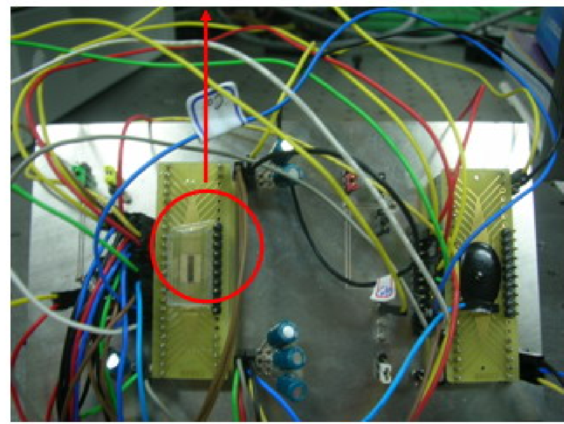



Fig. 4.3 The setup of testing environment of the fabricated infrared readout chip.

Power and Bias Board



ROIC



(a) (b)

Fig. 4.4 The photograph of measurement board: (a) Bias board and ROIC test board. (b) closer view of ROIC test board.

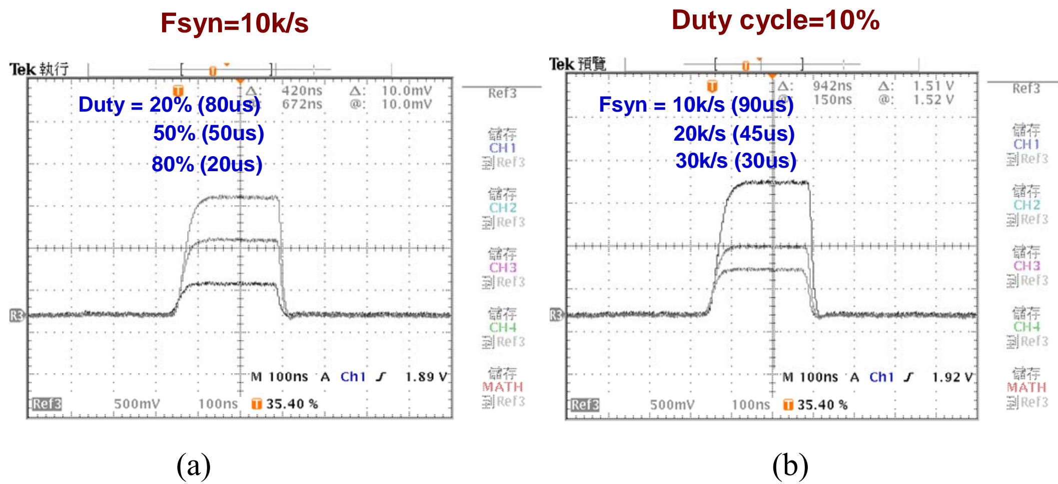



Fig. 4.5 The measured results of independent integration time control with Cint = 5pF and Iin = 90nA: (a) different duty cycle of Fsyn. (b) different frequency of Fsyn.

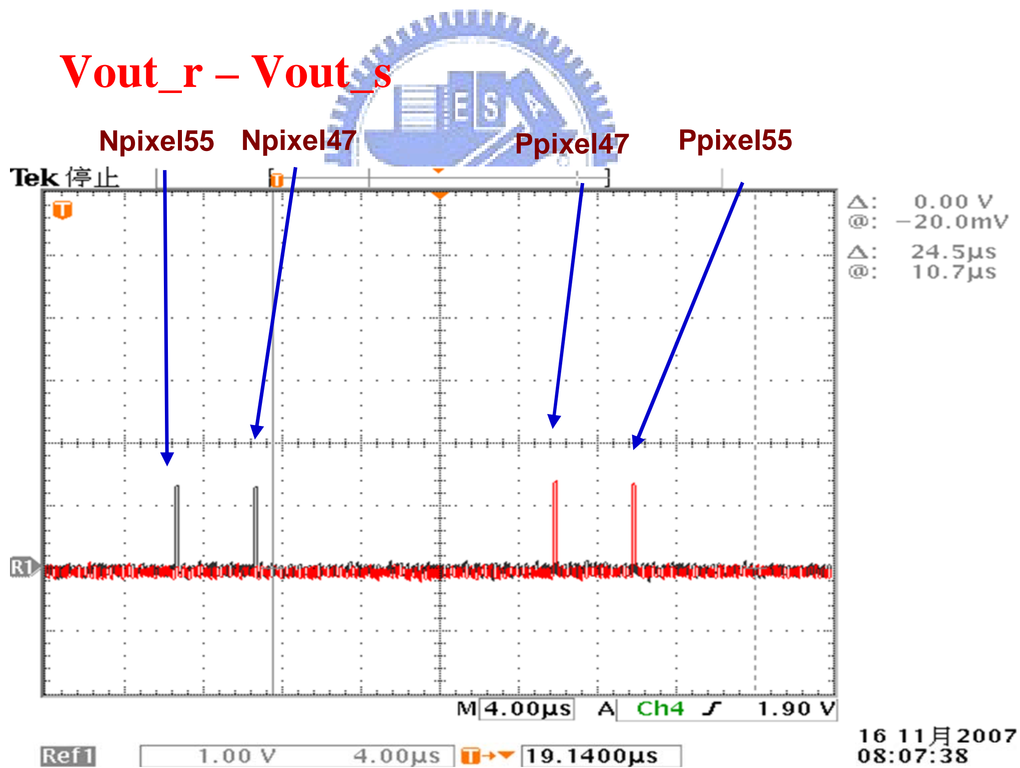



Fig. 4.6 Different output priority.

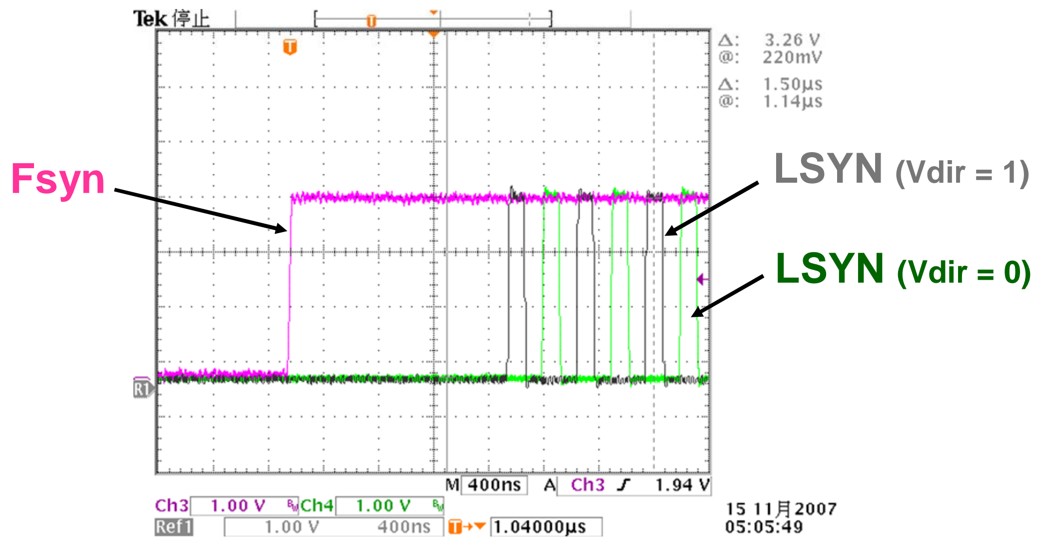



Fig. 4.7 Serial interlaced output.

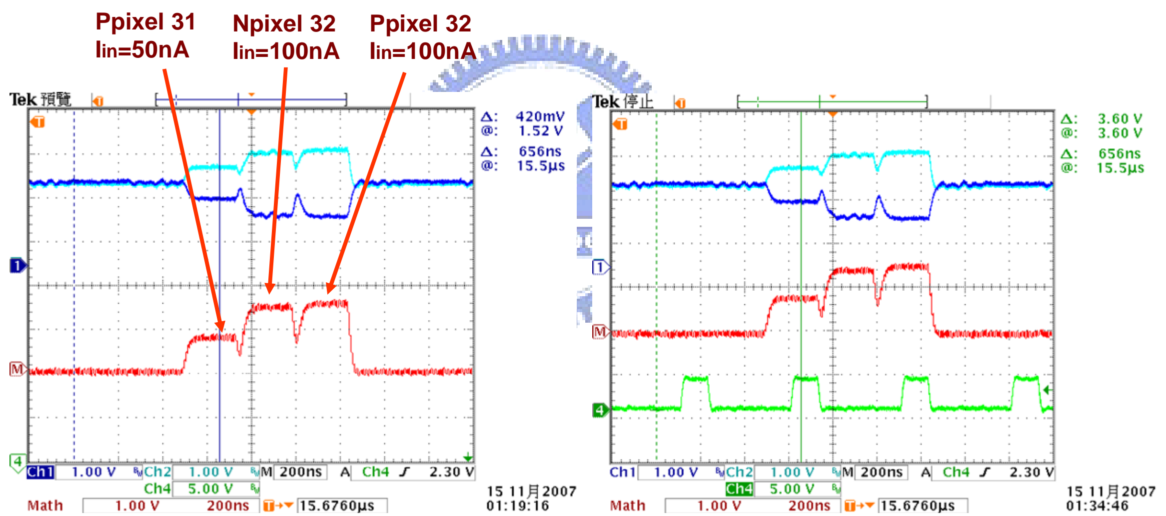
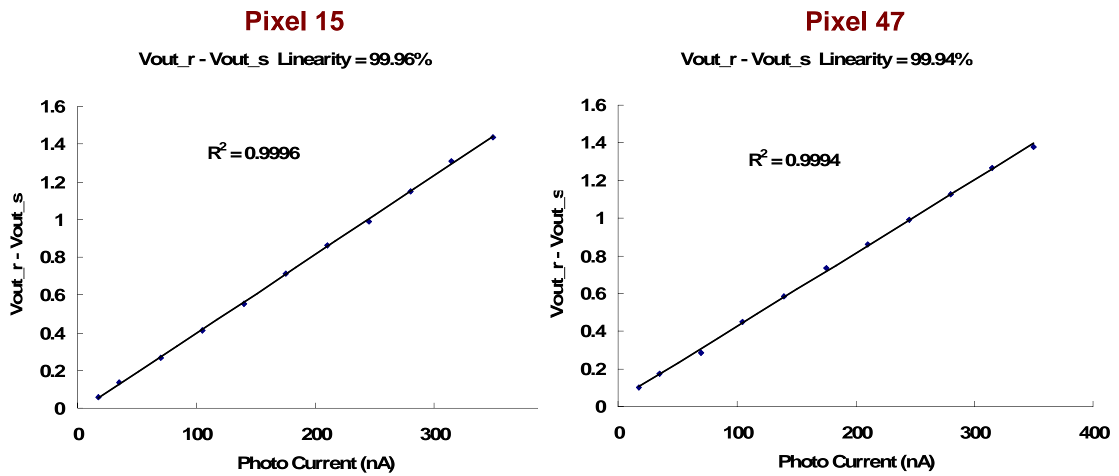



Fig. 4.8 The measured results of two chip combined.

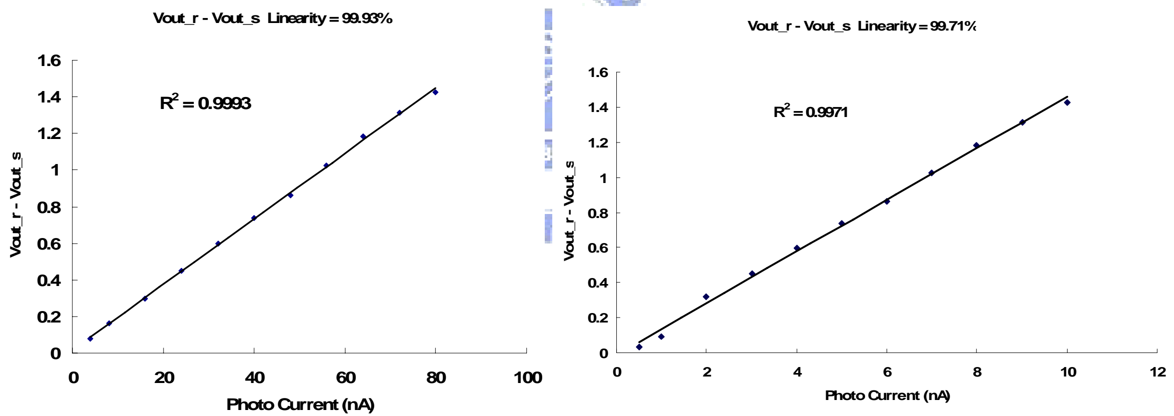
Fsyn = 10kHz Clk = 4MHz Duty cycle = 20% Tint = 80 us Cint = 20pF




(a)

Fsyn = 10kHz Clk = 4M Hz Duty cycle = 10% Tint = 90 us

Cint = 5pF Pixel 23 Cint = 0.3pF Pixel 23




(b)

Fig. 4.9 The measured differential voltage, vout_r - vout_s, versus input current with (a) different pixels. (b) different integration capacitors and input current range for pixel 23.

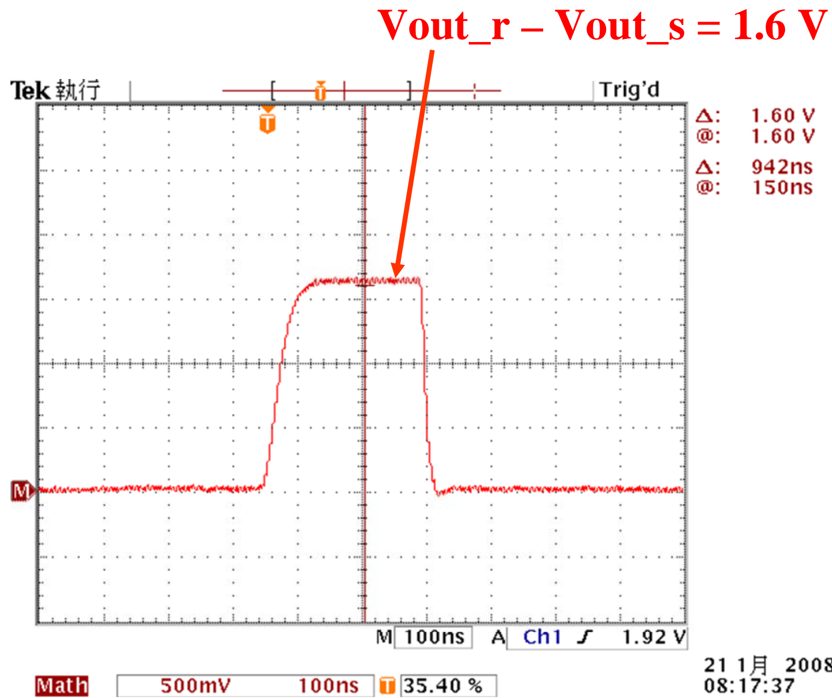



Fig. 4.10 The waveform shows that maximum swing is 1.6V.

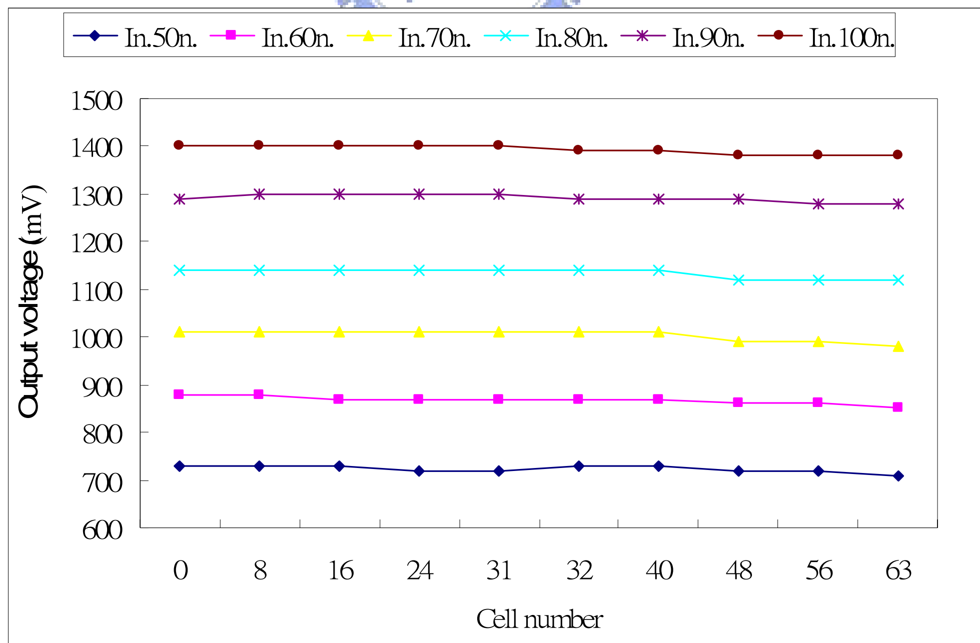



Fig. 4.11 The uniformity of ROCI chip with different input currents from 50nA to 100nA.

# CHAPTER 5

# CONCLUSIONS AND FUTURE WORK

## 5.1 CONCLUSIONS

In this thesis, a CMOS readout circuit for 1 x 128 InGaAs infrared detector array is designed, analyzed, and experimentally verified. By using the buffered direct injection (BDI) circuit with selectable integration capacitors, good injection efficiency, stable detector bias, high charge detection sensitivity and large dynamic range can be achieved. Selectable integration capacitors and independent time control can help to achieve wide application range. The cascoded current source and Vsb=0 in source follower improve linearity and increase output swing. Careful design in Ccds capacitor can enhance output swing. The improved double delta sampling (DDS) circuit is used to suppress fixed pattern noise, clock feedthrough noise, and channel charge injection. An experimental 1 x 64 readout chip has been designed and fabricated to verify the function and performance by using 0.35μm 2P4M N-well CMOS technology. Some noise shielding techniques for mixed-mode IC are used in the readout chip, such as the separation of the analog and digital power, the different analog and digital ground, and the independent substrate bias line.

This 1x128 readout chip is designed to work under 3.3 V power supply. The chip is bonded on PCB. Off-chip testing current sources are used to simulate the photo-current of IR detectors. It is shown that the linearity performance of the readout chip is better than 99.73% and the maximum output swing is 1.6V. The maximum readout speed is 4 MHz. The maximum frame rate at 4 MHz readout speed is 30k frames/sec. The integration time tunable

range at 26k/s frame rate is from 37.42us to 0.935us. The total active chip power is below 14.5 mW at 298K. The function and performance of the readout circuit has been verified by HSPICE simulation and the measurement on a 1 x 128 format experimental chip.

## 5.2 FUTURE WORK

In the future, the fabricated readout chip will be combined with the whole linear IR detector array. Then, based on the experimental results, a readout chip with large array size will be designed and fabricated.

Two dummy cells should be added to two sides of column readout circuit to reduce the effect of process variations. In the design of the analog circuit of 1 x 128 ROIC, the gain loss in the source follower of NMOS device can be avoided by using the mask of deep N-well (shared for all cells to reduce the area) to increase the output voltage dynamic range if the process can be shifted from 0.35um to 0.18um. In addition, the MIM capacitor can be available to replace the double poly capacitor and then the voltage swing drop due to the effect of large parasitical capacitance of bottom poly can be reduced.

In this thesis, CMOS readout techniques for infrared detector array of IR imaging systems are proposed and analyzed. All the structures and technologies discussed above have their uniqueness and features for different applications. Due to the development of commercial IR imaging systems and the fast advancement of submicron CMOS technologies, high-performance and low-cost IR imaging system will be developed through the inventions of new circuit techniques and structure. Moreover, the emerging technologies of CMOS visible-light imaging systems will share the advantages of the developed IR imaging systems due to their similarities. Both will be driven by rapid development and wide applications of multimedia systems. Thus the proposed CMOS readout structure can be further modified and designed as new techniques for the other application. With innovative development of readout

circuit, a new generation of CMOS imaging systems is highly expected.

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# 簡　　歷

姓　　名：鄭人文

學　　歷：

私立輔仁大學電子工程學系　　　　　(87年9月–91年6月)

國立交通大學IC設計產業研發碩士班　(94年7月–96年7月)

論文名稱：

1 x 128 紅外線偵測器陣列之互補式金氧半讀出積體電路設計與分析

THE DESIGN AND ANALYSIS OF CMOS READOUT INTEGRATED CIRCUIT FOR 1 x 128 LINEAR INFRARED PHOTODETECTOR ARRAY