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Formation of cobalt silicide under a passivating film of molybdenum or tungsten

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A very simple and reproducible cobalt silicide process with Mo/Co or W/Co bilayer metallization to overcome the oxidizing liability of Co annealed in a normal flowing-nitrogen furnace has been developed. Cobalt is deposited on blank and patterned silicon wafers in an electron-beam evaporation system followed by Mo (or W) deposition without breaking the vacuum. The cobalt silicidation is carried out using a two-step annealing process. The first annealing is performed at a temperature ranging from 400 to 600 °C, during which the role of the upper layer of Mo (or W) is to protect the underlying Co layer from being oxidized while not disturbing the cobalt's silicidation process. Perfect selective etching of Mo (or W) can be accomplished by a $\text{NH}_4\text{OH} + \text{H}_2\text{O}_2 + (2-3)\text{H}_2\text{O}$ solution. The second annealing is performed at a higher temperature of 750 °C to completely transform the CoSi obtained in the first annealing into CoSi_2 and induce grain growth of CoSi_2 , thus lowering the resistivity. X-ray diffraction, Auger electron spectroscopy, scanning electron microscopy, and sheet resistance measurement are used to characterize the silicide phase and microstructure.

I. INTRODUCTION

Metal silicides are necessary for the gates and interconnects in scaled-down very large scale integration (VLSI) because a lower resistivity, about two to three orders less than that of the highly doped polysilicon ($10^4 \mu\Omega \text{ cm}$),¹ can improve RC time delay and IR potential drop. Use of silicides can also reduce the series resistance of shallow junction and contact resistance.² Other important features of the metal silicides are stability at high temperatures and self alignment with silicon and polysilicon at contacts, gates and interconnects. Furthermore, the work functions do not change when the gates are made of polycides. Thus, formation of silicides is compatible with the existent VLSI processes.

Among the metal silicides the merits of CoSi_2 include low resistivity, self alignment capability, high eutectic temperature (1195 °C), low formation temperature, good chemical stability, Co's nonreaction with silicon oxide below 900 °C and inertness to nitrogen,³⁻⁵ no formation of cobalt-dopant (As and B) compound,⁶ and epitaxial silicide growth on silicon.⁷ However, cobalt silicide still has its drawback. Cobalt is liable to form cobalt oxide when Co film deposited on silicon is annealed in a flowing-nitrogen furnace. In order to prevent the Co film from oxidation before silicidation, very stringent control over the annealing ambient and procedure was found to be critical, otherwise some passivation schemes must be applied. Unfortunately, the existent methods still have some disadvantages, e.g.,

- (i) vacuum anneal: low throughput,
- (ii) rapid thermal annealing and laser annealing: low throughput and thermal stress,
- (iii) SiO_x passivation: plasma or HF is needed to strip the silicon oxide,
- (iv) $\alpha\text{-Si/W}$ passivation⁸: unsatisfactory selectivity owing to plasma etch and poor reliability due to complex structure/process,
- (v) $\alpha\text{-Si}$ passivation⁹: step coverage problem due to very

thin amorphous silicon deposition.

All in all, a simpler structure and more reliable process need to be developed.

The refractory metals, which have a high melting point as well as a high silicidation temperature, may be deposited on top of a Co film to passivate the Co from oxidation during the normal flowing-nitrogen furnace annealing. The Mo/Ti bilayer metallization for a self-aligned TiSi_2 process has been reported.¹⁰ In fact, refractory metals are more suitable to protect Co, since Co has a lower silicide formation temperature. Thus, a wider temperature range exists between the oxidizing or silicidizing temperatures of refractory metals and the silicidizing temperature of Co. Among the refractory metals, tungsten (W) and molybdenum (Mo), which feature higher melting point, higher oxide/metal volume ratio and lower oxygen solubility, are the best candidates for the purpose of passivation. Furthermore, Mo and W do not mix with Co according to the Darken and Gurry plot since their electronegativity and atomic radii differ greatly.¹¹ In an N_2 -flowing environment a Mo or W passivating film of appropriate thickness is stable up to 600 °C for a long enough time for the underlying Co film to be completely transformed into Co-silicide. The more important point is that W and Mo can easily be etched away by an $\text{NH}_4\text{OH} + \text{H}_2\text{O}_2 + x\text{H}_2\text{O}$ solution, which does not hurt the CoSi and CoSi_2 . In this work, we report the complete silicidation of a Co layer by employing a passivating film of Mo or W of pertinent thickness and controlling the annealing condition.

II. EXPERIMENTAL

The Mo/Co and W/Co bilayer metallization was carried out in an electron-beam evaporator on (100) Si blank wafers and patterned wafers with a thermal silicon oxide coating of 6000 Å. Prior to metal depositions, the wafers were dipped in 10:1 HF for 10 s, rinsed in deionized (DI) water for one

minute and then kept in methanol. The metal film deposition was performed with a base pressure below 2×10^{-6} Torr. A Co film of 600 Å in thickness was first deposited at a rate of 2 Å/s, followed by a 400 Å Mo (or W) film deposition at 1.5 Å/s without breaking the vacuum. Cobalt silicidation was carried out using a two-step annealing process. The first annealing was performed at 400–600 °C in a conventional flowing-nitrogen furnace. Selective etching of the overlying Mo (or W) and its oxide, as well as the unreacted Co layer over the silicon oxide was accomplished simultaneously in a solution of $\text{NH}_4\text{OH} + \text{H}_2\text{O}_2 + 2\text{H}_2\text{O}$ at 70 °C. The second annealing was then performed in the same N_2 environment at 750 °C for 30 min. X-ray diffraction (XRD), Auger electron spectroscopy (AES), scanning electron microscopy (SEM), and sheet resistance measurement were used to characterize the silicide phase and surface morphology.

III. RESULTS AND DISCUSSION

A. First annealing

1. At 400 °C

Cobalt and silicon can react to form silicide at this temperature. The first silicide formed is Co_2Si , which is followed by the simultaneous growth of CoSi as determined by XRD analysis. Figure 1 shows the AES depth profiles of the as-deposited as well as the 400 °C annealed Mo(400 Å)/Co(600 Å)/Si structure. In a 40 min anneal, the CoSi phase appears located close to the Si substrate with Mo (or W), Co and Co_2Si topping it as shown in Fig. 1 (b). In a 120 min anneal, all the Co is transformed into Co_2Si and CoSi as shown in Fig. 1 (c). After 360 min anneal, only the CoSi phase remains, but the outer part of the CoSi layer contains a high concentration of oxygen as shown in Fig. 1 (d). Since the etching solution of $\text{NH}_4\text{OH} + \text{H}_2\text{O}_2 + (2-3)\text{H}_2\text{O}$ will attack Co_2Si and a long time annealing for complete transformation into the CoSi phase would lead to a high concentration of oxygen in the surface layer, it is not suitable to do the first annealing at this temperature.

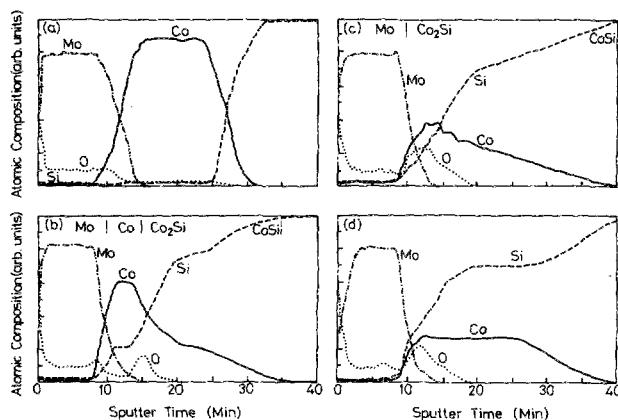


FIG. 1. AES depth profiles of Mo(400 Å)/Co(600 Å)/Si annealed at 400 °C (a) as-deposited, (b) for 40 min, (c) for 120 min, and (d) for 360 min.

It has been reported that the oxygen contained in the as-deposited cobalt is expelled when Co and Si react to form silicide.³ In the Mo (or W)/Co system the oxygen is initially swept out of the growing silicide and segregates at the Co/Co₂Si interface [Fig. 1 (b)], then stays in the Co₂Si layer when the Co is absent [Fig. 1 (c)], and finally stays in the outer CoSi layer as it is the only phase left [Fig. 1 (d)]. Hence, the oxygen content is high in the last transformed outer CoSi layer. Based on the segregation of oxygen, it is anticipated that the oxygen contamination in the as-deposited Co would affect the silicide phase transformation. A longer annealing time (360 min in this case) is needed to complete the phase transformation at this temperature.

It is shown in Fig. 1 that the passivating layer keeps almost intact at this temperature. Both Mo and W are only slightly oxidized on the surface and are not silicidized at all. In addition, since the electronegativity and atomic radii of Mo (or W) and Co differ greatly, they do not mix with each other.

Because of the apparent resistivity difference among the Co_2Si (40 $\mu\Omega$ cm), CoSi (120 $\mu\Omega$ cm), and CoSi_2 (18 $\mu\Omega$ cm), the phase transformation can be inferred from the measured sheet resistances.¹² Figure 2 shows the measured sheet resistances of the Mo(400 Å)/Co(600 Å)/Si samples annealed at various temperatures for various times. At 400 °C anneal, the sheet resistance increases with annealing time and then saturates at a high resistance value because of the increasing fraction of CoSi which is the final phase at 400 °C. For the bilayer metallization system of Mo/Co or W/Co annealed at a temperature below 500 °C, Mo or W keeps intact or is only slightly oxidized. Thus, the changing trend of the sheet resistance which reflects the cobalt silicide phase transformation is not expected to change appreciably by this overlying Mo or W film. If the samples are annealed at a temperature of 550 or 600 °C, and the Mo or W layer is mostly or entirely oxidized, the sheet resistance lowers

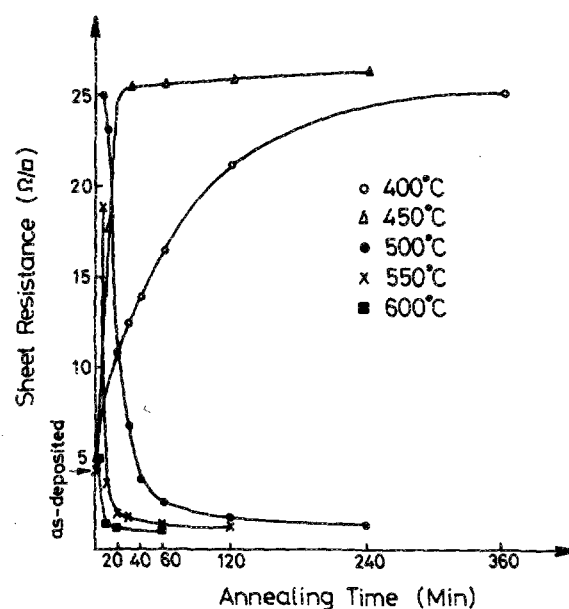


FIG. 2. Sheet resistance versus annealing time of the first annealing at 400, 450, 500, 550, and 600 °C.

slightly after etching due to the removal of the molybdenum oxide or tungsten oxide which does not conduct well. Thus, the changing trend of the postetch sheet resistance is nearly the same as that of the preetch sheet resistance. The oxidation of Mo and W will be discussed later in more detail.

2. At 450 °C

The phase transformation is similar to that at 400 °C, but with a faster silicide formation rate. For a 30 min anneal, the XRD spectrum reveals that CoSi is the only phase of cobalt silicide. The CoSi is not transformed into CoSi₂ even after 240 min of annealing; this implies that CoSi₂ can not be formed at 450 °C. The fact that the sheet resistance reaches a saturation value after a 30 min anneal, as shown in Fig. 2, also infers that there is no phase transformation from then on; nevertheless the AES depth profile shown in Fig. 3 indicates that the oxygen can be expelled out of the cobalt silicide at this temperature. The passivating overlayer still remains nearly inert at 450 °C.

3. At 500 °C

After a 5 min anneal at 500 °C, all the Co is transformed into CoSi; no Co or Co₂Si is detected from the XRD analysis. After a 10 min anneal, CoSi₂ is detected and its fraction increases with the annealing time at the expense of CoSi. It is seen that the sheet resistance continuously decreases after the first 5 min (Fig. 2) because of the increasing fraction of the CoSi₂ phase and its grain growth. The passivating layer is observed to be partially oxidized on the surface after a 60 min anneal as revealed by the AES depth profile shown in Fig. 4(a), while the underlying Co has already been transformed into CoSi and CoSi₂ as confirmed by the XRD analysis shown in Fig. 5. The CoSi₂ phase is located next to the Si substrate.

4. At 550 and 600 °C

The phase transformation of the underlayer Co is similar to that at 500 °C but with a faster rate (Fig. 2). For a 20 min anneal at 600 °C, all the Co has been completely transformed into CoSi₂ as confirmed by XRD analysis. At these tempera-

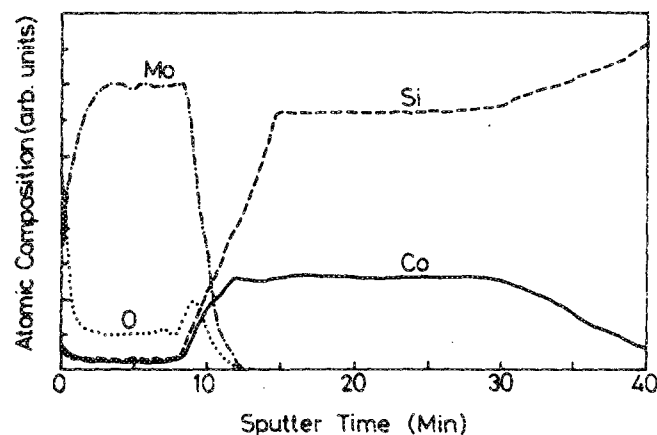


FIG. 3. AES depth profile of Mo(400 Å)/Co(600 Å)/Si annealed at 450 °C for 30 min; the oxygen is expelled out of the CoSi.

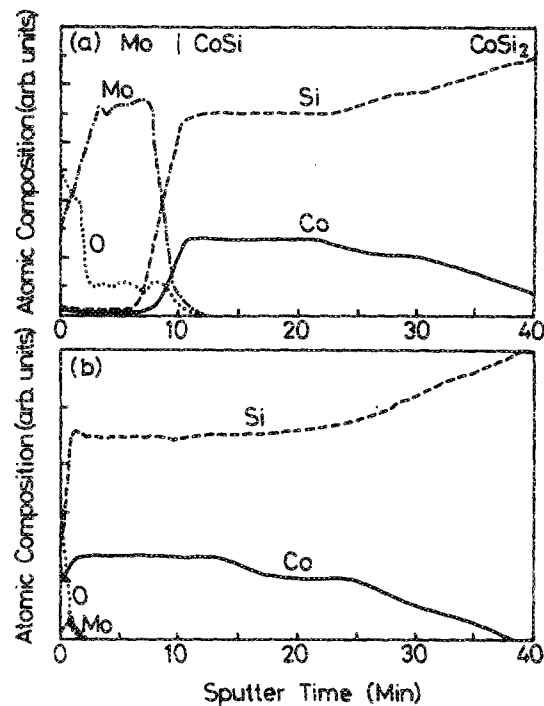


FIG. 4. AES depth profiles of Mo(400 Å)/Co(600 Å)/Si annealed at 500 °C for 60 min (a) before etching, and (b) after etching.

tures, it is important to note that Mo (or W) is entirely oxidized, while the cobalt silicide transformation occurring underneath is not disturbed, as shown in Fig. 6. The fact that the upper Mo (or W) layer becomes oxidized instead of being silicidized in our experiments actually insures process simplicity and repeatability. The result of the cobalt silicide's transformation not being disturbed by the oxidation of the upper Mo (or W) layer implies that the formation of cobalt silicide has already finished before the Mo (or W) is oxidized completely.

It is important to note that annealing for too long a time in the first annealing step will cause lateral growth of silicide. Fig. 7 shows the SEM micrograph for the sample annealed at 550 °C for 2 h. The lateral growth of CoSi₂ is clearly observed. It is speculated that the Si atom movement in Co-silicide causes lateral growth.

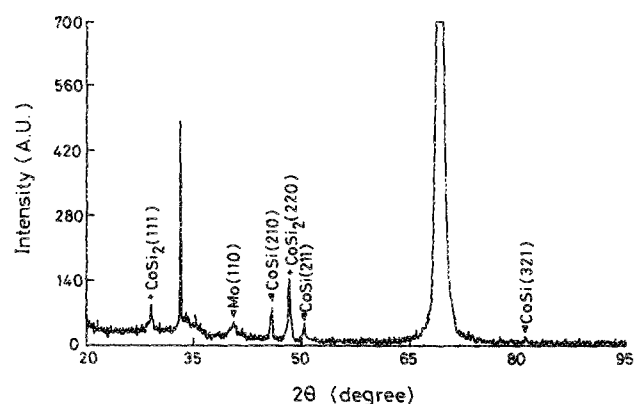


FIG. 5. XRD pattern of Mo(400 Å)/Co(600 Å)/Si annealed at 500 °C for 60 min showing both peaks of the CoSi and CoSi₂.

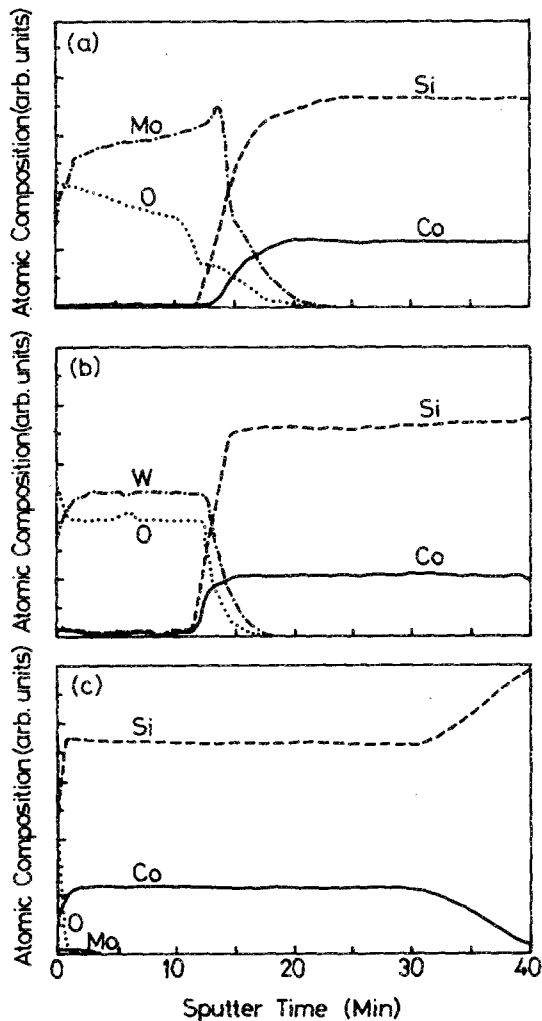


FIG. 6. AES depth profiles of (a) Mo(400 Å)/Co(600 Å)/Si annealed at 600 °C for 20 min, (b) W(400 Å)/Co(600 Å)/Si annealed at 600 °C for 220 min, and (c) after etching of (a).

B. Selective etch

A solution of $\text{NH}_4\text{OH} + \text{H}_2\text{O}_2 + 3\text{H}_2\text{O}$ at 70 °C was used to etch away the 400 Å overlayer Mo (or W) completely within two minutes without removing the underlying CoSi and CoSi₂ layers on the blank silicon wafers as illustrated in the AES depth profile shown in Fig. 4(b). The solution can etch the molybdenum oxide [Fig. 6(c)] and the tungsten oxide as well. The overlayer Mo (or W) and the 600 Å unreacted Co over SiO₂ of the patterned wafers can also be etched away by a slightly concentrated solution of $\text{NH}_4\text{OH} + \text{H}_2\text{O}_2 + 2\text{H}_2\text{O}$ at 70 °C in eight minutes without removing the CoSi and CoSi₂ in the window at all. Figures 8(a) and 8(b) show the SEM micrograph of the Mo/Co/Si sample annealed at 550 °C for 20 min followed by etching; it is evident that no residues of Mo and Co remain over the silicon oxide, and that silicide lateral growth and silicon oxide damage do not occur. If the Mo (or W) (400 Å)/Co(600 Å)/patterned-Si samples are annealed at 550 or 600 °C for a longer time, so that the overlayer Mo (or W) and the Co over the SiO₂ are oxidized, it would be harder to

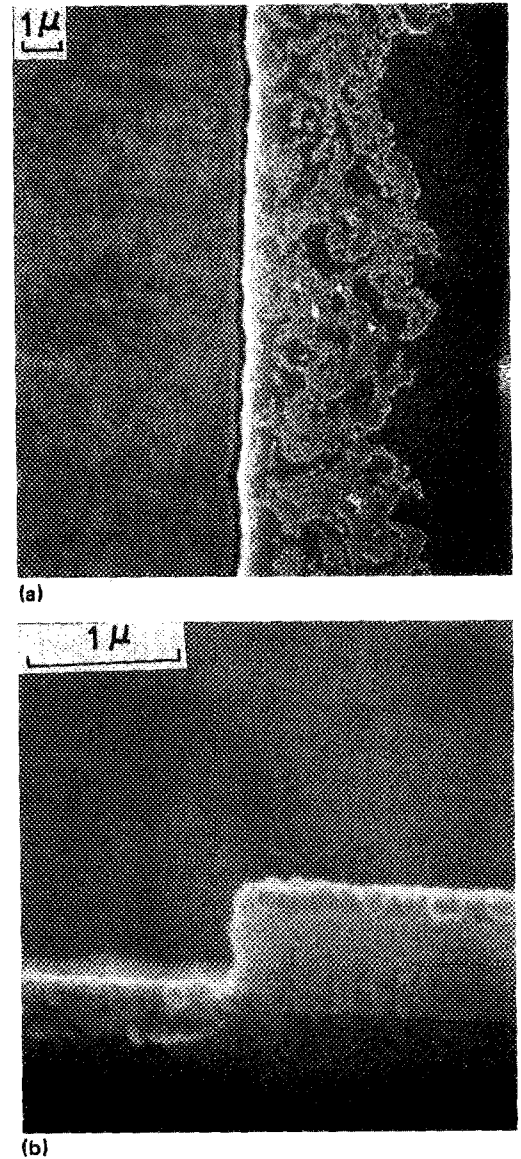


FIG. 7. SEM micrographs of the sample annealed at 550 °C for 2 h and etched: (a) plan view, and (b) cross-sectional view. Silicide lateral growth is observed.

strip the cobalt oxide with the same etching solution. However, it is noted that the oxidation of the underlayer of Co over the SiO₂ occurs later than the silicide lateral growth.

Since the etching solution can attack Co and Co₂Si, it is very important that all the Co must be transformed into CoSi and/or CoSi₂ during the first annealing. If some Co and/or Co₂Si are left after the first annealing, the sheet resistance after the etch will differ greatly from those before the etching and will increase with etching time.

C. Second annealing

The purpose of the second annealing at 750 °C for 30 min is to completely transform the CoSi and/or CoSi₂, formed during the first annealing into CoSi₂ [Fig. 8(c)] and to increase its grain size. Thus the sheet resistance is reduced. It is noted that the final resistances are all nearly equal to 1.12

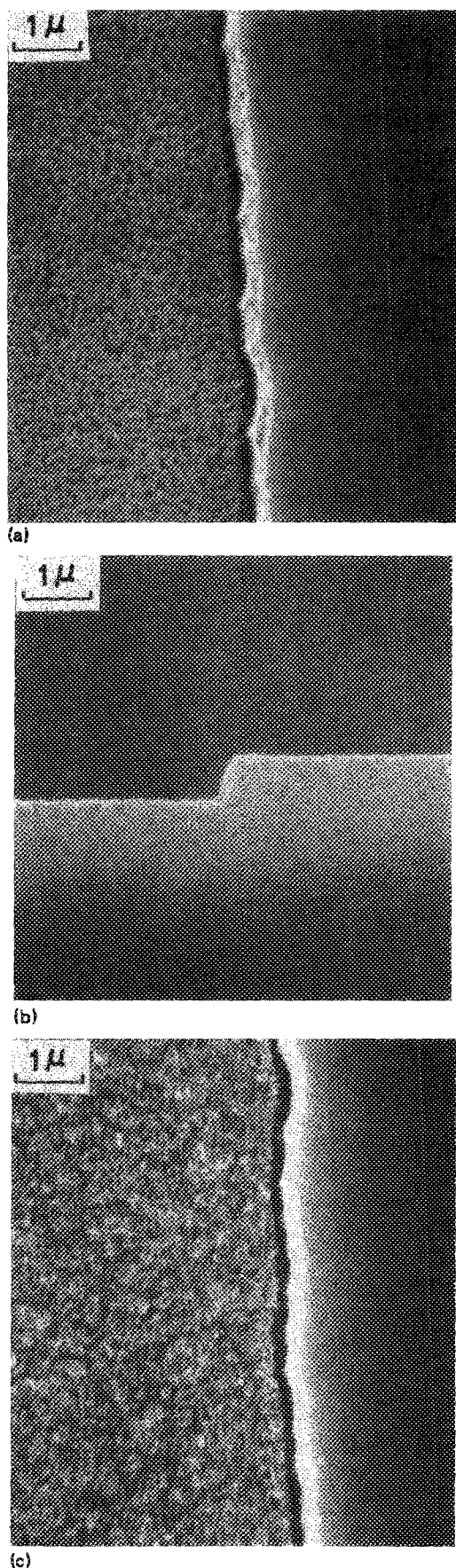


FIG. 8. SEM micrographs of the Mo/Co/Si samples annealed at 550 °C for 20 min and etched: (a) plan view, (b) cross-sectional view, and (c) plan view after the second annealing.

Ω/\square , regardless of the relative fraction of CoSi and CoSi₂ and the sheet resistance after the first annealing, provided that all the Co has been completely transformed into CoSi and/or CoSi₂. The XRD analysis and AES depth profile indicate that the CoSi and CoSi₂ were not oxidized during the second annealing in a normal flowing-nitrogen furnace; very good quality of CoSi₂ was formed.

D. Optimum conditions for the first annealing

Considering as factors that Co and Co₂Si would be attacked by the etchant, that the oxygen contained in the as-deposited Co must be expelled, and that the ratio of CoSi to CoSi₂ after the first annealing does not affect the final sheet resistance following the second annealing, it is required that the "lower" limit for the first annealing is to transform all the Co into CoSi and/or CoSi₂. This is to say that the first annealing must be performed in a normal flowing-nitrogen furnace at 450 °C for more than 30 min or at 500–600 °C for more than 5 min for the Mo(400 Å)/Co(600 Å)/Si or W(400 Å)/Co(600 Å)/Si bilayer metallization system. The "upper" limit is, not to anneal for too long a time at each pertinent temperature, in order to prevent the lateral growth of the silicide. The thickness of Mo (or W) and Co may be varied according to the thickness of CoSi₂ and the step coverage required.

E. Schottky diode

We have fabricated 2.0 × 2.0 mm² CoSi₂/n-Si Schottky diodes with guard rings using the Mo/Co and W/Co bilayer metallization scheme. The thickness of Mo (or W) and Co are 400 Å and 1000 Å, respectively. A silicon epitaxial wafer with 6 μm thick phosphorus doped 0.8 Ω cm n-type epitaxial layer on arsenic-doped 0.001 Ω cm n-type (111) Si substrate was employed. The first annealing was performed at 550 °C for 20 min. After selective etching, the second annealing was performed at 750 °C for 30 min. The barrier height obtained from the *I*-*V* measurement is 0.62 eV, and the forward ideality factor of the diode is 1.02.

IV. SUMMARY

A very simple and reliable cobalt process with Mo/Co or W/Co bilayer metallization using a two-step annealing scheme in a normal flowing-nitrogen furnace has been developed. The first annealing, with conditions falling between the two limits, can be performed at a temperature ranging from 450 to 600 °C. The lower limit is to transform all the Co into CoSi and/or CoSi₂, and the upper limit is not to anneal for too long a time at the above mentioned temperatures in order to prevent lateral growth of the silicide. The overlying Mo (or W) layer is to protect the underlayer Co from being oxidized during the silicidation process, and it does not disturb the Co silicidation process whether it becomes oxidized or not. Mo (or W) does not mix with Co below 600 °C in the Mo/Co/Si or W/Co/Si metallization system. At a temperature of 550–600 °C, which is higher than the silicidation temperatures of Mo and W, the outer Mo (or W) layer begins to form stable oxide inwards instead of silicidation. Following the first annealing, $\text{NH}_4\text{OH} + \text{H}_2\text{O}_2 + (2-3)\text{H}_2\text{O}$ at 70 °C

can completely etch away Mo, W and their oxide as well as the unreacted Co over SiO₂ without removing the CoSi and CoSi₂. The second annealing in a normal flowing-nitrogen furnace at a higher temperature of 750 °C is to transform the CoSi and/or CoSi₂ into CoSi₂ completely and to increase the grain size. The sheet resistance and the silicide phase resulting from the first annealing would not affect the final result after the second annealing, as long as the first annealing condition falls between the upper and lower limits.

ACKNOWLEDGMENTS

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¹S. M. Sze, *VLSI Technology*, 1st ed. (McGraw-Hill, New York, 1983), Chap. 3.

²D. B. Scott, W. R. Hunter, and H. Shichijo, *IEEE Trans. Electron Devices*, **ED-29**, 651 (1982).

³A. E. Morgan, E. K. Broadbent, M. Delfino, B. Coulman, and D. K. Sadana, *J. Electrochem. Soc.* **134**, 925 (1987).

⁴S. P. Muraka, *Silicide for VLSI Applications*, 1st ed. (Academic, New York, 1983), Chap. 1.

⁵S. P. Muraka, D. B. Fraser, A. K. Sinha, H. T. Levinstein, E. J. Llord, R. Liu, D. S. Williams, and S. J. Hillenius, *IEEE Trans. Electron Devices*, **ED-34**, 2108 (1987).

⁶K. Maex, R. De Keersmaecker, G. Ghosh, L. Delaey, and V. Probst, *J. Appl. Phys.* **66**, 5327 (1989).

⁷L. J. Chen, J. W. Mayer, and K. N. Tu, *Thin Solid Films*, **93**, 135 (1982).

⁸M. Z. Lin and C.-Y. Wu, *J. Electrochem. Soc.* **136**, 258 (1989).

⁹H. H. Tseng and C.-Y. Wu, *IEEE Electron Devices Lett.* **EDL-7**, 623 (1986).

¹⁰H. K. Park, J. Sachitano, G. Eiden, E. Lane, and T. Yamaguchi, *J. Vac. Sci. Technol. A* **2**, 259 (1984).

¹¹L. S. Darken and R. W. Gurry, *Physical Chemistry of Metals* (McGraw-Hill, New York, 1953).

¹²A. Appelbaum, R. V. Knoell, and S. P. Muraka, *J. Appl. Phys.* **57**, 1880 (1985).