# 國立交通大學

## 電機學院IC設計產業研發碩士班

## 碩士論文

具有部分隨機匹配的12位元250百萬赫芝電流式互補式
金氧化半導體數位類比轉換器

12-bit 250MSample/s Current-Steering CMOS D/A
Converters with Partial Random Element Matching

研究生：白逸維

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中華民國九十六年十二月

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# 具有部分隨機匹配的12位元250百萬赫芝電流式互補式金氧化半導體數位類比轉換器

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## 摘　　要

高速數位類比轉換器是目前高效能系統，如資料通訊系統中不可獲缺的主要電路。然而電流驅動式數位類比轉換器因為製程不匹配效能往往受靜態和動態線性度限制。在本篇論文，主要設計一個簡單的隨機架構去改善製程不匹配。我們利用多輸入多輸出多工器架構再配合隨機產生器讓原本固定的線路去隨機改變，再配合特殊的電流源開關的佈局去改善不同製程的改變，我們可以打亂諧波，將能量平均分散到 noise floor 而增加 SFDR。

本論文是配合上述簡單隨機架構的一個 12 位元 250MHz 數位類比轉換器，在數位類比轉換器電路的實現，切換電流源式是一個很好的實現方法。在數位類比轉換器中包含在較低的 4 位元為 2 進位權重架構和較高的 8 位元為含有隨機匹配的溫度計編碼架構。除此之外，為了增進數位類比轉換器的動態效能及提高解析度與元件間的匹配，分別使用了抑制突波的拴鎖器和特殊的佈局，來增加數位類比轉換器的效能。同時也考量了在佈局繞線時產生的寄生電容，所造成速度還有信號不同步的效應。數位類比轉換器採用 TSMC 0.18 μm 1P6M mixed-signal CMOS 製程來實現，沒有部分隨機架構整體晶片的面積為 1.788 $mm^2$，另外有含部份隨機架構整體晶片面積為 1.838 $mm^2$。

# 12-bit 250MSample/s Current-Steering CMOS D/A Converters with Partial Random Element Matching

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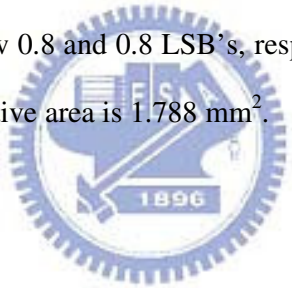
## ABSTRACT

Current-Steering digital-to-analog converters (DACs) are very significant blocks of nowadays high-performance systems, such as data communication links using multilevel signaling. However, these current-steering DACs suffer from the element mismatch of technologies and this limits both the static and dynamic performance. This thesis proposes a simple random structure to improve the element mismatch is presented. We can use a multiplexer with 8-bit input and 8-bit output, to implement the random selection. The random generator controls the selection of the element in the MSB part so that the harmonics caused by mismatch can be attenuated. The simple random structure can be used to randomize tones such that spurious-free dynamic range is increased. To cooperate with a special geometrical arrangement of unit cells in the current sources of the MSB, along with a new switching sequence, results in full cancellation of gradient errors.

Utilizing the simple random structure, a 12-bit 250-MSample/s current-steering D/A converter is implemented in this thesis. The DAC includes a 4-bit binary-coded LSBs, 8-bit

MSBs with thermometer decoders, and random element matching. The differential switches of current sources are controlled by de-glitch latch. The routing complexity and parasitic capacitance have to be considered for speed and signal synchronization.

12-bit current-steering D/A converters in a TSMC 0.18μm CMOS technology are presented. The simulation results of a 12-bit current-steering D/A converter with the partial random element matching show that with the signal frequency of 100.83 MHz at the update rate of 250 MHz, the SFDR is 66.4 dB. The differential nonlinearity and integral nonlinearity are below 0.5 and 0.7 least significant bits (LSB's), respectively. The converter consumers a total power of 75 mW and its active area is 1.838 $mm^2$. The simulation results of D/A converter without the partial random element matching shows that with the signal frequency of 100 MHz at the update rate of 500 MHz, the SFDR is 68.9 dB. The differential nonlinearity and integral nonlinearity are below 0.8 and 0.8 LSB's, respectively. The converter consumers a total power of 73 mW and its active area is 1.788 $mm^2$.



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# Table of Contents

# List of Figures

## Chapter 2



## Chapter 3

## Chapter 4

## Chapter 5

# List of Tables

## Chapter 2



## Chapter 4



## Chapter 5



# *Chapter1*

# Introduction

In many signal processing and telecommunication applications, the digital-to-analog converter (DAC) is a critical building block limiting the accuracy and speed of the overall system. When applications require high speed and high resolution, the current-steering DAC architecture is almost exclusively used. It is more convenient to characterize the performance in the frequency domain using measures as the spurious-free dynamic range (SFDR) [1]. Since be specified as circuit errors, because the impact of DACs errors can be modeled.

## 1.1 Motivation

For high-speed application, the current-steering DACs are often used, since they can drive an output resistive load directly without requiring the use of an extra buffer [2]. However, the static linearity of current-steering DACs is sensitive to current-source mismatch [3]-[18]. Designers often use large devices [3], randomized layouts [8], [10], [12], calibration [15], etc. to reduce this mismatch. These techniques improve linearity, but at the expense of die area or dynamic performance.

In this thesis, a new simple random structure to improve the matching accuracy of the current source and efficiently increase the SFDR is applied for high-resolution and high-speed DACs. The DAC noise is transferred to white noise and the SFDR is optimal. The yield performance of DACs is enhanced by the new algorithm. In additional, a special layout method called Balanced-Ring [12] will help overcome the variation across a range of process. A high-speed

and high-accuracy latch is designed to attain good dynamic performance.

12-bit 250MHz current-steering segmented architecture DACs fabricated in TSMC 0.18μm CMOS is designed by using segmented current-steering architecture that consists of 8 MSB's of unary cells and 4 LSB's of binary cells. In addition, a high speed and low crossing point switch driver is designed to minimize glitch error during dynamic switching transition.

## 1.2 Organization

This thesis is organized as six chapters. Brief content of each chapter is described as follows. In chapter2, the fundamental concepts and architectures of DAC are described first. In addition, the static and dynamic specifications that will impact a DAC's performance are discussed. Chapter 3 presents the non-idealities of current-steering DAC, including finite output impedance, mismatch in current source, timing non-idealities, and non-idealities due to switching in a current-steering DAC. In Chapter 4, based on the consideration discussed in chapter 2 and chapter 3, the design and implementation of a 12-bit 250MHz current-steering with the partial random element matching segmented architecture DAC is described in chapter 4.

Chapter 5 presents the simulation and measurement results. Conclusion and future work are in chapter 6.

# *Chapter2*

# Nyquist-Rate Digital-to-Analog Converter

Digital-to-analog converters (DACs) are essential in data processing systems. DACs interface the digital output of signal processors with the analog world and reconstruct the continuous-time analog signal. The digital-to-analog (D/A) converts a discrete amplitude, discrete time signal to a continuous amplitude, continuous time output.

A DAC is shown in Fig. 2.1. It converts a digital signal into an analog representation [25]. If the DAC generate large glitches during switching from one code to another, then a deglitching circuit is used to mask the glitches. Finally a low-pass filter is required to suppress the sharp edges introduced by the DAC [24].

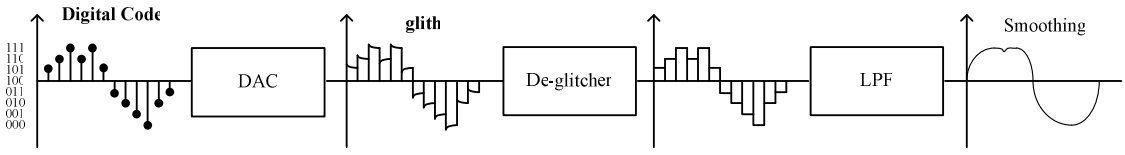



Figure2.1 Digital-to-analog conversion

In this chapter, the fundamental of DAC and different techniques for converting a digital signal into an analog signal representation is presented. The approaches differ in speed, chip area, power efficiency, achievable accuracy, etc

## 2.1 Ideal D/A Converter

A digital-to-analog converter produces an analog output $V_{out}$ that is proportional to the digital input $B_{in}$. For a N-bit D/A converter shown in Fig. 2.1, the output $V_{out}$ can be expressed as:

$$V_{out} = V_{ref}\left(D_0 2^0 + D_1 2^1 + \cdots + D_{n-2} 2^{n-2} + D_{n-1} 2^{n-1}\right) \qquad (2.1)$$

where $D_i$ equals 1 or 0. We also define $b_0$ as the least significant bit (LSB) and $D_{n-1}$ as the most significant bit (MSB). In a D/A converter, a further classification is by the scaling methods. Three methods are called current, voltage and charge scaling.

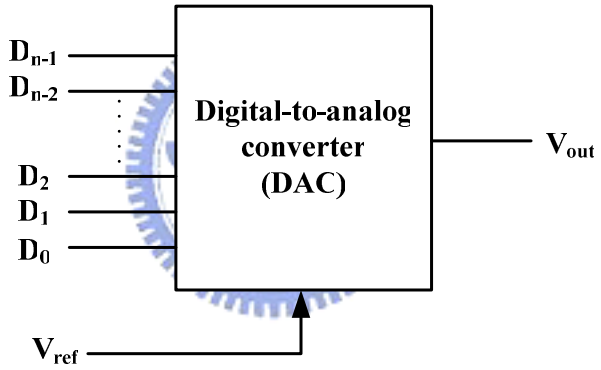



Figure 2.2 Block diagram of a n-bit D/A converter

## 2.2 Performance Metrics

The characterization of DACs is very important in understanding its design. The characteristics of the digital-analog converter can be divided into static, dynamic and dynamic range properties [1].

### 2.2.1 Static Performance

Five basic static parameters are major content of this section of this section, which are offset error, gain error, INL, DNL and monotonicity. To distinguish all values of calculations in the DAC, $X_a(k)$ corresponds to the actual analog output for kth input code and $X_i(k)$ corresponds for the ideal one.

**Offset Error**

The analog output should be 0V for digital input=0. However, an offset exists if the analog output voltage is not equal to zero. This can be seen as a shift in the transfer curve as illustrated in Fig. 2.3.

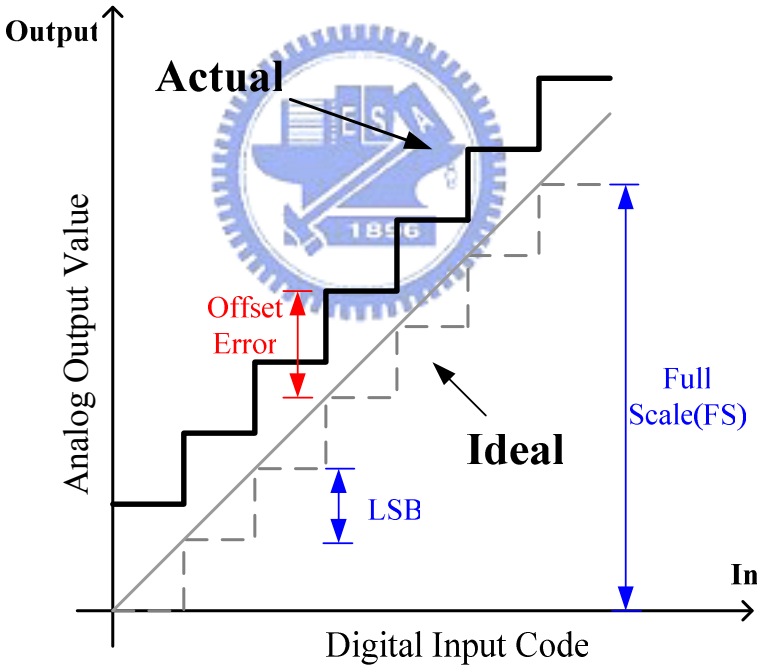



Figure 2.3 Non-ideal transfer curve with offset error

**Gain Error**

Gain error is the difference at the full-scale value between the ideal and actual when the offset error has been reduced to zero. For a non-ideal transfer curve with gain error shown in

Fig. 2.4, the gain error can be expressed as:

$$GainError = \frac{X_a - X_i}{(2^N - 1) \bullet LSB} \tag{2.2}$$

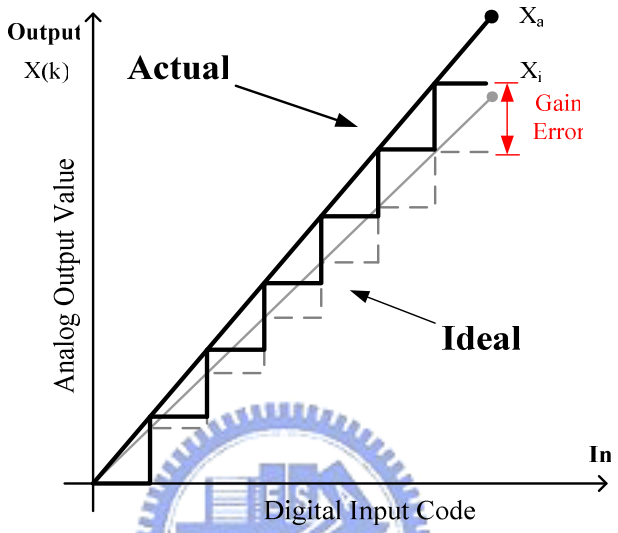



Figure 2.4 Non-ideal transfer curve with gain error

**Differential Non-Linearity(DNL)**

The step size in the non-ideal data converter deviates from the ideal size △ and this error is called the differential nonlinearity (DNL) error. For a DAC the DNL can be defined as the difference between two adjacent analog outputs minus the ideal step size, i.e.

$$DNL_k = X_{a,k+1} - X_{a,k} - \Delta \tag{2.3}$$

The DNL is often normalized with respect to the step size to get the relative error, i.e.

$$DNL_k = \frac{X_{a,k+1} - X_{a,k} - \Delta}{\Delta} \tag{2.4}$$

The above definitions are often most practical for DACs since the analog values can be directly measured at the output

**Integral Non-Linearity (INL)**

The total deviation of an analog value from the ideal value is called integral nonlinearity (INL). For non-ideal transfer function with INL and DNL errors shown in Fig. 2.5, the normalized INL can be expressed as

$$INL_k = \frac{X_{a,k} - X_{i,k}}{\Delta} \tag{2.5}$$

The relation between INL and DNL is given by

$$INL_k = \sum_{t=1}^{k} DNL_t \tag{2.6}$$

The nonlinearity errors are usually measured using a low frequency input signal to exclude dynamic errors appearing at high signal frequencies. The DNL and INL are therefore usually used to characterize the static performance.

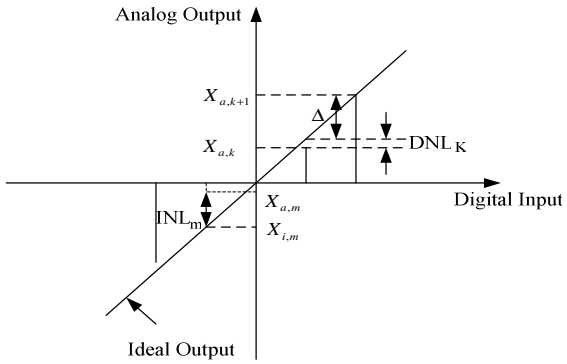



Figure2.5 Non-ideal transfer function with INL and DNL errors of DAC

**Monotonicity**

If the analog amplitude level of the converter increases with increasing digital code, the converter is monotonic. An example of a non-monotonic DAC is shown in Fig. 2.6.

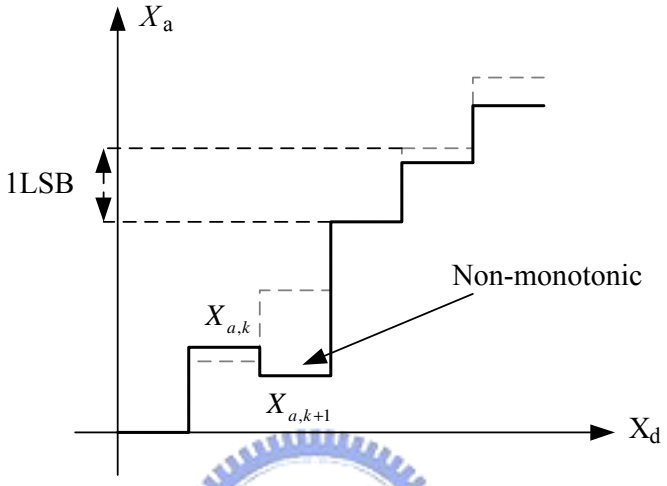



Figure 2.6 A non-monotonic DAC

Monotonicity is guaranteed if the deviation from the best-fit straight line is less than half a LSB, i.e.

$$\left|INL_k\right| \le \frac{1}{2} LSB \quad \text{for all k} \tag{2.7}$$

This implies that the DNL errors are less than one LSB , i.e.

$$\left|DNL_k\right| \le 1LSB \quad \text{for all k} \tag{2.8}$$

It should be noted that the above relations are sufficient to guarantee monotonicity, but it is possible to have a monotonic converter that does not meet the relations in (2.7) and (2.8).

There are some data converters architectures that are monotonic by design, e.g. a thermometer coded DAC.

### 2.2.2 Dynamic Performance

In addition to the static errors that are caused by mismatch in the components in the data converter, several other error sources will appear when the input signal change rapidly. These dynamic errors are often dependent on signal frequency and increases with signal amplitude and frequency. They appear in data converter but are usually more critical in DACs since the shape of the analog wave form determines the performance.

**Settling Time**

The settling time is defined as the time it takes for the converter to settle within some specified amount of the final value. The primary dynamic characteristic of the DAC is the conversion speed. The setting time define the operation frequency of DAC. The factors that determine the settling time of the DAC are the gain bandwidth, slew rate of op amp and parasitic capacitor. The output of transition can be illustrated as Fig. 2.7.

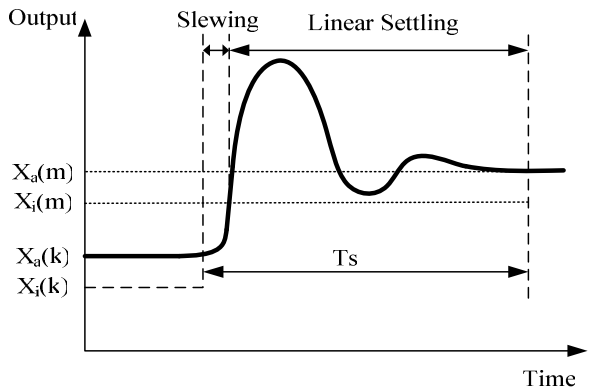



Figure 2.7 Actual output signal and ideal output signal (dashed) of a DAC

The settling can be divided in two phases, a non-linear slewing phase and a linear settling phase. The output signal of an actual DAC can not change its value instantly. The time it takes for the output to settle within a certain accuracy of the final value, for instance 0.1%, is called the settling time $T_s$, and determines the highest possible speed of the circuit. The slewing phase should be as small as possible since it both increases the settling time and introduces distortion in the analog waveform. The slewing is normally caused by a too small bias current in the circuit driving the output and is therefore increased for large steps when more current is needed.

**Glitch**

When the switching time of different bits in binary weighted DAC is unmatched, the glitch occurs. As Fig. 2.8, if a DAC decodes 011 code to 100 code sequentially, the fast MSB changes previously than others. The output of a DAC will occur the error value. The plus effect of the output caused by different switching is called glitch.

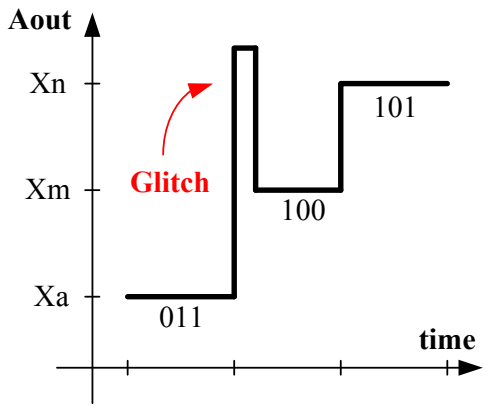



Figure 2.8 Glitch output

### 2.2.3 Dynamic range

For DACs used in communications applications, the INL and DNL are not sufficient to characterize the performance. It is more convenient to characterize the performance in the frequency domain using measures as the signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR). The can be illustrated as Fig. 2.9.

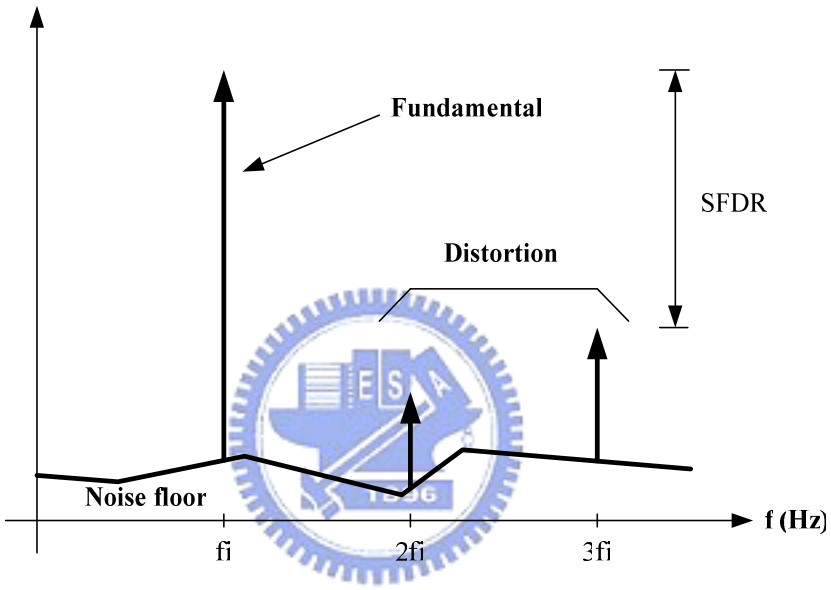



Figure 2.9 Output spectrum of a DAC

**Signal-to-Noise Ratio (SNR)**

The signal-to-noise ratio (SNR) is the ratio of the signal power and the total noise power. SNR is usually expressed in dB as

$$\mathrm{SNR}(dB) = 10 * \log\left(\frac{\text{Signal Power}}{\text{Total Noise Power}}\right) \tag{2.9}$$

**Spurious Free Dynamic Range (SFDR)**

The spurious free dynamic range (SFDR) is the ratio of the power of the signal and the

power of the largest spurious within a certain frequency band. SFDR is usually expressed in dBc as

$$\mathrm{SFDR}(dBc) = 10 * \log\left(\frac{\text{Signal Power}}{\text{Largest Spurious Power}}\right) \tag{2.10}$$

**Total Harmonic Distortion (THD)**

The total harmonic distortion (THD) is the ratio of the total harmonic distortion power and power of the fundamental in a certain frequency band, i.e.

$$\mathrm{THD} = 10 * \log\left(\frac{\text{Total Harmonic Distortion Power}}{\text{Signal Power}}\right) \tag{2.11}$$

**Signal-to-Noise and Distortion Ratio (SNDR)**

The signal-to-noise and distortion ratio (SNDR) is the ratio of the power of the fundamental and the total noise and distortion power within a certain frequency band, i.e.

$$\mathrm{SNDR} = 10 * \log\left(\frac{\text{Signal Power}}{\text{Noise and Distortion Power}}\right) \tag{2.12}$$

## 2.3 Binary Weighted DAC Architecture

The most popular approach for realizing at least some portion of D/A converter is to combine an appropriate set of signals that are all related in a binary fashion. This binary array of signals might be currents, but binary-weighted arrays of charge are also commonly used. The binary weighted DAC utilizes a number of reference element that are binary weighted. The output signal can be written as

$$X_a(nT) = A_0\left[b_0(nT) + 2\cdot b_1(nT) + \cdots + 2^{N-1}\cdot b_{N-1}(nT)\right] \quad (2.13)$$

Where A0 is the reference and T is the update period of the DAC.

### 2.3.1 R-2R Ladder DAC

A very popular architecture for D/A converter uses R-2R ladders. These ladders are useful for realizing binary-weighted current with a small number of components and with a resistance ratio of only 2, independent of the number of bits, N.

The R-2R ladder can be used to obtain binary-weighted current while using only a single-size resistor. (The resistors of size 2R are made out of two resistors size R, to improve matching properties). As a result, this R-2R approach usually gives both a smaller size and a better accuracy than a binary-size approach.

A N-bit DAC that uses an R-2R ladder is shown in Fig. 2.10. For the R-2R based circuit, we see that

$$I = \frac{V_{ref}}{2R} \quad (2.14)$$

and

$$V_{out} = R_F \sum_{i=1}^{N} \frac{b_{i-1} I}{2^{i-1}} = V_{ref}\left(\frac{R_F}{R}\right)\sum_{i=1}^{N}\frac{b_{i-1}}{2^i} \quad (2.15)$$

However, as already mentioned, although the resistance ratio has been reduced, the current ratio through the switches is still large, and thus the switch sizes are usually scaled in size to accommodate the widely varying current levels. One approach to reduce this current ratio is shown in Fig. 2.10, where equal current flow through all the switches. However, this configuration is typically slower since the internal nodes of the R-2R ladder now exhibit some

voltage swings.

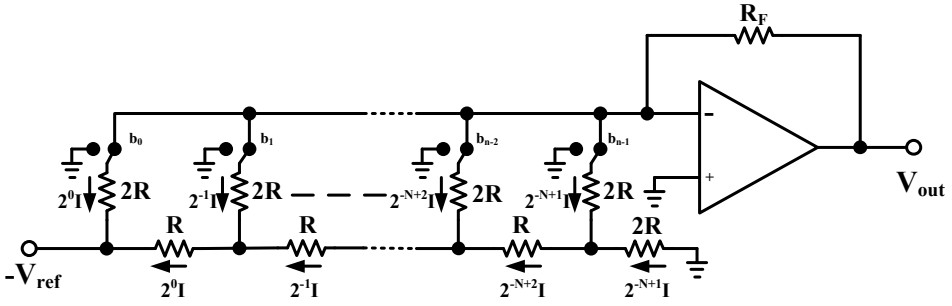



**Figure 2.10 N-bit R-2R based DAC**

## 2.3.2 Charge Redistribution DAC

The charge redistribution DAC is a switch capacitor (SC) circuit, where the charge stored on a number of binary weighted capacitors is used to perform the conversion. Fig. 2.11 is an example of a N-bit converter. Typically, the weighted capacitors are created using a number of unit capacitors.

At time $nT$ ( on phase $\phi_1$ ), the bit $b_i$ determine which of the binary weighted capacitors that should be charged from the reference voltage, $V_{ref}$ . During this phase, the plates of capacitor $C_N$ are connected to ground and virtual ground at the input of the op amp, i.e., there is no charge on $C_N$, and $q_N(nT) = 0$. Capacitor $C_C$ is used for offset compensation.

The total charge on the binary weighted capacitors at time $nT$ is given by

$$q_T(nT) = V_{ref}\sum_{l=0}^{N-1} C_l \cdot b_l = V_{ref}\sum_{l=0}^{N-1} 2^l \cdot C \cdot b_l = V_{ref} \cdot C \cdot k(nT) \qquad (2.16)$$

At time $nT + T/2$ , on phase $\phi_2$, the weighted capacitors are discharged since their plates are connected to DC and virtual grounds. The charge is redistributed to ground and $C_N$ . The

charge on $C_N$ at the end of the settling is

$$q_N(nT+\frac{1}{2}T)=C_N\cdot V_{out}(nt+T/2) \tag{2.17}$$

Charge conservation gives

$$q_N(nT+\frac{1}{2}T)=-q_T(nT) \tag{2.18}$$

Using (2.11) and (2.12) in (2.13) we have

$$V_{out}(nt+T/2)=\frac{C}{C_N}\cdot k(nT)\cdot V_{ref} \tag{2.19}$$

The architecture in Fig. 2.6 is insensitive to offset voltage and finite gain of the amplifier. The limitations of the converter are the matching of the capacitors, the switch-on resistance, and finite bandwidth of the amplifier.

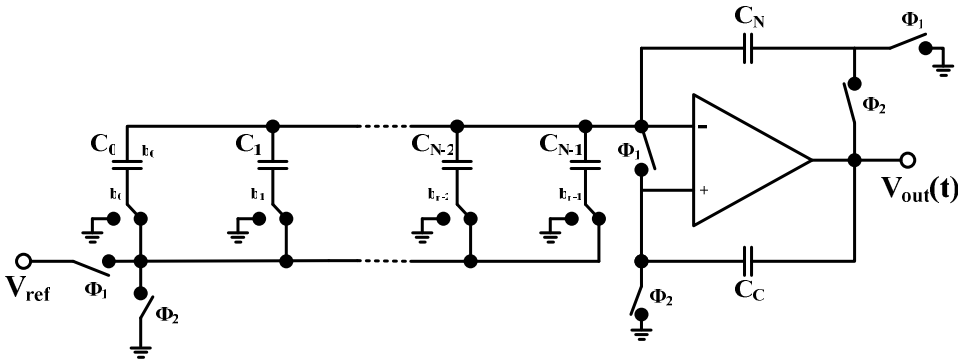



**Figure2.11 The architecture of a N-bit charge-redistribution DAC**

### 2.3.3 Current-Mode DAC

Current-mode DACs are very similar to resistor-based converter, but are intended for higher-speed applications. The basic idea is to switch currents to either the output or to ground, as shown in Fig. 2.12.

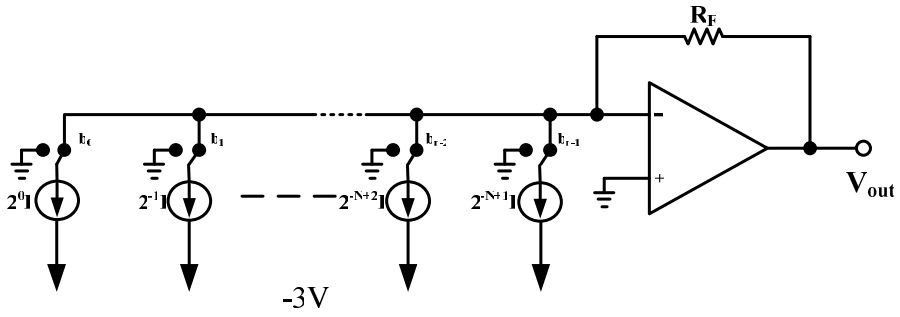



**Figure2.12 N-bit binary-weighted current-mode DAC**

Here, the output current is converted to a voltage through the use of $R_f$, and the upper portion of each current source always remains at ground potential.

The technology of usable switched-current of the current-mode is gone to realize. The switched-current technique is a natural choice in a CMOS process, since reference and sum element as well as switches are relatively easy to implement. The current-steering DAC has the advantage of being quite small for resolution below 10 bits and it is very fast. The major disadvantage is the sensitivity to device mismatch, glitches, and current source output impedance for higher number of bits. Another good property of the current-steering DAC is that its high power-efficiency since all power is directed to the output. The current-steering DAC is suitable for high-speed high-resolution applications, especially when special care is taken to improve the matching of the converter.

To achieve monotonicity, reduce the influence of glitches and reduce the sensitivity to matching errors, the DAC should be segmented into a coarse and fine part. The coarse part is

realized by thermometer coded and fine part is kept binary weighted. This is referred to as a segmented converter and is discussed further.

## 2.4 Thermometer Coded DAC Architecture

The thermometer coded DAC architecture utilizes a number of equally weighted elements. The binary input code is encoded into a thermometer code as illustrated in Table 2-1 for 3-bit input code. Generally, with N binary bits, we have $M=2^N-1$ thermometer coded bits. The analog output at time nT is give by

$$X_a = A_0 \cdot \sum_{i=1}^{M} C_i(nT) \qquad (2.20)$$

where $C_i = (nT) \in \{0,1\}, 1 \le i \le M$ are the thermometer coded bits.

| Decimal | Binary | Thermometer |
|---|---|---|
| 0 | 000 | 0000000 |
| 1 | 001 | 0000001 |
| 2 | 010 | 0000011 |
| 3 | 011 | 0000111 |
| 4 | 100 | 0001111 |
| 5 | 101 | 0011111 |
| 6 | 110 | 0111111 |
| 7 | 111 | 1111111 |

Table 2-1 Decimal, binary, thermometer code representations.

In the thermometer code DAC the reference element are all equally large and the matching of the individual element becomes simpler than for the binary case. The total sum of all weights is $2^N-1$. The transfer function of the thermometer code converter is monotonic and the DNL and INL is improved compared to the binary version. The requirements on element

matching are also relaxed. In fast, if the matching is within a 50% margin, the converter is still mon0tonic.

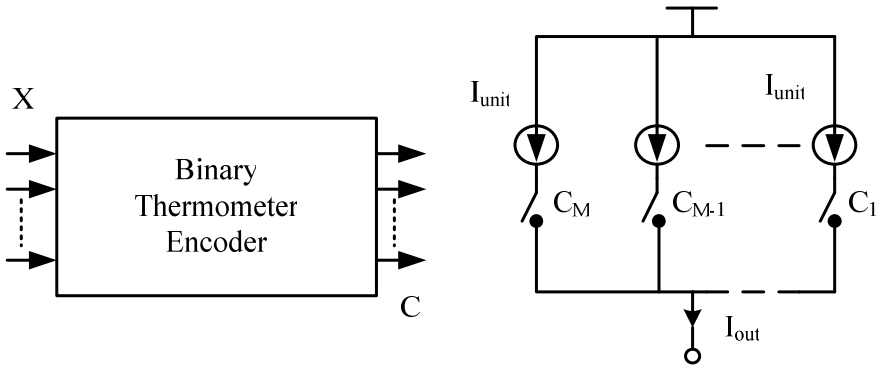



Figure 2.13 A thermometer coded current-steering DAC with encoding circuit

In Fig. 2-13 we show a current-steering implementation of a thermometer coded DAC with binary-to-thermometer encoder. All current sources are equally large, $I_{unit}$. For a large number of bits, the digital circuit converting the binary code (X) into thermometer code (C) and the number of interconnecting wires become large, since the number of outputs is growing exponentially. This implies a more complex circuit layout. The encoding circuit can easily be pipelined and the propagation time through the encoder can be controlled.

## 2.5 Hybrid DAC Architecture

Combining the techniques discussed in Fig. 2-14 for realizing different portions of a D/A converter result in hybrid designs. Hybrid designs are an extremely popular approach for designing converters because they combine the advantages of binary-weighted and thermometer-coded architectures. For example, it is quite common to use a thermometer-code approach for the top few MSBs while using a binary-scaled technique for the lower LSBs. In this way, glitch is significantly reduced and accuracy is high for the MSB where it is needed

most. However, in the LSBs where glitch and accuracy requirements are much reduced, valuable circuit area is saved with a binary-scaled approach.

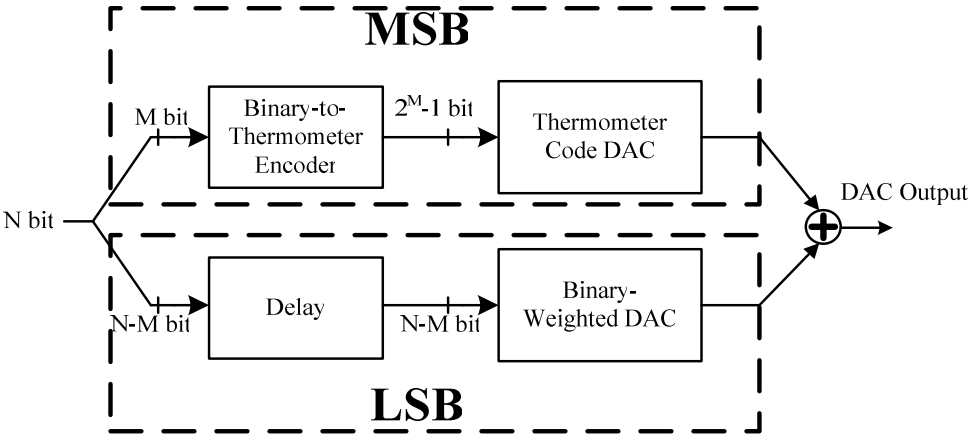



Figure 2-14 A N-bit segmented DAC where M MSBs are thermometer-code

## 2.6 Summary

In this chapter, the fundamental of the digital-to-analog Converters (DACs) is presented first. The performance parameters used to characterize the specifications of DAC is also described. Also, different types of Nyquist-Rate DACs are introduced.

According to the discussions of the advantages and disadvantages for different type DACs, we can choose the suitable architecture for our applications among several trades-off, like power consumption, speed, and die area.

# *Chapter3*

# System Analysis of DAC Design

Current-steering DAC is a popular topology when high speed and high resolution is needed since it can drive resistive loads directly, and do not require high speed amplifiers at the output. A differential output type current steering DAC is preferred because it can lower the common mode noise and second harmonic distortion. But it still has some non-idealities that will degrade the performance of the DAC. The errors sources that cause the non-idealities include finite output impedance effect, current source mismatch, timing non-idealities and non-idealities due to switching the current cells [1].

## 3.1 Major Error Sources in Current-steering DACs

**Output impedance of current source:**

The finite output resistance affects the linearity of the converter. This is primarily due to the fact that the output resistance of the converters is signal-dependent. We often use the cascsde structure to increase the output impedance of current source.

**Matching errors:**

Matching errors in the process cause the oxide thickness and threshold voltage, to vary, the unit currents are unequal, which also affects the linearity. The matching errors are of both stochastic and deterministic nature.

**Doping and thermal gradients:**

Since doping and thermal gradients oxide thickness and mobility to vary, the unit

currents are unequal, which also affects the linearity. This error is often overcome by using the careful unit-cell placement.

**Edge effects**:

Edge mismatch error occurs when the element does not see the same surroundings within a certain radius around them. This error is often eliminated by placing a number of dummy rows and columns around current source arrays and the external cost is the area of dummy current source.

**Increased Random Noise:**

An increase in the noise floor in the signal band reduces the dynamic range of the converter. Sources of random noise include the thermal noise of transistors and resistors and the coupling of noise from digital circuitry into the analog circuits through the common substrate, package, and supply lines.

**Harmonic Distortion:**

Signal-dependent non-idealities result in harmonic distortion in the DAC output. Ideally, even harmonics are completely cancelled through the use of a differential topology, but mismatch between the differential paths results in some residual even-harmonic distortion. In the following section, we discuss the non-idealities of current-steering DAC and the effects they will cause on both static performance and spectrum specification.

## 3.2 Finite output impedance of current source

The output impedance and the parasitic impedance of interconnections and switches in the converter will strongly influence the performance. Any non-ideal current source has a finite output resistance and can be modeled [1].

Fig. 3.1 shows a current-steering array including output impedance of each current source. It is a thermometer coded structure, where $R_o$ represents the output impedance of each

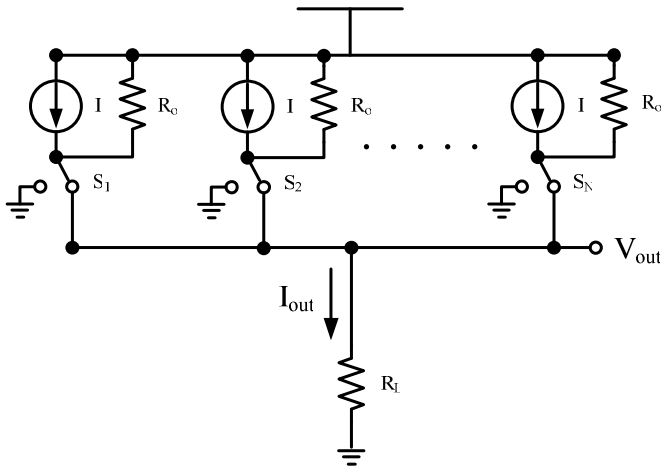



Figure 3.1 Current sources with finite output impendence

current source. For the thermometer code of height N, the actual output voltage is

$$V_{out,N}=NI\left(R_L \| \frac{R_0}{N}\right) \tag{3-1}$$

therefore the ideal output voltage for height j is

$$V_{out,j}=jI\left(R_L \| \frac{R_0}{N}\right) \tag{3-2}$$

The difference between the ideal and actual voltage can result in INL error

$$INL_j=jI\left(\frac{R_L R_o}{R_o+jR_L}-\frac{R_L R_o}{R_o+NR_L}\right)=\frac{IR_L^2}{R_o}j(N-j) \tag{3-3}$$

Fig. 3.2 shows an example of INL profile for a 12-bit DAC with variable current source

output impedance. From the figure we can find that INL decreased when the current source impedance increases. Also, the maximum INL value occurs when the middle digital input is applied.

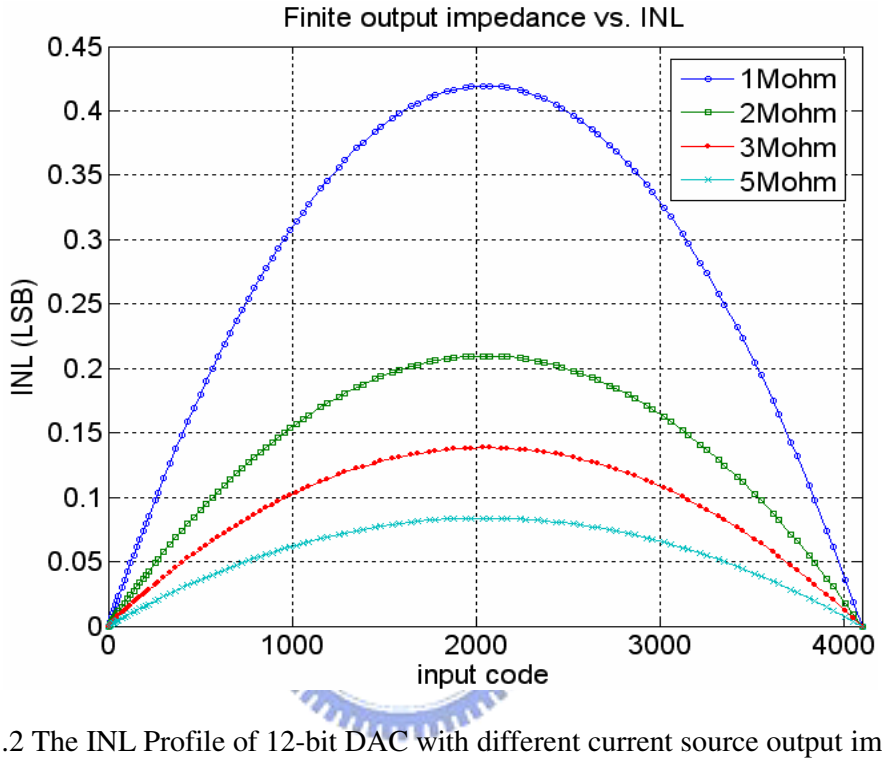



Figure 3.2 The INL Profile of 12-bit DAC with different current source output impedance

Besides of static linearity, the finite output impedance of the current sources also has relation with dynamic performance. The SFDR is an index between dynamic performance and output impedance. The equation of SFDR can be calculated as

$$SFDR=\left\{\frac{1+\rho\bullet K_{dc}}{\rho\bullet K_{ac}}+\left[\sqrt{\left(\frac{1+\rho\bullet K_{dc}}{\rho\bullet K_{ac}}\right)-1}\right]\right\}^{2} \qquad (3\text{-}4)$$

where

$$K_{ac}=K_{dc}=\frac{2^{N}-1}{2},\ \rho=\frac{R_{L}}{R_{o}} \qquad (3\text{-}5)$$

In general, output impedance of current source is farther great than output loading. When ρ is very high, the approximate equation can be written as

$$\text{SFDR} \approx 40\log\left(\frac{1}{\rho}\right)\text{-}12\left(\text{N-}2\right)\text{dBc} \qquad (3\text{-}6)$$

Figure 3.3 shows another example how the output impedance affects the SFDR for differential output. This implies the output impedance of unit current source must be larger than 3MΩ if the SFDR is guaranteed to larger than 72dB.

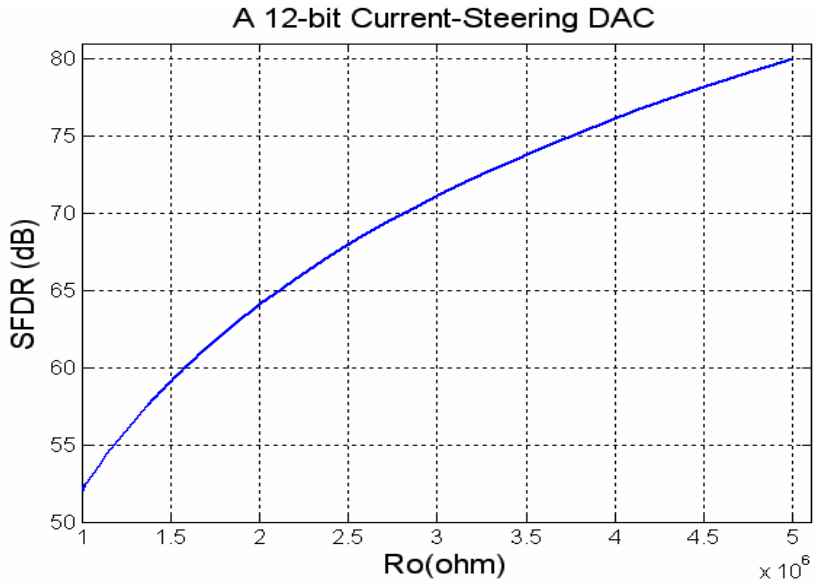



Figure 3.3 Simulate SFDR in different output-impedance conditions

## 3.3 Current Source Mismatch

Intrinsic high linearity can be achieved by tacking all possible systematic, graded, and random errors. Important effects that must be taken are

1. Random errors: device mismatches.
2. Systematic and graded errors: edge effects, voltage drops in the supply lines,

thermal gradients, doping gradients, and oxide thickness gradients resulting in a $V_t$ shift across in the die.

In Fig3.4 show the average simulated and calculated SFDR for 12-b DAC with 8MSB thermometer-coded that have different mismatch pattern. Specifically input signal was formed by adding dither to the signal where amplitude is full swing, the ratio of the input signal frequency $F_{in}$ to clock frequency $F_{clk}$ is 1/4, and then quantizing the result to the resolution of DACs. The dither added to the sinusoidal input, was a while sequence with a triangular probability density function supported on, so the quantization error was white noise[15]. The curves are saturated at low mismatch, since in the simulations the harmonics are hidden in the noise floor.

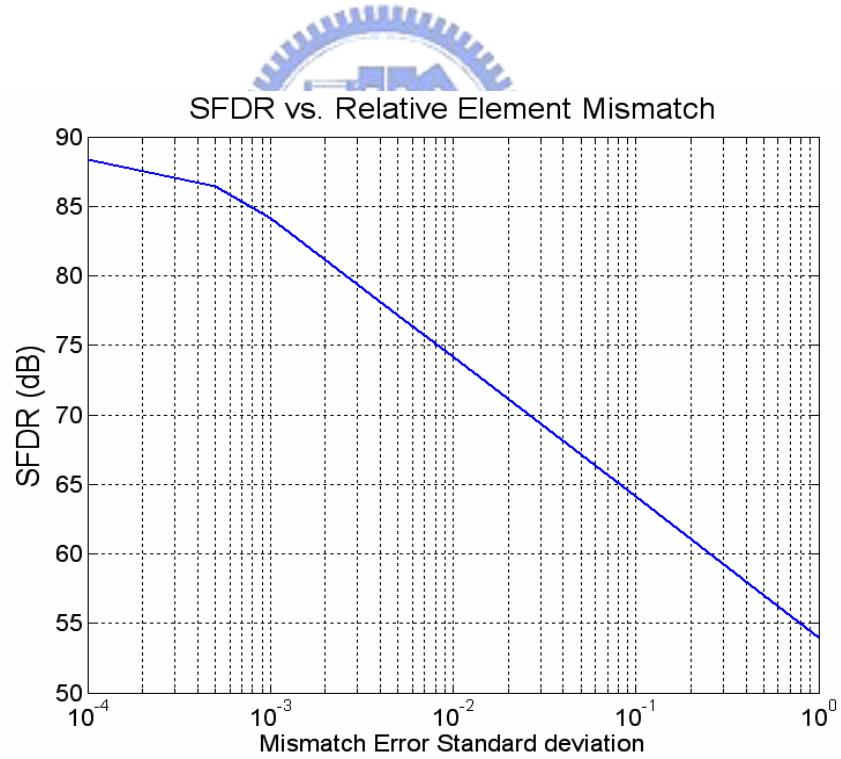



Figure 3.4 The average simulated and calculated SFDR for a 12-bit DAC with 8MSB thermometer-coded that have different mismatch pattern

The random error of the current sources is determined by matching properties of the

MOS transistors. Consider two normally identical current sources and random mismatch between two identical devices as shown in Fig. 3.5. The output currents $I_1$ and $I_2$ exhibit mismatch components due to mismatch between transistors $M_1$ and $M_2$. The nominally identical devices suffer from a finite mismatch due to uncertainties in each step of the manufacturing process. For example, the gate dimensions of MOSFETs suffer from random, microscopic variations and hence mismatches between the equivalent lengths and widths are laid out [19].

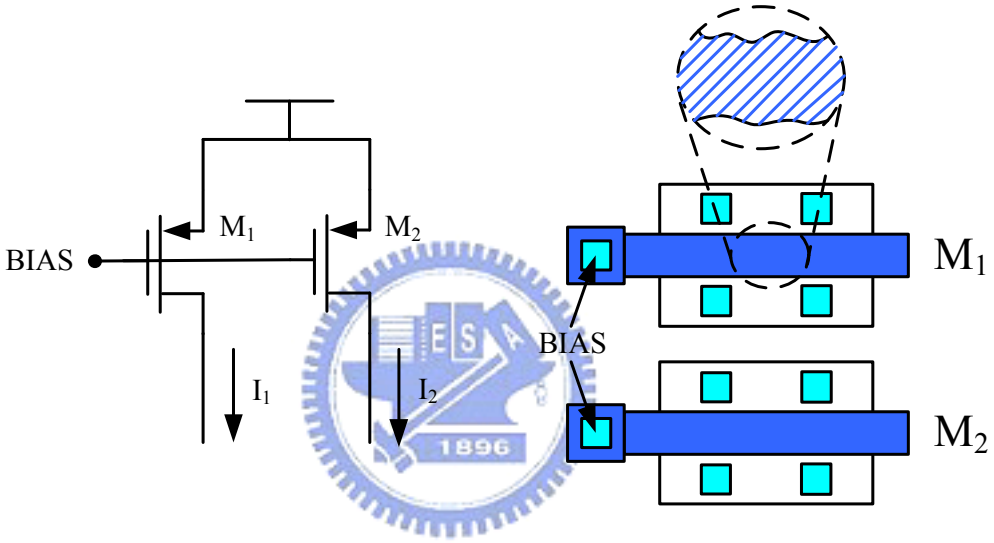



Figure 3.5 Identical MOS current sources and random mismatch between two identical devices

For Fig. 3.4, assume $M_1$ and $M_2$ are nominally identical and have square-law I-V characteristics：

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{GS} - V_T\right)^2 \tag{3.7}$$

Usually we increase $W$, $L$, and $V_{GS}$ to lower the mismatch in the drain current. However, larger W leads to higher drain-substrate and gate-drain capacitance and large area,

larger L requires higher $V_{GS}$-$V_T$ to attain a given $I_D$, and increasing $V_{GS}$-$V_T$ limits the voltage swing at the drain of $M_1$ and $M_2$. As a consequence, some compromise is usually necessary to obtain a reasonable combination of accuracy, speed, and output voltage swing.

In order to reduce to effect of current mismatch, proper dimensions of current sources should be chosen. An estimation of the minimum channel area of transistor versus mismatch parameters are described as follow [13]：

$$I_D = \frac{1}{2}\beta\left(V_{GS} - V_T\right)^2 \tag{3.8}$$

Where $\beta=\mu C_{ox}(W/L)$, the relative current mismatch is

$$\sigma^2\left(\frac{\Delta I}{I}\right) = \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + 4\frac{\sigma^2(\Delta V_T)}{\left(V_{GS} - V_T\right)^2} \tag{3.9}$$

According to [6], the minimum size of current source is equal to

$$\left(WL\right)_{\min} = \frac{\frac{1}{2}\left[A_\beta^2 + \frac{4A_{VT}^2}{\left(V_{GS} - V_T\right)^2}\right]}{\left(\frac{\sigma_I}{I}\right)^2} \tag{3.10}$$

Where

$$\sigma^2\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta}{WL} \tag{3.11}$$

$$\sigma^2(\Delta V_T) = \frac{A_{VT}}{WL} \qquad (3.12)$$

The parameter $A_{VT}$ and $A_\beta$ are technology parameter, depended on the given process. From (3-10), we can see that the minimum area of the current source, $(WL)_{min}$ , is function of overdrive voltage, $(V_{GS}\text{-}V_T)$ , and the current mismatch standard deviation ( $\sigma_I/I$ ). By increasing the overdrive voltage, and minimum area required for current source can be decreased.

Fig 3.6 shows the required gate-area of the unit current source transistor as function of $(V_{GS}\text{-}V_T)$. By increasing the $(V_{GS}\text{-}V_T)$, the minimum area required can be decreased. For very large values, however, the mismatch is mainly determined by the $A_\beta$ term and barely decrease with the $(V_{GS}\text{-}V_T)$. Consequently, a convenient criterion to determine the gate overdrive voltage of the current source transistor is to make the two mismatch contributing terms in about equal.

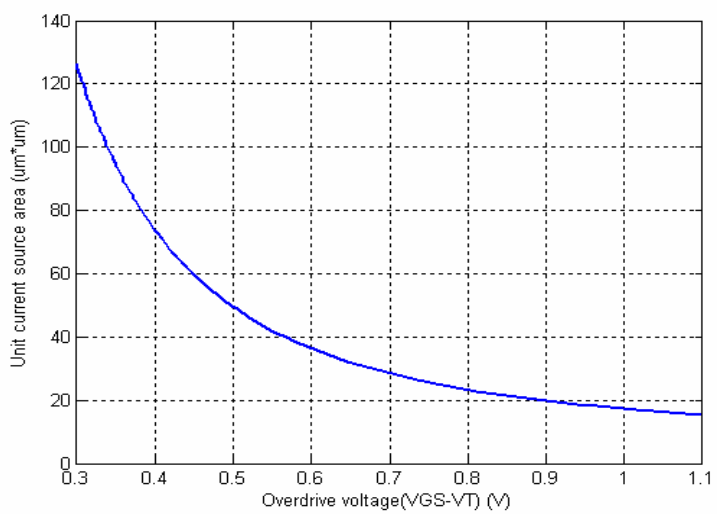



Figure 3.6 Minimum gate-area of the unit current source transistor as function of the gate voltage overdrive

Systematic and graded errors have become an important concern in high-resolution converters. Major sources of gradient error are oxide thickness and dopant variation. These parameters vary smoothly enough that they could be considered linear over the active area of D/A converter. Systematic and graded errors result from parameter variations, such as temperature generated within the active area of the converter.

If the resolution of the DAC increases by a single bit, the number of current-source array doubles. The area occupied by a single unity current source also doubles because of random matching constraint. This leads to a four times area increase for the current source array for each additional bit. For DAC with a resolution of 10-bit and higher, the dimension of the current source array become so large that process, temperature, and electrical gradients have to be considered. The nonlinearity errors introduced by these gradients can be partially compensated by the introduction of a special switching scheme. We only focus on the error source here.

The current error caused by the voltage drop in the ground lines is given by [8]

$$i_{voltage\ \ drop}(x) = \sqrt{g_m R_{gnd}}\ \frac{\cosh(\sqrt{g_m R_{gnd}}\, x)}{\sinh(\sqrt{g_m R_{gnd}})} \approx a_0 + a_1 x^2 + \ldots \qquad (3.13)$$

where x is the coordinate of the current source along the ground line.

It is well know that wafers exhibit, in general, a radial pattern in the oxide thickness. This gives rise to a shift in the nominal values of the current sources approximately linear with the devices separation distance. On the other hand, temperature gradients and stress gradients are responsible for errors approximately parabolic across the array matrix.

The thermal gradients and technology-related errors are approximated by a Taylor

series expansion around the center of the current source array.

$$i_{thermal,technology,\cdots}(x,y) = b_0 + b_1 x + b_2 y + b_3 xy + b_4 x^2 + b_5 y^2 + \cdots \qquad (3.14)$$

where (x,y) is the coordinate of the unit in the current source array.

The current source array thus contains units with errors that are (to first order) linear and (to second order) quadratic in spatial distribution. These linear and quadratic error profiles are shown in Fig. 3.7.

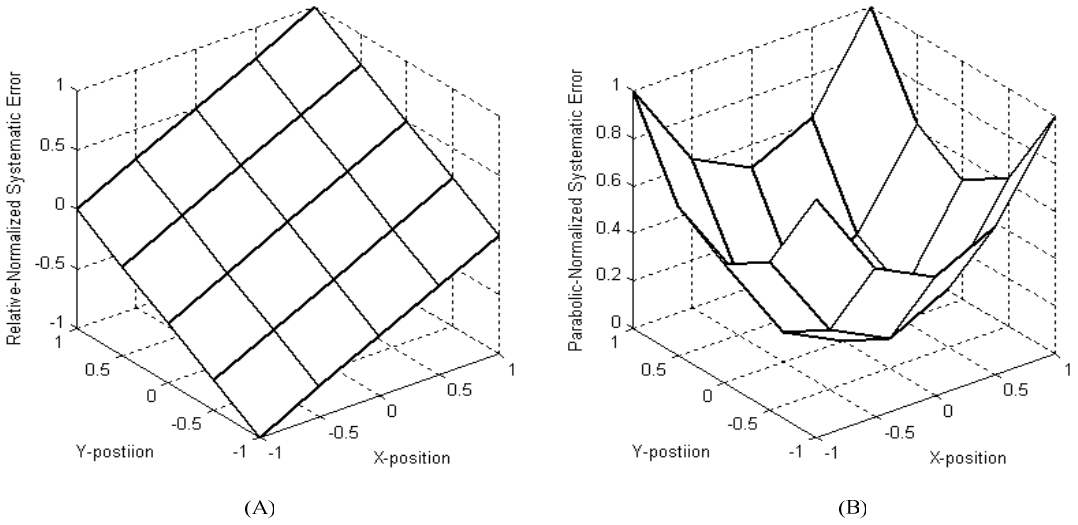



Figure 3.7 (a) Linear error (first-order error) (b) Systematic error (Second-order error) In DAC current element

The edge effect means current matching error at the edge of the current source array as shown in Fig. 3.8. It can be avoided by placing sufficient rows and columns of dummy current cells at the edges.

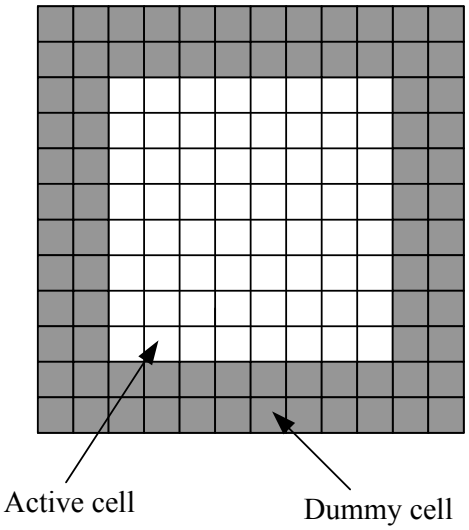



Figure 3.8 Current cell matrix with dummy cell

## 3.4 Switched Gate Driver

The differential output switch pair (M3, M4; Fig. 3.9(a)) could be driven directly with full supply rail swing outputs of the CMOS logic. This would be the lowest power solution. However, it is well known that for the best SFDR performance, the crossing point for the gate drive signals of the output current switch pair needs to be optimized [16]. The circuit that drives the differential switch should ensure that both switches are never completely off at the same time so that the current from the current source is always flowing at a constant value. This minimizes the excursion of the voltage on the switch common source node, $C_i$, during a transition. Any current lost to parasitic capacitor $C_a$ causes nonlinearity. The disturbance on $C_i$ should be symmetric around the nominal DC value. To the extent that the disturbance cannot be completely eliminated it is important that $C_a$ be minimized. It is also important to note that it is not necessary to bring the gates of the switch devices any higher than the voltage on the common source node $C_i$, when turning off the device ($V_{gs}$=0). Limiting the swing in this way reduces any feed-through of the gate drive signals to the outputs or to the common source

node.

These circuits have been proposed that limit the voltage fluctuation, by ensuring that the two switching transistors are never simultaneously switched off. This design criterion turns out to have an important positive impact on the dynamic characteristics of the DAC because any asymmetry in the output lines of each current cell give rise to a glitch at the DAC output during a code transition. The correct timing of the switching control signals is thus of crucial importance because it reduces simultaneously the voltage swing at the internal nodes and the amplitude of the glitch.

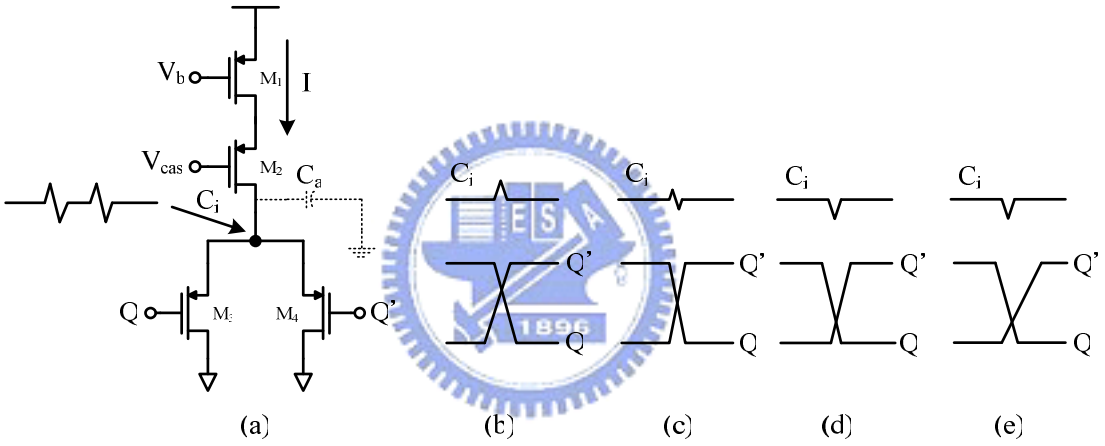



Figure 3.9 The Output waveforms of switch drivers used for driving the current cell. (a) Output switch gate waveforms (b) High crossing points due to use the driver of intrinsic delay (c) Middle crossing points (d) Low crossing points due to use the driver of intrinsic delay (e) Low crossing points due to use the driver of rise / fall time

This circuit put one switching transistor at the threshold of conducting by lowering the crossing point of the switching control signals, so that as soon as one of the switching transistors begins to switch off, the complementary switching transistor begins to switch on. Two different alternatives have been proposed: (1) circuits the use different rise/fall times [23] and (2) circuits that introduce a delay in one of the transitions [6] [8]. Both classes of circuits

have a high switching speed. Fig. 3.9 shows the waveform of crossing point of the switching driver. Fig. 3.9 (b) show the high crossing points that both the switching transistors turn on at the time of transition for using the driver of intrinsic delay. Fig. 3.9 (c) shows the middle crossing point that both the switching transistors may be off at the same time. Fig. 3.8 (d), (e) show the low crossing points that both the switching transistors turn on at the time of transition for using different types of switching drivers, as mentioned above.

## 3.5 Random routing

A major error source of DAC nonlinearity is the current source mismatch due to process and environmental variations, which includes random, gradient and quadratic errors. The gradient and quadratic errors can be effectively compensated by optimizing switching schemes or using local biasing techniques [5]. The random variation of current source are determined by the inherent properties of the technology used and can be assumed to independent from each other and follow normal distribution.

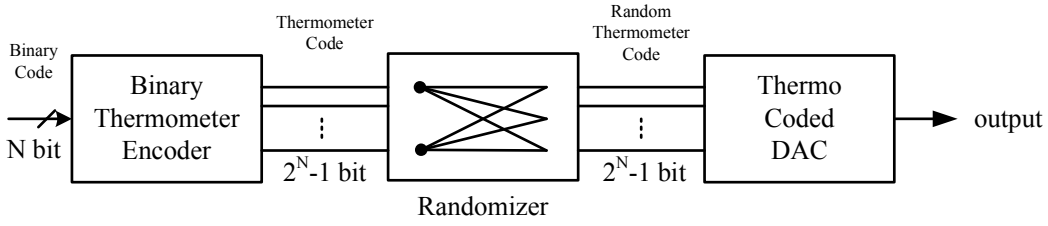



Figure 3.10 Randomization of bits in a thermometer coded DAC. The matching error becomes uncorrelated with the signal.

In a conventional thermometer code DAC, the input number (M), is represented by using $2^M$ fixed reference element in the DAC. The matching errors become strongly single-dependent, since a reference is associated with specific input code. To reduce the

distortion, the binary to thermometer encoder can be designed so that, at different times, different reference are chosen to represent M, we do not fix a reference to a certain code. If we choose the references in a way that is uncorrelated with the signal, the matching errors will no longer be signal dependent and hence the error will become noise. This is achieved by using a randomizer or scrambler as illustrated in Fig 3.10. In a real implementation the randomization can be implemented with a random generator. We can also choose to assign the references I a cyclic way, which does not give a completely uncorrelated error signal, but the improvement can be significant.

We can create MUX of L-bit input and L-bit output, hence the MUX utilizes selection to control L-way. There are MUX between local decoders and switch element. Fig. 3.11 shows a $2^{M-1}$ bit randomizer receiving at random generator controls. The random generator controls the selection of the element in the MSB part so that the harmonics caused by mismatch can be attenuated. A perfect synchronization of the control signals at the DAC, so the random generator is controlled with the clock, thus well-designed synchronized driver is used in entire circuit.

To illustrate dynamic randomization, we show in Fig. 3.12 a simulation result where a full-scale sinusoid has been applied to a 12-bit DAC with 8MSB thermometer-coded D/A converter. To all current sources in the DAC a Gaussian distributed random error with standard deviation equal to 10% is applied. In Fig 3.12(a) we find clear distortion terms and in (b) the distortion has been reduced and the noise floor has increase. The SFDR is in both cases approximately 7dB.

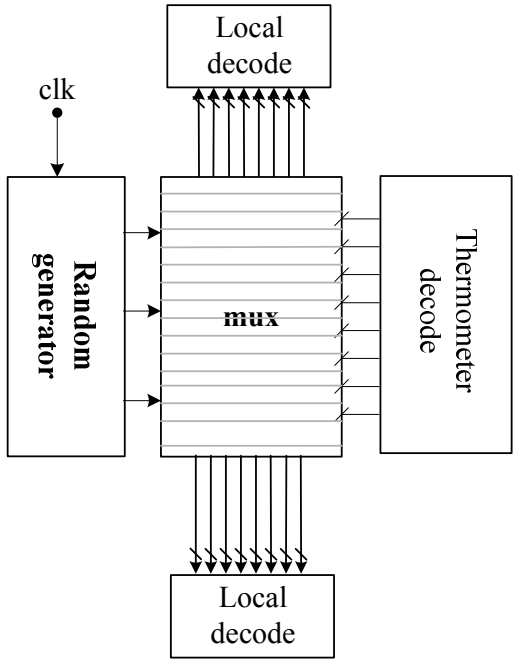



Figure 3.11 A $2^{M-1}$ bit randomizer receiving at random generator controls

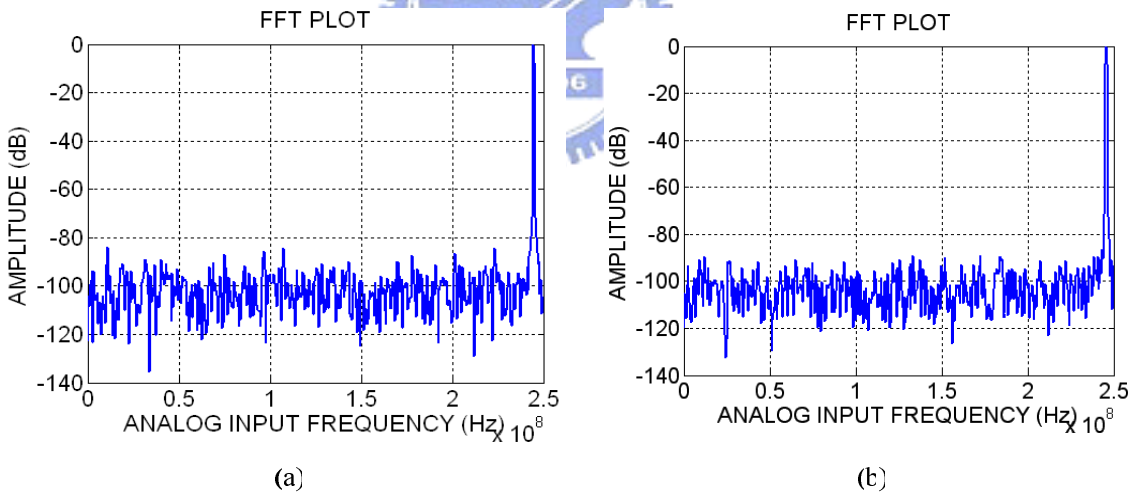



Figure 3.12 Output amplitude spectrums from a 12-bit DAC with 8MSB thermometer-coded DAC (a) without randomization and (b) with randomization

As is evident from the numerous spurs distributed across the spectrum in Fig. 3.12(a), rather severe harmonic distortion results from the static DAC-element errors in the absence of

random switching. The maximum-amplitude spur occurs at a frequency of approximately 1.5π rad, and has power 82.5 dB below the power of the desired sinusoidal signal of frequency $\omega_0$ numerous additional simulations performed by the authors show that the DAC exhibits similar behavior when driven by inputs of different frequencies. It follows that merely 82.5 dB of SFDR is provided. The data in Fig. 3.12(b) indicates that harmonic distortion is not visible with full randomization DEM. As demonstrated by the simulation results and confirmed in the following section, the DAC easily provides 90 dB of SFDR.

## 3.6 Summary

In this chapter, we determine the proper output impedance, variance, and the size of current source. We invent a simple random structure to correct the mismatch error of current source. In order to design a high-speed and high-resolution current steering DAC, we should pay more attention to these non-idealities. The approaches to improve the non-idealities are also mentioned in this chapter.

# *Chapter4*

# Circuit Design of DAC

In this chapter, the designed architecture of a 12-bit 250-MSamples/s current–steering CMOS D/A converter with the partial random element matching is introduced at first. Then each block of the DAC is presented and the circuit design is discussed. To design a high speed and high resolution DAC, we should pay more attentions to choose the proper architecture that can achieve a balance between good static and dynamic specifications versus a reasonable circuit power, area, and complexity. Besides, special layout technique is also presented to compensate the systematic and gradient errors, as mentioned in chapter 3.

## 4.1 The System Structure of DAC

The architecture of a 12-bit 250-MSamples/s current–steering CMOS D/A converter with the partial random element matching presented in this thesis is shown in Fig. 4.1. There are several blocks in this DAC, including digital circuits, randomizer, latches, current cells, and bias circuit. The input binary codes are either processed through digital circuits, then changed to thermometer codes ($B_{11} – B_4$) or simply equally delayed ($B_3 – B_0$). The processed signals then pass through the latches to keep synchronization used for driving switches of the current cells. In addition to synchronization, the latches can also reduce the glitch effect due to the drain voltage fluctuations of current sources. Finally, the current cell matrix can provide differential output currents controlled by the switches whose input signals have been synchronized. In the following, all the sub-circuitry of this DAC will be further discussed.

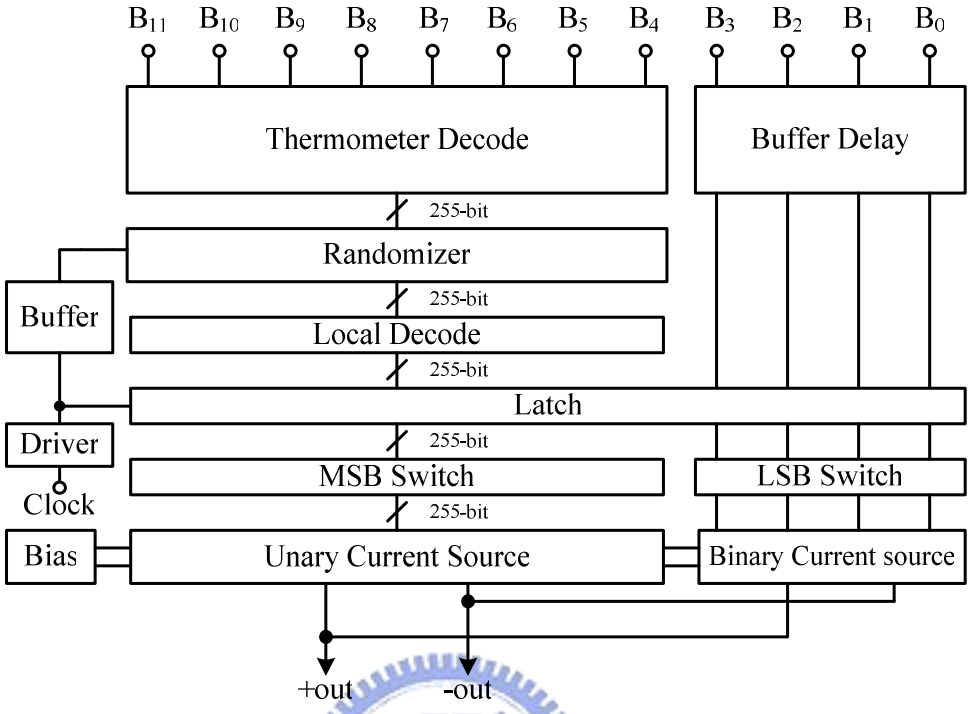



Fig. 4.1 12-bit DAC architecture

Fig. 4.2 presents the block diagram of the DAC architecture. The DAC has a 4+8 segmented architecture: first, the eight most significant bits are linearly decoded with random element matching; second, the four least significant bits are also binary weighted.

The matrix that implements the 8 MSB's is logically seen as being composed of four identical 8-bit unit elements DAC's, connected in parallel. In two of the four unit element DAC's, a two-stage row-column decoding logic and a randomizer, is implemented. The connection in parallel of four unit current sources provides the correct current scaling of the 8 MSB's relative to the four binary bits.

The remaining 4 LSB's select directly four binary weighted current sources. Note that that by removing the 4 LSB's from this architecture, one obtains also a very interesting architecture for an 8-bit resolution DAC, but with 12-bit accuracy.

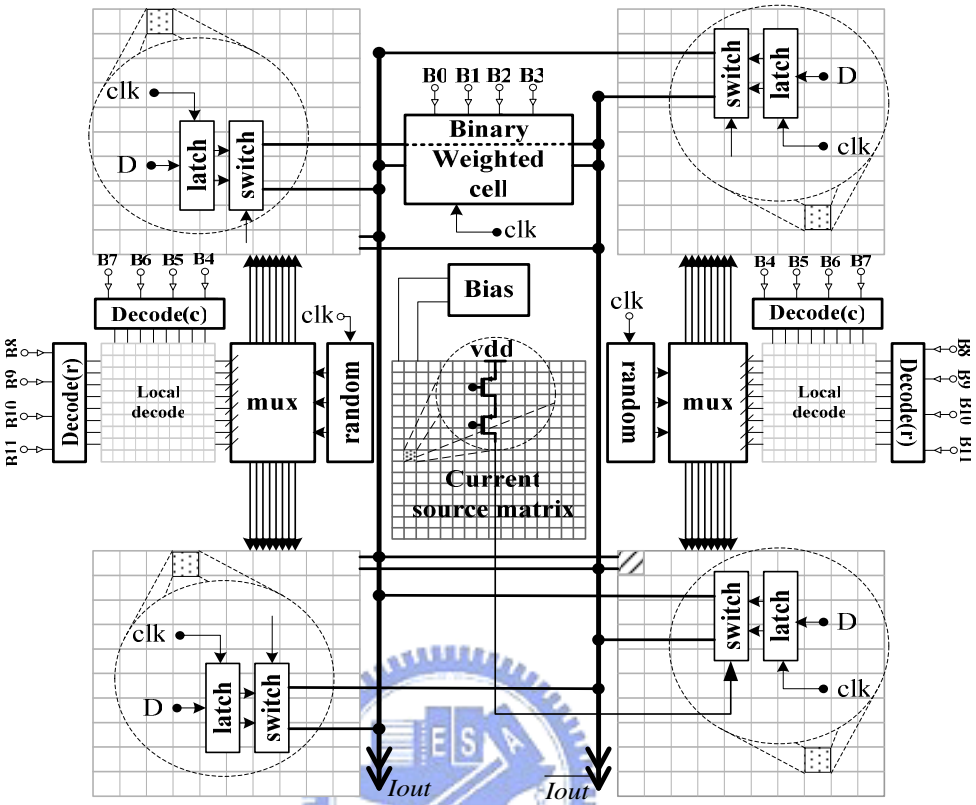



Figure 4.2 Simplified block diagram of the DAC architecture

## 4.2 Digital Circuits

In a segmented current-steering DAC, the function of the digital circuits it to convert the binary code to either thermometer code or only delayed the binary code and the digital circuit of randomizer structure and high-speed latch. To design the digital circuits, several issues should be taken into account:

- High speed operation
- Circuit complexity
- Power consumption

### 4.2.1 Thermometer decoder

Discrete quantities of information are represented in digital system by binary codes. A binary code of n bits is capable of representing up to $2^n$ distinct element of coded information. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of $2^n$ unique output lines. If the n-bit coded information has unused combinations, the decoder may have fewer than $2^n$ outputs.

Binary-to-thermometer decoder accomplishes the equivalence of elements from binary code. The Tab. 4.1 shows truth table of a 4-to-16 line decoder. The circuit of the 4-to-16 bits binary-to-thermometer decoder will be realized. Finally, the Boolean function between the binary-input and thermometer-output are described in tab. 4.2.

| Decimal | d | c | b | a | A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10 | A11 | A12 | A13 | A14 | A15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 2 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 3 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 4 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 6 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 7 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 8 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 10 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 11 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 12 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 13 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 14 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 15 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 4.1 Truth Table of a 4-to-16 Line Decoder

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| A0 | $\overline{(a+b+c+d)}$ | A1 | $\overline{(b+c+d)}$ | A2 | $\overline{(a \bullet b+c+d)}$ | A3 | $\overline{(c+d)}$ |
| A4 | $\overline{(((a+b) \bullet c)+d)}$ | A5 | $\overline{(b \bullet c+d)}$ | A6 | $\overline{(a \bullet b \bullet c+d)}$ | A7 | $\overline{d}$ |
| A8 | $\overline{((a+b+c) \bullet d)}$ | A9 | $\overline{((b+c) \bullet d)}$ | A10 | $\overline{((a \bullet b+c) \bullet d)}$ | A11 | $\overline{(c \bullet d)}$ |
| A12 | $\overline{(a \bullet b+c+d)}$ | A13 | $\overline{(b \bullet c \bullet d)}$ | A14 | $\overline{(a \bullet b \bullet c \bullet d)}$ | A15 | 1 |

Table 4.2 Boolean functions between the binary-input and thermometer-output

From the Fig. 4.2, the system block diagram reveals that one kind of 8-bit thermometer decoder is essential. The 8-bit thermometer decoder is divided into tow 4-bit thermometer decoder. Row-column selection decoding is a simple method to supply high speed transformation [6]. In high speed realization, the adopted decoder can limit the clock rate of the D/A converter.

### 4.2.2 Randomizer

Thus, a remaining problem is to develop high resolution DAC's that achieve such low levels of harmonic distortion. In the past, random element matching techniques have been successfully applied to de-correlate the DAC noise from the input signal in various DAC topologies.. For most digital input values, there are many possible input codes to the bank of randomizer that nominally yield the desired analog output value. Thus, the DAC noise arising from errors introduced by the randomizer can be "scrambled" by randomly selecting one of the appropriate codes for each digital input value. Although DAC's based on this approach have been shown experimentally [23], and through quantitative analysis [19] to achieve excellent SFDR's.

Fig. 4.3 (a) shows a $2^M$ bit input and $2^M$ bit output randomizer. The random control bit is common to a random generator. Fig. 4.3 (b) shows 8-bit input and output MUX with 3-bit selection. The random generator controls the selection of the element in the MSB part so that the harmonics caused by mismatch can be attenuated. A perfect synchronization of the control signals at the DAC, so the random generator is controlled with the clock, thus well-designed synchronized driver is used in entire circuit. Fig 4.4 shows the circuit of random generator.

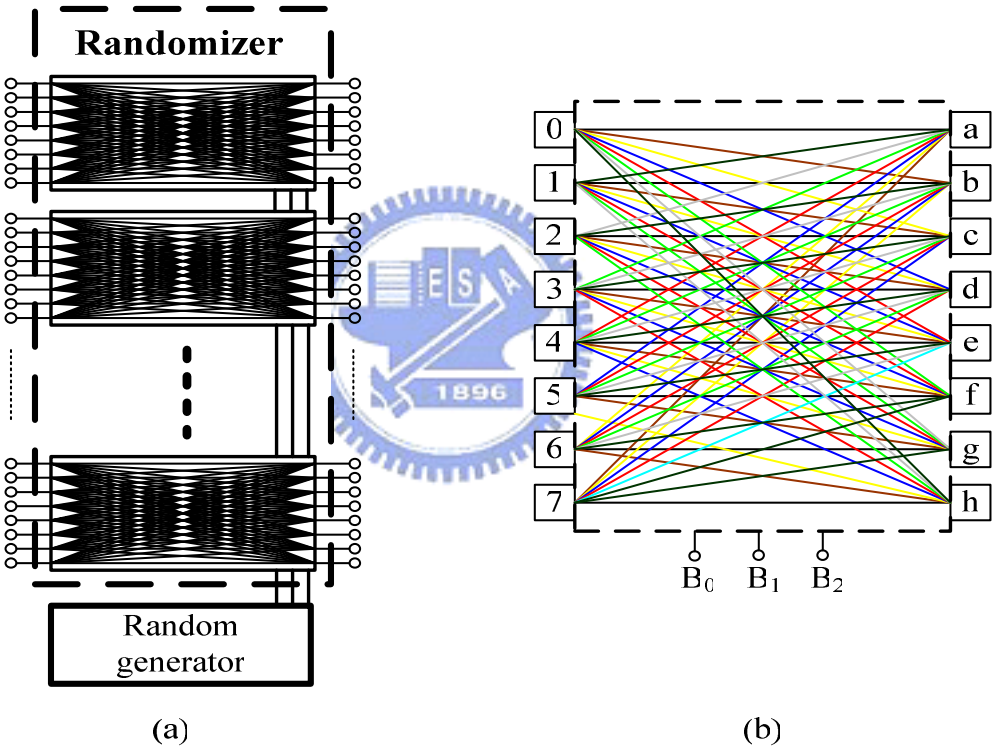



Figure 4.3 (a) A $2^M$ bit input and $2^M$ bit output randomizer (b) 8-bit input and output MUX with 3-bit selection.

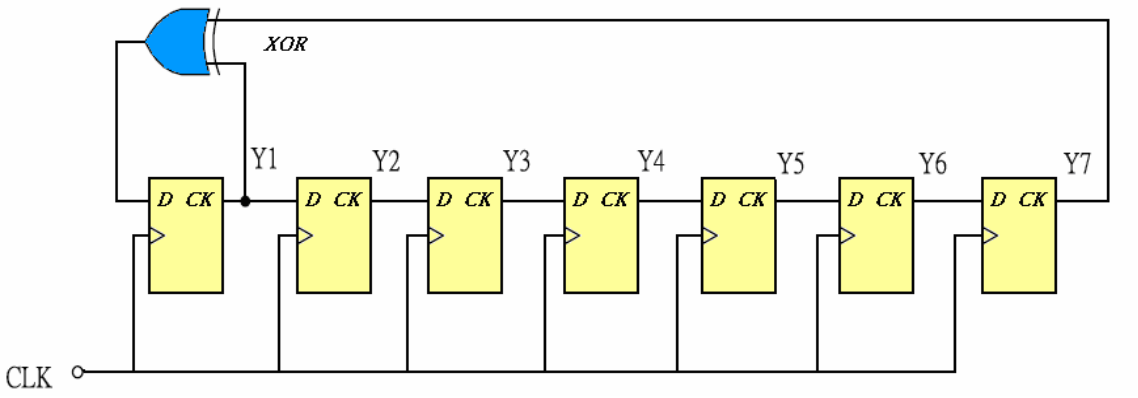



Figure4.4 Random generator

### 4.2.3 High speed latch

The dynamic performance degradation of a current-steering DAC can be caused by several reasons associated with current source switching. Some important issues that have been identified to cause dynamic limitations are:

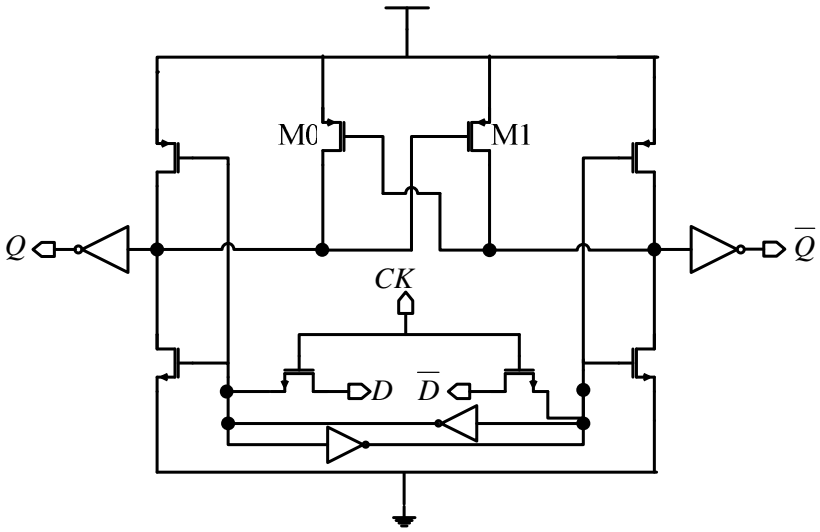
- Imperfect synchronization of the control signals at the switches.
- Drain-voltage variations of the current-source transistors caused by the fact that both switch transistors are simultaneously in the off state.
- Coupling of the control signals through the $C_{gd}$ of the switches to the output.

To minimize the three effects, a well-designed synchronized driver is used. The high speed, low glitch latch is illustrated in Fig. 4.5(a). It provides two complementary signals needed at the input of the current switches.

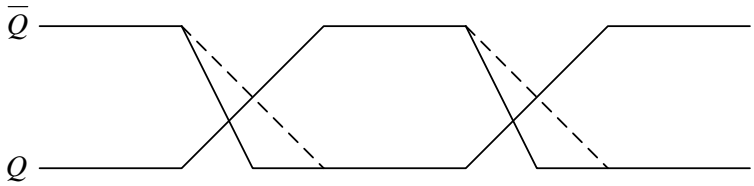
In the conventional latch, both switches will be off for a short period. As a result, the capacitance at the drain of the current source transistor will be charged and then the current source will turn off. To recover the normal operation, the current source must progress through the linear region and back into saturation. Hence, turning off the current source not

only slows down the speed but also increases glitch at the output. To solve the problem, the function of this latch is designed to shift down the crossing point of the differential signals used for driving the switches of the current cell.

The latch used here is a rise/fall time based driver. In order to obtain instantaneous change for output node with falling input, extra PMOS transistors (M1 and M2) are placed in parallel with each other cross-coupled at the top of the circuit. When the transitions of input signals (high → low or low → high) occur, the transistors M3-M10 will immediately change their states. However, the crossed-coupled PMOS transistors M1 and M2 will hold their states for a short period. After these transistors change their states, the charging speed will be increased. Thus, the combination of the ($\mu_n$ / $\mu_p$) scaled PMOS transistors and the PMOS positive feedback loop results in the rise time that is much faster than the fall time of the driver circuit. Due to the use of two additional inverters at the output of the driver and properly sizing the transistors of the whole latch, a lower crossing point can be realized. Fig. 2 (b) shows the voltage waveforms of the differential outputs, $Q$ and $\overline{Q}$. This latch not only performs the final synchronization of the signals used for switching different current cells but also reduces the delay between the different digital decoders.




(a)




(b)

Figure.4.5 (a) Dynamic latch schematic diagram (b) Output signals

## 4.3 Current Cell

To generate the accurate current, several concerns should be taken into account. First, the size of the current sources should be properly designed to reduce the mismatch error between different current sources due to the fabrication. Second, the finite output impedance of each current source is designed large enough to get a good static performance. Finally, a bias circuit used to generate the bias current of current source is also required. The design considerations and circuit implementation of each circuit is described in next subsections.

### 4.3.1 Implementation of Switch Unit Current Cell

The PMOS current source has two advantages. PMOS devices built in n-well are thus shielded from the substrate. PMOS has less flicker noise than NMOS. The circuit schematic of the cascode switch current cell is shown in Fig. 4.6(a). The output impedance of the current cell which is $r_{o_{cas}} + r_{o_{cs}} \cdot \left(1 + g_{m_{cas}} \cdot r_{o_{cas}}\right)$ is very large. Beside, this design utilizes Gain-Boosting to increase the output impedance ( $A \times gm_{cas} r_{o_{cas}}$ ) in current-voltage feedback in Fig 4.6(b). The output impedance is A times the size of the cascode without Gain-Boosting. In the following content, we will continue to find out what size of current source transistor should be used. If we want to decide the size of the current cell, we need INL_yield, process parameter

($A_\beta$ and $A_{VT}$), and gate overdrive voltage ($V_{GS}$-$V_T$) . We also need to consider DAC specification, including INL and SFDR [1]

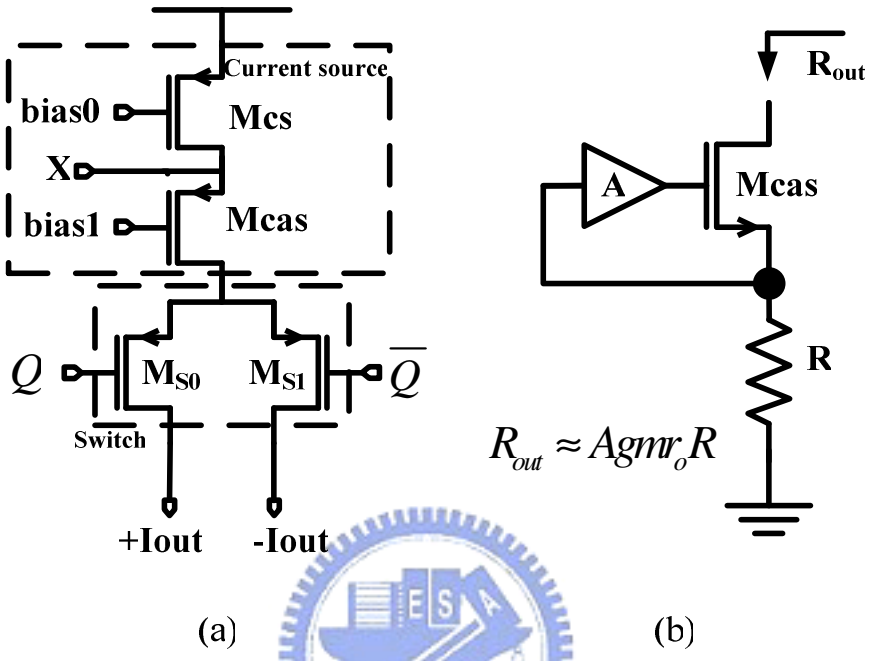



Figure.4.6 (a) The circuit schematic of the cascode current cell (b) Gain-Boosting

Using the mismatch model derived in [14], the minimum area requirement for the LSB current-source transistors is :

$$(WL)_{min} = \frac{\frac{1}{2}\left[A_\beta^2 + \frac{4A_{VT}^2}{(V_{GS} - V_T)^2}\right]}{\left(\frac{\sigma_I}{I}\right)^2} \qquad (4.1)$$

And the square-law model W/L ratio can then expressed as:

$$\frac{W}{L} = \frac{2I_{LSB}}{\beta\left(V_{GS} - V_T\right)^2} \tag{4.2}$$

In this way, we can find out the size of the current cell.

### 4.3.2 Reference Current Generation

Fig. 4.7 shows the biasing scheme for the cascode current sources. An external resistor, *R*, is used to generate the reference current. The NMOS sections of the biasing circuits are labeled as "global biasing" while the PMOS sections are labeled as "local biasing." The cascode current mirror in the current cell can be used to reduce short-channel effects and increase the output impedance, but it will limit the signal swing. In order to reduce this limitation, a wide-swing cascode current mirror bias scheme is shown in "local biasing" of Fig. 4.7. The transistors M6 is gain-boosting

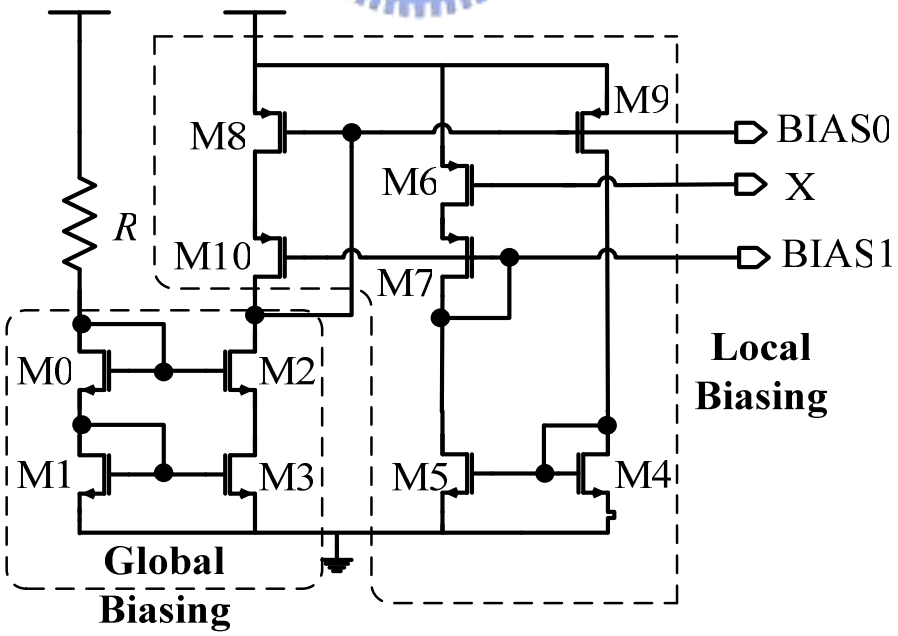



Figure 4.7 The circuit schematic of the bias circuit

## 4.4 Layout

The layout of the DAC plays an important role since the random mismatch of current source due to process variation will degrade the accuracy of the DAC significantly. Thus we should pay mode attention to the floor plan of the DAC and special layout technique should be used, like [6] , [8] and [10] . Fig. 4.8 shows “balanced ring” technique of this work for reduction of quadratic errors. We utilize this technology to divide the unit of the current cell into four groups, each group is two rings. To compensate for symmetrical and graded errors caused by temperature, process, and electrical gradients, special switching schemes should be implemented.

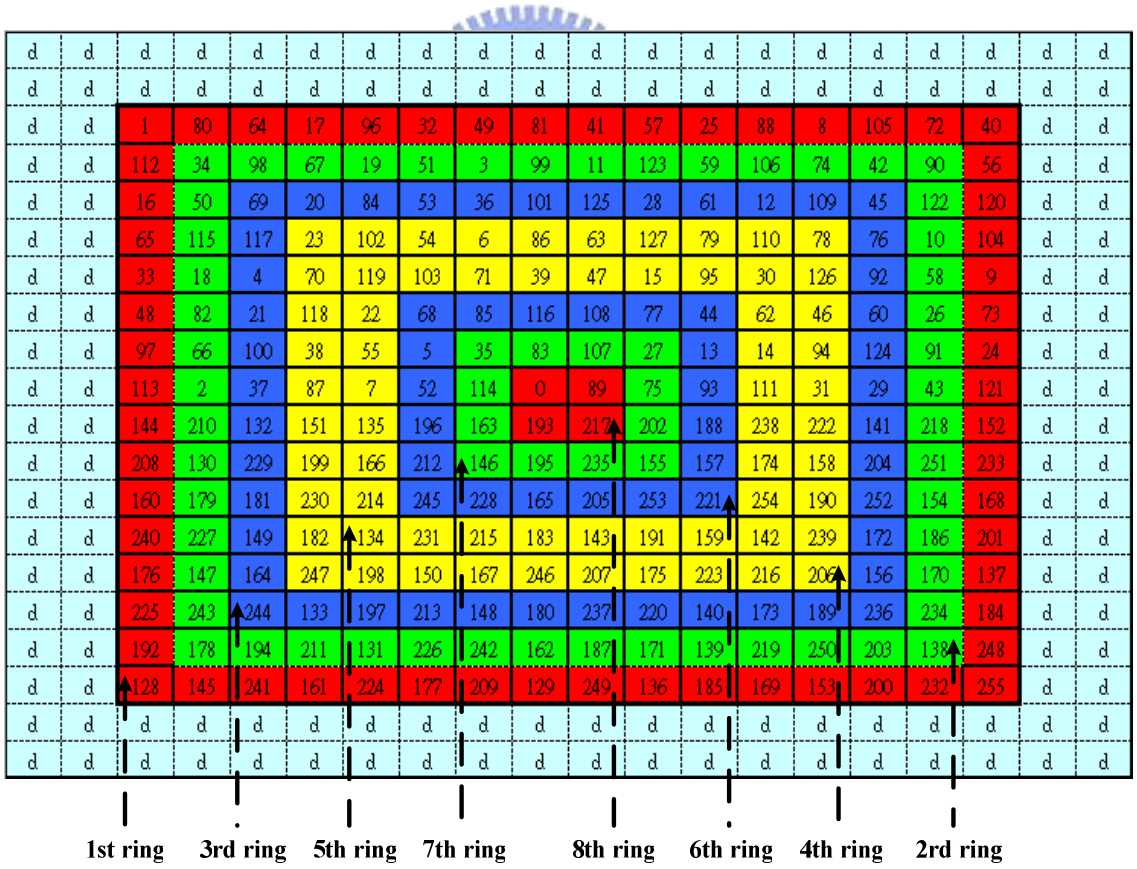



Figure. 4.8 “Balanced ring” technique of this work for reduction of quadratic errors.

(a) (1,8) rings (b) (2,7) rings (c) (3,6) rings (d) (4,5) rings

Original "balanced-ring" technology may be unable to reach match because the ones that assign are not perfect enough. So we need to utilize and calculate the way distribute the position of the current source cell again. We first consider a quadratic error oriented to the main axes of array. The origin of the coordinate system is location at the common boundary of four subschemes. The systematic error is described by

$$\varepsilon ( x , y ) = a_x^2 + b_y^2 . \tag{4.3}$$

The error for a unary source is

$$\varepsilon_{unit} = \sum_{i=1}^{16} \left( a_{x\_i}^2 + b_{y\_i}^2 \right). \tag{4.4}$$

A constant offset to all unary sources does not affect the linearity, and thus the quadratic error is cancelled.

We now consider a quadratic error with its axes rotated with respect to the array. The error is oriented along the axes x' and y' in Fig. 4.9 and is described by

$$\varepsilon(x', y') = a_{x'}^2 + b_{y'}^2 . \tag{4.5}$$

and

$$x' = x\cos(\alpha) + y\cos(\alpha) \tag{4.6}$$

and

$$y' = -x\sin(\alpha) + y\cos(\alpha) \tag{4.7}$$

After transformation, this yields

$$\varepsilon(x,y) = a(x^2\cos^2(\alpha) + y^2\sin^2(\alpha) + 2xy\cos(\alpha)\sin(\alpha)) + b(x^2\sin^2(\alpha) + y^2\cos^2(\alpha) - 2xy\sin(\alpha)\cos(\alpha)) \quad (4.8)$$

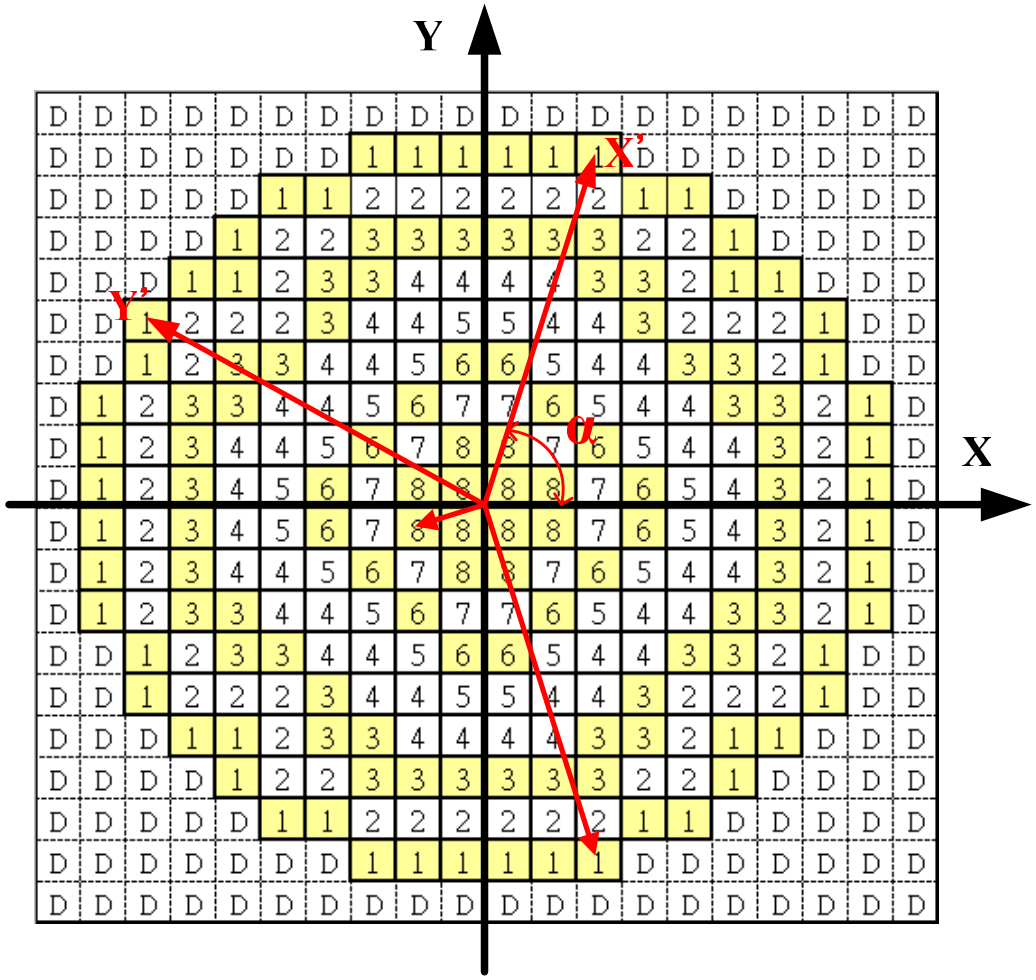



Figure 4.9 Orientation of the axes X' and Y'. Rotation of the quadratic error compared error compared to the main axes of the current source array.

The sum of terms in $x^2$ and $y^2$ is constant over each unary source, as seen above. Once again, a constant offset to all unary sources does not affect the linearity. We still need to need to

show that the sum of terms in xy is constant over each source. Let us consider the $x_i y_i$ products row by row. All sources have exactly two elements in each row, one in each half. Each row i contribute a term $x_i y_i$ and a term - $x_i y_i$ to sum. Due to this symmetry, all terms in xy are cancelled. This type of quadratic error is cancelled also.

| | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D |
| D | D | D | D | D | D | D | D | 96 | 4 | 12 | D | D | D | D | D | D | D | D |
| D | D | B1 | D | D | 140 | 52 | 193 | 42 | 26 | 187 | 180 | 164 | 116 | D | D | B0 | D | D |
| D | D | D | B0 | 64 | 162 | 70 | 102 | 58 | 122 | 62 | 158 | 86 | 34 | 76 | B1 | D | D | D |
| D | D | D | 200 | 242 | 14 | 79 | 251 | 150 | 136 | 50 | 203 | 30 | 234 | 174 | 21 | D | D | D |
| D | D | 236 | 92 | 82 | 227 | 210 | 32 | 25 | 220 | 216 | 72 | 239 | 106 | 131 | 84 | 149 | D | D |
| D | 60 | 156 | 6 | 110 | 38 | 88 | 168 | 172 | 108 | 196 | 232 | 69 | 206 | 11 | 23 | 249 | 81 | D |
| D | 224 | 138 | 178 | 134 | 160 | 184 | 152 | 240 | 46 | 120 | 16 | 188 | 56 | 142 | 219 | 95 | 113 | D |
| D | 209 | 154 | 54 | 230 | 204 | 8 | 228 | 114 | 214 | 183 | 212 | 144 | 252 | 195 | 74 | 171 | 133 | D |
| D | 48 | 222 | 127 | 66 | 104 | 177 | 146 | 19 | 1 | 167 | 246 | 245 | 44 | 119 | 199 | 190 | 101 | D |
| D | 40 | 2 | 90 | 28 | 124 | 36 | 98 | 128 | 254 | 129 | 99 | 37 | 125 | 29 | 91 | 3 | 41 | D |
| D | 100 | 191 | 198 | 118 | 45 | 244 | 247 | 166 | 0 | 18 | 147 | 176 | 105 | 67 | 126 | 223 | 49 | D |
| D | 132 | 170 | 75 | 194 | 253 | 145 | 213 | 182 | 215 | 115 | 229 | 9 | 205 | 231 | 55 | 155 | 208 | D |
| D | 112 | 94 | 218 | 143 | 57 | 189 | 17 | 121 | 47 | 241 | 153 | 185 | 161 | 135 | 179 | 139 | 225 | D |
| D | 80 | 248 | 22 | 10 | 207 | 68 | 233 | 197 | 109 | 173 | 169 | 89 | 39 | 111 | 7 | 157 | 61 | D |
| D | D | 148 | 85 | 130 | 107 | 238 | 73 | 217 | 221 | 24 | 33 | 211 | 226 | 83 | 93 | 237 | D | D |
| D | D | D | 20 | 175 | 235 | 31 | 202 | 51 | 137 | 151 | 250 | 78 | 15 | 243 | 201 | D | D | D |
| D | D | D | B1 | 77 | 35 | 87 | 159 | 63 | 123 | 59 | 103 | 71 | 163 | 65 | B0 | D | D | D |
| D | D | B0 | D | D | 117 | 165 | 181 | 186 | 27 | 43 | 192 | 53 | 141 | D | D | B1 | D | D |
| D | D | D | D | D | D | D | D | 13 | 5 | 97 | D | D | D | D | D | D | D | D |
| D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D | D |

Figure.4.10 Selection sequence for MSB part of input code for improved “balanced-ring” technique

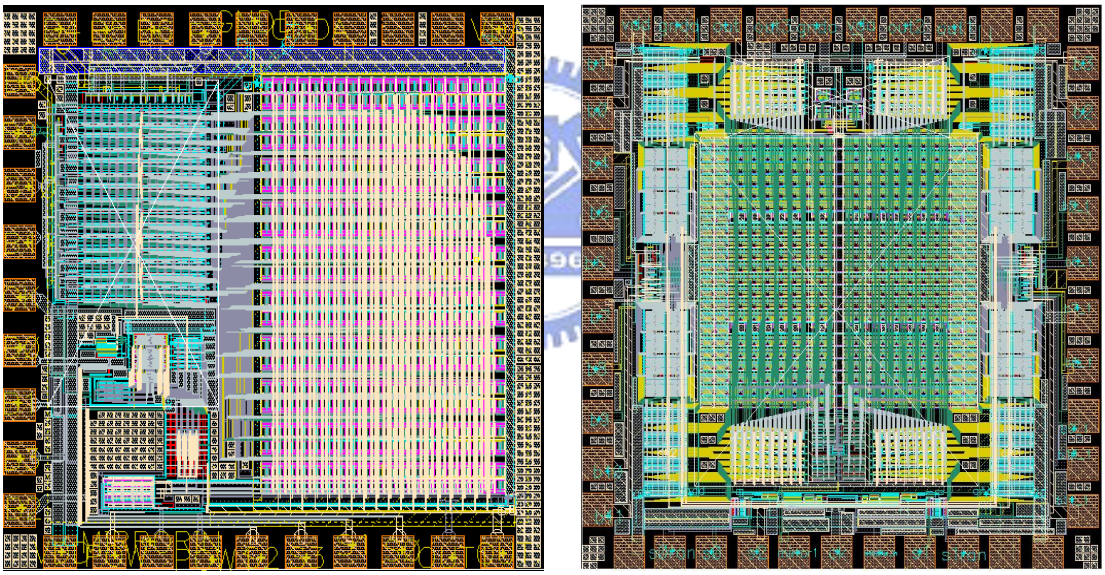
In this design a floor plan of current cell matrix called improved “Balanced-ring” is used, as shown in Fig. 4.10. In the improved “balanced-ring” technique, the array is subdivided into rings as shown by rings 1 to 8. First, we add up the quadratic errors of the cells within each ring. Then, starting from the ring 1 and 8, we determine how many of the ring 2 and 7 and ring 3 and 6 and ring 4 and 5 are required to cancel the error in ring 1 and ring 6. It turns out that eight rings will do the job as shown in Fig. 4.8. Due to systematic and quadratic effects, the parameters of the transistors vary depending on their location in the current source array. A good switching sequence switches the sources so that the errors do not accumulate, is seen in Fig. 4.9. Now in each step we select the cells from counterpart rings in a way that avoids accumulation of quadratic errors, as described above. Of course all these selections also obey the procedure.

Dummy cells and bias circuits can be placed in the “d” cell matrix. But additional rows or columns of dummy current source will not cause significant area increase of the current cell matrix.

Fig. 4.11 (a) shows A 12-bit 250MHz current-steering segmented architecture DAC without the partial random element matching. The digital part of the DAC is placed on the left and the current cell matrix is placed on the right. Fig. 4.11 (b) shows A 12-bit 250MHz current-steering segmented architecture DAC with the partial random element matching. The current source is placed on the middle and the digital part of the DAC is placed on both sides. To minimize the systematic error introduced by the voltage drop in the ground lines of the current-source transistors, wide sheets of metal have been used. Special care has been taken to realize a symmetrical interconnection array in order not to degree the matching performance. The power domains were separated into three parts: analog, digital and guard ring to avoid the analog section disturbed by the transient current of logic switching. The pins for ground and

output were assigned more than one because of reducing the *IR* drop effect and parasitic inductance. In the current source array, dummy cells were adopted to lower the edge effect and can be treated as decoupling capacitor on the sensitive bias nodes. They are created by dummy transistor with body, source and drain all connected.

The chip will be fabricated with TSMC 0.18 μm mixed signal technology. The final layout was shown in the Fig. 4.11. These numbers in the graph means the pin orientation in the package. The active die size has 1.788 $\mu m^2$ and 1.838 $\mu m^2$.



(a) (b)

Figure.4.11 The final layout

## 4.5 Summary

A 12-bit 250-MSamples/s current–steering CMOS D/A converter with the partial random element matching show that with designed in this chapter. The architecture is shown first. Then, the design consideration and circuit diagram of each sub-block is described in each section. Finally, the layout concern and the switching scheme of current cell matrix have also been discussed. Since the DAC has been designed, the simulation and result of this DAC should also be presented to test the performance. This will be done in the next chapter.

# *Chapter5*

# Simulation Result and Measurement

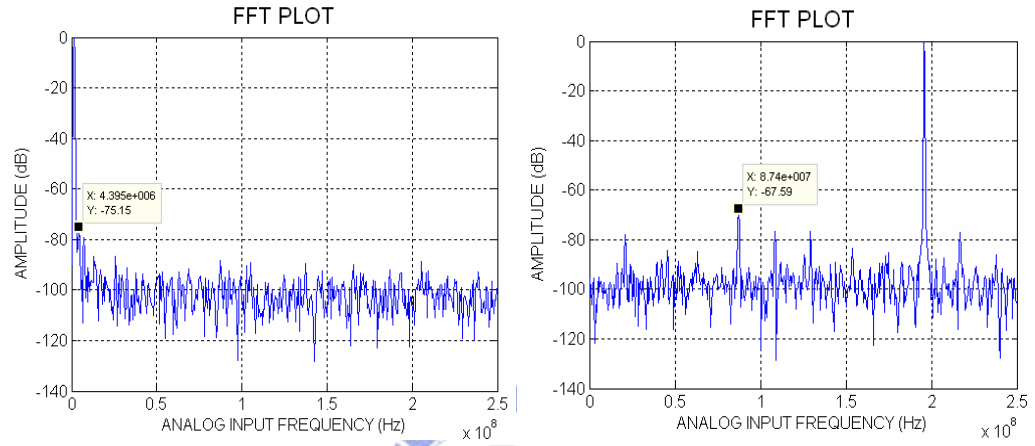
This current DAC has been designed and laid out by using the TSMC 0.18 μm CMOS Mixed-Signal process with one poly and six metals. In this chapter, we present simulation resultant and the testing environment. The measured results are presented in this chapter, too.

## 5.1 Simulation results

First a 12-bit 500-MSample/s D/A converter without partial random element matching, is 67.59 dB for signal frequencies up to 195.8 MHz. The major target specification for SFDR of this paper, a 12-bit 250-MSample/s D/A converter with partial random element matching, is 60 dB for signal frequencies up to 170 MHz. An additional design goal was to derive maximum benefit from this relatively advanced technology.

A simulate sine wave spectrum for (a) $F_s$ = 500 MHz and $F_{sig}$ = 1.46 MHz (b) $F_s$ = 500 MHz and $F_{sig}$ = 195.8 MHz without partial random element matching is shown in Fig. 5.1. Fig. 5.2 shows the SFDR of input frequency between 0.488 MHz and 245.6 MHz without partial random element matching at the sample rate 500 MHz. The differential nonlinearity (DNL) and integral nonlinearity (INL) without partial random element matching are shown in the Fig 5.3. A simulate sine wave spectrum for (a) $F_s$ = 250 MHz and $F_{sig}$ = 0.244 MHz (b) $F_s$ = 250 MHz and $F_{sig}$ = 100.83 MHz with partial random element matching is shown in Fig. 5.4. Fig. 5.5 shows the SFDR

of input frequency between 0.244 MHz and 122.8 MHz at the sample rate 250 MHz MHz. The differential nonlinearity (DNL) and integral nonlinearity (INL) without partial random element matching are shown in the Fig 5.6. The total simulation result of this DAC is summarized in Table 5-1.




**(a)** **(b)**

Figure.5.1 Sine wave spectrum for (a) $F_s$ = 500 MHz and $F_{sig}$ = 1.46 MHz (b) $F_s$ = 500 MHz and $F_{sig}$ = 195.8 MHz without partial random element matching

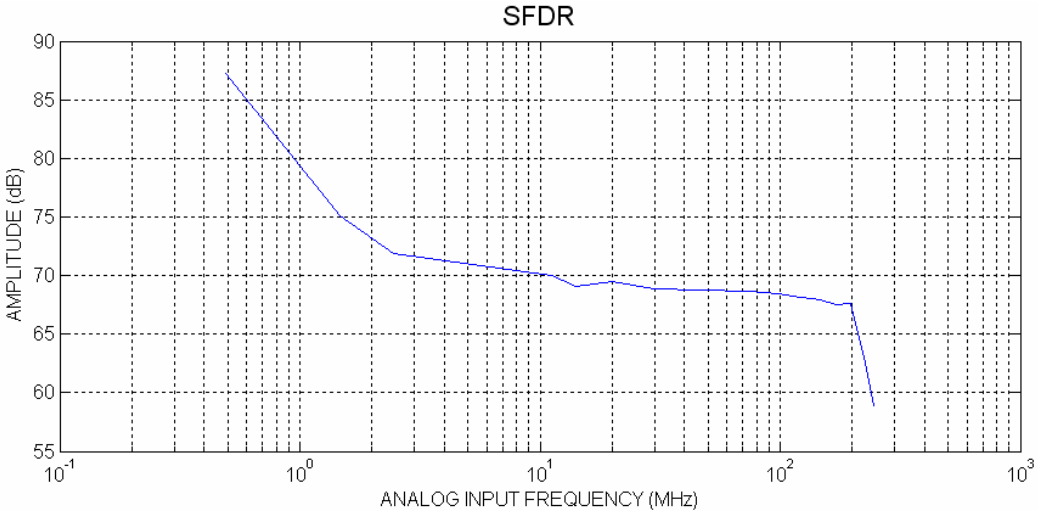



Figure5.2 The SFDR of input frequency between 0.488 MHz and 245.6 MHz at the sample rate 500 MHz without partial random element matching

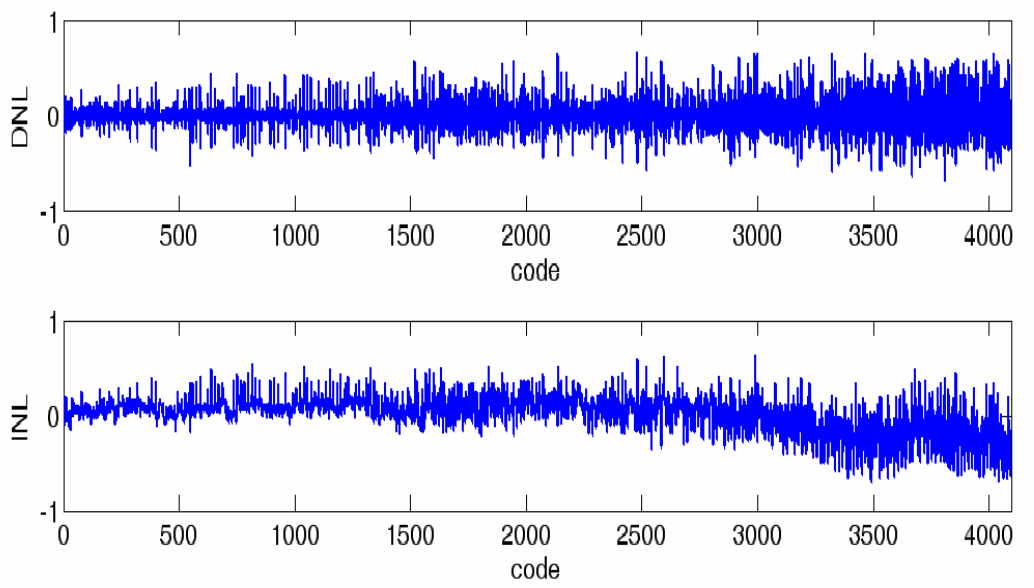



Figure5.3 The differential nonlinearity (DNL) and integral nonlinearity (INL) without partial random element matching

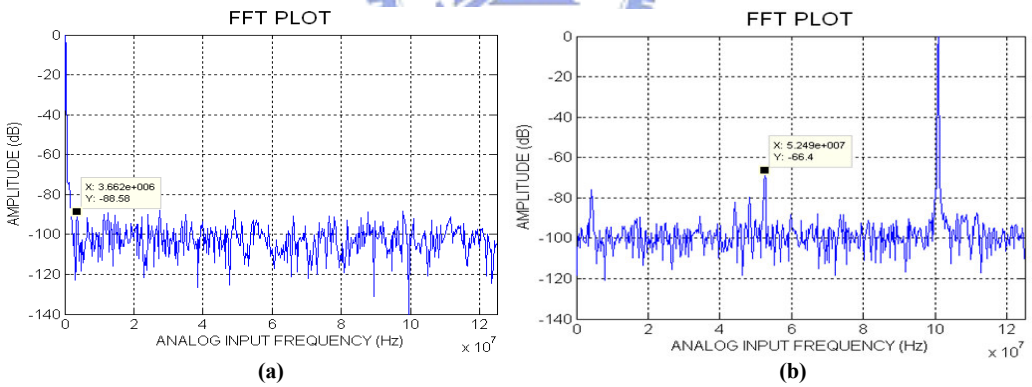



Figure.5.4 Sine wave spectrum for (a) $F_s$ = 250 MHz and $F_{sig}$ = 0.244 MHz

(b) $F_s$ = 250 MHz and $F_{sig}$ = 100.83 MHz with partial random element matching

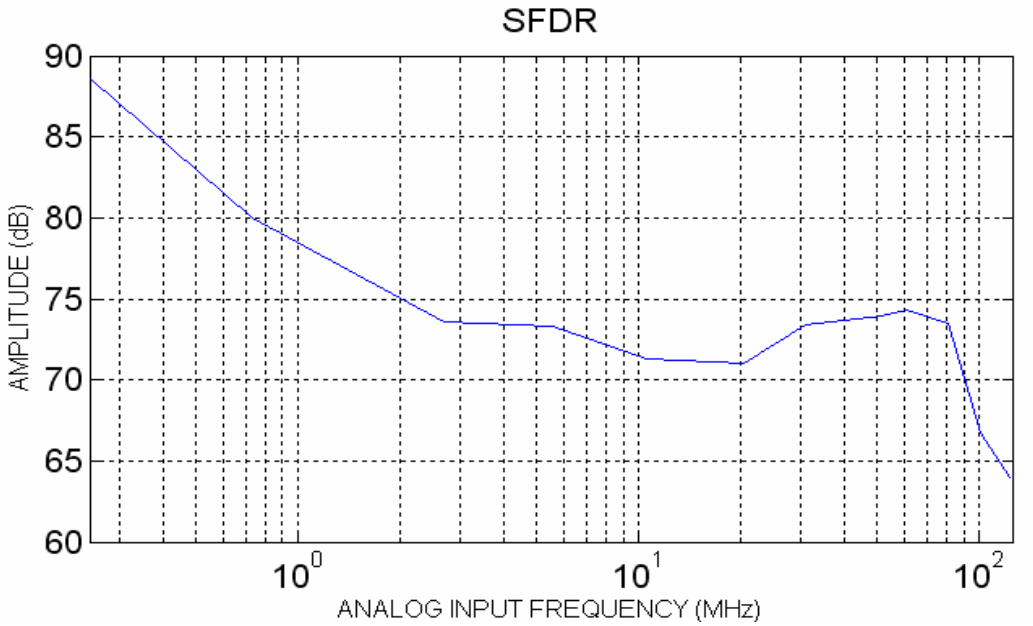



Figure 5.5 The SFDR of input frequency between 0.244 MHz and 122.8 MHz at the sample rate 250 MHz with partial random element matching

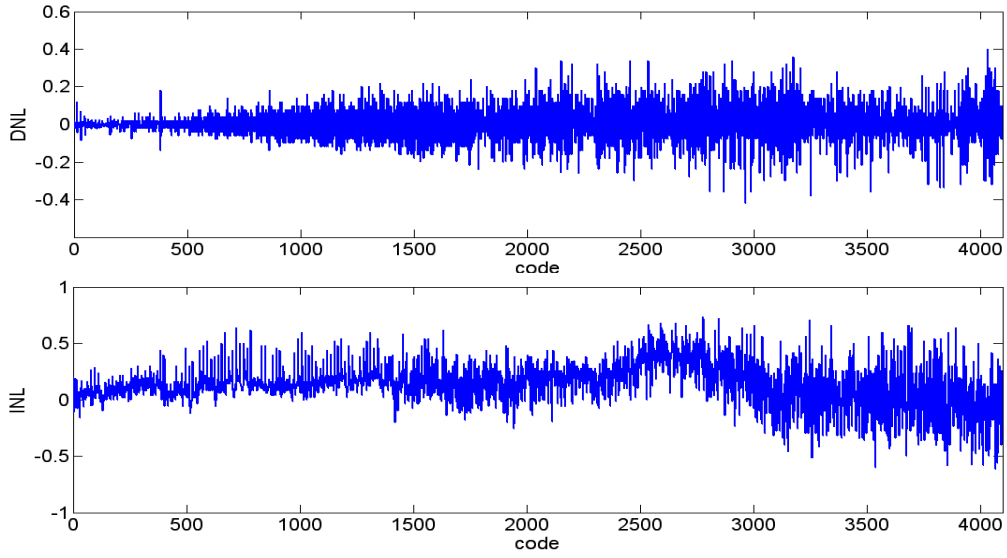



Figure 5.6 The differential nonlinearity (DNL) and integral nonlinearity (INL) with partial random element matching

Table 5-1 The total simulation results of this DAC

| Structure | Without partial random element matching | With partial random element matching |
|---|---|---|
| Process | TSMC 0.18 μm CMOS Mixed-Signal | TSMC 0.18 μm CMOS Mixed-Signal |
| Supply Voltage | Digital supply 1.8 V Analog supply 3.3 V | Digital supply 1.8 V Analog supply 3.3 V |
| Sampling Frequency | 500 MHz | 250 MHz |
| DNL | < 0.8 LSB | < 0.5 LSB |
| INL | < 0.8 LSB | < 0.7 LSB |
| SFDR (Fin = 100 MHz) | 68.5 dB @ CLK = 500 MHz | 66.4 dB @ CLK = 250 MHz |
| Power Dissipation | 73 mW | 75 mW |
| Active Area | 1.788 $mm^2$ | 1.838 $mm^2$ |

## 5.2 Test Circuits

Fig. 5.7 shows the measurement setup of the overall DAC testing. In the setup, the input digital code is generated by Agilent 16902B Logic analysis System. The differential output of the DAC is converted to a signal-ended output by using an active probe to provide rejection of common mode noise and even order distortion. This signal-ended output is measured by Agilent E4440A 3 Hz-26 GHz PSA Series Spectrum Analyzer to get spectrum performance. The Voltage transient output signals

are measured by Agilent 34401 Digital Multi-meter. Two precise power supplies are used to generate both analog and digital supply.

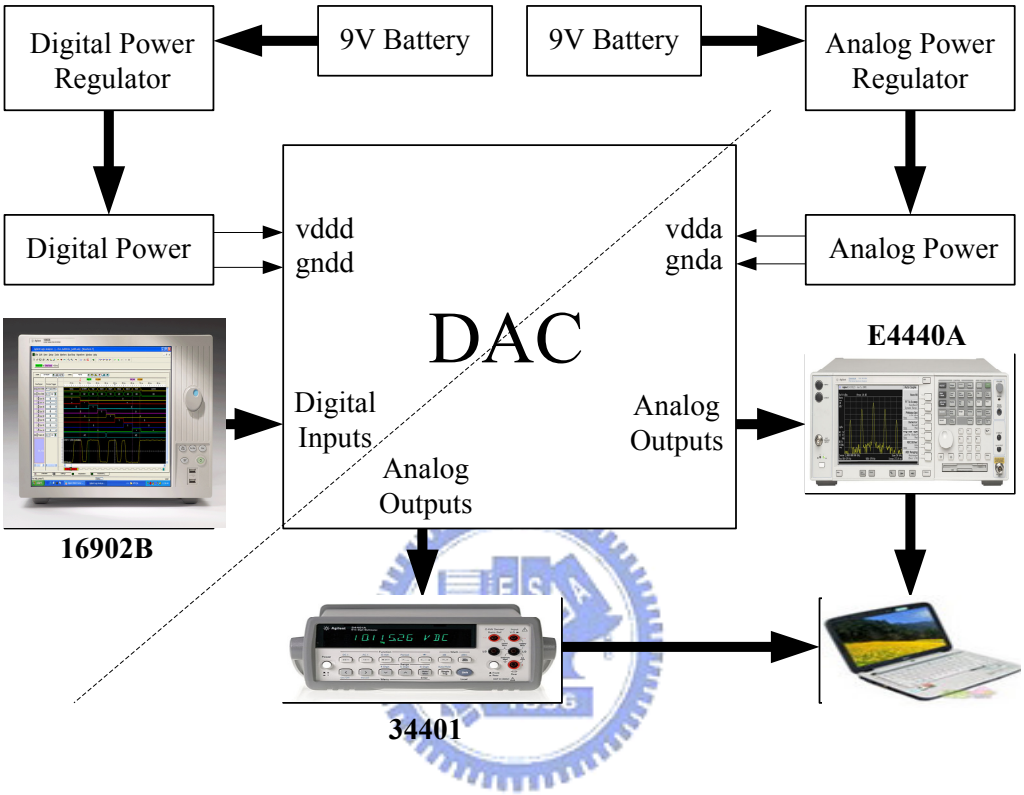



Fig. 5.7 Testing setup

The analog and digital power supplies are generated by the application of the LM317 adjustable regulators shown in Fig. 5.8. The capacitor C1 is used to improve the ripple rejection and capacitor C2 is the input bypass capacitor. The resistor R1 is the fixed resistor and resistor R2 is the precise variable resistor. The inductance L1 and the capacitor C3, C4, C5 and C6 is a low-pass filter. The output voltage of the Fig. 5.8 can be expressed as

$$V_{out} = 1.25V \cdot (1 + \frac{R_2}{R_1}) \cdot I_{ADJ} \cdot R_2 \qquad (5.1)$$

Where $I_{ADJ}$ is the DC current that flows out of the adjustment terminal ADJ of the regulator. By the way, the resistor R1 can use the low temperature coefficient of the metal film resistor to get the stable output voltage.

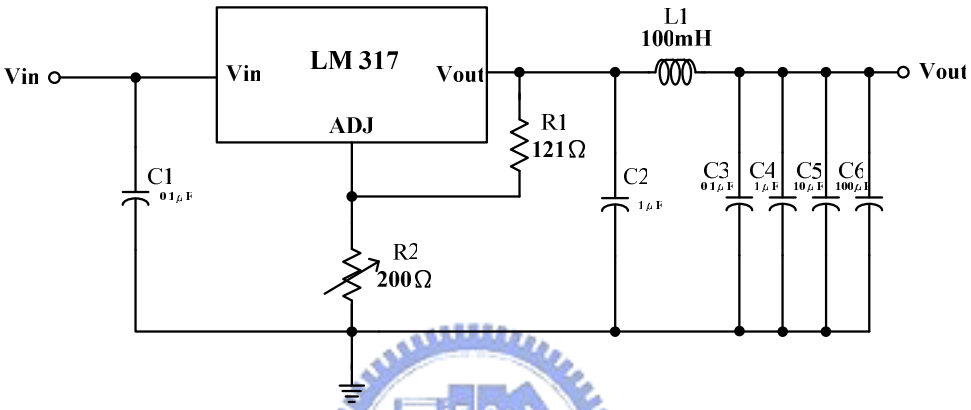



Fig. 5.8 Power supply regulator

## 5.3 Measurement Results

The sample rate is set to 100 MHz at input frequency 2 MHz, 5.17 MHz, 12.83 MHz, 20.67 MHz and 29.15 MHz, respectively. A measured sine wave spectrum for $F_s$ = 20 MHz and $F_{sig}$ = 1 MHz is shown in Fig. 5.9. A measured sine wave spectrum for $F_s$ = 100 MHz and $F_{sig}$ = 2 MHz and 9.8758 MHz is shown in Fig. 5.10 and Fig. 5.11. A measured sine wave spectrum for $F_s$ = 200 MHz and $F_{sig}$ = 19.81 MHz is shown in Fig. 5.12. Fig. 5.13 shows the SFDR of input frequency between 2 MHz and 29.15 MHz at the sample rate 100 MHz. The differential nonlinearity (DNL) and integral nonlinearity (INL) are shown in the Fig 5.13. The total measured result of this DAC is summarized in Table 5-2 and the die microphotograph is shown in Fig. 5.14.

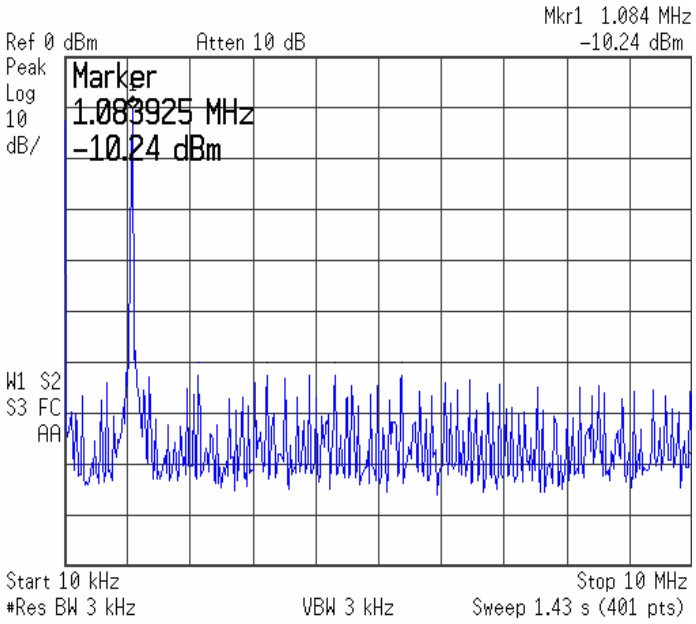



Figure.5.9 Sine wave spectrum for $F_s$ = 20 MHz and $F_{sig}$ = 1 MHz

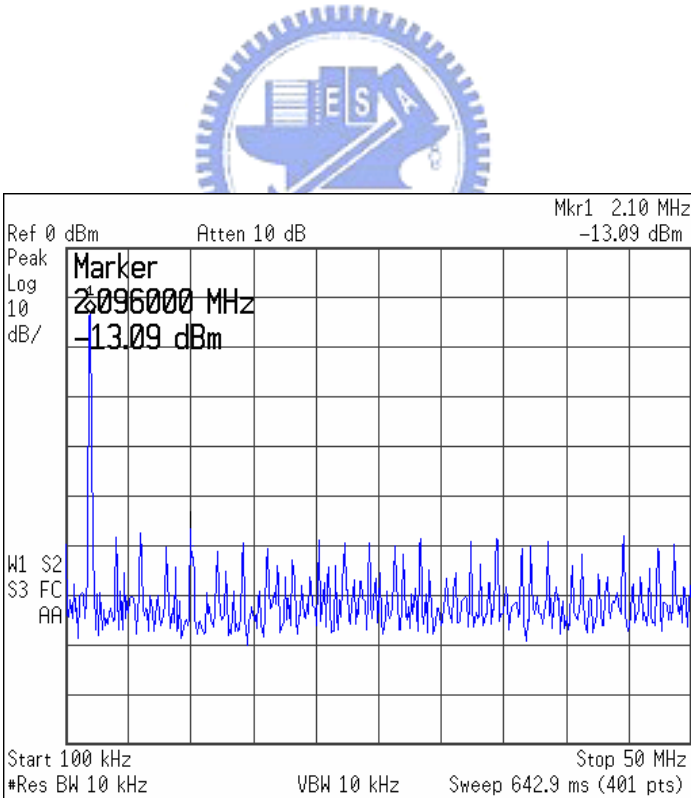



Figure.5.10 Sine wave spectrum for $F_s$ = 100 MHz and $F_{sig}$ = 2 MHz

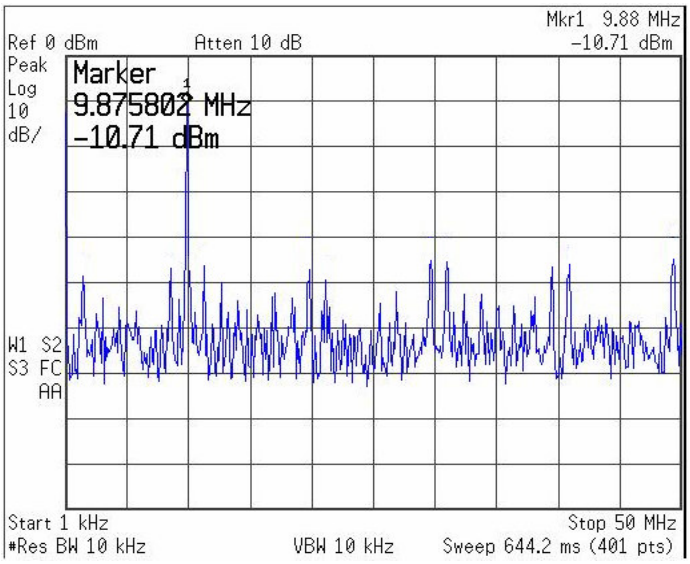



Figure.5.11 Sine wave spectrum for $F_s$ = 100 MHz and $F_{sig}$ = 9.8758 MHz

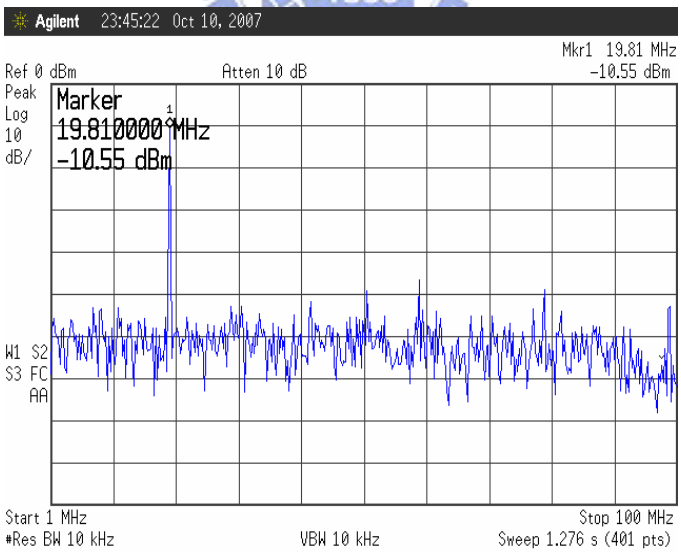



Figure.5.12 Sine wave spectrum for $F_s$ = 200 MHz and $F_{sig}$ = 19.81 MHz

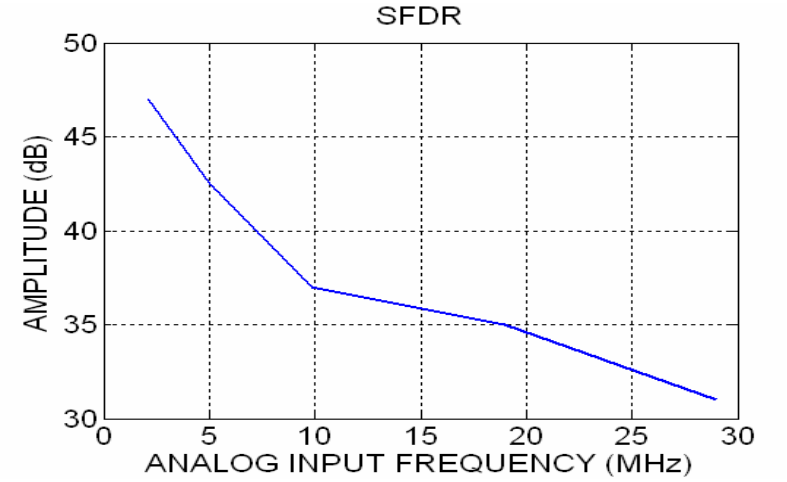



Figure 5.13 The SFDR of input frequency between 3 MHz and 34.33 MHz at the sample rate100 MHz

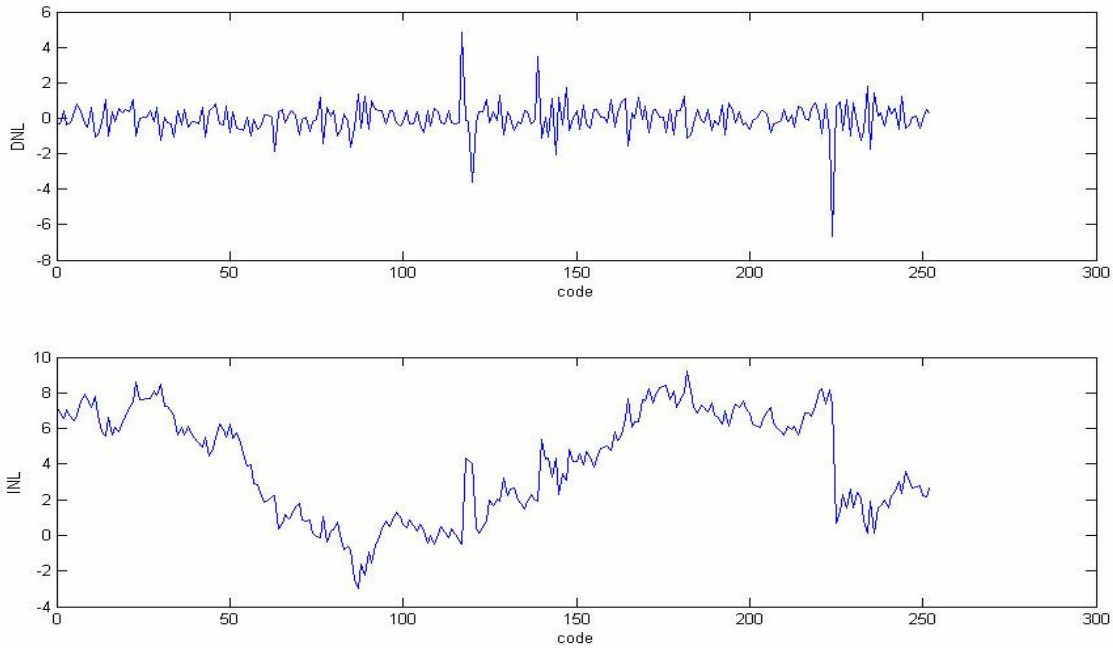



Figure 5.14 The differential nonlinearity (DNL) and integral nonlinearity (INL)

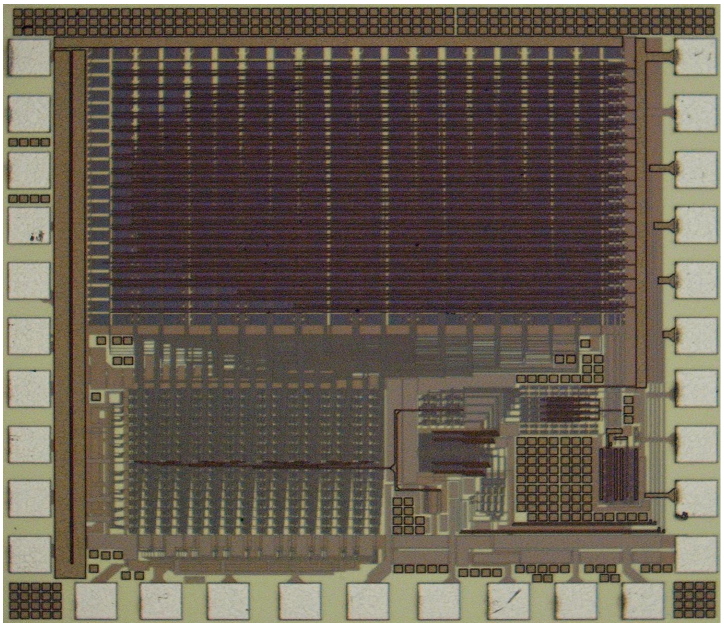


Figure 5.15 The die microphotograph

Table 5-2 The total measurement results of this DAC

| | |
|---|---|
| Process | TSMC 0.18 μm CMOS<br>Mixed-Signal |
| Supply Voltage | Digital supply 1.8V<br>Analog supply 3.3V |
| Sampling Frequency | 100 MHz |
| DNL | < 5 LSB |
| INL | < 9 LSB |
| SFDR(Fin = 2 MHz) | 46 dB @ CLK = 100 MHz |
| Power Dissipation | 125 mW |
| Active Area | 1.778 $mm^2$ |

# *Chapter6*

# Conclusions and Future Work

In this thesis, the 12-bit 250-MHz DAC is implementation. We propose a new simple random structure and special layout to improve the static and dynamic linearity. The current source is properly designed to reduce the nonlinearity caused by finite output impedance of current source. To overcome the random error and systematic error, the proper area of current source is selected and special layout technique is used. A high speed, low crossing point latch is implemented to compensate the error at the DAC output due to switching in the current cells. The DAC is fabricated by 0.18μm 1P6M CMOS Mixed-Signal. Besides, the power dissipation is 125mW. The measure resultant of a 12-bit current-steering D/A converter without the partial random element matching shows that the signal frequency of 9.87 MHz at the update rate of 100 MHz, the SFDR is 37 dB. The differential nonlinearity and integral nonlinearity are below 5 and 9 least significant bits (LSB's).

The DAC can be improved from several points of view in the future. First, due to lack of considering the parasitic loading effect caused by the layout, the post-layout dynamic performance simulation results will be degraded than the pre-layout simulation at high input frequency. Therefore, the DAC should be designed to keep enough margins to endure the loading effect and the floor plan should be modified to decrease the parasitic loading. Second, after passing through multi-bit registers to sample the input digital data, the MSBs and LSBs are binary-weighted. Third, the clock should be designed carefully because the current DAC operated at high speed.

And pay more attention to routing between circuit block. Finally, we can propose a calibration structure to improve the matching accuracy of the current sources is applied for high-resolution DACs. Because of the lower matching requirement of the current sources, the chip area is smaller and the cost is lower, too.

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