國 立 交 通 大 學

電機學院 IC 設計產業研發碩士班

碩 士 論 文

應用於數位電視和 WIMAX
之低相位雜訊三角積分調變頻率合成器

Low-Noise Delta-Sigma Frequency Synthesizers for
DTV and WIMAX Applications

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摘　　要

本論文提出低相位雜訊三角積分之分數型頻率合成器，兩種不同架構的分數型頻率合成器被實現,這些電路皆應用於數位電視以及 WIMAX 行動通訊上。

在射頻系統上，頻率合成器的設計仍然是最具有挑戰性議題之一。因為它必須要達到非常嚴格要求，例如:穩定時間(setting time)、相位雜訊、參考愧入(reference feedthrough)，又被稱作參考邊頻 (reference spur) ，・・等。在設計頻率合成器中，有幾個取捨(trade-off)會出現。首先，穩定時間長短主要取決於迴路頻寬 (loop bandwidth) 大小。同時因為考量迴路的穩定性，迴路頻寬會被限制在大約 1/10 的參考頻率。接著，壓控振盪器的相位雜訊只有在小於迴路頻寬時才會被回授的迴路所降低。最後，我們需要縮小迴路頻寬來降低參考邊頻。為了解決這些取捨，我們設計出幾種新的架構採取電流匹配以及動態式電容取樣，隨機充電等概念來降低參考邊頻的鎖相迴路。

量測結果:再 DTV 系統下可調整輸出頻寬為 2110~870 兆赫茲，相位雜訊為 -81.62 分貝/赫茲 @1 赫茲，再 WIMAX 系統下可調整輸出頻寬為 2890~2100 兆赫茲，相位雜訊為-81.67 分貝/赫茲 @2.5 赫茲，寄生雜頻較主頻低 69.78 分貝，49.49 分貝。

Low-Noise Delta-Sigma Frequency Synthesizers for DTV and WIMAX RF Applications

Student：De-Wen Liao Advisors：Dr. Chung-Chih Hung

Industrial Technology R&D Master Program of
Electrical and Computer Engineering College
National Chiao Tung University

ABSTRACT

This thesis focuses on low-noise sigma-delta fractional-N synthesizers. Two fractional-N synthesizers are presented. These circuits are targeted for DTV and WIMAX applications.

Synthesizer design still remains one of the most challenge issues in RF system because it must meet very stringent requirements such as: setting time phase noise, reference feedthrough, etc. Several trade-offs exist in the synthesizer design. First, the settling time is largely determined by the loop bandwidth which is limited to approximately 1/10 of the reference frequency for the loop stability consideration. Second, the phase noise of the oscillator is reduced by the feedback loop only within the loop bandwidth. Finally, in order to suppress the reference spur, a small loop bandwidth is required. To solve all these trade-offs, we have proposed several new architectures adopting consists of current match, dynamically switched capacitors, and random charge to achieve low reference spur PLL.

The measurement results show that: the synthesizer output frequency for DTV system is tunable between 2110~870MHz, and phase noise is -81.62dBc/Hz @1-MHz offset. The output frequency for WIMAX system is tunable between 2890~2100MHz, and phase noise is -81.67dBc/Hz@2.5-MHz offset with spurious tones -69.78dBc, and -43.49dBc.

誌　　謝

隨著這份碩士論文的完成，兩年來在交大的求學生活也即將告一個段落，往後迎接著我的，又是另一段嶄新的人生旅程。本論文得以順利完成，首先，要感謝我的指導教授洪崇智老師在我兩年的研究生活中，對我的指導與照顧，並且在研究主題上給予我寬廣的發展空間。而類比積體電路實驗室所提供完備的軟硬體資源，讓我在短短兩年碩士班研究中，學習到如何開始設計類比積體電路，乃至於量測電路，甚至單獨面對及思考問題的所在。此外要感謝李育民教授、黃淑娟教授、溫宏斌教授撥冗擔任我的口試委員並提供寶貴意見，使得本論文更為完整。也感謝國家晶片系統設計中心提供先進的半導體製程，讓我有機會將所設計的電路加以實現並完成驗證。

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最後，所有關心我、愛護我和曾經幫助過我的人，願我在未來的人生能有一絲的榮耀歸予你們，謝謝你們。

廖德文 于 交通大學電資大樓 710 實驗室
2007.12.25

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Chapter 1

Introduction

1.1 Motivation

The system for fixed and portable reception of digital terrestrial television, known as digital television video (DTV), has been available for several years. Many countries such as America, Europe, Japan, have already advertised relative transmission standard and rules of application [1]-[4]. At the same time, Taiwan has also started the transition from analog to digital television.

By the rapid development and large demand of wireless communication, fully integrated monolithic radio transceivers are the most significant considerations for communication applications. The recent rapid growth of the wireless communication market inspires many people to research the concerned region with strong passion. Of such a many developments, enhanced operating frequency of CMOS technology encourages the designer to implement single-chip RF-to-baseband systems. One of the important design goals of portable wireless system is low power consumption for long battery life. CMOS technology satisfies the requirements of low power consumption, low cost, reduced size, and also a few GHz operating frequency in wireless systems.

Frequency synthesizer is an important topic of the RF front-end. As an example, for a direct-conversion receives to demodulate RF signal received from antenna, the

RF front-end amplified the signal by a low noise amplifier (LNA) first. And then the entire spectrum, both the wanted and unwanted signals, is translated to baseband by a mixer. In this step, a local oscillator (LO) is needed to down convert the RF signal. The oscillators used in RF transceivers are usually embedded in a synthesizer to achieve a precise definition of output phase and frequency. Synthesizer design still remains one of the most challenge issues in RF system because it must meet very stringent requirements such as: setting time phase noise, reference feedthrough (also called reference spur), etc. Several trade-offs exist in the design synthesizer. First, the settling time is largely determined by the loop bandwidth which is limited to approximately 1/10 of the reference frequency for the loop stability considerations. Second, the phase noise of the oscillator is reduced by the feedback loop only within the loop bandwidth. Finally, in order to suppress the reference spur, a small loop bandwidth is required. To solve all these trade-offs, we have proposed several new architectures adopting the current match 、dynamic switch cap and random charge concept to achieve low reference spur PLL which their characteristics are introduced in chapter3 and 4.

1.2 RF front-end overview

In typical RF front-end circuits, frequency synthesizer actions as a local oscillator (LO) for up/down conversion in communication transceivers. Fig. 1-1 shows a general block diagram of a transceiver. It contains a low-noise amplifier (LNA), a power amplifier (PA), mixers, and band-pass filters. In order not to distort the received signals, the excellent noise performance of frequency synthesizer is required. Besides, the switch time of circuit is also significant. The design of phase-locked loops (PLLs) must generally deal with a tight trade-off between the

setting time and the amplitude of the ripple on the oscillator control line. In conclusion, we can judge a synthesizer by following three parameters: phase noise, sideband interface (spurious tones), and locking time. Based on the above reason, we realize two sigma-delta fractional-N type synthesizers.

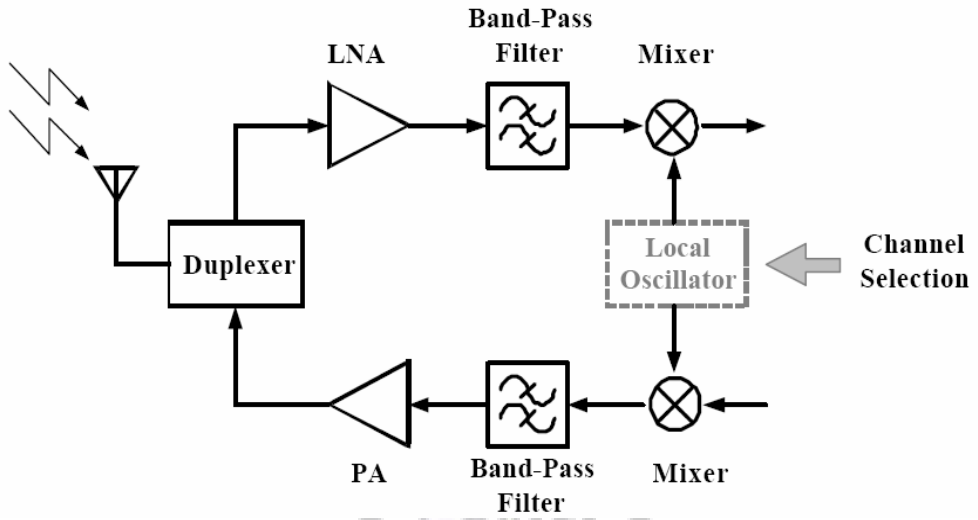


Fig. 1.1 Block diagram of a general transceiver front-end

For the sake of reducing the demand for tracking filter, more and more tuners are designed by Double Conversion structure, composed of frequency synthesizers, mixers, and low noise amplifiers, as shown in Fig. 1.2. The first local oscillator (LO) is synthesized by a PLL and controlled by a microprocessor. The second LO is a fixed reference oscillator. This type of tuner converts the entire input band of 50-860MHz up to a fixed first intermediate frequency (IF), that is above the highest input frequency of interest, and selects the desired channel by the RF saw filter. This process rejects the image of the downconversion. Then, the selected channel is down converted to the second intermediate center at 43.75MHz and passes through the second IF saw filter. Finally, the output signal feeds the next stage to demodulate DTV (WIMAX) signal. The detailed spectrum is shown in Fig. 1.3.

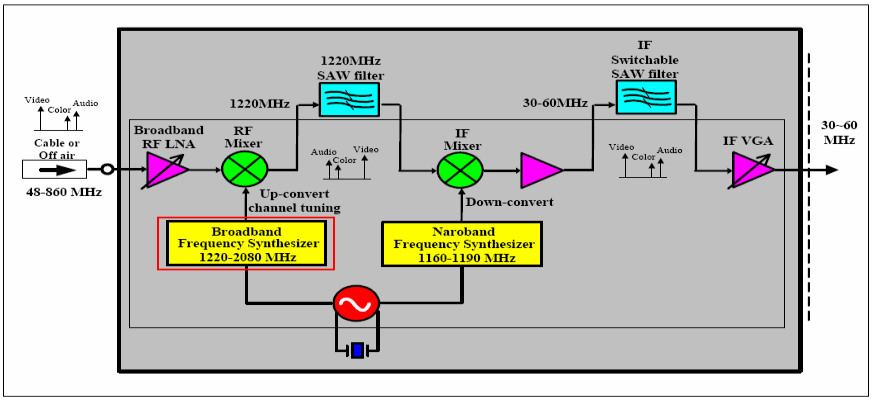


Fig. 1.2 Double-Conversion tuners

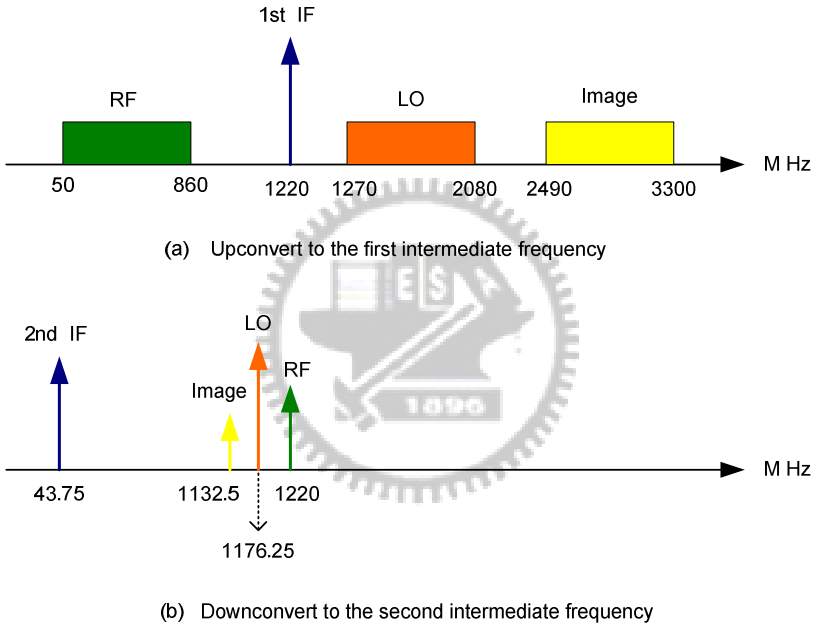


Fig. 1.3 Double-Conversion system spectrums

1.3 Thesis Overview

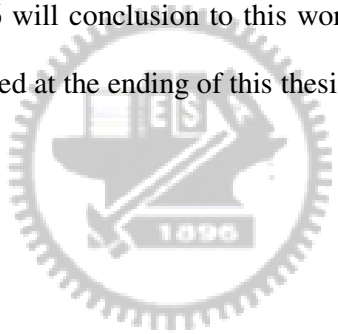
Chapter 2 will give basic ideas of phase-locked loops (PLLs) as well as some important characteristics in a frequency synthesizer. A design flow is described along with detailed parameter setting and architecture together with some examples is demonstrated.

Chapter 3 will present frequency synthesizer which is Fractional N synthesizer. At first we will discuss the motivation including several design issues, such as: jitter and Phase noise in Ring VCO Then, analysis and implementation of circuit are introduced in detail.

In chapter 4, A spur-reduction architecture will be proposed to further improve the spur reduction function. At first we will discuss the motivation including several design issues and several building block, such as: phase noise, reference spur …..Then, analysis and implementation of our circuit are introduced in detail.

In chapter 5 also; the experimental results will be presented in the end of this chapter.

Finally, chapter 6 will conclusion to this work is given. Suggestions for future works are recommended at the ending of this thesis.



Chapter 2

Fundamental of frequency synthesizers

2.1 Introduction to PLL

In general, the charge pump PLL contains five major building blocks which are phase/frequency detector charge pump, loop filter, voltage-controlled oscillator, and divide. By varying the dividing ratio of the divider, the PLL can synthesizer an output frequency which is a multiple of the input clock. Since the loop characteristics would be influenced by the dividing ratio, we need consider the loop stability carefully when we design the loop parameters. Fig 2.1 shows the topology of a typical frequency synthesizer. The oscillator generates a waveform whose fundamental oscillation frequency is controlled by the input voltage. When a divider is used, this oscillation frequency is divided by an integer number N. THE Phase of the resulting waveform is compared with a reference clock in a phase/frequency divider. Both up and down signals are generated to indicated which direction should the oscillation frequency be corrected. The error signal is low-passed filtered and finally fed a control voltage to the oscillator. The frequency division ratio N adjustable, several oscillation frequencies can be synthesized. Under condition of lock, two inputs of the phase detector have a constant phase relationship and thus equal frequency.

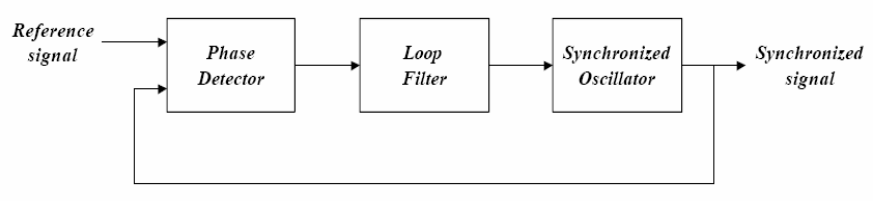


Fig. 2.1 Typical frequency synthesizer architecture

The main applications of PLL are as follows:

1. Clock recovery: Some data streams, especially high-speed serial data streams, (such as the raw stream of data from the magnetic head of a disk drive) are sent without an accompanying clock. The receiver generates a clock from an approximate frequency reference, and then phase-aligns to the transitions in the data stream with a PLL. In order for this scheme to work, the data stream must have a transition frequently enough to correct any drift in the PLL's oscillator. Typically, some sort of redundant encoding is used; 8B10B is very common.

2. Deskewing: If a clock is sent in parallel with data, that clock can be used to sample the data. Because the clock must be received and amplified before it can drive the flip-flops which sample the data, there will be a finite, and process-, temperature-, and voltage-dependent delay between the detected clock edge and the received data window. This delay limits the frequency at which data can be sent. One way of eliminating this delay is to include a de-skew PLL on the receive side, so that the clock at each data flip-flop is phase-matched to the received clock.

3. Clock generation: Most electronic systems include processors of various sorts that operate at hundreds of megahertz. Typically, the clocks supplied to these processors come from clock generator PLLs, which multiply a lower-frequency reference clock (usually 50 or 100 MHz) up to the operating frequency of the processor. The multiplication factor can be quite large in cases where the operating frequency is multiple gigahertzes and the reference crystal is just tens or hundreds of

megahertz.

4. Spread spectrum: All electronic systems emit some unwanted radio frequency energy. Various regulatory agencies (such as the FCC in the United States) put limits on this emitted energy and any interference caused by it. The emitted noise generally appears at sharp spectral peaks (usually at the operating frequency of the device, and a few harmonics). A system designer can use a spread-spectrum PLL to reduce interference with high-Q receivers by spreading the energy over a larger portion of the spectrum. For example, by changing the operating frequency up and down by a small amount (about 1%), a device running at hundreds of megahertz can spread its interference evenly over a few megahertz of spectrum, which drastically reduces the amount of noise seen by FM receivers which have a bandwidth of tens of kilohertz.

2.2 General Consideration

In additional to frequency accuracy and channel selection, two other aspects also influence the performance of a transceiver front-end: phase noise, and spurs.

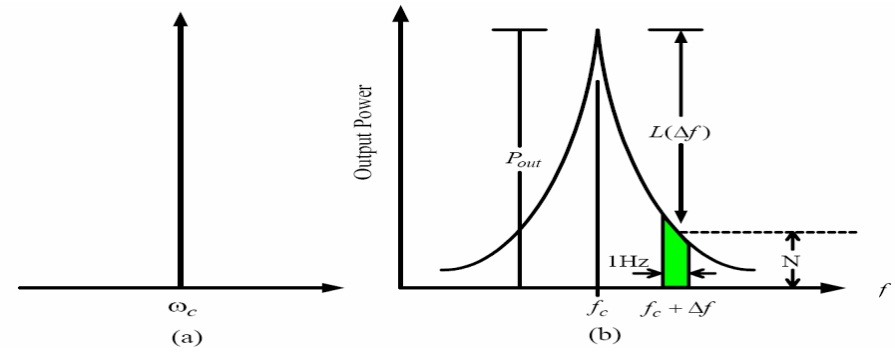


Fig. 2.2 (a) Ideal; (b) Practical power spectrum of an oscillator

2.2.1 Phase Noise

Ideally, the output of the frequency synthesizer should be pure tones as shown in Fig. 2.2(a). However, due to the thermal noise of the resistors and transistors in

the oscillator or some noise at the frequency tuning input of the oscillator, the phase of the oscillation will fluctuate. In frequency domain, the phase fluctuation forms a skirt of noise power around the carrier impulse as shown in Fig. 2.2(b). In order to quantify the phase noise, the noise power per unit bandwidth at an offset frequency ($\triangle$w) with respect to the carrier frequency (w_c) is compared with the carrier power, and this quantity is expressed in the unit of dBc/Hz. If the noise source is white, the phase noise in the frequency domain is proportional to $1/\triangle f^2$.

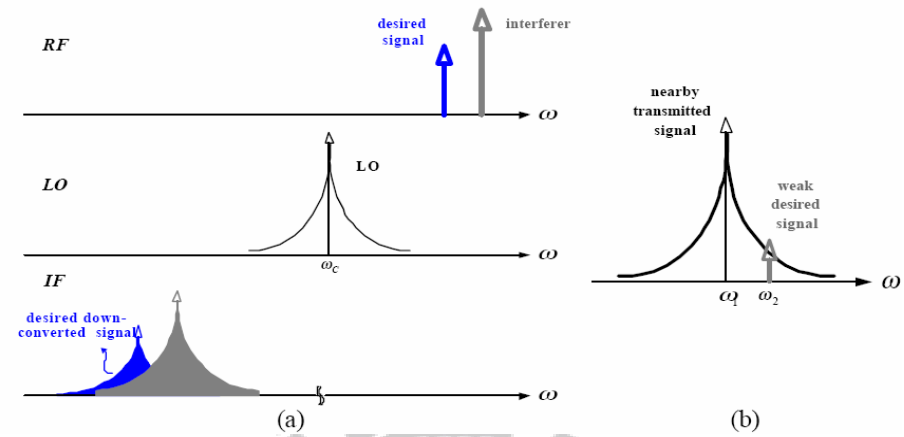


Fig. 2.3 (a) Receiver and (b) Transmitter

The effects of the phase noise in both the receiver and transmitter are shown in Fig. 2.3, which shows the receiver path. If there is a large interference signal near the small desired signal, both the desired signal and interference will be mixed down to the IF. In the mixing both signals will also have the same noise skirt as that of the impure LO signal because the down-conversions is actually a convolution in the frequency domain. Since the power of the interfering signal is generally large, the noise down-converted to the frequency of the desired signal can significantly degrade the signal-to-noise ratio (SNR) of the desired signals. The effect is called "reciprocal mixing." However, the effect in the transmit path is shown in Fig.2.3(b), where larger-power transmitted signals with substantial phase noise can corrupt weak nearby signals. Therefore, the output spectrum of the LO must be

extremely sharp, and set of stringent phase-noise requirements must be satisfied in the wireless communication system.

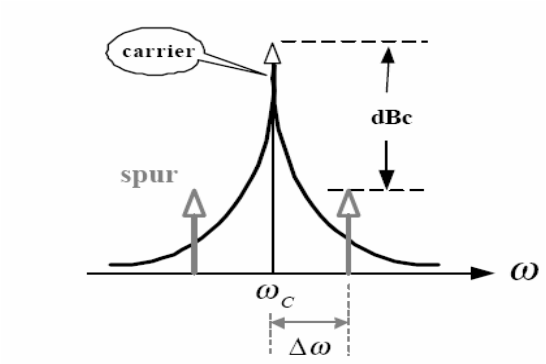


Fig. 2.4 Frequency domain representation of spur

2.2.2 Spurs

Other than the phase noise due to the internal thermal noise and external noise, the oscillator can also be modulated by some noise of fixed frequency due to the switching of other circuits in the synthesizer. One of the main noise sources is the switching noise of the charge pump at the reference frequency. The input noise modulate the control voltage and hence the output frequency of the VCO. Two to will appear at the upper and lower sideband of the carrier as shown in Fig.2.4. The tones are called reference spurs and measured by the difference between the power the carrier and the spurs at some frequency offset (△w) in the units of dBc.

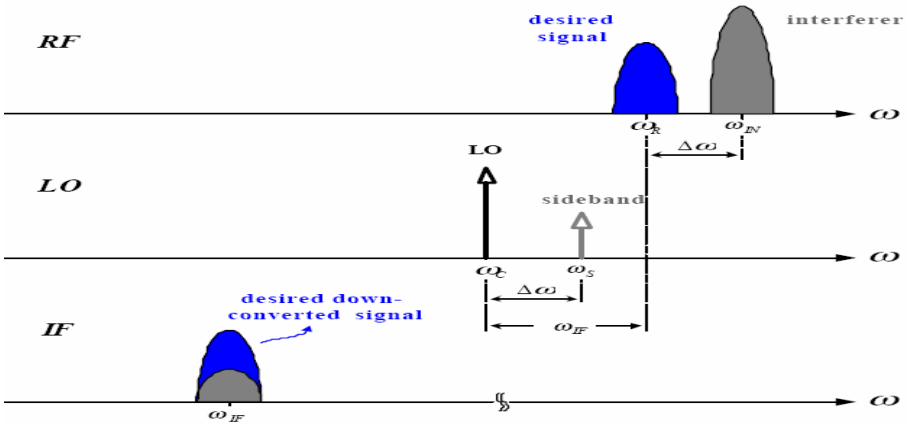


Fig. 2.5 Effect of sideband in a receiver

Similar to the case of phase noise, as shown in Fig. 2.5, if there is a interference signal appearing at the frequency which reference spur also exist the desired signal and the interference will be mixed down to the IF, as degrade SNR of the desired one. In a zero-IF system, the down-converted interferer generation the dc offset and thus still affects the system SNR.

2.3 Phase-Locked Loop (PLL) Fundamentals

When designing a PLL-based frequency synthesizer, it is very important to understand the behaviors of each functional block as well as the overall closed-loop behavior. The following discussion focuses on charge-pump PLLs, which is the most popular type of PLLs nowadays and is adopted in our work.

2.3.1 Phase Frequency Detector (PFD)

Phase frequency can detector both phase and frequency difference between the reference signal and the output signal of the frequency divider. As shown in Fig. 2-6, if the frequency of A is greater than the frequency of B, then Q_A is high, but Q_B is still low. If the frequency of A and B are equal, then the circuit will check the phase difference between the two inputs, and generates a pulse equal to the phase difference at Q_A or Q_B (depends on which input has phase leading).

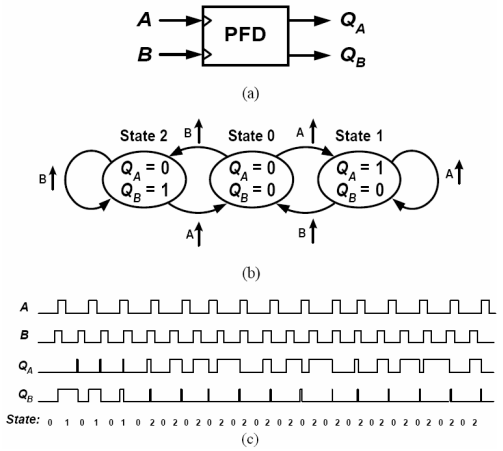


Fig. 2.6 (a) PFD block diagram (b) PFD state diagram (c) PFD timing diagram

Fig. 2-7(a), it shows a possible implementation of the above PFD. This circuit contains two reset table D-flip flops and a NAND gate. The input signals of A and B are as clock input and the input of two D-flip flops is always high. And we set the initial condition is Q_A=Q_B=0. If A is from 0 to 1, until B is from 0 to 1 and QB becomes high to make the two D-flip flops reset. And Fig. 2-7(b), shows the input-output characteristic of the PFD.

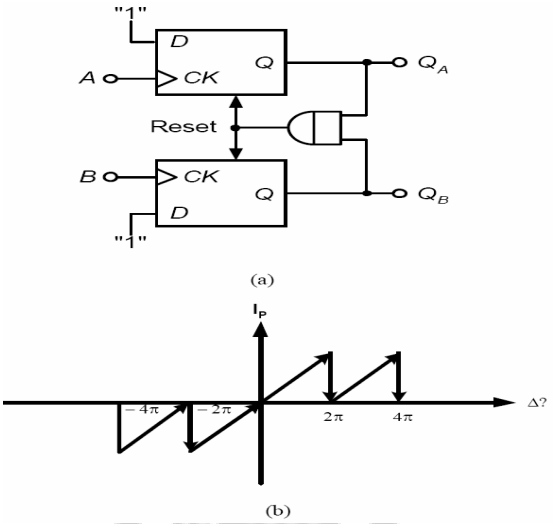


Fig. 2.7 (a) PFD implementation (b) PFD characteristic

Fig. 2-8(a) shows the PFD circuit. It is negative-trigger and has the same function as we discuss above. But it still has a drawback. When this type of PFD incorporated with charge pump circuit, it has a drawback that a dead zone exist, as shown in Fig. 2-8(b). If the reset signal is not delayed sufficiently, the output of charge pump will not change for small phase error, thus the dead zone translates to jitter in PLL and must be voided. In Fig. 2-8(a), the delay chain to increase delay of reset signal for eliminating dead zone.

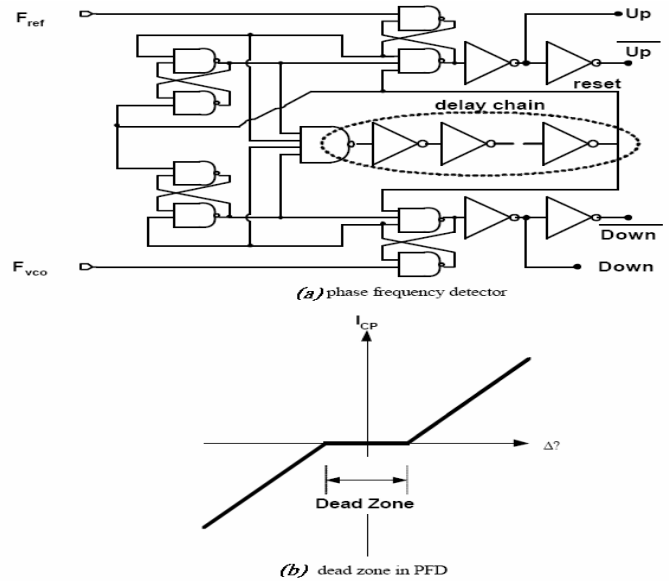


Fig. 2.8 (a) Phase frequency detector (b) Dead zone in PFD

2.3.2 Charge pump

A PFD could not alone provide the exact voltage (or current) signal proportional to the phase difference at its inputs. A charge pump serves to convert the two digital output signals Q_A and Q_B of the PFD into charge flows whose quantity is proportional to the phase error. A passive filter then shape the output current signal of the charge pumps to suppress the useless messages buried in that signal.

A PFD together with a charge pump and a single capacitor C_1 as the loop filter are shown in Figure 2.9, with the corresponding time-domain response shown as well. As a higher frequency than B or has the same frequency as B but with a leading phase, the charge pump sources a constant-valued current I_1 through switch S_1 into the capacitor, and the output voltage increases steadily. Similarly, if the frequency of input A is lower or the phase is lagging, the output waveform will be a steadily downward one. What happens if the inputs are exactly the same? Careful examination shows that Q_A and Q_B will have pulses of short duration. In this case, if the currents of the two current sources are the same in quantity, as indicated in

Figure 2.10, at the time that both S_1 and S_2 are on, the current sourced by I_1 is exactly sunk by I_2. Thus no net current will flow through C_1 and V_{out} remains unchanged as in the case when both S_1 and S_2 are off.

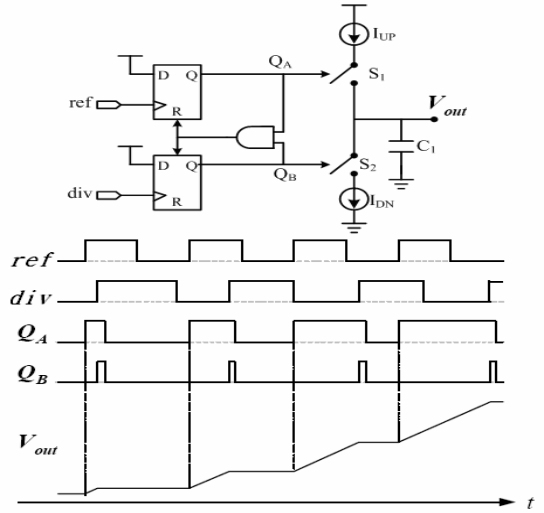


Fig. 2.9 PFD with charge pump and the timing diagram

The phase frequency detector and the charge pump can be together characterized as:

$$I_{pump} = I \frac{\phi_e}{2\pi} \tag{2.1}$$

Where I_{PUMP} is the output current of the charge pump, $\phi_e = \phi_A - \phi_B$ represents the phase error between the two PFD inputs and I=I1-I2 is the current value of the two current sources in the charge pump. This representation, however, is an approximate one. One should note that the charge pump is a discrete-time system, and it provides good approximation only when the loop bandwidth is much less than the input reference frequency.

The single-capacitor loop filter nevertheless has an infinite dc gain, which might unstablilize the close loop. To avoid instability, a resistor R_P in series with CP is added, which in effect adds a LHP (left-half-plane) zero to the overall open-loop transfer function. The transfer function of the resolution loop filter is:

$$F(s) = R_P + \frac{1}{sC_P} \tag{2.2}$$

Note that this representation indicates a conversion from an input current a output voltage, and thus is directly applicable in conjunction with Equation. (2.1).

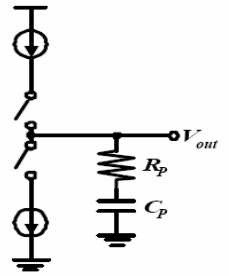


Fig. 2.10 Addition of a zero to a charge pump

2.3.3 Voltage-Controlled Oscillator

Many applications need that the oscillators be "tunable". The most popular circuit is the voltage-controlled oscillator, whose frequency is a linear function of its input control voltage. The transfer function is as follows:

$$\omega_{out} = \omega_0 + K_{VCO} V_{cont} \tag{2.3}$$

Here ω_0 is the free running frequency, K_{VCO} is gain or sensitivity of the VCO, (usually in rad/s/V). Next, we want to derive the phase transfer function:

$$\int \omega_{out} = \omega_0 t + K_{VCO} \int V_{cont} dt \tag{2.4}$$

Only the second term of the total phase is of interest. We call $K_{VCO}\int_0^t V_{cont} dt$ as the "excess phase", denoted by ϕ_{ex}. In fact, in the analysis of PLLs, we respect the VCO as a system whose input as the control voltage and output as the excess phase. If the system is LTI, then we get:

$$\phi_{ex} = K_{VCO} \int V_{cont} dt \tag{2.5}$$

$$\frac{\phi_{ex}}{V_{cont}} = \frac{K_{VCO}}{s} \tag{2.6}$$

Therefore the VCO acts as an ideal integrator, providing a pole at $s = 0$ in the open loop transfer function in the PLL.

2.3.4 Loop Filter

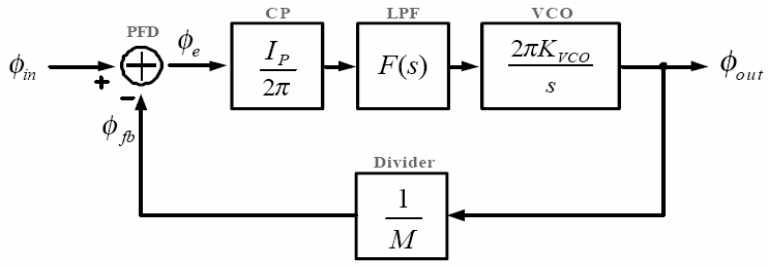


Fig. 2.11 PLL-based frequency synthesizer linear model

However, before further examining the loop filter, linear models of the PLL-based frequency synthesizer should be established. With proper characteristic of each function block, the close-loop behavior of frequency synthesizers can be analyzed. A linear model of a charge-pump PLL-based frequency synthesizer is shown in Fig. 2.11. Note that the input and output signals are phase (rad/s). Phase error ϕ_e, the difference between the input phase ϕ_{in} and the feedback ϕ_{fb}, is extracted by the PFD, which is represented by a simple PLL in the linear model. The charge pumps (CP) then translate ϕ_e into a current signal with a gain of $I_P/2\pi$, where I_P is the pump current. This current signal (A) flows into the passive filter (Ω), and is converted to voltage signal (V) at the control input of the VCO. The VCO generates an output signal whose frequency is related to the control input voltage with a gain of K_{VCO} (Hz/V). Since the phase signal rather than frequency signal is the variable in this linear model, the VCO block include a "1/ s" term that integrates the frequency signal to derive the phase signal. The frequency divider in the feedback path is still a sample "1/ M" factor since division in frequency domain has the same effect in phase domain. Hence, the open-loop transfer function can be represented as:

$$G(s) = \frac{I_P}{2\pi}.F(s).\frac{2\pi K_{VCO}}{s}.\frac{1}{M} \tag{2.7}$$

$$G(s) = \frac{I_P \cdot K_{VCO}(1+s\cdot R_P C_P)}{s^2 \cdot M \cdot C_P} = \frac{I_P \cdot K_{VCO} \cdot R_P}{M} \cdot \frac{s+w_z}{s^2}$$
$$,where\ w_z = \frac{1}{R_P C_P} \tag{2.8}$$

The loop bandwidth K, defined as the unity gain frequency of the open-loop transfer function, can be found assuming that K is much greater than w_z:

$$G(s) = \frac{I_P \cdot K_{VCO} \cdot R_P}{M} \cdot \frac{s+w_z}{s^2} \approx \frac{I_P \cdot K_{VCO} \cdot R_P}{M} \cdot \frac{1}{s} = 1$$
$$\Rightarrow \quad K \approx \frac{I_P \cdot K_{VCO} \cdot R_P}{M} \tag{2.9}$$

Thus the open-loop transfer function can be rewritten as:

$$G(s) = K \cdot \frac{s+w_z}{s^2} \tag{2.10}$$

The simplest LPF is to connect a capacitor to the control voltage. The open-loop transfer function is derived as follows:

$$\frac{V_{out}}{\Delta\phi}(s) = \frac{I_p}{2\pi C_p}\frac{1}{s} \tag{2.11}$$

$$\frac{\phi_{out}}{\phi_{out}}(s)\Big|_{open} = \frac{I_p}{2\pi C_p}\frac{K_{vco}}{s^2} \tag{2.12}$$

Since the loop gain has two poles at the origin, this topology is called a “type II” PLL. It is unstable because the loop gain has two poles at the origin. As illustrated in Fig. 2.12(a), each integrator provides constant 90° phase shift. Thus the system will oscillate at the unit-gain frequency. So, we have to add a zero to increase phase margin.

We can thus add a resistor in series with the original capacitor. The open-loop transfer function is derived as follows:

$$\frac{V_{out}}{\Delta\phi}(s) = \frac{I_p}{2\pi}\left(R_P + \frac{1}{sC_P}\right) \tag{2.13}$$

$$\frac{\phi_{out}}{\phi_{out}}(s)\Big|_{open} = \frac{I_p}{2\pi}\left(R_P + \frac{1}{sC_P}\right)\frac{K_{vco}}{s} \tag{2.14}$$

As shown in Fig. 2.12(b), the phase margin will increase because of the zero $1/(R_P C_P)$ and the system will not oscillate at the unit-gain frequency. However, a severe problem occurred in such PLLs. Due to the resistor in series with capacitor, each time a current is injected into the loop filter and then produces large voltage jump. It makes ripples of control voltage of VCO and degrades the purity of the output frequency spectrum.

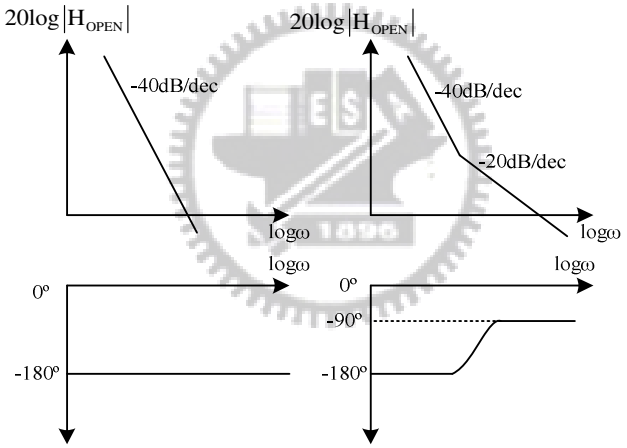


Fig. 2.12 (a) Loop gain of simple PLL (b) addition of zero

We can ease this effect by adding a second capacitor in parallel with R_P and C_P. The loop filter is now of 2nd order and the open loop transfer function of PLL now is of third-order and has stability problem, as shown in Fig. 2.13 (a). But if we make C_2 is about one-fifth to one-tenth of C_P, the open-loop transfer function is near the second-order and would be stable.

$$F(s) = K_h \frac{s + w_2}{s\left(\frac{s}{w_1} + 1\right)} \tag{2.15}$$

where $K_h = \frac{C_P R_p}{C_P + C_2}$, and $\omega_2 = \frac{1}{C_P R_p}$, $\omega_1 = \frac{C_2 + C_P}{C_2 C_P R_p}$

Moreover, current switching in the charge pump at the reference frequency f_{ref} would cause unwanted sidebands at the frequency spectrum of VCO. We can add additional LPF to suppress the spur that is f_{ref} offset from the carrier frequency, as shown in Fig. 2.13 (b). The loop filter transfer function is

$$F(s) = K_h \frac{s + w_2}{s\left(\frac{s}{w_1} + 1\right)\left(\frac{s}{w_3} + 1\right)} \tag{2.16}$$

where $K_h = \frac{C_2 R_2}{C_1 + C_2}$, and $\omega_2 = \frac{1}{C_2 R_2}$, $\omega_1 = \frac{C_1 + C_2}{C_1 C_2 R_2}$

$$\omega_3 = \frac{1}{C_3 R_3}$$

The additional pole must be lower than the reference frequency in order to significantly attenuate the spurs. However, it must be at least five times higher than the loop bandwidth, or the loop will almost assuredly become unstable.

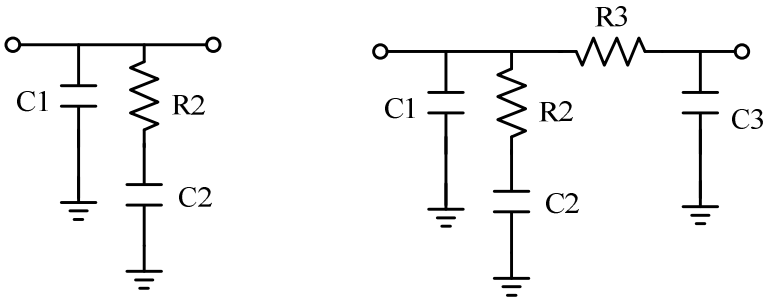


Fig. 2.13 (a) 2nd order loop filter (b) 3rd order loop filter

2.3.5 Frequency Divider

Frequency dividers are used to synthesize a high frequency LO from a precise low frequency crystal oscillator. The output frequency f_{div} equals the input frequency f_{in} divided by an integer number. From this information we could derive a model for

the divider in the phase domain.

The phase θ_{in} of the input signal is given by

$$\theta_{in}(t) = 2\pi f_{in} t + \theta_p \sin 2\pi f_m t \tag{2.17}$$

And the instantaneous frequency of the input signal is:

$$f_{inst}(t) = \frac{1}{2\pi} \frac{d\theta_{in}(t)}{dt} = f_{in} + \theta_p f_m \cos 2\pi f_m t \tag{2.18}$$

$$f_{div} = \frac{f_{inst}}{N} = \frac{f_{in}}{N} + \frac{\theta_p f_m \cos 2\pi f_m t}{N} \tag{2.19}$$

And the phase of the output signal can now be found as:

$$\begin{aligned} \theta_{div}(t) &= \int 2\pi f_{div}(t)\, dt \\ &= 2\pi \frac{f_{in}}{N} t + \frac{\theta_p}{N} \sin 2\pi f_m t = \frac{\theta_{in}(t)}{N} \end{aligned} \tag{2.20}$$

2.4 Noise Analysis of the PLL Synthesizer

The job of any frequency synthesizer is to generate a spectrally pure output signal. An ideal periodic output in the frequency domain has only an impulse at the fundamental frequency and perhaps some other impulse energy at DC and harmonic. In the actual oscillator implementation, the zero crossings of the periodic wave vary with time as shown in Fig. 2.14. This varying of the zero crossings is known as time domain jitter.

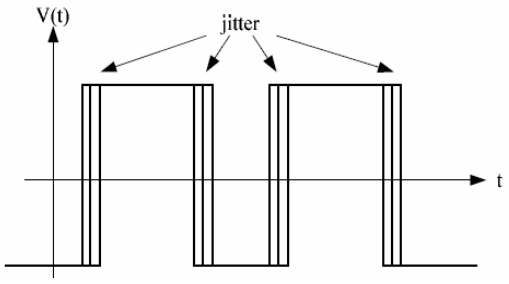


Fig. 2.14 Periodic signal with jitter

A PLL-based frequency synthesizer suffers from introduced at input or

generate by the other building blocks. It is important to learn how different noise sources affect the noise performance of the output signal. The sources of noise may be classified into two types: (1) the noise at input, and (2) the noise of VCO.

2.4.1 Input Noise Source

An input reference signal with phase noise can be modeled in the PLL as shown in Fig. 2.15(a) [5].

The input noise, Φ_{in}, is treated as an input signal and the same PLL transfer function for the input noise transfer function. The input phase noise transfer function is plotted in Fig. 2.15(b).

$$\frac{\Phi_{out}(s)}{\Phi_{in}(s)} = N \cdot \frac{s\left(2\zeta w_n - \frac{Nw_n^{\,2}}{dx}\right) + w_n^{\,2}}{s^2 + 2\zeta w_n s + w_n^{\,2}} \tag{2.21}$$

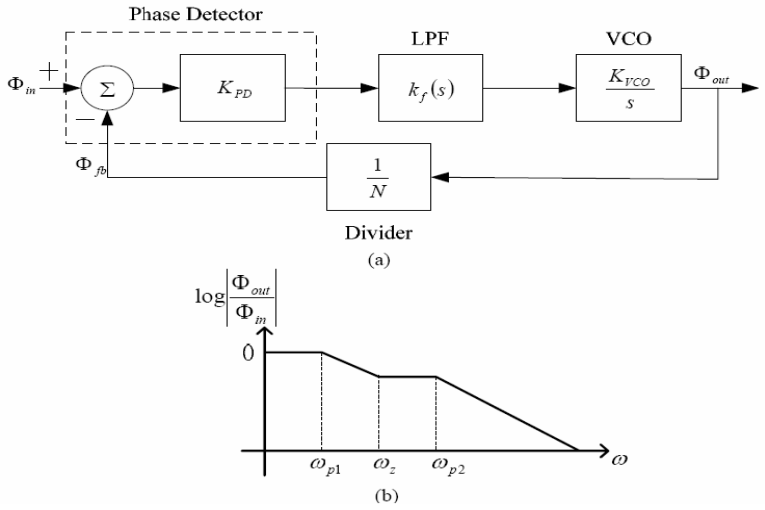


Fig. 2.15 (a) PLL Input Phase Noise Model
(b) Bode plot normalized transfer function

The input phase is shaped by the low-pass characteristic of the second-order PLL. In order to reduce the phase noise in the output signal due to the input phase noise it is desired to make the PLL bandwidth as narrow as possible. Notice that the input noise is amplifier by a factor of *N*. If input noise is a concern, the lowest possible value of *N* should be used. Usually in frequency synthesizer design the

input phase noise is not a concern because the reference signal generally comes from a low phase noise crystal oscillator.

2.4.2 Noise of VCO

The phase noise of the VCO can be modeled as Fig. 2.16(a) [5]. The VCO phase noise, V_{CON}, is treated as an input signal and following transfer function is plotted in Fig. 2.16(b).

$$\frac{\Phi_{out}(s)}{\Phi_{vcon}(s)} = \frac{s^2 + \frac{sw_n{}^2 N}{K_{PD}K_{VCO}}}{s^2 + 2\xi \cdot \omega_n s + \omega_n{}^2} \tag{2.22}$$

The VCO phase noise is shaped by a high-pass characteristic by the second-order PLL. In order to reduce the phase noise in the output signal due to the VCO phase noise it is desirable to make the PLL bandwidth as wide as possible. Here a tradeoff regarding loop bandwidth position and its effect on input phase noise contribution and VCO phase noise contribution is observed. The optimum loop bandwidth depends on the application. It is optimal to have a narrow loop bandwidth for input noise performance.

Narrow band loops aid in the cases where the PLL is operating with a noisy reference signal. It is optimal to have a wide loop bandwidth for VCO noise performance. Usually the dominant source of noise is the VCO in fully integrated frequency synthesizer design [6].

The VCO phase noise is caused by such things as the upconverted *1/f* noise from the transistor used to design the VCO, noise in the control path, and cycle-to cycle fluctuations in the power supply[7][8]. With the VCO contributing significant phase noise it is optimal to make the loop bandwidth as wide as possible.

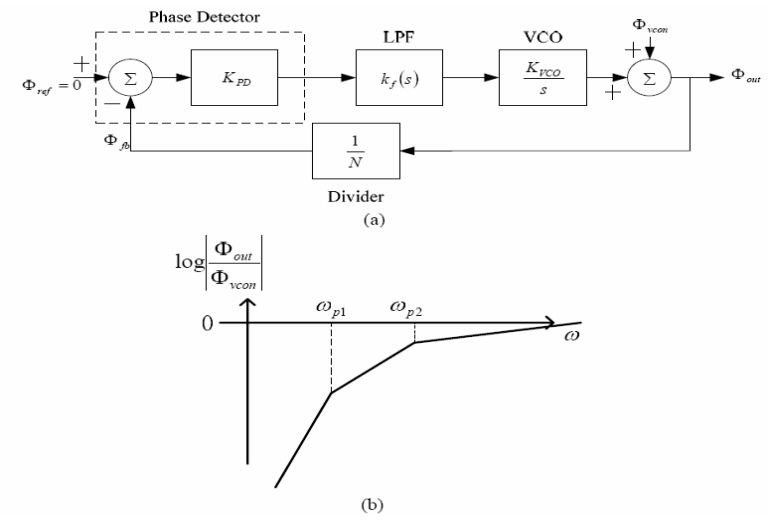


Fig. 2.16 (a) Noise transfer function of a PLL from VCO to output
(b) Bode plot of the normalized transfer function

The total phase noise can be derived by adding the above two eventual phase noises, as shown in Fig. 2.17. It is obviously that when the frequencies nears carrier, the REF in the closed loop dominate the total phase noise. Otherwise, the VCO dominates. If we want to suppress the phase noise of REF, we can decrease the BW. However, it will raise the phase noise of VCO. On the contrary, increasing the BW will suppress the phase noise of VCO but raise the phase noise of Ref. It is a trade off. How we decide the best BW is important.

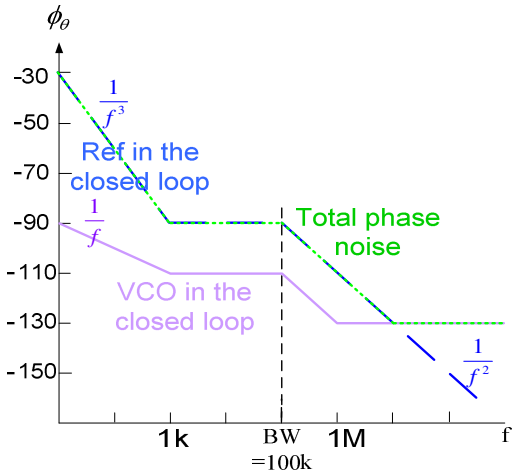


Fig. 2.17 Total output phase noise

Chapter 3

Fractional-N PLL

3.1 The Fractional Mechanism

Before studying the fractional architecture, we make an observation. Suppose, as shown in Fig. 3.1, a pulse is removed every T_P seconds from a periodic signal *x(t)* that has a frequency *f1*. The resulting waveform, *y(t)* then exhibits $f1 \cdot T_P$-1 pulses every T_P seconds, i.e., *y (t)* has an "average" frequency equal to $f1$-$1/T_P$. This method can be used to vary the average frequency of a signal by small steps. We should note, however, that *f (t)* is not a strictly periodic signal. The idea of removing pulses nevertheless useful in fine-step frequency synthesis.

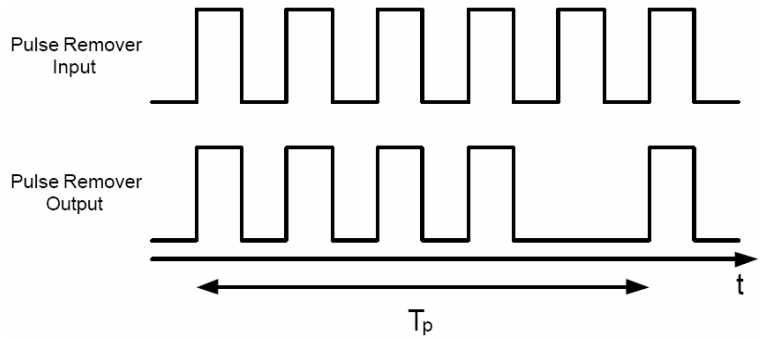


Fig. 3.1 Periodic removal of a pulse from a periodic waveform

Fig. 3.2(a) shows simple fractional-N architecture. In addition to the PFD, LPF, and VCO, the loop incorporates a pulse remover, a circuit that blocks one input pulse upon assertion of the remove command. Since under locked condition the two

frequencies presented to the phase detector must be equal, the average output frequency of the pulse remover equals f_{ref}, and hence $f_{out}=f_{ref}+1/T_P$, where T_P is the periodic with which the remove command is applied. Note that f_{out} can vary by a fraction of f_{ref} because the frequency $f_p=1/T_P$ can be derived from f_{ref} by simply division. Provided by a crystal oscillator, f_{ref} is typical limited to a few tents of megahertz. Thus, as shown in Fig. 3.2(b), a fractional-N synthesizer incorporates a divider in the feedback to generate high output frequencies.

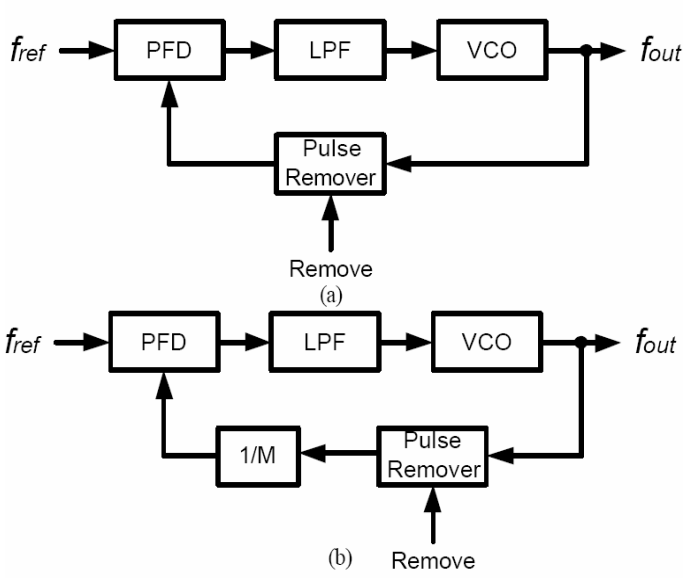


Fig. 3.2 (a) simple fractional-N synthesizer (b) use of divider in the loop

While the original fractional-N topology was based on the pulse remover concept [9], modern implementations of this architecture operate on a somewhat different principle. Depicted in Fig. 3.3, such a synthesizer replaces the pulse remover and the divider of Fig. 3.2 (b) with a dual-modulus prescaler. If the prescaler divides by N for T_N output pulses (of the VCO) and by $N+1$ for T_{N+1} output pulses, shown in Fig. 3.3 (b), then the equivalent divide ratio is shown as

$$
\begin{aligned}
f_{vco,avg} &= \frac{1}{(T_N + T_{N+1})}\left[T_N \cdot N \cdot f_{ref} + T_{N+1} \cdot (N+1) \cdot f_{ref}\right] \\
&= \left[N + T_{N+1}/(T_N + T_{N+1})\right] \cdot f_{ref} \\
&= (N \cdot f) \cdot f_{ref}
\end{aligned}
\tag{3.1}
$$

This value can vary between *N* and *N+1* in fine steps by proper choice of A and B. The resulting modulus is sometimes written as *N.f*, where the dot denotes a decimal point and *N* and *f* represent the integer and fractional parts of the modulus.

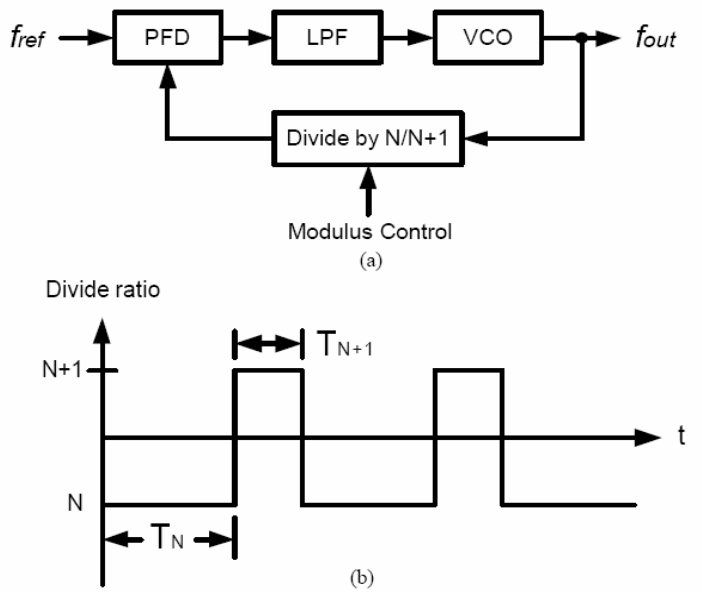


Fig. 3.3 (a) Fractional-N synthesizer using a dual-modulus divider,

(b)Timing diagram

3.2 The First Order Fractional-N Synthesizer

Fig. 3.4 shows the fractional-N PLL [10] which the accumulator and the cycle swallower become part of the circuit. The operation principle of this structure is the same as the one described in Fig. 3.3(b). Fig. 3.5 shows the detail circuits and timing diagram of the cycle swallower. To operate, a chain of VCO pulses serves as the clock for the flip-flop. A swallow trigger signal is illustrated generally as being asynchronous with the VCO pulses. However, flip-flop will trigger on the negative

edge of swallow trigger and output a Q_1 pulse to flip-flop. When the next negative edge of VCO signal appears at the clock of flip-flop, the Q_2 output goes negative. This output resets flip-flop and also provides an "off" input to AND gate. Thus, the next VCO pulse will not appear at the output of AND gate; that is, has been swallowed. The negative edge of pulse again triggers flip-flop allowing the subsequent pulses of the VCO signal to pass through AND gate.

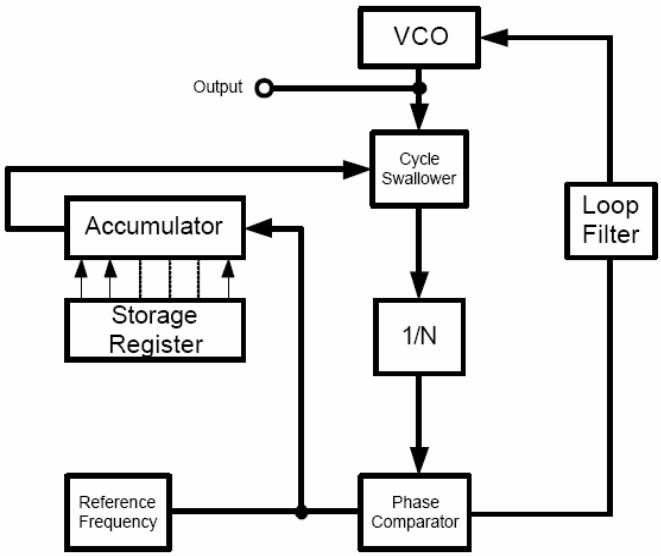


Fig. 3.4 Fractional-N synthesizer using a cycle swallower and an accumulator

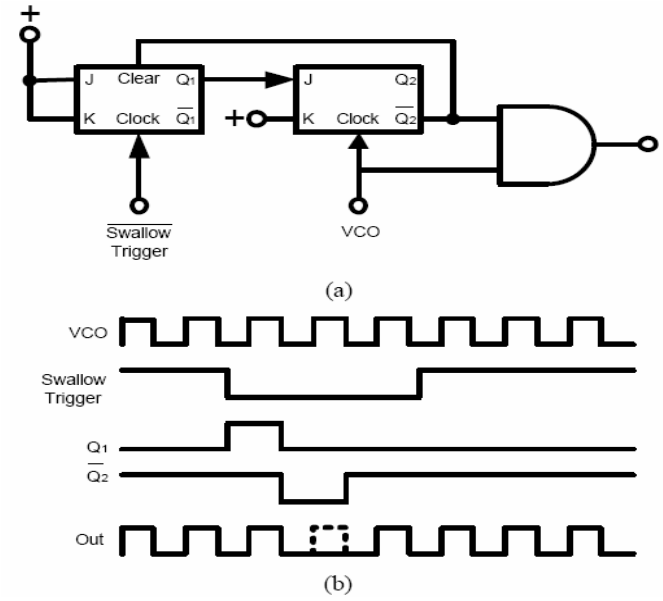


Fig. 3.5 (a) Cycle swallower circuit, (b) Its timing diagram

From Fig. 3.3(b), this periodic modification of the divider modulus gives rise to a sawtooth phase error (Fig. 3.6). If unfiltered, the phase error causes severe spurious tones-fractional spurs at all multiples of the offset frequency (.$f \times f_{ref}$).

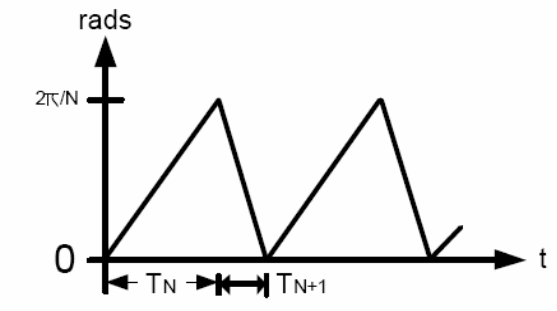


Fig. 3.6 Sawtooth phase error for the first order fractional-N synthesis

3.3 The Second Order Fractional-N Synthesizer

The fractional spurs in the above-mentioned averaging fractional-N synthesis are a serious problem. An important can be achieved by analog compensation of the phase error [11, 12, 13]. The output of the phase register of the digital accumulator is a measure for the phase error. The phase register is a kind of "bookkeeping system" that tracks the phase advancement of the VCO for every reference cycle. Due to the loop integration the actual phase detector output becomes an analog sawtooth waveform which is mentioned in Fig.3.7.Using a DAC (Digital-to-Analog) the staircase output of the phase register can be converted to an analog sawtooth current, scaled by A (Fig. 3.7) to match the phase error. By summing the phase detector output and the DAC output on the loop filter capacitors, the AC component is in the ideal case removed from the phase error. The VCO output is now only driven by the wanted DC phase error, canceling all fractional spurs in the output spectrum.

However, this method has several disadvantages. First of all, the maximum

amplitude of the phase error depends on f_{ref}, such that the DAC output amplitude must be variable, while its input is constant. Secondly, the sampling frequency of the DAC can be rather high. To have fast setting (large loop bandwidth), the f_{ref} can easily be some tens of MHz. The sampling frequency of the DAC must be at least $2\times f_{ref}$, for a full Nyquist DAC, to be able to compensate spurs up to the reference frequency. To have a spurious suppression of at least -70dB, required in most telecommunication system, the accuracy of the DAC must be around 8 bits [14]. This occupies a larger chip area and dissipates the power consumption. Thirdly, due to matching issues, the accuracy of the cancellation is limited, requiring external adjustment and calibration. Therefore, the analog compensation method is not a viable solution for all integration of frequency synthesizers for wireless communication systems in CMOS technology.

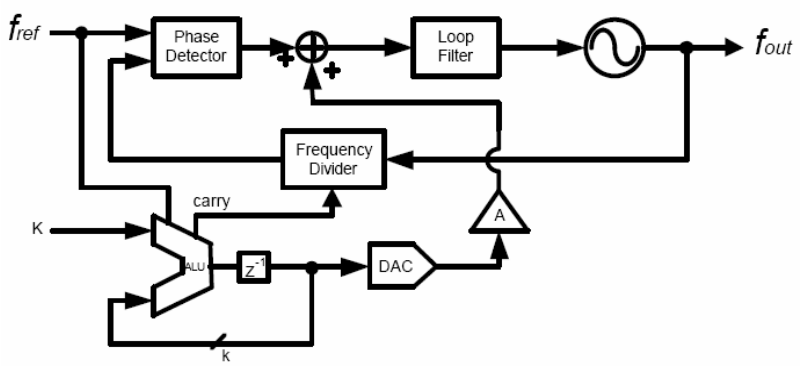


Fig. 3.7 The analog phase interpolator

3.4 The Third Order Fractional-N Synthesizer

The next significant evolutionary step for fractional-N synthesizer will be an all-digital implementation, known as *delta-sigma modulator (DSM)*, eliminating spurious digitally and allow good phase noise performance by digitally noise-shaping techniques, as shown in Fig. 3.8 [15]. The DSM architecture used in this paper terms as a Multistage Noise Shaping (MASH) which is cascaded by three

first-order modulator to ensure the stability. It is assumed random to model each 1-bit quantizes as a unity gain element with added quantization noise. N.F is the desired rational divide ratio and N_{div} (k) is the actual sequence presented to the integer divider. The transfer function is

$$Ndiv(z) = N_{.}f(z) + (1 - z^{-1})^3 \times E_{q3}(z) \tag{3.2}$$

In a locked PLL,

$$\begin{aligned} f_{out} &= N_{div} \times f_{ref} \\ F_{out}(z) &= N_{.}F(z) \times f_{ref} + E_{q3}(z)(1 - z^{-1})^3 \times f_{ref} \end{aligned} \tag{3.3}$$

Where the first term is the desired frequency and the second term represents frequency noise due to delta-sigma modulation.

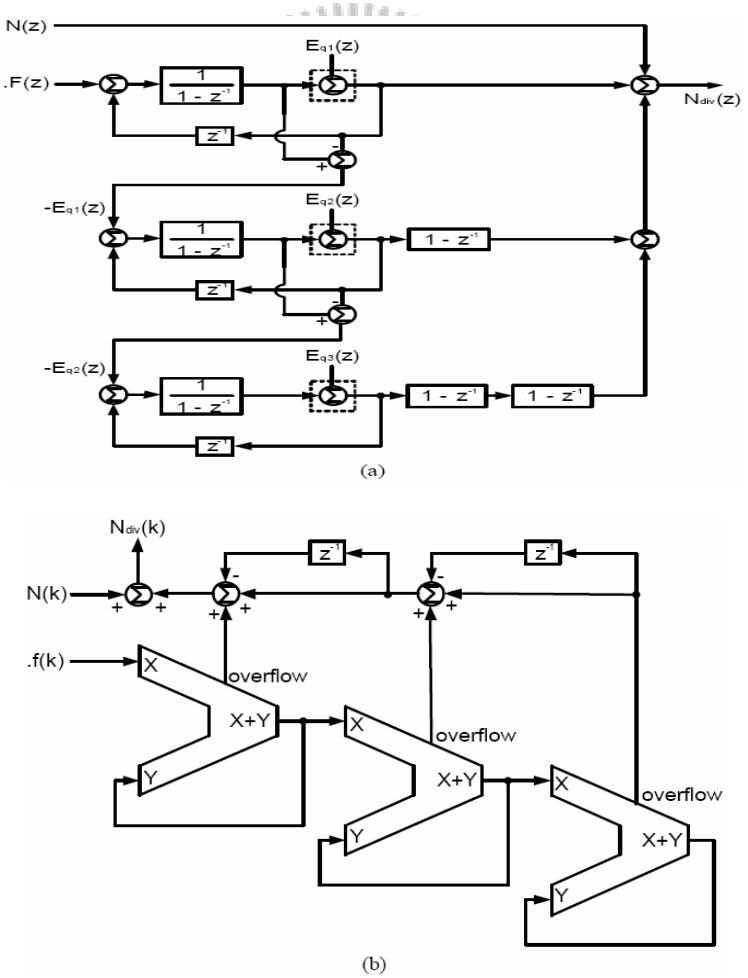


Fig. 3.8 (a) 3-order MASH DSM (b) Its digital equivalent architecture

By converting to the frequency domain and generating to any number of modulators, the power spectral (PSD) which is considered with small offset ranges compared to the reference frequency is [15].

$$S_E(f) \approx \frac{(2\pi)^2}{12 f_{ref}} \left[\frac{2\pi f}{f_{ref}} \right]^{2(m-1)} \quad rad^2 / Hz \tag{3.4}$$

The system in Fig. 3.8 can be simplified when it is recognized that an accumulator is a compact realization of the delta-sigma modulator as shown in Fig. 3.8 (b). This architecture leads to the all digital implementation easily. Regardless of the advantages of low phase noise, low reference feedthrough spurs, fast tuning speed, and small step size for this architecture, fractional spurs is a design issue to overcome. In addition, when the DSM is fed with a DC input, the quantized signal bounces between two levels and may be periodic. The structure of such quantization is known as pattern noise, or idle tones. Since this is the desired architecture for the fractional-N synthesizer in this thesis, we will consider this problem and figure out how to solve these problems?

3.4.1 Delta-sigma modulators

DSMs are basically divided into two types: *single-stage* and *cascaded*. Digital DSMs, unlike their analog counterparts, don't have any non-idealities, and when the modulator is stable, there is no overload problem. Cascaded digital modulators won't suffer from mismatches and noise leakage from front stages, and multi-bit quantizer won't suffer from any nonlinearity, which doesn't exit digital modulator at all.

To understand the function of the DSM, one should know the building block: the first-order DSM or the accumulator. A block diagram of the first-order DSM with the error-feedback topology is shown in Fig. 3.9(a), where the quantizer is modeled as an additive white noise source e[n]. The signal-flow graph for this modulator in its digital implementations is illustrated in Fig. 3.9(b), where the m-bit

input signal K[n] is summed with the m-bit register content to produce the (m+1)-bit quantizer input signal v[n]. The 1-bit quantization process is accomplished by simply taking the most significant bit (MSB) of v[n]. The residual m-bit signal, which represents the negative of the quantization error signal, is then stored in the m-bit register to be summed with the input signal at the next clock cycle. The accumulator overflow and the accumulator result correspond to the 1-bit quantizer output and the negative of the quantization error at any time, respectively.

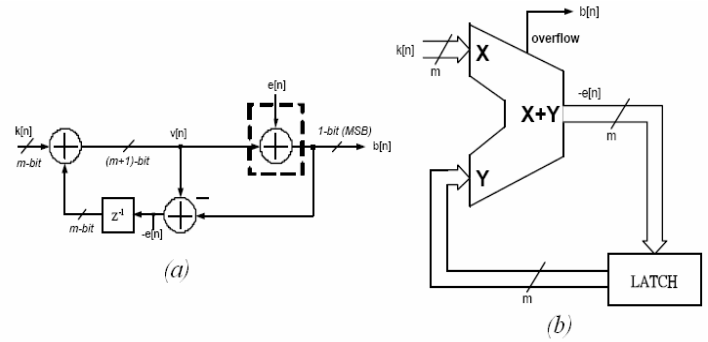


Fig. 3.9: A first-order DSM (a) block diagram, (b) its digital implementation

The transfer function of the first-order DSM is

$$B(z) = K(z) + (1 - z^{-1})E(z) \tag{3.5}$$

Thus the power spectral density is

$$S_B(f) = S_K(f) + \left[2\sin\left(\frac{\pi f}{f_s} \right) \right]^2 S_E(f) \tag{3.6}$$

Where f_s is the sampling frequency or the reference frequency, f_{ref}, for the synthesizer. Note that 1-bit quantizer is assumed to have uniform quantization error and the power is spread over a bandwidth of f_{ref}. Consequently, the power spectral density (PSD) of quantization error is 1/ (12 f_{ref}). Note that the second term of Eq. 3.7 is the PSD introduced by the quantization noise. Generally, where m is the order of the DSM.

$$S_f(f) = \frac{1}{12 f_{ref}} \left[2\sin\left(\frac{\pi f}{f_{ref}} \right) \right]^{2m} \tag{3.7}$$

To illustrate the noise shaping action of the DSM, one can apply a sinusoid with amplitude A, frequency f_o to the DSM input. Fig. 3.2 shows the PSD of the first-order DSM. The high frequency band shows the 20dB/dec noise shaping. Note that there exists many spurs around the signal which will effect the noise requirement targeted in many wireless system. Thus, the first DSM is not suitable to the fractional-N synthesis.

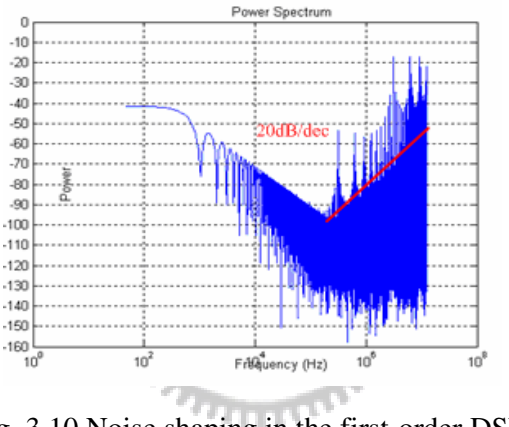


Fig. 3.10 Noise shaping in the first-order DSM

2nd and 3-order DSMs are practically used for fractional-N synthesizers. 4th or even higher order modulators are rarely used because it's difficult to suppress the phase noise at higher frequencies by limited order of loop filter. We will study the second-order cascaded and single-loop DSM in the next two sections.

3.4.2 The Cascaded Modulator

The cascaded 1-1 or MASH (multi-stage noise-shaping) DSM modulator is shown in Fig. 3.11. The MASH modulator consists of a cascaded of first-order modulators, whose quantization error $-E_i$ is the input to the next modulator. By summing the filtered versions of the first-order outputs, the quantization error of the first modulator is cancelled. Since the DSM modulator in fractional-N PLLs is an all

digital implementation, the cancellation is perfect. The output of the modulator with perfect cancellation is:

$$\begin{aligned} Y &= .f + (1 - z^{-1})E_1 + \left[-E_1 + \left(1 - z^{-1}\right)E_2 \right]\left(1 - z^{-1}\right) \\ &= .f + (1 - z^{-1})^2 E_2 \end{aligned} \tag{3.8}$$

Thus,

$$N_{div} = N.f + (1 - z^{-1})^2 E_2 \tag{3.9}$$

The equations expose the most important quality of a MASH modulator, i.e. its unconditional stability for any modulator order, because of its first order nature. Another advantage is the integration of the MASH modulator in plain CMOS technology, since only adders and register are needed to implement the noise shaping function.

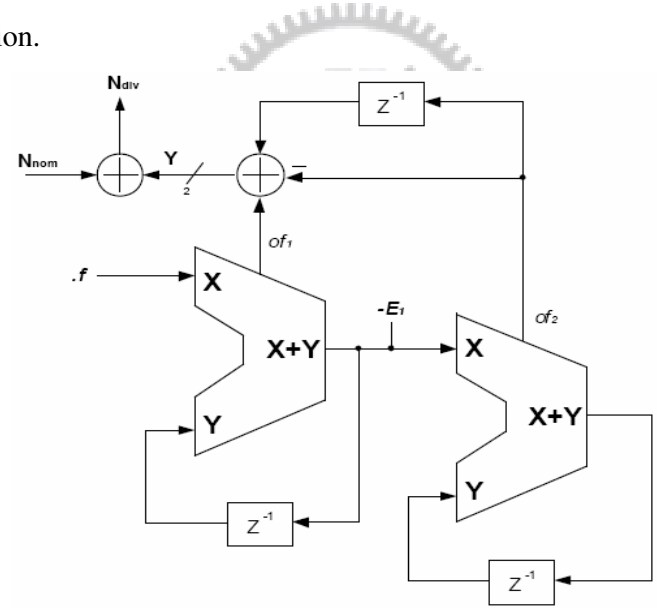


Fig. 3.11 The 2nd –order MASH modulator

In the implementation of Fig. 3.11, the output is a 2-bit word with a mean value, fractional number *.f*. With N_{norm} added, the nominal frequency could be tuned for the purpose of targeted frequency band. Note that to increase the output dynamic range of the modulator to accommodate more division moduli, multiple MSBs can be taken as outputs of the first-order modulators instead of the single bit output, of_1[16].

To obtain the theoretical PSD in the locked PLL, using Eq. (3.10)

$$F_{out}(z) = N \cdot f(z) f_{ref} + (1 - z^{-1}) f_{ref} E_2(z) \tag{3.10}$$

Applying the PSD of $E_2=1/(12f_{ref})$ and knowing that the second term of Eq. (3.11) is the frequency fluctuations of $F_{out}(z)$,

$$\begin{aligned} S_{fE}(z) &= \left|(1 - z^{-1})^2 f_{ref}\right|^2 (1/12 f_{ref}) \\ &= \left|1 - z^{-1}\right|^4 (f_{ref}/12) \end{aligned} \tag{3.11}$$

We want phase fluctuations, not frequency fluctuation.

$$\phi(t) = \int w(t)\,dt = 2\pi \int f_E\,dt \tag{3.12}$$

Employing a simple rectangular integration to represent $\int dt$ in the z-domain,

$$\Phi(z) = \frac{T_s w(z)}{1 - z^{-1}} = \frac{2\pi T_s F_E(z)}{1 - z^{-1}} \tag{3.13}$$

Where $T_s=1/f_{ref}$ is the sample period. With Eq. (3.12) and Eq. (3.13), we obtain

$$\begin{aligned} S_{\Phi}(z) &= \frac{(2\pi)^2}{\left|1 - z^{-1}\right|^2 f_{ref}^2} \cdot \frac{\left|1 - z^{-1}\right|^4 f_{ref}}{12} \\ &= \frac{(2\pi)^2}{12 f_{ref}} \left|1 - z^{-1}\right|^2 rad^2/Hz \end{aligned} \tag{3.14}$$

Converting to the frequency domain and generalizing to any number of modulator sections,

$$S_E(f) = \frac{(2\pi)^2}{12 f_{ref}} \left[2 \sin\left(\frac{\pi f}{f_{ref}}\right)\right]^{2(m-1)} rad^2/Hz \tag{3.15}$$

We can simplify the above expression by taking advantage of the assumption that the offset range is small compared to the reference frequency.

$$S_E(f) \approx \frac{(2\pi)^2}{12 f_{ref}} \left[\frac{2\pi f}{f_{ref}}\right]^{2(m-1)} rad^2/Hz \tag{3.16}$$

Note that this is the derivation of Eq. (3.4).

In the frequency domain, the intensive use of modulus dynamic range translates

in substantial levels of high frequency. This is reflected in the noise transfer function (NTF) of the MASH modulator, which is $(1-z^{-1})^2$ (see Eq. (3.10)). Fig. 3.12 shows the simulated output spectrum for this MASH 1-1 modulator. Compared to the Eq. (3.8), it provides the 40Db per decade for high frequency noise shaping.

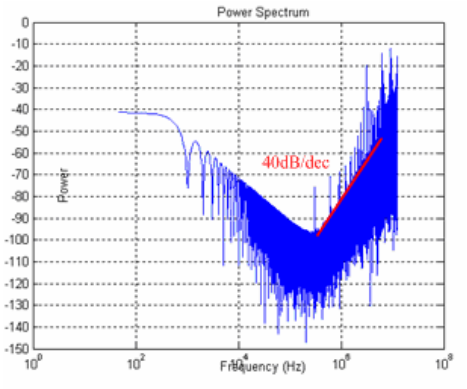


Fig. 3.12 The theoretical and simulated output spectrum for the MASH 1-1 modulator

3.4.3 The Single-Loop DSM Modulator

The single loop DSM multiple-feedback modulator is shown in Fig. 3.13. In contrast to the MASH modulator, this modulator consists of a single, 2^{nd}-order discrete time filter with multiple feedback coefficients, which influence the NTF. Compared with MASH architectures, single-loop architecture has better noise shaping characteristics for dc inputs. But it is subject to instability and smaller stable input range. The latter limitation can be eliminated with a multi-bit quantizer in digital DSMs. Note that the input is also subject to a non-unity transfer function. This poses no problem for frequency synthesis, since the DC value of the input is passed unaltered. But problems arise when the synthesizer is used for data transmission, where the modulated data stream will be shaped by the DSM signal transfer function. The dc output of this modulator is given by X/M where X and M are parameters that can be set externally. Thu use of an M quantizer allows the channel spacing to be the reference frequency divided by a selectable M rather than

a fixed 2^k. The introduction of M is also for the stability purpose making the wider quantization room.

The NTF of this single-loop DSM is:

$$H_n(z) = \frac{z^{-1}(1 - z^{-1})^2}{(1 - z^{-1})^2 + (1 - z^{-1})^2} \tag{3.17}$$

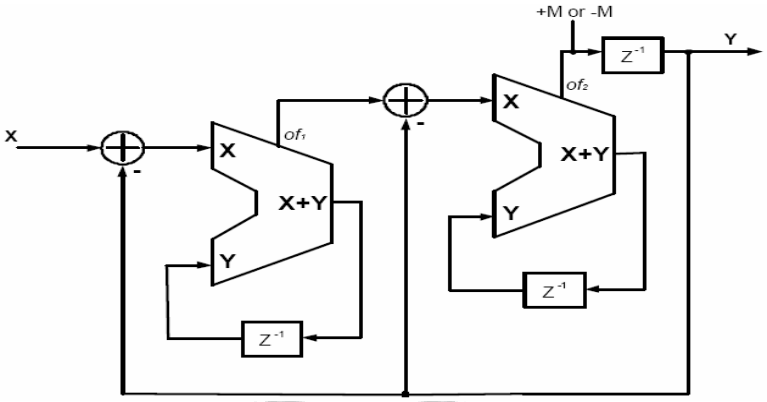


Fig. 3.13 The 2nd-order single-loop DSM with multiple feedback coefficients

3.5 Other Types

The basic idea adopted by the three kinds of the structures discussed previously is to get the fractional output frequency by changing the "integer" ratio in the trick of averaging. A technique, fractional-N synthesizer, evolves from the fundamental principles of integer-N synthesis. The only difference is that the frequency divider is replaced with a fractional divider. A fractional frequency divider is no longer a simple digital counter. The period of the divider output, T_{do}, is given by

$$T_{do} = (N + 0.F) \times T_{VCO} \tag{3.18}$$

Where *0.F* denotes a fractional number and T_{VCO} is the period of the VCO. Here we need to emphasize that the period of a fractional divider output is ideally not time varying once *N* and *0.F* are set. In other words, a rising edge occurs at the output each and every *N* and *0.F* VCO cycles. Fig. 3.14 is a timing diagram

illustrating the operation of a fractional divider where N.F is set to be 2.25.

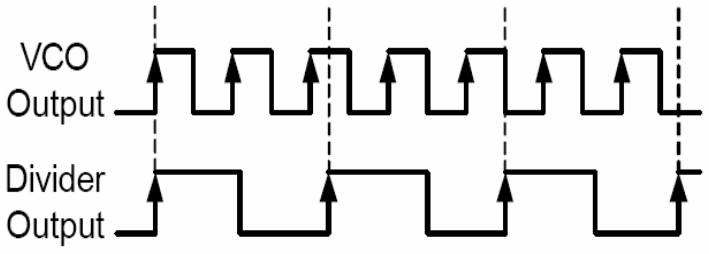


Fig. 3.14 Timing diagram of a fractional-N frequency divider

$$f_{VCO} = (N + 0.F) \times f_{ref} \tag{3.19}$$

A brief description of a simple circuit realization of a fractional frequency divider is given. The block diagram is depicted in Fig. 3.15(a) [17]. As is clear from this figure, the divider comprises a dual modulus divider (DMD), a delay locked loop (DLL), a multiplexer (MUX) and digital phase accumulator (DPA). Note, however, that a fractional divider does not have to be based on a DLL. The DLL shown in this figure consists of a set of cascaded, tunable, delay element, a PD, a CP and a D-type flip-flop. The negative nature of the feedback in the DLL ensures that the total delay through the delay line is one VCO cycle. Since the delay elements are, ideally, identical, a VCO period is broken up into Nd equal of phase, where Nd is the number of delay elements in the delay line.

A simple digital phase accumulator is made of an adder and a register, as is shown in Fig. 3.15(b). The register is clocked by the reference. The input to the DPA is an m-bit word. The content of the register are used to control the MUX. On every reference rising edge, the contents will be incremented by the value of the input, x, which is presented by an m bits word. The output of the DPA, ie., the carry-out of the adder, is a 1-bit quantization of the input. The number of bits in the accumulator is related to the number of discrete of phase by N^d=2m, the output of the DPA controls the DMD. When carry-out is high, the DMD divides by N+1 as opposed to

N when carry-out is low. As we will see in the following example, the fractional division ratio, N+0.F, for a DPA input of x is equal to $N+x/2^m$. Suppose the DPA has 3 bits and, therefore, the delay line has 8 elements each phase corresponds to 1/8 of a VCO cycle. Also assume that the input is equal to 2, which corresponds to a 0.F of 2/8. When no carry-out occurs, the DMD divides by N. Its output, however, is not immediately presented to the PFD of the PLL. Rather, it will be delayed by a number of phase controlled or selected by the MUX. This number is equal to the content of the PDA, which is incremented by 2 every reference cycle. This means that the output is phase shifted by a progressively increasing number of phase, i.e., 0, 2, 4, 6, 8 each reference cycle. As a result, the period of the DMD output is increased by 2/8 of a VCO cycle. Therefore, the effective division ratio becomes N+0.25, which is what it should be. When the DPA content reaches 8, the content of DPA will be reset and the output of the DMD will not be delayed by the delay line. However, this coincides with a carry-out, which forces the DMD to divide by N+1. This is equivalent to the DMD dividing by N and its output being delayed by 8 phase, i.e., one VCO cycle.

The design of the fractional divider dictates the fractional modulus or fractional denominator to be Nd, the number of delay elements. Since all the elements in the delay line operate at the VCO speed, the added power consumption can be significant, especially when the VCO frequency and/or fractionality are high. Another drawback of this method is that the edges of the fractional divider output mat be contaminated or jittery as a result of jitter on the outputs of the delay elements. Jitter is present due to mismatch and phase error due to the phase error correcting action of the DLL. The edge contamination may result in a significant increase in the PD noise floor.

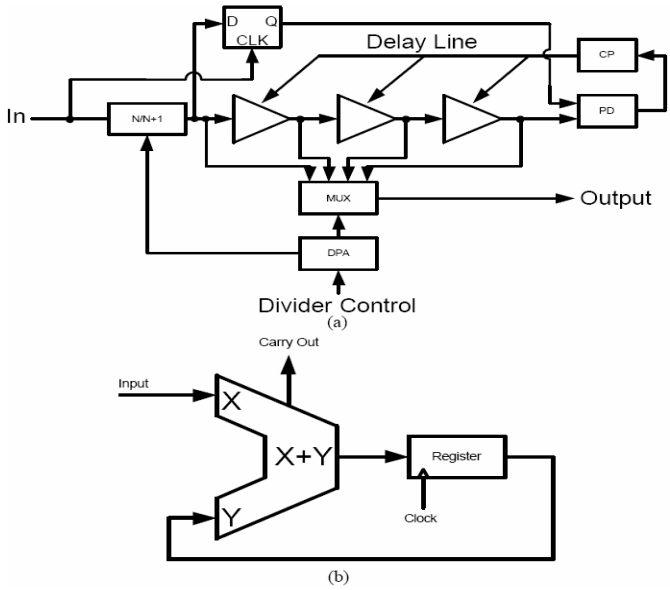


Fig. 3.15: (a) An example of fractional-N divider (b) digital phase accumulator

3.6 Expressions for Jitter and Phase noise in Ring Oscillator

Although the expressions obtained in the section for the rms and dc value of the ISF can be used to calculate the phase noise, it is desirable to express phase noise and jitter in terms of design parameters such as power dissipation and frequency. In this section, several expressions for the phase noise and jitter of different types of ring oscillators are derived in terms of such parameters.

This section, it is assumed that the symmetry criteria for minimizing Γ_{dc}(and hence the upconversion of *1/f* noise) are already met and that the jitter and phase noise of the oscillator are dominated by white noise. For CMOS transistor, the drain current noise spectral density is given by [18].

$$\frac{\overline{i_n^2}}{\Delta f} = 4kT\gamma g_{do} = 4kT\gamma u C_{ox} \frac{W}{L} \Delta V \tag{3.20}$$

Where g_{do} is the zero bias drain-source conductances, u is the mobility, C_{ox} is the gate oxide capacitance per unit area, *W* and *L* are the channel width and length, and ΔV is the gate voltage overdrive. The coefficient γ is 2/3 for long channel

devices in the saturation region and typically 2-3 times greater for short-channel devices [18] [19]. Equation (3.20) is valid in both short and long channel regimes, as long as an appropriate value for γ is used.

3.6.1 Single-Ended CMOS Ring Oscillator

The first case considered is a single-ended CMOS ring oscillator with equal-length NMOS and PMOS transistors. Assuming $V_{TN}=V_{TP}$, the maximum total channel noise from the NMOS and PMOS devices, when both the input and output are at *VDD/2*, is given by

$$\frac{\overline{i_n^2}}{\Delta f} = \left(\frac{\overline{i_n^2}}{\Delta f}\right)_N + \left(\frac{\overline{i_n^2}}{\Delta f}\right)_P = 4kT\gamma u_{eff} C_{ox} \frac{W_{eff}}{L} \Delta V \qquad (3.21)$$

Where

$$W_{eff} = W_n + W_p \qquad (3.22)$$

And

$$u_{eff} = \frac{u_n W_n + u_p W_P}{W_n + W_p} \qquad (3.23)$$

And ΔV is the overdrive in the middle of the transition, *i.e.*, $\Delta V = (V_{DD}/2)-V_T$.

During one period, each node is charged to q_{max} and then discharged to zero. In an N-stage single-ended ring oscillator, the power dissipation associated with this process is $Nq_{max}V_{DD}f_o$. However, during the transitions, some extra current, known as crowbar, is drawn from the supply. This current does not contribute to ground through both transistors. These two components of the total current drawn from supply are shown in Fig. 3.16. In a symmetric ring oscillator, these two components are comparable and their difference will depend on the ratio of the rise time to stage delay: therefore, total power dissipation is approximately given by

$$P = 2\eta N V_{DD} q_{max} f_o \qquad (3.24)$$

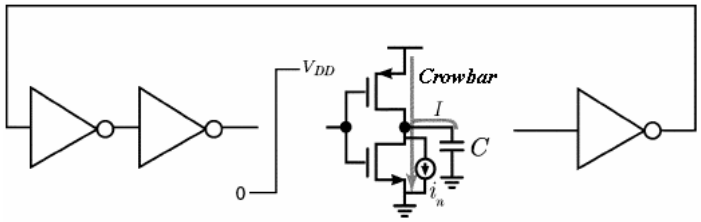


Fig. 3.16 Capacitor and crowbar current in an inverter

Assuming $u_nW_n=u_pW_p$ to make the waveforms symmetric to first order, the frequency of oscillation for long channel devices can be approximated by

$$fo = \frac{1}{2 N t_D} = \frac{1}{\eta N (t_r + t_f)} \approx \frac{u_{eff} W_{eff} C_{ox} \Delta V^2}{8 \eta N L q_{max}} \tag{3.25}$$

$$L\{\Delta w\} = 10 \log \left(\frac{\Gamma_{rms}^2}{q_{max}^2} \cdot \frac{\overline{i_n^2} / \Delta f}{2 \cdot \Delta w^2} \right) \tag{3.26}$$

$$\Gamma_{rms} \approx \sqrt{\frac{2\pi^2}{3\eta^3}} \cdot \frac{1}{N^{1.5}} \tag{3.27}$$

Where t_D is the delay of each stage and t_r and t_f are the rise and fall time associated with the maximum slope during a transition.

Assuming that the thermal noise source of the different devices are uncorrelated, and assuming that the waveform (and hence the ISF) of all the node are the same except for a phase shift, the total phase noise due to all *N* noise sources is *N* times the value given by (3.26). This equation gives the phase noise spectrum of an arbitrary oscillator in the *1/f²* region of the phase noise spectrum and will be referred to frequently. Note the absence of any fitting parameter. Taking only these inevitable noise sources into account, (3.26), (3.27), (3.21), (3.24) and (3.25) result in the following expressions for phase noise and jitter:

$$L\{\Delta w\} \approx \frac{8}{3\eta} \cdot \frac{kT}{P} \cdot \frac{V_{DD}}{V_{char}} \cdot \frac{w_o^2}{\Delta w^2} \tag{3.28}$$

$$\kappa \approx \sqrt{\frac{8}{3\eta}} \cdot \sqrt{\frac{kT}{P} \cdot \frac{V_{DD}}{V_{char}}} \tag{3.29}$$

Where κ is a proportionality constant determined by circuit parameters and V_{char} is the characteristic voltage of device. For long channel devices $V_{char}=\triangle V/\gamma$. Any extra disturbance, such as substrate and supply noise, or noise contributed by extra circuitry or asymmetry in the waveform, will result in a large number than (3.28) and (3.29). Note that lowering threshold voltages reduces the phase noise and could be exploited to improve the phase noise. Therefore, the minimum achievable phase noise and jitter for single-ended CMOS ring oscillator, assuming all symmetry criteria are met, occur for zero threshold voltage:

$$L\{\Delta w\} > \frac{16\gamma}{3\eta} \cdot \frac{kT}{P} \cdot \frac{w_o^2}{\Delta w^2} \tag{3.30}$$

$$\kappa > \sqrt{\frac{16\gamma}{3\eta}} \cdot \sqrt{\frac{kT}{P}} \tag{3.31}$$

As can be seen, the minimum phase noise is inversely proportional to the power dissipation and grows quardratically with the oscillation frequency. Further, note the lack of dependence on the number of stages (for a given power dissipation and oscillation frequency). Evidently, the increase in the number of noise source (and in the maximum power due to the higher transition currents required to run at the same frequency) essentially cancels the effect of decreasing Γ_{rms} as N increases, leading to no net dependence of phase noise on N. This somewhat surprising result may explain the confusion that exists regarding the optimum N since there is not a strong dependence on the number of stages for single-ended CMOS ring oscillators.

A similar calculation for the short channel case can be carried out. For such devices, the drain current may be expressed as:

$$I_D = \frac{u C_{ox}}{2} W E_c \Delta V \tag{3.32}$$

Where E_c is the critical electrical field. Combining (3.20) with (3.32), the following expression for the drain current noise of a MOS device in short channel is

obtained:

$$\frac{\overline{i_n^2}}{\Delta f} = 8kT\ \frac{\gamma I_D}{E_C L} \tag{3.33}$$

The frequency of oscillation can be approximately by:

$$f_o = \frac{1}{2NT_D} = \frac{1}{\eta N (t_r + t_f)} \approx \frac{u_{eff} W_{eff} C_{ox} \Delta V^2}{8\eta N L q_{max}} \tag{3.34}$$

Using (3.33), the same expressions for phase noise and jitter as given by (3.28) and (3.29) are obtained, except for a new V_{char}:

$$V_{char} = \frac{E_c L}{\gamma} \tag{3.35}$$

This results in a larger phase noise and jitter than the long channel case by a factor of $\gamma\Delta V/E_cL$.

3.6.2 Differential CMOS Ring Oscillators

Now consider a differential MOS ring oscillator with resistive load. The total power dissipation is:

$$P = N I_{tail} V_{DD} \tag{3.36}$$

Where N is number of stages, I_{tail} is the tail bias current of the differential pair, and V_{DD} is the supply voltage. The frequency of oscillator can be approximated by:

$$f_o = \frac{1}{2NT_D} \approx \frac{1}{2\eta N t_r} \approx \frac{I_{tail}}{2\eta N q_{max}} \tag{3.37}$$

The ISF (impulse sensitivity function) associated with the tail current source has a fundamental frequency which is double the oscillation frequency. This doubling is expected since the tail node is pulled up every time each one of the differential NMOS transistors turns on and thus the tail node moves at twice the frequency of the differential voltage.

Due to this frequency doubling, the c_1 coefficient for the tail ISF is zero and therefore the noise of the tail current source in the vicinity of w_0 has no effect on the

differential noise current. However, even-order coefficients such as c_2 are significant, and therefore noise components around even harmonics of w_0 have a significant effect on the phase noise, as shown in Figure 3.17.

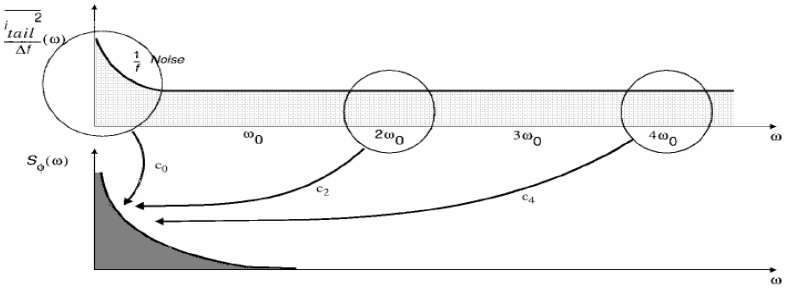


Fig. 3.17 Evolution of tail noise current

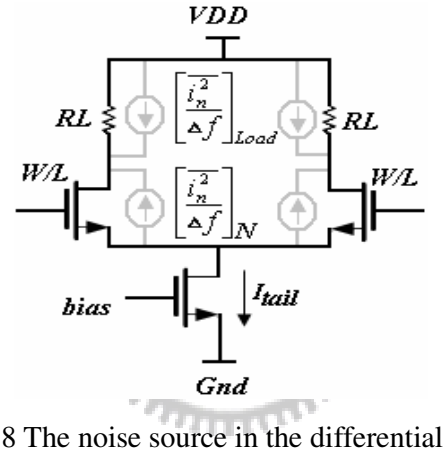


Fig. 3.18 The noise source in the differential buffer stage

Therefore, only the noise of the differential transistors and the load is taken into account, as shown in Figure 3.18. Total current noise on each single-ended node is given by:

$$\frac{\overline{i_n^2}}{\Delta f} = \left(\frac{\overline{i_n^2}}{\Delta f}\right)_N + \left(\frac{\overline{i_n^2}}{\Delta f}\right)_{Load} = 4kTI_{tail}\left(\frac{1}{V_{char}} + \frac{1}{R_L I_{tail}}\right) \quad (3.38)$$

Where R_L is the load resistor, $V_{char} = (V_{GS}-V_T)/\gamma$ for a balanced stage in the long channel limit and $V_{char} = E_c L/\gamma$ in the short channel regime. Assuming zero correlation among the various noise sources, the phase and jitter due to all *2N* noise sources is *2N* times. Using (3.39), the expression for the phase noise of the differential MOS ring oscillator is Equation 3.40. κ is given by Equation 3.41.

$$\Gamma_{rms} \approx \sqrt{\frac{2\pi^2}{3\eta^3}} \cdot \frac{1}{N^{1.5}} \tag{3.39}$$

$$L\{\Delta w\} \approx \frac{8}{3\eta} \cdot N \cdot \frac{kT}{P} \cdot \left(\frac{V_{DD}}{V_{char}} + \frac{V_{DD}}{R_L I_{tail}} \right) \cdot \frac{w_0^2}{\Delta w^2} \tag{3.40}$$

$$f_o = \frac{1}{2Nt_D} \approx \frac{1}{2\eta N t_r} \approx \frac{I_{tail}}{2\eta N q_{max}} \tag{3.41}$$

Chapter 4

Spur-reduction Frequency Synthesizers for DTV and WIMAX Applications

4.1 Introduction

In this chapter, a proposed architecture of synthesizer with spur-reduction techniques is introduced. Section 4.2 introduces some design considerations such as tuning range, and reference spur for this work. Sections 4.3 describe in detail the proposed architecture where dynamic switch cap, random charge and select band to reduce reference spur. Section 4.4 describes building blocks of our circuit and circuit-level simulation using HSPICE will be done in section 4.4.

4.2 Motivation

DTV and WIMAX (mobile) are the new specification for communication reception. The DTV require a very wide-range and high-purity local signal for the front-end to demodulate the received signal. The WIMAX (mobile) requires high-purity local signal and best phase noise for the front end to demodulate the received signal. This several important design-considerations are discussed in detail as following.

4.2.1 Tuning range

In this work, the America specification is utilized. Considering the specification for the America area, the operational band for DTV is 1270~2080 MHz, tuning range. Furthermore, to tolerate the process variation, we need design an oscillator with an even large tuning-range than specification, which may lead to a tuning range. The large operating range nevertheless implies a high VCO gain (K_{vco}) would increase the sensitivity of the PLL and noise in the control line so that undesired large reference spurs will be generated. The operational band for WIMAX (mobile) is 2500~2700 MHz, tuning range. To achieve both the large tuning and stringent phase noise by DTV and WIMAX (mobile).

4.2.2 Reference spur

Reference spur is also an important design issue of frequency synthesizer. The reference spurs at the PLL-based frequency synthesizer output are generated by the periodic ripples on the control line of voltage-controlled oscillators. The magnitude of the reference spurs can be approximately by narrow-band FM and is determined by the VCO gain (K_{vco}), the amplitude of ripples on the control line (Am), and the reference frequency (F_{ref}), as demonstrated by the following relation between spur amplitude (A_{spur}) and carrier amplitude ($A_{carrier}$) [20]:

$$\frac{A_{spur}}{A_{carrier}} = \frac{1}{2} \times \frac{K_{vco} \times A_m}{2\pi f_{ref}} \tag{4.1}$$

From the equation above, it is evident that reducing both K_{vco} and A_m, or increasing F_{ref} can minimize the reference spur. But K_{vco} is restricted to the tuning range of specification as described above. And F_{ref} is usually not a design variable in a conventional integer-N based PLL because it is determined by system specification and PLL architecture. Consequence, we may focus on reducing Am to reduce reference spur.

First, we may need to understand how the spur generates. The generation of spur is explanted in Figure 4.1 [21] [22]. When there is mismatch between the up and down currents in the charge pump, static phase error will be generated to maintain the loop remained locked. Thus, a ripple is generated on control line which is proportional to the extent of current mismatch. This is depicted in Figure 4.1(a). Besides, if there is any mismatch between the up and down signal paths, despite the perfect match for the values of charge pump currents, a ripple is generated responding to the timing mismatch. This is illustrated in Figure 4.1(b).

Typical synthesizers employ large capacitors in the loop filter to suppress the *Am.* This is an effective method but change the value of the loop filter means to change the loop characteristics. Also, some trade-offs exist between the loop bandwidth, setting time and phase noise, etc. Thus, we proposed a new concept to reduce the ripples on control line of VCO effectively without changing the loop characteristics significantly.

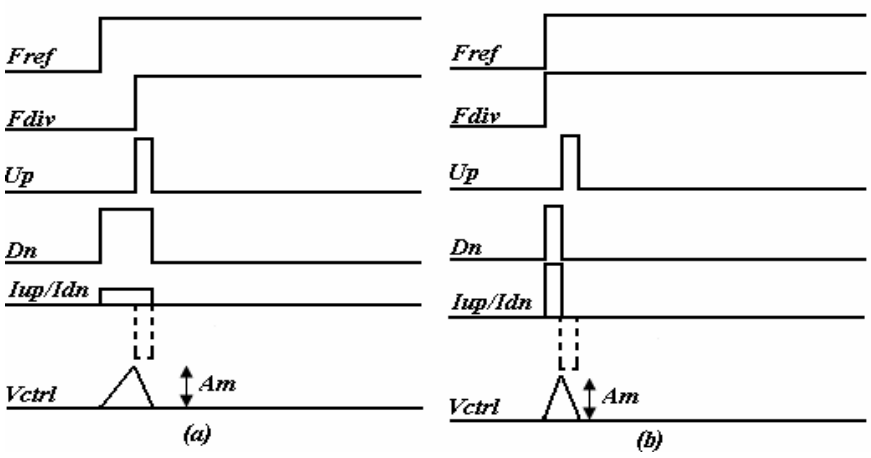


Fig. 4.1 Spur generation concept (a) Charge pump currents mismatch

(b) Up & Dn signal timing mismatch

Nevertheless, nonzero current flows through the loop filter due to the Up/Dn current source mismatch, different arrival time and pulse width, and hence, charges

or discharges the capacitor periodically, exhibiting ripples on the control line. The ripples on the control line modulate the oscillation frequency of the VCO, generating sidebands around the carrier.

4.3 Proposed System Architecture

In this section, the system structure is introduced first. Following that spur-reduction controlling concept is illustrated and HSPICE simulation will be depicted also.

4.3.1 Synthesizer architecture

The design issue described requires a low phase noise, wide tuning range, and low spur for DTV and WIMAX (mobile) system. The high-performance RF frequency synthesizer are often required: (1) to have smooth transition among channel intervals; (2) to have low phase noise and frequency variation; (3) to work over a wide frequency range which can cover the desired range; (4) to have an integrated loop filter on the chip. In the previous chapters we discussed system level design issues of a frequency synthesizer. Based on the knowledge, we will implement a three-order ΣΔ frequency synthesizer for DTV and WIMAX broadband RF tuner. The DTV synthesizer provided a 36MHz input reference signal and several bits digital codes, the circuit can generate a frequency tuning range from 1.27 to 2.08 GHz with 6 MHz channel bandwidth. The WIMAX (mobile) synthesizer provided a 25MHz input reference signal and several bits digital codes, the circuit can generate a frequency tuning range from 2.5GHz to 2.7 GHz with 5 MHz channel bandwidth. The DTV such large tuning range, transfer gain of the VCO (*Kvco*) must be as large as 675MHz/volts with 1.8V power supply in 0.18-um process. Therefore, tuning range is achieved by a combination of continuous analog voltage control and digital, 4bits switching turn on. By this method, the transfer gain

can be reduced to less than 70.2MHz/V~321MHz/V at most and trade-off between phase noise and tuning range can be solved.

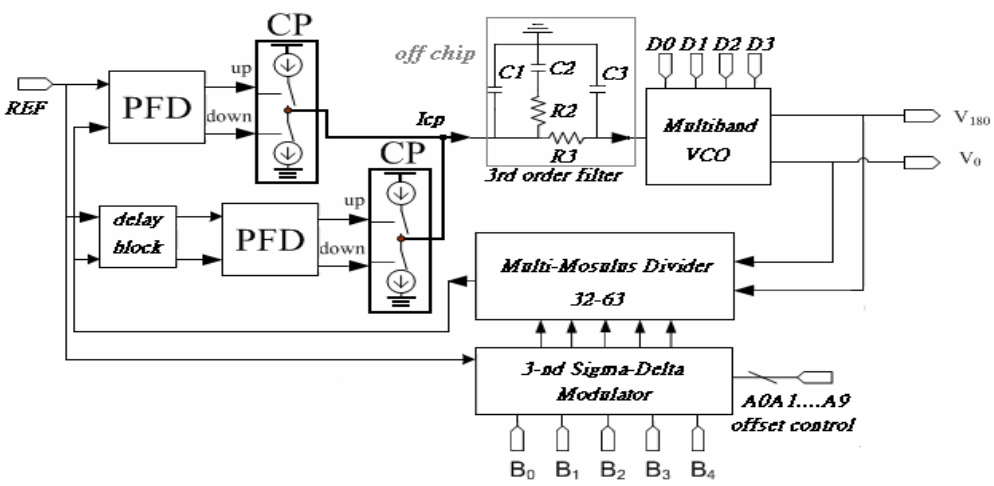


Fig. 4.2 The architecture of DTV based on three-order $\Sigma\Delta$ modulator

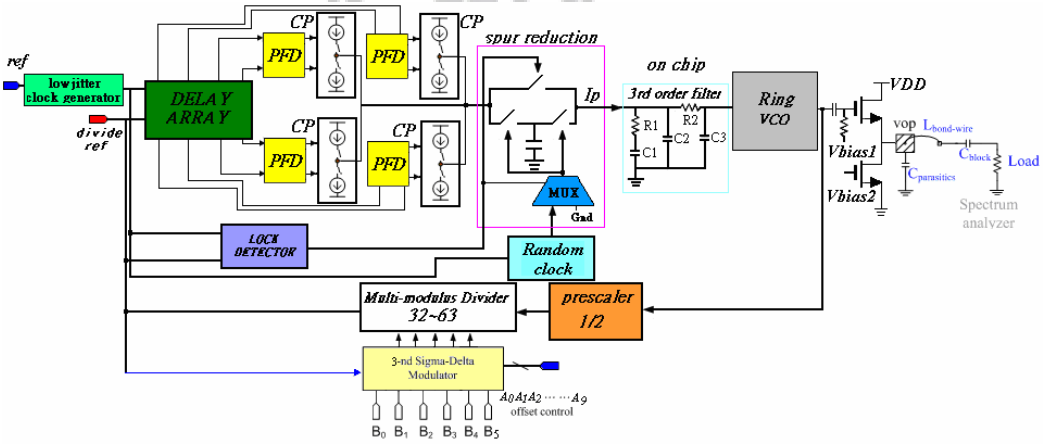


Fig. 4.3 The first architecture of WIMAX (mobile) based on

Three-order $\Sigma\Delta$ modulator

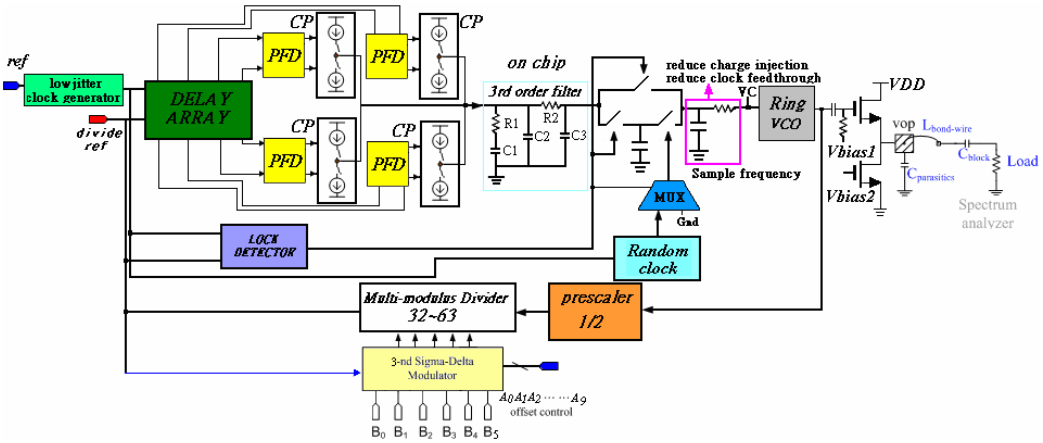


Fig. 4.4 The second architecture of WIMAX (mobile) based on

Three-order $\Sigma\Delta$ modulator

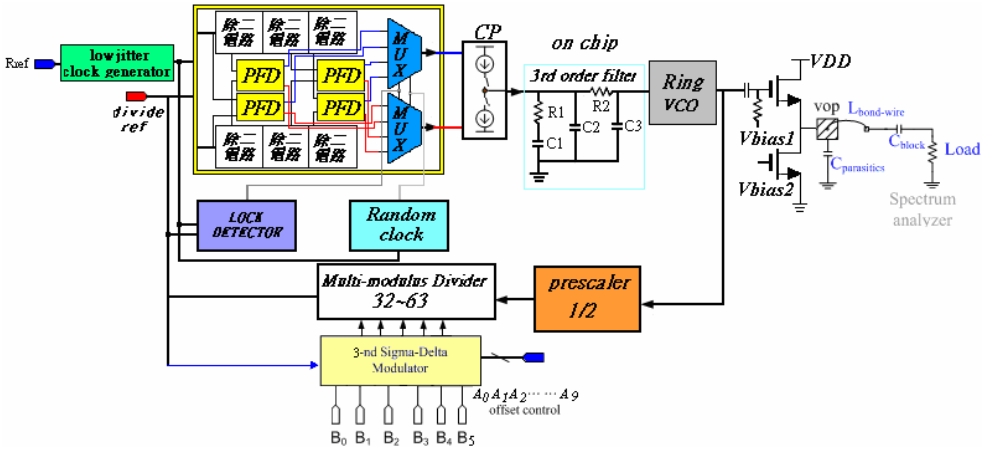


Fig. 4.5 The third architecture of WIMAX (mobile) based on

Three-order $\Sigma\Delta$ modulator

4.3.2 Spur-reduction control

Reviewing the spur generation described in 4.2.2, mismatch of charge pump currents and timing skew in the up and down signals lead to the periodical ripples of the control line of VCO. Many publications have made much effort on reducing the amplitude of ripples, such as charge pump calibration [23], chopping of signal paths. However, no matter how large the current mismatch and timing skew are the loop can be remained locked if and only if the charge conservation is hold. In other words, to sustain the locked state of loop, a static phase error proportional to the mismatch

is generated between the reference clock and the output programmable divide. Therefore, if we can "skip" the ripples generated by charge pump and sample clean voltage, we could see a "relative smooth" voltage on loop filter. What we can random the ripple of the charge pump generated. This concept leads to the idea of using dynamic switch cap; random charge and select band reduce the K_{VCO} of the PLL synthesizers.

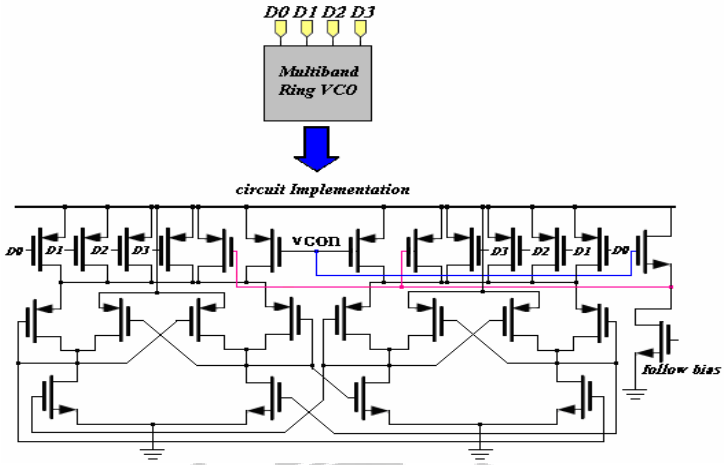


Fig. 4.6 Reduce K_{vco} circuit implementation

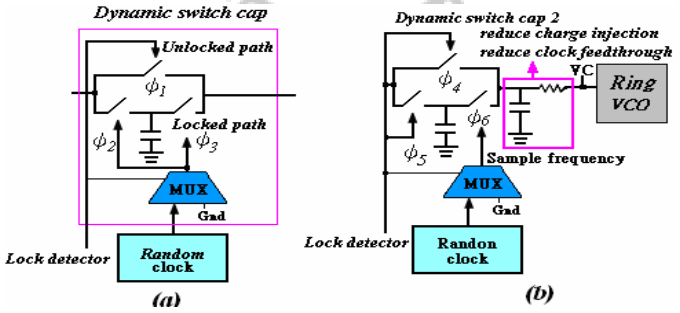


Fig. 4.7 The dynamic switch cap circuit implementation

This concept leads to the idea of using the dynamic switch cap circuit in Fig. 4.7. From Fig 4.7(a) Compared to linking charge pump circuit and loop filter directly, we break the linking path with two switches and one capacitor inserted between the two blocks. From Fig 4.7 (b) to link loop filter and VCO directly, we break the link path with two switches, two capacitors and one resistance inserted. As shown in Fig 4.7, the switches are divided into two sets that operate differentially. In

the propose structure, switching of the current path and voltage sample are used to facilitate the transient response. When judgment signal of lock detector is unlocked, $\overline{LD}$ is high while $\varphi 3$, $\varphi 5$ and $\varphi 6$ are low. In this state, the loop behaves like conventional PLL structure, i.e. charge pump circuit connects to loop filter directly and loop filter connects to VCO directly. Once lock detector recognizes the loop is locked, *LD* is low while $\varphi 1$ and $\varphi 4$ are low, $\varphi 2$=randomb *and* $\varphi 3$= random, $\varphi 5$=high *and* $\varphi 6$= random. In fact, random clock generates periodical pattern which its periodic $2^k - 1$ times of period of the original clock, which k is the number of bits length of random clock generator. Thus a periodic of 7*TCLK and 7 bits random clock generates a signal with a period of 127*TCLK. Hence, there would be a fundamental frequency, which is $\frac{F_{clk}}{2^k - 1}$, appears on the spectrum. Also, the randomness of reference spur is proportional to the number of bits. Therefore, 7-bits random clock generator provides a lower reference spur level and a relative "smooth" spectrum. Circuit analysis is done later to give some concepts of choosing the number of bits. As shown in Fig. 4.8 we use *LD* and random clock generator are generating the random charge to charge pump, which can randomness of reference spur. From Fig. 4.8 we can reduce reference spur and no external circuit in voltage control line, that voltage control line is sensitivity. We provide a low reference spur level and reduce voltage control line external noise that can relative smooth spectrums.

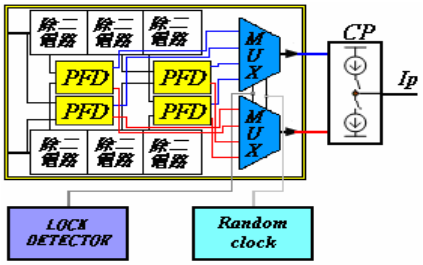


Fig. 4.8 Dynamic charge circuit implementation

4.3.3 Circuit analysis

The ripples on control voltage of VCO denoting as g(t), are modeled as narrow, rectangular pulses having a width $\triangle T$ and a height $\triangle V$, as shown in Fig.4.9[24]. V1 is the dc value of control voltage and the periodic of ripples are mTref which equals to the period of the decomposing random clock generator signal.

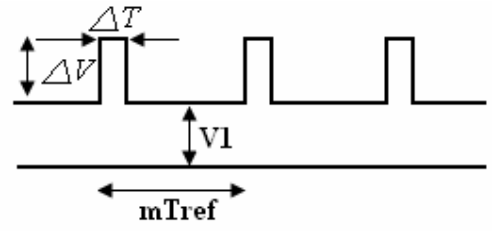


Fig. 4.9 Simplified model for disturbance on control line

By making the assumptions above, we can express the output of VCO as:

$$V_{out}(t) = V_0 \cos\left[w_{FR} t + K_{vco} \int g(t)\,dt + K_{VCO} \int V_1\,dt \right] \quad (4.2)$$

The Fourier series expansion of g (t) is given by

$$g(t) = \frac{\triangle V \triangle t}{m\,Tref} + \sum_{n \neq 0} a_n \cos\left(n \frac{w_{REF}}{m} t + \theta_n \right) \quad (4.3)$$

Where the first term represents the dc component and can be merged with V1.

Inserting Equation (4.2) into (4.3), we can approximate Vout (t) as:

$$\begin{aligned} V_{out}(t) \simeq\ & V_0 \cos\left(w_{FR} + K_{vco} \frac{\triangle V \triangle t}{T_{REF}} + K_{vco} V_1 \right) t \\ & - K_{vco} \left[V_0 \sum_{n \neq 0} \frac{m\,a_n}{n\,w_{REF}} \sin\left(n \frac{w_{REF}}{m} t + \theta_n \right) \right] \\ & \times \sin\left(w_{FR} + K_{vco} \frac{\triangle V \triangle t}{T_{ref}} + K_{vco} V_1 \right) t \end{aligned} \quad (4.4)$$

Considering sidebands at $\pm w_{REF}$ only which means n=m in Equation (4.4), Vout (t) can be expressed as:

$$V_{out}(t) = V_0 \cos(w_0 t) - K_{vco}\left[V_0 \times \frac{a_m}{w_{ref}} \sin(w_{ref} t + \theta_n)\right] \times \sin(w_0 t) \quad where \quad w_0 = w_{FR} + K_{vco}\frac{\Delta V \Delta t}{T_{REF}} + K_{vco} V_1 \tag{4.5}$$

The Fourier coefficients of g (t) denoted as a_m can be expressed as:

$$\begin{aligned} a_m &= \frac{1}{m T_{REF}} \int_{m T_{REF}} g(t) \cos(m \frac{w_{REF}}{m} t) dt \\ &= \frac{1}{m T_{REF}} \int_0^{\Delta T} \Delta V \cos(w_{REF} t) dt \\ &= \frac{1}{m T_{REF}} \times \frac{\Delta V}{w_{REF}} \times \sin(w_{REF} t)\Big|_0^{\Delta t} = \frac{k_0}{m} \\ where \quad k_0 &= \frac{\Delta V}{2\pi} \sin(w_{REF} t)\Big|_0^{\Delta t} \end{aligned} \tag{4.6}$$

Let us consider our proposed circuit first. Fig 4.10 illustrates the normal periodic ripples and those disturbed by random clock. We can know if random clock generates a "1", a pulse is generated aligned with the original one. And if random clock generates a "0", it means the pulse will deviate from the original one 1/2Tref. In other word, 0 and 1 of random clock outputs represent different delay the position of ripples.

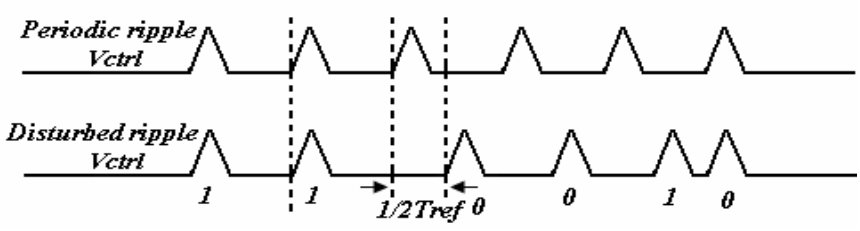


Fig. 4.10 Illustration of Random clock disturbance

4.3.4 Sampling Switches

An important attribute of the switch, in CMOS, is that under DC conditions the gate of the MOSFET does not draw a current. Therefore, neglecting capacitances from the gate to the drain/source, we find that the gate control signal does not interfere with information being passed through the switch. Figure 4.11 shows

fundamental component of any dynamic circuit is the switch. Figure 4.12 shows the small-signal resistance of the switch of Figure 4.11 plotted against input voltage. The benefits of using the CMOS transmission gate are seen from the figure, namely overall resistance. Another benefit of using the CMOS TG is that it can pass a logic high or logic low without a threshold voltage drop. The largest voltage that an NMOS switch can pass is *VDD- V_{THN}*, while the lowest voltage a PMOS switch can pass is V_{THP}.

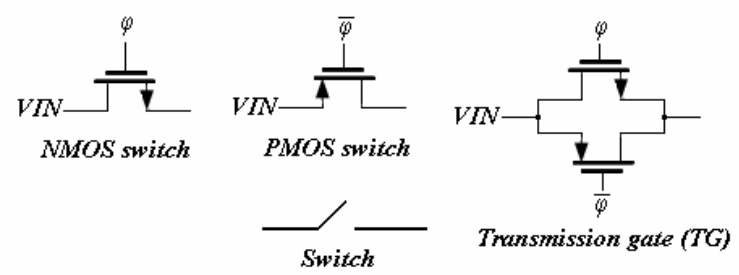


Fig. 4.11 MOSFETs used as switch

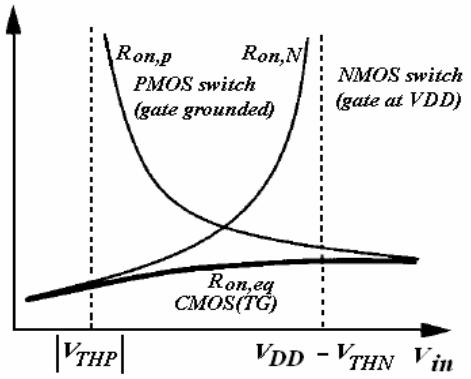


Fig. 4.12 Small-signal on resistance of MOSFET switches

While MOS switches may offer substantial benefits, they are not without some detraction. Two nonideal effects typically associated with these switches may ultimately limit the use of MOS switches in some application. These two effects are known as *charge injection* and *clock feedthrough*.

Charge injection can be understood with the Fig. 4.13. When the MOSFET switch is on and VDS is small, the charge under the gate oxide resulting from the

inverted channel is Q'_{ch}. When the MOSFET turns off, this charge is injected onto the capacitor and into V_{in}. Because V_{in} is assumed to be a low-impedance, source-driven node, the injected charge has effect on this node. However, the charge injected onto C_{load} results in a change in voltage across it. However, the fact the input voltage is connected to C_{load} through the channel resistance makes this error unimportant (the voltage across C_{load} charges to V_{in} through the MOSFET's channel resistance).

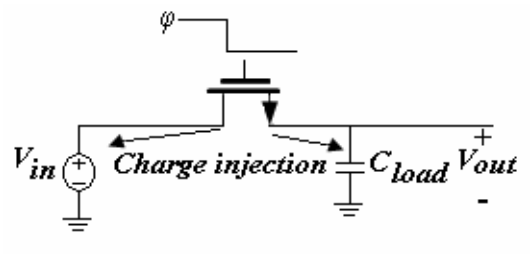


Fig. 4.13 Simple configuration using an NMOS switches to how charge injection

In Fig. 4.14 the schematic of the NMOS switch representation clock feedthrough. Here the capacitances between the gate/drain and gate/source of the MOSFET are modeled with the assumption that the MOSFET is operating in the triode region. When the gate clock signal, ϕ, goes high, the clock signal feeds through the gate/drain and gate/source capacitances. However, as the switch turns on, the input signal, V_{in}, is connected to the load capacitor through the NMOS switch. The result is that C_{load} is charged to V_{in} and the capacitive feedthrough has no effect on the final value of V_{out}. However, now consider what happens when the clock signal makes the transition low, that is, the n-channel MOSFET turn off. A capacitive voltage divider exists between the gate-drain (source) capacitance and the load capacitance. As a result, a portion of the clock signal, ϕ,appears across as:

$$\Delta V_{load} = \frac{C_{overlap} \cdot VDD}{C_{overlap} + C_{load}} \tag{4.7}$$

Where $C_{overlap}$ is the overlap capacitance value, and LD is the length of the gate

that overlaps the drain/source.

$$C_{overlap} = C_{ox}' \cdot W \cdot LD \tag{4.8}$$

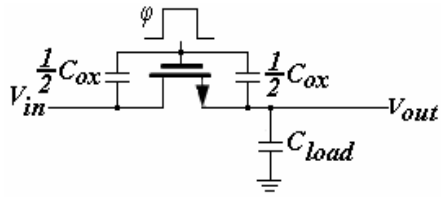


Fig. 4.14 Illustration of capacitive feedthrough

Many methods have been reported that reduce the effects of charge injection and clock feedthrough. One of the most widely used is the dummy switch, as seen in Fig. 4.15. Here, a switch, M2, with its drain and source shorted is placed in series with the desired switch M1. Notice that the clock signal controlling the dummy switch is the complement of the signal controlling M1, and in addition, should also be slightly delayed.

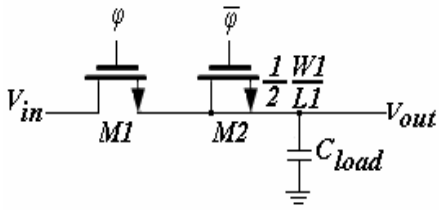


Fig. 4.15 Dummy switch circuit used to minimize charge injection

When M1 turns off, half of the channel charge is injected toward the dummy switch, this explaining why the size of M2 is one-half that of M1. Although M2 is effectively shorted, a channel can still be induced by applying a voltage on the gate. Therefore, the charge injected by M1 is essentially matched by the charge induced by M2, and the overall charge injection is canceled. Note what happens when M2 turns off. It will inject half of its charge in both directions. However, because the drain and source are shorted and M1 is on, all of the charge from M2 will be injected into the low-impedance, voltage-driven source, which is also charging C_{load}. Therefore, M2's charge injection will not affect the value of voltage on C_{load}.

Another method for counteracting charge injection and clock feedthrough is to replace the switch with a CMOS transmission gate (TG) in Fig. 4.16. This results in low changes in V_{out} because the complementary signals that are used will act to cancel each other. However, this approach requires precise control on the complementary clocks (the clocks must be switched at exactly the same time) and assumes that the input signal, V_{out}, is small since the symmetry of the turn-on and turn-off waveforms depend on the input signal.

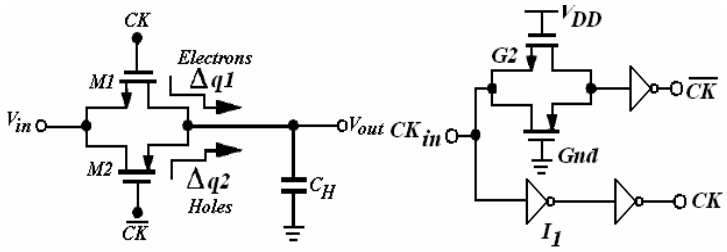


Fig. 4.16 Use of complementary switches to reduce charge injection

4.4 Building Blocks

In this section, Low jitter clock generator, Phase-frequency detector (PFD), Charge Pump (CP), Voltage control oscillator (VCO), Random clock generator, lock detector (LD), Programmable Frequency Divider, Prescaler, loop filter and three-order sigma-delta would be introduced and transistor-level simulation to prove their function.

4.4.1 Low jitter clock generator, PFD, CP

This clock needs to have sufficiently low jitter in order not to increase the VCO output noise floor due to non-shaped jitter noise. Some design strategies are adopted to minimize clock jitter due to device and supply noise. Figure 4.17 shows the simplified circuit to generate the low jitter clock. To reduce common mode noise probably coupled to the testing board and to obtain the least amount of clock jitter from the external clock source. It is critical to use as few clock driver stages as

possible to generate the low jitter clock with sufficient driving capability because any extra stages generate extra device noise, hence larger clock jitter. To reduce the supply noise, a dedicated and clean supply is used solely for the low jitter clock generation circuit. Fig. 4.18 simulates its operation situation

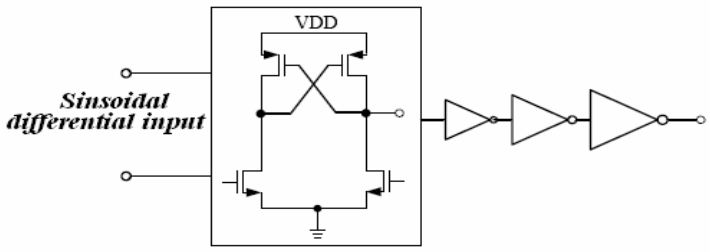


Fig. 4.17 Low jitter on-chip clock generator

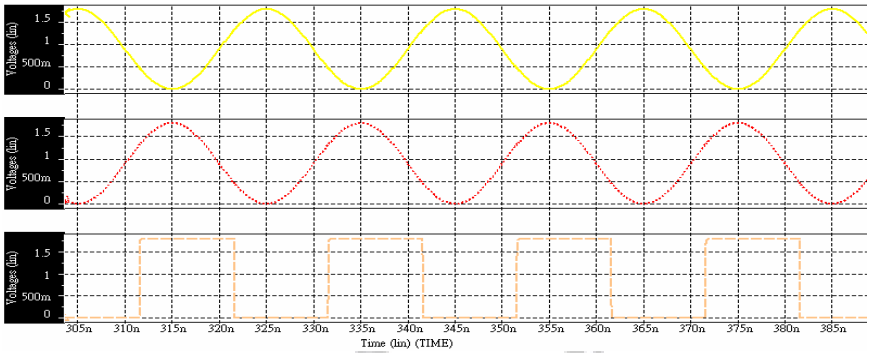


Fig. 4.18 Low jitter clock generator simulation

A common drawback for some phase frequency detector is a dead zone in the phase characteristic at the equilibrium point. The dead zone generates phase jitter because the control system does not change the control voltage when the phase error is within the dead zone. This influence can be improved by increasing the precision of the PFD. To reduce the dead zone and to overcome the speed limitation, we choose the dynamic phase frequency detector shown in Fig. 4.19 [25]. Compared with the conventional PFD, the transistor numbers are decreased to 12 and thus possesses smaller parasitic inherently. According to the phase difference between both input signals, UP is used to increase and DN is used to decrease the frequency of the output signal. Fig. 4.20 simulates its operation situation.

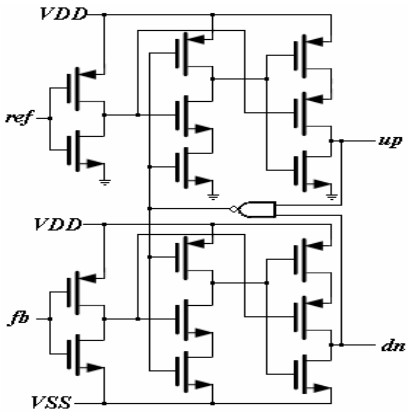


Fig. 4.19 Phase frequency detector

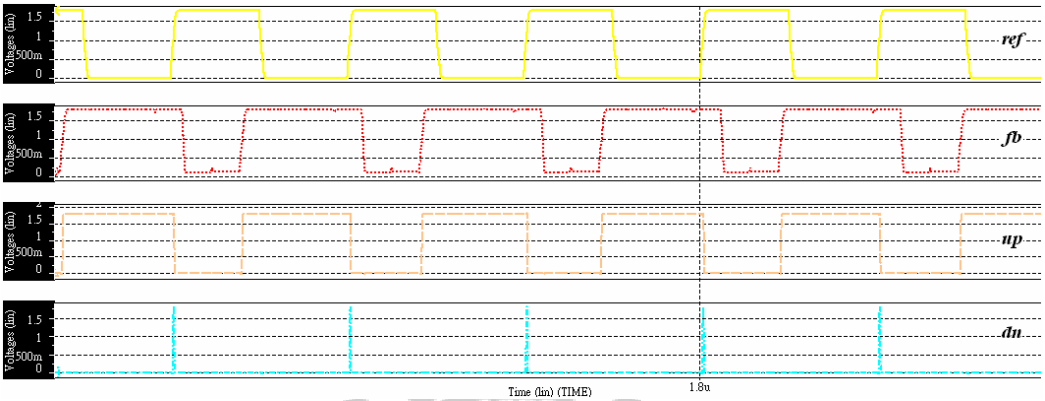


Fig. 4.20 The time diagram of the PFD

The implementation of a charge pump is illustrated in Fig. 4.21. The switch-at-gate charge pump has more stable output voltage than the switch-at-drain charge pump because it eliminates charge sharing and clock feed-through errors and thus reduces output voltage jitter. Although it may suffer from reviewed switching speed due to the large parasitic capacitance at the gate, we design the current flow such that it eliminates the parasitic charge. Cascade NMOS and PMOS are design to reduce channel length modulation. The current mismatch of the charge pump in the PLL generates a phase offset which increases spurs in the PLL output signals. When the current mismatch occurs in the charge pump, the amount of the phase offset is given by:

$$\Phi_{\varepsilon} = 2\pi \frac{\Delta t_{on}}{T_{ref}} \frac{\Delta_i}{I_{cp}}$$

$$P_r = 20\log\left[\frac{\sqrt{2}\left(I_{cp} R / 2\pi\right)\Phi_{\varepsilon} K_{vco}}{2 f_{ref}}\right] - 20\log\frac{f_{ref}}{f_{pl}} \tag{4.9}$$

where Φ_{ε}, Δ_{ton}, T_{ref}, I_{cp} and Δ_i are the phase offset, the turn-on time of the PFD, the reference clock period, the charge pump current, and the current mismatch of the charge pump, R is the resistor value in the loop filter, Kvco is the VCO gain, f_{ref} is the reference frequency for the PFD and f_{pl} is the frequency of the pole in the loop filter respectively. Pr is the amount of reference spur. The Fig. 4.21 shows a charge pump circuit and charge pump current match. The Fig. 4.22 shows PFD and charge pump Dead zone. The Fig. 4.23 shows output voltage range of charge pump

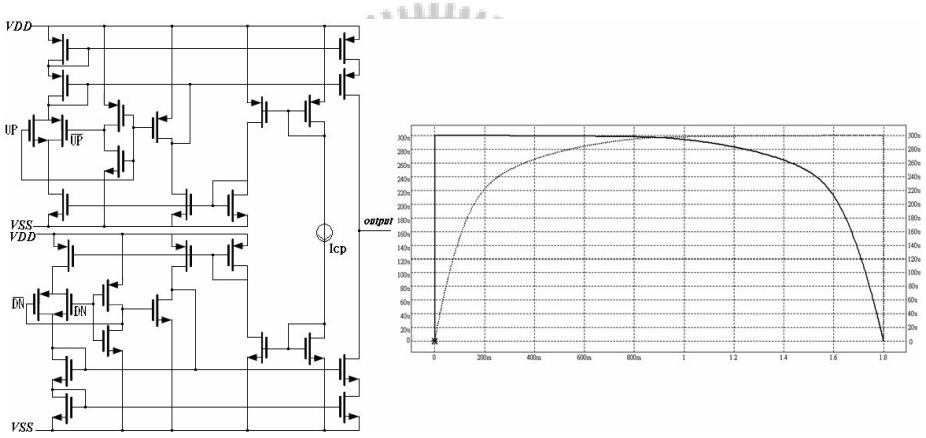


Fig. 4.21 The charge pumps circuit and simulation

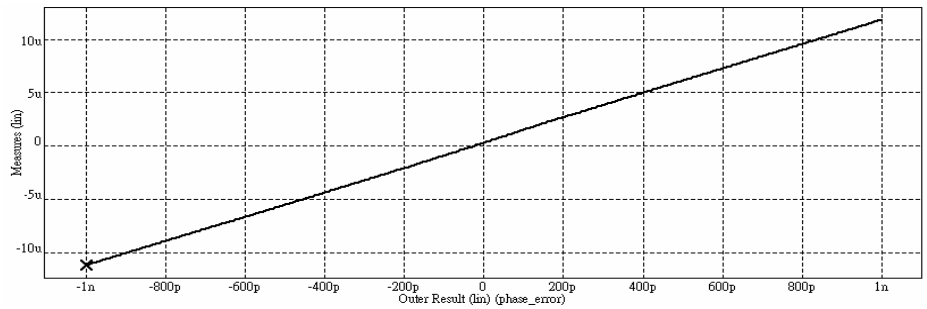


Fig. 4.22 Dead zone simulation of PFD with CP

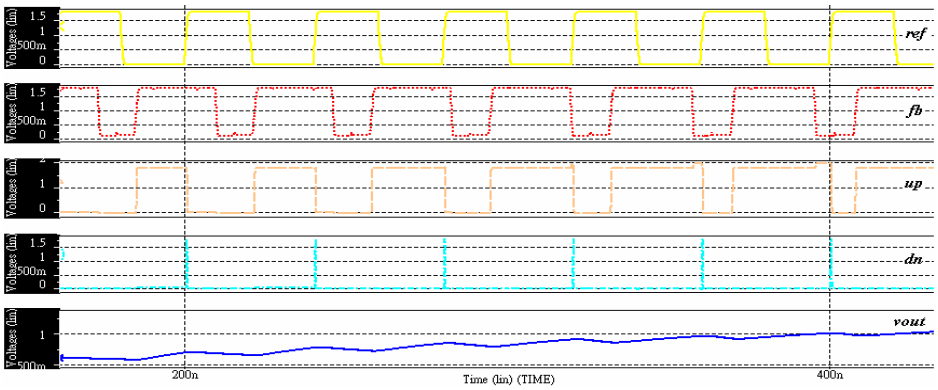


Fig. 4.23 The output voltage range of charge pump

4.4.2 Voltage control oscillator (Ring VCO)

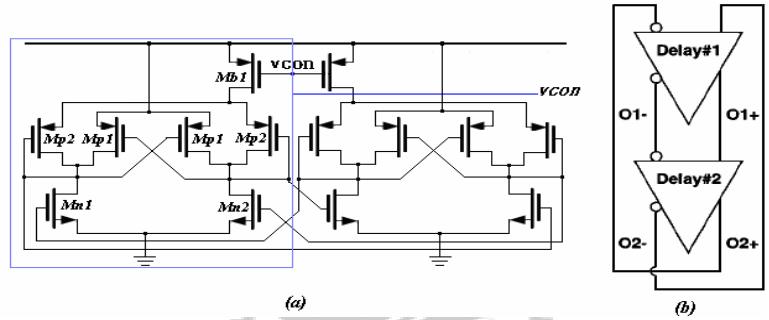


Fig. 4.24 Circuit implementation of the propose (a) delay cell (b) ring oscillator

The circuit schematics of the proposed delay cell and the whole ring oscillator are shown in Fig. 4.24. The delay cell consist of one NMOS input pair (Mn1), one PMOS positive feedback pair (Mp1) for maintaining oscillator, one diode-connected PMOS (Mp2), and one PMOS transistor (Mb1) for frequency tuning. The ring oscillator consists of two delay cells for power-consumption and phase-noise minimization. The design guidelines that determine the delay-cell design are as follows.

A. High-Frequency Operation:

An NMOS input pair is used to maximize the transconductance-tocapacitance (gm=C) ratio to achieve high operating frequency with low power dissipation. To reduce the gm requirement and thus power dissipation, only parasitic capacitors of devices are utilized. Moreover, only two delay cells are included in the oscillator to

minimize the power consumption.

B. Wide Frequency-Tuning Range

A large tuning range is required to overcome the problem of process variation. The operating frequency of a ring oscillator can be tuned by variable capacitor (varactor) or by variable load impedance. A varactor is typically implemented by p-n-junction, and therefore frequency-tuning range is limited to be within 10~ 20%. In this design, frequency tuning is achieved by tuning the transconductance (gm) of the diode-connected PMOS devices Mp2. By controlling the current of Mb1, gm of Mp2 can be adjusted from zero to a value close to gm of Mp1. Therefore, over 50% tuning range can be easily achieved.

C. Low Phase-Noise Performance

As phase noise is defined as the difference between carrier power and noise power, phase-noise performance can be improved by either increasing carrier power or reducing noise power. In the proposed design, the source nodes of devicesMp1 are directly connected to supply to eliminate current limitation of the output nodes and thus maximize output amplitude. Since output amplitude becomes large, transistors are turned off periodically. As shown in Fig. 4.25, noise current nn1, np1, np2 is zero when output amplitude is large. The carrier power is increased and the noise power is reduced simultaneously, and as a result, the phase-noise performance is improved [26].

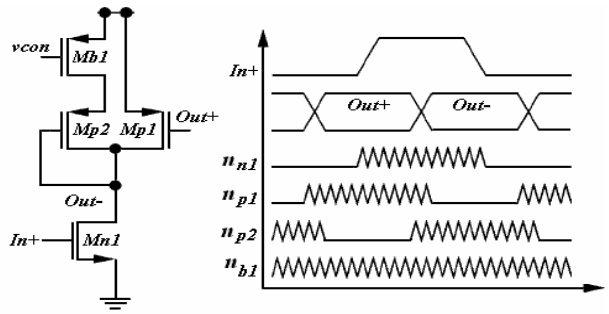


Fig. 4.25 Delay cell waveforms and thermal noise current

For DTV system the VCO designs: In Fig. 4.26, the VCO design for the DTV system and Fig. 4.27, the simulation for HSPICE. The Fig. 4.26 (b) we add source follow extended frequency [27].

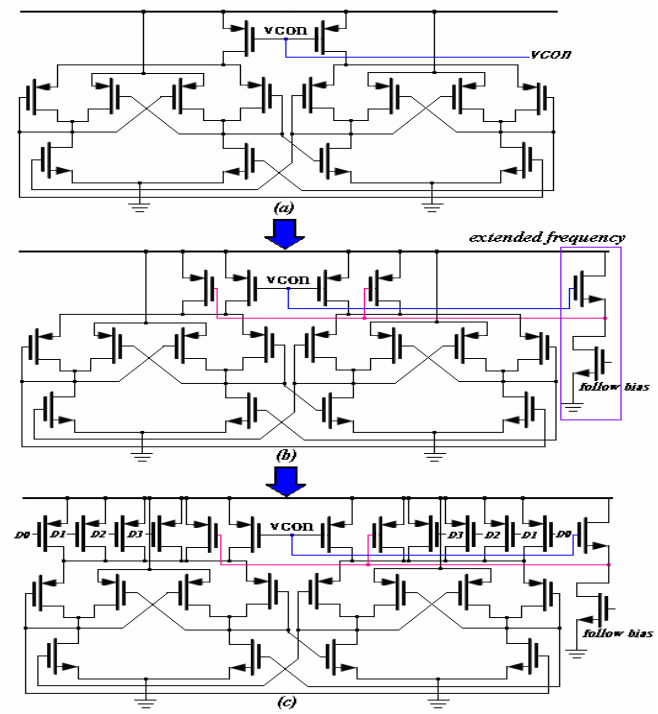


Fig. 4.26 The VCO design for the DTV system

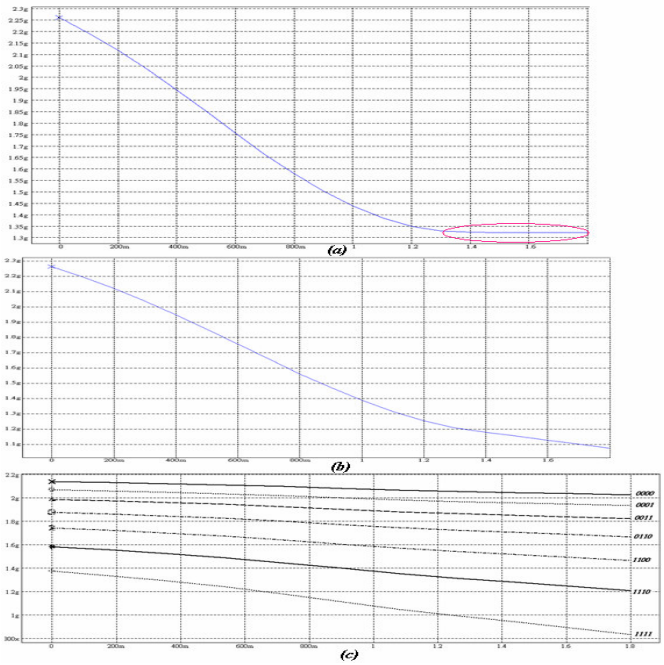


Fig. 4.27 The VCO simulation for HSPICE

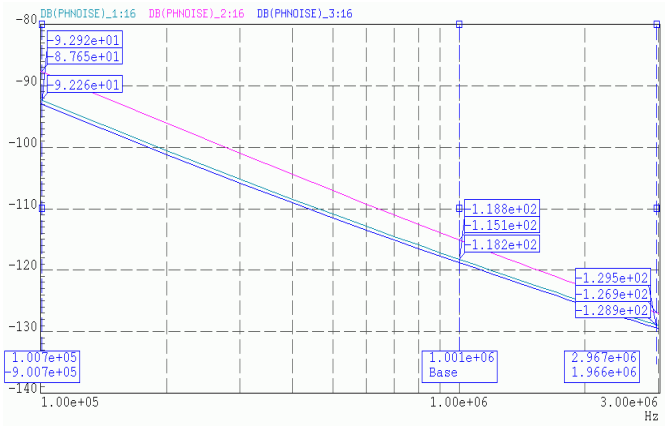


Fig. 4.28 Phase noise of the VCO

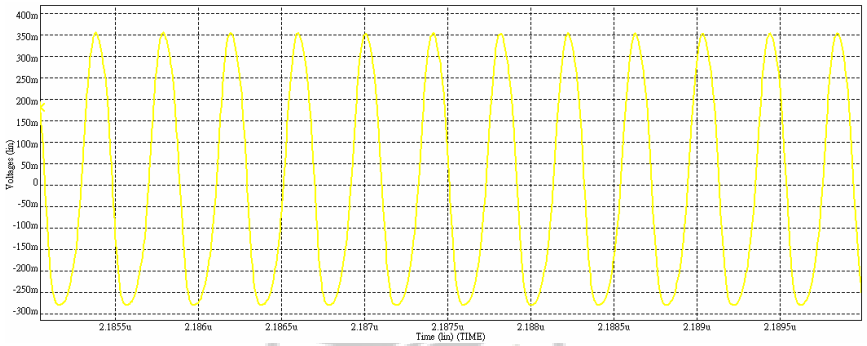


Fig. 4.29 The output swing with the PAD effect

TABLE 4-1 Process corners simulation (DTV)

Process Corners	TT	FF	FS	SS	SF
Frequency(GHz) Band: (0000)	2.06~2.17	2.11~2.24	2.08~2.19	2.03~2.14	2.06~2.18
Frequency(GHz) Band: (0001)	1.96~2.10	2.02~2.17	2.00~2.13	1.93~2.06	1.95~2.10
Frequency(GHz) Band: (0011)	1.85~2.01	1.90~2.08	1.90~2.05	1.82~1.97	1.81~2.0
Frequency(GHz) Band: (0110)	1.69~1.90	1.74~1.98	1.77~1.96	1.66~1.86	1.63~1.87
Frequency(GHz) Band: (1100)	1.49~1.77	1.53~1.84	1.60~1.84	1.46~1.72	1.38~1.71
Frequency(GHz) Band: (1110)	1.22~1.61	1.26~1.69	1.40~1.71	1.22~1.55	1.07~1.52
Frequency(GHz) Band: (1111)	0.843~1.39	0.869~1.48	1.10~1.54	0.836~1.34	0.634~1.26

TABLE 4-2 Process corners simulation (DTV):

Process Corners	TT	FF	FS	SS	SF
Frequency(GHz)	0.843~2.17	0.869~2.24	0.84~2.16	0.836~2.14	0.634~2.18

In Fig. 4.28, shows its phase noise performance. Fig. 4.29 shows the out swing is approach 650mV considering the PAD effect. Finally, we simulate the VCO tuning range in the different corner conditions shown in the Table 4-1 and Table 4-2.

For WIMAX (mobile) system, the VCO tuning range in Fig. 4.30. We simulate the VCO tuning range in the different corner conditions shown in the Table 4-3.

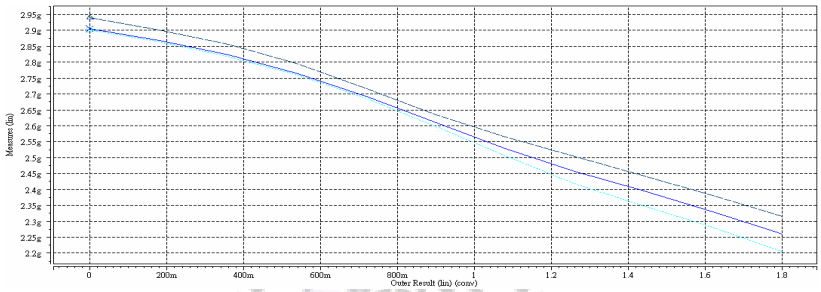


Fig. 4.30 The VCO tuning range (corner case: TT, FF, SS)

TABLE 4-3 Process corners simulation (WIMAX mobile):

Process Corners	TT	FF	SS
Frequency(GHz)	2.25~2.9	2.32~2.95	2.2~2.87

4.4.3 Programmable Frequency Divide, Prescaler, Loop filter

Programmable dividers have to operate at the highest VCO frequency. Therefore, the choice of the divider architecture is essential for achieving low power dissipation and high design flexibility. Fig. 4.31 depicts the programmable frequency divider. These feedback lines enable simple optimization of power dissipation. Another advantage is that the topology of the different cells in the divider is the same, therefore facilitating layout work.

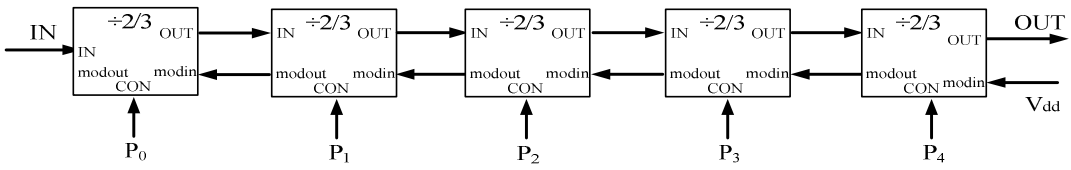


Fig. 4.31 The architecture of programmable frequency divider

The programmable divider can provide an output signal with a period of:

$$T_{out} = \left(2^5 + p_4 \cdot 2^4 + p_3 \cdot 2^3 + p_2 \cdot 2^2 + p_1 \cdot 2^1 + p_0\right) \times T_{in} \qquad (4.10)$$

Therefore, this equation shows that the division ratios from 32 (if all p_n=0) to 63 (if all p_n=1) is achieved. The circuit of the 2/3 divider is shown in Fig. 4.32 (a). The logic functions of the 2/3 cells are implemented with the Source Coupled Logic (SCL) structure presented in Fig. 4.32 (b). The logic tree combines a latch function with an AND gate [28].

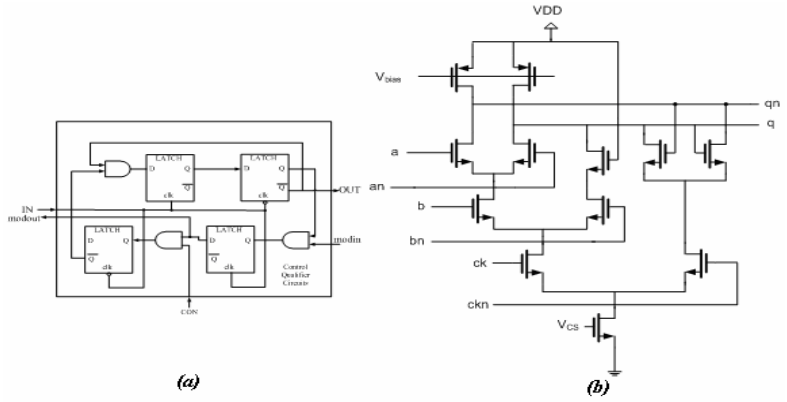


Fig. 4.32 (a)Functional blocks and logic implementation of a 2/3 divider cell

(b)SCL implementation of an AND gate combined with a latch function

Because of the oscillatory frequency of the VCO is very high, we first employ a prescaler to decrease the input clock frequency of the following multi-modulus divider. Fig. 4.33(a) shows the block diagram of common 1/2 frequency divider using two D-latches in a master-slave configuration with negative feedback. In high speed operation, it's usual practice to design the slave as the "dual of the master", such that they can be driven by a single clock [29]. Nevertheless, duality will make one of the latches uses PMOS devices in the signal path, lowering the maximum operation speed. Razavi proposed a divider utilizing two identical D-latches, driving by complementary clocks [30], as illustrated in Fig. 4.33(b). The transmission gate in the non-inverted phase is to minimize the skew between CK and $\overline{CK}$.

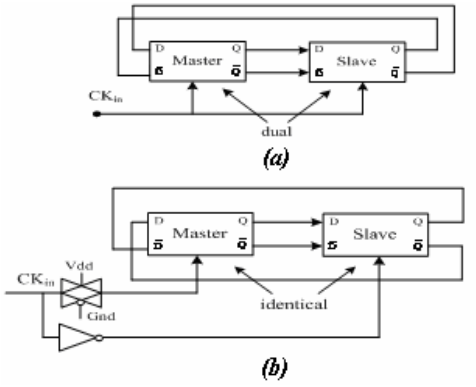


Fig. 4.33 Master-slave divider with (a) single clock (b) complementary clocks

Fig. 4.34 shows the high speed divider circuit [30]. Each latch comprises two sense devices (M1, M2, M7, M8), a regenerative loop (M3, M4, M9, M10), and two pull-up devices (M5, M6, M11, M12). When the CK is high, M5 and M6 are off, and the master is in the sense mode. In the same time, M11 and M12 are on, and the slave is in the store mode. When CK changes to low, the reverse occurs. In Fig 4.35 shows VCO, Prescaler and Programmable dividers are linked simulation in HSPICE.

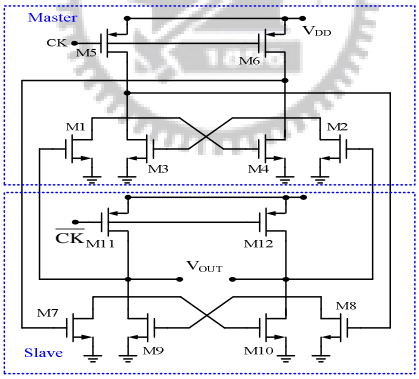


Fig. 4.34 High speed, low voltage frequency divider

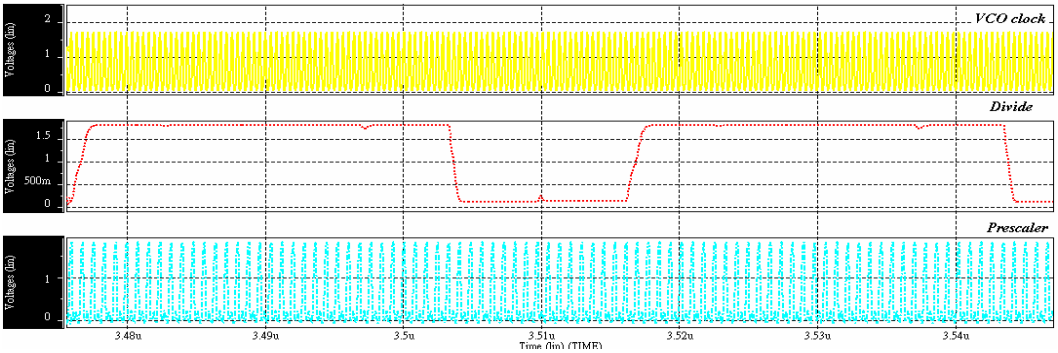


Fig. 4.35 VCO, Prescaler and Programmable dividers simulation

As we know, the loop filter mainly determines the noise and dynamic performance of the PLL. In order to effectively attenuate the reference spur, we adopt the 3rd order loop filter. To decide the proper values of each element, the basic steps are as follows:

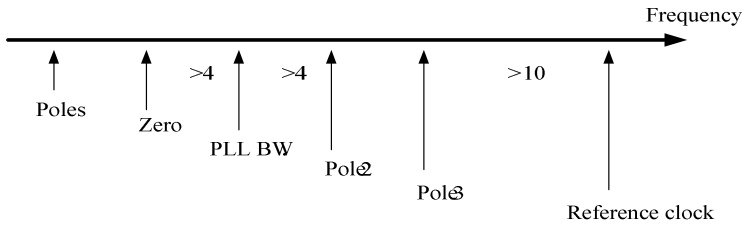


Fig. 4.36 Relationship between zero, poles, reference and loop bandwidth

1. As a rule, the relationship between zero, poles, and reference and loop bandwidth are shown in Fig. 4.36. Deciding the proper values of open-loop unity-gain bandwidth ω_P, phase margin ϕ and the added attenuation from the third pole.
2. Calculate the time constant T_1 and T_3. Then we can get the new unity-gain bandwidth ω_C due to the added third pole.

$$T_1 = \frac{\sec\phi_p - \tan\phi_p}{\omega_p} \tag{4.11}$$

$$T_3 = \frac{1}{\omega_3} = \sqrt{\frac{10^{(ATTEN/10)} - 1}{(2\pi F_{ref})^2}} \tag{4.12}$$

$$\omega_c = \frac{\tan\phi \cdot (T_1 + T_3)}{\left[(T_1 + T_3)^2 + T_1 T_3\right]} \times \left[\sqrt{1 + \frac{(T_1 + T_3)^2 + T_1 T_3}{\left[\tan\phi \cdot (T_1 + T_3)\right]^2}} - 1\right] \tag{4.13}$$

3. Calculate the time constant T_2.

$$T_2 = 1 \Big/ \left[\omega_c^2 (T1 + T3)\right] \tag{4.14}$$

4. Thus we can derive the value of each element.

$$C_1 = \frac{T_1}{T_2} \frac{K_{pd} K_{vco}}{\omega_c^2 N} \left[\frac{(1 + \omega_c^2 T_2^2)}{(1 + \omega_c^2 T_1^2)(1 + \omega_c^2 T_3^2)}\right]^{1/2} \tag{4.15}$$

$$C_2 = C_1\left(\frac{\omega_1}{\omega_2} - 1\right), \quad R_2 = \frac{1}{C_2\omega_2} \tag{4.16}$$

5. As rule of thumb chooses $C_3 \le C_1/10$, otherwise T_3 will interact with the primary poles of the filter.

$$C_3 = C_1/10, R_3 = T_3/C_3 \tag{4.17}$$

Fig. 4.37 shows bode plot of the open close transfer function of PLL. The result is as we expect. It proves the above equations are precise enough to estimate PLL parameters.

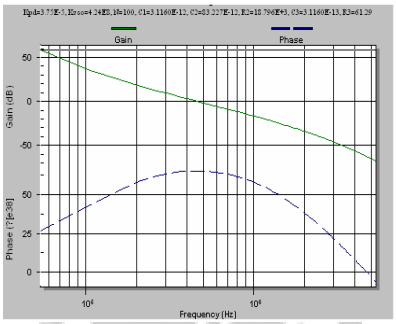


Fig. 4.37 Bode plot of close loop PLL

4.4.4 Lock detector (LD), Random clock generator

We need a lock detector to switch the current paths and the voltage paths to facilitate the transient behavior. The implementation of lock detector circuit is shown in Fig. 4.38. The concept is very simple: we use two DFFs for Ref and Clk to sample each other. Two delay lines, T and 2T specify the locking window to judge if the two inputs are closed enough. Fig. 4.39 shows the timing diagram for explanation. The first DFF uses CLK as its sampling clock and Ref, which is delayed by T, as input data. Therefore, if the Ref leads Clk by more than T, the transition edge of the delayed Ref will go up earlier than that of Clk and this DFF would output logic 0 for $\overline{Q}$. On the other hand, the second DFF adopts Clk, which is delayed by 2T, as sampling clock and Ref, which is delayed by T, as input data.

Hence, if the Ref lags Clk by more than T, logic 0 is generated in Q for the second DFF. After combining the outputs by the NAND gate, $\overline{LD}$ is low if the absolute value of phase difference for Ref and Clk is less than T and vice versa.

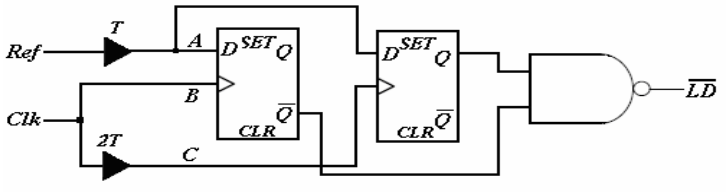


Fig. 4.38 Lock detector

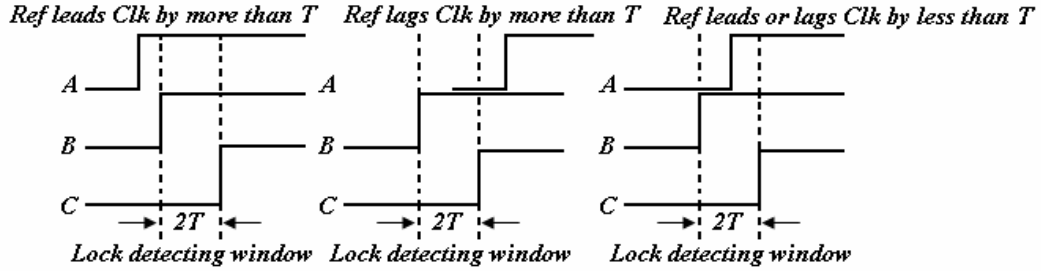


Fig. 4.39 Timing diagram of lock detector

This detecting strategy describe above is quite simple. But now can we determine the delay of locked windows? If we allocate a large value for T, it means the lock detector would send a message, "the loop is locked", to charge pump and spur-reduction control too early. If we chose T which is smaller than the static phase error, Ref and Clk never have chance to come closely enough and the lock detector always outputs an "unlocked" message to spur-reduction control. Therefore, by considering the trade-off describe above, T is set to about 1.18ns to ensure stability. Fig 4.40 shows the circuit architecture Random clock generator. It consists D flip-flops and one XOR logic. Fig 4.41 shows simulation in HSPICE.

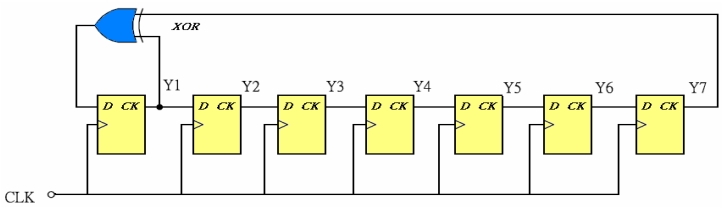


Fig. 4.40 Timing diagram of Random clock generator

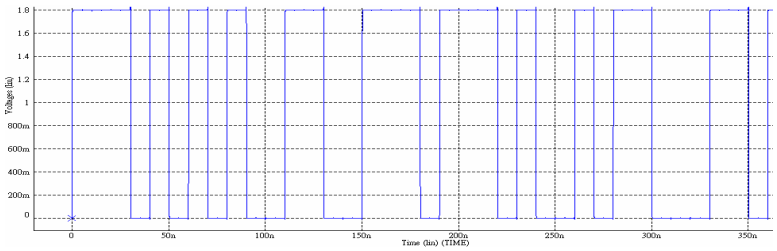


Fig. 4.41 Random clock generator simulation

4.4.5 Three-order Sigma-Delta Modulator

In the actual implementation, the limited precision of the accumulators result in the loss of accuracy and minimum frequency resolution synthesizer can achieve. In general, the higher dynamic range accumulator provides better tracking on the desired mean value but increases the power consumption and chip area. For the other consideration of frequency resolution, the required frequency resolution of the system. To achieve this requirement, the data length of DSM (dynamic range of accumulator) should be as:

$$\Delta f = \frac{f_{range}}{2^{L}} \leq system\ resolution \tag{4.18}$$

Where $\triangle f$ is the frequency resolution, f_{range} is the output frequency range (i.e. the product of reference frequency and division ratio of prescaler) and L is the data length of DSM. In this design, the reference frequency is 36MHz and 25MHz, the division ratio is 58 and 100 hence, the 10-bits of DSM are derived. Note that, the divide-by-2 prescaler causes a one-bit resolution loss. Therefore, the extra 1-bit should be added to data length of DSM for compensation. Then the frequency resolution can be revised as:

$$\Delta f = \frac{f_{ref} \times prescaler\ ratio}{2^{L-\log_2(prescaler\ ratio)}} \tag{4.19}$$

Finally, comprising the above two consideration, the 10-bits DSM is used in this design. The pipelined MASH 1-1-1 DSM is now depicted in Fig. 4.42. The detail of circuit design will be discussed in the following two parts.

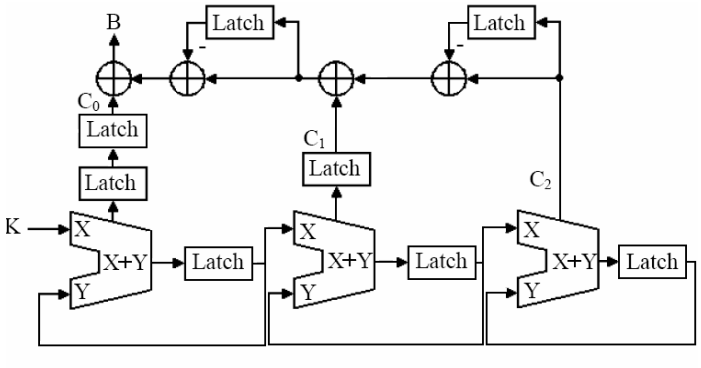


Fig. 4.42 Pipelined 3rd-order ΣΔ modulator

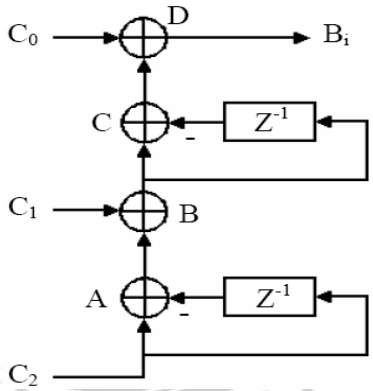


Fig. 4.43 Noise cancellation network of MASH 1-1-1 DSM

From Fig. 4.43, we can find if we design the circuit intuitively, two 4-bits adders (B, D) and two 4-bits two's complement adders (A, C) are needed. However, in order to simplify design, we analyze each adder's logic states and design the decoder for the noise cancellation network instead. First of all, the adder A has three states (-1, 0 and 1), as shown as Table 4-4:

TABLE 4-4 Noise cancellation Network coding (A)

C_2	C_2^{-1}	Decimal number	2's complement
0	0	0	000
0	1	-1	111
1	0	1	001
1	1	0	000

Observe the 2's complement table, we can find that the highest two bits are the same. So, we can simplify the out of adder A as

$$\text{Two MSB} = \overline{C_2} \times C_2^{-1} \tag{4.20}$$

$$\text{LSB} = C_2 \oplus C_2^{-1} \tag{4.21}$$

We check the adder B where C_1 is added to the output of adder A. Only three half-adders are used here and adder B's output is tabulated in Table 4-5. Next, we check the output of adder C in Fig. 4.43. The output of B and it's 2's complement value should be added in the last cycle operation. Output of adder B has only four states (001, 000, 111 and 010), and the 2's complement transformation is tabulated in Table 4-6.

TABLE 4-5 Noise cancellation Network coding (B)

C_2	C_2^{-1}	C_1	Decimal number	2's complement
0	0	0	0	000
0	1	0	-1	111
1	0	0	1	001
1	1	0	0	000
0	0	1	1	001
0	1	1	0	000
1	0	1	2	010
1	1	1	1	001

TABLE 4-6 Noise cancellation Network coding (C)

B's output	2's complement
001	111
000	000
111	001
010	110

With cautious supervision, the two MSB are the same and equal to the result of the two LSB of adder B's output to have XOR operation. And the LSB of 2's complement is equal to the LSB of adder B's output. Therefore, the 2's complement transformation with only one XOR gate and only three adders with one XOR gate are necessary in adder C. The output states of adder C are also tabulated in Table 4-7. Finally, the adder D can be decoded with a few logic gates. And the control signal

corresponding to DSM output is as shown in Table 4-8.

TABLE 4-7 Noise cancellation Network coding (D)

Decimal number	C's output
-3	101
-2	110
-1	111
0	000
1	001
2	010
3	011

TABLE 4-8 Noise cancellation Network coding (E)

DSM output (Decimal number)	Control signal (4-bits Binary)
-3	0001
-2	0010
-1	0011
0	0100
1	0101
2	0110
3	0111
4	1000

According to Table 4-7 and Table 4-8, an inverter is connected to the MSB of adder C's output and the resulting output transmitted with two LSB into a 3-bits adder. And the MSB of control signal is the carry output of the 3-bits adder. From the above analysis the total error cancellation circuit is demonstrated in Fig. 4.44.

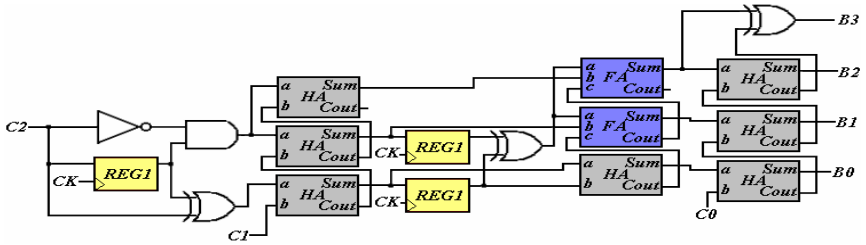


Fig. 4.44 Realization of the noise cancellation network

4.5 Fractional-N Frequency Synthesizer System

Fig. 4.2 shows architecture of DTV based on three-order *ΣΔ* modulator. Fig. 4.45 (a) shows the VCO control voltage. We can obviously find that the control voltage is stability. Fig. 4.45 (b) shows the carrier spectra, the reference spur about 65dbm.

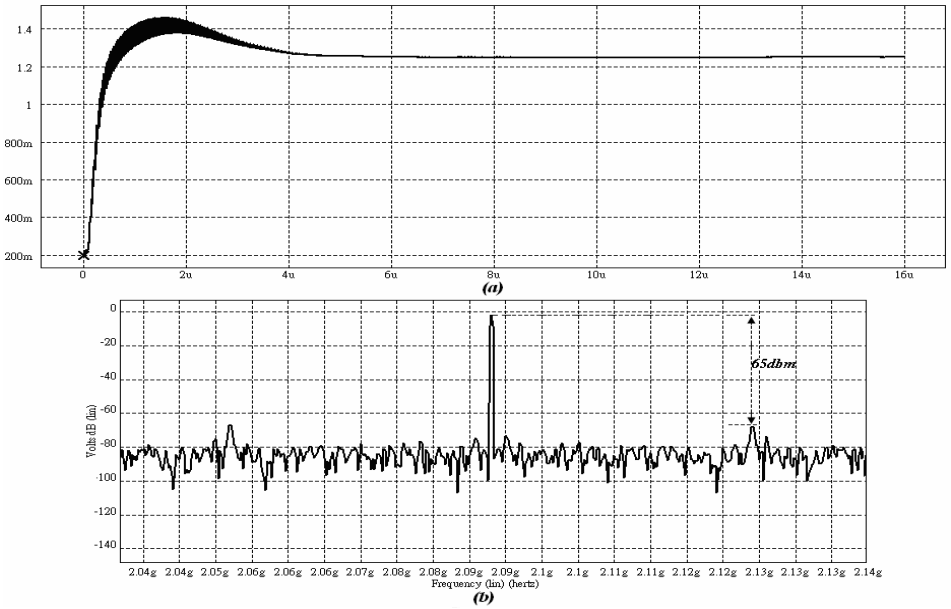


Fig. 4.45 (a) VCO control voltage and (b) Out Spectrum when LO is 2.088GHz

Fig. 4.3, Fig. 4.4 shows architecture of WIMAX (mobile) based on three-order ΣΔ modulator. Fig. 4.46 (a), Fig. 4.47 (a) shows the VCO control voltage. We can obviously find that the control voltage is stability. Fig. 4.46 (b), Fig. 4.47 (b) shows the carrier spectra, the reference spur about 71dbm, 70dbm.

The random charge PLL in Fig. 4.5 shows architecture of WIMAX (mobile) based on three-order ΣΔ modulator. Fig. 4.48 (a) shows the VCO control voltage. We can obviously find that the control voltage is stability. Fig. 4.48 (b) shows the carrier spectra, the reference spur about 80dbm.

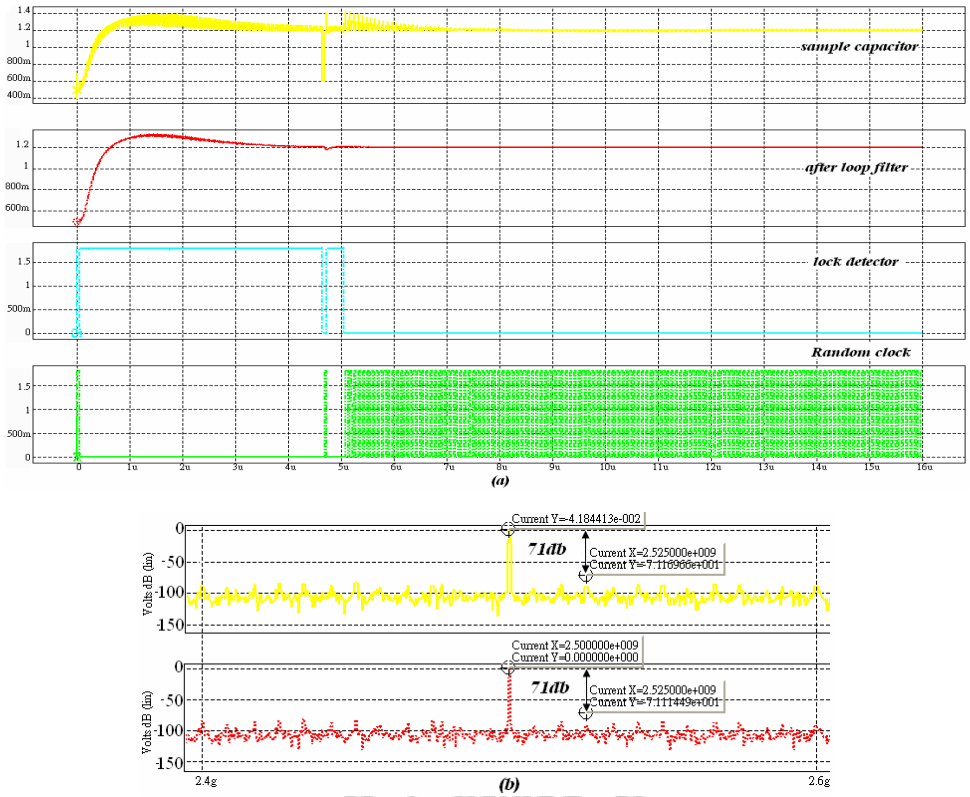


Fig. 4.46 (a) VCO control voltage, sample capacitor, lock detector and random clock (b) Out Spectrum is 2.5GHz

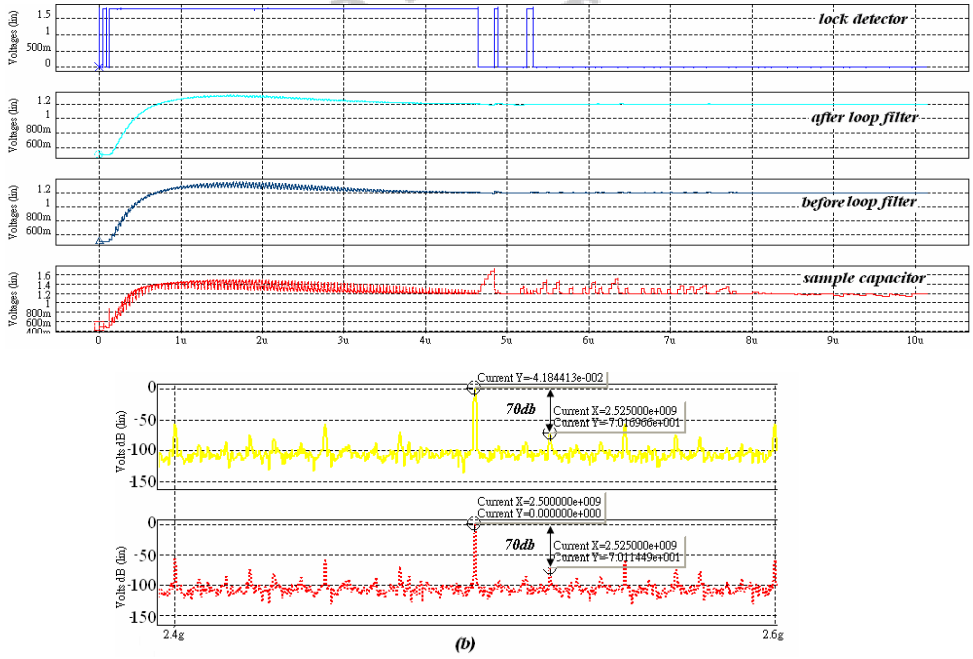


Fig. 4.47 (a) VCO control voltage, sample capacitor, lock detector and random clock (b) Out Spectrum is 2.5GHz

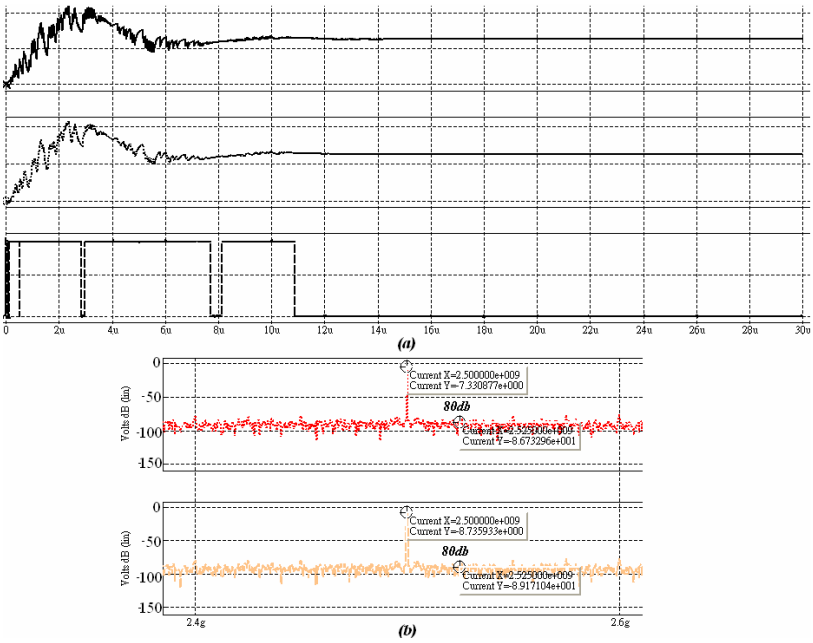


Fig. 4.48 (a) VCO control voltage and lock detector

(b) Out Spectrum is 2.5GHz

The closed-loop simulation results in Fig. 4.45, Fig. 4.46, Fig. 4.47 and Fig. 4.48, using HSPICE are done. The parameters and performance summaries of the frequency synthesizer are listed in Table 4-9.

TABLE 4-9 Fractional-N PLL performance summaries

Technology	TSMC 0.18-um 1P6M CMOS
Chip area	1.14mm × 1.14mm
Supply voltage	1.8V
Reference frequency	36 MHz
Output frequency	800MHz ~ 2.16GHz
VCO gain	70.26 MHz/V~324MHz/V
VCO output swing	700mV
Phase noise@1MHz offset	-112.1dBC/Hz
Phase margin	56 度
Loop bandwidth	450 kHz
Channel bandwidth	6 MHz
Setting time	< 6us
Maximum power consumption	約 33.9mW

DTV System Fig(4.2)

Technology	TSMC 0.18-um 1P6M CMOS
Chip area	1.200mm × 1.250mm
Supply voltage	1.8V
Reference frequency	25MHz
Output frequency	2.2GHz ~ 2.9GHz
VCO gain	431MHz / V
VCO output swing	800mV
Phase noise@1MHz offset	-118.1 dBC/Hz
Phase margin	65 度
Loop bandwidth	625kHz
Channel bandwidth	5MHz
Setting time	< 7us
Maximum power consumption	約 33 mW

WIMAX(mobile) Fig(4.3)

Technology	TSMC 0.18-um 1P6M CMOS
Chip area	1.055mm × 1.200mm
Supply voltage	1.8V
Reference frequency	25MHz
Output frequency	2.2GHz ~ 2.9GHz
VCO gain	431MHz / V
VCO output swing	800mV
Phase noise@1MHz offset	-118.1 dBC/Hz
Phase margin	65 度
Loop bandwidth	625kHz
Channel bandwidth	5MHz
Setting time	< 7us
Maximum power consumption	約 32 mW

WIMAX(mobile) Fig(4.4)

Technology	TSMC 0.18-um 1P6M CMOS
Chip area	1.200mm × 1.050mm
Supply voltage	1.8V
Reference frequency	25MHz
Output frequency	2.2GHz ~ 2.9GHz
VCO gain	431MHz / V
VCO output swing	800mV
Phase noise@1MHz offset	-118.1 dBC/Hz
Phase margin	70 度
Loop bandwidth	625kHz
Channel bandwidth	5MHz
Setting time	< 11us
Maximum power consumption	約 30 mW

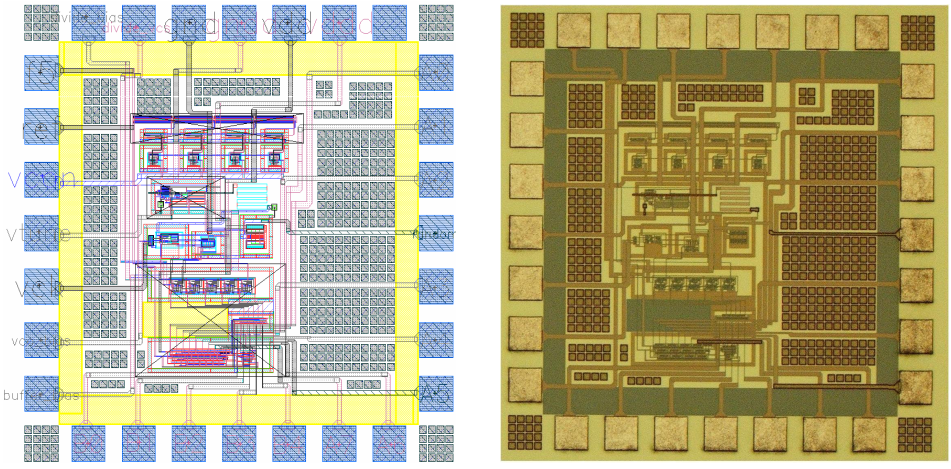
WIMAX(mobile) Fig(4.5)

Chapter 5

Testing Setup and Experimental Results

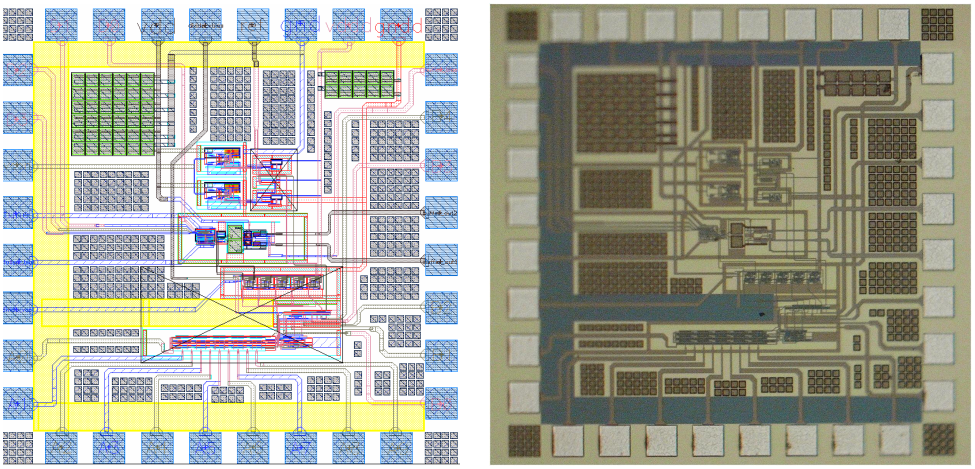
5.1 Experimental Results

The proposed ΣΔ frequency synthesizer has been fabricated in a 0.18-μm 1P6M mixed-signal technology. Shown in Fig. 5.1(a), 5.2(a) is the layout and 5.1(b), 5.2(b) is the die photo of the chip. This chip occupies an area of 1.027*1.026mm^2, 1.14 X 1.14mm^2. Shown in Fig. 5.3(a), Fig. 5.3(b), Fig. 5.3(c), is representation from Fig. 4.3, Fig. 4.4, and Fig. 4.5.



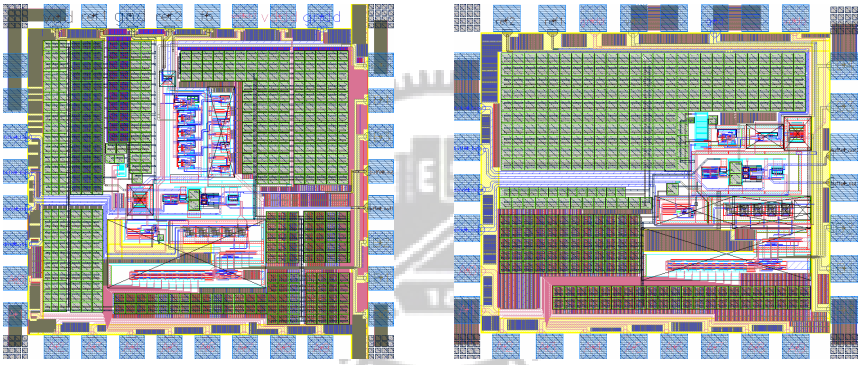
(a) (b)

Fig. 5.1 (a) Layout (b) Die photo

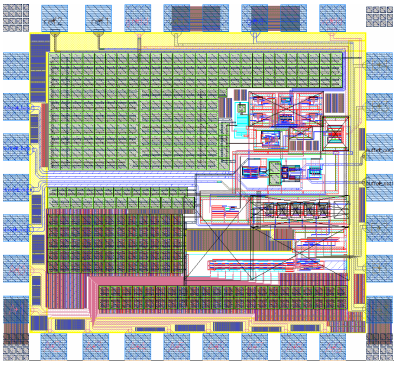


(a) (b)

Fig. 5.2 (a) Layout (b) Die photo



(a) (b)



(c)

Fig. 5.3 (a) Layout1 (b) Layout2 (c) Layout3

5.2 Test Setup

The fabricated synthesizer was tested to determine its performance. Measurement was performed with raw dies mounted on the PCB to prevent the parasitic effect of the package. Because the synthesizer is a mixed-mode system, we separate the powers and grounds of digital and analog parts. Then, we connect the ground of analog part and that of digital part with an inductor. The inductor shorts the DC voltage of the digital and analog grounds, while preventing the high-frequency noise in the digital circuit from coupling to the analog circuit by their grounds.

The analog and digital powers are generated by LM317 adjustable regulators as shown in Figure 5.4. The regulator circuit is easy to use and the output voltage could be predicted by equation (5.1)

$$V_{OUT} = 1.25\left(1 + R_1 / R_2\right) + I_{ADJ} \cdot R_2 \qquad (5.1)$$

The I_{ADJ} is the DC current that flows out of the ADJ terminal of the regulator. Besides, the capacitors C_1 and C_2 are the bypass capacitors.

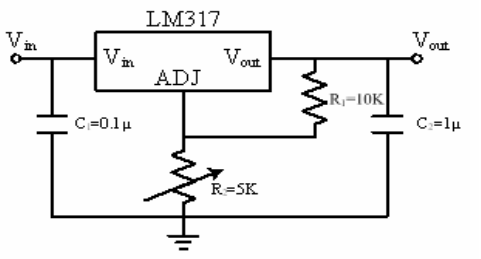


Fig. 5.4 LM317 regulator

The outputs of the regulators are bypassed on the PCB with the parallel combination capacitors then connected to the chip. The bypass filter network is combined by 10μF, 1μF, 0.1μF and 0.01μF capacitors as shown in Fig. 5.5. The

arrangement can provide decoupling of both low-frequency noise with large amplitudes and high-frequency noise with small amplitudes [31].

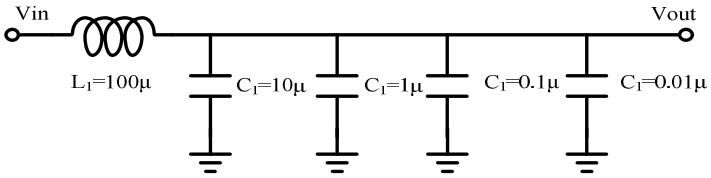


Fig. 5.5 Bypass filter at the regulator output

The measurement setup of the synthesizer is shown in Fig. 5.6. The input clock is produced from the signal generator (Agilent 81110A). The output spectrum is observed by a Spectrum Analyzer (Agilent E4440A).The testing PCB is shown in Fig. 5.7.

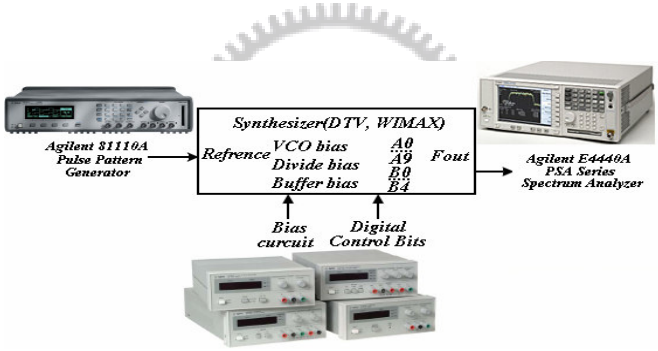


Fig. 5.6 Measurement setup of the synthesizer

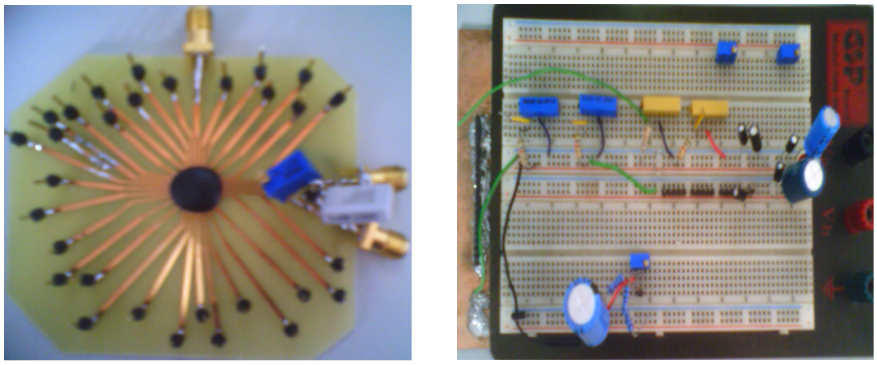


Fig. 5.7 The testing PCB in the synthesizer

5.3 Measurement Results

Fig. 5.8 shows the measured transfer curve of VCO. The measure tuning range is 2.11GHz~0.732 GHz, 2.86GHz~2.1GHz for VCO. The DTV system has 7 bands

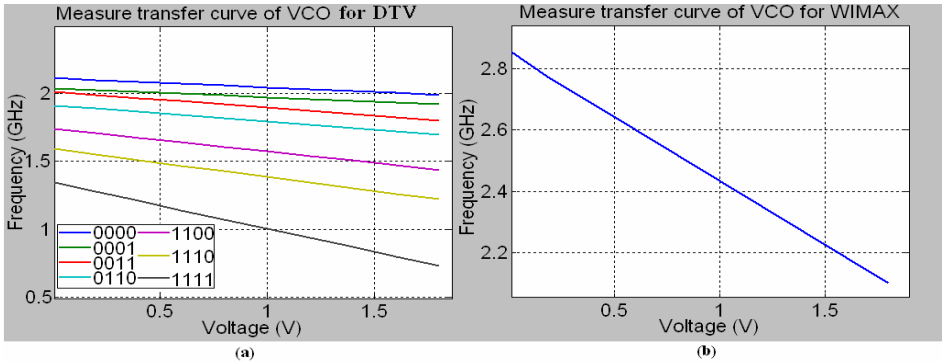
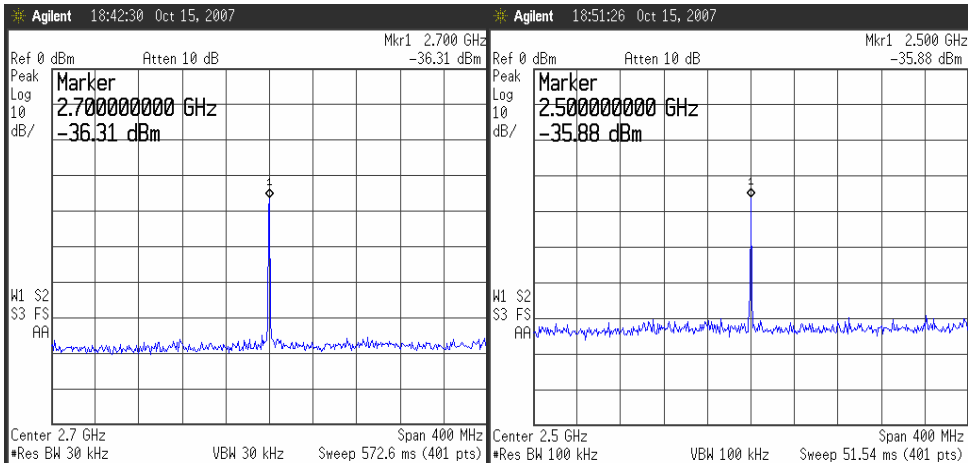
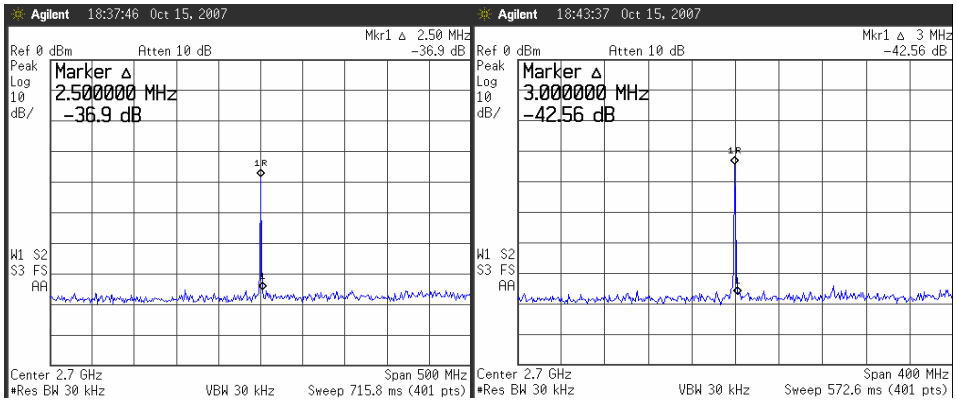


Fig. 5.8 Measure VCO transfer curve



(a) (b)

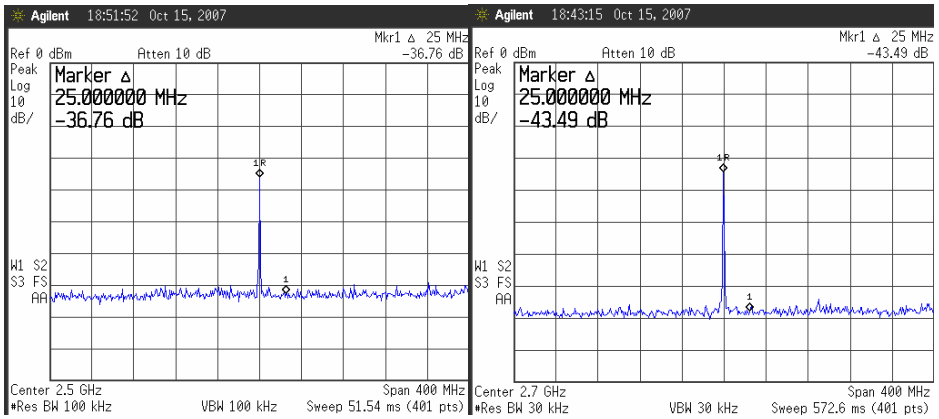
Fig. 5.9 Measured output spectrum of WIMAX (mobile) synthesizer



(a) 2.5MHz offset (b) 3MHz offset

-36.9-10log (30 • 10^3) =-81.67dBc/Hz -42.56-10log (30 • 10^3) =-87.33dBc/Hz

Fig. 5.10 Measured phase noise of lock synthesizer for WIMAX



(a) (b)

Reference spur=-36.76dBc Reference spur=-43.49dBc

Fig. 5.11 Measured reference spur of lock synthesize

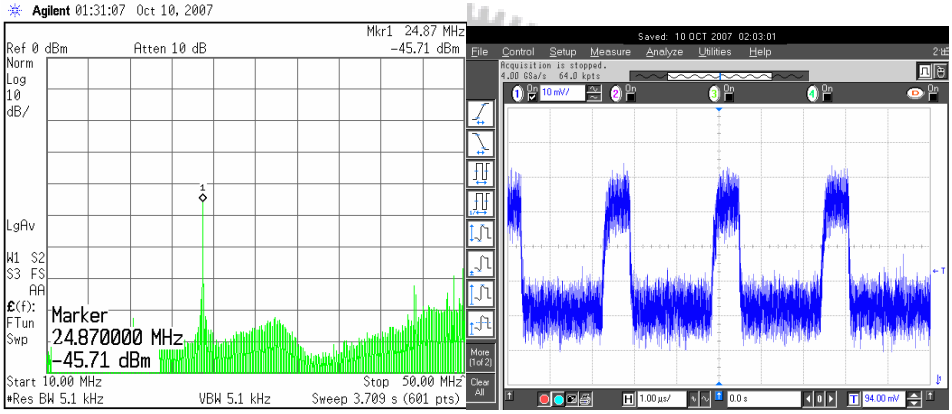


Fig. 5.12 Measured output spectrum of divide in lock 2.5GHz

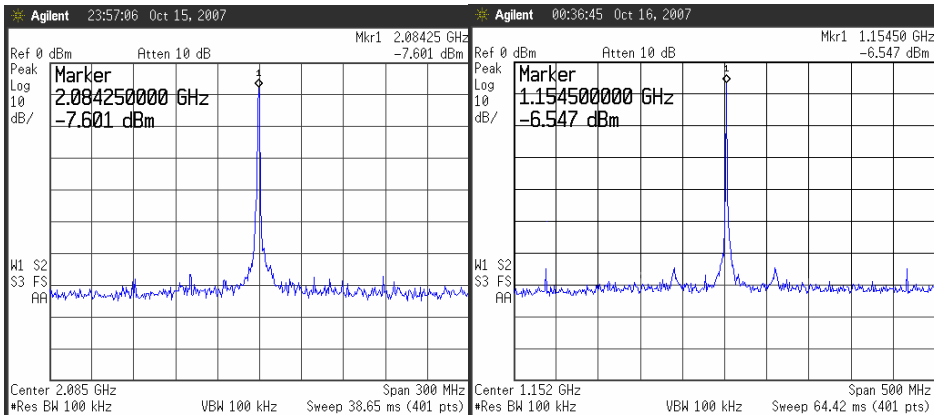
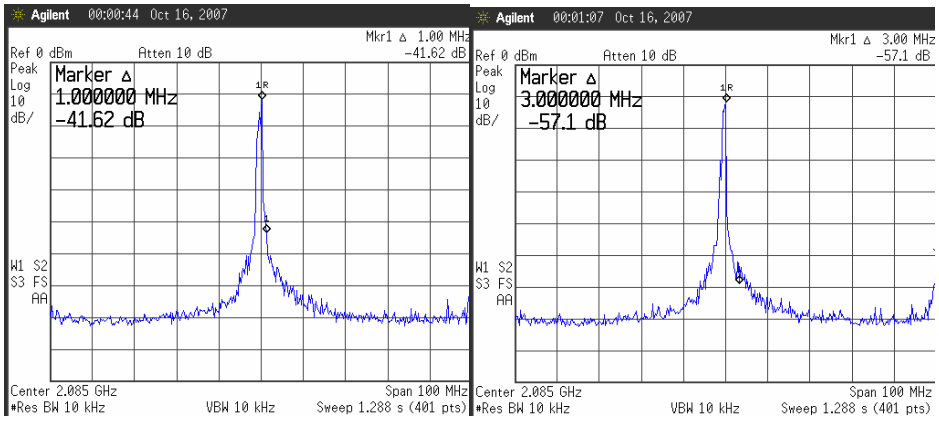


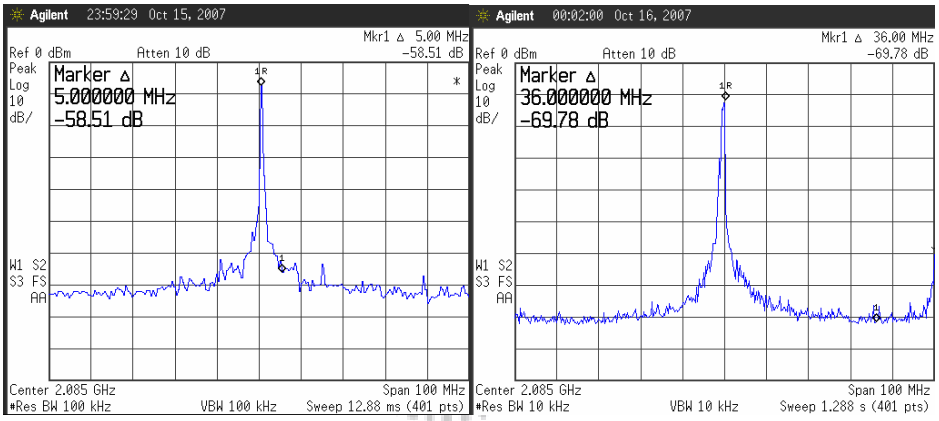
Fig. 5.13 Measured output spectrum of DTV synthesizer



(a) 1MHz offset (b) 3MHz offset

-41.62-10log (10 • 10^3) =-81.62dBc/Hz -57.1-10log (10 • 10^3) =-97.1dBc/Hz

Fig. 5.14 Measured phase noise of lock synthesizer for DTV



-58.51-10log (100 • 10^3) =-108.51dBc/Hz Reference spur=-69.78dBc

Fig. 5.15 Measured phase noise and reference spur of lock synthesizer for DTV

5.4 Measured Summary

In Fig. 5.9 shows the measured output spectrum of WIMAX (mobile) synthesizer where the PLL is locked. The output frequency is 2.5GHz, 2.7GHz which equals dividing ratio of 100, 108. In Fig. 5.11 the measured value of reference spur, there are 36.76dBc, 43.49dBc.Table 5.1 summarized the measured performance of the propose frequency synthesizer for DTV, WIMAX (mobile) system.

TABLE 5.1 Measure synthesizer performance summaries

Technology(TSMC)	0.18-um CMOS	0.18-um CMOS
Carrier Frequency	2.5GHz ~2.7GHz	1.15GHz~2.08GHz
Reference Frequency	25MHz	36MHz
Phase Noise @1MHz	N/A	-81.62dBc/Hz
Phase Noise @2.5MHz	-81.67dBc/Hz	N/A
Phase Noise @3MHz	-87.33dBc/Hz	-97.1dBc/Hz
Phase Noise @5MHz	N/A	-108.51dBc/Hz
Spur Level	-43.49dBc	-69.78dBc
Power dissipation	32mW	33mW
Supply Voltage	1.8V	1.8V
Die area	1.027mm×1.026 mm	1.14mm×1.14 mm

Chapter 6

Conclusions

6.1 Conclusions

A propose suppression technique is proposed for integer-N frequency synthesizer to reduce the amplitude and random the periodic ripple in lock without changing the loop parameter. The PLL synthesizer is composed of five building blocks: the phase frequency detector, the charge pump, the loop filter, the VCO and the programmable divider. A lot of design challenges can be found in each block, but this work has tackled the problems of the VCO, reference spur. We reduce the VCO gain and random the ripple in the frequency synthesizer.

The all-digital DSM is widely used in the fractional-N synthesizer because of many good properties. One major advantage is the reduction of the reference spur by randomizing the feedback division ratio such that the quantization noise of the fractional-N divider is transferred to higher frequency.

Some suggestions for the future work are given as follows. Firstly, the ESD protection should be considered in the circuit design and physical layout to avoid the instantaneous high voltage breaking down the circuit. Finally, parallel control bits of the modulator can be designed as serial input scheme to reduce the large number of PAD, which will save the area.

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