國立交通大學

電資學院光電顯示科技產業研發碩士班

碩士論文

底閘極多晶矽薄膜電晶體結晶方式之研究

Study on Thin Film Crystallization for Buttom Gate Poly-Si TFT

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摘　　要

以各種不同的結晶方式改善多晶矽薄膜電晶體的製程或特性，近年來受到廣泛的研究。一般而言，多晶矽薄膜結晶方式分為固相結晶和雷射退火結晶兩大類，在本論文中，吾人分別針對此兩類各提出一種結晶製程來製作底閘極多晶矽薄膜電晶體，固相結晶方面是採用旋塗奈米鈀溶液的方式來達到金屬誘發結晶；雷射退火結晶方面則利用沈積熱滯留層的方式來改善結晶狀態。而使用底閘極結構，除了減少製程複雜度外，針對目前日漸普及的汽車電子，亦能提供一個降低背照光漏電的參考途徑。

在金屬誘發結晶製程中，有別於傳統使用濺鍍的方式沈積金屬層，吾人採用旋塗奈米鈀溶液於非晶矽薄膜上，經由爐管退火成功轉變為多晶矽薄膜。藉拉曼和場發射掃描式電子顯微鏡輔助分析，吾人得知此製程在 450°C即可形成結晶，而在 550°C下的結晶速率約為每小時 4 μm，是傳統SPC的十倍。最後吾人亦實際應用此製程成功製作出底閘極多晶矽薄膜電晶體。

在準分子雷射退火製程方面，我們利用 SiON 薄膜的半穿透特性作為熱滯留層覆蓋在非晶矽薄膜上，並在雷射退火之後以時差式光學反射分析儀來做結晶狀況的分析。吾人從分析結果中證實加上熱滯留層的確可以增加非晶矽在雷射退火下熔融態時間，而從場發射掃描式電子顯微鏡輔助分析下，也證實了此法有助於多晶矽晶粒的成長，甚至達到橫向長晶的目的。

Study on Thin Film Crystallization for Buttom Gate Poly-Si TFT

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Abstract

Improving the process or performance of poly TFT by all kinds of crystallization methods have been wildly studied. Generally speaking, the crystallization method of poly thin film is divided into two classes, one is “Solid Phase Crystallization” (SPC), and the other is “Excimer Laser Crystallization”(ELC). In this thesis, we propose one crystallization process for two classes respectively to produce bottom gate poly TFT. In SPC, we used spin coating the nano Pd solution to get “Metal-Induce-Crystallization”(MIC), and in ELC, we deposited the “Heat-Retainenhance-Layer”(HRL) to enhance grain growth. We select bottom gate structure because of its uncomplicated process, moreover, it may be provides one way to reduce the back light leakage current for popular day by day car electronics.

In MIC, different from the conventional method of sputtering Pd layer on a-Si film, we spin coated nano Pd solution on a-Si film, and we get the poly film successfully after furnace annealing. To analyse with Raman and Scanning Electron Microscope(SEM), we observed the poly film could be formed in 450°C by this process, and the grain growth rate is 4μm/hr approximately, which is ten times to conventional SPC. Finally, we also applying this process to produced a bottom gate poly TFT successfully.

In ELC, we deposited SiON as HRL capped on a-Si layer because of its half-transparent

characteristic, and we analysed with “Time-Resolved Optical Reflectivity” to observe the crystallization condition after ELA process. With analysis data, the phenomenon that capping HRL will increase the melting duration is well confirmed. It is also verified that this process will enhance the grain growth, even to achieve lateral grain growth.

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Chapter 1

Introduction

1.1 Flat Panel Display

Flat panel display (FPD) technologies have advanced significantly during the last two decades. As computer and other intelligent electronics shrink to pocket size, FPD technology becomes more important. Newer flat panel technologies have been developed and are expected to surpass CRTs in market share. The Fig. 1-1 shows the FPD market scale in recent years, and it also estimates the output value will reach 92 billion dollars in 2007 in advance.

Thin films transistor (TFT) is a primary element in AMLCD, TFT-FED and AMOLED, as Fig. 1-2, so the research about the fabrication or electric characteristic of TFT is very wildly in recent years.

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1.2 Brief Introduction of a-Si:H TFT's and Poly-Si TFT's

A thin film transistor (TFT) is defined as follows: a field-effect transistor built using a semiconductor thin film which is originally deposited on an insulating substrate and processed at temperatures below the melting point of the semiconductor material [1]. For TFT's using Si thin films, they are divided

into amorphous Si (a-Si) TFT's and polycrystalline silicon (poly-Si) TFT's.

1.2.1 *a*-Si TFTs technology

For several years, hydrogenated amorphous silicon (a-Si:H) TFT's have played a significant role in large-area electronics because of the following advantages: low temperature process (< 350℃) compatible with large area glass substrate, continuous process, and low leakage current property suitable for pixel switching[2]-[4]. However, the application of *a*-Si:H TFT was constrained due to its poor field-effect mobility (< 1cm2/V.s) and small on-current. With increasing pixel density of TFT-LCD, high mobility TFTs are required to shorten the charging time of pixel electrodes. But the mobility of *a*-Si TFT is too low to meet this requirement. Thus, the high-resolution TFT LCD display needs to find a solution to improve the mobility of TFTs. The poly-Si TFTs technology is one of the potential methods to achieve this goal. The mobility for *a*-Si TFTs can be improved easily by introducing poly-Si film instead of *a*-Si as an active layer of TFTs.

1.2.2 poly-Si TFTs technology

Recently, poly-Si is believed a more promising material compared with a-Si due to its much higher carrier mobility (ranging from 10 to 300 cm^2/V-s) [5]-[6]. Fig. 1-3 shows the circumstances. In 1966, the first polycrystalline silicon thin-film transistors (Poly-Si TFTs) were fabricated by Fa et al. [7]. Up to now, poly-Si TFTs have received lots of attention because of their wide applications in driving circuits and pixel devices of active matrix liquid crystal displays (AMLCDs)[8]-[12] and light emitter polymer displays (LEPDs)[13],

field emission displays (LEDs)[14]-[16], memory devices[17]-[20], image sensors[21], thermal printer head[22], and photodetector amplifier[23].

A variety of techniques have been investigated for formation of poly-Si films, they could be divided into two classes according to whether the thin film melt or not : (1) solid-phase crystallization (SPC), (2) excimer laser crystallization (ELC).

1.2.2.1 SPC

Conventionally, the as-deposited amorphous Si is annealed by a furnace using SPC method to transform its morphology into polycrystalline. In the SPC method, the *a*-Si films were crystallized at 600 ℃ for tens hours in the furnace. SPC method occurs through the processes of nucleation and grain growth [24][25], and it has the advantages of simplicity, low cost and good uniformity [26][27]. However, the main disadvantage of this technique is that the crystallization may take a long time (several hours at 600℃) so that the thermal cycle still warped the glass substrate[28]. Efforts have been made to reduce the incubation time without sacrificing conditions favorable to the maximization of grain size.

1.2.2.2 ELC

In recent years, excimer laser processing used to crystallize a-Si thin film has been extensively researched [29]-[32]. Laser crystallization is a much faster process than SPC and can produce large grained poly-Si with a low dislocation density[33]-[35]. The basic principle of laser crystallization is the transformation from amorphous to crystalline silicon by melting the silicon for a

very short time(about tens of nanoseconds). After removing the laser, crystallization is seeded from the underlying remaining grains. Strictly speaking, laser crystallization is not a low temperature process as the silicon is heated well above 1200 °C. However, the high temperatures are only sustained for a very short time. Due to the short time scale the thermal strain on the low-temperature substrates does not lead to severe damage or destruction of these substrates. The crystallization technology is now applied to TFT production for flat panel displays [36]-[38]. LTPS TFTs fabricated by ELC of a-Si thin films has been widely studied due to its good electrical properties, such as high mobility and low threshold voltage.

However, for laser energy greater than a threshold value, called full-melt threshold (FMT) energy, complete melt of the film occurs. The situation results in homogeneous nucleation, producing much smaller grain. Therefore, the laser beam energy should be precisely controlled in a narrow window. It can be regarded as low temperature process because substrate heating is not needed.

1.3 Motivation

With LCD market popularization, all kinds of research that how to improve the performance of LCD have been wildly. Among them also include how to promote the performance of TFT(mobility, aperture ratio…etc. , for example), because it is a essential device of LCD. As the statement in the front, the application of Poly-Si TFTs will be paid attention to LCD because of its better performance than a-Si TFTs, produce an instance, the LCD will have higher resolution, lower power consumption, and it maybe reach the purpose of

“system on panel” like Fig. 1-4.

As a result, in this thesis, we propose one crystallization process for two classes in the former discussion respectively to produce bottom gate poly TFT. In SPC, we used spin coating the nano Palladium (Pd) solution to get “Metal-Induce-Crystallization” (MIC), and in ELC, we deposited the “Heat-Retainenhance-Layer” (HRL) to enhance grain growth. With this research, we expect to offer the method that could simplify traditional process, increase production efficiency, and it still could have good performance of TFT, in the hope of achieving the goal of reducing the production cost effectively. On the other hand, we select bottom gate structure because of its uncomplicated process and better electric characteristic, Moreover, it maybe provides one way to reduce the back light leakage current for popular day by day car electronics.

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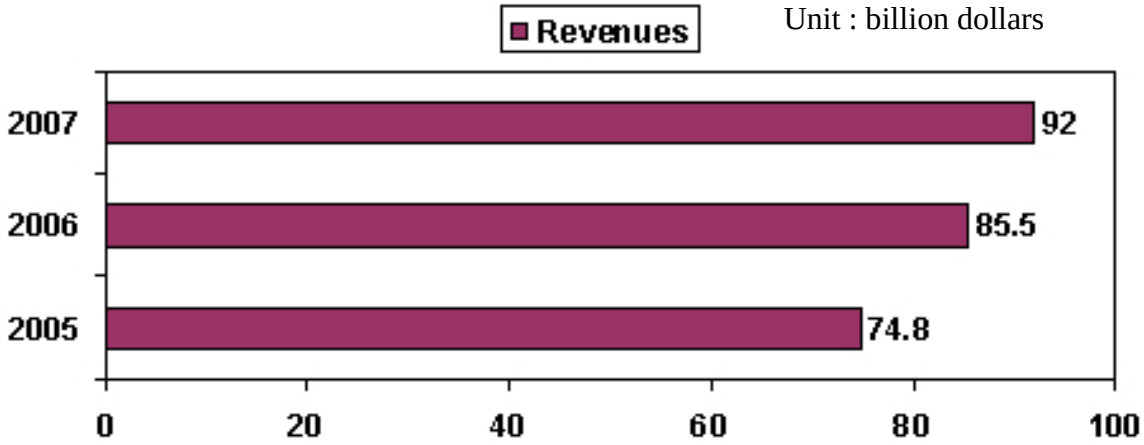


Fig. 1-1

Source :DisplaySearch，Science & Technology Policy Research and Information Center（STPI），2007/01

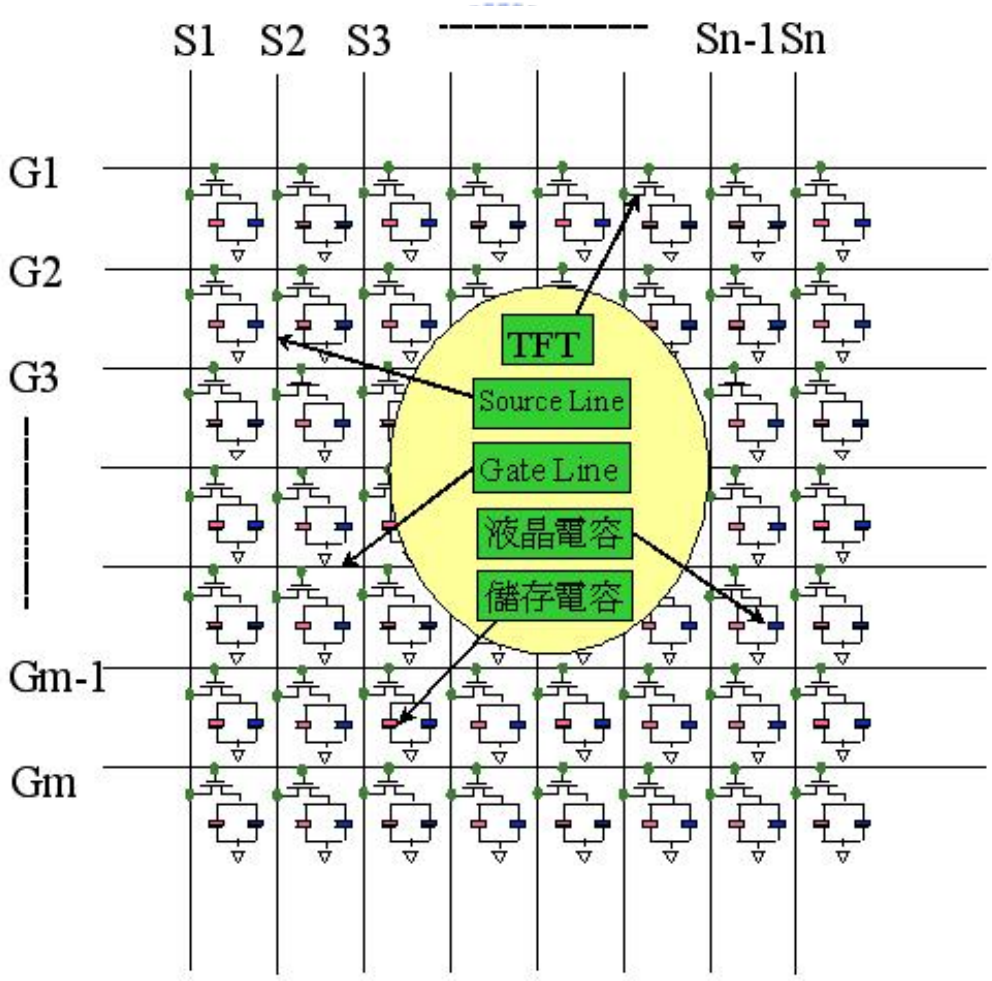


Fig. 1-2

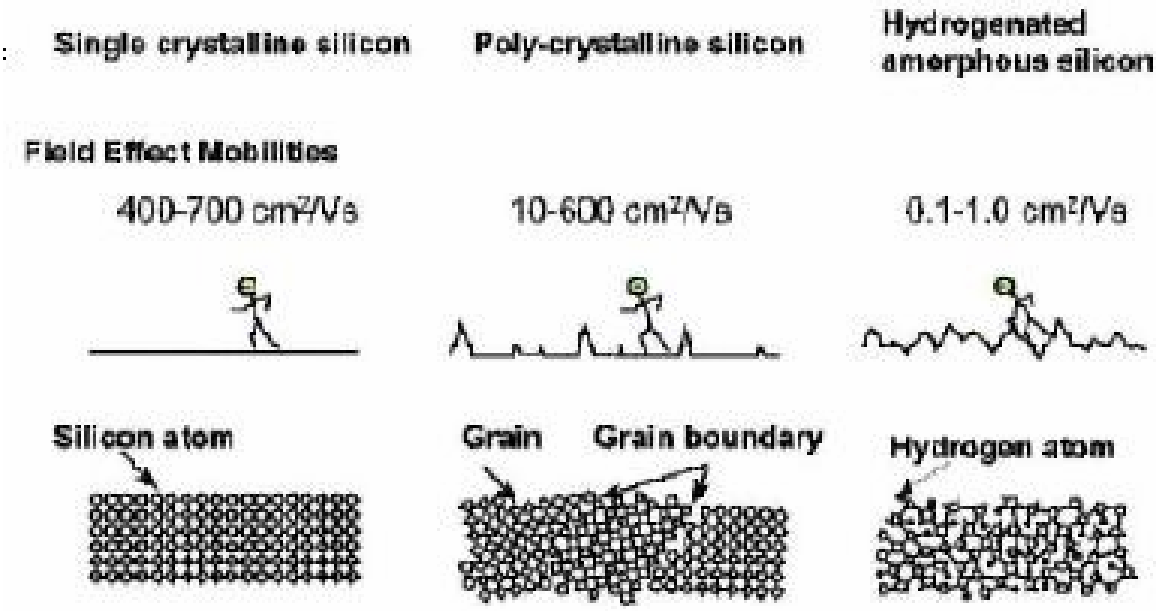

Single crystalline silicon
Poly-crystalline silicon
Hydrogenated amerpheus silicon
Field Effect Mobilities
400-700 cm²/Vs
10-600 cm²/Vs
0.1-1.0 cm²/Vs
Silicon atom
Grain
Grain boundary
Hydrogen atom

Fig. 1-3

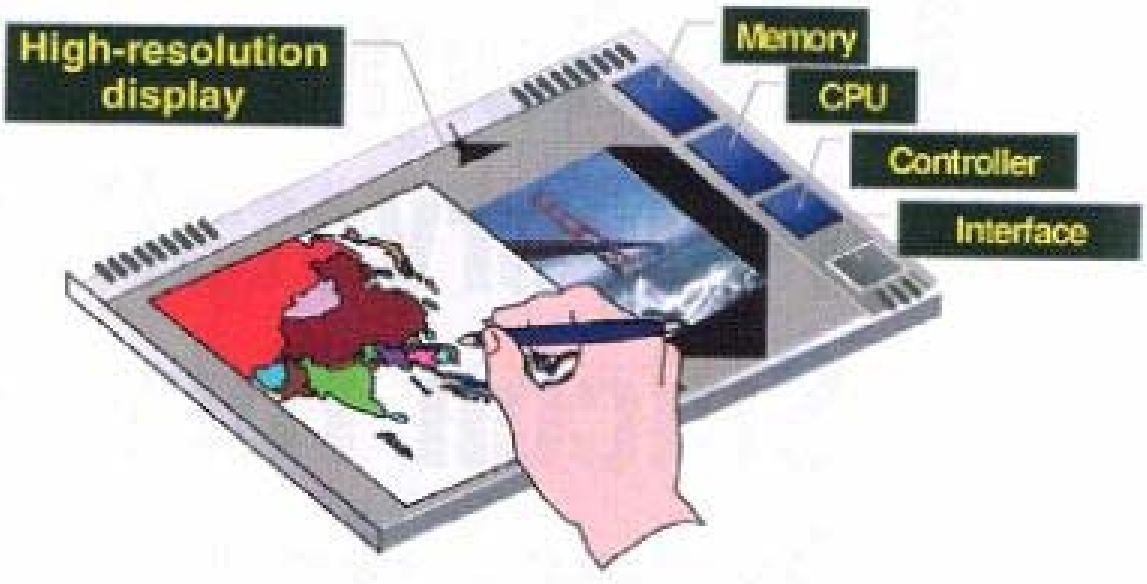

High-resolution display
Memory
CPU
Controller
Interface

Fig. 1-4

Chapter 2

Pd MIC Process

2.1 Introdoction

The disadvantages of SPC method are its high temperature and time-consuming thermal furnace annealing process, which has hindered SPC from commercial applications. These disadvantages could be improved by MIC/MILC method. Many studies have reported that the crystallization temperature of *a*-Si can be lowered with the addition of some metals which can be classified into two large groups. One is eutectic-forming metals such as Ag[39][40], Au[41], Al[42], Sb[43], and In[44], and the other, silicide-forming metals such as Pd[45][46], Ti[47], Ni[48]–[50], and Cu[51].

In previous studies, non-siliside forming metal such as the former metals are known that metal atoms dissolved in *a*-Si films may weaken Si bonds and enhance nucleation of crystalline silicon(*c*-Si). On the other hand, in the case of nickel among the latter metals, it is known that preformed nickel disilicides, for which the lattice mismatch is only 0.4% with Si, act as nuclei for *c*-Si. And then the grain growth of Si proceeds by the diffusion of Si atoms through a thin $NiSi_2$ layer. However, in the case of palladium, crystallization behavior is different from that of other metal.

2.2 The Mechanism of Pd MIC

According to the research in the past, Pd is a fast interstitial diffuser and almost insoluble in *c*-Si below 500 °C, but the solubility of fast diffusing species in *a*-Si is known to be higher than that in *c*-Si and very sensitive to the defect concentration in *a*-Si[52]. For this reason, the Pd metal contamination in poly-Si film might be less than other metal after annealing. This is necessary to fabricate poly-Si TFTs without metal contamination, so the Pd metal was chosen to induce crystallization of a-Si in our study.

The mechanism of Pd MIC/MILC which is described below was reported by Lee et al.[53][54]. At first, we proposed the novel model of MILC phenomenon in the previous work[55], which states that there are three steps in MILC phenomena. The first step is the Si–Si bond breaking and the migration of the silicon atom to the silicide in the interface between the amorphous silicon and silicide (interface <1>). The second step is the silicon atom hopping to the interface between silicide and single-crystalline silicon (interface <2>). The last step is the rearrangement of the silicon atom to single-crystalline silicon. A thin Pd layer was deposited on *a*-Si film and lead to the formation of Pd_2Si in the early stage of thermal annealing. Pd_2Si had a hexagonal structure and its basal plane was epitaxial on the (111) plane of Si [56]. Therefore, the crystallization of *a*-Si might be initiated through epitaxial growth on previously crystallized Pd_2Si at the interface <1>.

Fig. 2-1 shows the schematic diagram of Pd induced crystallization of a-Si. The crystalline mismatch between Pd_2Si and Si is around 1.9%, and the

distance between Si atoms in (110) direction is 3.84 Å. The peeled Pd_2Si precipitates would prefer to cohere with *c*-Si structure, so that the size will be approximately 200 Å (3.84Å/1.9%). In order to maintain continuity of Si atoms in *c*-Si and Pd_2Si precipitates, the Pd_2Si sheets have to be bent as in Fig. 2-1. So the Si-Si bond is destroyed easily and help Pd_2Si to migrate to *a*-Si. The role of Pd_2Si is to catalyze the Si crystallized to form the needle-like poly-Si and this reaction is so called MIC.

2.3 Experiment

Different from the conventional MIC method of sputtering Pd layer on *a*-Si film, we used a kind of solution with Pd to spin coat on it. Compare with the sputter method before, our method will have some advantages below : It is a simple and fast process, so that it is beneficial to produce in a large amount, and then achieve the goal of lowering costs. On the other hand, the density of nano Pd in solution is less than sputter the Pd layer, so it maybe provide the way to more reduce metal contamination. In order to test and verify the condition of crystallization by this process, we have done the experiment procedure as fig. 2-2.

2.3.1 Sample Preparation

At first, as the material analysis sample, a thermal oxide film of 1μm was grown on a 6 inch silicon wafer after RCA clean, and then an *a*-Si film of 1000 Å was deposited at 650°C by low pressure chemical vapor deposition (LPCVD) using disilane as a source gas. Then we used photo resist(PR) to pattern source/drain figure to observe conveniently as Fig. 2-3 shows, and we

spin coated the Pd solution on the samples with 500 rpm by spin coater, then 100°C baked on hot plat for 60 seconds. Finally, the samples were dipped in HF around ten seconds to get rid of native oxide and annealed by backend atmospheric anneal furnace for different temperature or different time respectively.

2.3.2 Raman Spectrograph

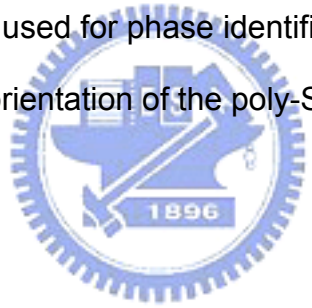
RENI-SHAW 2000 Raman shift spectroscopy with an Ar ion laser as an excitation source that has a scattering range from 0-600 cm^{-1} examined the microstructure of the film. The Raman measurement was performed at room temperature and repeated 10 times at the same measured position. Analysis in Raman signal, we can get the degree of the crystallization.

2.3.3 Scanning Electron Microscope Observation (SEM)

The surface morphologies of blank samples were observed by a Hitachi S-5700 field emission scanning electron microscope (FESEM). Before the SEM observation, samples were firstly seco etched by a special solution ($HF+Kr_2Cr_2O_7+H_2O$). We could observed the images of crystallization of the thin film, and then learn the grain growth rate.

2.3.4 Glacing Incidence X-Ray Diffraction Analysis (XRD)

The traditional tools for the determination of phase and crystal structure of thin films are glancing-angle X-ray diffraction (GIXRD) spectrometry. These techniques sacrifice lateral resolution to grain depth resolution. By using a glancing angle of incidence, a large area and hence a large volume of the thin-film sample is analyzed by the X-ray beam. The arrangement increases the in-depth resolving power of X-ray diffraction. Thin films with thickness of 10 to 30 nm can be analyzed. A Mac glancing angle X-ray diffractometer with the usual Bragg-Brentano geometry, equipped with a post sample monochrometer (bent graphite crystal), was used for phase identification. The incident angle of X-ray was fixed at 1^{o}. The orientation of the poly-Si thin film after annealing could be measured by it.



2.3.5 Application of Bottom Gate TFT

After analysis of material, we proposed a bottom gate structure TFT which applied the process, as Fig. 2-4. The detail procedure is below:

(1) 5500 Å wet oxide was deposited on 6 inch wafer by LPCVD as buffer oxide after RCA clean.

(2) 1000 Å N+ poly-Si was deposited by LPCVD.

(3) Gate patterned by photolithography process.

(4) 1000 Å TEOS oxide was deposited by LPCVD as gate oxide.

(5) 1000 Å *a*-Si was deposited by LPCVD and dopant phosphorous.

(6) Source/Drain patterned by photolithography process.

(7) 1000 Å *a*-Si was deposited by LPCVD.

(8) Active region patterned by photolithography process.

(9) Spin coat Pd solution and 550°C annealing by backend atmospheric anneal furnace for different time, 1hr to 5 hr.

2.4 Results and Discussion

2.4.1 Raman Spectrograph

As we know, the Raman signal peak of single crystalline silicon is around 520, and the more strong intensity on 520, the thin film has more pure poly type. Fig. 2-5 shows the Raman diagram of different temperature, 450°C, 500°C and 550°C, after 6hr annealing. In Fig. 2-5, we observe that the thin film could crystallize above 450°C, and with the increase of temperature, the higher peak value of 520 is. That means the higher anneal temperature will lead to the better crystallization, because higher temperature could offer more energy to crystallize. On the other hand, we find it under the same temperature, the longer time is to anneal, the state of the crystallization is better, as Fig. 2-6 shows. Besides, we notice that the states of crystallization are similar above 4hr annealing.

2.4.2 SEM

Fig. 2-7 ~ Fig. 2-12 show the grain growth image by SEM analysis. Fig. 2-7 is 1hr annealing, the crystallization type is not obvious. In Fig. 2-8, 2hr annealing, the needle-like grain begin to be observed, and it is more conspicuous in Fig. 2-9, 3hr annealing. With the increase of annealing time,

the grain growth is also increase, such as Fig. 2-10 ~ Fig. 2-12. That is tallied with the result of Raman analysis former. Finally, we draw a grain size with time diagram according these data, as Fig. 2-13, and we get the grain growth rate is around 4μm/hr. It is about 10 times to conventional SPC process.

Moreover, it is significant that the grain have two orientations which are measured by XRD followed: <111> direction for the primary growth and <211> direction for the secondary growth. The <111> direction grain is more and more great with annealing time increase, because the primary growth dominant Pd-MILC has a faster MILC rate [57].

2.4.3 XRD

Fig. 2-14 shows XRD diagram with different annealing time. There are indeed two orientation, <111> and <211>, of crystallization. Among them, the peak value of <111> is increase with annealing time increase. That means the state of crystallization is become great with longer time, and it is conformed to SEM analysis.

2.4.4 Application of Bottom Gate TFT

Among five different time sample, 1hr, 2hr and 5hr have no electric characteristic of TFT, because the source/drain activation is not yet enough below 2hr but over above 5hr. Fig. 2-15 shows the Vg/Id diagram of 3hr and 4 hr. The mobility are 58 and 67 (cm2/Vs) respectively. Among them, the TFT with 4hr annealing has higher on-current, leakage current and mobility

because of its bigger grain size.

2.5 Summary

In this chapter, we used the method of spin coating the solution with nano Pd on *a*-Si film, and it crystallization successfully after annealing by backend atmospheric anneal furnace to reach the purpose of MIC. It is observed that the longer annealing time or the higher annealing temperature would lead to better performance of crystallization. Finally, we also produce the bottom gate poly-Si TFT which is applied the process successfully.

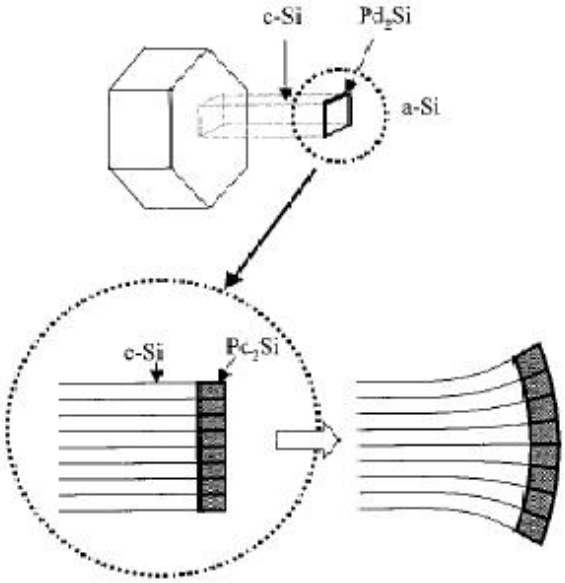

c-Si
Pd_2Si
a-Si
c-Si
Pd_2Si

Fig. 2-1

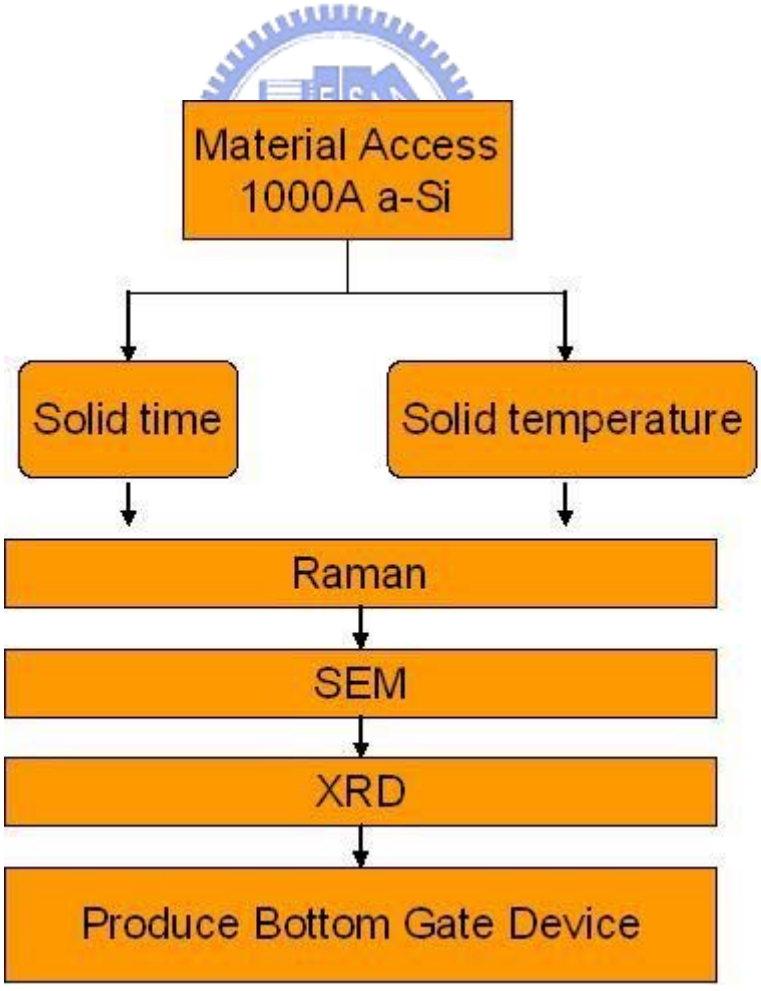

Material Access
1000A a-Si
Solid time
Solid temperature
Raman
SEM
XRD
Produce Bottom Gate Device

Fig. 2-2

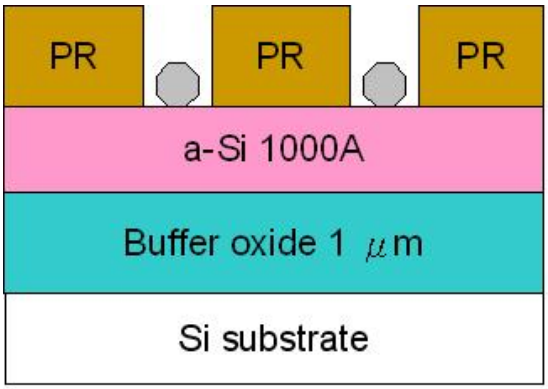


fig. 2-3(a)

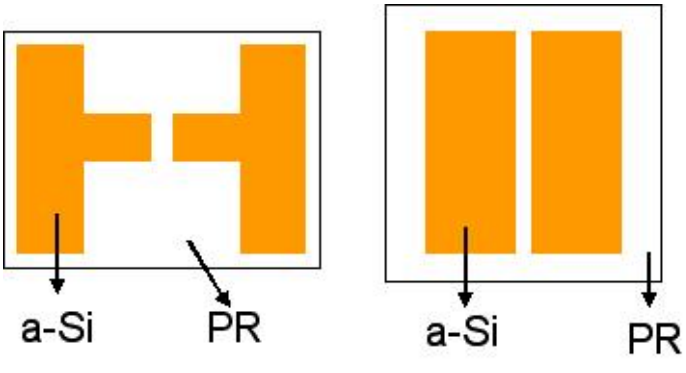


Fig. 2-3(b)

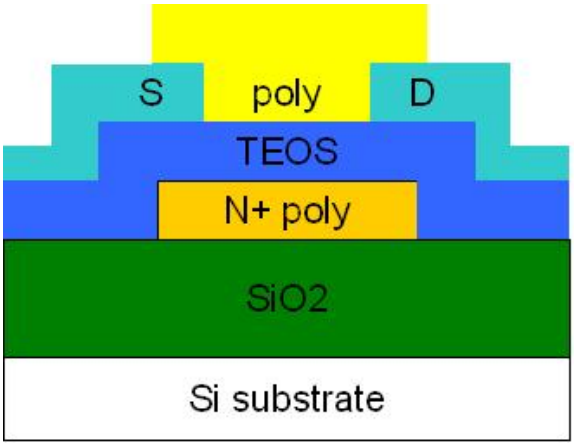


Fig. 2-4

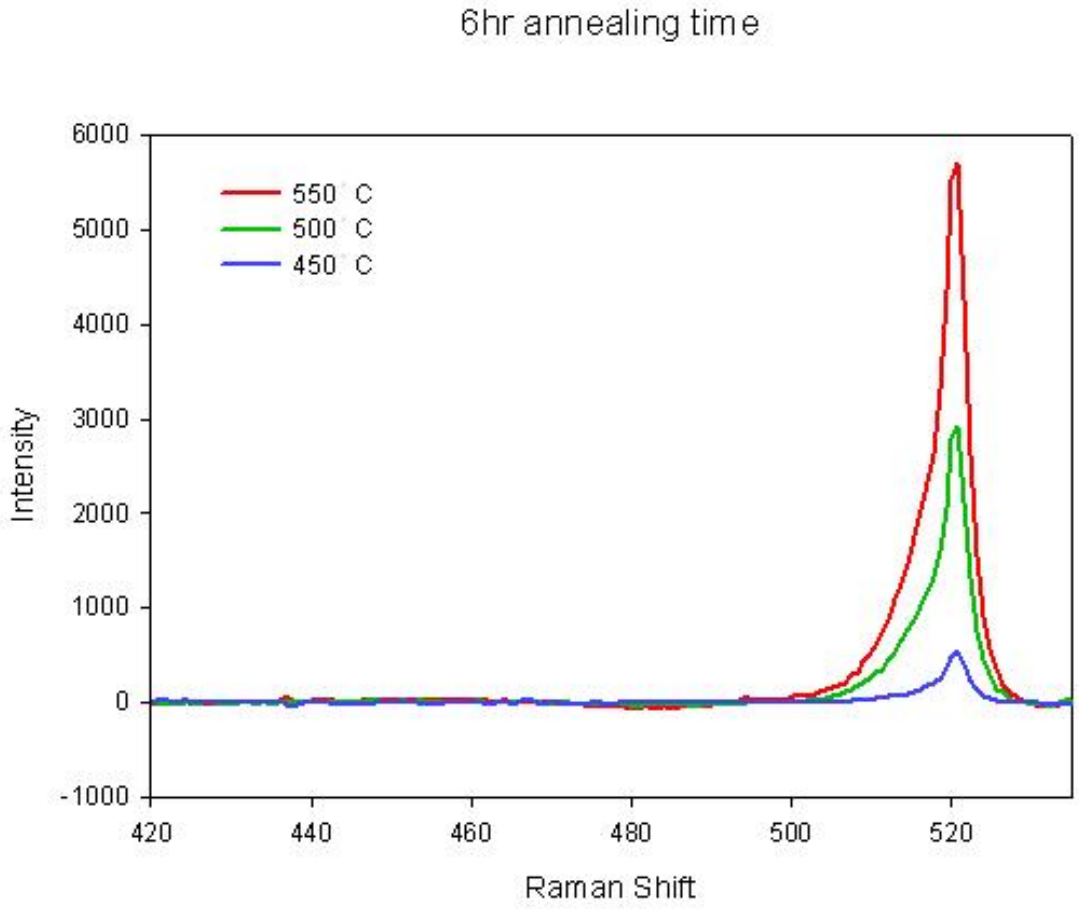

6hr annealing time
550 C
500 C
450 C
Intensity
6000
5000
4000
3000
2000
1000
0
-1000
420
440
460
480
500
520
Raman Shift

Fig. 2-5

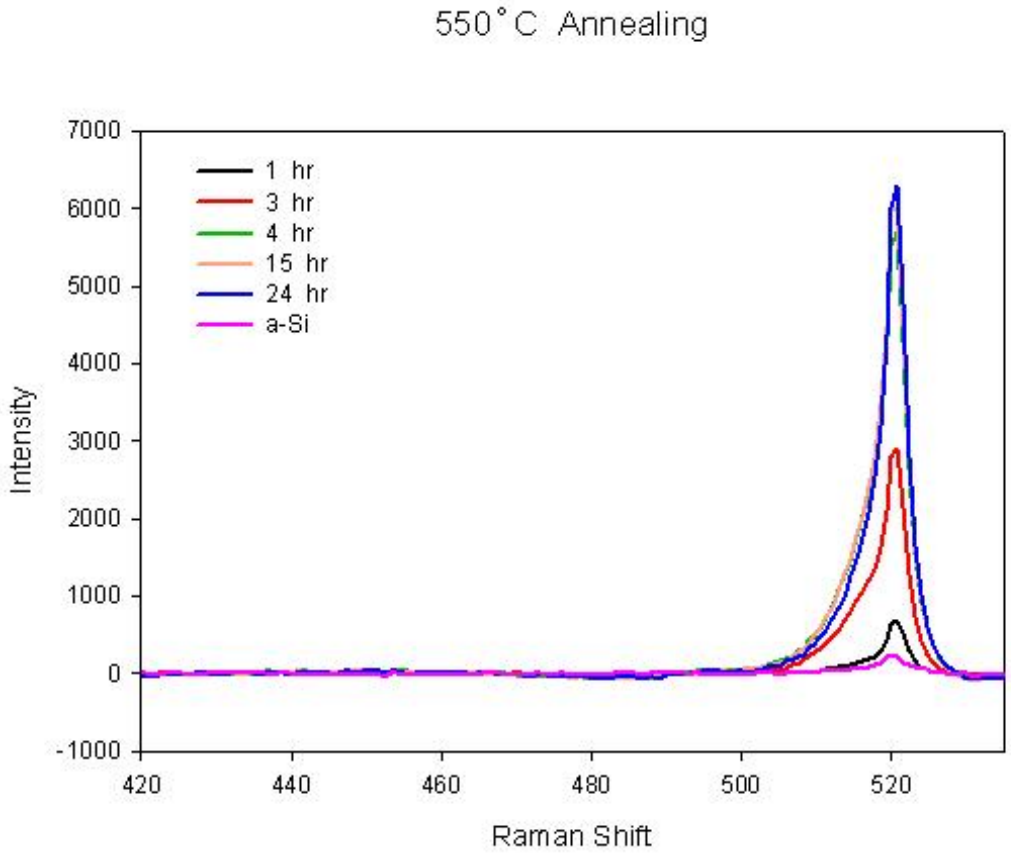

550°C Annealing
1 hr
3 hr
4 hr
15 hr
24 hr
a-Si
Intensity
Raman Shift
7000
6000
5000
4000
3000
2000
1000
0
-1000
420
440
460
480
500
520

Fig. 2-6

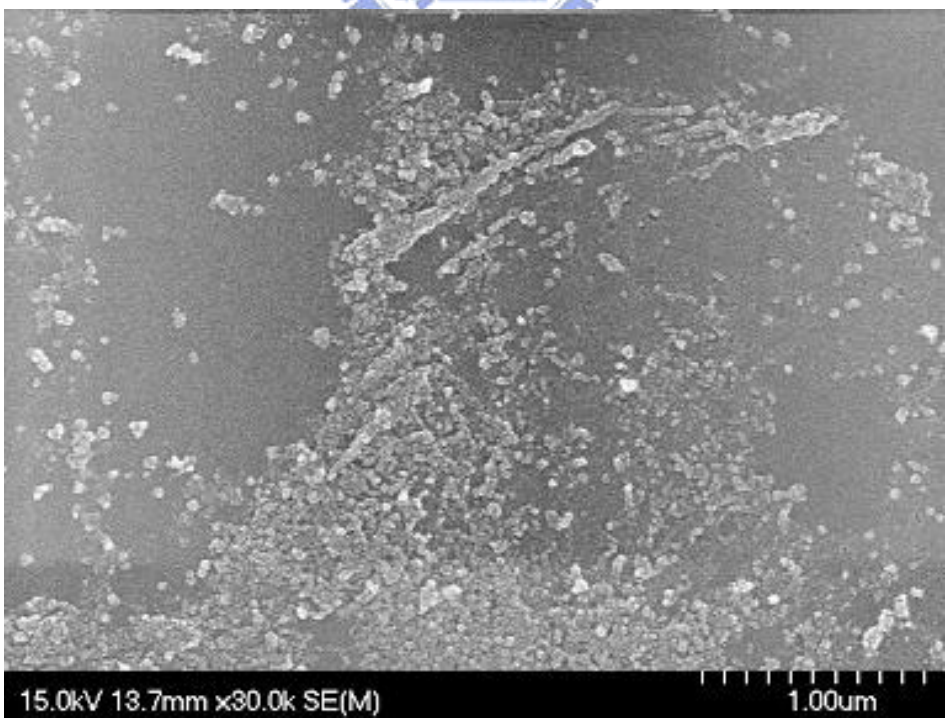

15.0kV 13.7mm x30.0k SE(M)
1.00um

Fig. 2-7

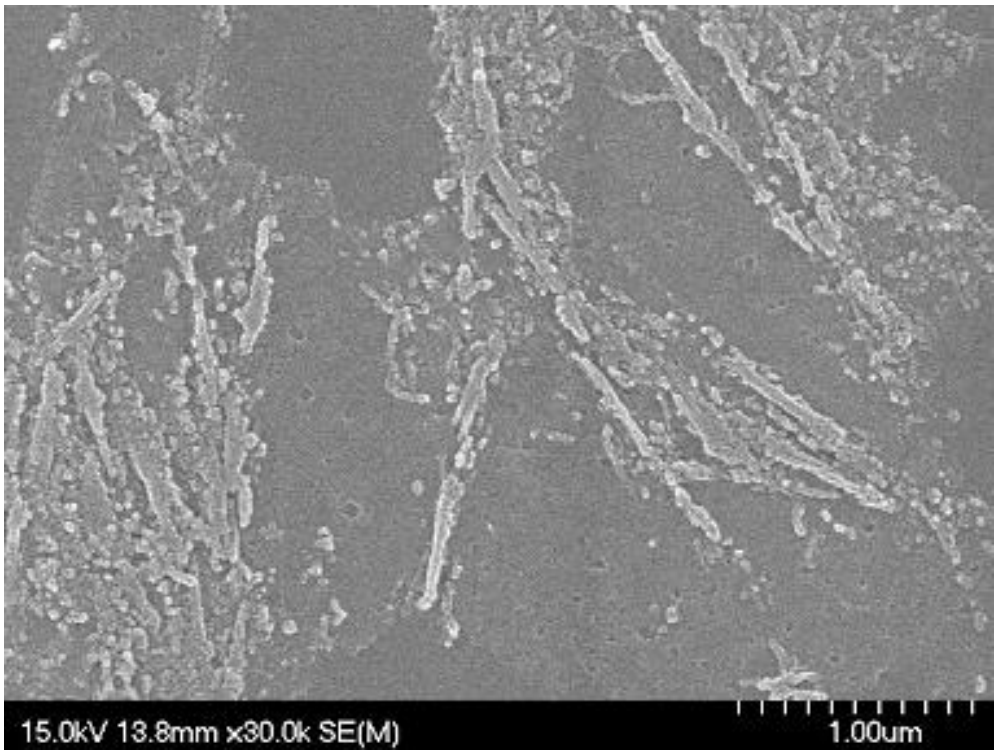

15.0kV 13.8mm x30.0k SE(M)
1.00um

Fig. 2-8

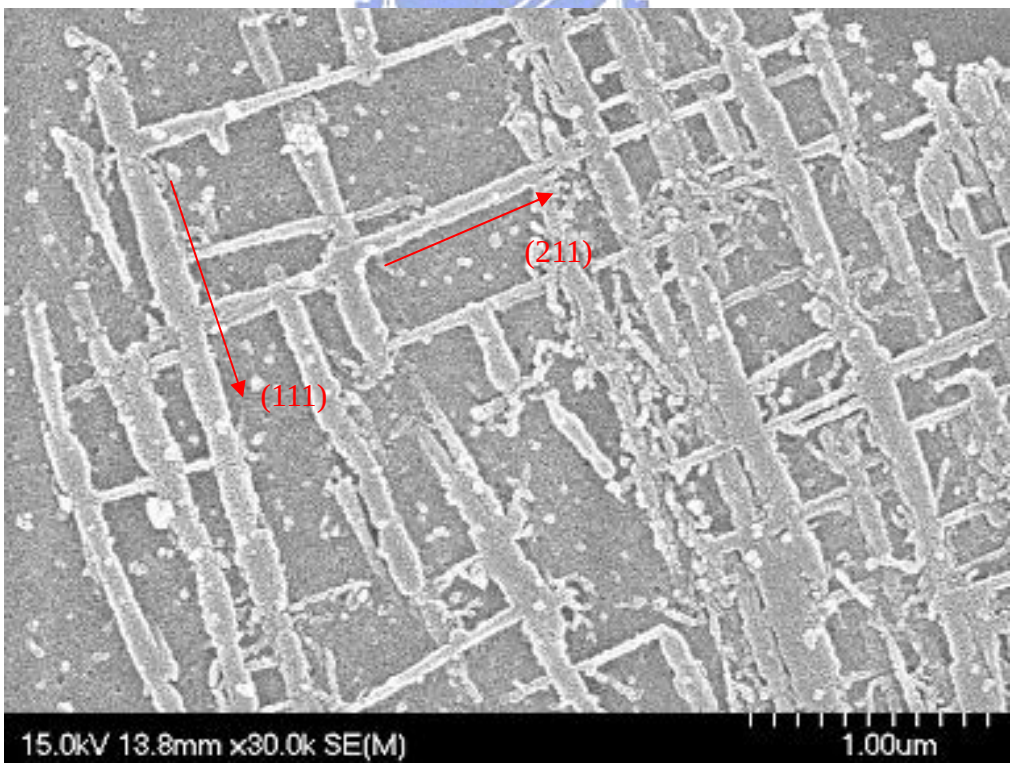

(211)
(111)
15.0kV 13.8mm x30.0k SE(M)
1.00um

Fig. 2-9

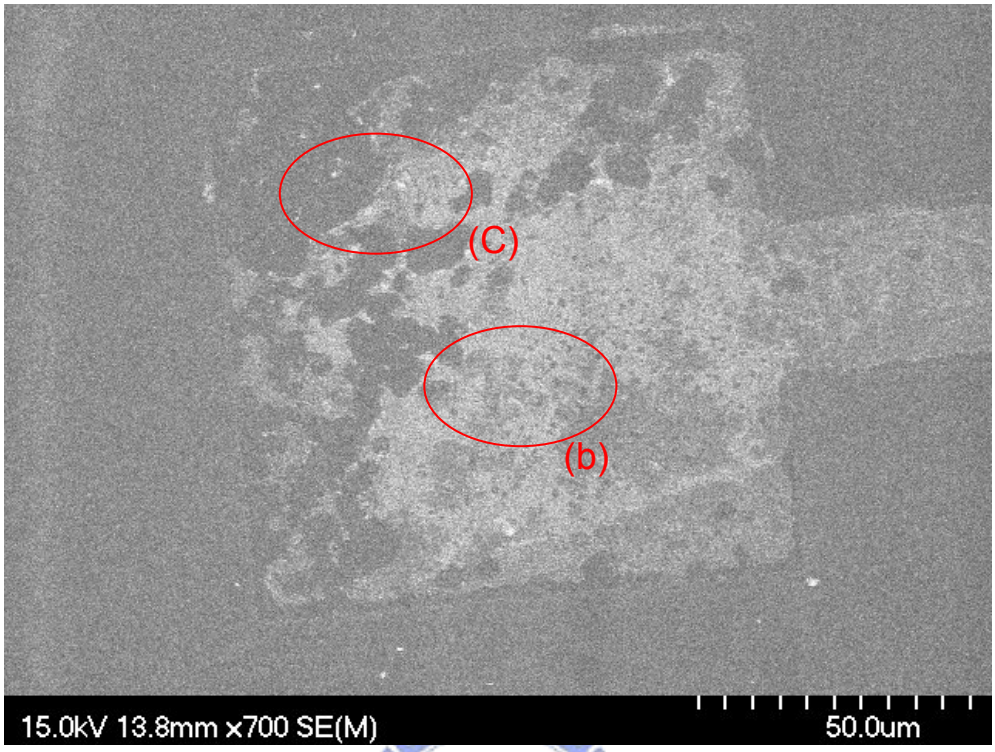


Fig. 2-10(a)

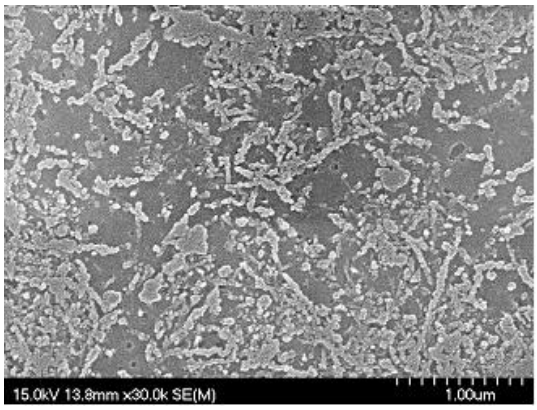


Fig. 2-10(b)

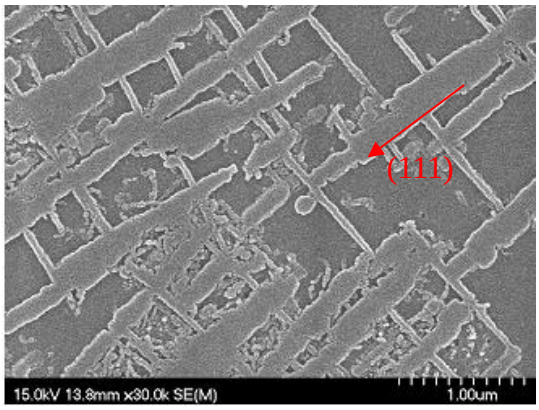


Fig. 2-10(c)

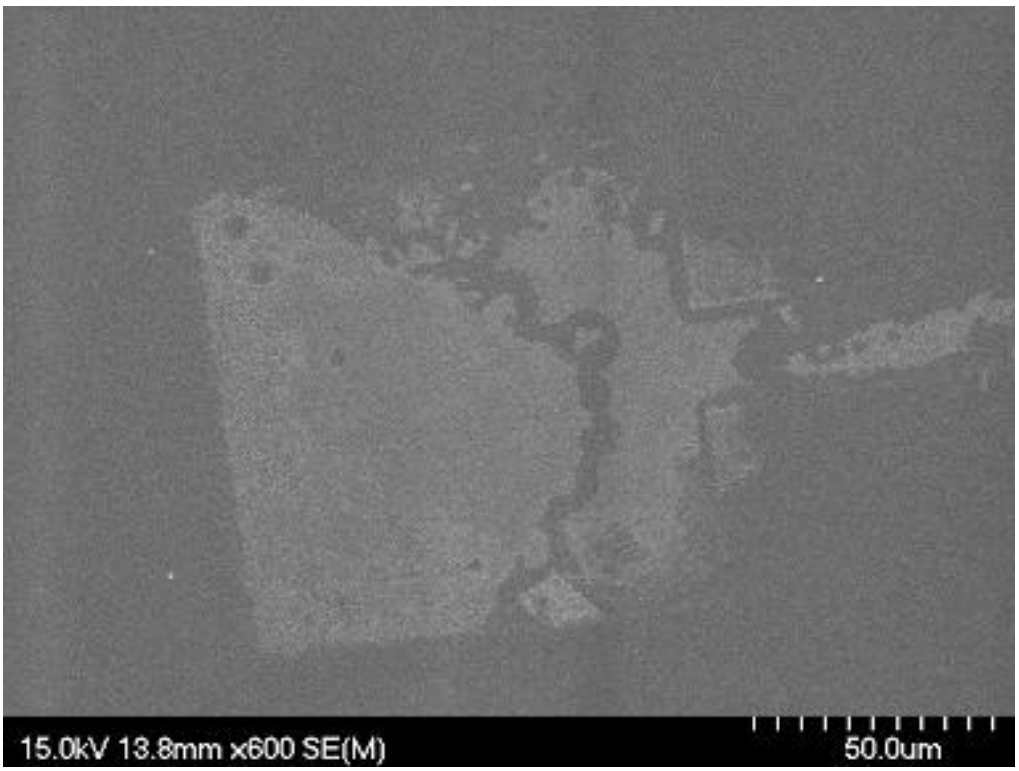


Fig. 2-11(a)

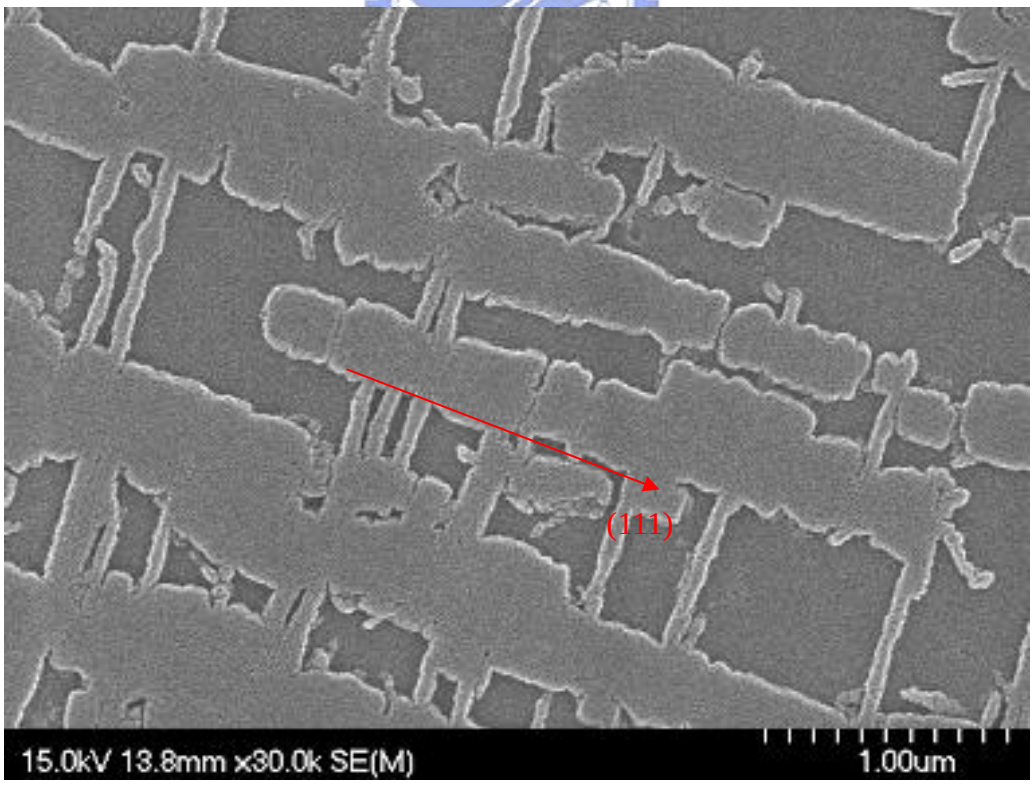


Fig. 2-11(b)

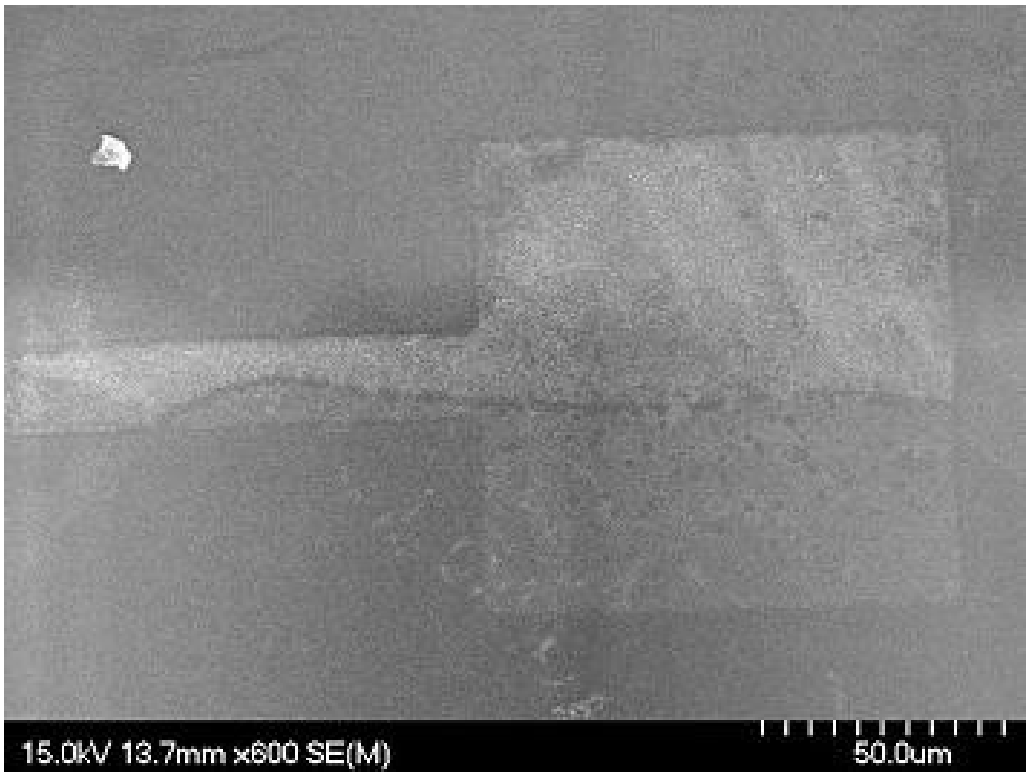


Fig. 2-12(a)

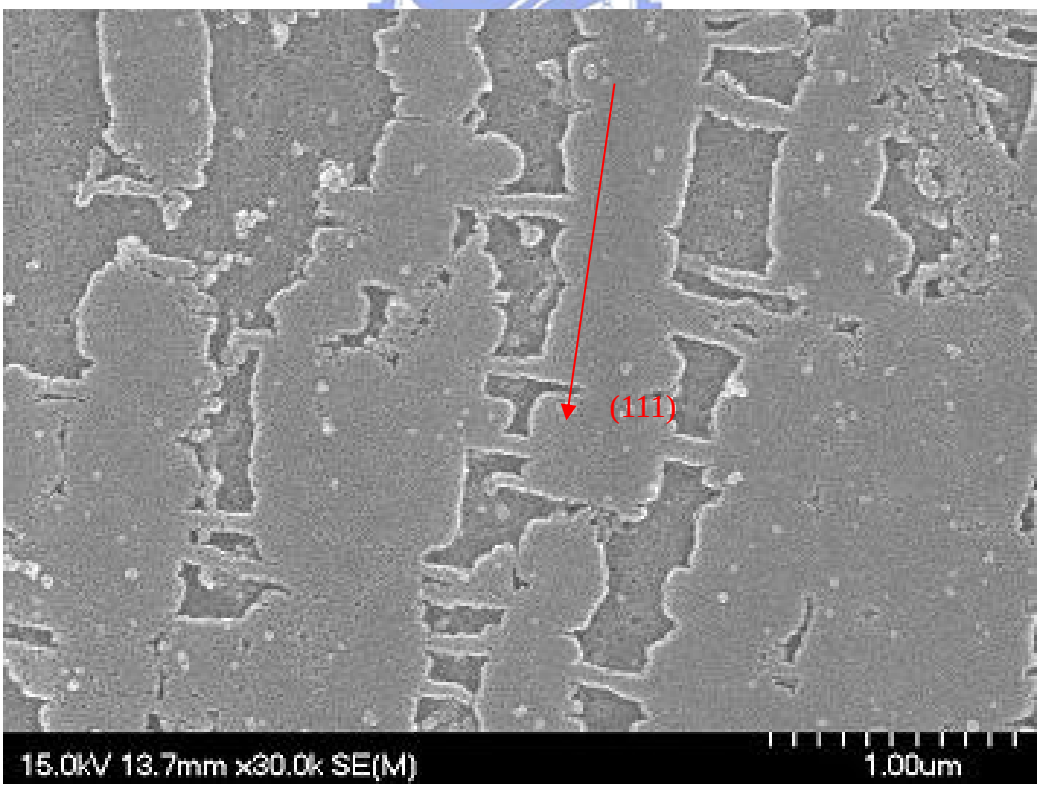


Fig. 2-12(b)

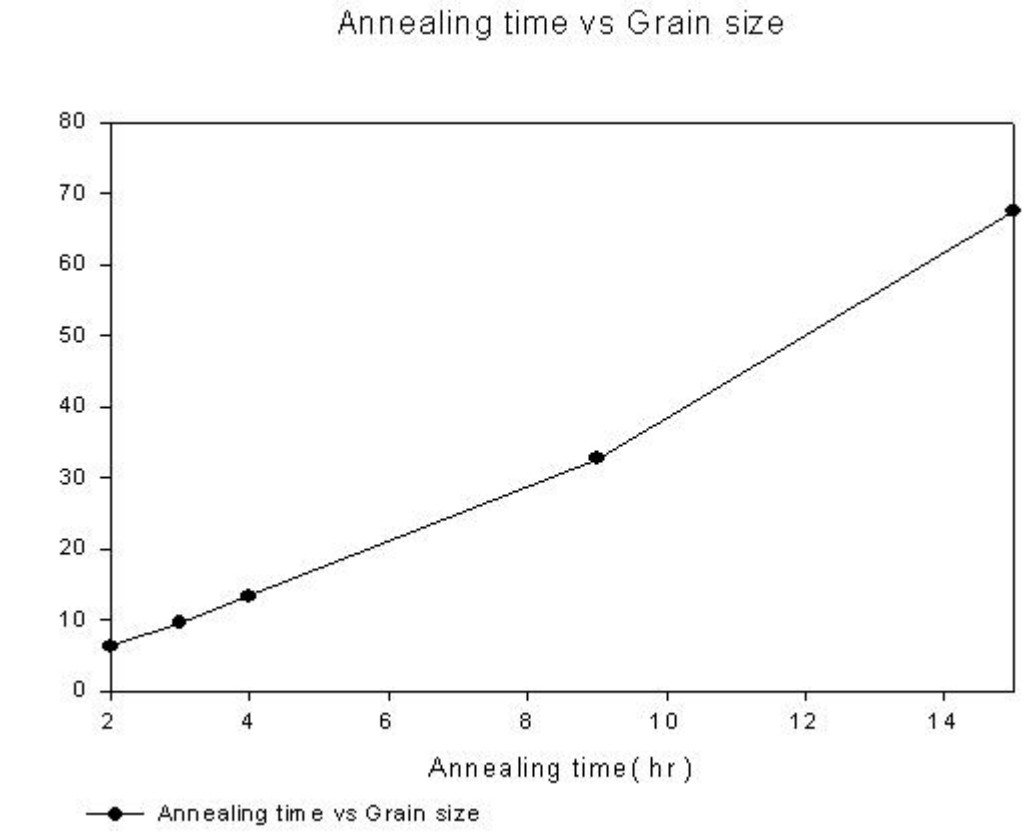


Fig. 2-13

XRD

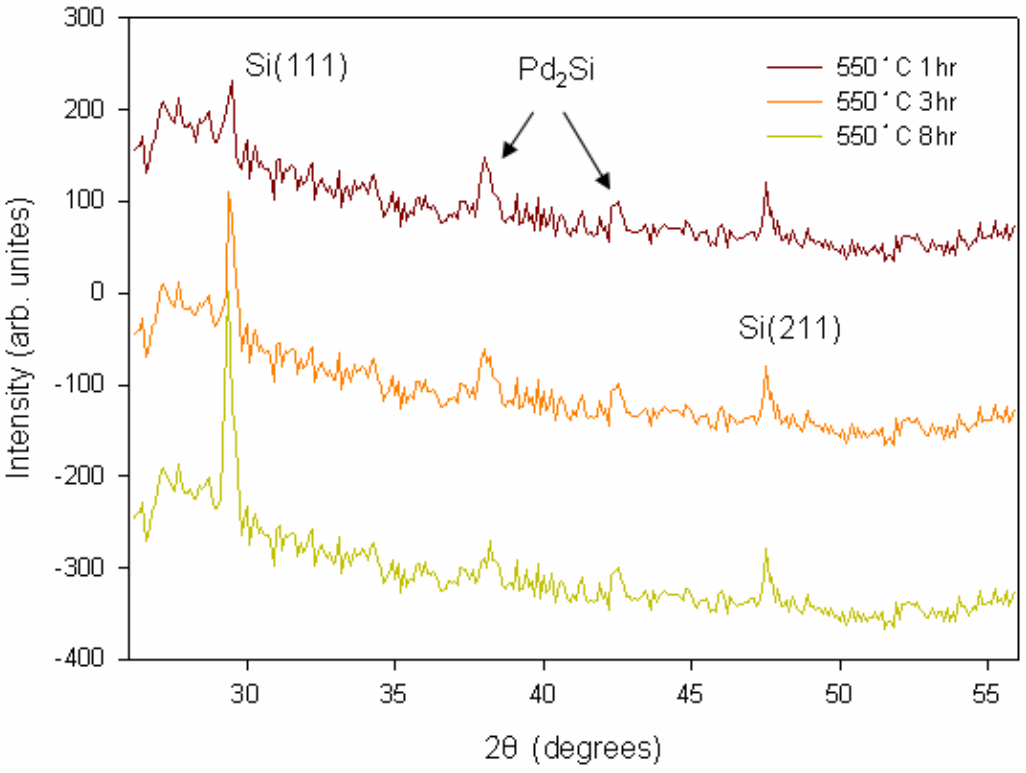


Fig. 2-14

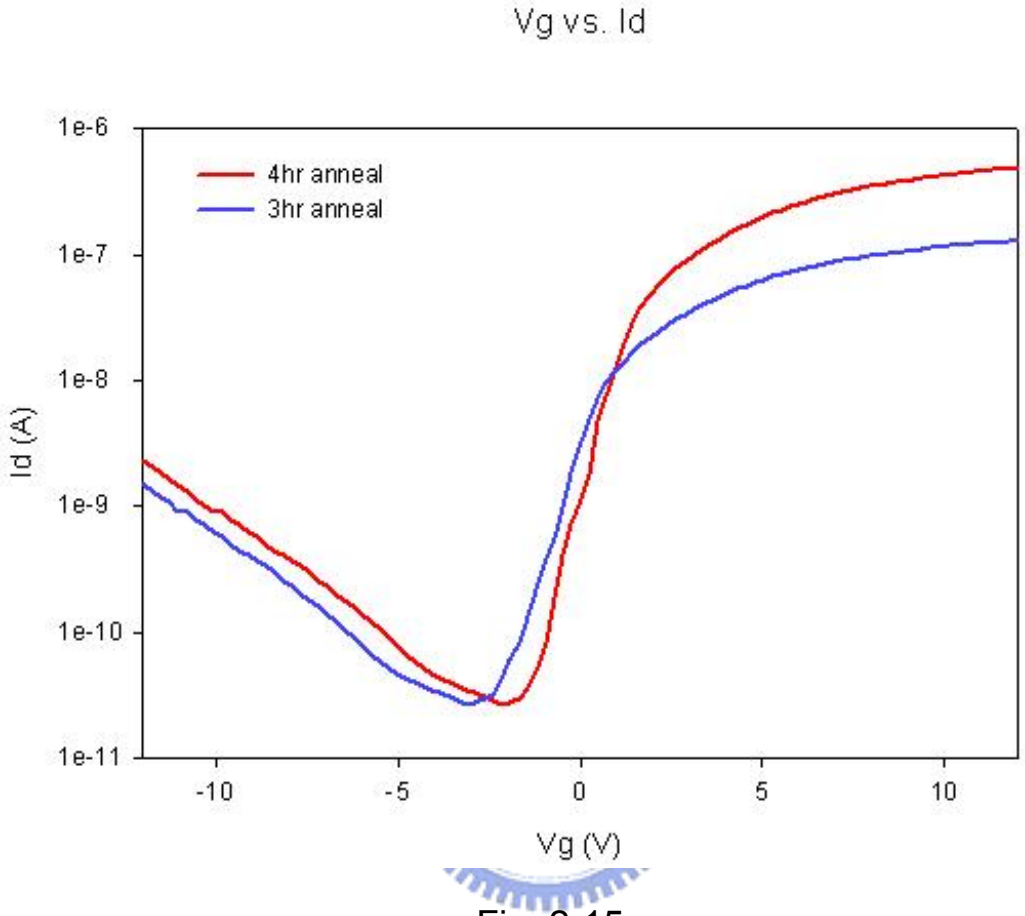

Vg vs. Id
1e-6
1e-7
1e-8
1e-9
1e-10
1e-11
Id (A)
4hr anneal
3hr anneal
-10
-5
0
5
10
Vg (V)

Fig. 2-15

Chapter 3

HREC Process

3.1 The Drawback of Excimer Laser Annealing (ELA)

As the statement former, the poly-Si TFT used ELA process has good performance, such as high mobility…etc. However, there are still several drawbacks on it as below.

(1) high cost for process and equipment maintenance:

The excimer laser beam is semi-gaussian profile, so that it must to irradiate repeatedly in order to eliminate the fine grain from uneven energy spread. Fig. 3-1 shows the situation. In Fig. 3-1(a), the semi-gaussian profile beam leads to different grain growth. However, the repeated irradiation process like Fig. 3-1(b) would increase the cost of TFT production and accelerate the aging speed of the equipment.

(2) the laser beam energy should be precisely controlled in a narrow window:

The crystallization type could be divided into three regime according to melting situation: partial melting regime as Fig. 3-2(a), complete melting regime as Fig. 3-2(b), and near-complete melting regime as Fig. 3-2(c). Among

them, near-complete melting regime could lead to lateral grain growth, but the laser energy is not stable in fact, so that it is difficult to control the laser energy in this region.

3.2 Method to Ameliorate ELA

The conventional ELC processes are usually difficult to control the location of grain, resulting in non-uniformed grain distribution. The non-uniform grain size and narrow process window make it difficult to achieve uniform TFT performance. The key technology for poly-si TFTs is required to develop a low cost, high quality, uniform polycrystalline silicon film crystallization process.

3.2.1 Sequential Lateral Solidification(SLS)

The SLS process is an excimer-laser projection-based scheme for crystallization of thin films on amorphous substrates[58][59]. This method can be used to readily produce a wide range of microstructures through manipulation of grain boundary placement within the crystallized material, as Fig. 3-3 shows.

However, low laser efficiency and complicated optical system also cause very high cost.

3.2.2 Phase Modulated Excimer Laser Annealing

This method was proposed by Masakiyo Matusmura et al. for sufficient control of the light intensity distribution[60]. For this PMELA method, a phase

shift mask is placed in the space between an excimer-laser system and the sample. When a plane wave of laser light passes through the mask, its phase is modulated, resulting in the light intensity, *I* , gradient on the sample surface due to the Fresnel diffraction. Consequently, grains grow laterally in the completely molten Si layer from the low *I* region to the high *I* region. Fig. 3-4 is the diagram of PMELA.

Nevertheless, laser phase modulated mask is difficulted to product and match on device for this method.

3.2.3 *μ*-Czochralski (grain-filter)

The *μ*-Czochralski (grain-filter) process is a promising method among the grain location-control techniques using the structural variations in the substrate by photolithography[61]-[63]. The method basically uses two phenomena: the dependence of complete melt threshold on a-Si film thickness and the occlusion of the grains by geometric selection through a constriction. As depicted in Fig. 3-5, the structure has a locally increased thickness of the a-Si film. The structure is irradiated with excimer-laser light having an energy density above the complete melt threshold of the surrounding thin *a*-Si film and below that for the thick Si. With this condition, at the end of the laser pulse, a residual fine grain poly-Si grains, will be left at the bottom of the Si column (grain filter). The unmolten Si will subsequently seed the grain growth.

However, too complicated process and need one more mask are the main disadvantages of this method.

3.3 Brief Introduction of HREC

In this thesis, a method called Heat Retaining Enhanced Crystallization, or H-REC, is reported. By capping the heat retaining layer (HRL), the additional heating from UV band semi-absorption will help to retain the silicon in molten state and decreased the cooling rate, thus long lateral grown poly silicon grain are obtained. The method has some advantages such as simple process ,and need no additional equipment and mask, so that it could reach the goal to enhance grain growth with low cost.

As Fig. 3-6, if it want to have enough absorbing coefficient to 308nm excimer laser, the material's energy bandgap must be smaller than incidence photon of 308nm energy. It is known that the energy bandgap of SiO_2 and Si_3N_4 is 9eV and 4.7eV respectively, and the absorbing wavelength is 137nm and 262nm respectively. In the past, the low energy bandgap material like SiC was added in SiO_2 or Si_3N_4 to regulate the material energy bandgap. However, it is apt to produce pollution to include C. In this thesis, we use SiON as half transparent layer plus TEOS oxide under SiON layer as anti-reflective layer which could increase laser energy efficiency to be HRL. Fig.3-7 shows the HRL capping on a-Si.

3.4 Time-Resolved Optical Reflection or Transmission(TR)

The technique was reported in 1978 by D. H. Auston et al.[64]. It makes use of different from the reflection of the solid Si and the liquid Si to observe the change of phase such as the silicon thin film melten or crystallization.

During laser annealing, the surface of *a*-Si film start to melt because of laser irradiation, and it leads to that the solid Si with lower reflection signal changes into the liquid Si with higher reflection signal from the check laser source measured. And then we could know the Si film start to melt and we could use it to measure the melt duration. Fig. 3-8 shows the instrument.

3.5 Experiment

At first, we prepared the samples which 300nm SiO2 was deposited as buffer oxide on glass substrate and 50nm *a*-Si was deposited followed. Then we divided these samples into three groups like Fig. 3-9. Among them, group(a) capped 490nm HRL and (b)(c) not. Group(c) is annealed by 8 times irradiation duration to others.

3.5.1 TR Analysis

The patterned flood irradiation, with the function of SLS, will provide a sharp localized energy density, pulse energy density varied from low to high, we can get initial explosive crystallization and complete melting, as Fig 3-10. Then we used TR analysis, optical microscope (OM) and SEM to observe the crystallization condition of the samples prepared former.

3.5.2 Recessed Channel Structure

The recessed channel structure is proposed by C.W. Lin et al.[65] as Fig. 3-11 shows. It has been reported that lateral thermal gradient could arise as a result of the heat generated at moving solid-melt interface. Similarly, when a

proper laser energy density irradiates the silicon thin film containing different thicknesses, the thin region is completely melted while the thick region is only partially melted, leaving behind islands of solid material. As a result, grain growth will come up from the residual, un-melted silicon islands in the thick region, and then stretch toward the completely melted thin channel until small grains, which homogeneously grow in the channel region, hinder the extending grains.

In this thesis, we try to combine HREC with recessed channel structure, and we expect to more enhance the lateral grain growth. Our detail procedure is below:

(1) 5500 Å wet oxide was deposited on 6 inch wafer by LPCVD as buffer oxide after RCA clean.

(2) 500 Å *a*-Si was deposited by LPCVD.

(3) Source/Drain patterned by photolithography process.

(4) 500 Å *a*-Si was deposited by LPCVD.

(5) 5800 Å SiON and 1000 Å TEOS were deposited by LPCVD as HRL

(6) ELA

Fig. 3-12 shows our structure.

3.6 Results and Discussion

3.6.1 TR Analysis

In Fig. 3-13, we discover that the a-Si film capped HRL on it could indeed increase the melting duration when excimer laser irradiated. On the other hand,

when the samples are both without HRL on it, the duration of laser irradiation extended could lead to increase of the melting duration, too. Moreover, the greatest grain growth is observed on HRL capped sample which has the longest melting duration through OM images.

Fig. 3-14 shows the TR analysis for HRL capped sample after different laser energy annealing. The oscillation at the onset of laser irradiation indicates the interference effect from explosive crystallization, which was less significant at higher energy densities[66]. We discover easily that higher laser energy irradiation cause increase of the melting duration.

Fig. 3-15~Fig. 3-17 show the SEM images as group(a), (b), and (c), respectively. The greatest lateral grain growth is HRL capped sample, and this resule conforms with the statement former.

Finally, we draw a “melt duration vs. laser energy” diagram as Fig. 3-18. The similar slope of uncapped samples indicates the same cooling rate, and the dramatically increased slope of HREC samples provides a evidence of Heat Retaining Capping enhancement. And we also draw a “grain size vs. laser energy” diagram as Fig. 3-19. Compare with them, we find the grain size curve exhibits a similar behavior to melt duration. This similarity could be explained by thermodynamic correlation of nucleation and lateral growth.

3.6.2 Recessed Channel Structure

Fig. 3-20 shows OM image of lateral grain growth around the pattern.

From the SEM image as Fig. 3-21, the lateral grain size is about 2.5μm.

3.7 Summary

In this chapter, we provide the method of capping the HRL on *a*-Si film to enhance the grain growth after ELA. With the TR analysis, it is proved that the melting duration is indeed increase during laser irradiation and the grain growth is better followed. And the recessed channel structure applied with HREC is successfully, too. We observe the 2.5μm lateral grain growth on channel region.

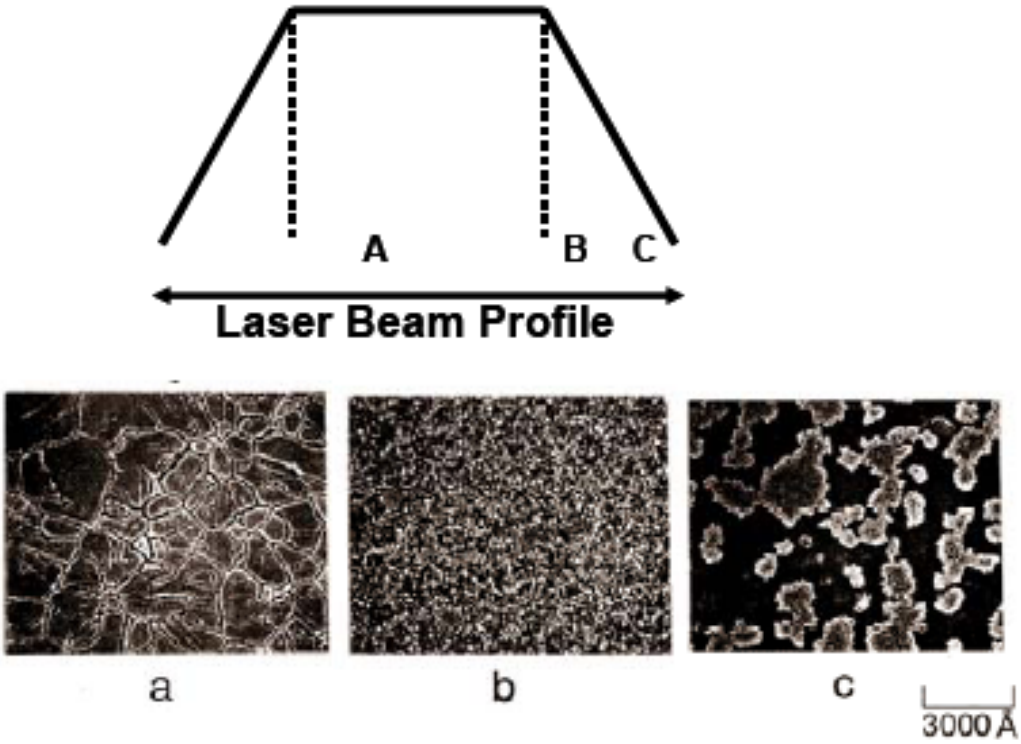


Fig. 3-1(a)

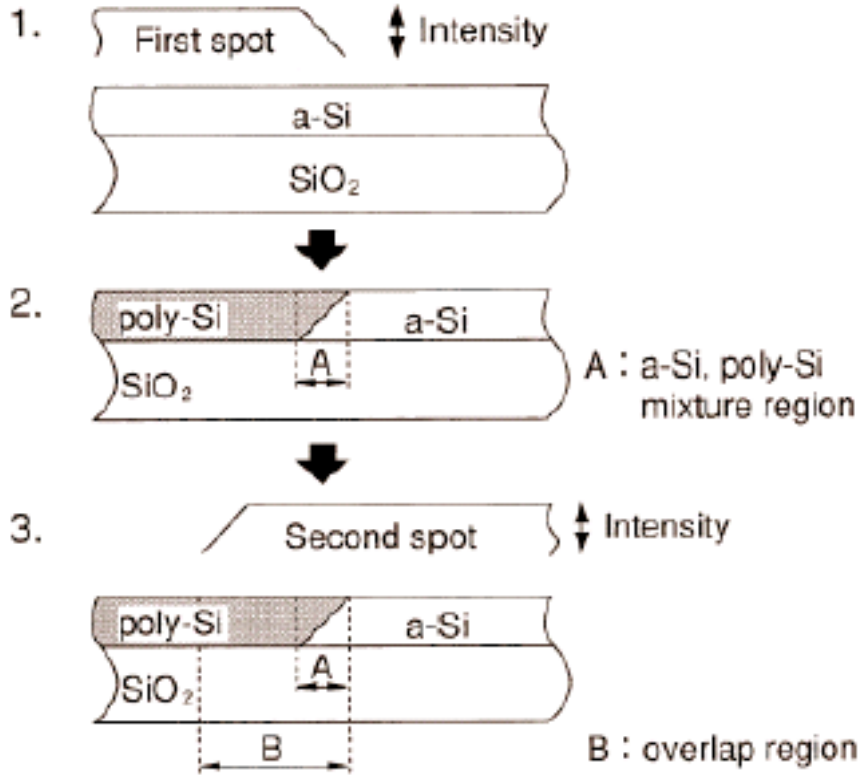
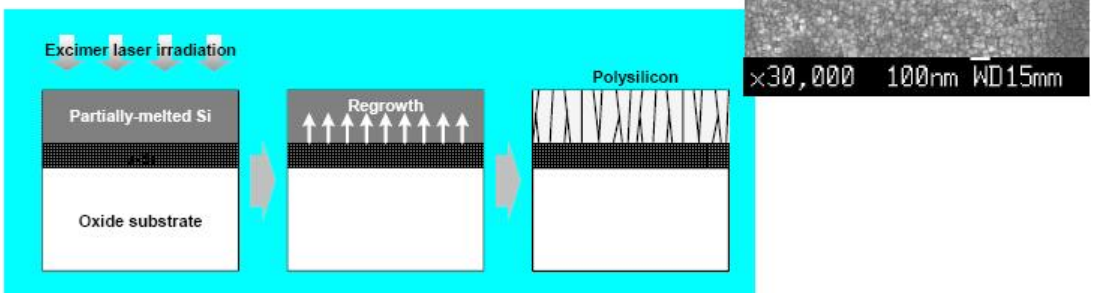


Fig. 3-1(b)

- Melt depth < film thickness
- Fine-grained and small-grained poly-Si
- Explosive crystallization, vertical regrowth



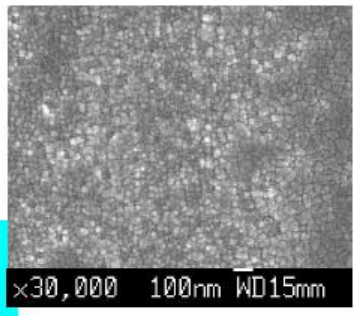
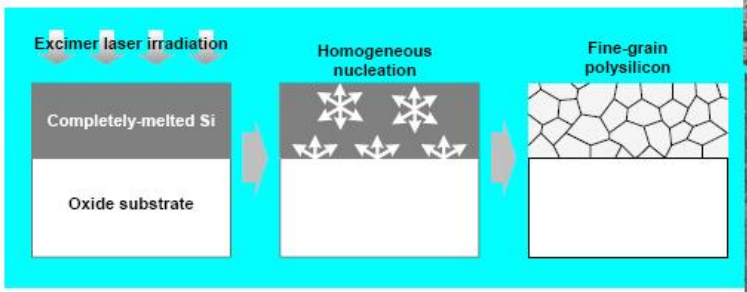
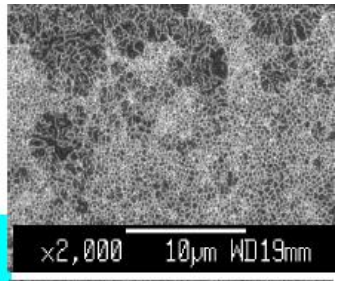


Fig. 3-2(a)

- No non-melted Si remains
- Deep supercooling followed by nucleation and growth of solid





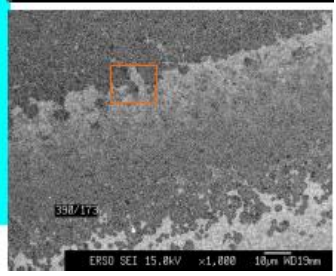
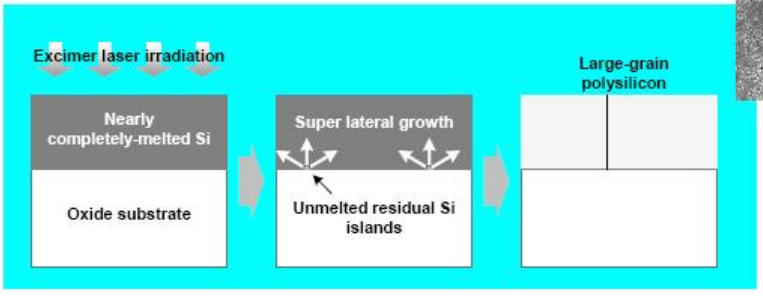


Fig. 3-2(b)

- Non-melted Si islands survive
- Significant lateral growth proceeds before impinging



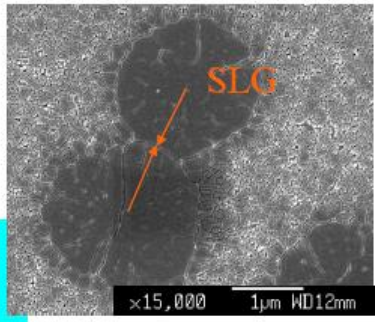


Fig. 3.2(c)

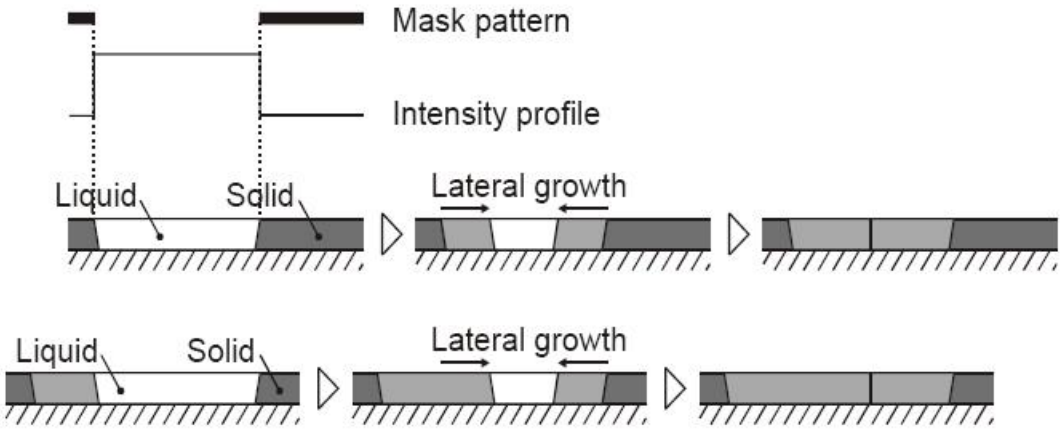


Fig. 3-3

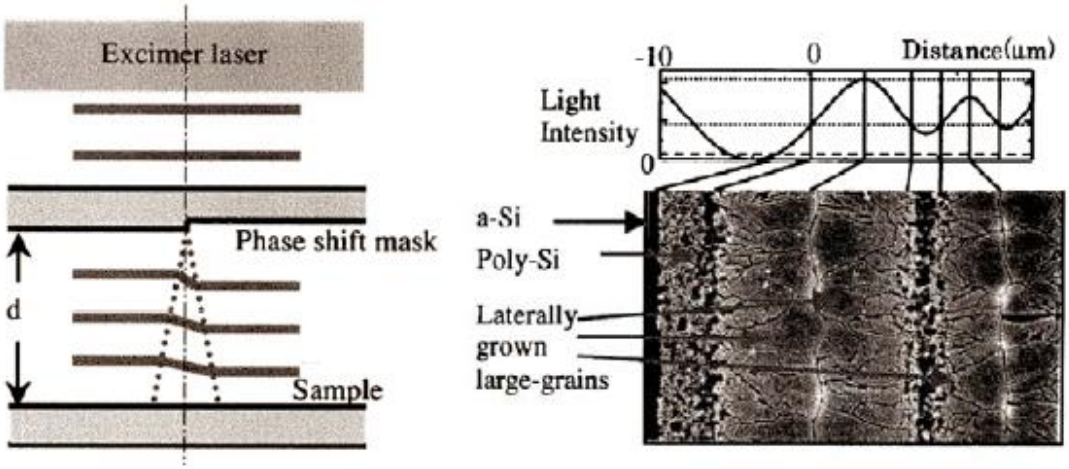


Fig. 3-4

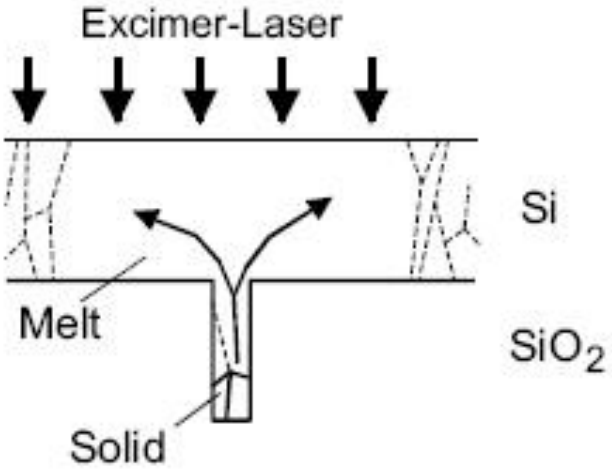


Fig. 3-5

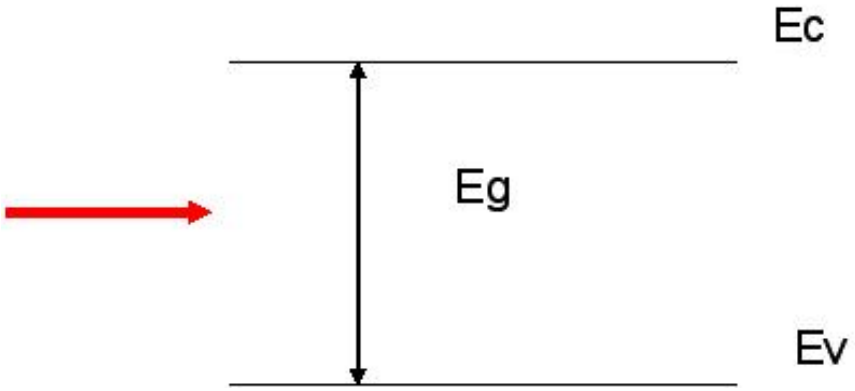


Fig. 3-6

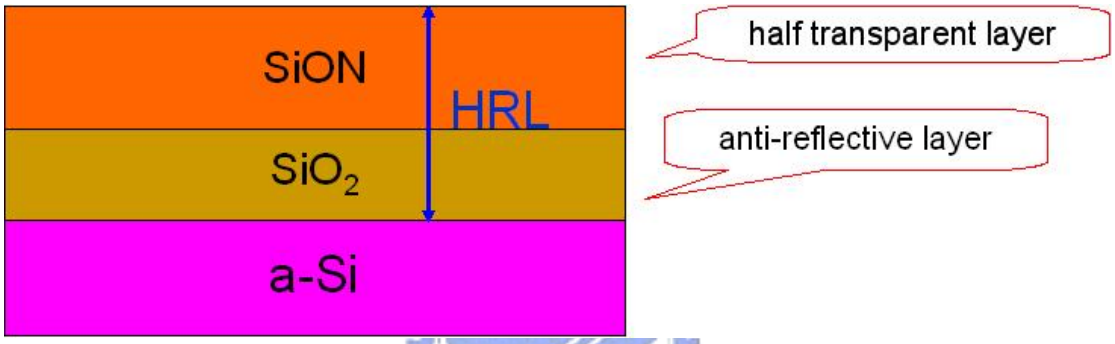
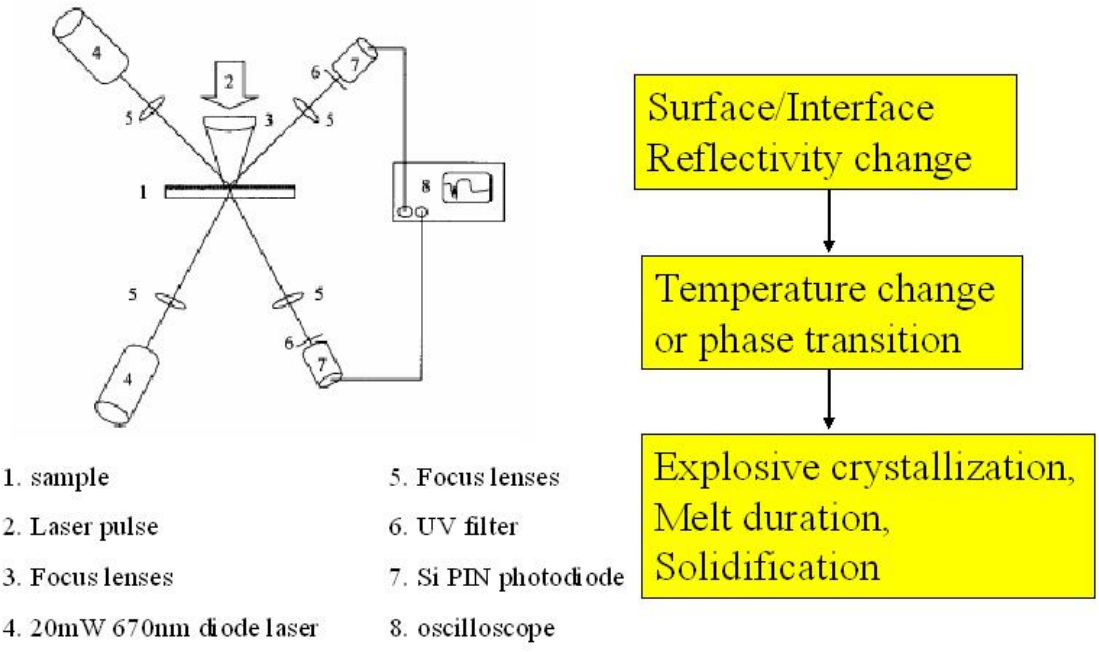


Fig. 3-7



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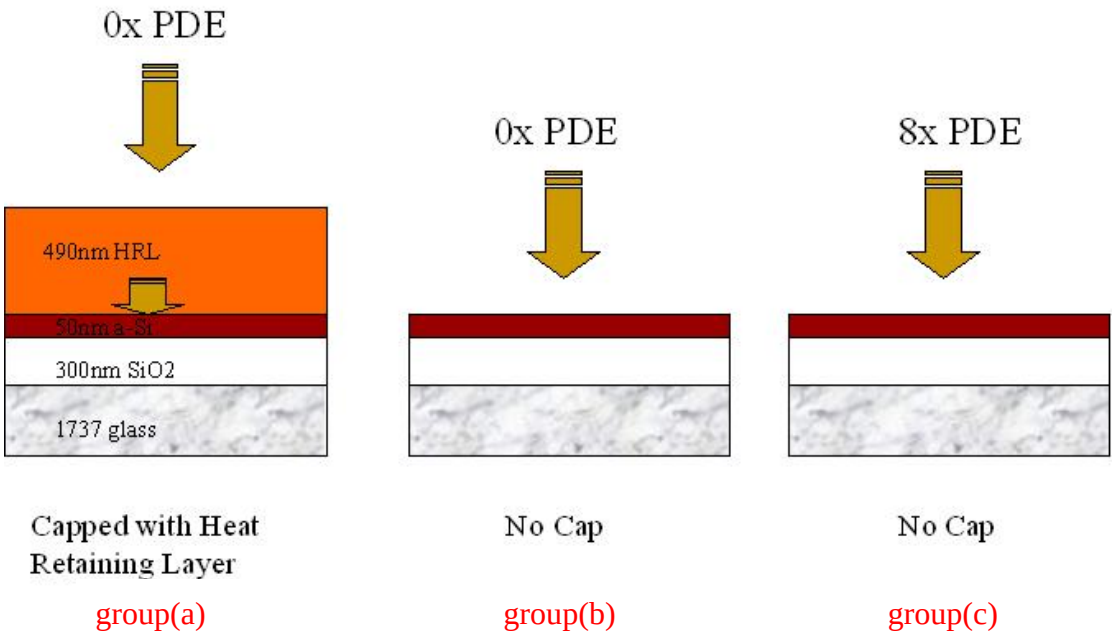


Fig. 3-9

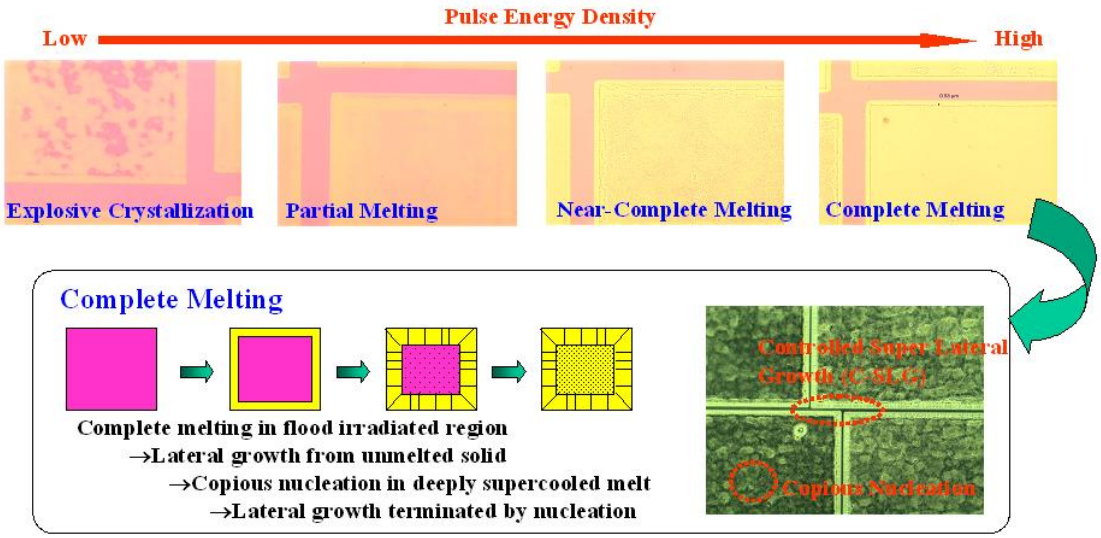


Fig. 3-10

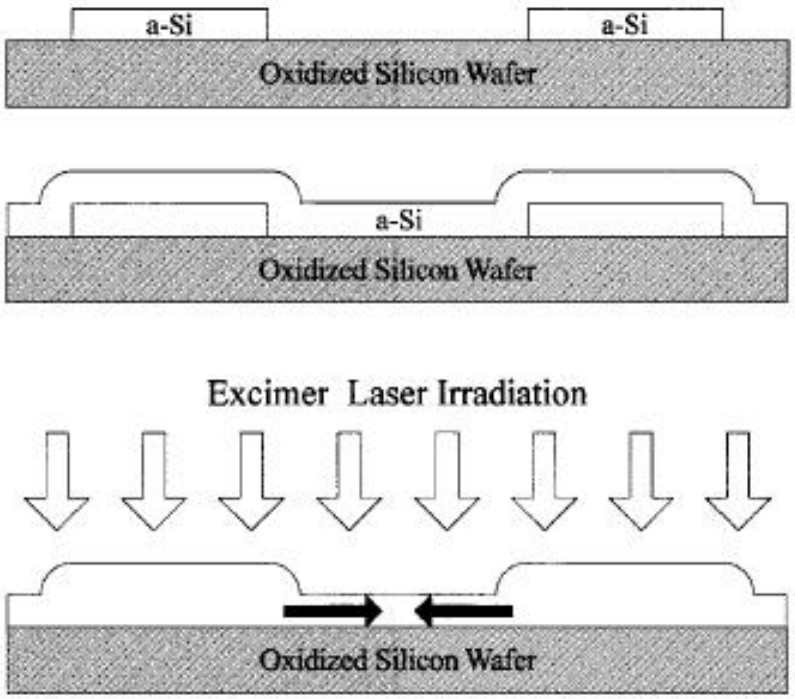


Fig. 3-11

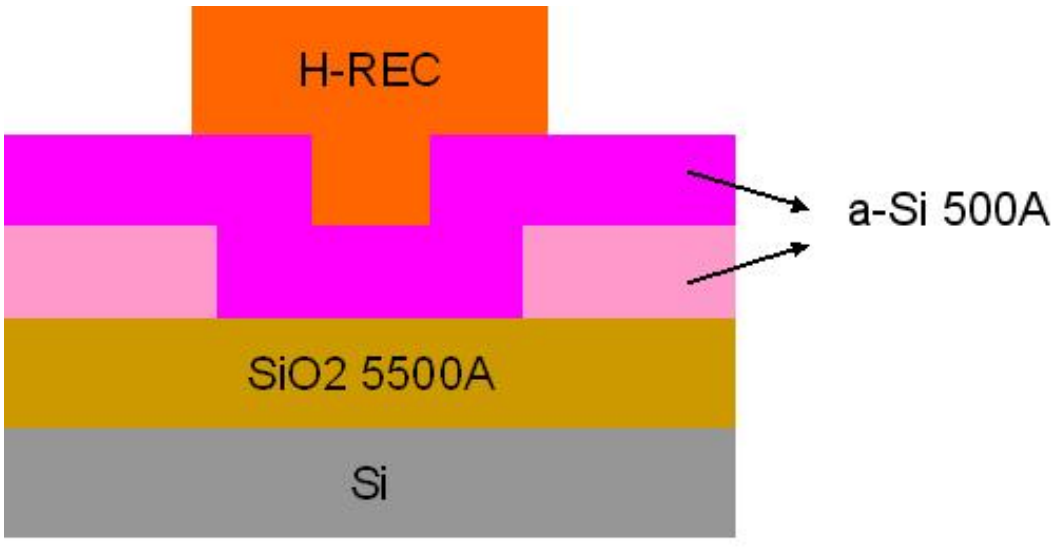


Fig.3-12

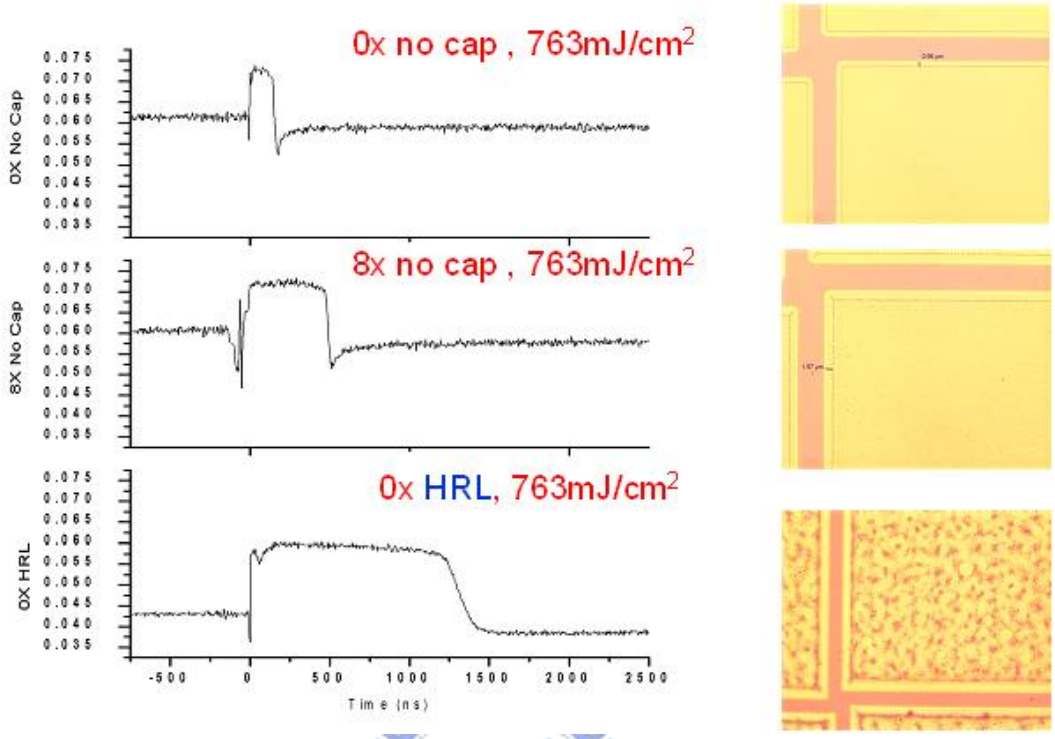


Fig. 3-13

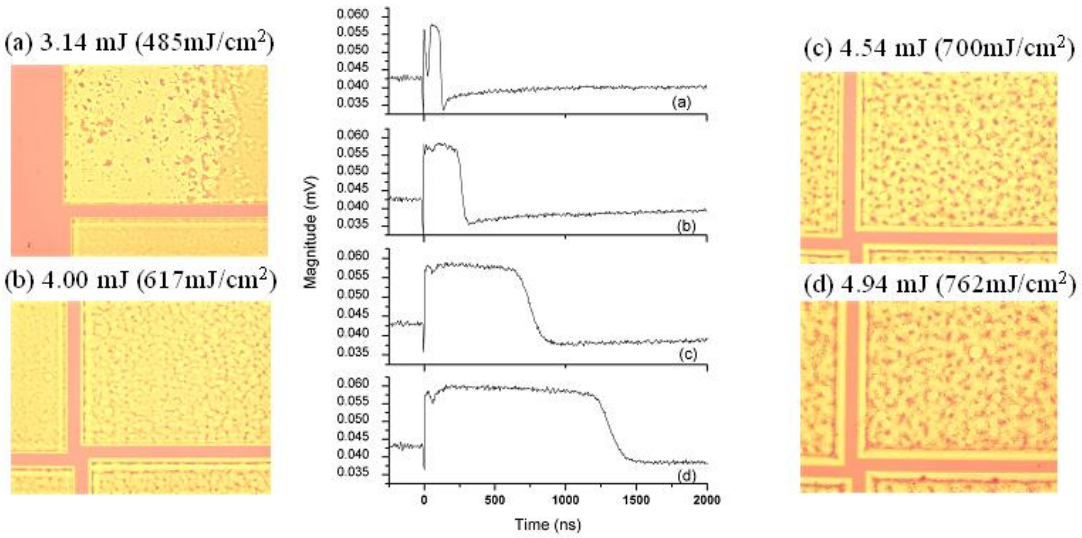
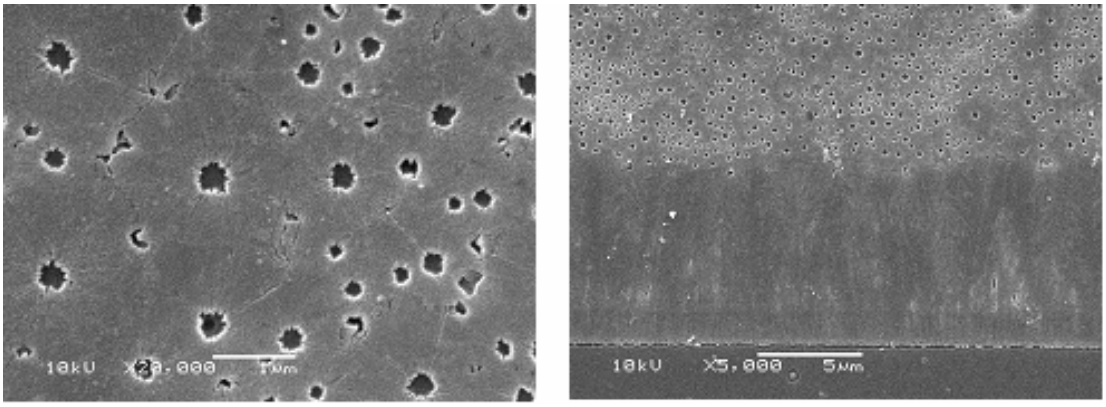


Fig. 3-14



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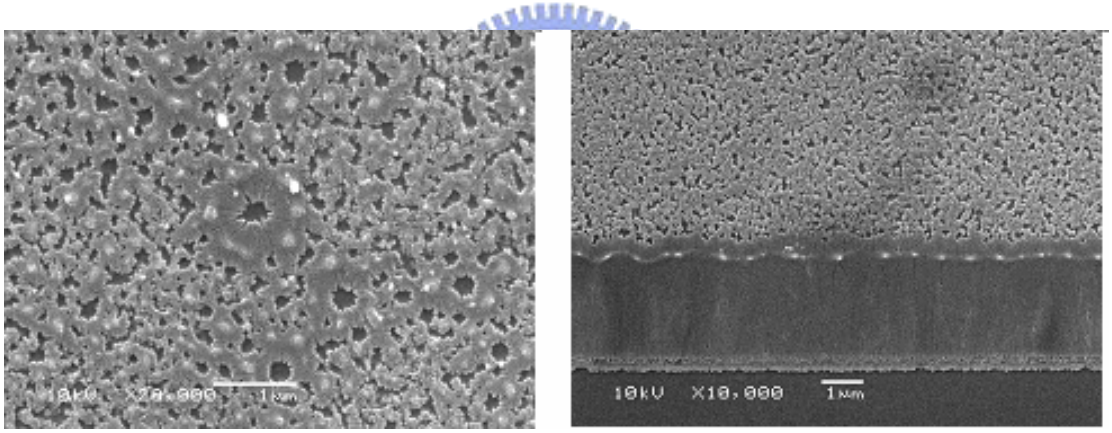

Fig. 3-16

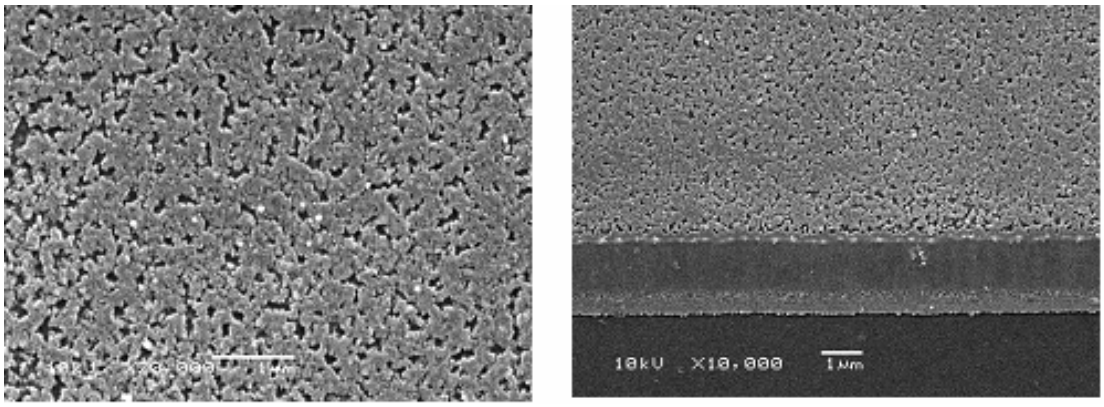

Fig.3-17

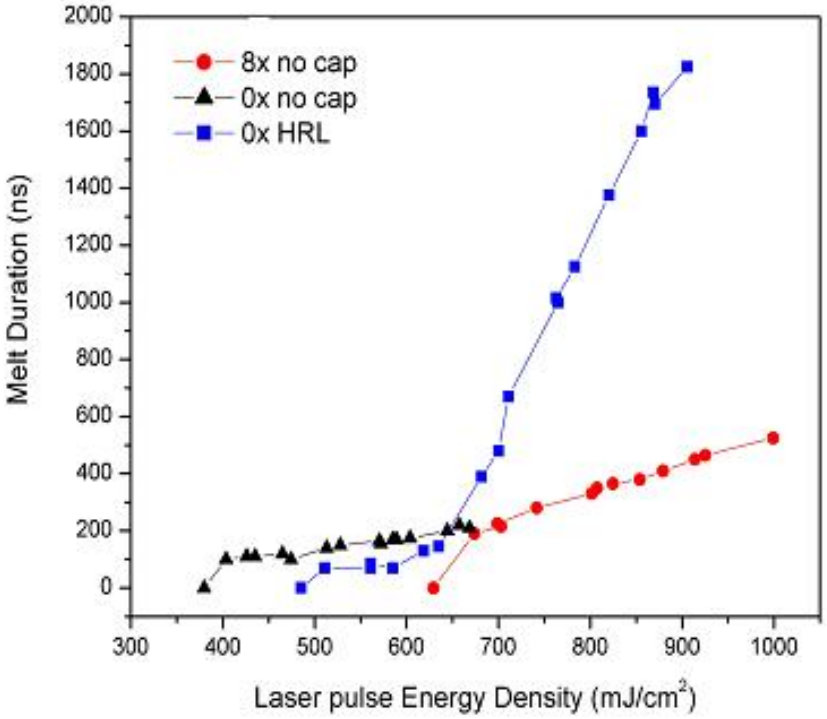

Fig. 3-18

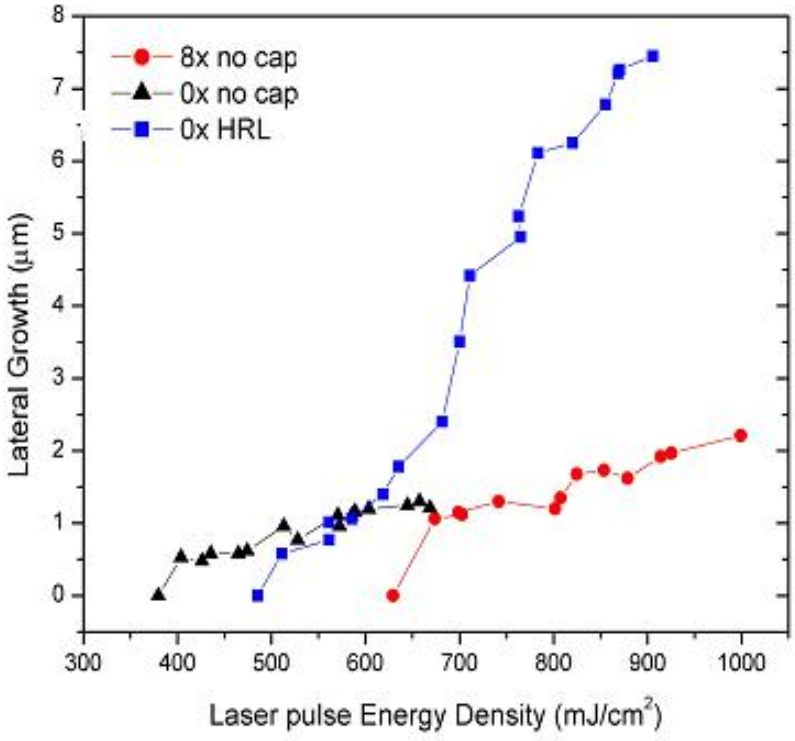

Fig. 3-19

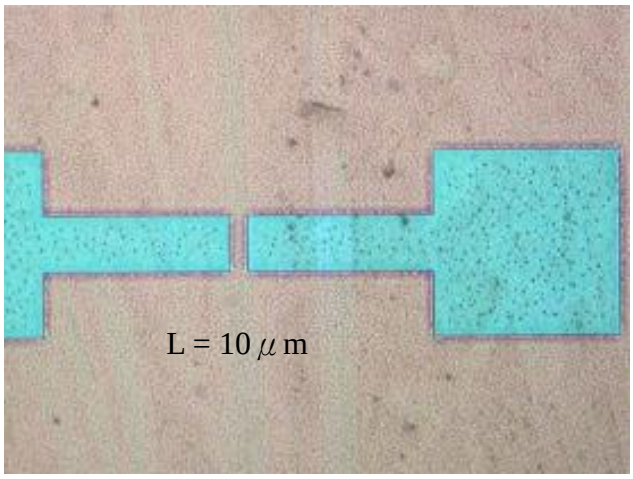

Fig. 3-20(a)

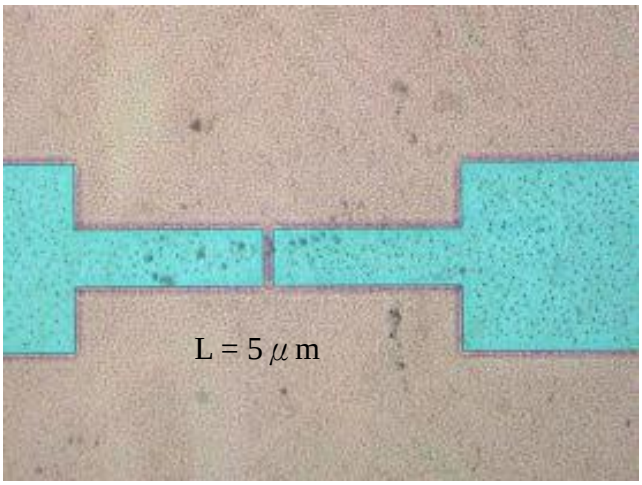

Fig. 3-20(b)

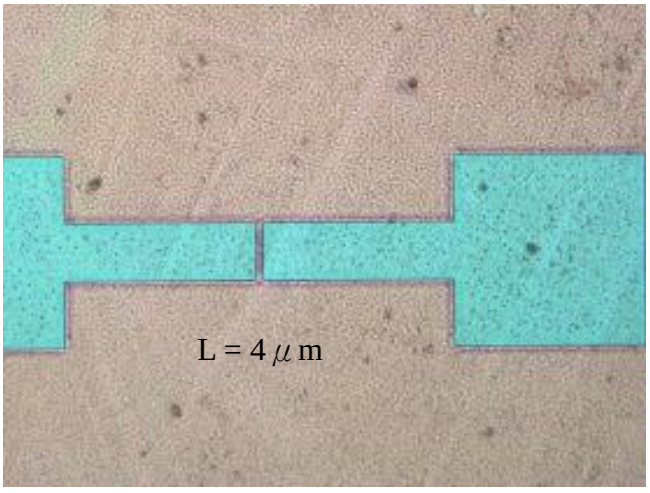

Fig. 3-20(c)

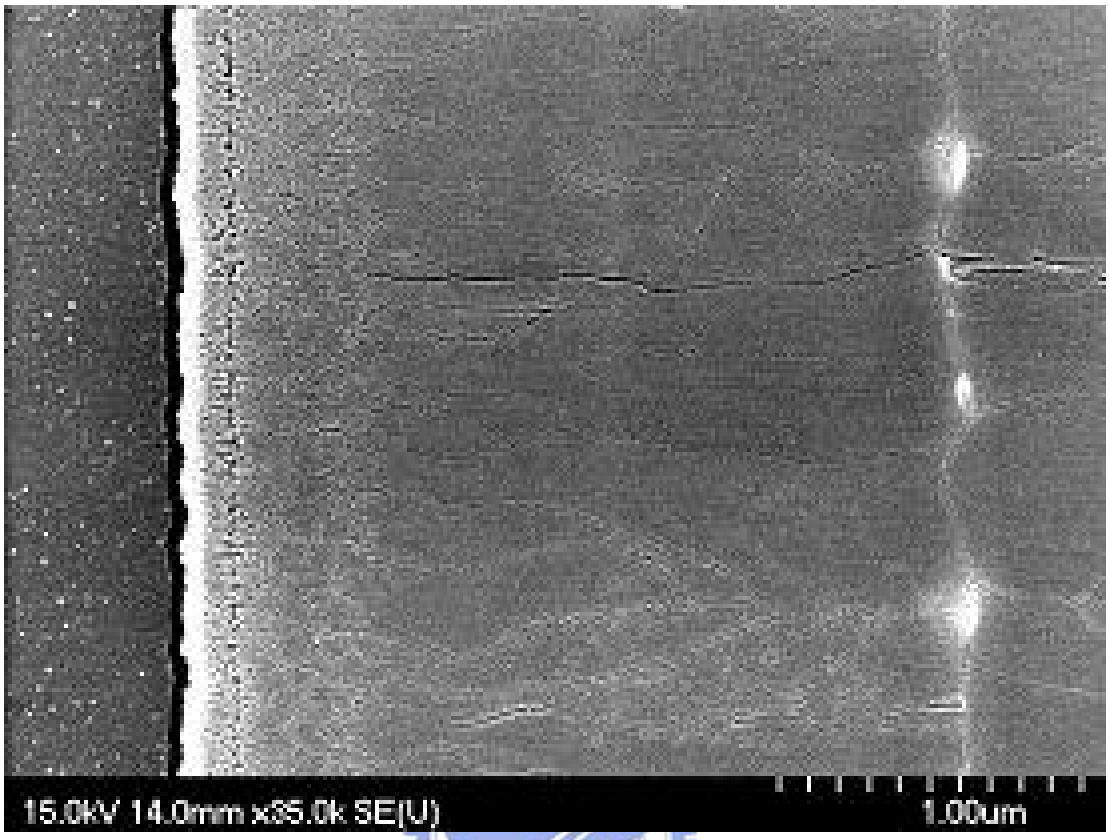

Fig. 3-21

Chapter 4

Conclusion

In this thesis, we propose one crystallization process for SPC and ELC respectively to produce bottom gate poly-Si TFT. In SPC, we used spin coating the nano Pd solution to get MIC/MILC, and in ELC, we deposited the HRL to enhance grain growth in ELA.

In Pd MIC/MILC, we spin coated nano Pd solution on a-Si film, and we get the poly film successfully after furnace annealing. To analyze with Raman and SEM , we observed the poly film could be formed in 450°C by this process and the grain growth rate is 4μm/hr approximately, which is ten times to conventional SPC. Finally, we also applying this process to produced a bottom gate poly-Si TFT which has 67(cm2/Vs) mobility successfully.

In ELC, we deposited SiON as HRL capped on a-Si layer because of its half-transparent characteristic to retain heat, and we analyzed with “Time-Resolved Optical Reflectivity” to observe the crystallization condition after ELA process. With analysis data, the phenomenon that capping HRL will increase the melting duration is well confirmed. It is also verified that this process will enhance the grain growth, even to achieve 2.5μm lateral grain growth in channel region from the experiment of the recessed channel structure applied to HREC process. Further more, we might design the bottom gate poly-Si TFT which is based on recessed channel structure with HREC

process, like Fig. 4-1 shows. We expect the structure has some advantages below: First, Source/Drain activation and ELA could be finished at the same time. And the HRL could be used as passivation layer. The most important thing is there would be the great lateral grain growth in channel region with one main grain boundary in center, so that it would have better characteristic like mobility or on-current.

Now, the LCD market is popular day by day, we hope that we could provide a way to simplify the process and lower the cost in this thesis.

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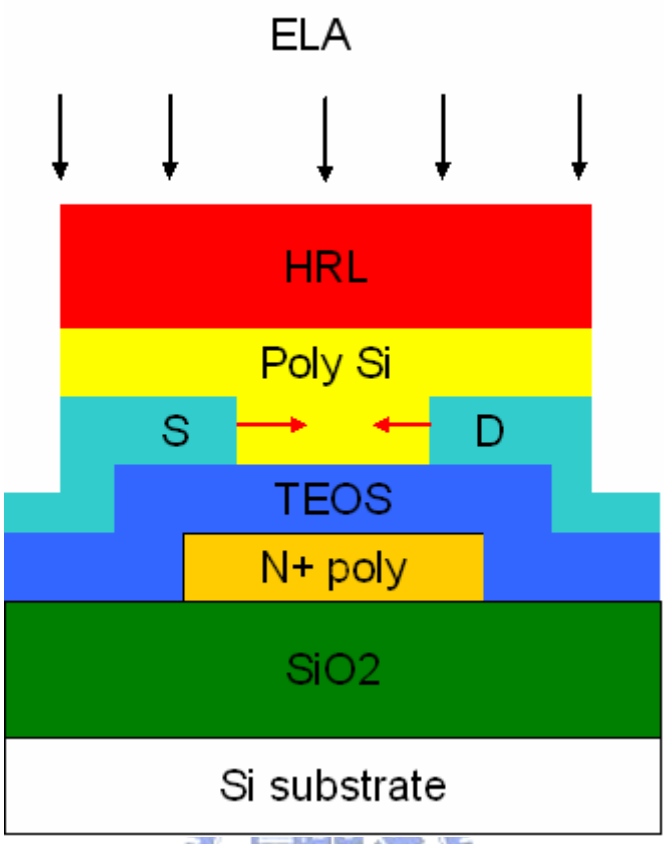

Fig. 4-1

Reference

[1] N. Yamauchi, and R. Reif, “Polycrystalline silicon thin films processed with silicon ion implantation and subsequent solid-phase crystallization: Theory, experiments, and thin-film transistor applications,” *J. Appl. Phys.*, vol. 75, pp. 3235-3257, 1994.

[2] Y. J. Choi, W. K. Kwak, K. S. Cho, S. K. Kim, and Jin Jang, “Hydrogenated amorphous silicon thin-film transistor with a thin gate insulator, “*IEEE Electron Device Lett.,* vol. 21, no. 1, pp. 18-20, 2000.

[3] W. J. Sah, J. L. Lin, and S. C. Lee, “High-performance a-Si:H thin-film transistor using lightly doped channel, “*IEEE Trans. Electron Devices*, vol. 38, no. 3, pp. 676-678, 1991.

[4] K. Khakzar, and E. H. Lueder, “Modeling of amorphous-silicon thin-film transistors for circuit simulations with SPICE, “*IEEE Trans. Electron Devices*, vol. 3, no. 6, pp. 1428-1434, 1992.

[5] Z. Shengdong, Z. Chunxiang, J. K. O. Sin, J. N. Li, and P. K. T. Mok, “Ultra-thin elevated channel poly-Si TFT technology for fully-integrated AMLCD system on glass, “*IEEE Trans. Electron Devices*, vol. 47, no. 3, pp. 569-575, 2000.

[6] I. W. Wu, “Low temperature poly-Si TFT technology for AMLCD’s,” *Proc. 1995 Int. Workshop on Active-Matrix Liquid-Crystal Displays*, Osaka, Japan, 1995.

[7] C. H. Fa and T. T. Jew, “The polysilicon insulated-gate field-effect transistors,” IEEE Trans. Electron Devices, vol. 13, no. 2, p. 290, 1966.

[8] Y. Aoki, T. Iizuka, M. Karube, T. Tsunashima, S. Ishizawa, K. Ando, H. Skurai, T. Ejiri, T.Nakzono, M. Kobayashi, H. Sato, N. Ibaraki, M. Sasaki, N. Harada, SID 99 Dig.,p. 176,1999.

[9] Mimura, N. Knishi, K. Ono, J-I Ohwada, Y. Hosokawa, Y. A. Ono, Y. Suzuki, k. Miyata,and H. Kawakami, IEEE Trans. Elec. Dev., 36, p. 351, 1989.

[10] G. Lewies, D. D. Lee, and R. H. Bruce, IEEE J. Solid-State Circuits, 27, p. 1833, 1992.

[11] G. Lewis, I-W Wu, T. Y. Huang, A. Chiang, and R. H. Bruce, IEDM 90, p. 843, 1990.

[12] T. Marita, Y. Yamamoto, M. Itoh, H. Yoneda, Y. Yamane, S. Tsuchimoto, F. Funa, and K.Awane, IEDM Tech. Dig., p. 841, 1995.

[13] Simon W-B. Tam, Yojiro Matsueda, Hiroshi Maeda, Mutsumi Kimura, Tatsuya Shimoda, and Piero Migliorato, IDW ’99, Sendai Int. Center, Sendai, Japan, 1999.

[14] H. Gamo, S. Kanemaru, and J. Itoh, Appl. Phys. Lett. 73, p. 1301 (1998)

[15] H. Gamo, S. Kanemaru, and J. Itoh, Jpn. Appl. Phys. 37, p. 7134 (1998)

[16] H. C. Cheng, W. K. Hong, F. G. Tarntair, K. J. Chen, J. B. Lin, K. H. Chen and L. C. Chen, Electrochem. Solid-State Lett., 4 p.H5 (2001)

[17] S. D. S. Malhi, H. Shichijo, S. K. Banerjee, R. Sundaresan, M. Elahy, G. P. Polack, W. F.Richardson, A. H. Shah, L. R. Hite, R. H. Womack, P. K. Chatterjee, and H. W. Lam, IEEE Trans. Elec. Dev., 32, p. 258, (1985).

[18] T. Yamanaka, T. Hashimoto, N. Hasegawa, T. Tanaka, N. Hashimoto, A. Shimizu, N. Ohki, K. Ishibashi, K. Sasaki, T. Nishida, T. Mine, E. Takada, and T. Nagano, IEEE Trans. Elec.Dev., 42, p. 1305, (1995).

[19] K. Yoshizaki, H. Takahashi, Y. Kamigaki, T. Yasui, K. Komori, and H. Katto, ISSCC Digest of Tech. Papers, p. 166, (1985).

[20] N. D. Young, G. Harkin, R. M. Bunn, D. J McCulloch, and I. D. French, IEEE Trans. Elec, Dev., 43, p.1930, (1996).

[21] T. Kaneko, Y. Hosokawa, M. Tadauchi, Y. Kita, and H. Andoh, IEEE Trans, Elec. Dev., 38, p.1086, (1991).

[22] Y. Hayashi, H. Hayashi, M. Negishi, T. Matsushita, IEEE Solid State Circuit Conference (ISSCC), p.266, (1998).

[23] N. Yamauchi, Y. Inaba, and M. Okamura, IEEE Photonic Tech. Lett., 5, p.319, (1993)

[24] V. Subramaniam, P. Dankoski, L. Degertekin, B. T. K. Yakub, and K. C. Saraswat, “Controlled two-step solid-phase crystallization for high-performance polysilicon TFT’s, “*IEEE Electron Device Lett.,* vol. 18, no. 8, pp. 378-380, 1997.

[25] K. S. Nam, Y. H. Somg, J. T. Baek, H, J, Komg, and S.S. Lee, “Thin-film transistors with polycrystalline silicon prepared by a new annealing method,” *Jan. J. Appl. Phys.*, vol. 32, no. 5, pp. 1908-1912, 1993.

[26] A. Nakamura, F. Emoto, E. Fujii, and A. Tamamoto “A high-reliability, lowoperation-voltage monolithic active-matrix LCD by using advanced solid-phase growth technique,” *IEDM Tech. Dig.*, pp. 847, 1990.

[27] R. Carluccio, J. Stoemenos, G. Fortunato, D, B, Meakin, and M. Bianconi, “Microstructure of polycrystalline silicon films obtained by conbined furnace and laser annealing, “*Appl. Phys. Lett.*, vol. 66, no. 11, pp.1394-1396, 1995.

[28] S. Seki, O. Kogure, and B. Tsujiyama, IEEE Elec. Dev. Lett., 8, p. 368, (1987)

[29] N. Kubo, N. Kusumoto, T. Inushima, and S. Yamazaki, “Characterization of polycrystalline-Si thin film transistors fabricated by excimer laser annealing method,” *IEEE Trans. Electron Devices,* vol. 40, pp. 1876-1879, 1994.

[30] M. Cao, S. Talwar, K. J. Kramer, T. W. Sigmon, and K. C. Saraswat, “A high-performance polysilicon thin-film transistor using XeCl excimer laser crystallization of pre-patterned amorphous Si films,” *IEEE Trans. Electron Devices,* vol. 43, no. 4, pp. 561-567, 1996.

[31] G. K. Giust and T. W. Sigmon, “High-performance thin-film transistors fabricated 36 using excimer laser processing and grain engineering,” *IEEE Trans. Electron Devices,* vol. 43, no. 4, pp. 561-567, 1996.

[32] T. Serikawa, and F. Omata, “High-mobility poly-Si TFTs fabricated on flexible stainless-steel substrates, “*IEEE Electron Device Lett.,* vol. 20, no. 11, pp. 574-576, 1999.

[33] J. H. Joo, “Low-temperature polysilicon deposition by ionized magnetron sputtering,” J. Vac. Sci. Technol. A18, 2006-2011 (2000).

[34] Y. Mishima, M. Takei, T. Uematsu, N, Matsumoto, T. Kakehi, U. Wakino, and M. Okabe, “Polycrystalline silicon formed by ultrahigh-vacuum sputtering system,” J. Appl. Phys. 78, 217-223 (1995).

[35] D. B. Meakin and W. Ahmed, “LPCVD of in-situ phosphorous doped polysilicon from PH3/Si2H6 mixtures,” 1986 Electrochemical Society Meeting (San Diego, Oct. 1986), abstract 267, 398-399 (1986).

[36] M. Bonnel, N. Duhamel, L. Haji, B. Loisel, and J. Stoemenos,77 “Ploycrystalline silicon thin-film transistors with two step annealing

process,” IEEE Electron Device Lett. 14, 551-553 (1993).

[37] S. D. Brotherton, D. J. McCulloch, J. P. Gowers, J. R. Ayres, and M. J. Trainor, “Influence of melt depth in laser crystallized poly-Si thin film transistors,” J. Appl. Phys. 82 4086-4094 (1997).

[38] S. Morozumi, K. Oguchi, S. Yazawa, T. Kodaira, H. Ohshima, and T. Mano, “B/W and color LC video display addressed by poly-Si TFTs,” Society for Information Display (SID) Dig. 156 (1983).

[39]G. Ottaviani, D. Sigurd, V. Marrello, J. W. Mayer, and J. O. McCaldin, J. Appl. Phys. 45, 1730, 1974.

[40]T. J. Konno and R. Sinclair, Mater. Sci. Eng., A 179/180, 426 ~1994!.

[41] L. Hultman, A. Robertsson, H. T. G. Hentzell, and I. Engstrom, J. Appl. Phys. 62, 3647, 1987.

[42] G. Radnoczi, A. Robertsson, H. T. G. Hentzell, S. F. Gong, and M.-A Hasan, J. Appl. Phys. 69, 6394, 1991.

[43]S. F. Gong, H. T. G. Hentzell, A. E. Robertsson, L. Hultman, S.-E. Hornstrom, and G. Radnoczi, J. Appl. Phys. 62, 3726, 1987.

[44]E. Nygren, A. P. Pogany, K. T. Short, J. S. Williams, R. G. Elliman, and J. M. Poate, Appl. Phys. Lett. 52, 439, 1988.

[45]R. J. Nemanichi, C. C. Tsai, M. J. Thompson, and T. W. Sigmon, J. Vac. Sci. Technol. 19, 685, 1981.

[46] G. Liu and S. J. Fonash, Appl. Phys. Lett. 55, 660, 1989.

[47] R. J. Nemanichi, R. T. Fulks, B. L. Stafford, and H. A. Vanderplas, J. Vac. Sci. Technol. A 3, 938, 1985.

[48] Y. Kawazu, H. Kudo, S. Onari, and T. Arai, Jpn. J. Appl. Phys., Part 1 29, 2698, 1990.

[49] C. Hayzelden and J. L. Batstone, J. Appl. Phys. 73, 8279 , 1993.

[50] T. Hempel and O. Schoenfeld, Solid State Commun. 85, 921 , 1993.

[51] S. W. Russell, J. Li, and J. W. Mayer, J. Appl. Phys. 70, 5153 , 1991.

[52] J. M. Poate, D. C. Jacobson, F. Priolo, and M. O. Thompson, Mater. Res. Soc. Symp. Proc. 128, 533 (1989).

[53]. S. W. Lee, Y. Jeon, and S. K. Joo, “Pd induced lateral crystallization of amorphous Si thin films”, Appl. Phys. Lett, vol 66, pp.1671- 1673, 1995.

[54]. S. W. Lee, Byung-Il Lee, T. K. Kim and S. K. Joo, “Pd2Si-assisted crystallization of amorphous silicon thin films at low temperature”, J Appl. Phys., vol 85, pp.7180 –7184, 1999.

[55] Y. S. Kim, H. U. Oh, and S. K. Joo, in *Thin Film Materials, Processes, and Reliability*, G. S. Mathad, H. S. Engelhardt, and K. Kondo, Editors, PV 2004–20, p. 147, The Electrochemical Society Proceedings Series, Pennington, NJ, In press.

[56]. W. D. Buckley and S. C. Moss, Solid State Electron. Vol. 15, 1331 (1972).

[57] Young-Su Kim,z Min-Sun Kim, and Seung-Ki Joo, *Journal of The Electrochemical Society,* 153 (2) H19-H22 (2006).

[58].R. S. Sposili and J. S. Im, Appl. Phys. Lett., 69 (1996) 2864.

[59].J. S. Im, US Pat US6322625 (2001).

[60] C. H. Oh, M. Ozawa and M. Matsumura: Jpn. J. Appl. Phys. 37 (1998) L492.

[61] P. C. van der Wilt and R. Ishihara, “Grain location-control in excimer-laser crystallised thin silicon films,” *Physica Status Solidi (a)* 166(2), pp. 619–627, 1998.

[62] R. Ishihara, A. Burtsev, and P. F. A. Alkemade, “Location-control of large Si grains by dual-beam excimerlaser and thick oxide portion,” *Jpn. J. Appl. Phys.* 39(7A), p. 3872, 2000.

[63] P. C. van der Wilt, B. D. van Dijk, G. J. Bertens, R. Ishihara, and C. I. M. Beenakker, “Formation of location-controlled crystalline islands using substrate-embedded-seeds in excimer-laser crystallization of silicon films,” *Appl. Phys. Lett.* 72(12), p. 1819, 2001.

[64] D. H. Auston，C. M. Surko，T. N. C. Venkatesan，R. E. Slusher，J. A. Golovchenko，”Time-resolved reflectivity of ion-implanted silicon during laser annealing”，Appl . Phy . Lett . 33(5)，1978.

[65] C.W. Lin , H. C. Cheng et al., IEEE Elec. Dev. Lett. V22, no.6, p269, June 2001.

[66] D. H. Lowndes, G. E. Jellison Jr., S. J. Pennycook, S. P. Withrow, D. N. Mashburn, *Appl. Phys. Lett.* 48 (1986) 1389.