國立交通大學

電機學院光電顯示科技產業研發碩士班

碩 士 論 文

N 型複晶矽薄膜電晶體在閘極開區域脈衝電壓及汲極直流偏壓下的劣化研究

Study of N-type LTPS TFTs Degradation under Gate Pulse Stress in ON Region with Drain Bias

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中 華 民 國 九 十 七 年 三 月

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N 型複晶矽薄膜電晶體在閘極開區域脈衝電壓及汲極直流偏壓下的劣化研究

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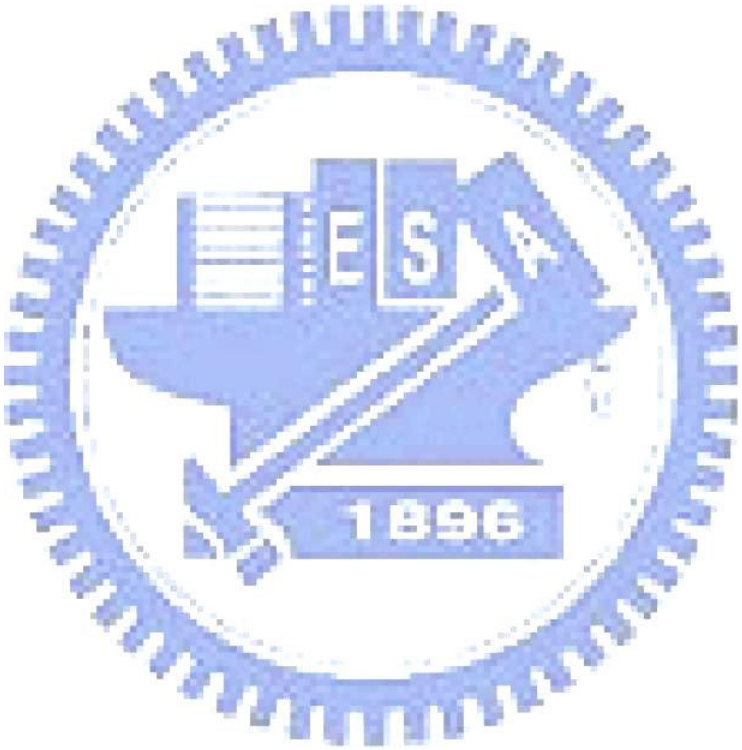
摘　要

本論文主要的目的是研究 N 型複晶矽薄膜電晶體在交流訊號操作下的劣化行為。這篇論文不同於先前的研究，其是研究 N 型複晶矽薄膜電晶體在閘極開區域交流訊號和汲極偏壓操作下的劣化特性，這將更接近實際電路應用上的操作條件。元件的劣化是透過改變不同交流閘極脈衝和汲極直流偏壓的條件來測試。我們觀察到元件的劣化受到汲極直流偏壓、閘極脈衝次數、閘極電壓位準和工作週期所影響。

基於皆有大汲極直流偏壓下的直流閘極操作和交流閘極操作之間的比較，我們提出一個新的指標（V_{GO}）來針對閘極交流訊號作直流閘極電壓的等效估算。由此結果更進一步的發現，直流操作下的熱載子效應（hot carrier effect）和自我發熱效應（self-heating effect）的特徵可對應於有汲極直流偏壓的交流閘極操作。除此新發現外，也清楚知道在交流操作下，不同工作週期與元件劣化之間的關係。即熱載子是主導低閘極電壓範圍操作的劣化，且劣化相對隨著閘極脈衝的工作週期減少明顯增加。然而，在高閘極電壓脈衝造成的劣化是由自

我發熱主導，並隨著閘極脈衝工作週期的增加而效應更明顯。根據直流操作和交流操作之間的相似處，在開區域的動態操作下，其複晶矽薄膜電晶體的可靠度便可藉由直流操作條件的可靠度行為做簡單地估算。



Study of N-type LTPS TFTs Degradation under Gate Pulse Stress in ON Region with Drain Bias

student：Chang-Lung Chan **Advisor：Dr. Ya-Hsiang Tai**

Industrial Technology R & D Master Program of
Electrical and Computer Engineering College
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ABSTRACT

The purpose of this thesis is to study the degradation behavior of N-type poly-Si TFTs under AC operation. It differs from previous studies, the characteristics of poly-Si TFTs under gate pulse AC operation in the ON region with drain bias are investigated, which would be much similar to the real operation conditions in applications. Degradation of the device is examined for various conditions of AC gate pulse and DC drain bias. It is observed that the degradation is affected by the drain bias, pulse repetition number, gate pulse level, and duty ratio.

On the basis of the comparison between the DC gate stress and AC gate stress both with large Vd, we proposed a new index V_{GO} to estimate the equivalent DC Vg for the gate AC signal. It is further found from the results that the features of hot carrier effect and self-heating effect in DC stress are corresponding to gate AC stress with drain bias. In addition to this new finding, the relation between the device

degradation and various duty ratios under AC operation with Vd is also evidenced. That is, hot carriers are the dominant cause of degradation under low-level of the gate voltage (Vgl), and the mobility degradation obviously increases with the decrease in duty ratio. However, the degradation is dominated by self-heating under high-level of the gate pulse (Vgh) and corresponding with the increase in duty ratio. Based on the similarity between the DC stress and AC gate stress, the reliability of poly-Si TFTs dynamically operated in the ON region could be simply estimated from its reliability behavior under DC stress conditions.

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Contents

Table Captions

Chapter 2 Experiments

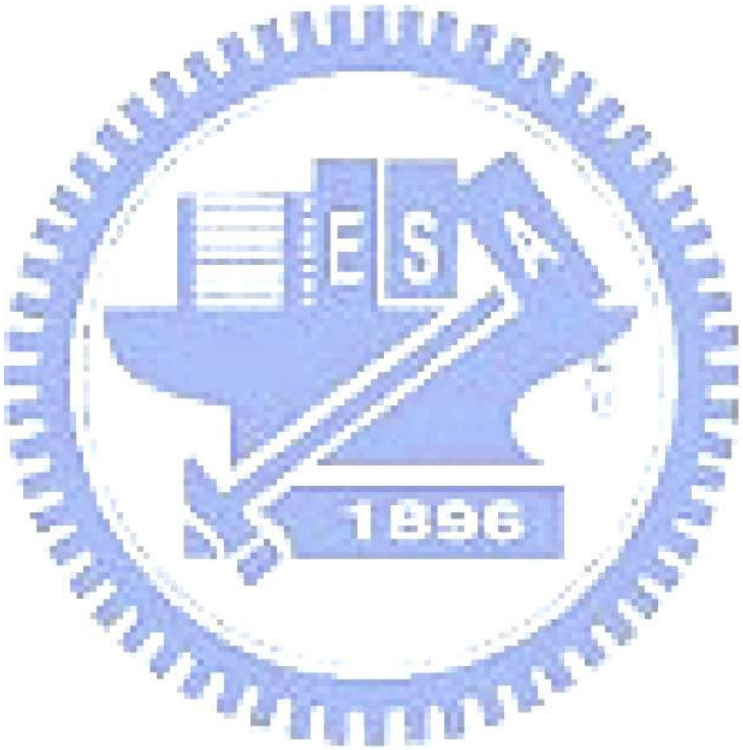
Chapter 3 Results and Discussion

Figure Captions

Chapter 1 Introduction

Chapter 2 Experiments

Chapter 3 Results and Discussion



Chapter 1 Introduction

1.1 Overview of Low-Temperature Polycrystalline Silicon Thin Film Transistors (LTPS TFTs)

In recent years, with the arrival of digital era and development of the flat panel display technology, the technology of low temperature polycrystalline silicon (LTPS) has become a pronoun of high-resolution displays. The LTPS thin-film transistors (TFTs) have attracted a great attention and have been used very successfully for active matrix displays, such as active matrix liquid crystal displays (AMLCDs) [1.1]-[1.6] and active matrix organic light emitting displays (AMOLEDs), due to allow for peripheral integration of driving circuits with pixel panel and a high current driving capability as compared to conventional amorphous Si (α -Si) TFTs [1.7]-[1.11].

Moreover, taking advantage from these features, poly-Si TFTs can be fabricated both as pixel TFTs and the peripheral circuits including n-channel and p-channel transistors. LTPS TFTs for displays have become a very mature and high yield manufacturing technology in the latest innovations underlining the unique capability. Advancing LTPS technology has led to the better display performance and up to now, several peripheral circuits have been successfully integrated on substrate [1.12]. Recently LTPS TFTs have been significant focus on the applications of the high level of device and circuit integration, such as Ambient Light Sensing, Integrated Touch, Ultra-Low Power Display Driving, and Advanced AMLCD Display Driving [1.13].

However, in spite of having superior applications, the degradation behavior of the poly-Si device is an important issue. Therefore, in order to realize the new applications and achieve those functions with LTPS TFTs, the improvement of the performance and the reliability of poly-Si TFTs is the most important requirement.

1.2 Review of Degradation for TFT under DC and AC Stress

In order to understand the degradation behavior of poly-Si TFTs, we briefly describe the mechanisms of device degradation under stress of different operating conditions as follows.

1.2.1 Degradation under DC Stress

Recently it was reported that poly-Si TFTs suffer from several degradation mechanisms, such as hot carrier effect [1.14]-[1.17], self-heating effect [1.18, 1.19], and photon-induced leakage current [1.20, 1.21]. In previous reports, Satoshi Inoue brought up the stress voltage dependence of the threshold voltage (V_{th}) shift in poly-Si TFTs, as shown in Fig. 1-1. Also, Satoshi Inoue (2003) presented the degenerated phenomena were classified to two main degradation regions including the stress voltage of region A and region B as shown in Fig. 1-2. It shows the effect of stress voltage on the I_{on} variation in TFTs [1.22, 1.23]. The two main degradation mechanisms of n-type TFTs are the hot carrier effect and the self-heating effect. In region A, the dominant degradation mechanism is self-heating, both the drain and gate voltages are high, typically over 10 V. Then, the dominant degradation mechanism is hot carrier in region B, where only the stress drain voltage is high, typically over 10 V, and gate voltage is low, typically from 2 V to 5 V.

At first, hot carrier degradation is considered to originate from the carriers under the high electric field around the drain; conduction carriers can obtain energy from the high electric field and become “hot” to cause the damage of the metal-oxide-semiconductor (MOS) interface and that of the channel near the drain of TFTs. Thus, the carriers with high kinetic energy can easily break the weak bonds existing in poly-

Si, creating many defect states and oxide charges.

As the gate voltage increases and correspondingly the equivalent lateral electrical field decreases, the hot carrier effect will be reduced. Instead, the power dissipation in the device is becoming high, causing the increase of device temperature due to Joule heat, which is known as self-heating or thermal effects [1.24]. Since TFTs are fabricated on glass substrates which have the poor thermal conductivity, the heat dissipation to the substrate is relatively low compared with Si substrate and makes the degradation worse. Besides, the influence of self-heating effects will increase with the width of TFTs.

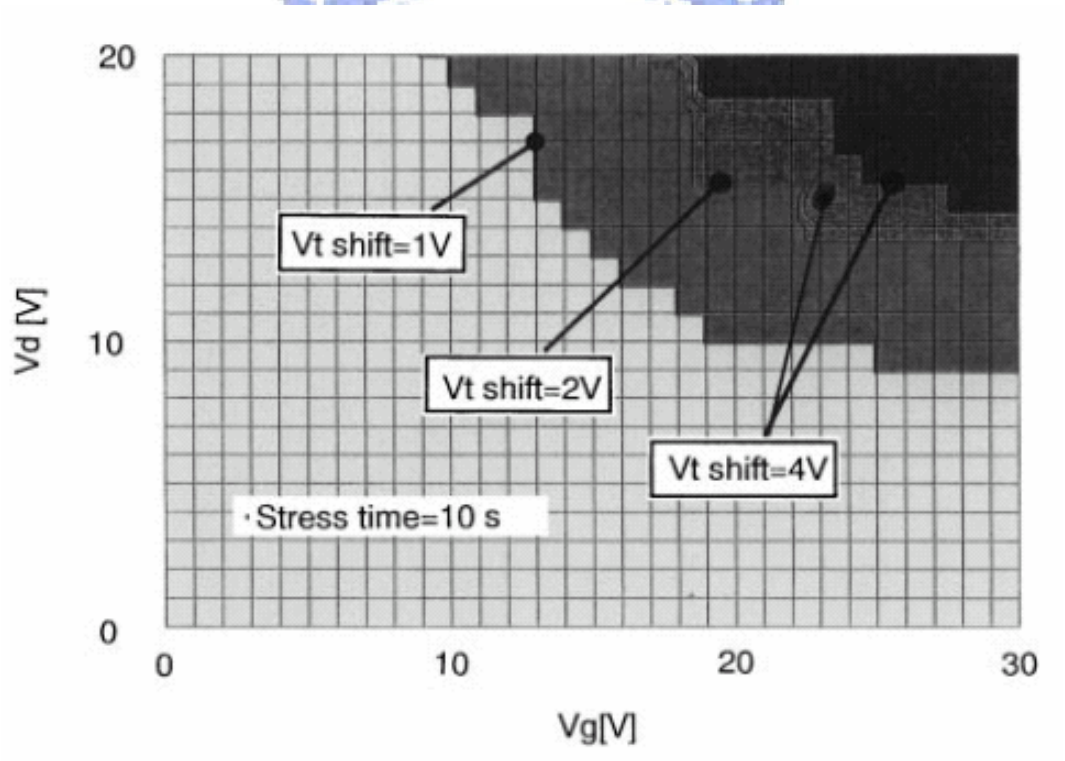


Fig. 1-1 Stress voltage dependence of the V_{th} shift of the TFTs

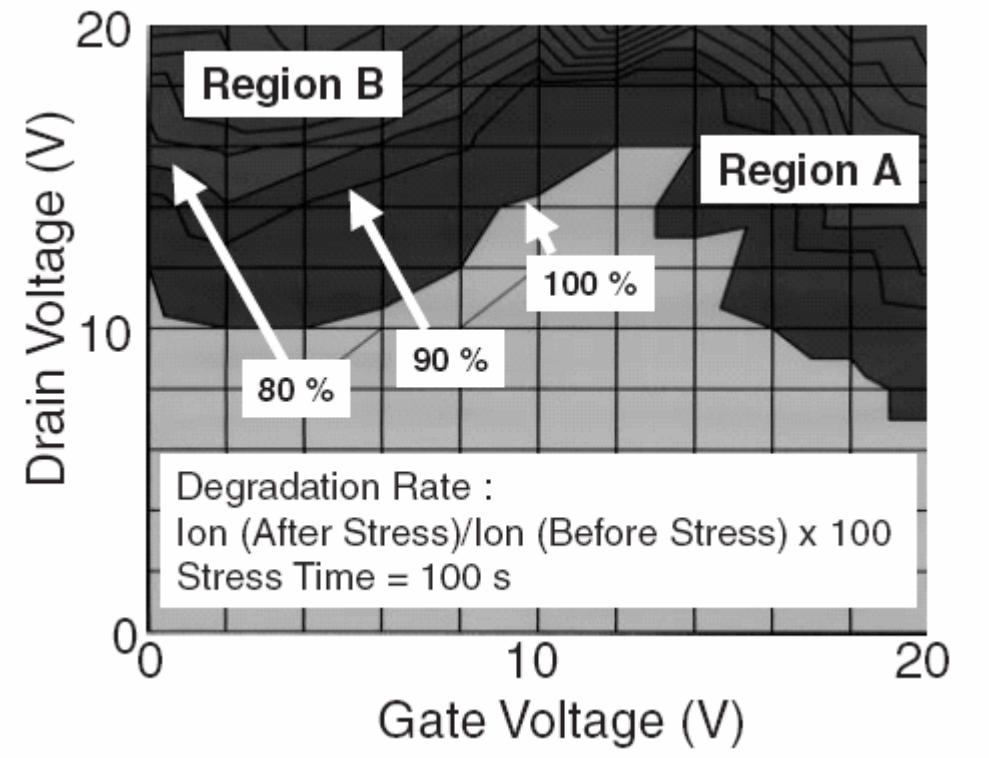


Fig. 1-2 Dependence of stress voltage on the *Ion* variation in the TFTs

1.2.2 Degradation under AC Stress

Conventionally, dynamic stress (AC Stress) indicates the imposition of a gate pulse causing the repetition of channel ON/OFF. Under dynamic stress, TFTs in driving circuits are more similar to the actual switching operation that occurs in real panel than conventional DC stress. Even a small degradation cannot be allowed under high-frequency operation. Therefore, the degradation mechanism under dynamic operation should be understood in detail [1.25, 1.26].

In previous reports, Uraoka et al. attributed the dominant of degradation mechanism to hot electrons generated by trapped electrons exposed to the high electric field and gain energy from the electric field during AC stress. The mechanism was analyzed by using a pico-second emission microscope and device simulation to examine the transient current experimentally and theoretically, respectively.

The degradation model under AC stress by Uraoka is described as follows. When the gate voltage is high (Vg=15V, ON state), the electrons gather to form a channel, as shown in Fig. 1-3 (a). When the gate voltage abruptly varies from high to low (Vg=15V→-15V), the electrons in the channel move rapidly to the source and drain, as show in Fig. 1-3(b). Some of the trapped electrons are exposed to the high electric field and gain energy from the field. Hot electrons are generated at this moment and form electron traps shown in Fig. 1-3 (c), result in the increase of density of state (DOS) in tail edge of poly-Si.

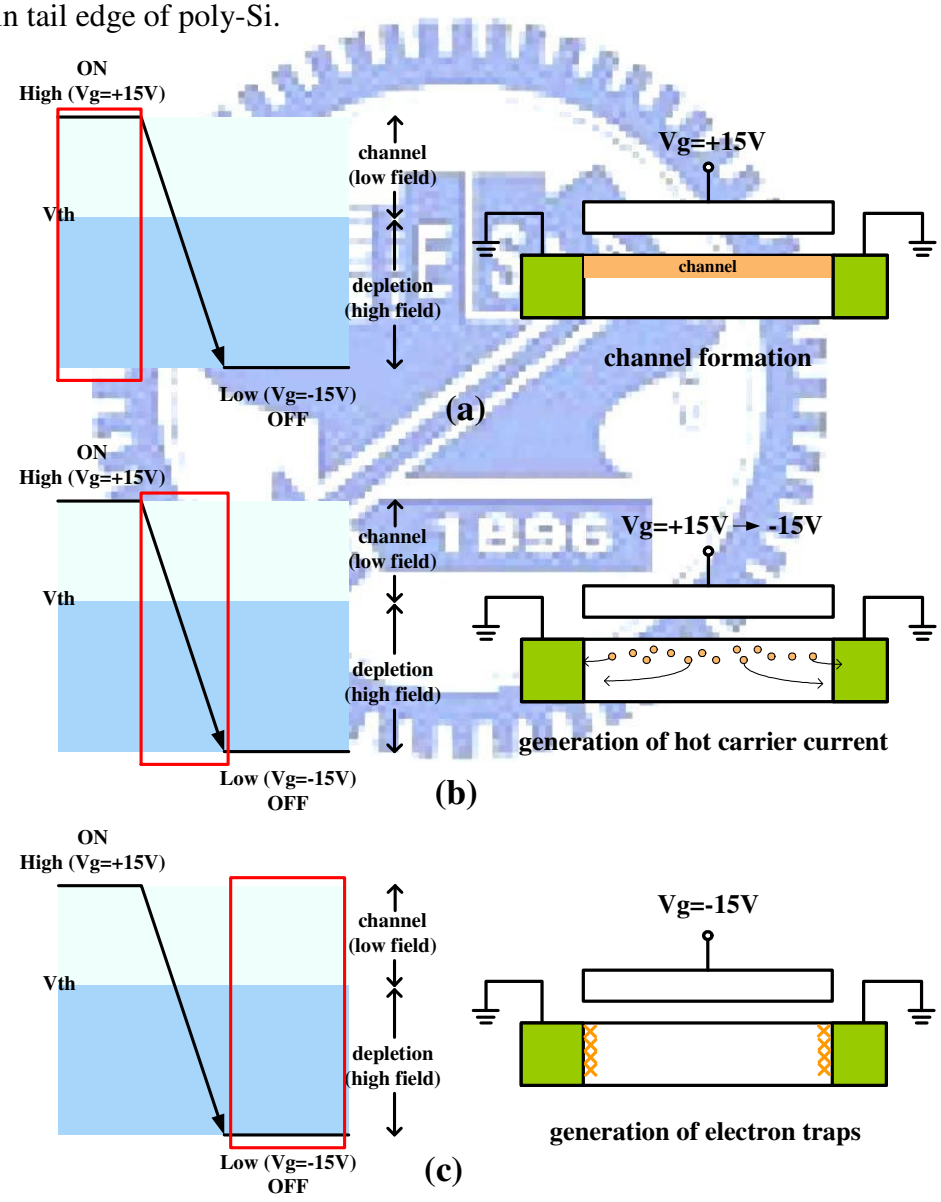


Fig. 1-3 A schematic diagram for degradation model of the N-type TFT

1.3 Motivation

While LTPS is developing towards integrated, system on panel (SOP) of high-efficiency, size of pixel and peripheral circuit shrink constantly, so extremely easy to destroy by the external force. Therefore, the quality of the device reliability has become the important key of deciding the issue of the battle. As compared to static stress, dynamic stress is closer to real operational condition and the enhanced degradation in poly-Si TFTs can be observed clearly. In addition, when the gate of the TFT is under dynamic operation, the drain-source voltage is usually present. Moreover, it is particularly important for circuit operation than pixel applications where drain biases of up to high voltage are necessary.

Although studies on static stress and dynamic stress for LTPS TFTs have been reported [1.27]-[1.32], to our knowledge a systematic study of the degradation in combination to that of dynamic and static stress has not been reported. The summary of previous researches is shown in Fig. 1-4. The purpose of the previous works was to better understand hot carrier degradation effects in the devices, and to be able to make reliable predictions of device lifetime. However, from the viewpoint of realizing devices of high reliability, hot-carrier-induced degradation under AC and DC stress is a critical issue.

In this thesis, the different aspects of the degradation in the characteristics of N-type poly-Si TFTs under gate pulse stress of the ON region with drain bias are described. Therefore, the investigation of N-type poly-Si TFT degradation phenomena including frequency, swing range, the profile of the gate pulse, and duty ratio will be discussed to verify the mechanisms under AC stress.

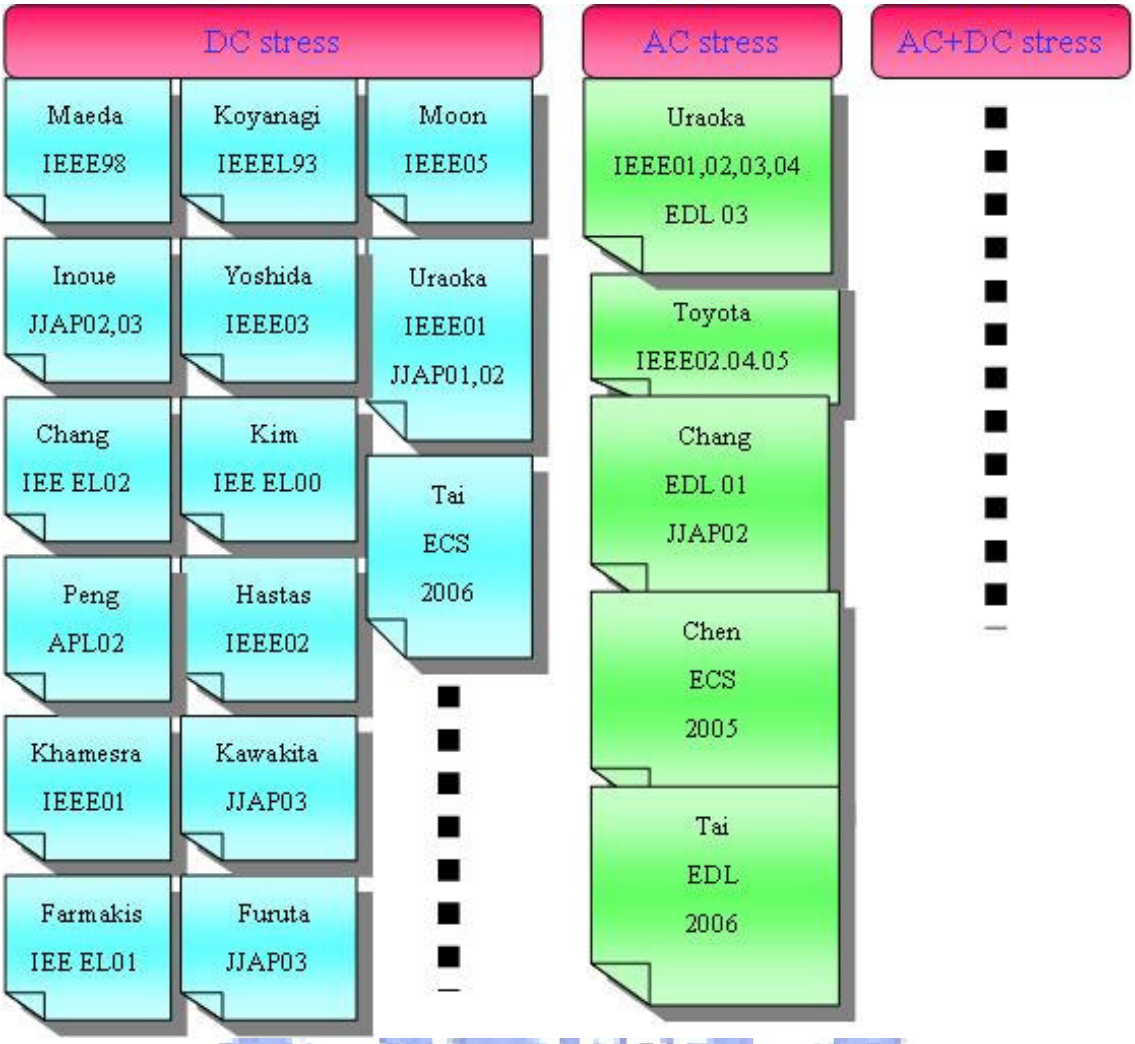


Fig. 1-4 Previous researches of LTPS TFT reliability

1.4 Thesis Organization

Chapter 1 Introduction

1.1 Overview of Low-Temperature Polycrystalline Silicon Thin Film Transistors (LTPS TFTs)

1.2 Review of Degradation for TFT under DC and AC Stress

1.2.1 Degradation under DC stress

1.2.2 Degradation under AC stress

1.3 Motivation

1.4 Thesis Organization

Chapter 2 Experiments

2.1 Procedure of Fabrication of LTPS TFTs

2.2 Extraction of Device Electrical Parameters

2.3 Stress Conditions

Chapter 3 Results and Discussion

3.1 Degradation of the Transfer Characteristics

3.2 Dependence on the Number of Gate Pulse Repetition

3.3 Effect of the Transient Time

3.4 Dependence on Gate Pulse Profile

3.4.1 Pulse Range

Chapter 2 Experiments

2.1 Procedure of Fabrication of LTPS TFTs

LTPS TFTs used in the experiment were the conventional top-gate structure and fabricated on glass substrates. The process flow of TFTs is described below. First, the buffer oxide and 50 nm thick a-Si:H films were deposited on glass substrates with plasma-enhanced chemical vapor deposition (PECVD). The samples were then put into the oven for dehydrogenation. The XeCl excimer laser of wavelength 308 nm and energy density of 400 mJ/cm^2 was applied to scan the a-Si:H film with the beam width of 4 mm and 98 % overlap to recrystallize the a-Si:H film to poly-Si. After poly-Si active area definition, 80 nm SiO_2 and 40 nm SiNx films were deposited with PECVD as the gate insulator. Next, the metal gate was formed by sputter and then defined. The lightly doped drain (LDD) and the n+ source/drain doping were formed by PH_3 implantation with dosage 2×10^{13} and 2×10^{15} cm^2 of PH_3, respectively. The LDD implantation was self-aligned and the n+ regions were defined with a separate mask. Then the interlayer of SiNx was deposited. Subsequently, the rapid thermal annealing was conducted to activate the dopants. Meanwhile, the poly-Si film was hydrogenated. Finally, the contact holes formation and metallization were performed to complete the fabrication work.

In this study, N-type TFTs with a channel width of 20 μm and a channel length of 5 μm with an LDD structure of length 1.2 μm are fabricated. Figure 2-1 shows the cross-section structure of the N-type poly-Si TFT with LDD.

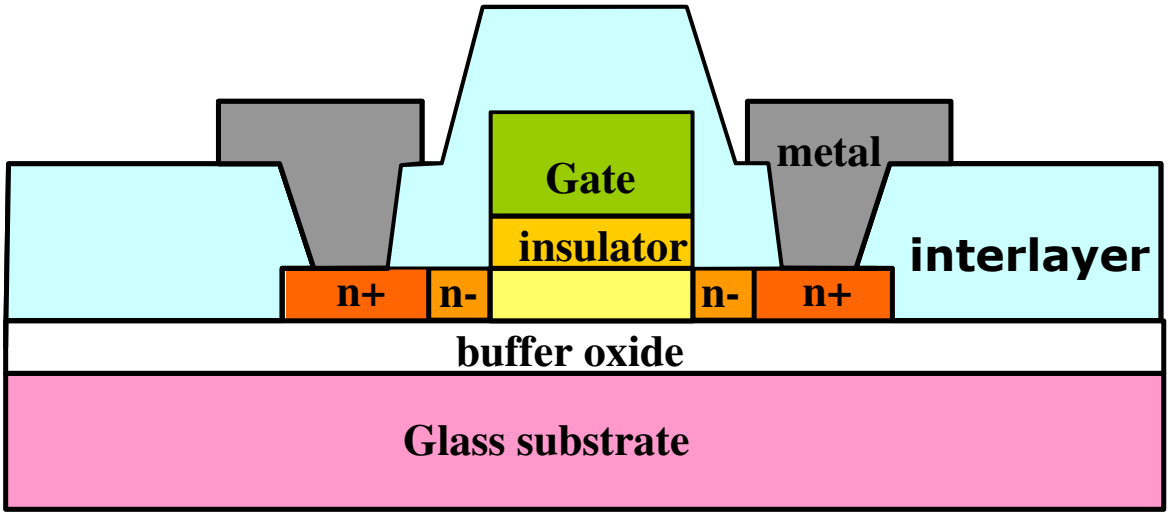


Fig. 2-1 The cross-section view of N-type LTPS TFT with LDD structure

2.2 Extraction of Device Electrical Parameters

Here, we will introduce the methods of the typical electrical parameter extraction, including threshold voltage (V_{th}), field-effect mobility (μ_{FE}), subthreshold swing (SS).

Determination of the Threshold Voltage (V_{th})

For most of the researches on TFT, the constant current method is widely-used to determine the threshold voltage (V_{th}). In this thesis, the Vth is determined by this method, which extracts the rated current (I_{Dt}) from the drain current curve. Thus, the corresponding voltage is the threshold voltage of the constant current. In general, the rated current is defined as

$$I_{Dt} = I_{DN} \frac{W}{L} \tag{2-1}$$

where I_{DN} is normalized drain current, i.e. threshold current. Typically, the threshold current is specified as 10 nA for $|V_{DS}|$ =0.1 V and 100 nA for. $|V_{DS}|$ =10 V.

Determination of the Field Effect Mobility (μ_{FE})

The transfer characteristics of poly-Si TFTs are similar to those of conventional MOSFETs. The MOSFETs can be applied to the poly-Si TFTs, so the first order I-V relation in the bulk Si. The field effect mobility (Mu, μ_{FE}) is derived from the maximum value of the transconductance (gm), which can be expressed as

$$I_D = \mu_{FE} C_{ox} \frac{W}{L} \left[(V_G - V_{th}) V_D - \frac{1}{2} {V_D}^2 \right] \tag{2-2}$$

where C_{ox} is the gate capacitance per unit area, W is channel width, L is channel length, V_{th} is the threshold voltage. If the drain voltage (V_D) is much smaller as compared with $V_G - V_{th}$, i.e. $V_D << (V_G - V_{th})$, and $V_G > V_{th}$ then the drain current can be approximated as

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}(V_G - V_{th})V_D \tag{2-3}$$

From the above equation, the gm can be obtained,

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const.} = \frac{WC_{ox}\mu_{FE}}{L} V_D \tag{2-4}$$

Therefore, the field effect mobility with Eq. (2-4) can be rewritten as

$$\mu_{FE} = \frac{L}{C_{ox} W V_D} g_m \tag{2-5}$$

In other words, the field-effect mobility can be extracted by taking the maximum value of the gm into (2-5) when V_D = 0.1 V.

Determination of the Subthreshold Swing (***S.S***)

When the gate voltage (Vg) is below the threshold voltage (V_{th}) and the channel of poly-Si appears weak inversion or depletion, the corresponding drain current is called the sub-threshold current. The subthreshold region tells how sharply the current drops with gate bias. In general, the subthreshold current is exponentially dependent on $V_G - V_{th}$, so the subthreshold swing (*S.S*) is used for observing the characteristic of turning on and turning off about the TFT. It can be shown that the expression for ***S.S*** is given by

$$S.S = \left[\frac{\partial(\log I_{DS})}{\partial V_{GS}}\right]^{-1} \tag{2-6}$$

Here, we extract the minimum value of *S.S* at the Id-Vg curve for |Vds| =0.1 V. Clearly, the smaller value of *S.S* correlates to the better characteristic of transistor, which means a small change in the input bias can modulate the output current considerably.

2.3 Stress Conditions

The Agilent 4156A precise semiconductor parameter analyzer with HP 41501B pulse generator was used to measure the I-V curve and stress the device with different conditions, respectively. The AC pulse voltage was performed on the gate electrode as the dynamic stress and the drain DC bias was applied with grounding source, which is shown in Fig.2-2. Regarding standard stress conditions, we used a rectangular pulse with amplitude of +15 V, duty ratio of 50 %, and frequency of 500 kHz, and both the rising time (Tr) and falling time (Tf) were fixed in 100 ns as shown in Fig.2-3. Furthermore, the drain bias and source were +15V and grounded respectively. The basic parameters of AC signal include frequency (F), i.e. the reciprocal of period (T), signal high level (Vgh), signal low level (Vgl), high-level time (T_vgh), low-level time (T_vgl), rising time (Tr), and falling time (Tf). Here, the definition of individual parameter is given as follows:

$$T = Tr + T\_vgh + Tf + T\_vgl \quad (2\text{-}7)$$

$$F = 1 / T \quad (2\text{-}8)$$

$$\text{Duty ratio} = (Tr + T\_vgh) / T \quad (2\text{-}9)$$

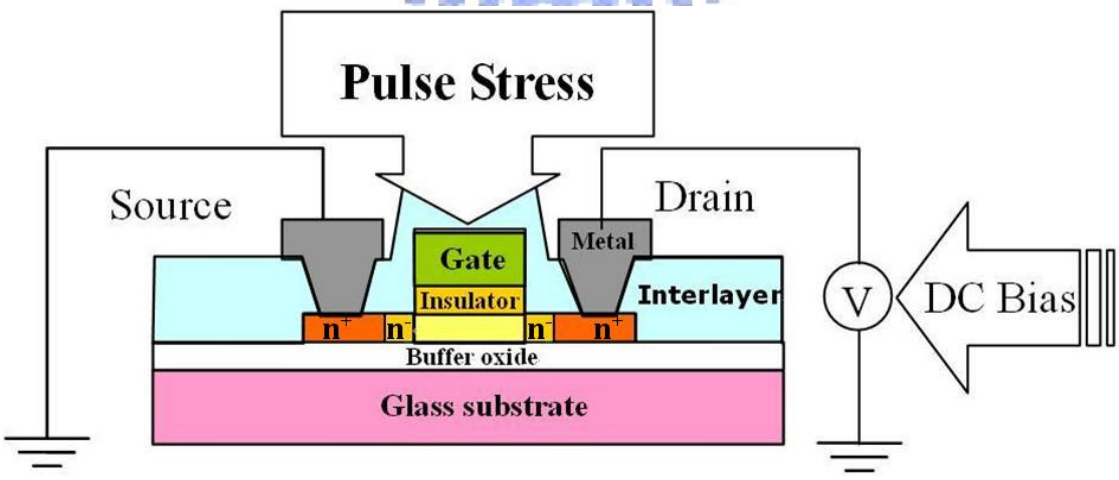


Fig. 2-2 TFT under gate AC stress with drain bias while source is grounded

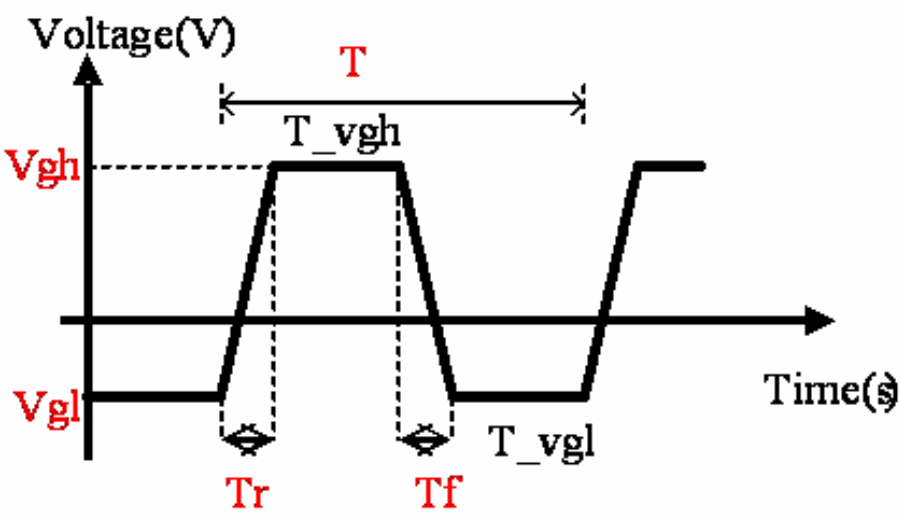


Fig. 2-3 Waveform and definition of the AC signal

In the beginning, Vd is changed from 0 V to 20 V as listed in Table 2-1. With the increase in drain bias, the stress condition is observed to result in the significant degradation. Therefore, to investigate which parameter of the stress pulse dominates the degradation of the n-type Poly-Si TFTs, we measured the various experiment results including the effects of pulse frequency, transient time, gate pulse range, and duty ratio.

Table 2-1 Experiment conditions of drain bias

Experiment	Stress Conditions				
	Gate Pulse	Drain Bias	Frequency	Duty Ratio	Stress time
Drain Bias	Vg=0~15V	Vd=0、5、10、15、20V	500kHz	50%	100s

First, we change frequency of gate pulse from 5 kHz to 500 kHz for the gate pulse repetition study. The conditions are listed in table 2-2.

Table 2-2 Experiment conditions of pulse repetitions

Experiment	Stress Conditions				
	Gate Pulse	Drain Bias	Frequency	Duty Ratio	Stress time
Pulse Repetition	Vg=0~15V	Vd=15V	5kHz 50kHz 500kHz	50%	100s 300s 500s

Next, the effect of transient time at fixed number of the pulse repetition for the degradation of the device is examined. Here, the Tr and Tf from 100 ns to 700 ns are changed. Meanwhile, the duration of signal high-level (T_Vgh) and signal low-level (T_Vgl) are fixed as 900 ns. The experiment conditions are listed in Table 2-3.

Table 2-3 Experiment conditions of transient time

(T_Vgh = TVgl = 900ns)

Experiment	Stress Conditions					
	Gate Pulse	Drain Bias	Rising Time	Falling Time	Pulse Period	Pulse Repetition Number
Rising Time	Vg=0~15V	Vd=15V	100 ns	100 ns	2 us	5.0E+07
			300 ns	100 ns	2.2 us	
			700 ns	100 ns	2.6 us	
Falling Time	Vg=0~15V	Vd=15V	100 ns	100 ns	2 us	5.0E+07
			100 ns	300 ns	2.2 us	
			100 ns	700 ns	2.6 us	

Subsequently, in order to compare the effects of gate pulse in different range, we classified the swing ranges of gate pulse into two categories. Namely, fixed low gate voltage Vgl of 0 V, and fixed high gate voltage Vgh of 15 V. To clarify the effect of the pulse level for the degradation dependence, the stress conditions of various Vg levels with fixed pulse swing are examined and are further distinguished according to the

duty ratio. Finally, we examine the dependence of degradation on DC offset of the gate pulse under various pulse ranges and duty ratios. The experiment conditions are summarized in Table 2-4.

Table 2-4 Experiment conditions of various pulse ranges and duty ratios

Experiment	Stress Conditions				
	Gate Pulse	Drain Bias	Frequency	Duty Ratio	Stress time
Pulse Range	Vg=0~5、10、15、20V (Fixed Vg_l=0V)	Vd=15V	500kHz	25% 50% 75%	100s
	Vg=0、2、5、10~15V (Fixed Vg_h=15V)	Vd=15V	500kHz	25% 50% 75%	100s
Pulse Swing of 5V	Vg=0~5V	Vd=15V	500kHz	25% 50% 75%	100s
	Vg=5~10V				
	Vg=10~15V				
	Vg=15~20V				
Pulse Swing of 10V	Vg=0~10V	Vd=15V	500kHz	25% 50% 75%	100s
	Vg=5~15V				
	Vg=10~20V				
Pulse Swing of 15V	Vg=0~15V	Vd=15V	500kHz	25% 50% 75%	100s
	Vg=5~20V				

Chapter 3 Results and Discussion

In previous research, Uraoka et al. proposed that the degradation of N-type poly-Si TFTs under gate AC operation as source and drain were grounded increases obviously with the variation of amplitude in the OFF region, as shown in Fig. 3-1 [3.1]. In the ON region, the degradation is negligible. However, with drain bias, the stress condition for gate AC operation is more similar to the actual switching operation that occurs in real panel. In order to further understand the phenomena, the degradation of N-type poly-Si TFTs under gate ON region AC stress with drain bias will be described and discussed in this chapter.

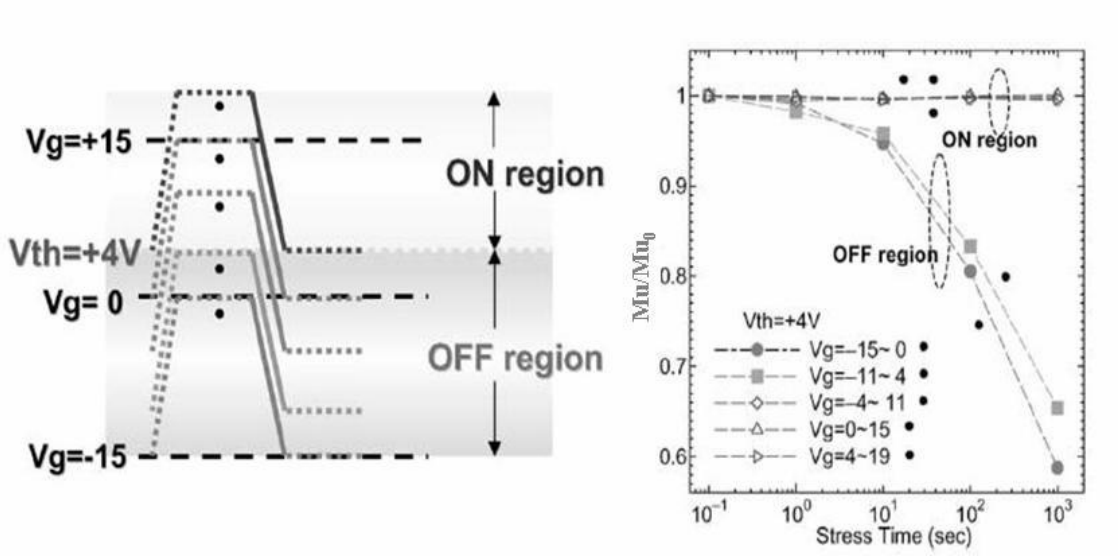


Fig. 3-1 Dependence of degradation on swing region of AC operation as source and drain were grounded

3.1 Degradation of the Transfer Characteristics

Figure 3-2 shows the transfer characteristics and extracted mobility for the N-type poly-Si TFTs before and after 100 s stress under gate pulse of 0~15 V with various drain bias (Vd) from 0 V to 20 V. The drain voltage used in the measurement was 0.1 V. It is observed that devices remain almost unchanged in the subthreshold region. However, the changes of the mobility curve and the decrease of ON-current are relatively obvious in this case. The dependence of mobility degradation at various Vd is shown in Fig. 3-3. The mobility degradation is expressed by the ratio of degraded mobility (Mu_S) to the initial mobility (Mu_0). It must be noted that the degradation is significantly accelerated on Vd of 15 V and 20 V.

Therefore, we can recognize from the result that the degradation of N-type poly-Si TFTs under gate AC operation in the ON region with drain bias is important. To obviously demonstrate the degradation in the case, the drain bias for the other experiment conditions is set to be 15 V.

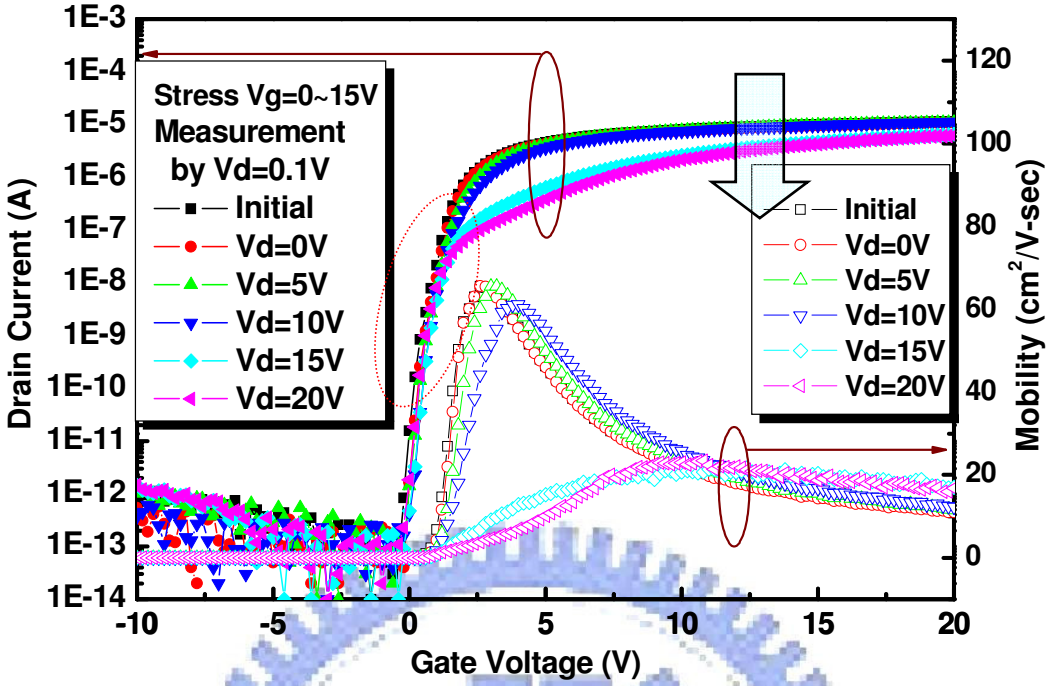


Fig. 3-2 The transfer characteristics and the extracted mobility before and after 100s stress under gate pulse of 0~15 V with various Vd

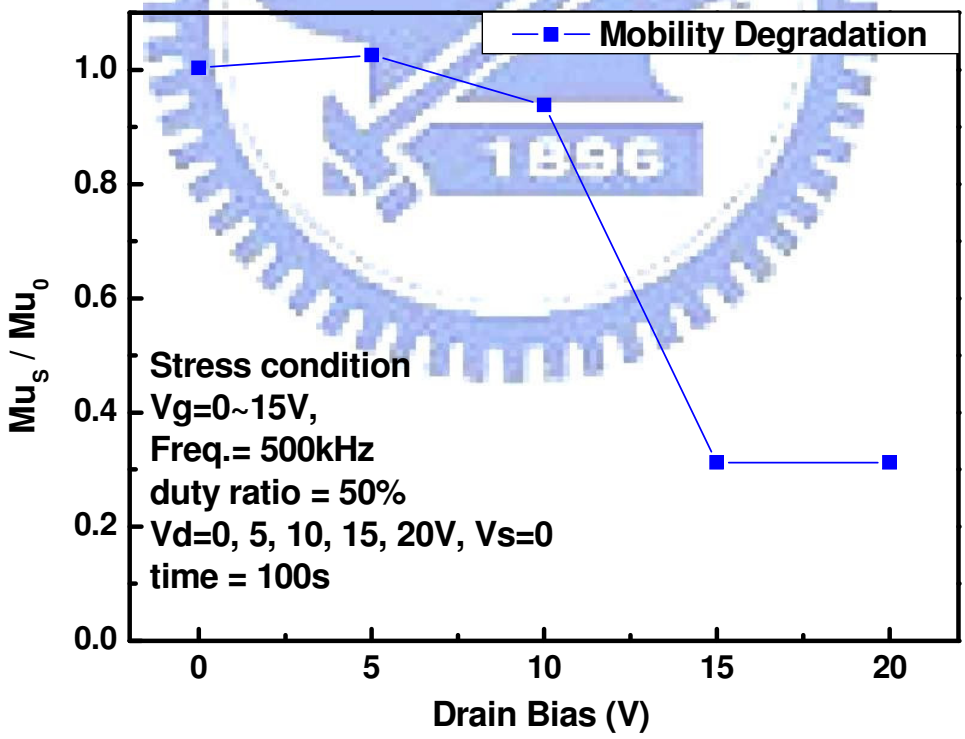


Fig. 3-3 Dependence of mobility degradation on various Vd with gate pulse stress of 0~15V

3.2 Dependence on the Number of Gate Pulse Repetition

Under gate AC pulse with various frequencies and fixed Vd of 15 V, the time dependence of the device degradation is shown in Fig. 3-4. Degradation is enhanced with the increase in frequency. And the degradation is changed violently in a shorter period of stress beginning for higher frequency. It occurs to us that the larger switching numbers take place in high frequency stress. Therefore, the number of the pulse repetition can be suggested as a reason for the degradation.

Then, the time dependence of the degradation for various frequencies is re-plotted as the repetition number dependence as shown in Fig. 3-5. The relationship between the degradation and the repetition number of the pulse is almost universal, and it is not apparently dependent on the frequency. As the slight degradation shift in the same number of repetition, we regard it as a consequence of the device variation. Since the degradation closely correlates with the number of gate pulse repetition, it is necessary to further investigate the transient effect. In the next section, the experiment conditions with various rising time and falling time will be performed.

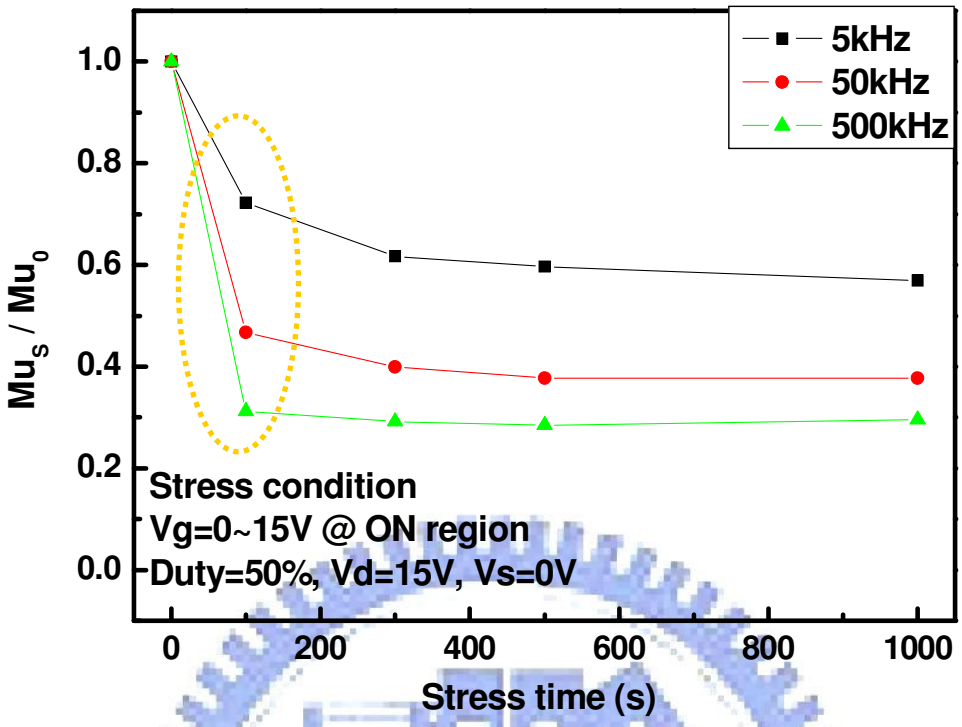


Fig. 3-4 Time dependence of degradation under gate AC pulse with various frequencies and fixed Vd of 15V

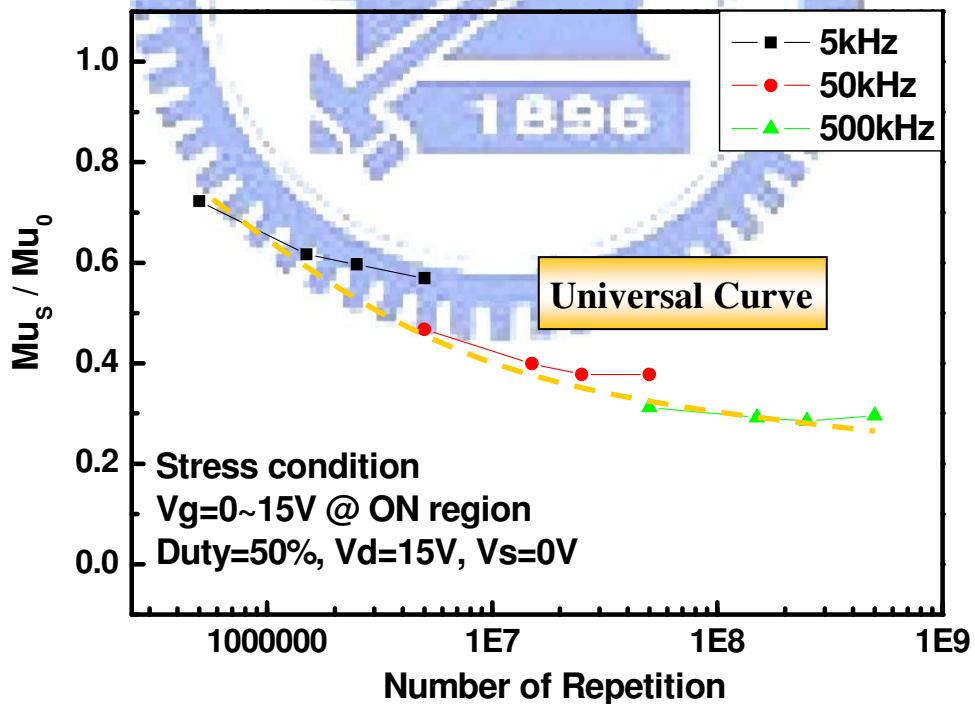


Fig. 3-5 Dependence of degradation on the repetition number of the gate AC pulse with fixed Vd of 15V

3.3 Effect of the Transient Time

In this section, we would like to investigate the effect of the transient time for the device degradation under ON region gate AC operation with drain bias. Here, we examine the transient time dependence for the degradation at fixed number of the pulse repetition. Because the duration of signal high-level (T_Vgh) and signal low-level (T_Vgl) are set the same as 900 ns. Therefore, as various stress conditions are set, the frequency could vary and the period (T) is about 2 ~ 2.6 us as illustrated in Fig. 3-6. The experiment conditions are listed in Table 3-1.

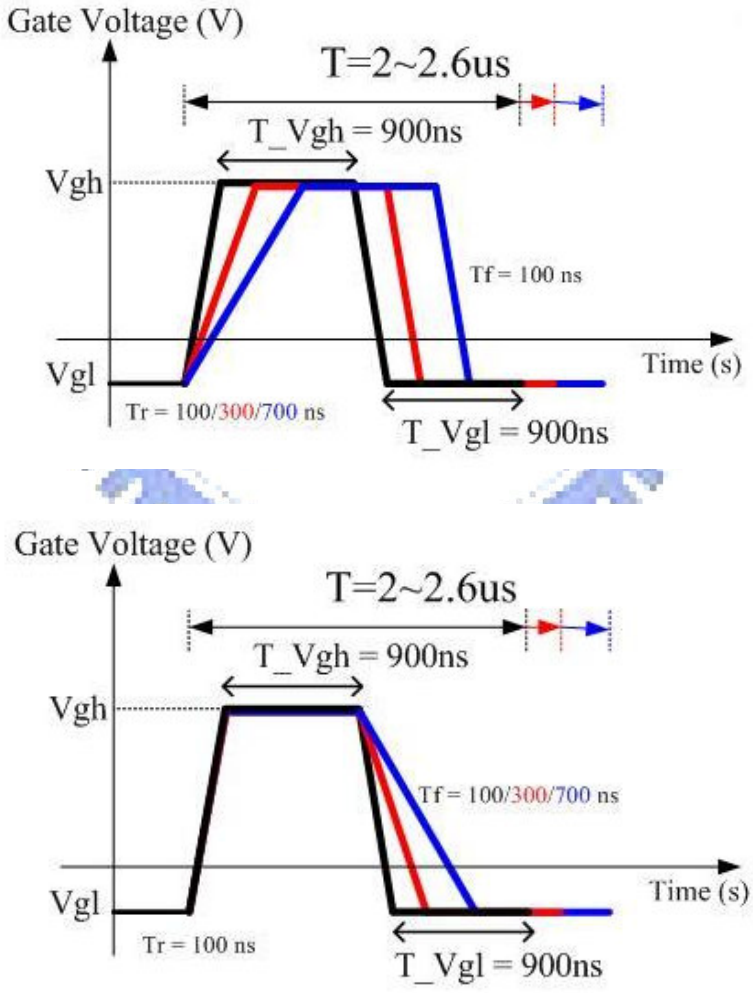


Fig. 3-6 The various transient time of the gate pulse with fixed duration of Vgh and Vgl

Table 3-1 Experiment conditions of transient time

(T_Vgh = TVgl = 900ns)

Experiment	Stress Conditions					
	Gate Pulse	Drain Bias	Rising Time	Falling Time	Pulse Period	Pulse Repetition Number
Rising Time	Vg=0~15V	Vd=15V	100 ns	100 ns	2 us	5.0E+07
			300 ns	100 ns	2.2 us	
			700 ns	100 ns	2.6 us	
Falling Time	Vg=0~15V	Vd=15V	100 ns	100 ns	2 us	5.0E+07
			100 ns	300 ns	2.2 us	
			100 ns	700 ns	2.6 us	

For those stress conditions with the rising time Tr from 100 ns to 700 ns at a fixed falling time Tf of 100 ns, no significant change in mobility degradation ratio (Mu_S/ Mu_0) is observed as shown in Fig. 3-7(a). Similarly, the degradation of the device has no obvious difference when we change the falling time Tf from 100 ns to 700 ns as shown in Fig. 3-7(b).

Based on the results of the pulse repetition number dependence and the pulse transient time dependence, we suggest that the degradation occurs mainly owing to the swing range of the gate pulse repetition. Therefore, the degradation behavior of the gate pulse range is interesting to be examined. Then, we measure different gate pulse ranges for the stress to validate the assumption in the next section.

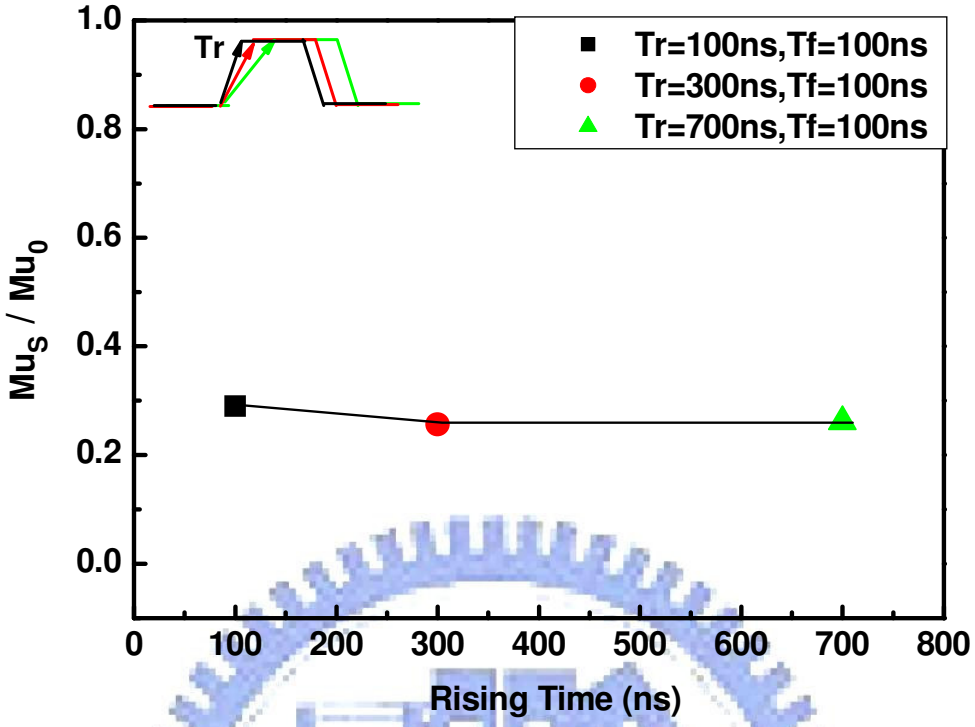


Fig. 3-7(a) Rising time dependence of the mobility degradation for AC stress with Vg of 0~15V and fixed Vd of 15V

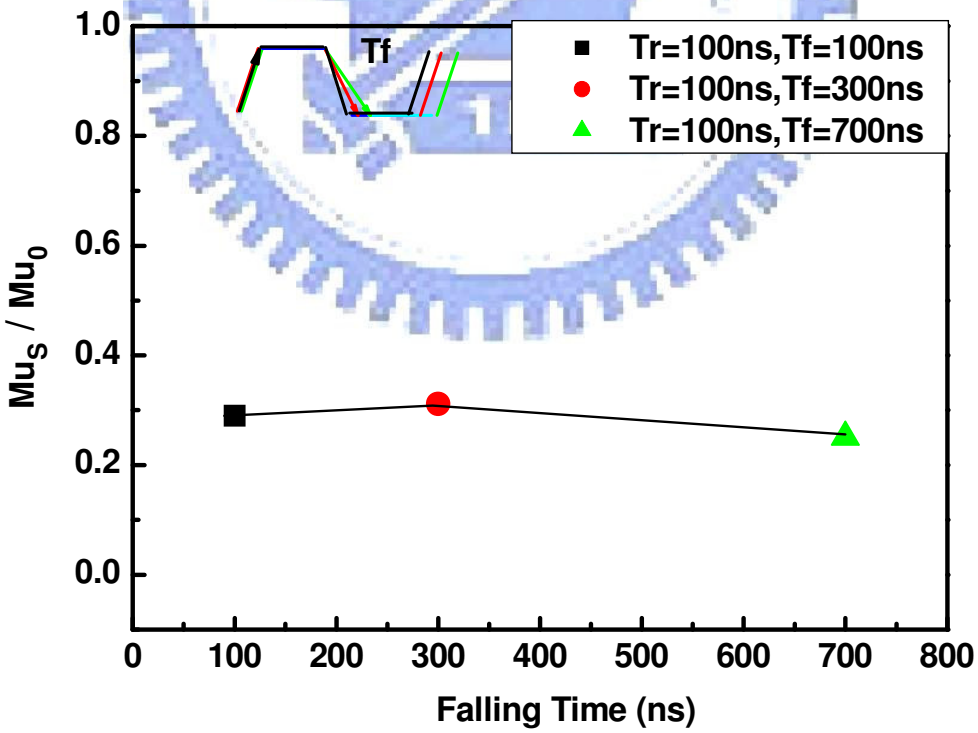


Fig. 3-7(b) Falling time dependence of the mobility degradation for AC stress with Vg of 0~15V and fixed Vd of 15V

3.4 Dependence on Gate Pulse Profile

3.4.1 Pulse Range

To investigate which range in gate voltage of the stress pulse dominates the degradation of the N-type poly-Si TFTs in the ON operation, the swing range is separated into two; one is the high-level range, and the other is the low-level range. We modulated the pulse swing by fixing the start voltages to the low-level and high-level of the gate pulse as shown in Fig. 3-8(a) and (b). Finally, we set the pulse swing fixed with different Vg level to further estimate the pulse range dependence for the degradation. The duty ratio and frequency of the gate pulse are 50 % and 500 kHz, respectively. In this section, we will present the experimental phenomena and discuss the degradation of the devices under various pulse range stress.

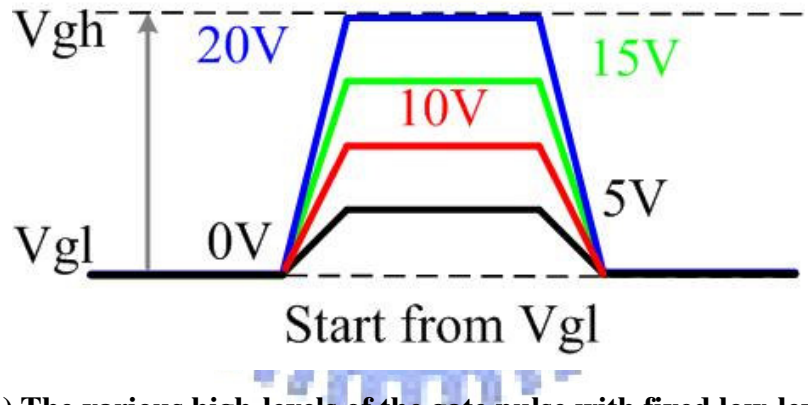


Fig. 3-8(a) The various high-levels of the gate pulse with fixed low-level voltage

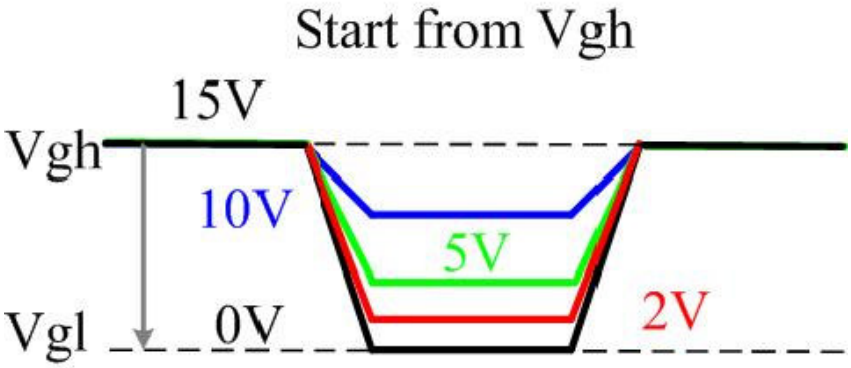


Fig. 3-8(b) The various low-levels of the gate pulse with fixed high-level voltage

3.4.1.1 High-Level of the Gate Pulse

The AC stress conditions with various high-levels of the gate pulse (Vgh) are illustrated in Fig.3-8(a). The low-level of the gate pulse (Vgl) is fixed at 0 V while Vgh varies from 5 V to 20 V. The dependence of mobility degradation on various Vgh stress is shown in Fig. 3-9. It is observed that the degradation increases with the decrease in Vg swing. The result obtained is contrary to our expectation. It is presumed that the device degradation would be enhanced as the Vg swing increases. As mention in section 1.2.1, with the increase in gate voltage, the power dissipation in the device is becoming high. The power dissipation causes the increase of device temperature due to Joule heat, which is known as self-heating or thermal effect. The degradation features of self-heating effect are increase in the amount of V_{th} shift and *S.S* change. In view of this, the degradation dependences of V_{th} shift and *S.S* change are shown in Fig. 3-10(a) and (b).

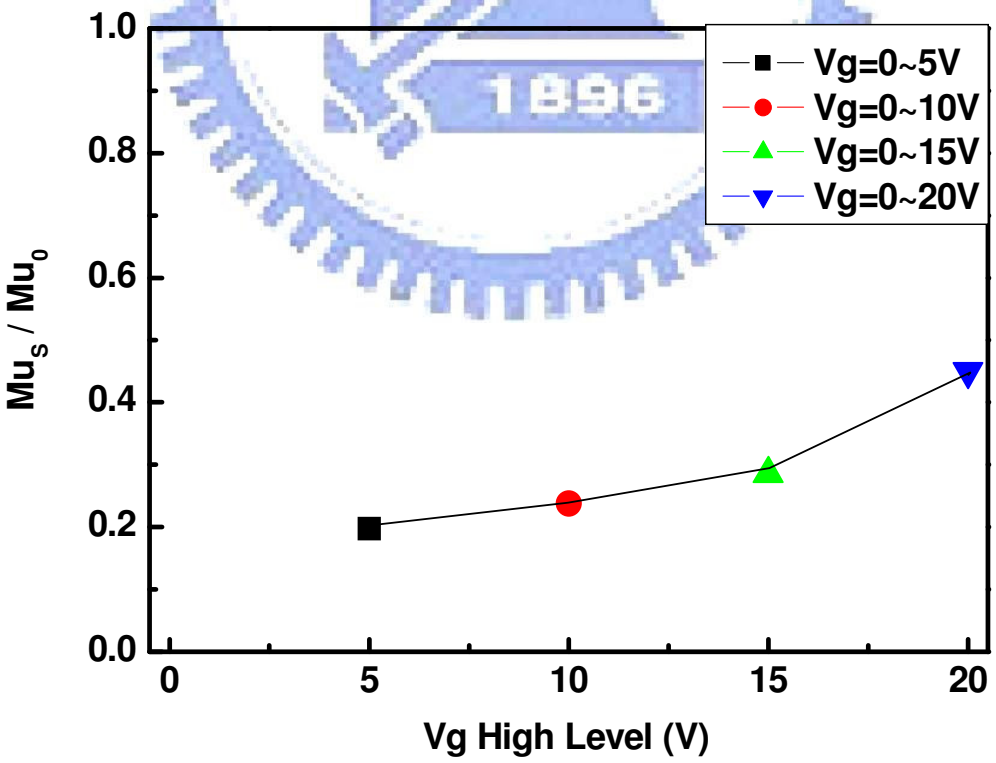


Fig. 3-9 Dependence of mobility degradation on various Vgh stress

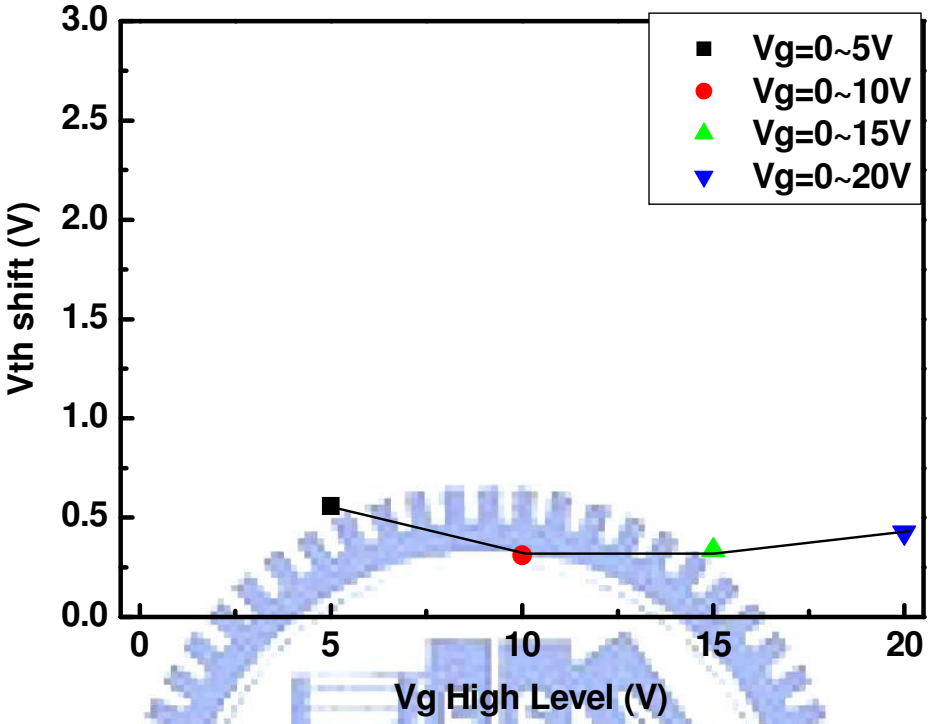


Fig. 3-10(a) Dependence of Vth shift on various Vgh stress

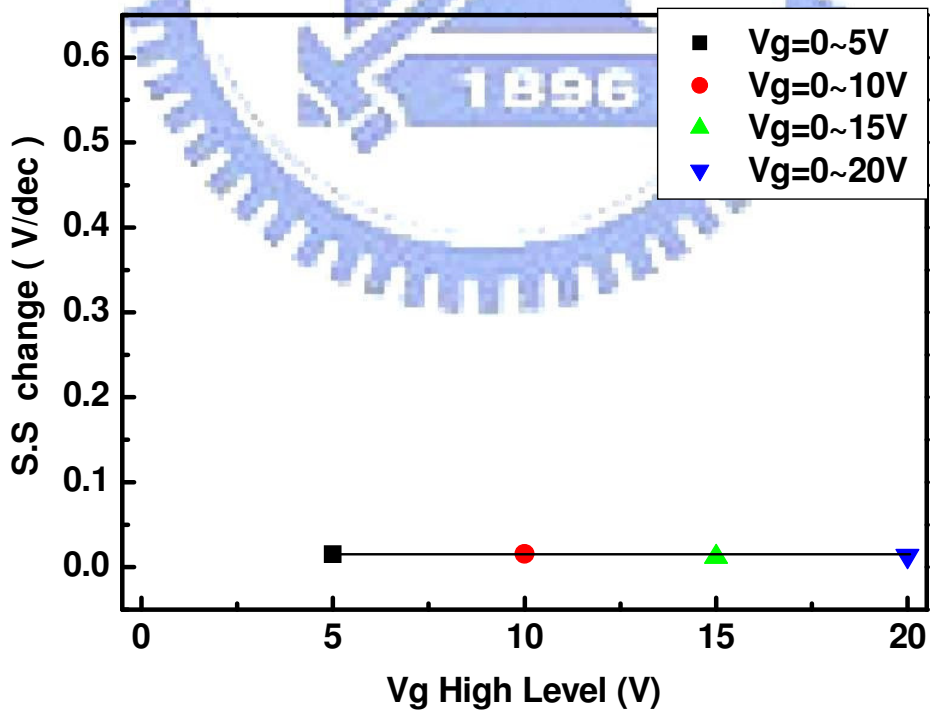
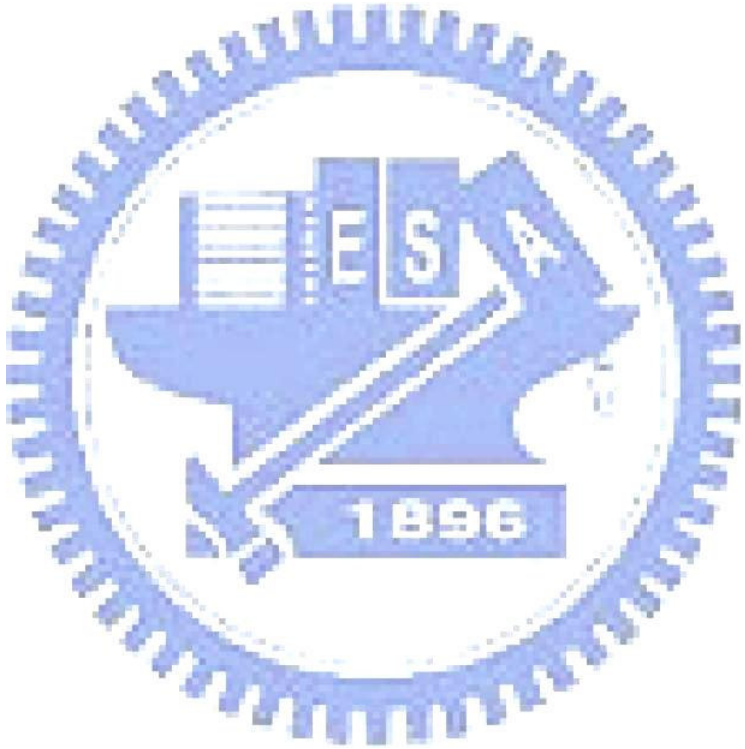


Fig. 3-10(b) Dependence of S.S change on various Vgh stress

With the increase in Vg swing, no significant change is observed on *S.S* change. However, the V_{th} shift is slightly increased for stress conditions of various Vgh. In the case of AC stress, these results lead us to the suggestion that the degradation is dominated by the lower Vg level. Therefore, the degradation caused by lower Vg level will be examined in detail later.



3.4.1.2 Low-Level of the Gate Pulse

To further evidence the lower Vg level is the dominant cause of degradation. The AC stress conditions with various Vgl are performed as illustrated in Fig.3-8(b). The Vgh is fixed at 15 V while Vgl varies from 0 V to 10 V. Figure 3-11 shows the dependence of degradation on Vgl stress. It is observed that the mobility degradation is the worst as Vgl is between 0 V and 5 V, which are around the threshold voltage (V_{th}) of the device. On the other hand, the mobility is relatively less degraded for the gate voltage swinging between 10 V and 15 V.

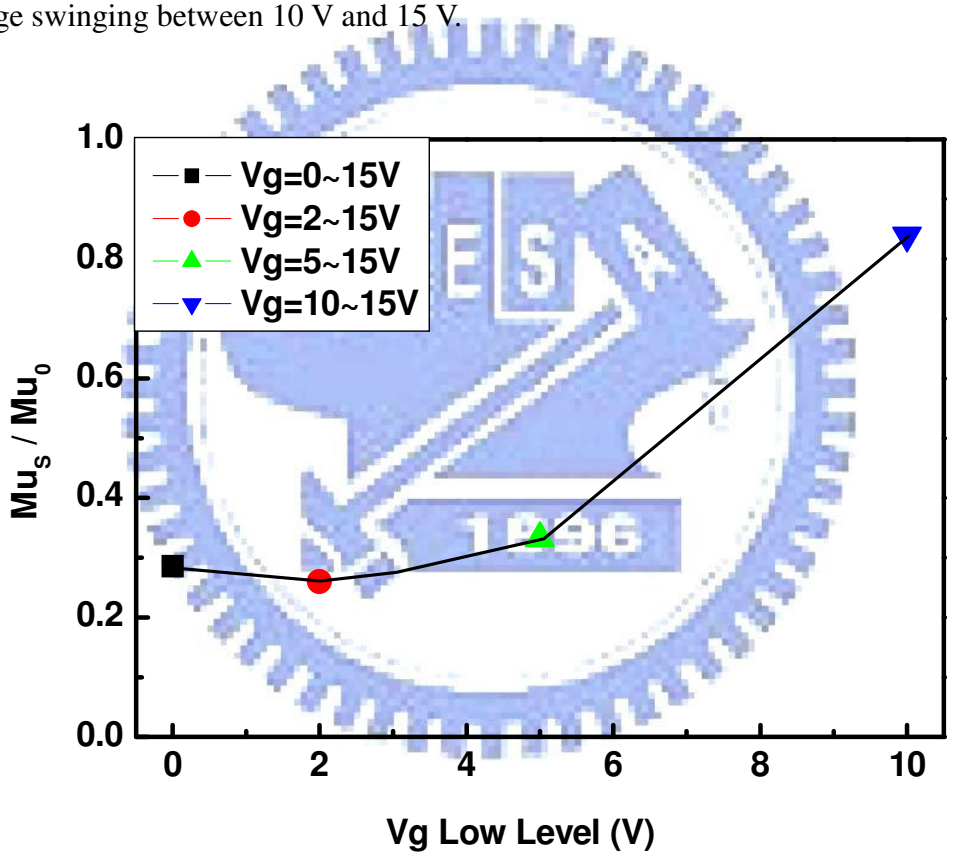


Fig. 3-11 Dependence of mobility degradation on various Vgl stress

The V_{th} shift is obviously increased at Vgl of 2V as shown in Fig. 3-12(a). However, *S.S* change is no significantly increased as shown in Fig. 3-12(b) For the stress conditions with various levels of the gate pulse, the results reveal that the degradation is more important in accordance with the lower level of the gate pulse when drain bias is present. Compared with unitary gate AC stress, i.e. the AC pulse is performed on the gate electrode with the source and drain grounded [3.1], this dependence is a unique feature to our knowledge.

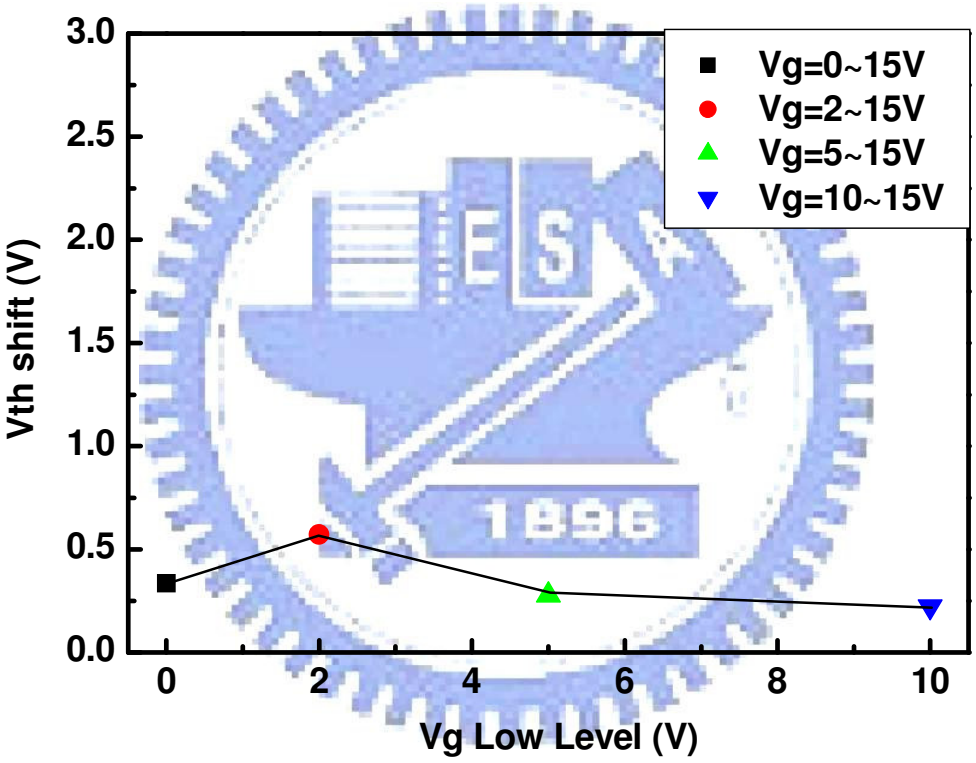


Fig. 3-12(a) Dependence of Vth shift on various Vgl stress

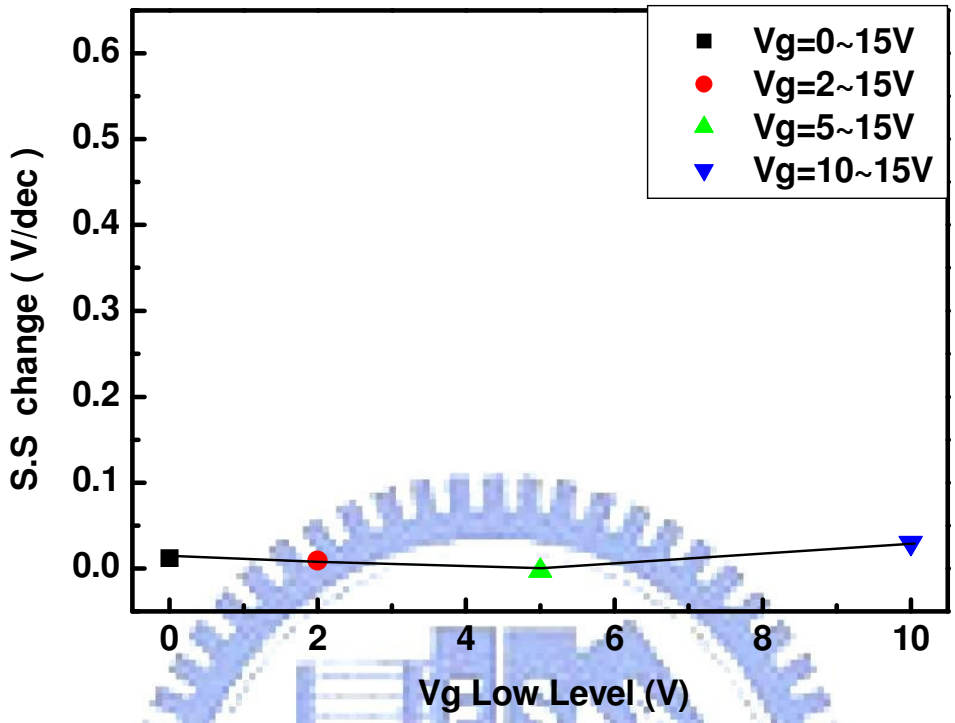


Fig. 3-12(b) Dependence of S.S change on various Vgl stress

3.4.1.3 Effect of the pulse level

In this section, we will clarify the effect of the pulse level for the degradation dependence. The AC stress conditions of various Vg levels with fixed pulse swing are examined as shown in Fig. 3-13. The dependence of mobility degradation on various Vg levels with fixed pulse swing is shown in Fig. 3-14.

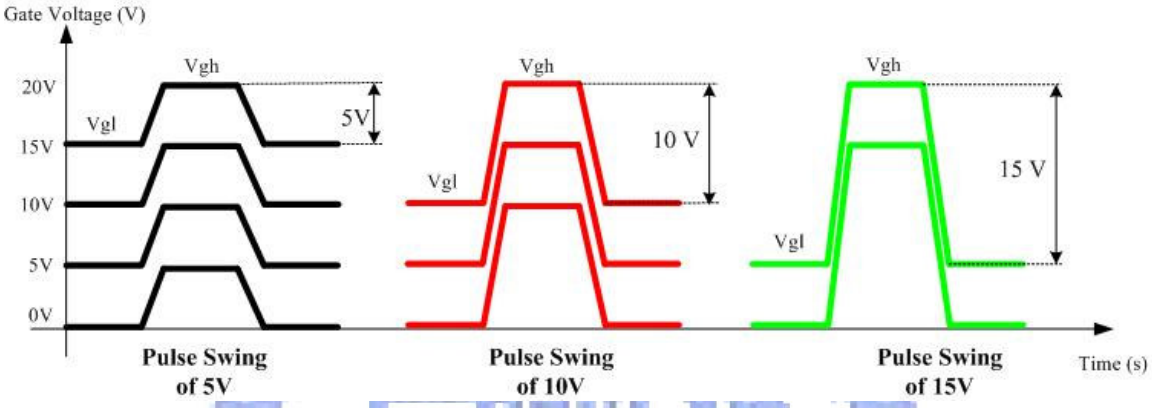


Fig. 3-13 The AC stress conditions of various Vg levels with fixed pulse swing

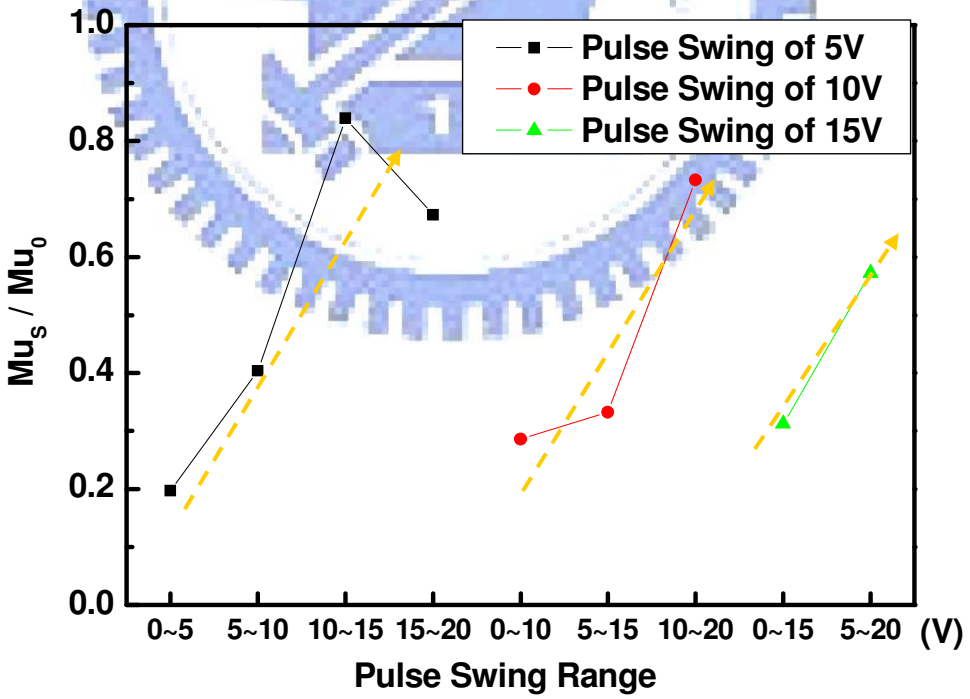


Fig. 3-14 Dependence of mobility degradation on various Vg levels with fixed pulse swing

It is observed that the degradation strongly depends on Vg level. The degradation is relieved as the Vg at high level range no matter the increase in pulse swing. The dependences of V_{th} shift and *S.S* change are shown in Fig. 3-15(a) and (b), respectively. It is obviously found that the V_{th} shift and *S.S* change are increased at high level range. The degradation behavior of Vg at high level range is similar to the case of DC self-heating effect as mentioned in section 1.2.1. In addition, the worst mobility degradation occurs at lower level of the gate pulse, especially for swing range around the V_{th} of the device. It means that the degradation behavior of Vg at low level range is similar to the case of DC hot carrier effect as mentioned in section 1.2.1. The hot carrier is generated by impact ionization under the high electric field which is induced by high Vd and low Vg around V_{th}. Based on the results of the pulse level for the degradation dependence, it occurs to us that the DC components of the AC stress waveform might play an important role. Therefore, in the next section, the degradation behaviors induced by DC components of the AC stress waveform will be further analyzed.

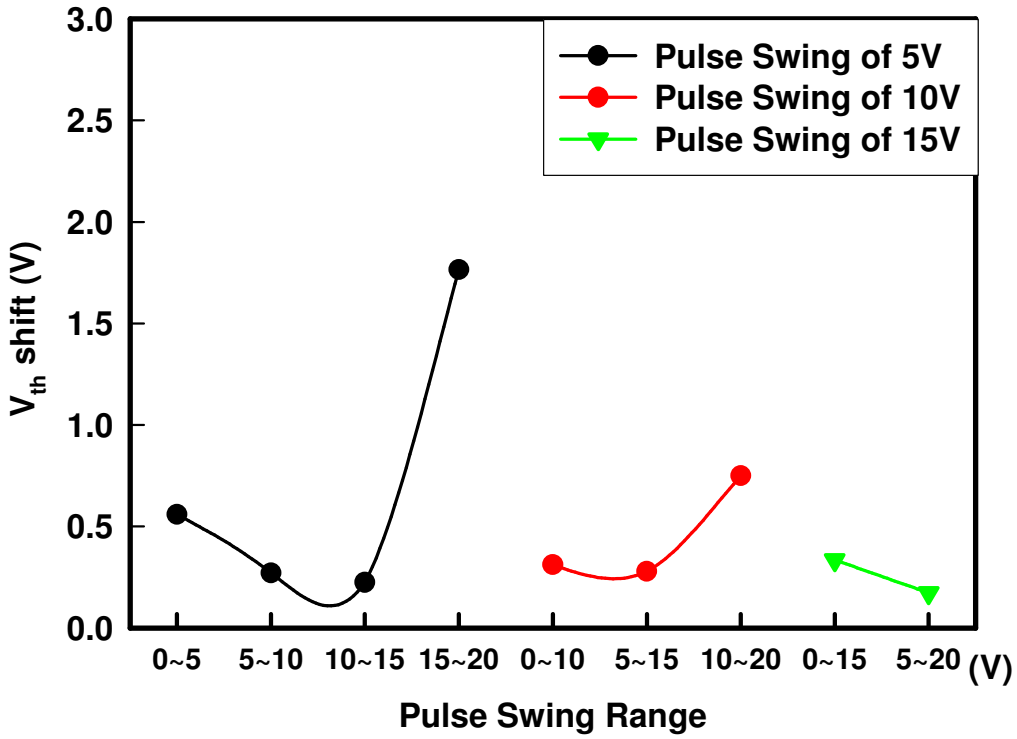


Fig 3-15(a) Dependence of Vth shift on various Vg levels with fixed pulse swing

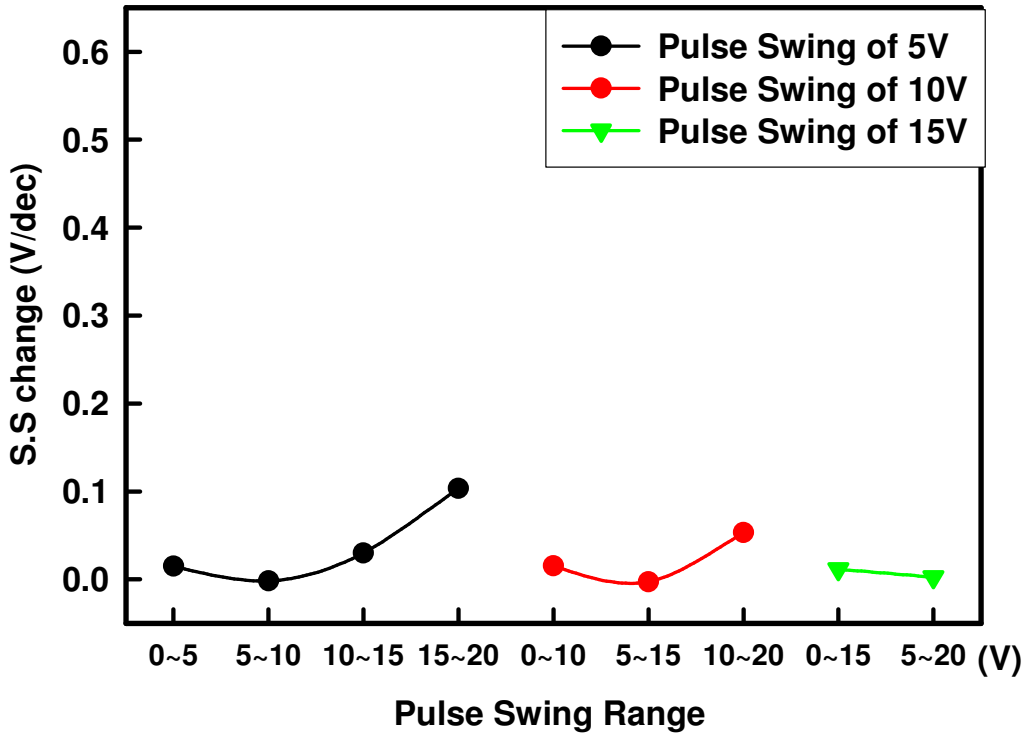


Fig 3-15(b) Dependence of S.S change on various Vg levels with fixed pulse swing

3.4.2 Duty Ratio

To study the degradation behavior induced by DC components of the AC stress waveform (Vgl and Vgh), we modulate the duty ratio from 25 % to 75 % to understand the relation during the different stress periods of single pulse. The duty ratio of the AC waveform (T_Vgl and T_Vgh) is illustrated in Fig. 3-16.

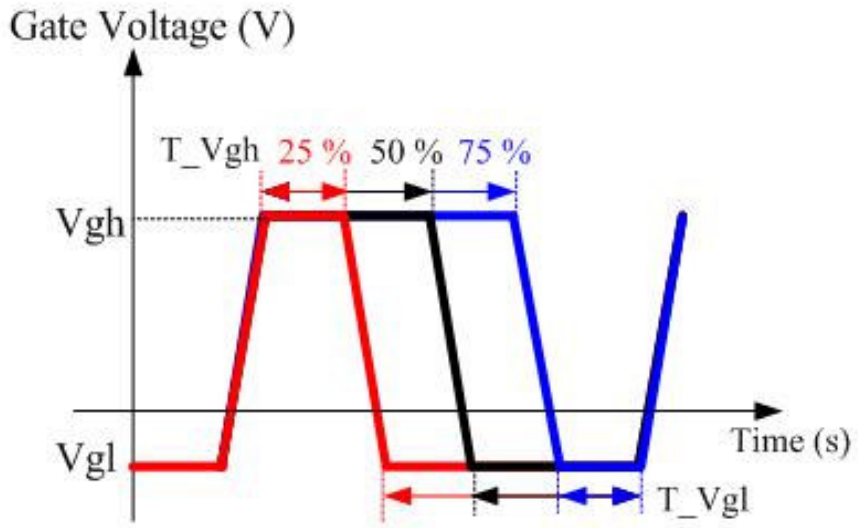


Fig. 3-16 Different stress duration of the Vg pulse level

For the stress pulse with fixed swing of 10 V as set in section 3.4.2.3, the dependences of mobility degradation on various duty ratios are shown in Fig. 3-17. It is observed that the serious degradation occurs at Vg of 0 V to 10 V and 5 V to 15 V with the decrease in duty ratio. In other words, the more degradation occurs when Vgl is around V_{th} of the device and stays longer. On the other hand, an opposite dependence trend on various duty ratios is found at Vg swinging between 10 V and 20 V. The degradation is enhanced with the increase in duty ratio. Moreover, the increase in the amount of V_{th} shift and *S.S* change are observed at the same pulse range for longer duty ratio as shown in Fig. 3-18. It is clearly indicates that the degradation strongly depended on the duty ratio and Vg pulse level.

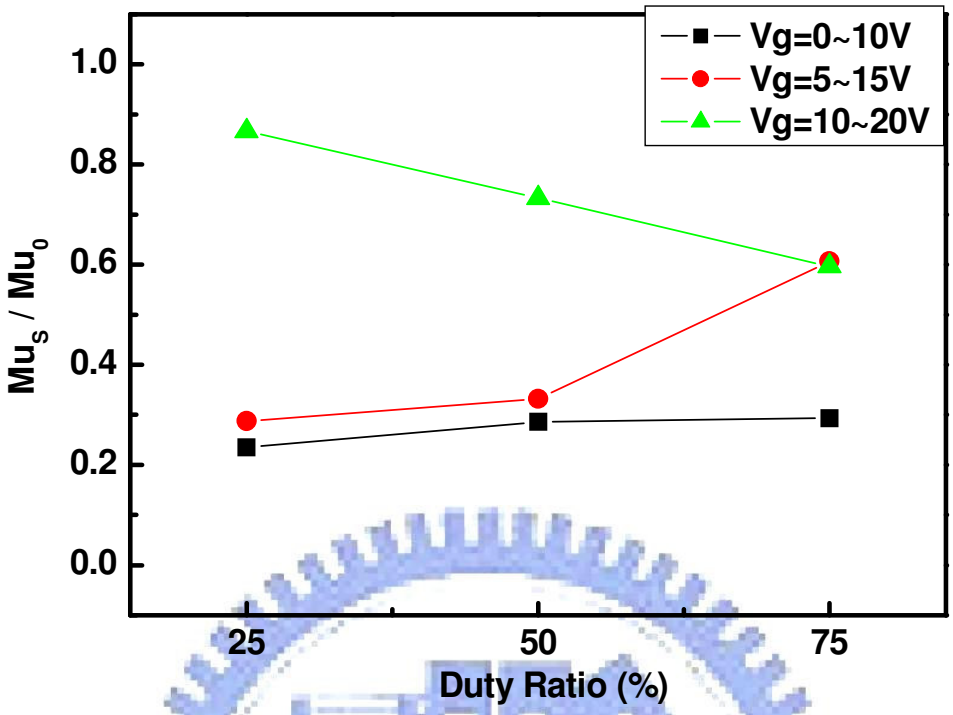


Fig. 3-17 Dependence of degradation on various duty ratios for the stress pulse with fixed swing of 10 V

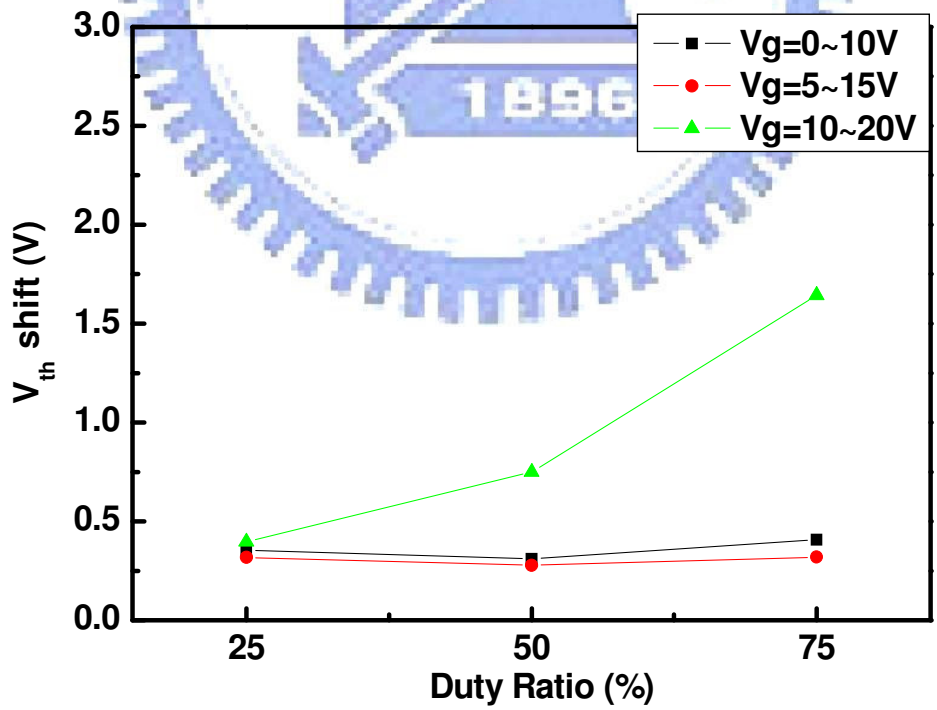


Fig. 3-18(a) Dependence of Vth shift on various duty ratios for the stress pulse with fixed swing of 10 V

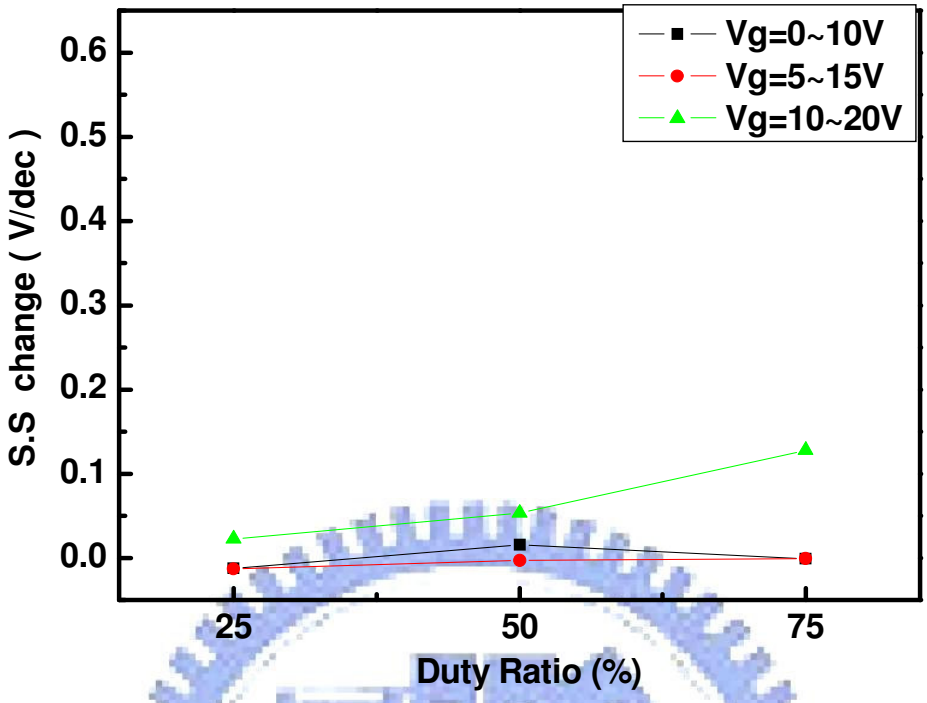


Fig 3-18(b) Dependence of S.S change on various duty ratios for the stress pulse with fixed swing of 10 V

Base on the results, the degradation behavior of higher Vg level is quite similar to the DC self-heating effect and is induced during the stress period of Vgh. As lower Vg level is around V_{th} and stays longer during the stress period of Vgl, the degradation behavior is similar to the DC hot carrier effect. It is reasonable to suppose that the difference in duty ratio dependence is attributed to the difference in degradation mechanisms. Therefore, it is presumed that the DC components of the AC stress waveform are the dominant cause of degradation behaviors in this case of AC stress. For the reason, the degradation behavior induced by AC stress will be analyzed based on its DC offset.

3.4.3 DC Offset of the AC Pulse

As mentioned in section 3.4.1 and 3.4.2, the AC pulse levels are the dominant cause of the degradation under ON region gate AC operation with drain bias. Moreover, the degradation behavior is similar to the case of DC stress effect. Then, considering the DC effects induced by the AC pulse, we will further discuss the DC components of the AC waveform. Since the gate AC waveform actually contains two DC components (Vgh and Vgl) and correspondingly lasts for different durations, we will extract the equivalent DC Vg of the AC pulse in simpler terms. Therefore, we use DC offset as the index for the AC pulse with different amplitudes and duty ratios. The index (V_{GO}) is proposed as follows,

DC Vg Offset (V_{GO}) = Vgh * duty % + Vgl * (1 – duty %)

First, we examine the dependence of degradation on V_{GO} under various pulse ranges with fixed pulse swing and duty ratio as set in section 3.4.1.3. Next, the stress conditions as set in section 3.4.1.1 and 3.4.1.2 with various duty ratios are discussed based on V_{GO} dependence.

3.4.3.1 Dependence on DC Offset of the AC Pulse with Fixed Swing Range

For the various pulse levels with fixed pulse swing, the relative V_{GO} are listed in Table 3-2. The dependence of mobility degradation on V_{GO} under various pulse levels with fixed pulse swing and duty ratio is shown in Fig. 3-19. For V_{GO} below 15 V, it can be observed that the trend of degradation distribution is gradually relieved as V_{GO} increases. Furthermore, the degradation is the worst at pulse range of 0~5 V, whose V_{GO} is 2.5 V around V_{th} of the device. On the other hand, the degradation is enhanced with the increase in V_{GO} as V_{GO} is greater than 15 V, which are high DC components of the AC waveform.

Table 3-2 DC offset of various pulse ranges with fixed pulse swing and duty ratio

Experiment	Stress Conditions	
	Pulse Range	DC Vg Offset(V_{GO}) Duty 50%
Fixed Pulse Swing of 5V	Vg=0~5V	2.5V
	Vg=5~10V	7.5V
	Vg=10~15V	12.5V
	Vg=15~20V	17.5V
Fixed Pulse Swing of 10V	Vg=0~10V	5V
	Vg=5~15V	10V
	Vg=10~20V	15V

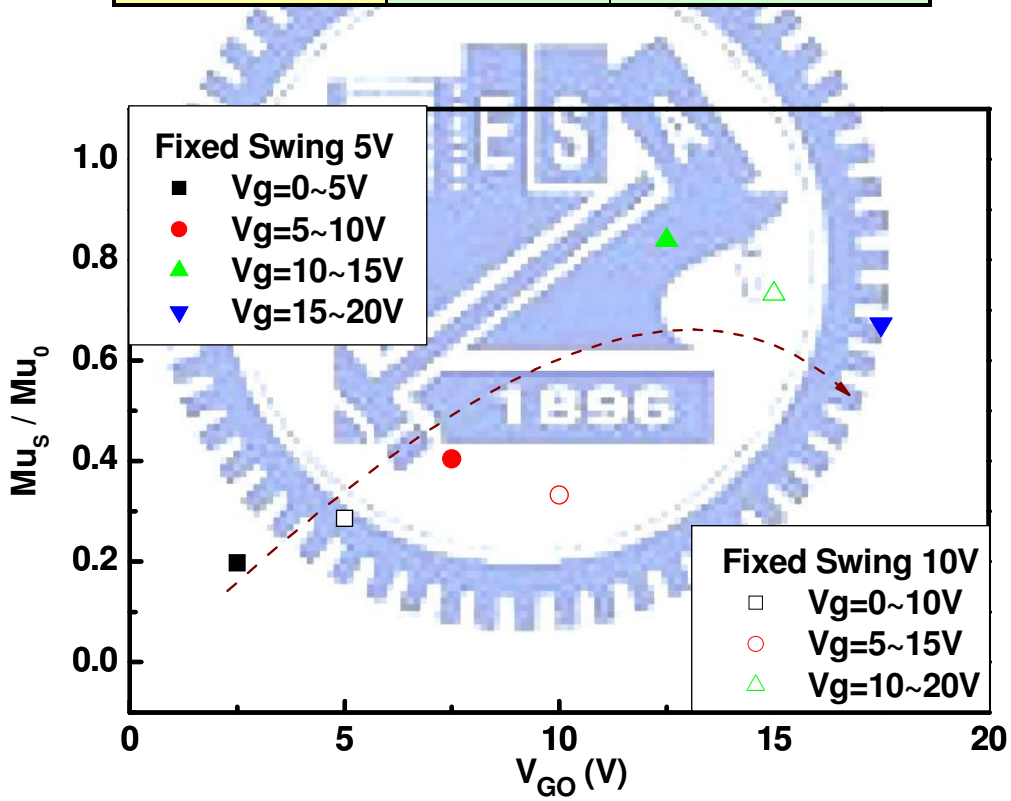


Fig 3-19 Dependence of mobility degradation on V_{GO} with fixed pulse swing of 5V and 10V

The dependences of V_{th} shift and *S.S* change are shown in Fig. 3-20(a) and (b), respectively. For lower V_{GO}, no significant changes are observed on V_{th} shift and *S.S* change. However, it is noted that the V_{th} shift and *S.S* change are obviously increased at V_{GO} of 15 V and 17.5 V, which are corresponding to high DC components of the AC waveform.

As previous mentioned in section 1.2.1, the DC hot carrier effect occurs at high Vd and low Vg around V_{th}. Here, the stress condition with low V_{GO} around V_{th} and high Vd reflects the similar degradation behavior. With the increase in V_{GO}, the stress conditions with high V_{GO} and high Vd cause increase in the amount of V_{th} shift and *S.S* change. The degradation behavior reveals the features of the DC self-heating effect. According to the results, it is reasonable to suppose that the degradation behaviors under ON region gate AC stress with drain bias are attributed to the DC effects. The DC effects induced by the DC components of the AC waveform with drain bias are based on its DC offset. Therefore, it is essential to further study the DC effects induced by the DC components of the AC waveform with drain bias. In the next section, the dependences of degradation based on V_{GO} are performed with various duty ratios of the gate pulse.

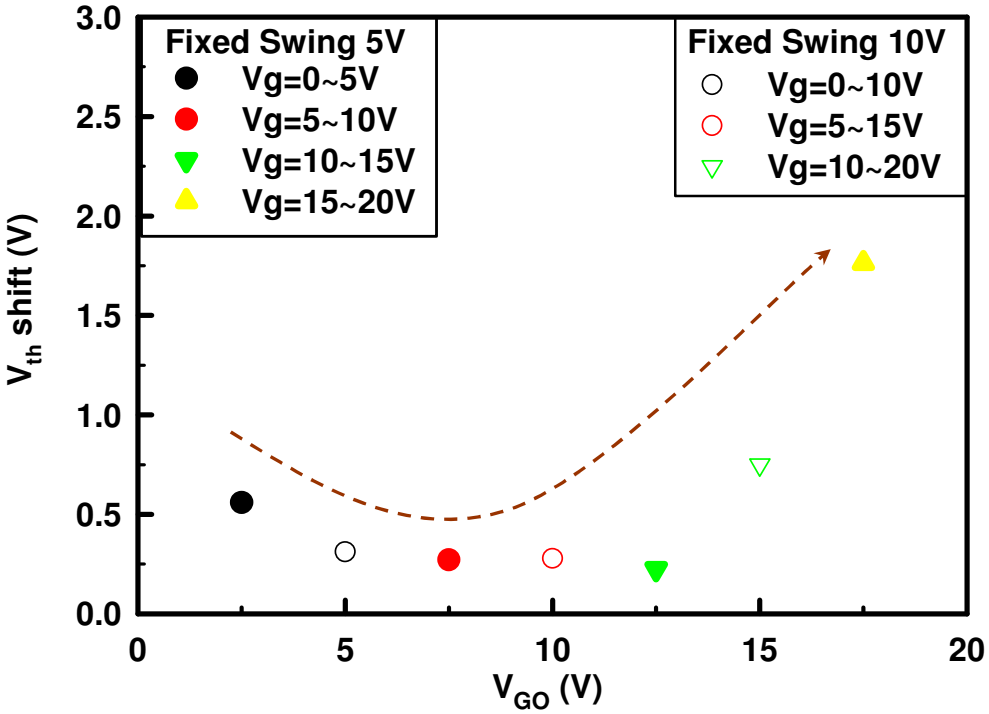


Fig 3-20(a) Dependence of Vth shift on V_{GO} with fixed pulse swing of 5V and 10V

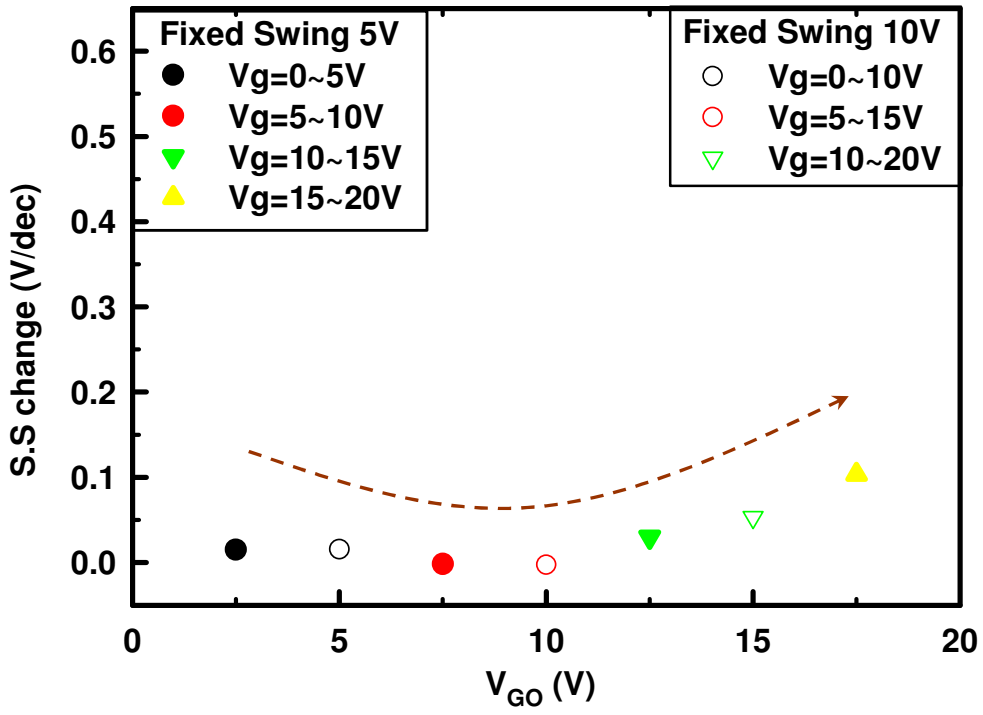


Fig 3-20(b) Dependence of S.S change on V_{GO} with fixed pulse swing of 5V and 10V

3.4.3.2 Dependence on DC Offset of the AC Pulse with Various Duty Ratio

For the stress conditions as set in section 3.4.1.1 and 3.4.1.2 with various duty ratios, the relative V_{GO} are summarized in Table 3-3. Based on the experimental data, we plot the mobility degradation of the device stressed as the V_{GO} dependence as shown in Fig. 3-21. It can be observed that the trend of degradation distribution is gradually relieved as V_{GO} increases. For lower V_{GO} around V_{th} of the device, the severe mobility degradation occurs during the longer stress period of Vgl. It is supposed that the DC effect induced by Vgl of the gate pulse is the dominant cause of degradation. With the increase in duty ratio and Vg level, namely, V_{GO} is increased, the mobility degradation is relieved due to the influence of the Vgl is decreased. The dependences of V_{th} shift and *S.S* change are shown in Fig. 3-22(a) and (b). It is found that no significant changes are observed in V_{th} shift and *S.S* change. As mentioned is the last section, V_{th} shift and *S.S* change are obviously increased at higher V_{GO}, that is, above 15 V. In this case, the relative V_{GO} are smaller than or equal to 15 V. Thus, the degradation phenomena are not revealed.

Table 3-3 DC offset of various levels and duty ratios of AC Pulse

Experiment	Stress Conditions			
	Pulse Range	DC Vg Offset		
		Duty 25%	Duty 50%	Duty 75%
High-Level of the Gate Pulse	Vg=0~5V	1.25V	2.5V	3.75V
	Vg=0~10V	2.5V	5V	7.5V
	Vg=0~15V	3.75V	7.5V	11.25V
	Vg=0~20V	5V	10V	15V
Low-Level of the Gate Pulse	Vg=2~15V	5.25V	8.5V	11.75V
	Vg=5~15V	7.5V	10V	12.5V
	Vg=10~15V	11.25V	12.5V	13.75V

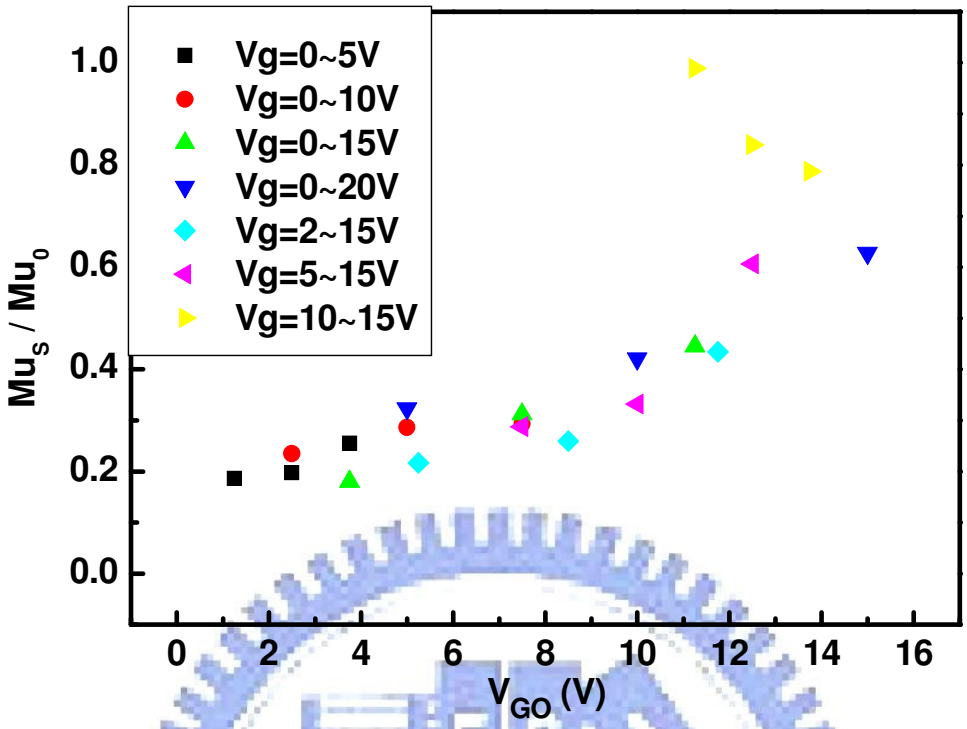


Fig 3-21 Dependence of mobility degradation on V_{GO} with various levels and duty ratios of the gate pulse

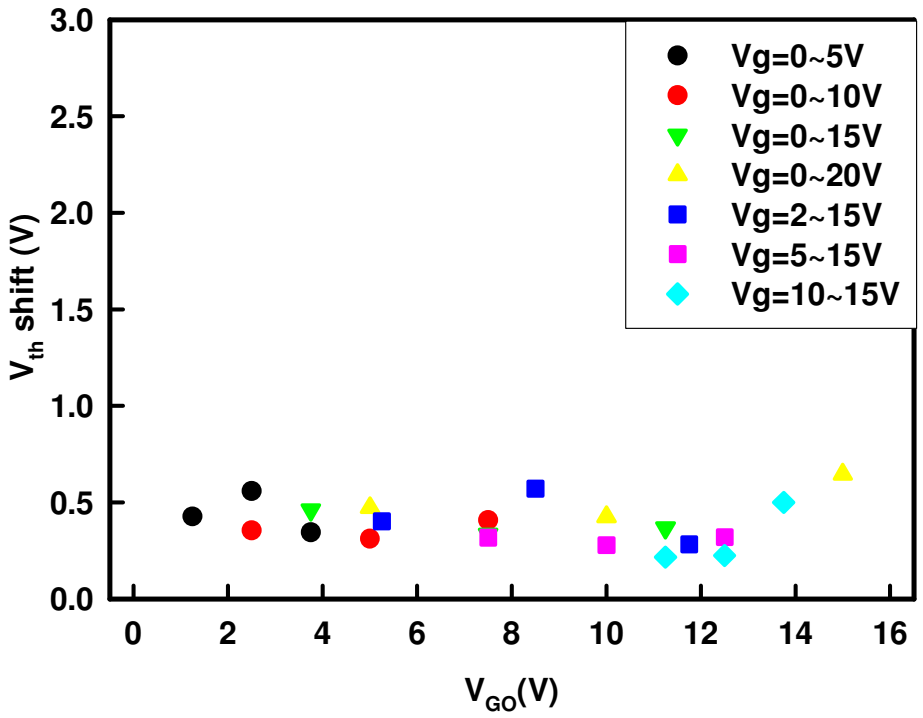


Fig 3-22(a) Dependence of Vth shift on V_{GO} with various levels and duty ratios of the gate pulse

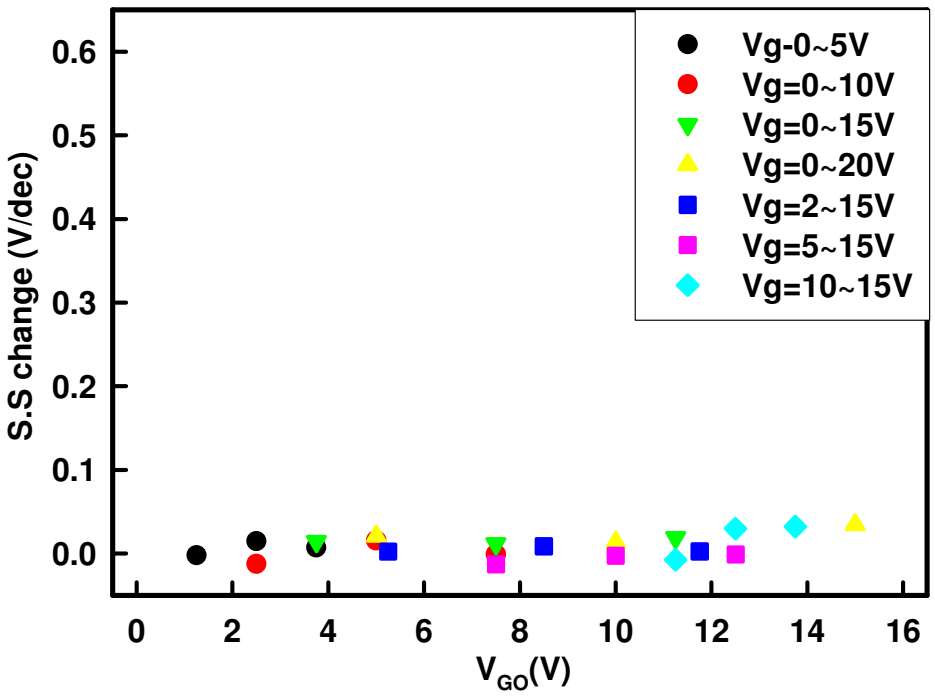
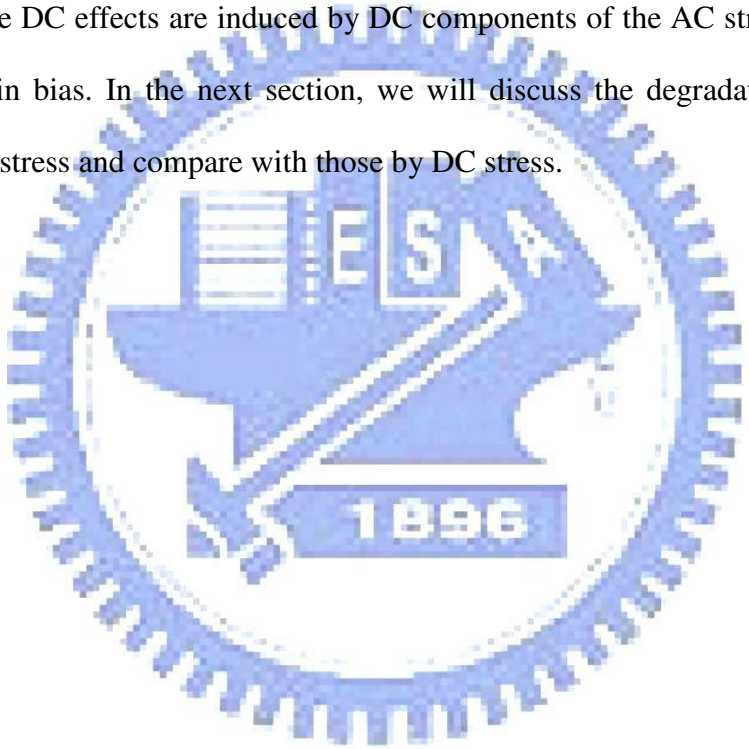


Fig 3-22(b) Dependence of S.S change on V_{GO} with various levels and duty ratios of the gate pulse

3.4.4 Summary

According to the above experiment results, the mobility degradation is not only dominated by Vg pulse level, but also depends on the duty ratio of the gate pulse. As the index is V_{GO} proposed, it is found that the degradation behavior is induced by DC components of the AC stress waveform. Otherwise, in this case of AC stress, the degradation behaviors are similar to the DC stress effect based on its offset. Therefore, it is reasonable to suppose that the degradation behaviors are attributed to the DC effects, and the DC effects are induced by DC components of the AC stress waveform with high drain bias. In the next section, we will discuss the degradation behaviors induce by AC stress and compare with those by DC stress.



3.5 Discussion

Based on the previous results and assumption, it would be essential to compare the degradation characteristic of the DC stress to that of AC stress with drain bias. First of all, let us further understand about the degradation behavior of the device under DC stress with the same drain bias.

Figure 3-23 shows the dependence of mobility degradation on various DC gate voltages with fixed Vd of 15 V stress. The dependences of V_{th} shift and *S.S* change are shown in Fig. 3-24. In the case of DC stress, the degradation is divided into two mechanisms by the stress voltage as mentioned in section 1.2.1. One is observed to be a large degradation at Vg around V_{th}, which is hot carrier effect and in consistent with the previous report [3.2]. With increase in gate voltage, the increases in the amount of V_{th} shifts and *S.S* change are induced by the other one. It is attributed to the increase of the effective vertical electrical field. Consequently, the hot carrier effect is relieved. For the gate voltage is larger than 15 V, self-heating effect could occur and then the mobility is degraded.

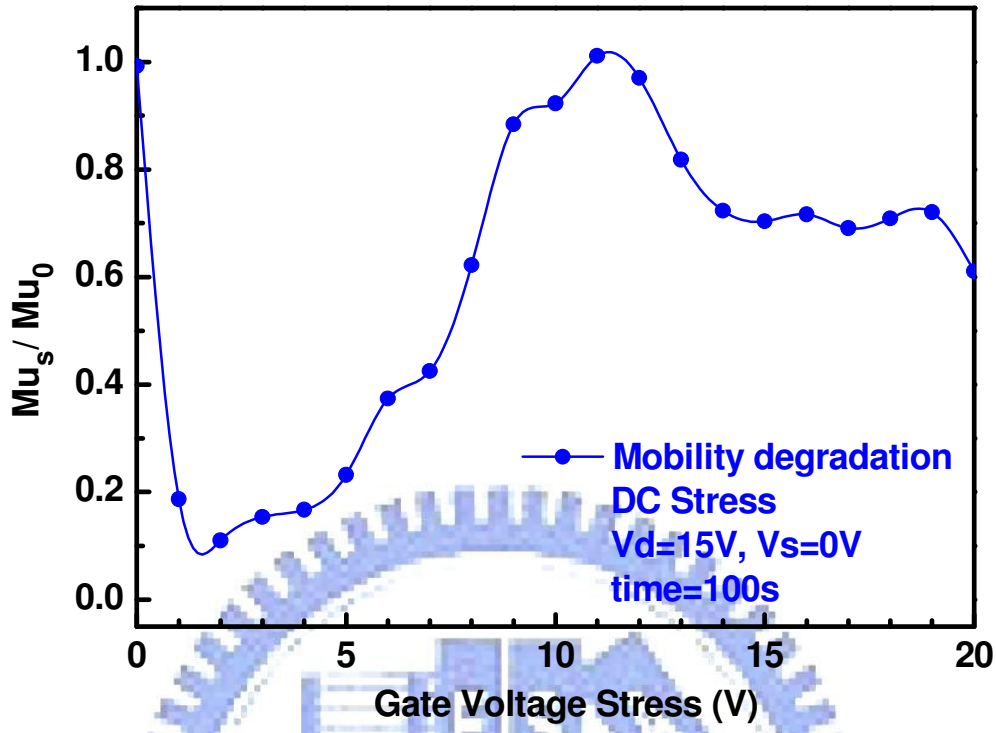


Fig. 3-23 Dependence of mobility degradation on various DC Vg with fixed Vd of 15V

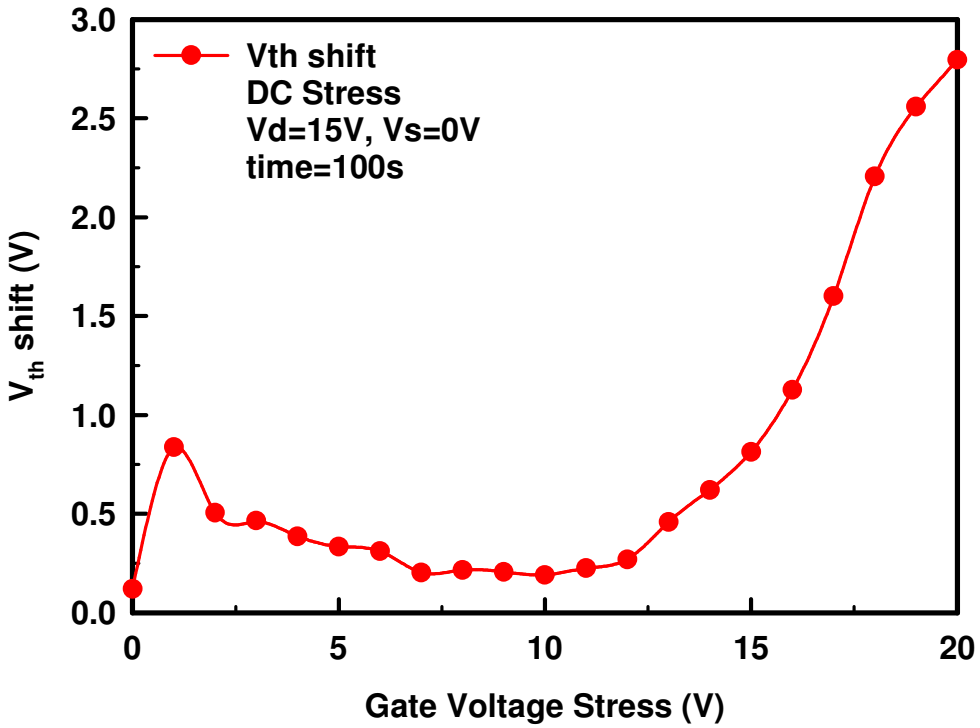


Fig. 3-24(a) Dependence of Vth shift on various DC Vg with fixed Vd of 15V

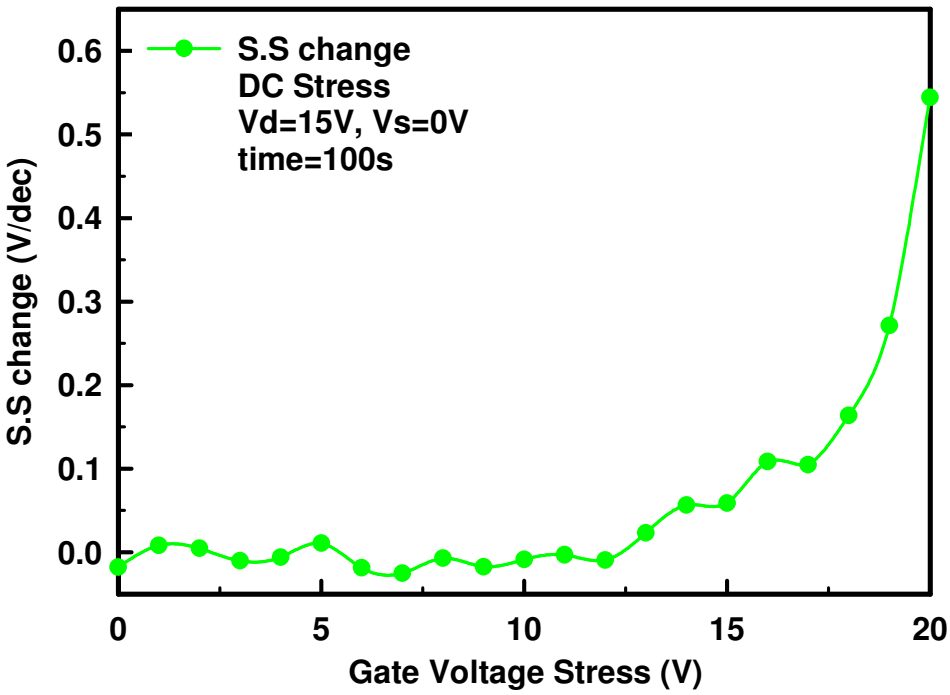


Fig. 3-24(b) Dependence of S.S change on various DC Vg with fixed Vd of 15V

Next, in order to compare the degradation behavior from the DC stress and AC stress both with large Vd, we perform the experiment conditions as set in section 3.4 with various duty ratios and plot the mobility degradation of the device stressed as the V_{GO} dependence as shown in Fig. 3-25.

It can be observed that the degradation distribution is the worst for V_{GO} is around 0~5 V and is gradually relieved at higher V_{GO}. Furthermore, the degradation dependence is similar to the DC stress described previously. Therefore, we merge the Fig. 3.25 with the Fig. 3-23 as shown in Fig. 3-26. For the degradation behavior at lower Vg/V_{GO} (Region B) and higher Vg/V_{GO} (Region A), similar dependences are observed between the DC stress and gate AC stress with drain bias. In region C, the mobility degradation of AC stress deviates from that of DC stress. The degradation on V_{th} shift and *S.S* change under AC Stress are corresponding to that under DC stress, as shown in Fig. 3-27.

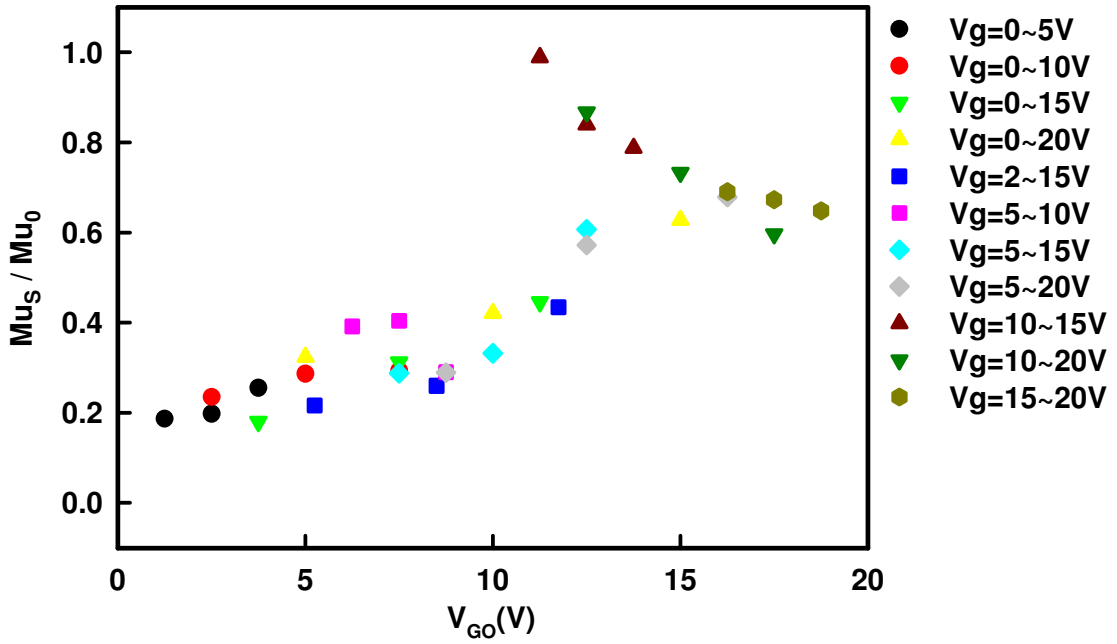


Fig 3-25 Dependence of degradation on V_{GO} of overall experiment conditions with various duty ratios

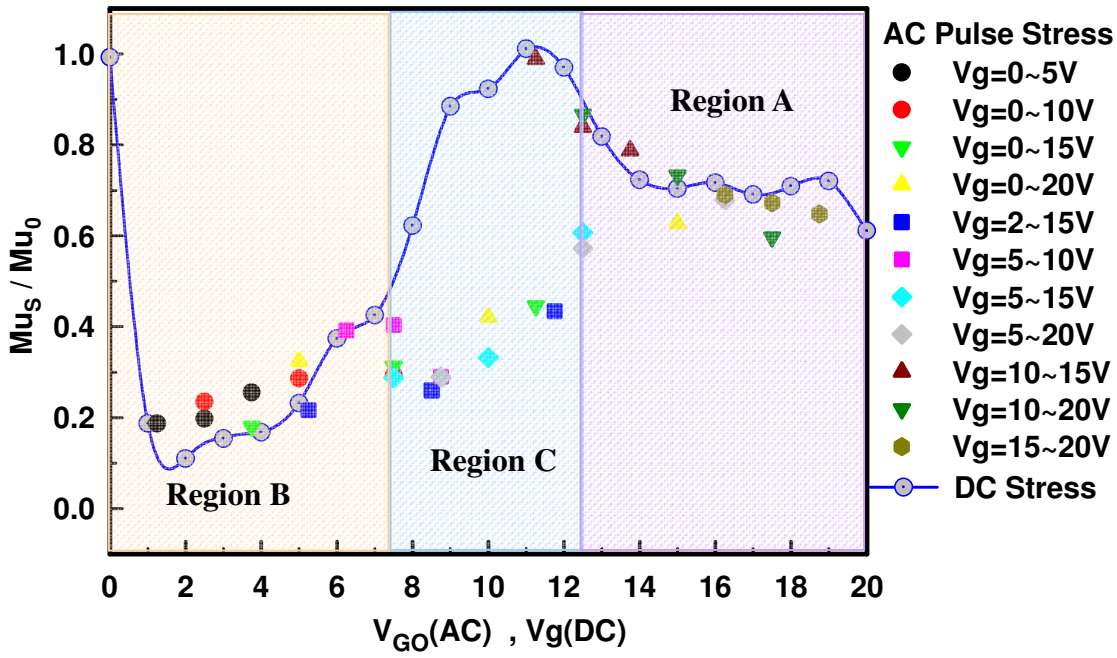


Fig. 3-26 Dependence of mobility degradation between V_{GO} under various stress conditions and Vg of DC stresses with drain bias

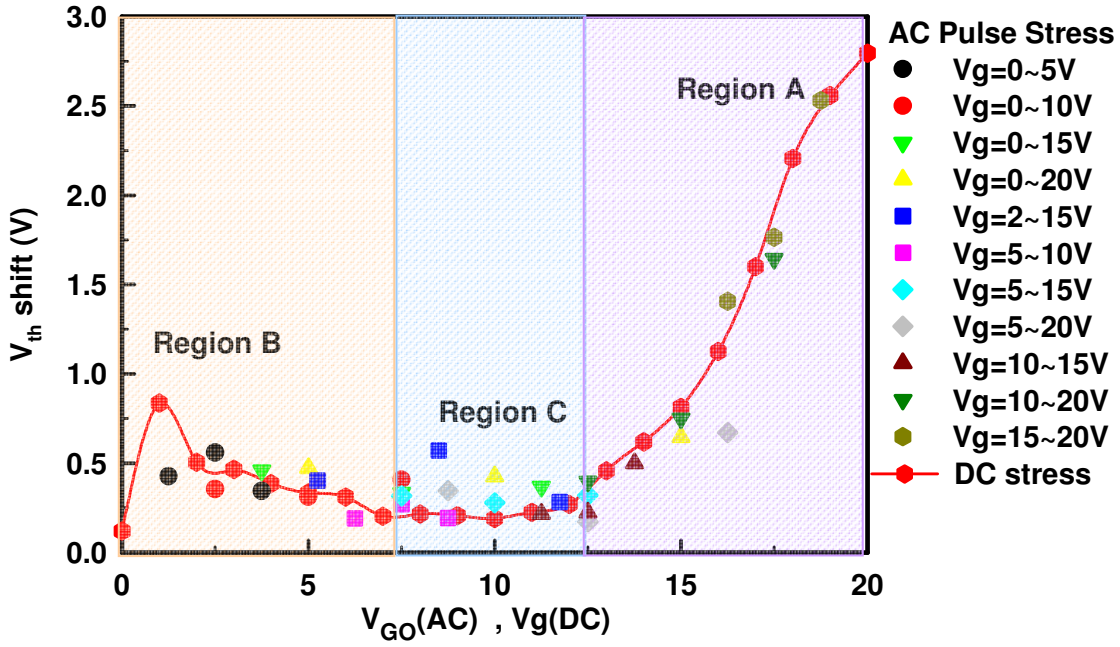


Fig. 3-27(a) Dependence of Vth shift between V_{GO} under various stress conditions and Vg of DC stresses with drain bias

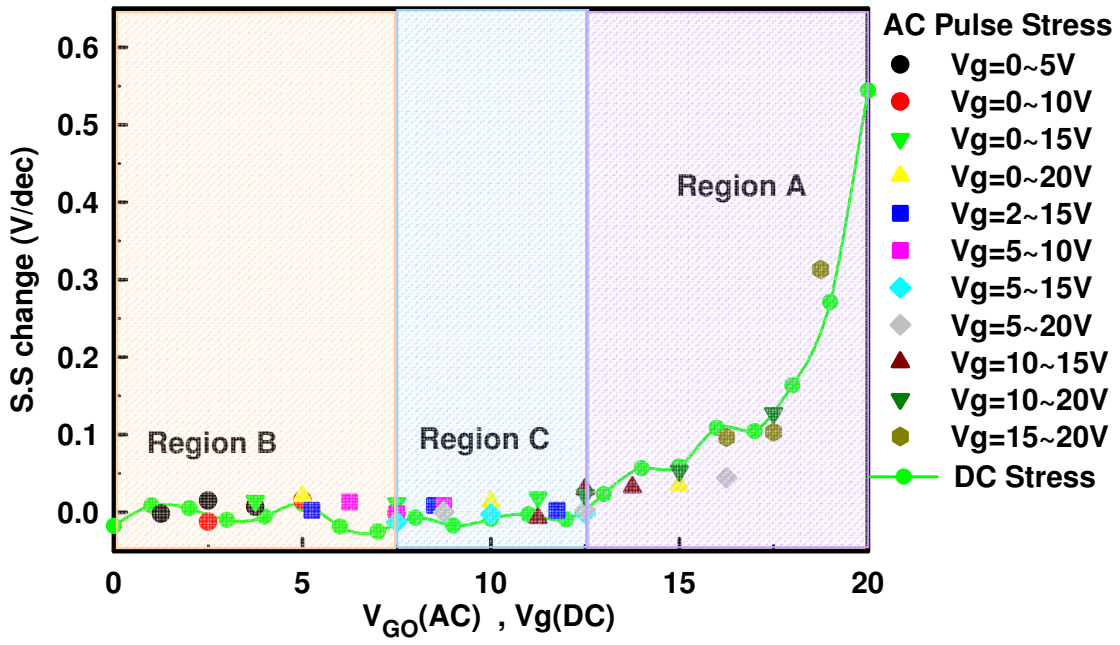


Fig. 3-27(b) Dependence of S.S change between V_{GO} under various stress conditions and Vg of DC stresses with drain bias

The results provide evidence that the mechanisms of AC stress responsible for the degradation are quite similar to those of DC stress. From this viewpoint, it appears that the degradation behaviors of gate AC stress with drain bias can be explained by the mechanisms of DC stress. In region A, the degradation behaviors are induced by the influence of self-heating effect, which is caused by higher DC components of the AC stress waveform with high drain bias. The V_{th} shift and *S.S* change are obviously increased with the increase in V_{GO}, which are consistent with high DC Vg as shown in Fig. 3-27.

On the other hand, the mobility degradation induced by DC hot carrier is most rapid for Vg near Vth as shown in Fig. 3-23. It can be explained that the DC hot carrier effect leads the degradation behaviors in region B and C due to the Vgl of stress pulse are closed to Vth. Although the degradation is dominated by Vgl in region C, the hot carrier effect will be reduced with the increase in Vgh of the pulse. As previous report, it is attributed to the increase of the effective vertical electrical field. The number of carriers available for heating is the lowest at low pulse level, and increases with high pulse level [3.3]. Consequently, self-heating effect is induced by the Vgh and large Vd, which are both over 10V. Therefore, it can be expected that the degradation behaviors in region C are not only dominated by the DC hot carrier but also affected by the DC self-heating effect.

3.6 Summary

We have investigated the degradation behavior of the N-type poly-Si TFTs under gate AC stress in the ON region with drain bias (Vd). It is discovered that the degradation is accelerated at large Vd, typically over 10 V. In addition, the degradation depends on number of gate pulse repetition but does not depend on transient time of pulse. According to the results of the pulse profile for the degradation dependence, it is obtained that the degradation is dominated by DC components of the AC stress waveform and is dependent on duty ratio of the AC pulse.

On the basis of the comparison between the DC stress and AC gate stress both with large Vd, we proposed a new index V_{GO} to estimate the equivalent DC Vg. It is further found that the features of hot carrier effect and self-heating effect in DC stress are corresponding to gate AC stress with drain bias (Vd). The results provide evidence that the mechanisms of AC stress responsible for the degradation are quite similar to those of DC stress. Therefore, it is reasonable explained that the degradation behaviors under ON region gate AC operation with Vd are attributed to the DC effects based on its offset.

Chapter 4 Conclusion

In this thesis, the degradation behavior of the N-type poly-Si TFTs under gate AC stress in the ON region with drain bias is investigated. Degradation is examined for various conditions of AC gate pulse and DC drain bias. In the case of AC stress, the significant degradation is observed at large drain bias. It is observed that the degradation is dependent on number of gate pulse repetition but is not affected by the rising time and falling time of gate pulse. In addition, the degradation behaviors are induced by DC components of the AC stress waveform with high drain bias and depend on duty ratio of the AC pulse.

Moreover, a new index V_{GO} is proposed to compare with the degradation behavior between the DC stress and AC gate stress both with large drain bias. The features of hot carrier effect and self-heating effect in DC stress are corresponding to the gate AC stress with drain bias. It appears that the degradation behaviors of gate AC stress with drain bias can be explained by the mechanisms of DC stress. Base on the similarity between the DC stress and AC gate stress, the reliability of poly-Si TFTs dynamically operated in the ON region could be simply estimated from its reliability behavior under DC stress conditions.

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