國立交通大學

電機學院光電顯示科技產業研發碩士班

碩 士 論 文

低溫複晶矽薄膜電晶體在閘極關閉區脈衝電壓及汲極直流偏壓下的劣化研究

Study of LTPS TFTs Degradation under Gate Pulse Stress in OFF Region with Drain Bias

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中 華 民 國 九十六 年 十二 月

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摘要

低溫複晶矽薄膜電晶體 (poly-Si TFTs) 與非晶矽薄膜電晶體 (a-Si TFTs) 相比，具有較高的驅動電流，這是因爲電子在複晶矽的傳輸速度較快、膜品質也較優良，因而可以使薄膜電晶體的尺寸更小，並增加顯示器的亮度及減少功率消耗。另外，低溫多晶矽薄膜電晶體可在玻璃基板上嵌入驅動元件，並且大幅減少驅動 IC 的空間，更提升液晶顯示面板的特性及可靠度，使面板的製造成本降低，因此它的發展將使顯示系統可以整合在玻璃基板上。然而，TFT 在系統面板中的電路之操作是多樣而動態的；因此，為了保證產品的壽命，TFT 在這些操作條件的可靠度必須加以探討。

在這篇論文中，我們排除了 overshooting 的效應，進一步研究了低溫複晶矽薄膜電晶體在閘極 (gate) 關閉區脈衝電壓、及不同汲極 (drain) 直流偏壓下的劣化情形。對 N-type TFTs 而言，當閘極電壓是在 ±15V 內操作、且源極 (source) 和汲極端接地時，元件的劣化只會和閘極脈波下降的時間有關，和上升的時間不相關；但是如果閘極交流電壓的操作範圍小於臨界電壓、又源極和汲極端接地時，元件的劣化會同時和閘極脈波上升及下降的時間有關。對 P-type TFTs 而言，則是和 N-type

TFTs 劣化情形不同，當閘極電壓是在 ±15V 內操作、且源極和汲極端接地時，元件的劣化只會和閘極脈波上升的時間有關，和下降的時間不相關；但是如果閘極電壓的範圍是從 0V 掃到 15V、又源極和汲極端接地時，元件的劣化會和閘極脈波上升及下降的時間皆不相關。

且根據實驗結果發現，對 N-type 和 P-type 在閘極關閉區脈衝電壓、汲極端加偏壓的情形，劣化會隨著汲極端偏壓的加大而更趨嚴重，且源極和汲極會產生不同的劣化行為。然而，P-type 不論在電流－電壓、還是電容－電壓曲線的劣化，都不如 N-type 明顯。同時元件的劣化也會和閘極電壓的範圍有關，而閘極電壓的上升時間和下降時間效應，因為汲極端的偏壓會產生其他影響，使得上升時間和下降時間的效應不明顯。

Study of LTPS TFTs Degradation under Gate Pulse Stress in OFF Region with Drain Bias

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ABSTRACT

The driving current of panel of low temperature polycrystalline silicon thin film transistors (LTPS TFTs) is higher than the amorphous silicon thin film transistors (a-Si TFTs). The fast mobility in the good film of LTPS TFTs can make the size of TFTs small. Therefore, the display luminance can be increased and power consumption can be reduced. Furthermore, LTPS TFTs can be used to implement active circuits on single glass substrates and diminish spaces of active IC. It not only promotes the characteristic and reliability in liquid crystal display, but also comes down the manufacturing cost. So, it makes display systems with integrated circuit on the glass substrates to be feasible. However, the operation of the TFTs in the circuit of display system can be diverse and dynamic. Therefore, to insure the lifetime of the product, the reliability of TFTs under such kinds of operation conditions must be studied.

In this thesis, the device degradation of low-temperature polycrystalline thin film

transistor under gate AC stress in off region with different drain bias has been investigated where the overshooting effect is prevented. For the N-type TFTs under the stress of gate voltage swinging from -15V to 15V with source and drain grounded, the device degradation depends on the falling time of gate pulse, but not on the rising time. However, under the stress of gate voltage lower than the threshold voltage, the degradation is dependent on both the rising time and falling time of the gate signal. For the P-type TFTs under the stress of gate voltage swinging from -15V to 15V with source and drain grounded, the device degradation depends on the rising time of gate pulse, but not on falling time. However, under the stress of gate voltage swinging from 0V to 15V, the degradation is independent of the rising time and falling time.

For the N-type and P-type TFTs under gate AC stress in off region with drain bias, the degradation becomes worse with increasing drain voltage. It results in different degradation behaviors near the source and drain regions. The I-V and C-V characteristic of P-type TFTs are not that much degraded than those of N-type TFTs. With the increase of the range of gate pulse, the degradation also increases. The applied drain voltage may introduce the effects of large electric field near the drain. In contrast, the effects of rising time and falling time are not obvious.

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Chapter 1

Introduction

1.1 Overview of Low-Temperature Polycrystalline Silicon Thin Film Transistors (LTPS TFTs)

Nowadays, the amorphous silicon (a-Si) thin film transistors (TFTs) are commonly used to be the switches of the pixel in active matrix liquid crystal displays (AMLCDs). Fig. 1-1 shows the block diagram of active matrix display. All the driver chips are buried together with the other application-specified ICs on PCB because the current driving capacity of a-Si TFTs is not good enough for the system integration. However, the integration of driver circuitry with display panel on the same substrate is very desirable not only to reduce the module cost but to improve the system reliability.

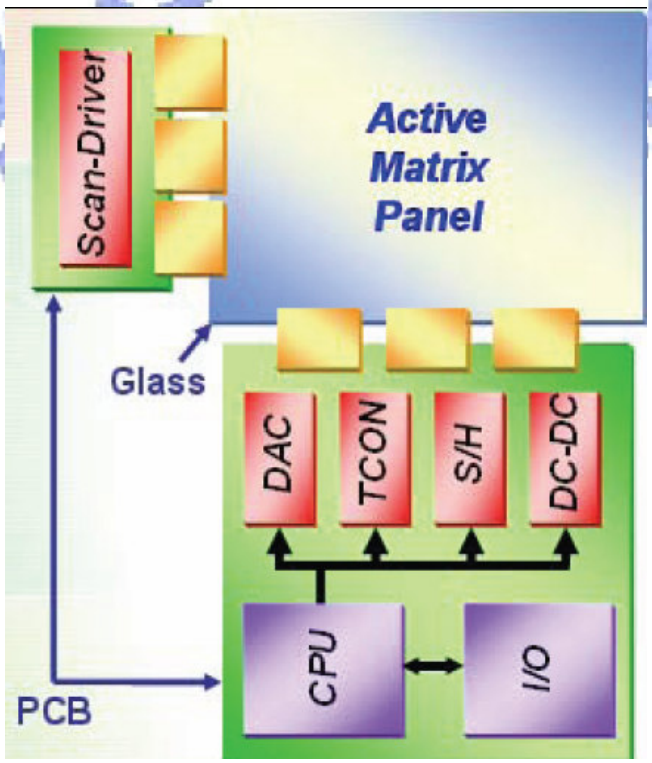

Fig. 1-1 The block diagram of active matrix display

For this reason, low-temperature polycrystalline silicon (poly-Si) thin film transistors (TFTs) have attracted much attention because they have been used very successfully for active matrix displays, such as active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting displays (AMOLEDs). Except large area displays, poly-Si TFTs have been applied into some memory device such dynamics random access memories (DRAMs), static random access memories (SRAMs), and have great potential for 3-dimension IC applications.

Compared with conventional a-Si TFTs, the field effect mobility of poly-Si TFTs is much higher. In polysilicon film, the carrier mobility larger than 100cm^2/Vs can be easily achieved, which is about 100 times larger than that of the conventional amorphous-silicon TFTs (typically below 1cm^2/Vs). Higher field effect mobility means transistors can provide higher driving current. The higher driving currents can allow the pixel-switching element TFT's dimension shrinkage, resulting in higher aperture ratio and lower parasitic gate-line capacitance for improved display performance. Besides, the superior mobility performance allows the integration of both the active matrix pixel switching elements and the peripheral driving circuitry on the same glass substrate, which brings the era of system-on-glass (SOG) that will include a memory, central processing unit (CPU), and display on the same glass. In this way, the process complexity can be greatly simplified and manufacturing cost can be substantially reduced. The ability of fabricating high-performance low temperature poly-Si (LTPS) TFTs enables their use in a wide range of new applications. Therefore, there is a great interest in improving the performance of LTPS TFTs.

In comparison with signal-crystalline silicon, poly-Si film contains many grain boundary defects and intra-grain defects. The order of poly-Si grain size is about 0.3um. At present, when poly-Si TFTs are used in LCD applications, the minimum channel length is typically much larger than 3μm, and therefore a large number of grain boundaries are

present in the channel. Electrons are scattered at the grain boundaries or trapped by the interface states, leading to lower mobility than in single crystal silicon. Much effort has been made to increase the performance of LTPS TFTs. Crystallization of a-Si thin films has been considered the most critical process for fabricating high-performance LTPS TFTs. Among various crystallization technologies, excimer laser crystallization has become the mainstream technology for mass production of flat panel displays (FPDs) because of high throughput, low temperature process compatible with glass substrate, and formation of high-quality poly-Si.

In summary, it is expected that the poly-Si TFTs will become increasingly important in future technology, especially when the 3-D circuit integration and SOG era is coming. There are lots of interesting and important topics that are worthy to be researched.

1.2 Review of Degradation Model for TFT under AC Stress

In order to realize the new applications for LTPS TFTs, we have to improve the performance such as enhancing mobility, decreasing the threshold voltage of TFTs, and shrinking the TFTs size. However, the poly-Si TFT reliability improvements are as critical for the insurance of product lifetime. Therefore, reliability testing and understanding of reliability mechanisms become very necessary.

In previous reports, Toyota *et al*. proposed that mobile carriers are able to follow the transient variation of gate voltage while the electrons trapped in the midgap state aren't. In addition, Uraoka *et al*. attributed the dominant AC degradation mechanism to hot electrons generated by trapped electrons exposed to the high electric field and gain energy from the electric field during AC stress. The mechanism was analyzed by using a pico-second

emission microscope and device simulation to examine the transient current experimentally and theoretically, respectively.

The earlier degradation model under AC stress is described as follow. As for the N-type TFTs, when the gate voltage is high of Vg=15V (ON state), the electrons gather to form a channel, as shown in Fig. 1-2 (a). When the gate voltage drops from Vg=15V to -15V (ON→OFF), the electrons in the channel move rapidly to the source and drain, as shown in Fig. 1-2 (b). Some of the trapped electrons are exposed to the high electric field and gain energy from the field. Hot electrons are generated at this moment and form electron traps, as shown in Fig. 1-2 (c), and a density of state (DOS) in tail edge of poly-Si is increased by the hot electrons.

As for the P-type TFTs, when the gate voltage is low of Vg=-15V (ON state), the holes gather to form a channel, as shown in Fig. 1-3 (c). When the voltage transition from low to high of Vg=-15V to 15V (ON→OFF), the holes in the channel move rapidly to the source and drain, as shown in Fig. 1-3 (b). Carriers gain energy from this electric field and become hot carriers. Therefore, more hot electrons are generated which causes trap formation at the grain boundaries around the drain edge, as shown in Fig. 1-3 (a).

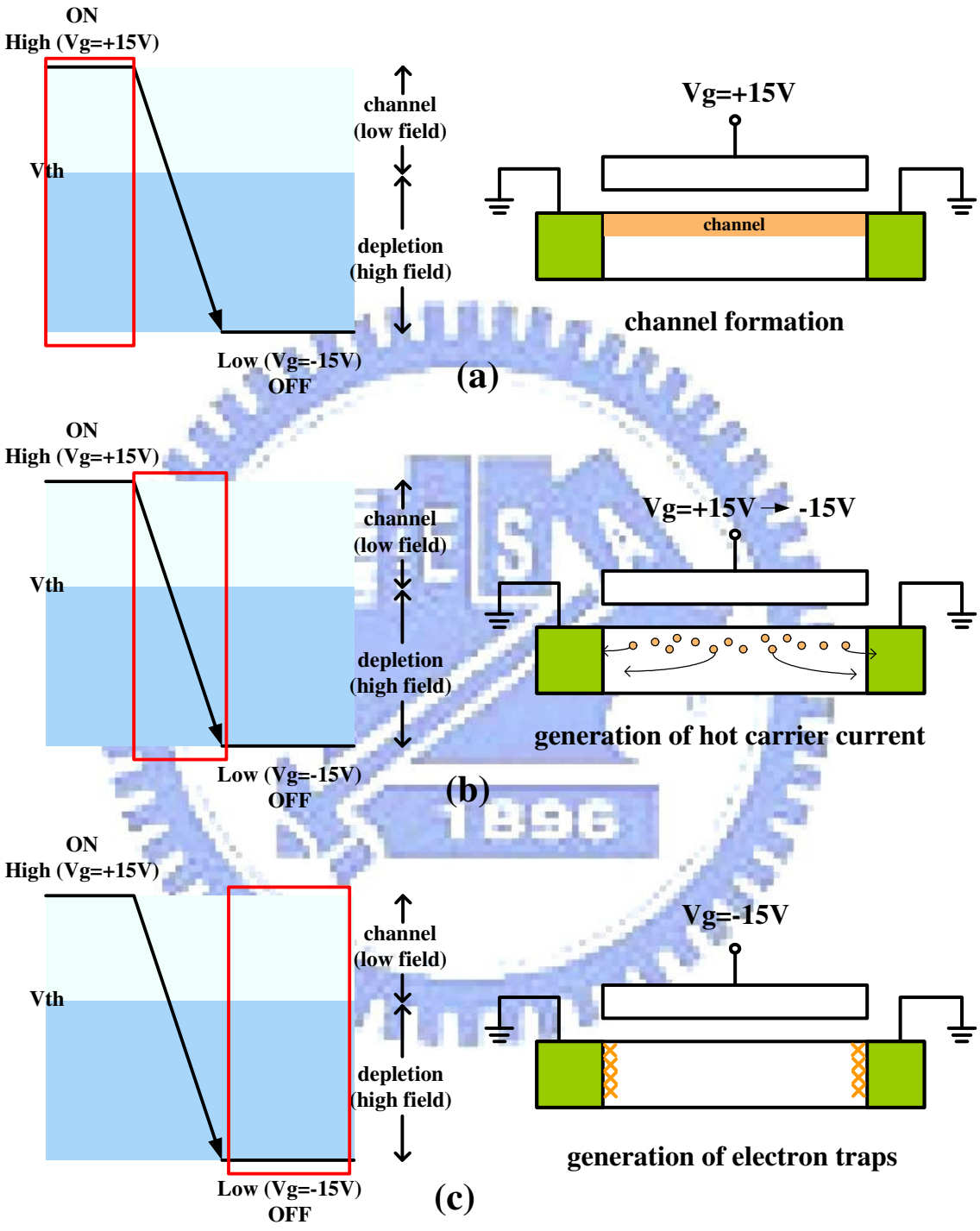

Fig. 1-2 A schematic diagram for degradation model of the N-type TFT

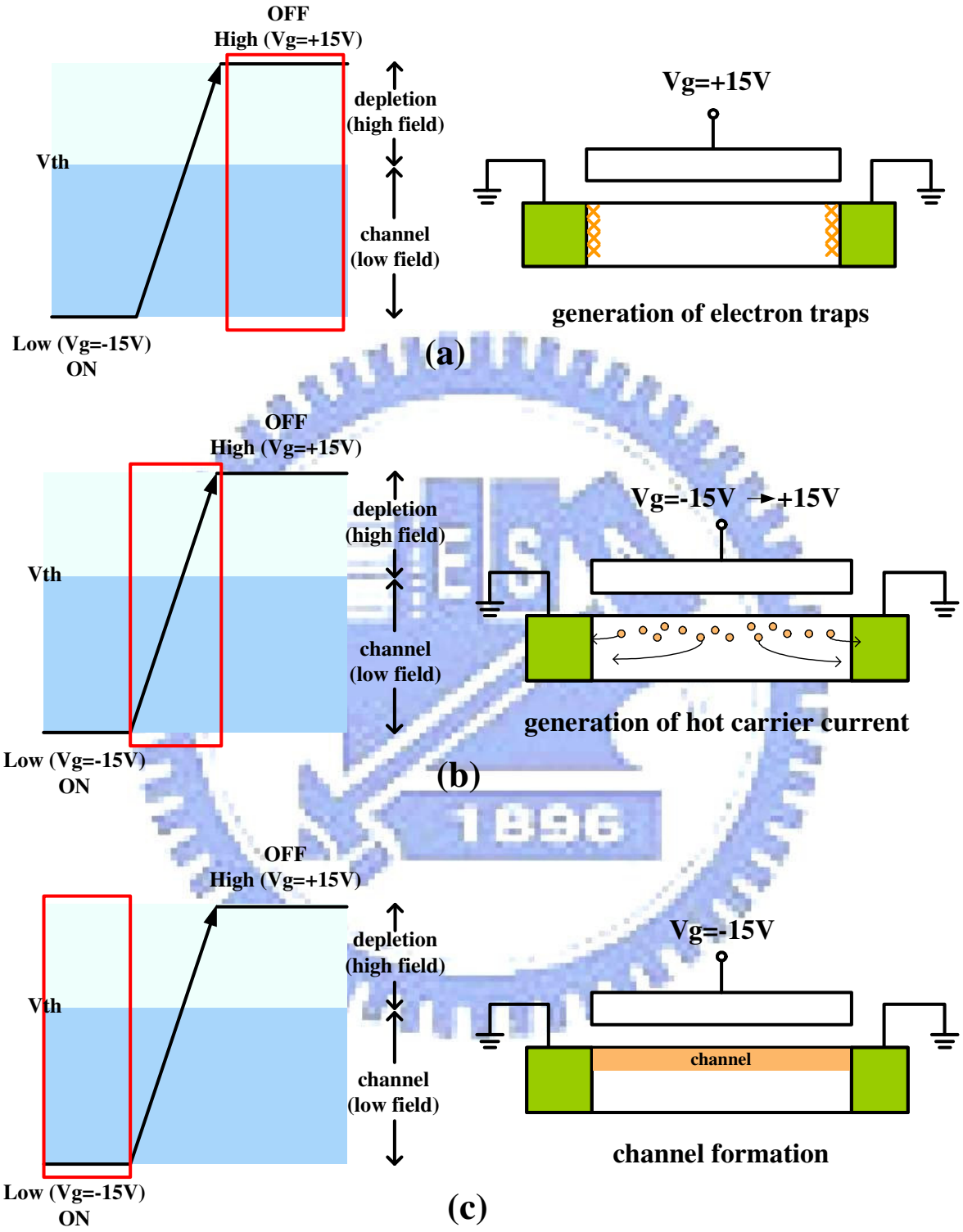

Fig. 1-3 A schematic diagram for degradation model of the P-type TFT

1.3 Motivation

The Poly-Si TFTs displays with integrated driving circuits have recently been developed. At present, the poly-Si TFTs are the best candidate to realize system on panel (SOP) and are widely considered for AMLCDs and active matrix organic light-emitting diodes (AMOLEDs).

The reliability mechanisms of LTPS TFTs under DC (direct current) bias stress and AC stress which source drain were ground have been widely discussed. However, up to now, the reliability of LTPS TFTs under gate AC stress with drain bias has been paid much less attention, shown in Fig. 1-4. In previous studies regarding AC stress, the source and drain were ground to avoid the DC effect during dynamic stress. However, when the gate of the TFT is under dynamic operation, the drain-source voltage is usually present. For example, the pixel TFTs driven by multi level gate scanning waveforms can be subject to the off-region AC stress at gate with DC drain bias.

Last, CMOS technology is necessary for driving circuits, which means that both the understanding of the reliability of N-type and P-type LTPS TFTs are necessary. Therefore, it is extremely important to understand the degradation mechanisms of N-channel and P-channel LTPS TFTs under AC stress.

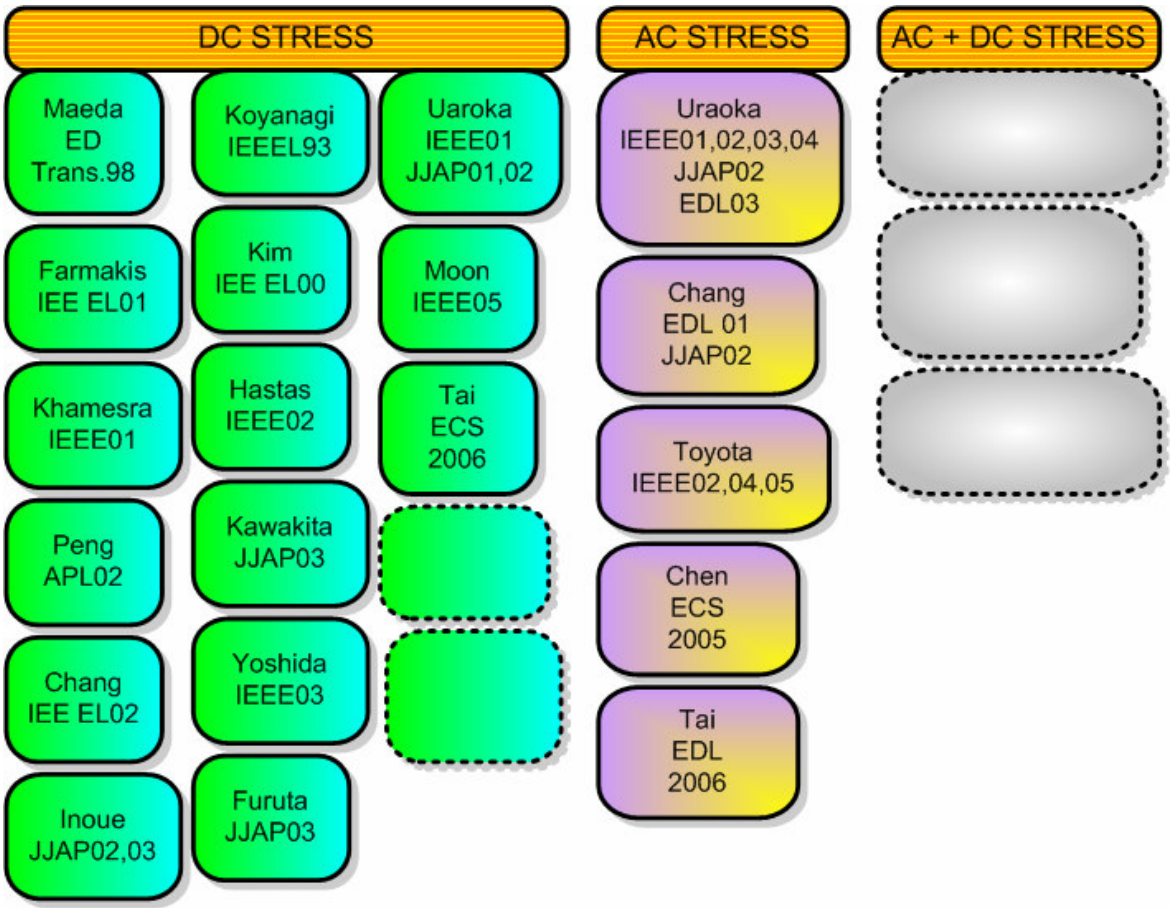

Fig. 1-4 Previous researches of LTPS TFT reliability

For the previous work in our lab (thesis of Wei-Lun Shih), it is not noticed that the applied gate signals overshoot beyond the target value we have set. Based on those results, it is found that the signal of Vgh is higher and Vgl is lower than the values we set, as shown in Fig. 1-5(a). The effect of overshooting could introduce other effect of the study of reliability.

Therefore, in this study, the overshooting is carefully avoided for the applied gate signals, as shown in Fig. 1-5(b). The degradation behavior can be free from the overshooting effect. Thus, we re-examine the degradation of N-channel and P-channel LTPS TFTs under off-region AC stress conditions with various drain bias with proper apparatus setup. The stress conditions including swing range, and falling/rising times of the gate pulse, were discussed to verify the degradation mechanism under gate AC stress

with drain bias.

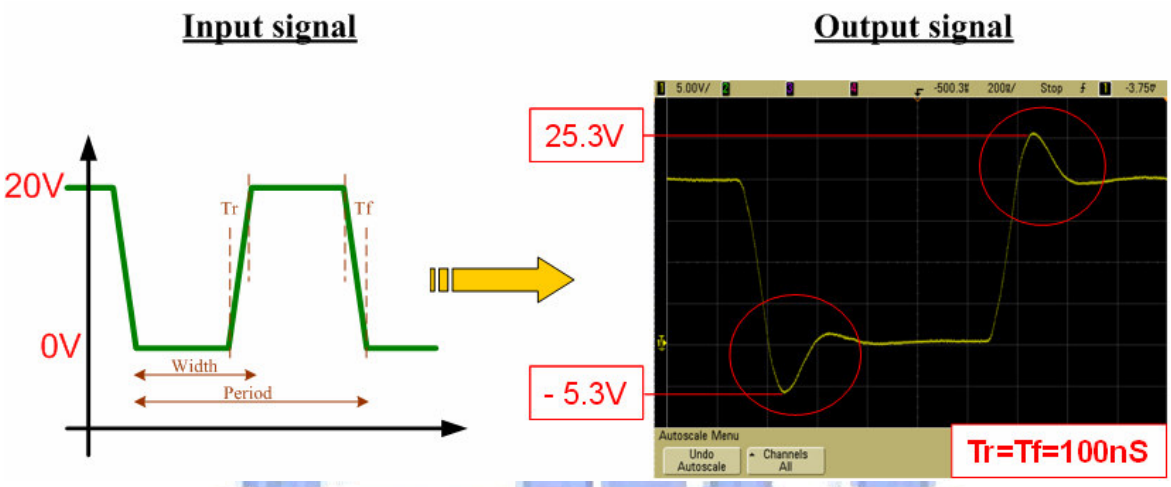

Fig. 1-5(a) the verification of output waveform with overshooting

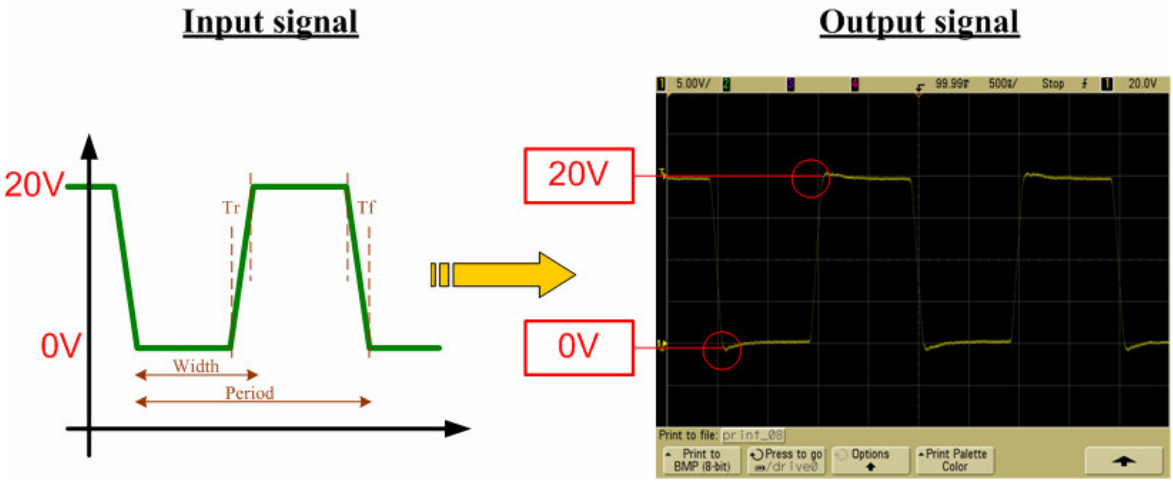

Fig. 1-5(b) the verification of output waveform without overshooting

1.4 Thesis Organization

Chapter 1 Introduction

1.1 Overview of Low-Temperature Polycrystalline Silicon Thin Film Transistors (LTPS TFTs)

1.2 Review of Degradation Model for TFT under AC Stress

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1.4 Thesis Organization

Chapter 2 Experimental Procedures

2.1 Procedures of Fabrication of LTPS TFTs

2.2 Extraction Method of Device Parameters

2.3 C-V Measurements

2.4 Stress Conditions

2.4.1 Gate Pulse Stress with Drain and Source Ground

2.4.2 Gate Pulse Stress with Drain Bias and Source Ground

Chapter 3 Degradation for Poly-Si TFT under Gate Pulse Stress with Drain and Source Ground

3.1 Frequency Dependence

3.2 Gate Voltage Leveling Dependence

3.3 Rising Time and Falling Time for Vg of ON and OFF Region

3.4 Rising Time and Falling Time for Vg in the OFF Region

Chapter 4 Degradation for N-type Poly-Si TFT under Gate Pulse Stress with Drain Bias

Chapter 2

Experimental Procedures

2.1 Procedures of Fabrication of LTPS TFTs

LTPS TFTs used in the experiment were the conventional top-gate structure and fabricated on the glass substrates. The cross-section views of N-channel and P-channel LTPS TFTs are shown in Fig 2-1 and Fig. 2-2 respectively. The basic process flow is described as follows. Firstly, the buffer oxide and a-Si:H films were deposited on glass substrates by the PECVD system. Then, XeCl excimer laser was used to crystallize a-Si:H film followed with poly-Si active area definition. Subsequently, gate insulator was deposited by PECVD. The thickness of gate oxide is 650Å. Next, the metal gate formation and source/drain doping were performed. Dopant activation and hydrogenation was carried out after interlayer dielectric deposition. Finally, contact holes formation and metallization were performed to complete fabrication work. The lightly doped drain (LDD) structure was used in the N-channel TFTs to enhance hot carrier endurance while not used in P-type devices. The width/length of the TFT was 20 μ m/5 μ m.

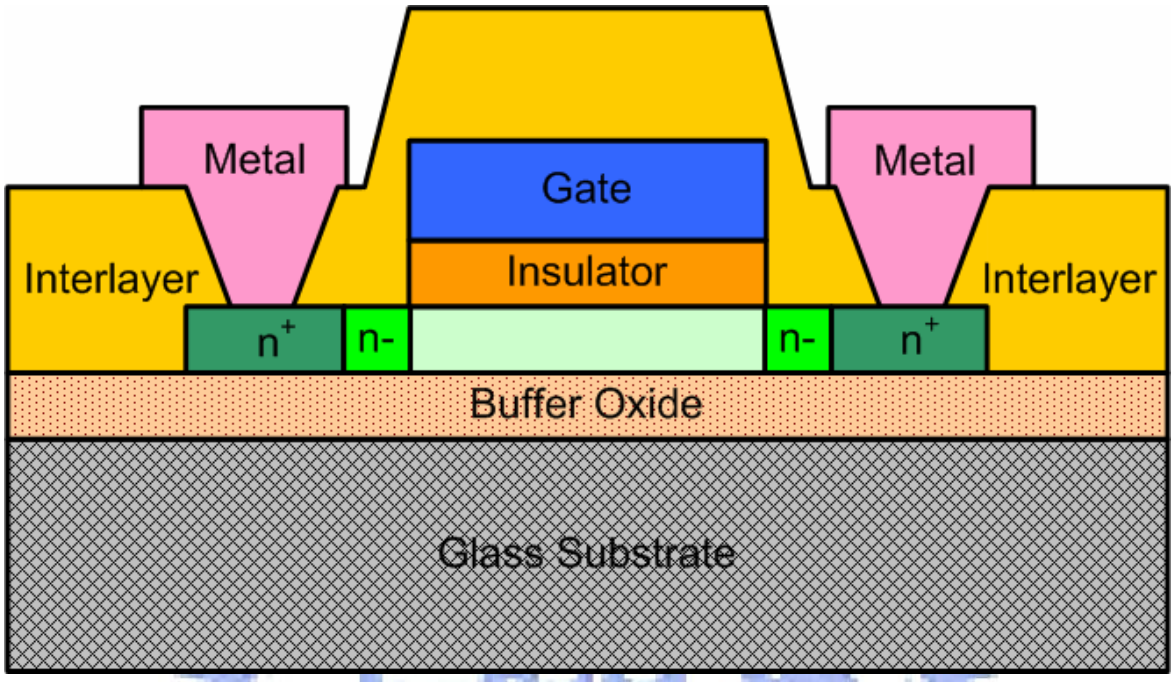


Fig. 2-1 The cross-section views of N-channel LTPS TFTs with LDD structure

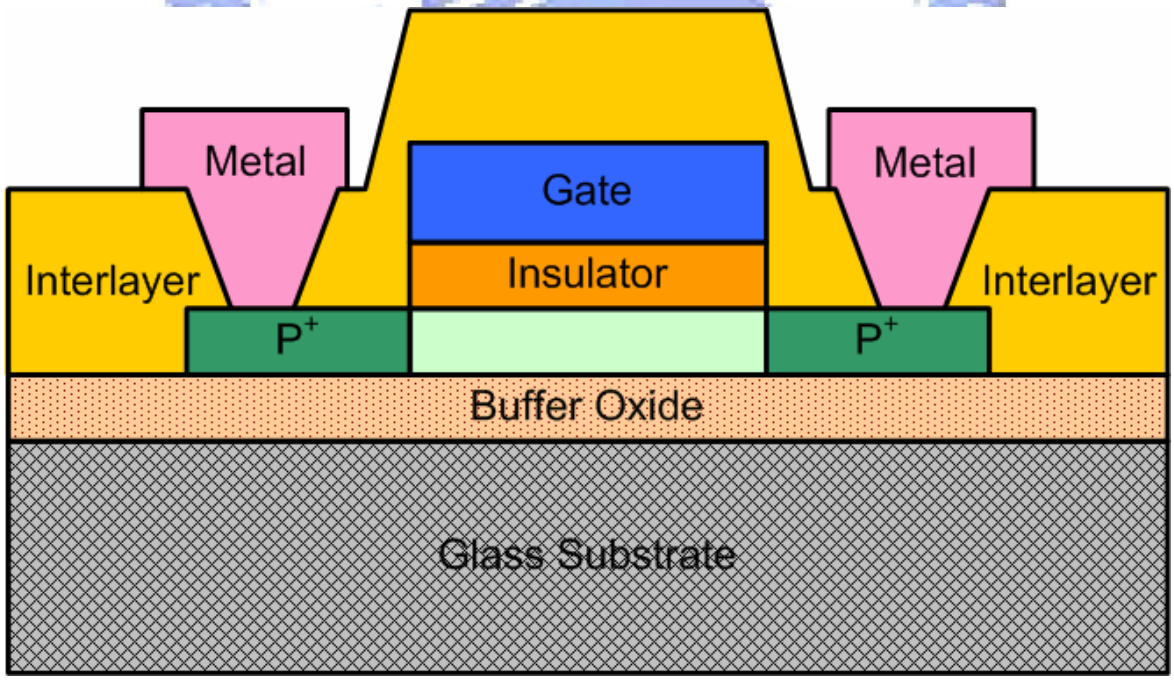


Fig. 2-2 The cross-section views of P-channel LTPS TFTs

2.2 Extraction Method of Device Parameters

The field effect mobility (Mu, μ_{FE}) is derived from the maximum value of the transconductance g_m, which can be expressed as:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}[(V_G - V_{th})V_D - \frac{1}{2}V_D{}^2] \quad (2\text{-}1)$$

Where

C_{ox} is the gate capacitance per unit area,

W is channel width,

L is channel length,

V_{th} is the threshold voltage.

If the drain voltage V_D is much smaller as compared with $(V_G - V_{th})$ (i.e. $V_D << V_G - Vth$), then the drain current can be approximated as:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}(V_G - V_{TH})V_D \quad (2\text{-}2)$$

And the transconductance is defined as:

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const.} = \frac{WC_{ox}\mu_{FE}}{L}V_D \quad (2\text{-}3)$$

Therefore, the field effect mobility can be expressed as:

$$\mu_{FE} = \frac{L}{C_{ox}WV_D} g_m \quad (2\text{-}4)$$

In other words, the field-effect mobility can be extracted by taking the maximum value of the g_m into (2-4) when $V_D = 0.1V$.

For most of the researches on TFT, the constant current method is widely-used to determine the threshold voltage (V_{th}). The threshold voltage in the thesis is determined from this method, which extracts V_{th} from the gate voltage at the normalized drain current $I_N = I_D/(W_{eff} - L_{eff}) = 10nA$ for $|V_{DS}| = 0.1V$.

2.3 C-V Measurements

Since the I-V transfer curves show the entire characteristics of the whole channel and may not distinguish the dominant mechanism, C-V measurements were further employed to investigate the asymmetry electric field at the source and drain of TFTs during the stress.

The C-V curves of the normalized gate-to-drain capacitance (C_{GD}) and the normalized gate-to-source capacitance (C_{GS}) before and after stress at different stress conditions were measured with the Agilent 4284Aprecision LCR meter. The normalized capacitance is the ratio of the measured capacitance to a constant of 60fF, which is the gate oxide capacitance of the TFT under test.

Since it is difficult to observe the defect position in TFTs with the I-V characteristic, the C-V measurement is used to examine the information about position and type of degradation in the device after stress. For instance, if carriers are trapped by defects, C-V curve stretch out slightly, or if states are generated additionally, C-V curve increase somewhat in the depletion region. Besides, the C−V curves are helpful to identify whether the dominant mechanism of degradation is the increase of fixed charges or trap states.

2.4 Stress Conditions

The Agilent 4156A semiconductor parameter analyzer with pulse generator was used to measure the I-V curve and stress the device with different conditions. The basic parameters of AC signal consists of frequency (F), signal high level (Vgh), signal low level (Vgl), high-level time (T_Vgh), low-level time (T_Vgl), rising time (Tr), and falling time (Tf). Fig 2-3 shows the waveform of the AC signal. In AC signal, the definition of individual parameter is given as above:

$$T = Tr + T\_vgh + Tf + T\_vgl \quad (2\text{-}5)$$

$$F = 1/T \quad (2\text{-}6)$$

$$\text{Duty ratio} = (Tr + T\_vgh)/T \quad (2\text{-}7)$$

where T is the signal period.

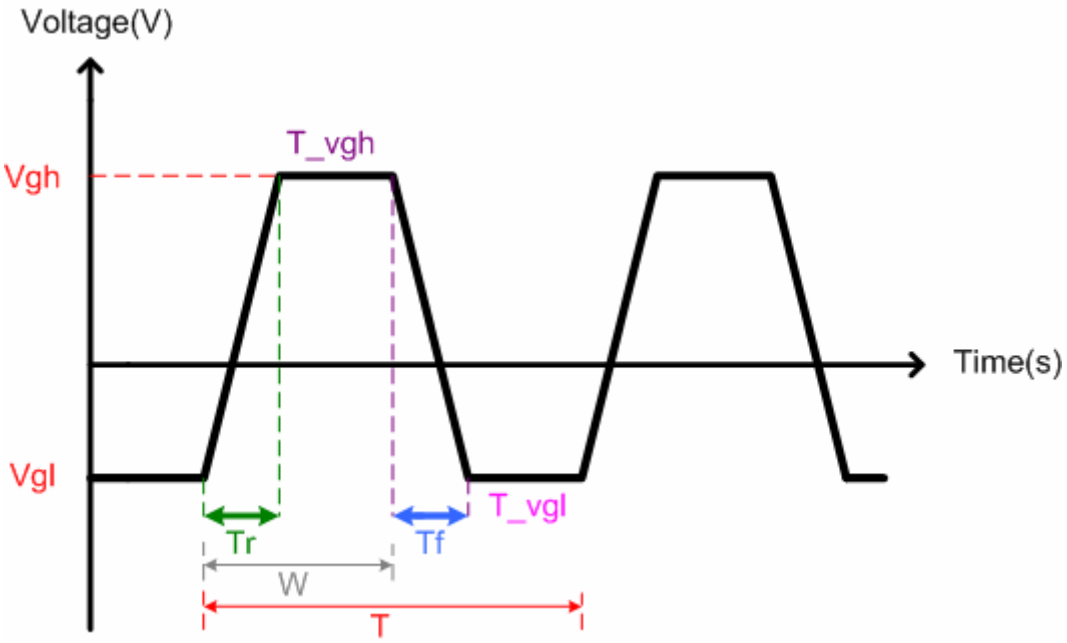


Fig. 2-3 Waveform and definition of the AC signal

2.4.1 Gate Pulse Stress with Drain and Source Ground

Under AC stress, pulse voltage was applied to the gate electrode and source and drain were grounded, which is shown in Fig. 2-4. The standard stress condition in the experiment is the gate voltage swing of -15V to 15V, F = 500 kHz, Tr and Tf are both 100ns, and duty ratio is 50%. These parameters can be adjusted and then various stress conditions on the gate electrode were performed to examine the reliability of LTPS TFTs.

To investigate which parameter of the stress parameters dominates the degradation of the N-channel and P-channel TFTs transfer characteristics, we will make four experiments.

Firstly, we change frequency from 0.5KHz to 500KHz. Secondly, we change Vgh and Vgl of AC signal fixed amplitude of 15V at one time, called Vg leveling. Thirdly, we will change Tr and Tf from 100ns to 700ns for gate swing range of -15V to 15V. And finally, we want to understand the effects of Tr and Tf for the gate swing in the depletion region. The experimental conditions are shown in Table 2-1 and Table 2-2. It will be investigated for reliability testing in the chapter 3.

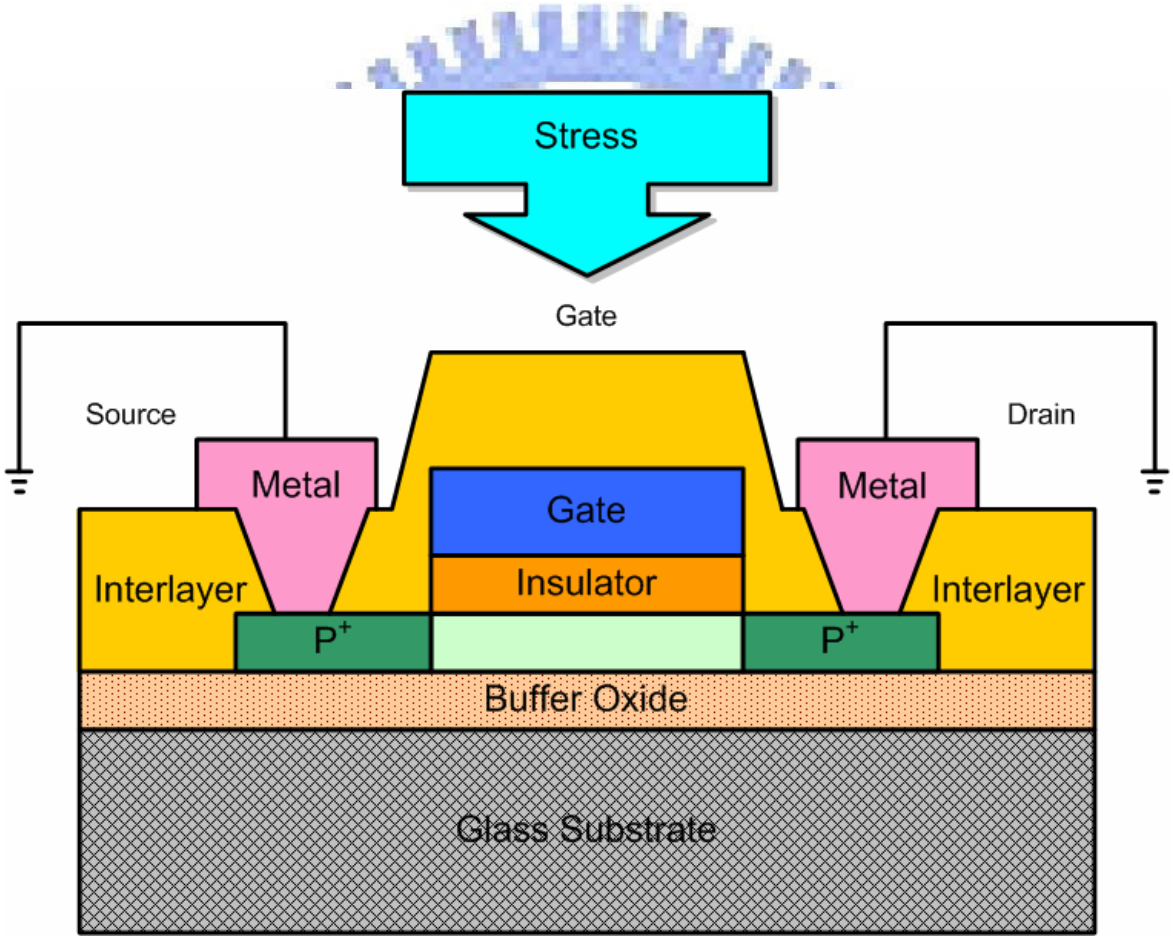


Fig. 2-4 TFT under AC stress with source and drain grounded

Table 2-1 The experiment condition forms for N-type under gate pulse with drain and source ground

Experiments	Gate Voltage Pulse(V)	Vd.Vs(V)	Frequency(Hz)	Rising Time(ns)	Falling Time(ns)
Frequency	-15V~15V	0V	0.5K,5K,50K,500K	100	100
Gate Voltage Leveling	-15V~0V,-13V~2V, -7.5V~7.5V, -2V~13V,0V~15V, 2V~17V,7.5V~22.5V	0V	500K	100	100
Tr (ON.OFF)	-15V~15V	0V	500K	100,300,700	100
Tf (ON.OFF)	-15V~15V	0V	500K	100	100,300,700
Tr (OFF)	-15V~0V	0V	500K	100,300,700	100
Tf (OFF)	-15V~0V	0V	500K	100	100,300,700

Table 2-2 The experiment condition forms for P-type under gate pulse with drain and source ground

Experiments	Gate Voltage Pulse(V)	Vd.Vs(V)	Frequency(Hz)	Rising Time(ns)	Falling Time(ns)
Frequency	15V~-15V	0V	0.5K,5K,50K,500K	100	100
Gate Voltage Leveling	0V~15V,-2V~13V, -7.5V~7.5V, -13V~2V,-15V~0V, -17V~-2V	0V	500K	100	100
Tr (ON.OFF)	15V~-15V	0V	500K	100,300,700	100
Tf (ON.OFF)	15V~-15V	0V	500K	100	100,300,700
Tr (OFF)	0V~15V	0V	500K	100,300,700	100
Tf (OFF)	0V~15V	0V	500K	100	100,300,700

2.4.2 Gate Pulse Stress with Drain Bias and Source Ground

In the second part of experiment, pulse voltage was applied to the gate electrode in off region with drain DC while source is grounded, which is shown in Fig. 2-5. The standard stress condition in the experiment includes the gate voltage swing of -15V to 0V for N-type, 0V to 15V for P-type, F = 500 kHz, Tr and Tf are both 100ns, and duty ratio is 50%. These parameters can be adjusted to perform then various stress conditions.

Firstly, V_D is changed from 0V to 20V for N-type and 0V to -20V for P-type, to study the effect of drain voltage under gate AC stress. Secondly, we change Vgl from -5V to -20V for N-type and Vgh from 5V to 20V for P-type, to investigate the effect of gate voltage range. Thirdly, we change Tr and Tf from 100ns to 700ns, to understand the transient time dependence. The stress conditions in this thesis are summarized in Table 2-3 and Table 2-4. It will be investigated for reliability testing in the chapter 4 and chapter 5.

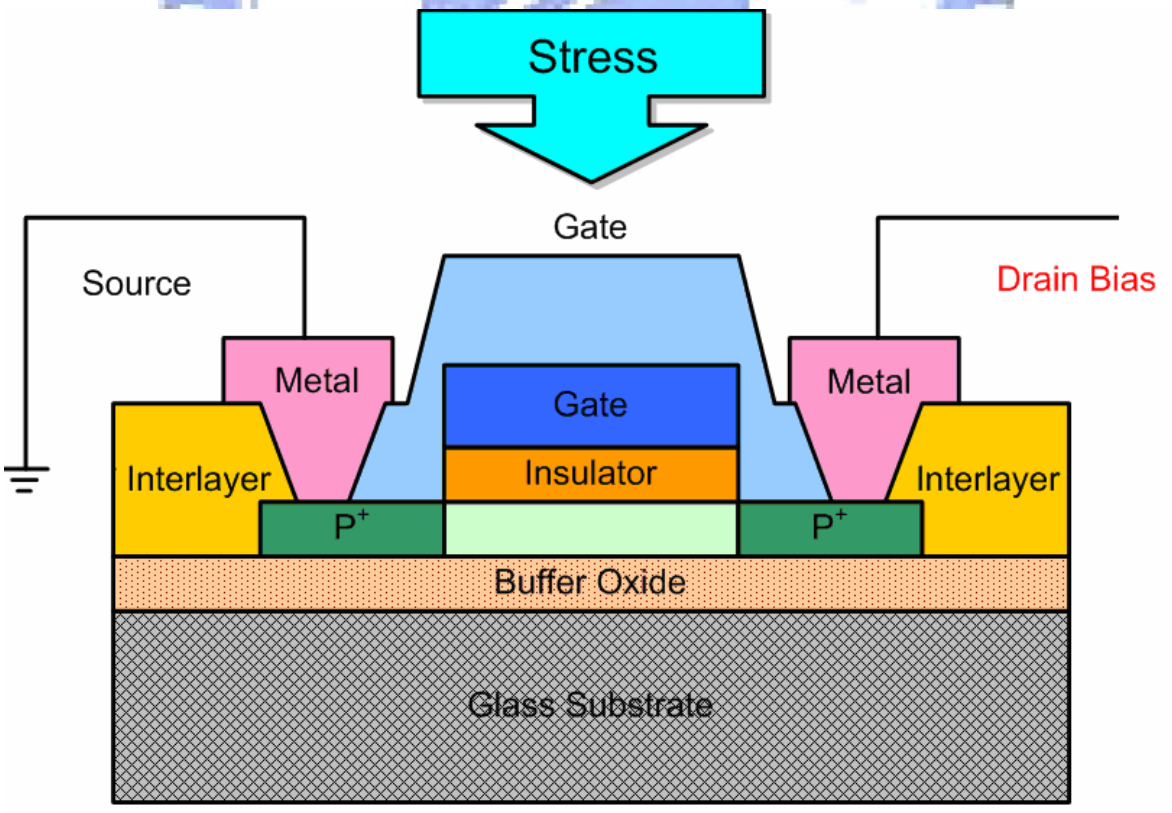


Fig. 2-5 TFT under AC stress with drain bias and source ground

Table 2-3 The experiment condition forms for N-type under gate pulse with drain bias and source ground

Experiments	Gate Voltage Pulse(V)	Drain Voltage(V)	Frequency(Hz)	Rising Time(ns)	Falling Time(ns)
Frequency	-15V~15V	20V	0.5K,5K,50K,500K	100	100
Drain Bias	-15V~15V	0V,5V,10V,15V,20V	500KHz	100	100
Drain Bias	-15V~0V	0V,5V,10V,15V,20V	500KHz	100	100
Gate Voltage Range	-5V,-10V,-15V,-20V~0V	20V	500KHz	100	100
Rising Time(ON.OFF)	-15V~15V	20V	500KHz	100,300,700	700
Rising Time(OFF)	-15V~0V	20V	500KHz	100,300,700	700
Falling Time(ON.OFF)	-15V~15V	20V	500KHz	700	100,300,700
Falling Time(OFF)	-15V~0V	20V	500KHz	700	100,300,700

Table 2-4 The experiment condition forms for P-type gate pulse with drain bias and source ground

Experiments	Gate Voltage Pulse(V)	Drain Voltage(V)	Rising Time(ns)	Falling Time(ns)
Drain Bias	0V~15V	0V,-5V,-10V,-15V,-20V	100	100
Gate Voltage Range	0V~5V,10V,15V,20V	-20V	100	100
Rising Time(ON.OFF)	-15V~15V	-20V	100,300,700	700
Rising Time(OFF)	0V~15V	-20V	100,300,700	700
Falling Time(ON.OFF)	-15V~15V	-20V	700	100,300,700
Falling Time(OFF)	0V~15V	-20V	700	100,300,700

Chapter 3

Degradation for Poly-Si TFT under Gate Pulse Stress with Drain and Source Ground

3.1 Frequency Dependence

Dependence of the device degradation on frequency for N-channel and P-channel TFT is shown in Fig. 3-1(a) and Fig. 3-1(b). The degradation are respectively expressed as the ratio of increased and decreased mobility (μ) for N and P-channel TFTs to their initial mobility (μ_0). μ_0 and μ are derived from the maximum transconductance at the drain voltage of 0.1 V (N-channel) and -0.1V (P-channel) before and after stress. For N-channel TFT, when the frequency increases from 0.5KHz to 500KHz, the mobility decreases. For P-channel TFT, when the frequency increases, the mobility slightly increases.

The changes are re-plotted with the number of pulses for N-channel and P-channel TFT , as shown in Fig. 3-2(a) and Fig. 3-2 (b). Independent of the frequency, the degradation of all lines exhibits almost the universal relationship with the number of pulses. The figure clearly indicates the relationship between the degradation and the repetition number and the independence of the frequency. In other words, the degradation arisen by the unchanging voltage can be ignored.

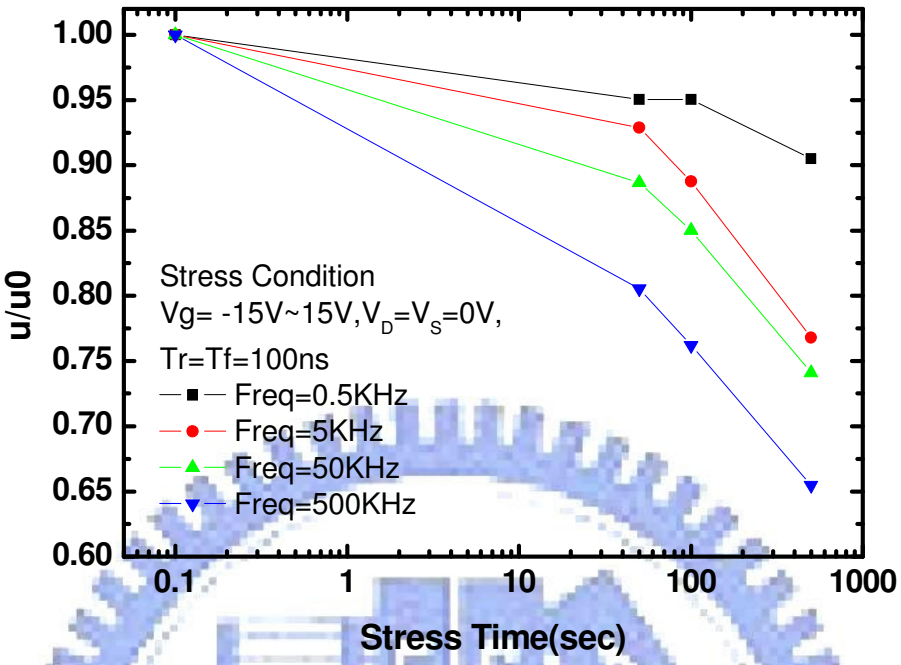


Fig. 3-1(a) **Frequency dependence of degradation of N-channel TFT under gate pulse with drain and source ground**

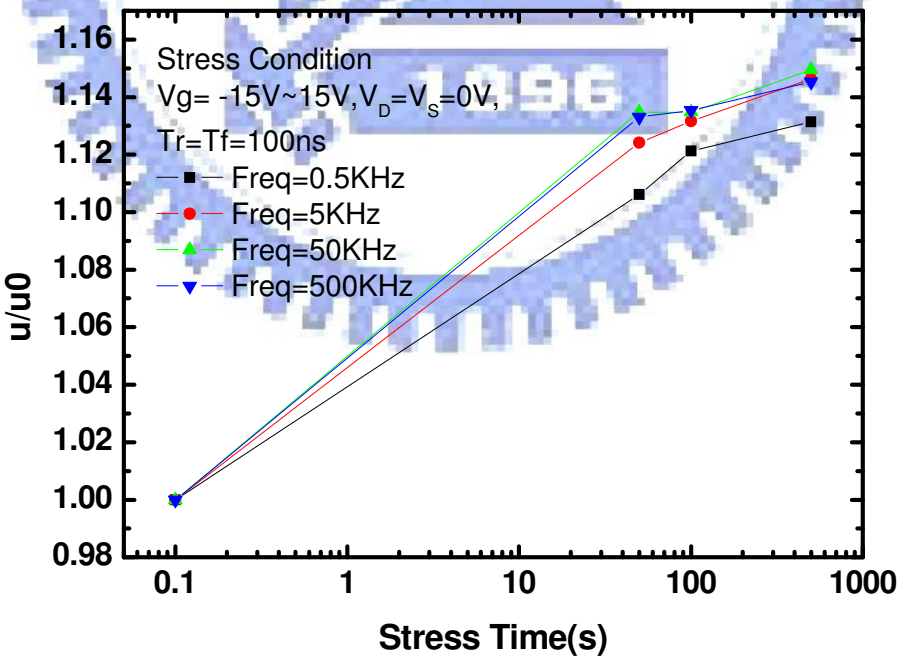


Fig. 3-1(b) **Frequency dependence of degradation of P-channel TFT under gate pulse with drain and source ground**

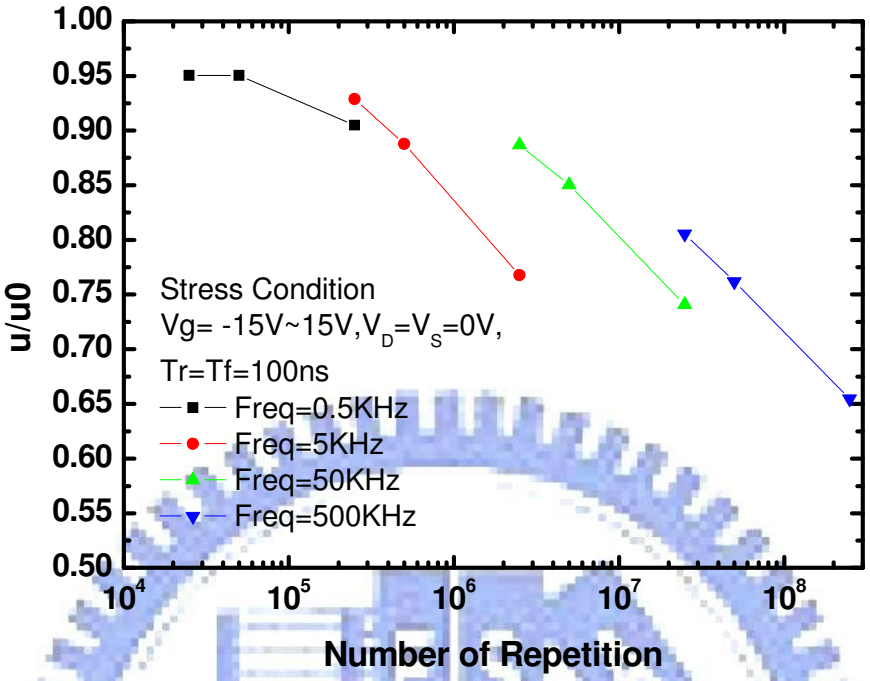


Fig. 3-2(a) **Dependence on the number of pulse repetitions of N-channel TFT under gate pulse with drain and source ground**

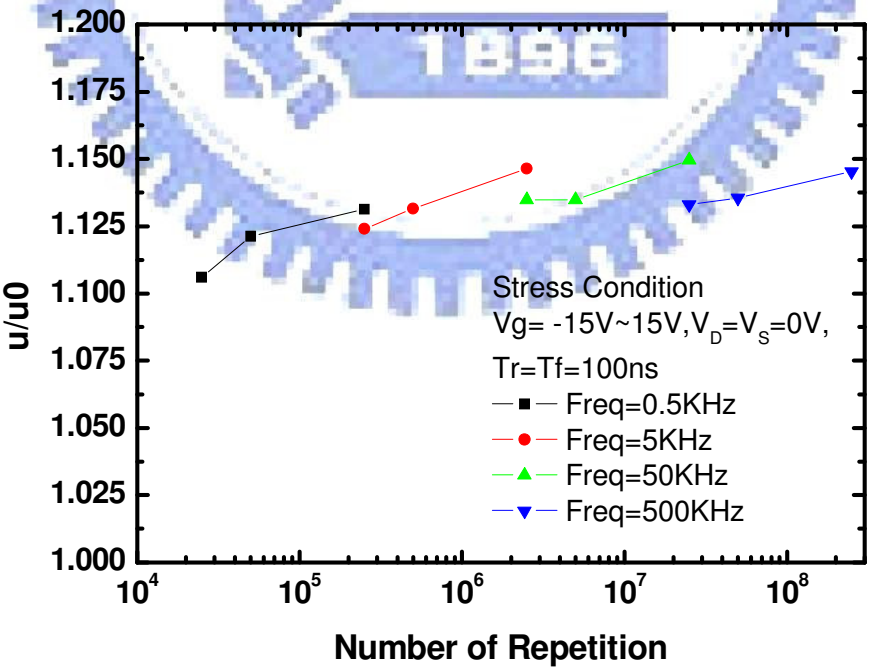


Fig. 3-2(b) **Dependence on the number of pulse repetitions of P-channel TFT under gate pulse with drain and source ground**

3.2 Gate Voltage Leveling Dependence

The range of the gate pulse swing is separated into two parts according to the threshold voltage, as shown in Fig. 3-3(a) and Fig. 3-4(a). In the ON region, the channel is formed, while in the OFF region, the channel was fully depleted. Fig. 3-3(b) and Fig. 3-4(b) clearly indicates that the degradation of mobility strongly depends on the levels of the gate voltage. For the gate pulse swing in the ON region, the degradation is very small, however, that for the gate pulse swing fully in the OFF region become large. It is because the transient electrical field is high in the OFF region, but that is very low in the ON region. Carriers can gain energy from high electrical field and become hot carriers, and the traps are generated.

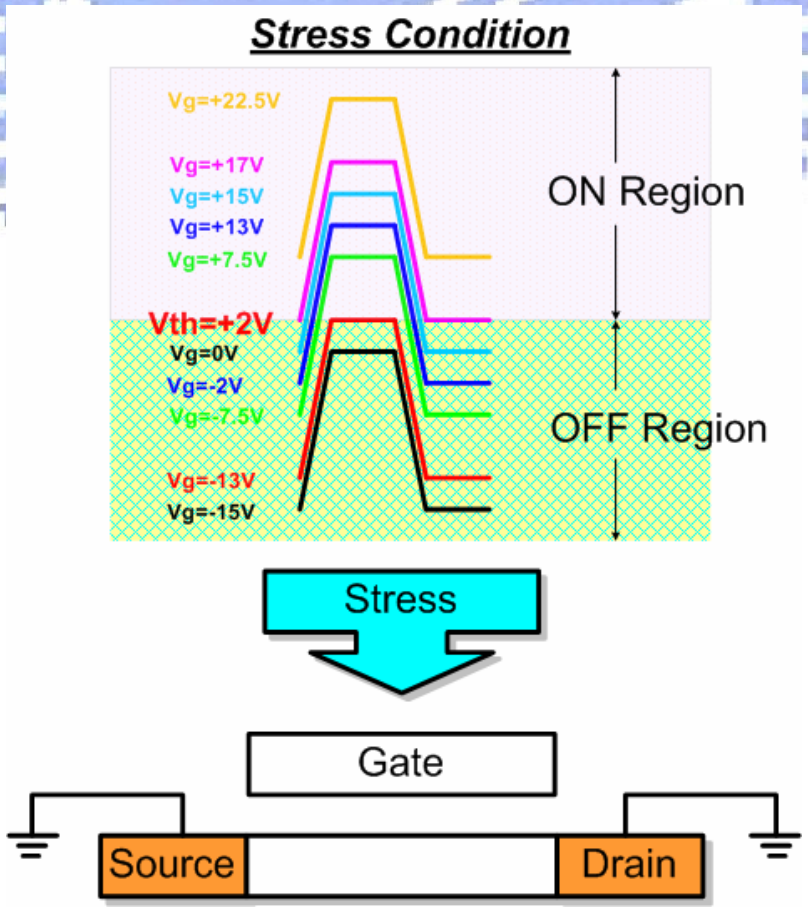


Fig. 3-3(a) Swing region for N-channel

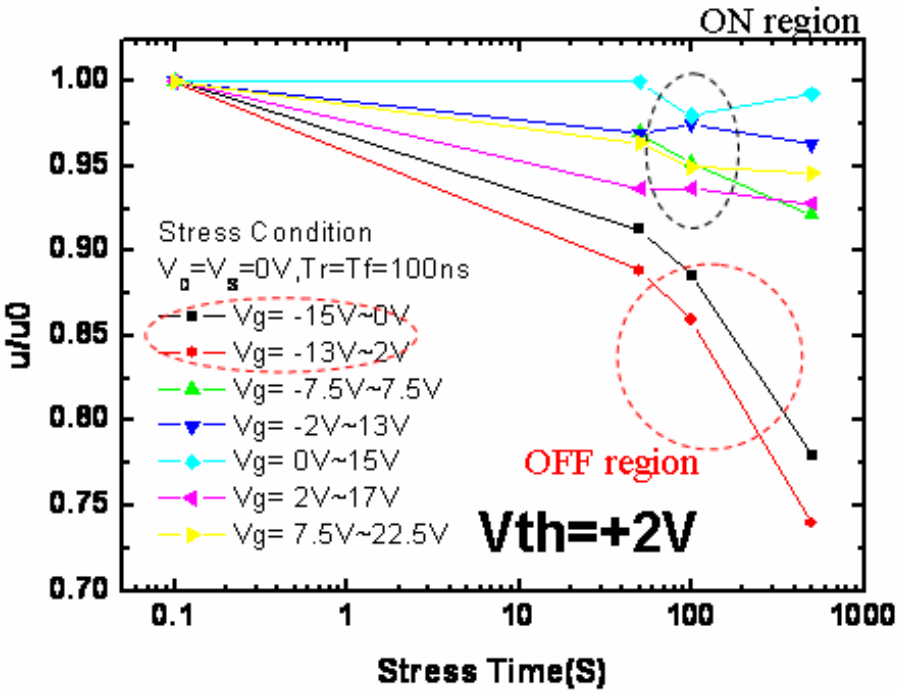


Fig. 3-3(b) Dependence of degradation on swing region for N-channel TFT

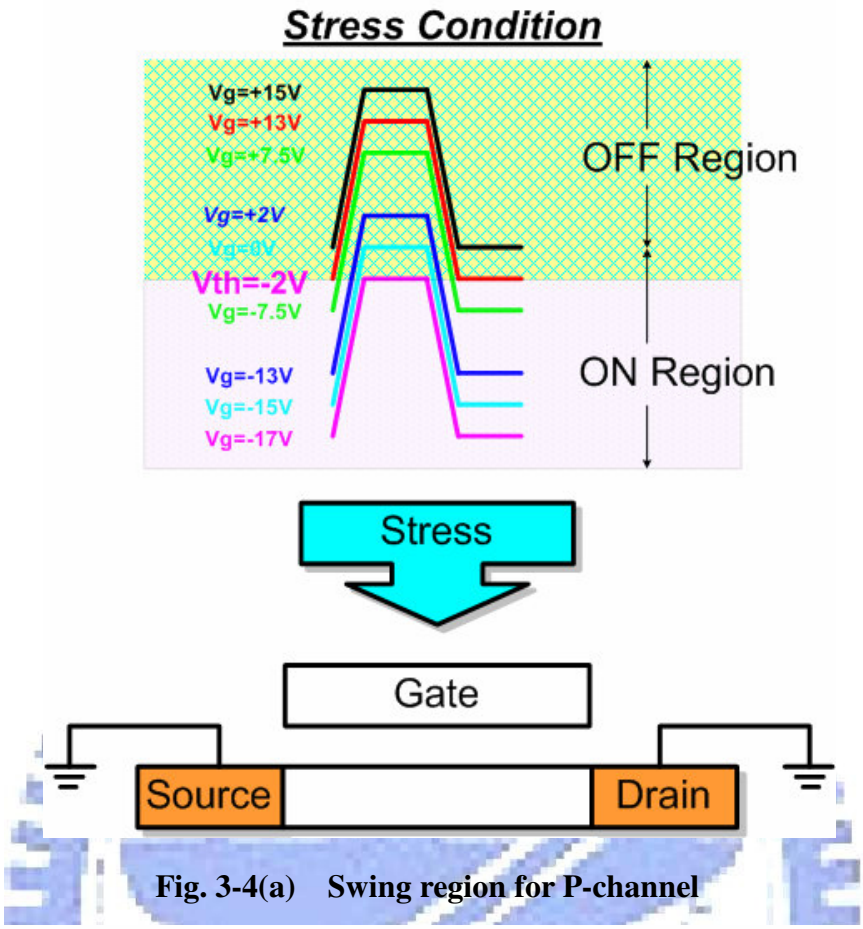


Fig. 3-4(a) Swing region for P-channel

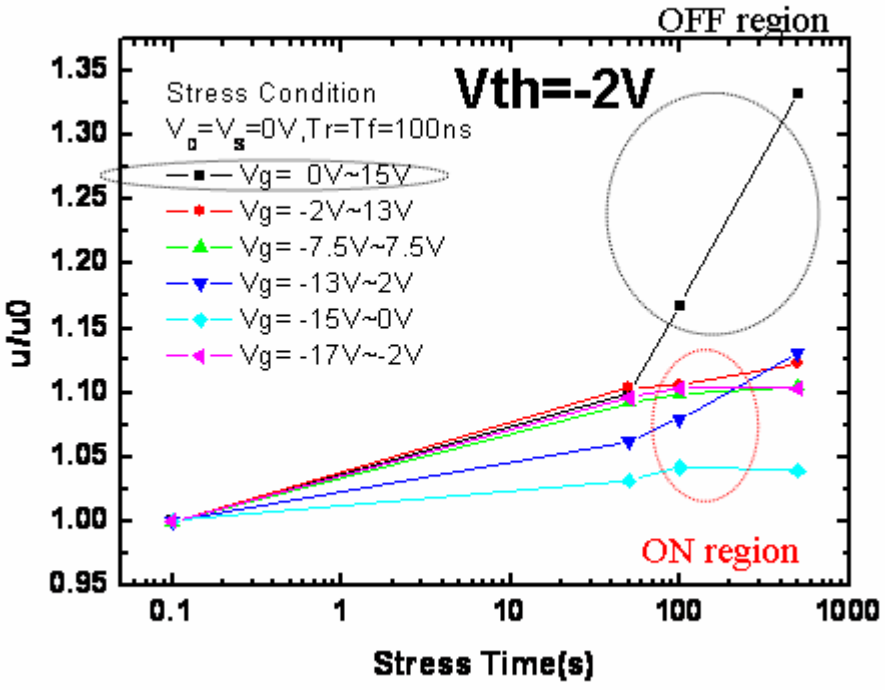


Fig. 3-4(b) Dependence of degradation on swing region for P-channel TFT

3.3 Rising Time and Falling Time for Vg of ON and OFF Region

For N-channel TFT, the transient time dependence for the degradation was examined as shown in Fig. 3-5. During the variation of rising time Tr from 100ns to 700ns with a fixed Tf of 100ns, no significant change in μ/μ_0 was observed as shown in Fig. 3-5(a). On the contrary, the degradation depended strongly on the falling time Tf as shown in Fig. 3-5(b). The degradation is remarkably accelerated with the decrease of the falling time from 700ns for 100ns for a fixed Tr of 100ns. In the case of changing rising time, the gate voltage varies from OFF region to ON region, and the mobile carriers are sited at so low electrical field that no device degradation is formed. But in the case of changing falling time, the gate voltage varies from ON region to OFF region, some carries remain in the channel and are subjected to the high electrical field becoming hot carries.

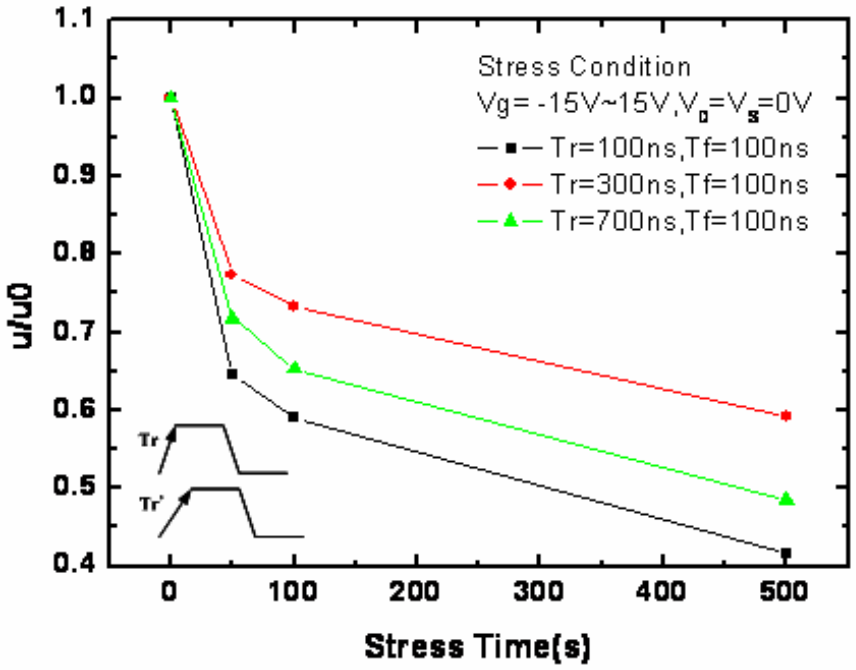


Fig. 3-5(a) Degradation of μ/μ_0 in N-channel TFT under AC stress with Vg = -15V to 15V measured for various rising times Tr and for Tf = 100ns.

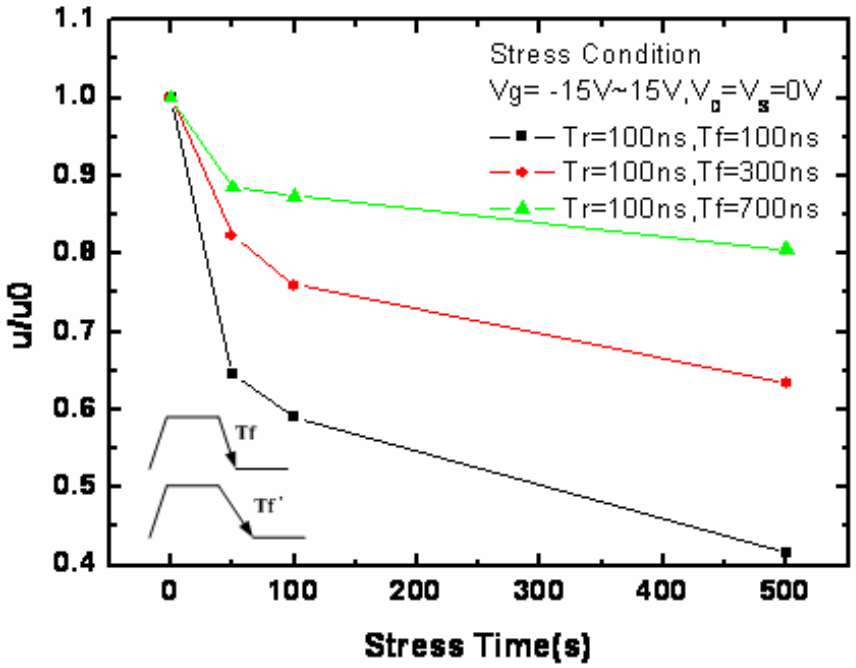


Fig. 3-5(b) Degradation of μ/μ_0 in N-channel TFT under AC stress with Vg = -15V to 15V measured for various rising times Tf and for Tr = 100ns.

For P-channel TFT, the transient time dependence for the degradation was also studied. The dependence of the mobility change on rising time and falling time is shown in Fig. 3-6(a) and Fig. 3-6(b), respectively. The change was accelerated for a variation in rising time; however, the change was not affected by the falling time. In the case of changing rising time, the gate voltage varies from ON region to OFF region, and some carriers are sited at so high electrical field that device degradation is formed. But in the case of changing falling time, the gate voltage varies from OFF region to ON region; carriers are sited at low electrical field not becoming hot carries.

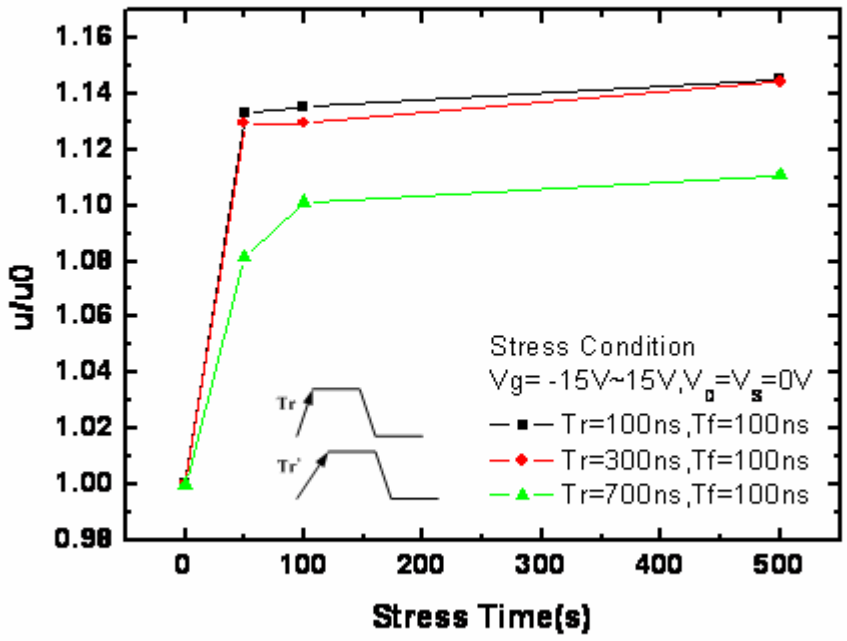


Fig. 3-6(a) Degradation of μ/μ_0 in P-channel TFT under AC stress with Vg = -15V to 15V measured for various rising times Tr and for Tf = 100ns.

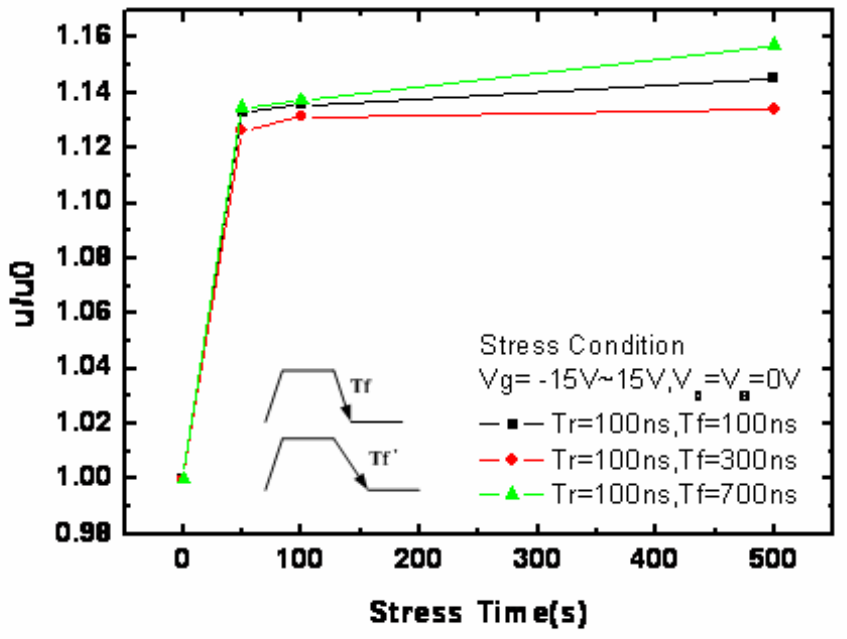


Fig. 3-6(b) Degradation of μ/μ_0 in P-channel TFT under AC stress with Vg = -15V to 15V measured for various rising times Tf and for Tr = 100ns.

3.4 Rising Time and Falling Time for Vg in the OFF Region

We have known that degradation by pulse swing for the ON region was very small, however, that by pulse swing for the OFF region was large. We have already observed the transient time dependence for the degradation under AC stress with Vg = -15V to 15V. For this gate swing of N-channel TFT, it can be taken as steps of Vg = -15V to 0V (OFF region) and Vg =0V to 15V (ON region). Because no device degradation is formed for N-channel TFT under AC stress with Vg = 0V to 15V, we are only interested in the transient time dependence for the degradation of N-channel TFT at Vg = -15 V to 0V. For the gate voltage swings from -15V to 0V, it is firstly observed that the degradation is obviously dependent on both the rising time and falling time, as shown in Fig. 3-7(a) and Fig. 3-7(b). Since there are no induced electrons for these applied gate voltages, it reveals that the previously proposed model may be incomplete.

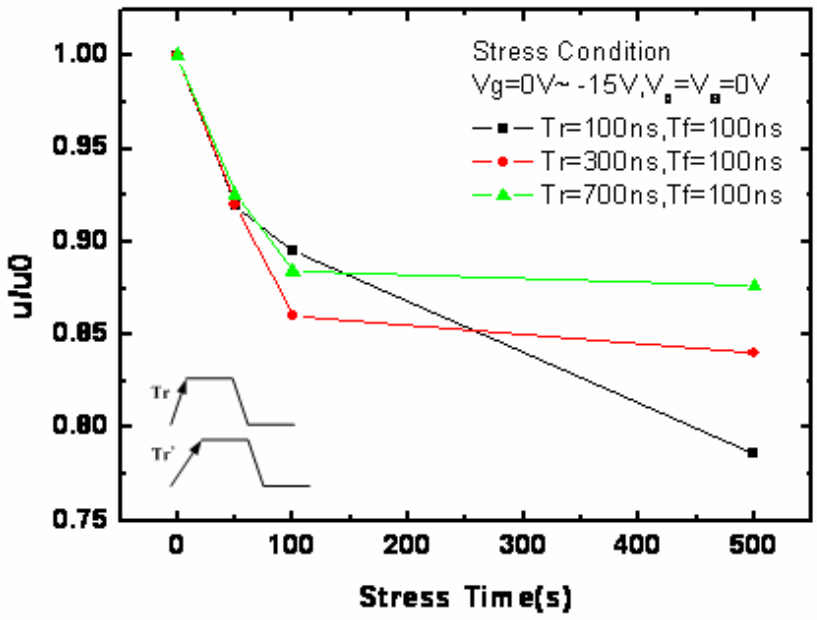


Fig. 3-7(a) Degradation of μ/μ_0 in N-channel TFT under AC stress with Vg = -15V to 0 V measured for various rising times Tr and for Tf = 100ns.

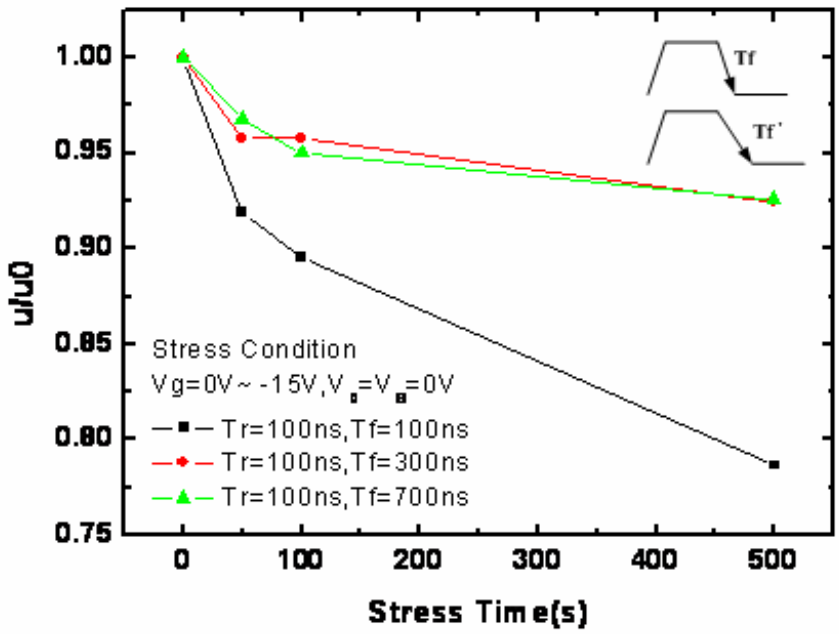


Fig. 3-7(b) Degradation of μ/μ_0 in N-channel TFT under AC stress with Vg = -15V to 0 V measured for various rising times Tf and for Tr = 100ns.

For P-channel TFT, Vg = 0V to 15V is OFF region, and Vg =-15V to 0V is ON region. Because no device degradation is formed for P-channel TFT under AC stress with Vg =-15V to 0V, we are also only interested in the transient time dependence for the degradation of P-channel TFT at Vg = 0V to 15V. For the gate voltage swings from 0V to 15V, it is observed that the degradation is independent on the rising time and falling time, which is different from P-channel TFT under AC stress with Vg =-15V to 15V, as shown in Fig. 3-8(a) and Fig. 3-8(b).

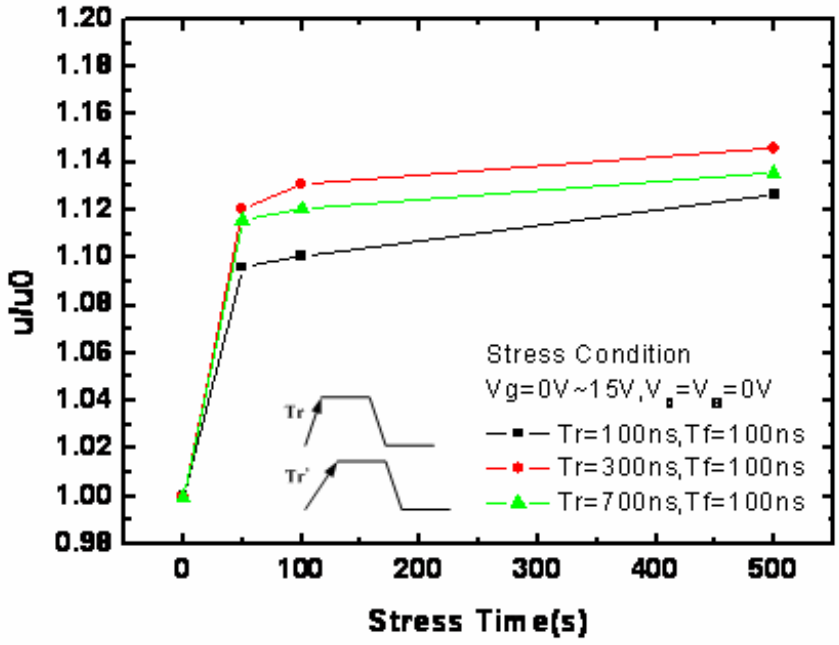


Fig. 3-8(a) Degradation of μ/μ_0 in P-channel TFT under AC stress with Vg = 0V to 15V measured for various rising times Tr and for Tf = 100ns.

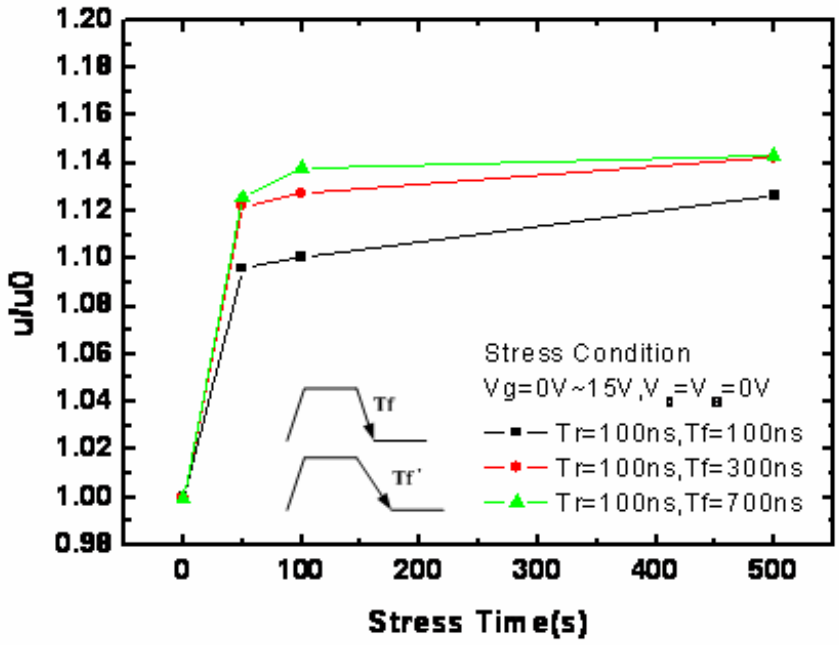


Fig. 3-8(b) Degradation of μ/μ_0 in P-channel TFT under AC stress with Vg = 0V to 15V measured for various rising times Tf and for Tr = 100ns.

Chapter 4

Degradation for N-type Poly-Si TFT under Gate Pulse Stress with Drain Bias

4.1 Frequency Dependence

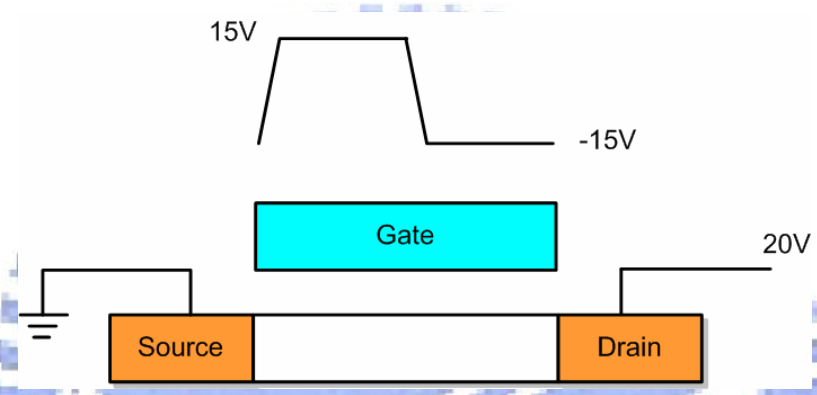


Fig. 4-1 TFT model in N-channel under Vg=-15V~15V and V_D=20V with different frequency

Fig.4-1 is the N-type poly-Si TFT model under different gate signal frequency. The dependences of the device degradation on frequency for the drain bias 20V with forward and reverse measurement are shown in Fig. 4-2(a) and Fig. 4-2(b), respectivity. When the frequency increases from 0.5KHz to 500KHz, the mobility largely decreases. And it is re-plotted with the number of gate pulses, as shown in Fig. 4-3(a) and Fig. 4-3(b). It is expected all lines exhibit the universal relationship in the equivalent repetition number as in the case of V_D=0V. However, the data are different from what we expect. The degradation of mobility u/u0 is not continuous for the case of V_D=20V. The degradation in the period with unchanged Vg can no longer be ignored. When the gate voltage is at 15V and the drain is biased at 20V, the TFT will suffer from the DC stress with large drain current, which makes the phenomena more complicated. The degradation of TFTs under

such an ON region AC gate stress will be further studied and not discussed in detail in this thesis.

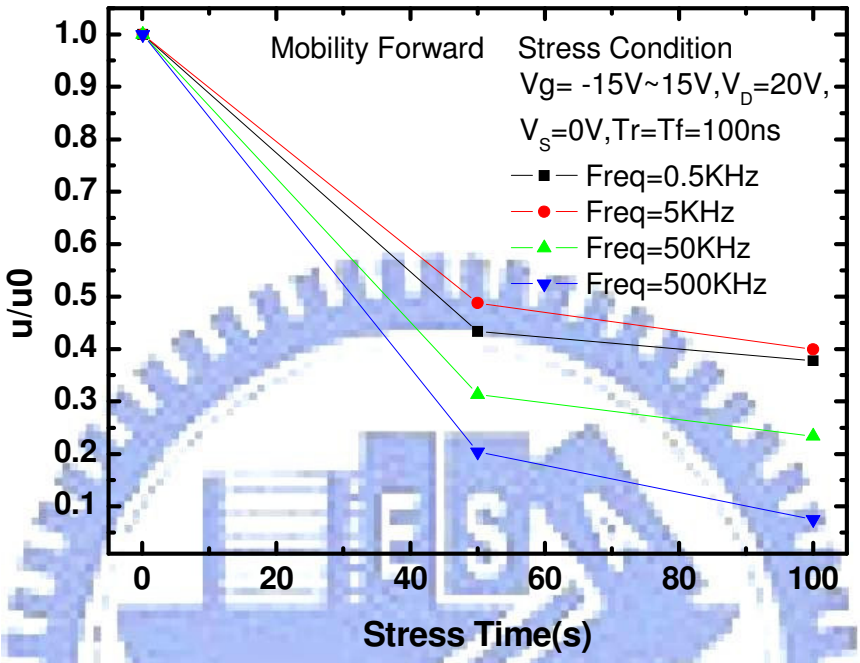


Fig. 4-2(a) The frequency dependence of degradation of N-channel TFT under Vg = -15V to 15V and V_D=20V with the forward measurement

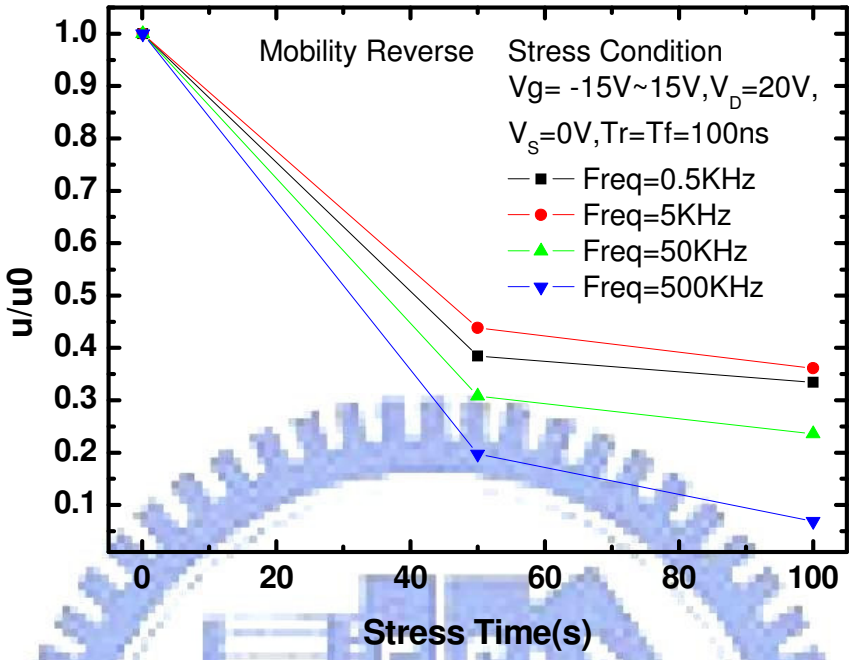


Fig. 4-2(b) **The frequency dependence of degradation of N-channel TFT under Vg = -15V to 15V and V_D=20V with the reverse measurement**

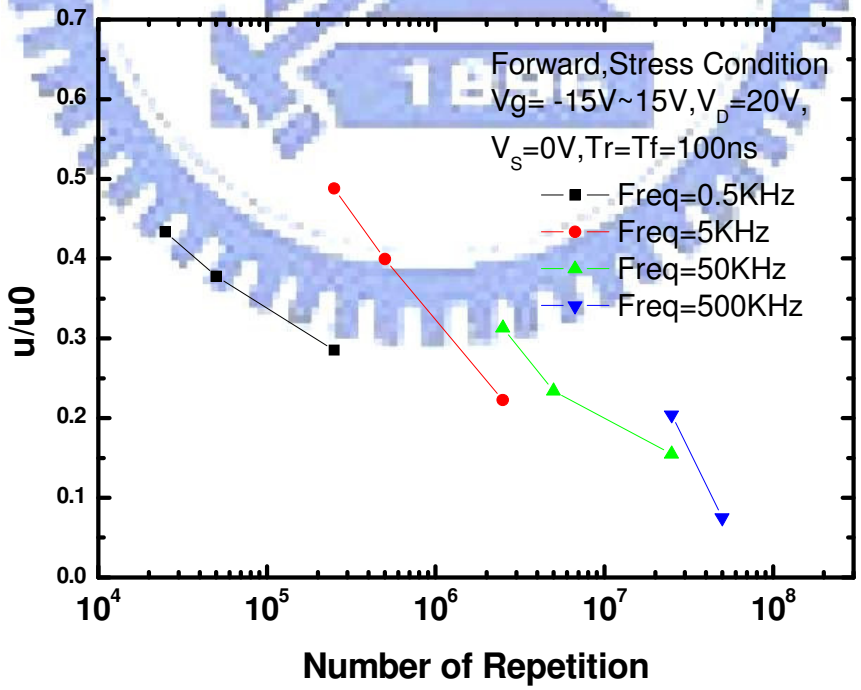


Fig. 4-3(a) **Forward dependence on the number of pulse repetitions of N-channel TFT under Vg = -15V to 15V and V_D=20V**

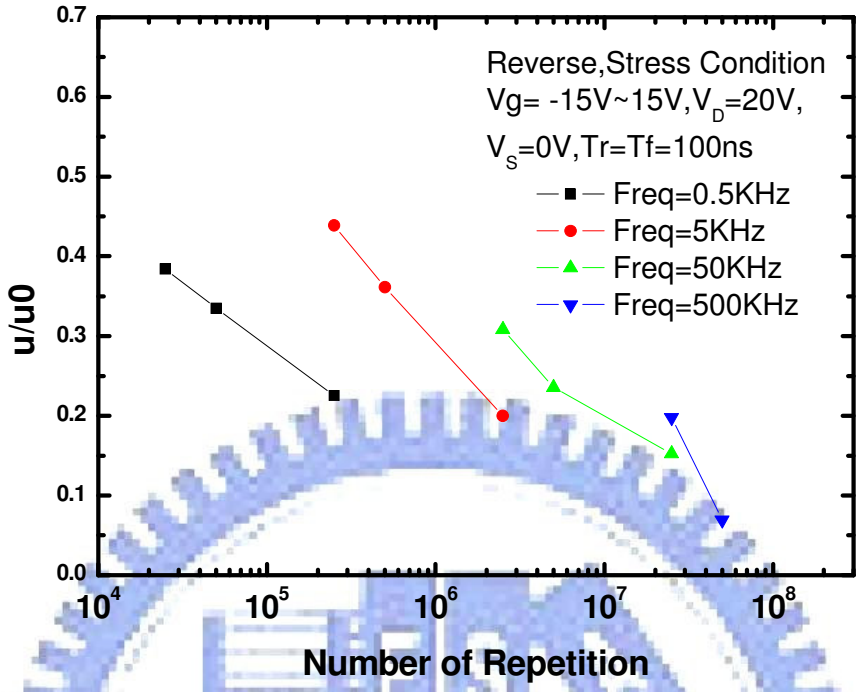


Fig. 4-3(b) Reverse dependence on the number of pulse repetitions of N-channel TFT under Vg = -15V to 15V and V_D=20V

4.2 Effect of Drain Bias

4.2.1 Vg in ON and OFF region

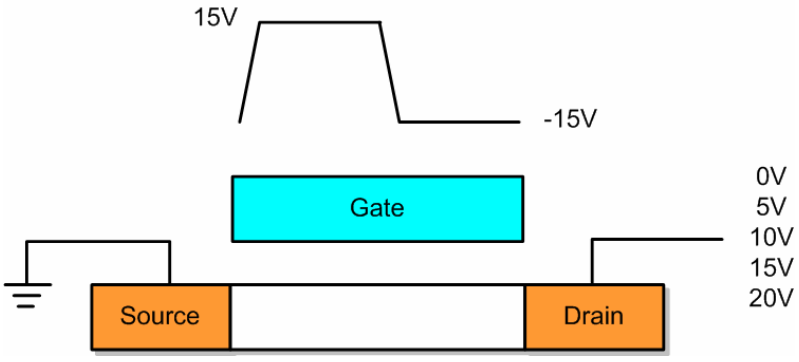


Fig. 4-4 TFT model in N-channel under various drain bias in on/off region

Fig. 4-4 shows the structure of N-type poly-Si TFT under various drain bias stressed in on/off region. The gate signal frequency is equal to 500KHz. Fig. 4-5(a) shows the I_d-Vg transfer curves of the TFT before and after 60s of dynamic gate stresses with different drain voltage $V_{DS.}$ The higher threshold voltage, lower mobility and higher sub-threshold swing are observed after stress. The phenomenon of degradation under various V_{DS} is similar to effects of hot carrier, which can create interface-trapped charge or some defects near the drain region. The initial mobility is 70 cm^2/V-sec. It decreases to only 10 cm^2/V-sec after AC stress with drain bias of 20 V. The initial sub-threshold swing is 0.24 V/dec. After the AC stress it degrades to 0.33 V/dec. The degradation seriously depends on the supplied drain bias, as shown in Fig. 4-5(b) and Fig. 4-5(c). The degree of mobility and sub-threshold swing degradation are almost the same in the forward and reverse measurement.

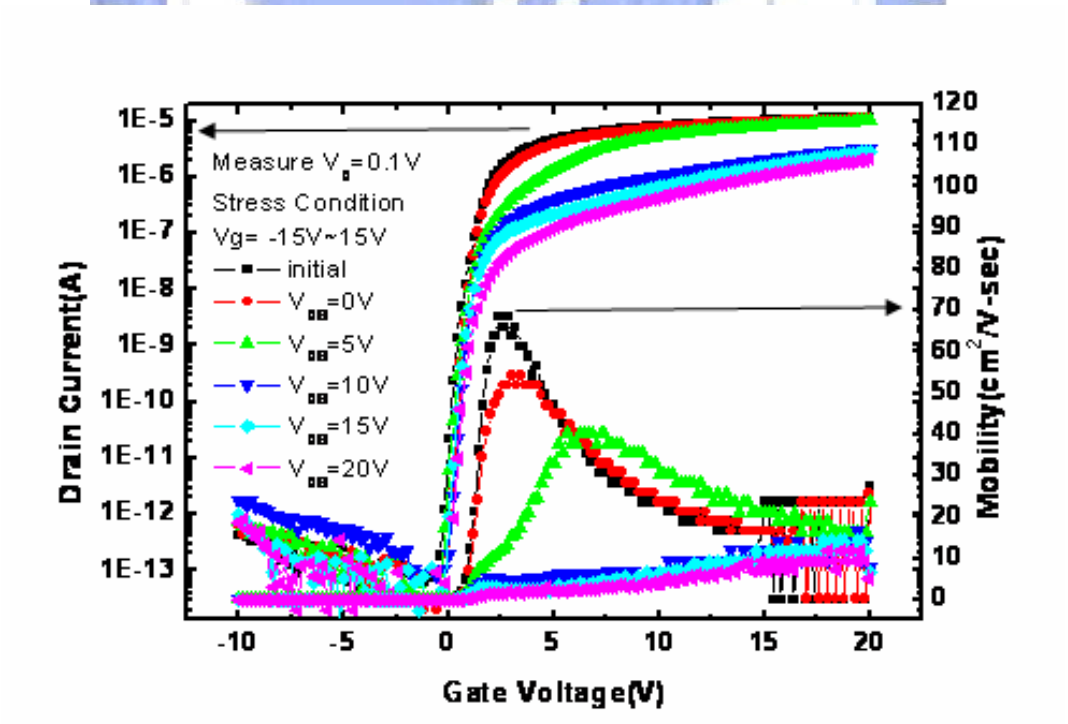


Fig. 4-5(a) Id-Vg forward curves before and after dynamic gate stress with various drain bias in on/off region

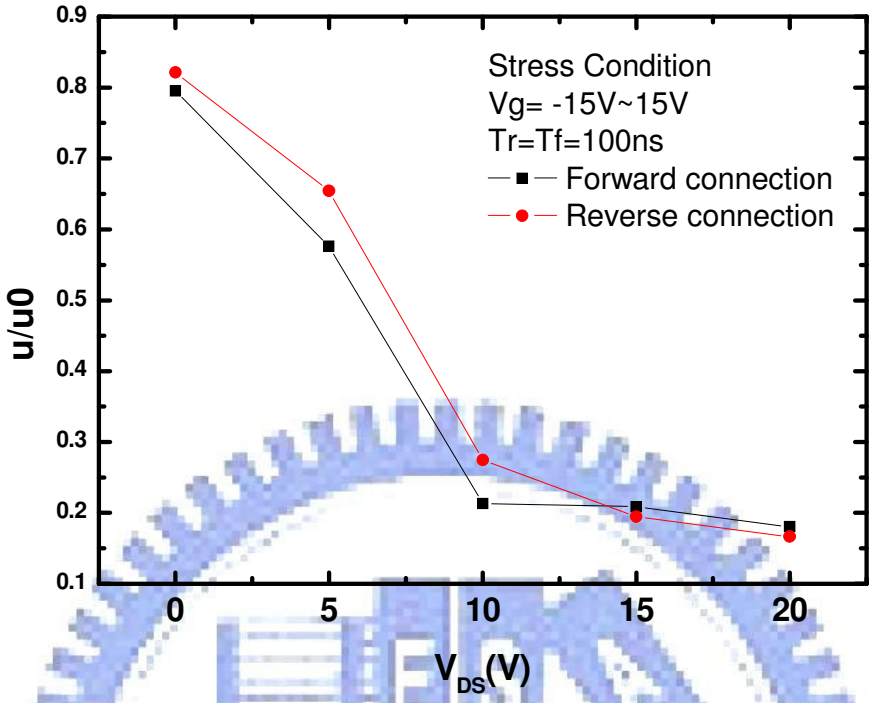


Fig. 4-5(b) Dependence of the mobility on V_{DS} with gate AC stress in on/off region

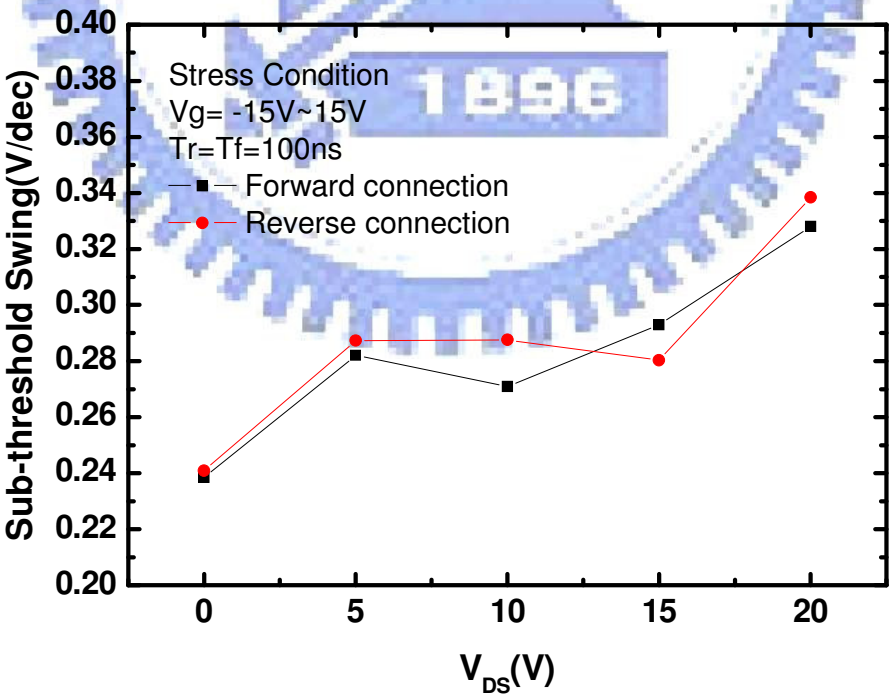


Fig. 4-5(c) Dependence of the Sub-threshold Swing on V_{DS} with gate AC stress in on/off region

Since the Id-Vg transfer characteristics could not distinguish the dominant degradation region, C-V curves were therefore employed. Fig. 4-6(a) shows the normalized gate-to-source capacitance (C_{GS}) curves before and after stress with different drain voltage. Fig. 4-6(b) shows the normalized gate-to-drain capacitance (C_{GD}) curves under the same stress conditions. The C_{GS} is measured with a floating drain and C_{GD} is measured with a floating source.

Referred to the two figures, for the gate dynamic stress with stress drain bias smaller than 10V, the C_{GS} curves after stress show almost no change. However, the C_{GD} curves significantly stretch out even for V_D smaller than 10V and shift in the positive direction with the stressed drain voltage. It is clearly illustrated that the degradation region is near the drain.

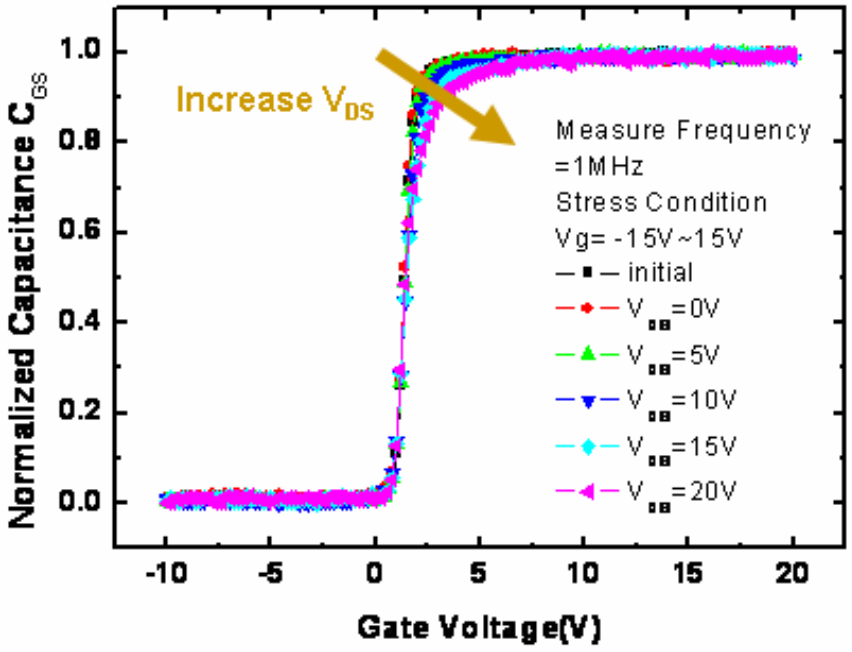


Fig. 4-6(a) Degradation of normalized C_{GS} curve in N-channel under various V_{DS} in on/off region at frequency=1MHz

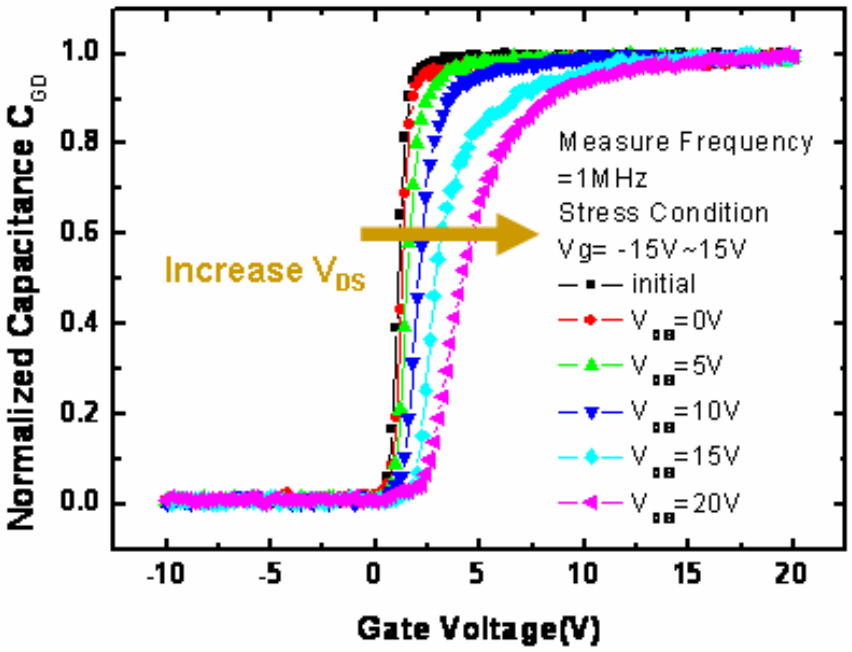


Fig. 4-6(b) Degradation of normalized C_{GD} curve in N-channel under various V_{DS} in on/off region at frequency=1MHz

4.2.2 Vg in the OFF region

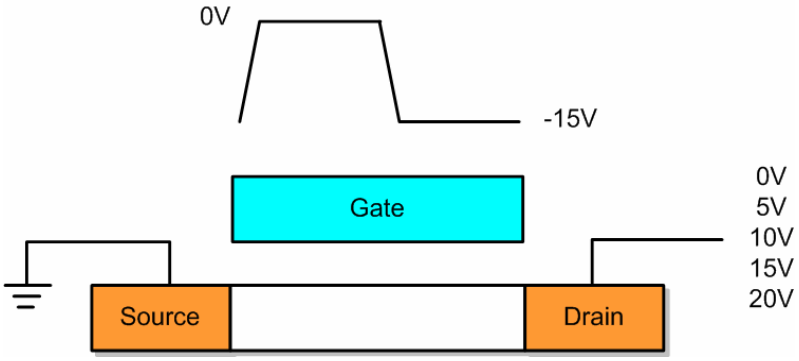


Fig. 4-7 TFT model in N-channel under various drain bias in off region

Fig. 4-7 shows the arrangement N-type poly-Si TFT under various drain bias stressed in the off region. The gate signal frequency is also equal to 500KHz. Fig. 4-8(a) shows the I_d-Vg transfer curves of the TFT before and after 60s of dynamic gate stresses with

different drain voltage $V_{DS.}$ The higher threshold voltage, lower mobility and higher sub-threshold swing are observed after stress just as the case discussed in section 4.2.1. The phenomenon of degradation under various V_{DS} is similar to effects of hot carrier, too. The initial mobility is 65 cm^2/V-sec. It decreases to only 5 cm^2/V-sec after AC stress with drain bias of 20 V. The initial sub-threshold swing is 0.26 V/dec. After the AC stress it degrades to 0.57 V/dec. They seriously depend on the supplied drain bias, as shown in Fig. 4-8(b) and Fig. 4-8(c). The degree of mobility degradation is the same in forward and reverse measurement, but the sub-threshold swing of reverse of V_D=20V degrades more than that in the forward measurement.

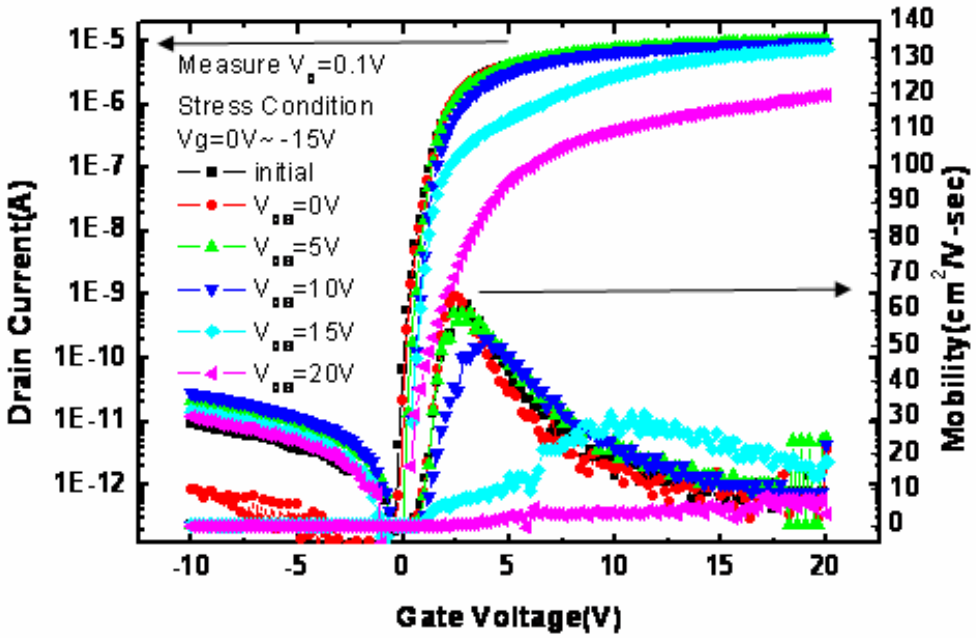


Fig. 4-8(a) Id-Vg forward curves before and after dynamic gate stress with various drain bias in off region

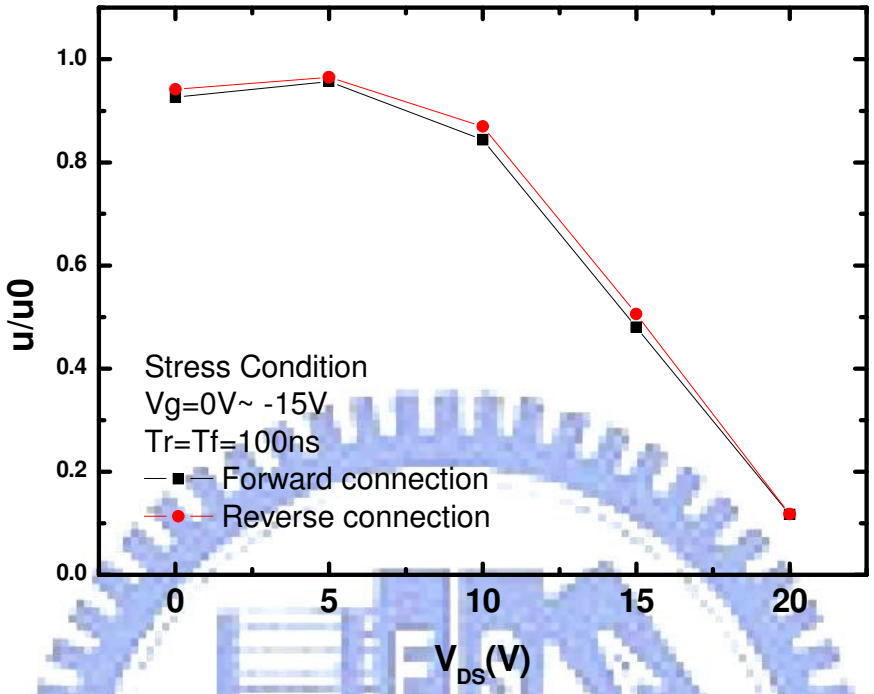


Fig. 4-8(b) Dependence of the mobility on V_{DS} with gate AC stress in off region

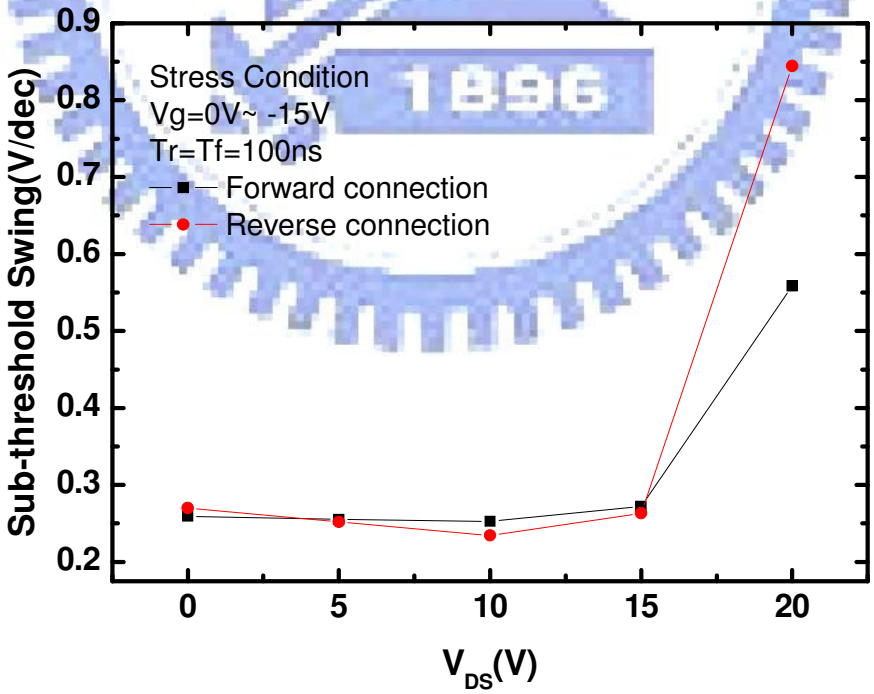


Fig. 4-8(c) Dependence of the Sub-threshold Swing on V_{DS} with gate AC stress in off region

Fig. 4-9(a) shows the C_{GS} curves before and after stress. Fig.4-9(b) shows the C_{GD} curves. For the gate dynamic stress with stress drain bias smaller than 15V, the C_{GS} curves show almost no change. The C_{GS} curves occur the phenomenon like hot carrier under DC stress condition. The C_{GD} curves show also almost no change under drain bias smaller than 10V. The C_{GD} curves significantly stretch out and shift in the positive direction for the stress voltage V_{DS}=15V and V_{DS}=20V, especially for V_{DS}=20V. It exhibits apparent degradation in the gate voltage larger than V_{FB} for the stress voltage V_{DS}=20V. The degradation of the device stressed in the off region with large drain bias is much worse than that in the on/off region as discussed in section 4.2.1. This is much different from our used expectation that the device degradation is slight as toggling in the off region, as compared with that in the on/off region. This reveals that the device degradation should deserve more study to clarify the mechanism.

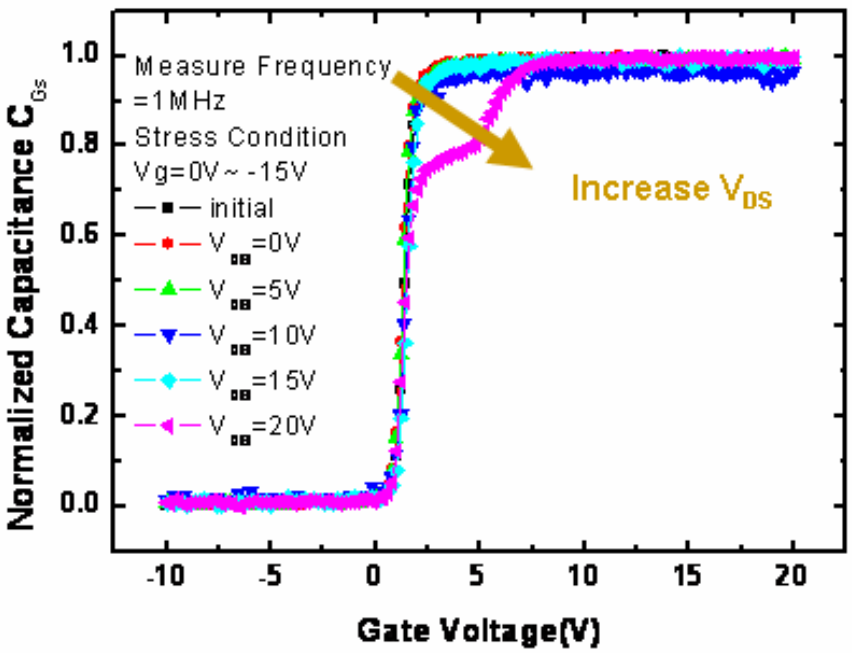


Fig. 4-9(a) Degradation of normalized C_{GS} curve in N-channel under various V_{DS} in off region at frequency=1MHz

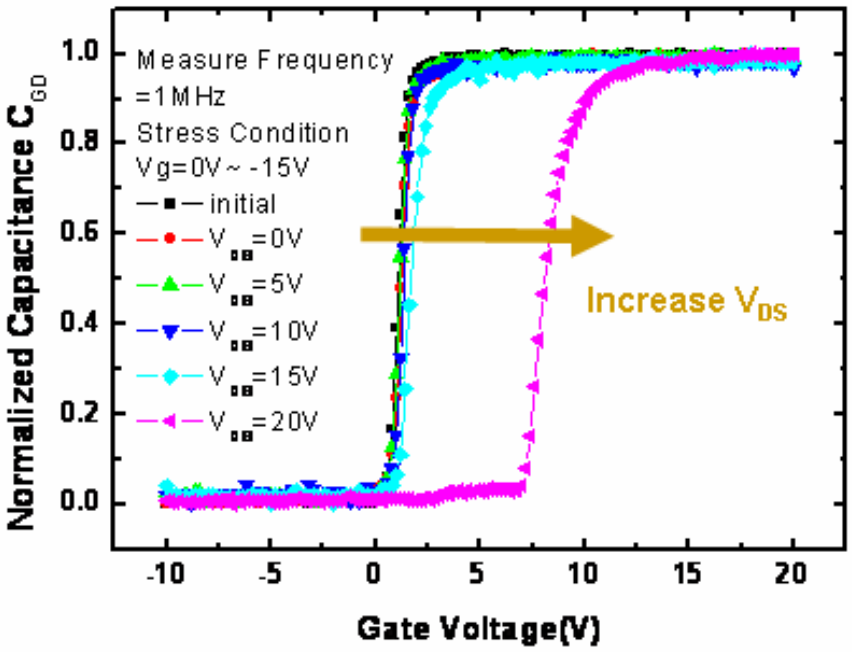


Fig. 4-9(b) Degradation of normalized C_{GD} curve in N-channel under various V_{DS} in off region at frequency=1MHz

Fig. 4-10(a) and Fig. 4-11(a) respectively show the forward and reverse Id-Vg transfer curves under various drain bias 60s stress with drain voltage of 10V measurements. It is defined the measurement of V_D=0.1V is linear region, and the measurement of V_D=10V is saturation region ($V_{DS} > V_{GS}-V_T$). Forward saturation currents with different drain bias stress are almost the same. Reverse saturation currents degrade more with increasing drain bias stress. Therefore, the forward ON-current saturation region is much better than the measured with source and drain reverse.

The pinch-off region appears near the drain for the forward measurement. The depletion region expands to the source with drain voltage increasing. Carriers are swept into the drain by the electrical field. As referred to Fig. 4-10(b), carriers move into pinch-off region. And, they move away the surface into the bulk. Fig. 4-11(b) shows the reverse measurement, carriers must flow through the damaged region which is near the

drain. It is observed that the forward saturation current is much better than the reverse.

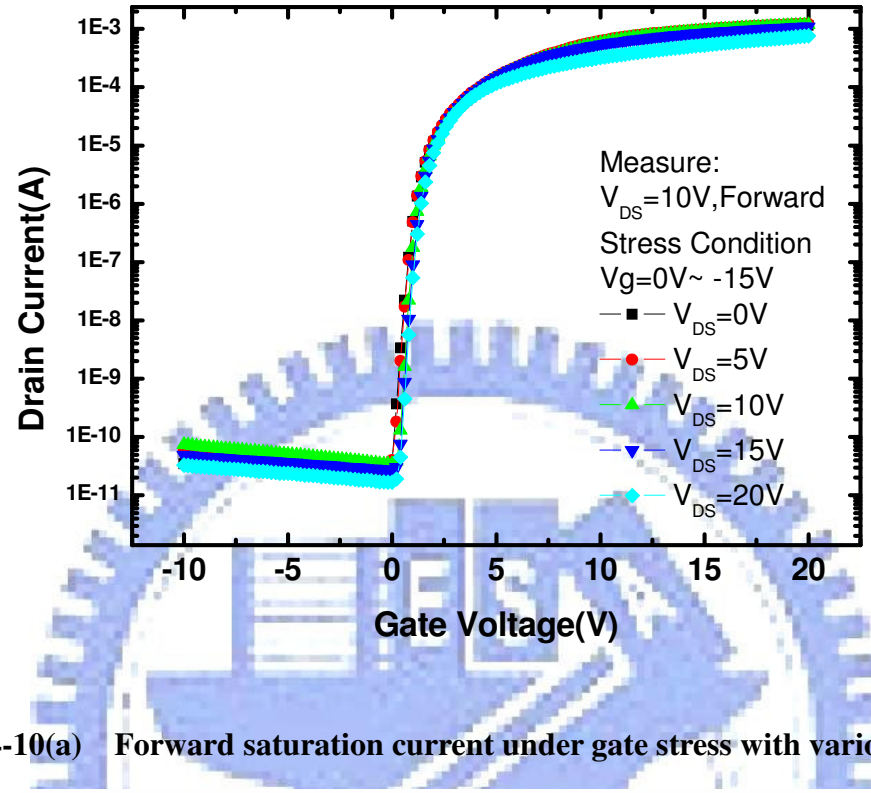


Fig. 4-10(a) Forward saturation current under gate stress with various drain

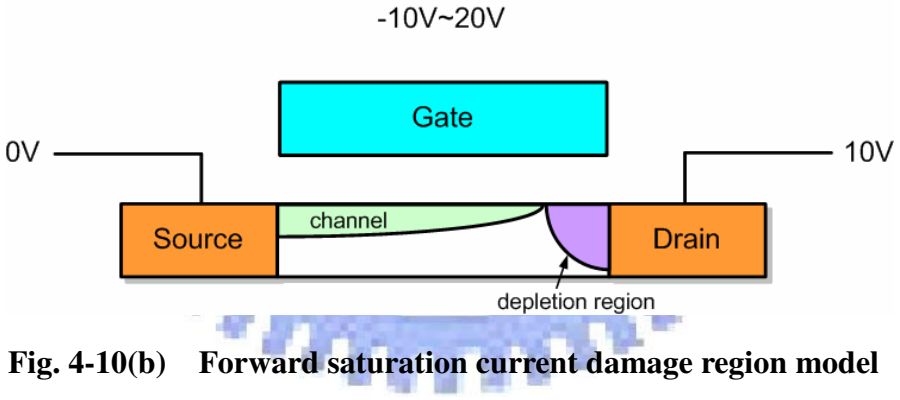


Fig. 4-10(b) Forward saturation current damage region model

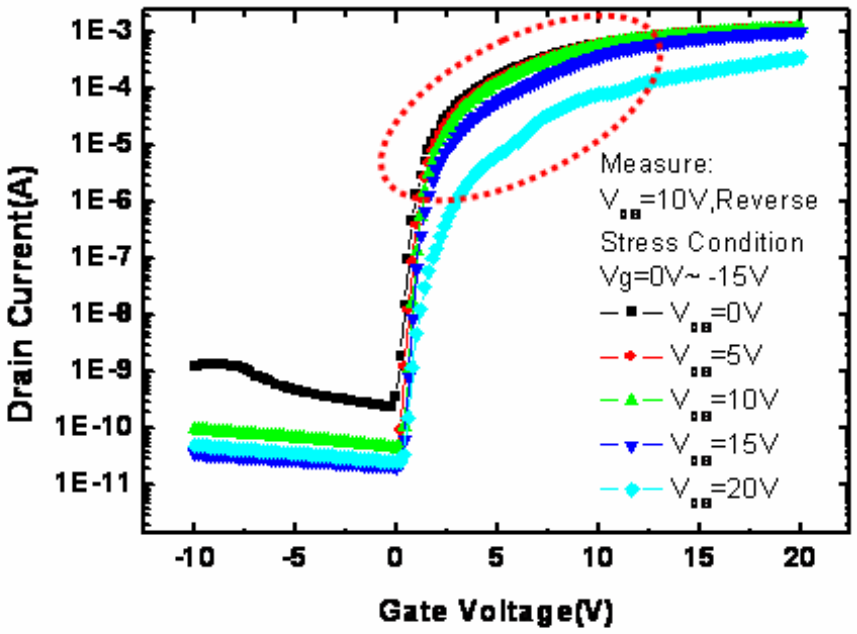


Fig. 4-11(a) Reverse saturation current under gate stress with various drain

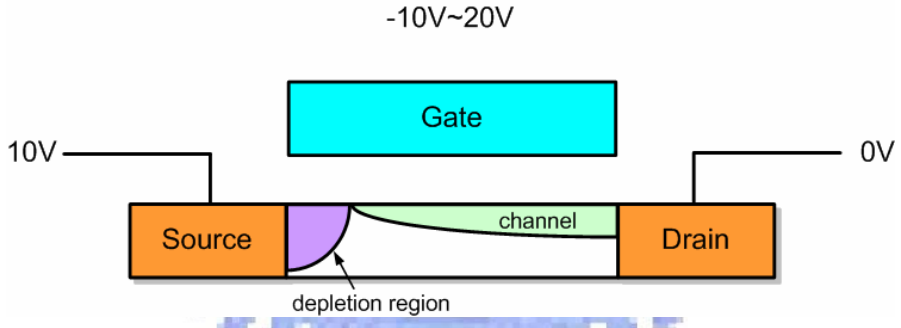


Fig. 4-11(b) Reverse saturation current damage region model

4.3 Effect of Gate Voltage Range

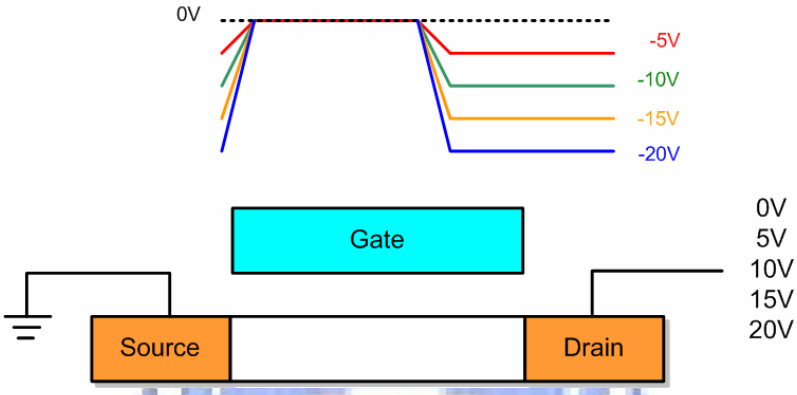


Fig. 4-12 TFT model in N-channel under various V_{DS} and range of gate voltage

Fig. 4-12 shows the degraded mobility after 60s dynamic gate stress with different drain voltage V_D for different gate voltage ranges. The frequency is equal to 500KHz. It is given the pulse signals Vgl ranging from -5V to -20V and Vgh fixed at 0V for the gate signal. Moreover, the various bias voltages are applied to the drain.

The larger gate voltage range and drain bias, the more degradation of the mobility is observed as shown in Fig. 4-13(a). Fig. 4-13(b) shows the degraded sub-threshold swing after stressing. It is observed when V_{DS} is smaller than 15V and Vg range is smaller than 10V, the sub-threshold swing exhibits almost no degradation. When V_{DS} is higher than 15V and Vg ranges beyond 10V, the sub-threshold swing is seriously degraded.

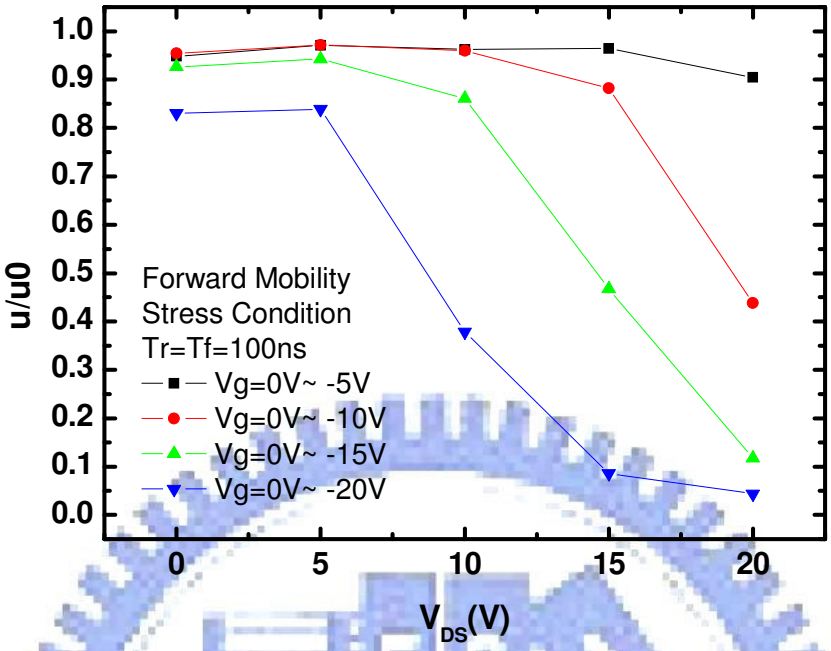


Fig. 4-13(a) Degradation of u/u0 in N-channel under various V_{DS} and range of gate voltage

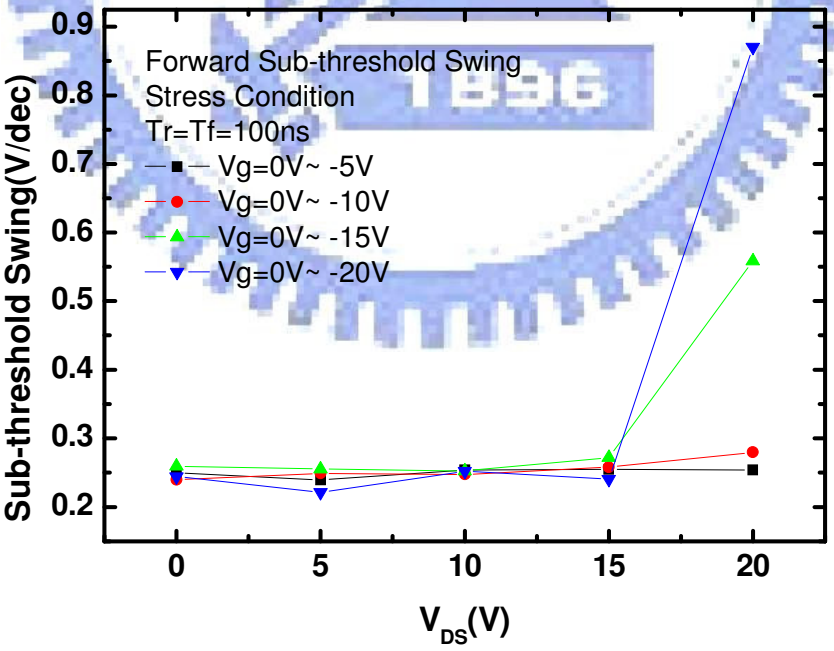


Fig. 4-13(b) Degradation of the sub-threshold swing in N-channel under various V_{DS} and range of gate voltage

Fig. 4-14(a) and Fig. 4-14(b) shows the C_{GS} and C_{GD} curves of the devices stressed by Vg=-5V~0V and various drain bias voltages, where Fig. 4-15~Fig. 4-17 respectively show those figures for the stressed gate signal Vg=-10V~0V, Vg=-15V~0V, and Vg=-20V~0V. It is observed the C-V curve shows serious distortion when V_{DS} is higher than 15V and Vg range is higher than 15V. Both the Vg range effect and drain bias dependence are responsible for the degradation.

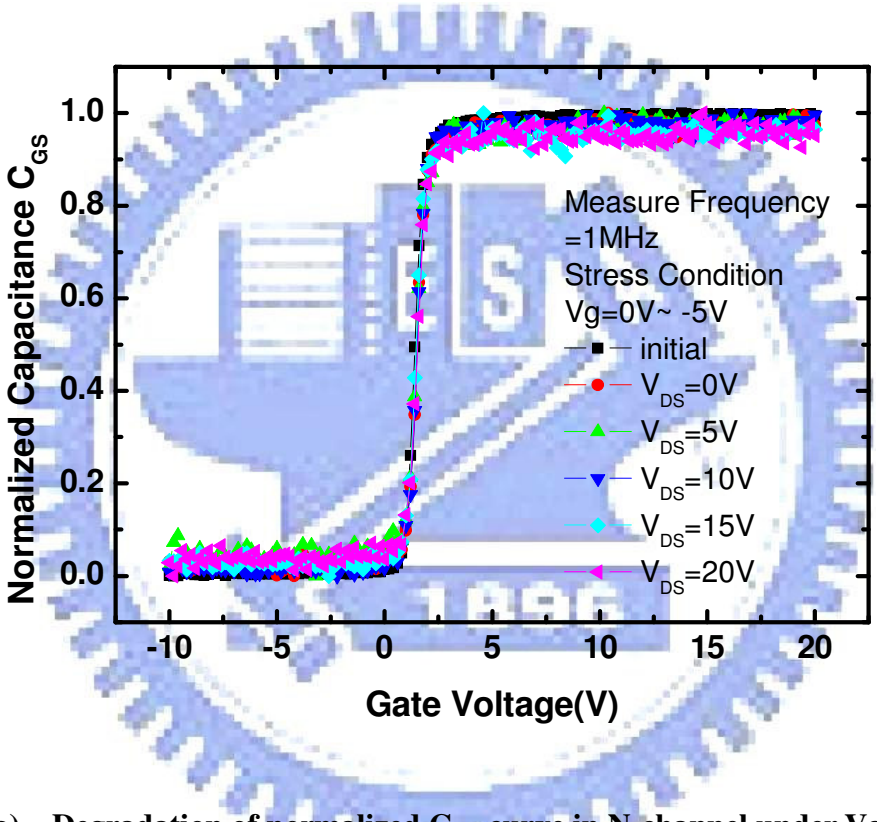


Fig. 4-14(a) Degradation of normalized C_{GS} curve in N-channel under Vg=-5V~0V with various V_{DS} at frequency=1MHz

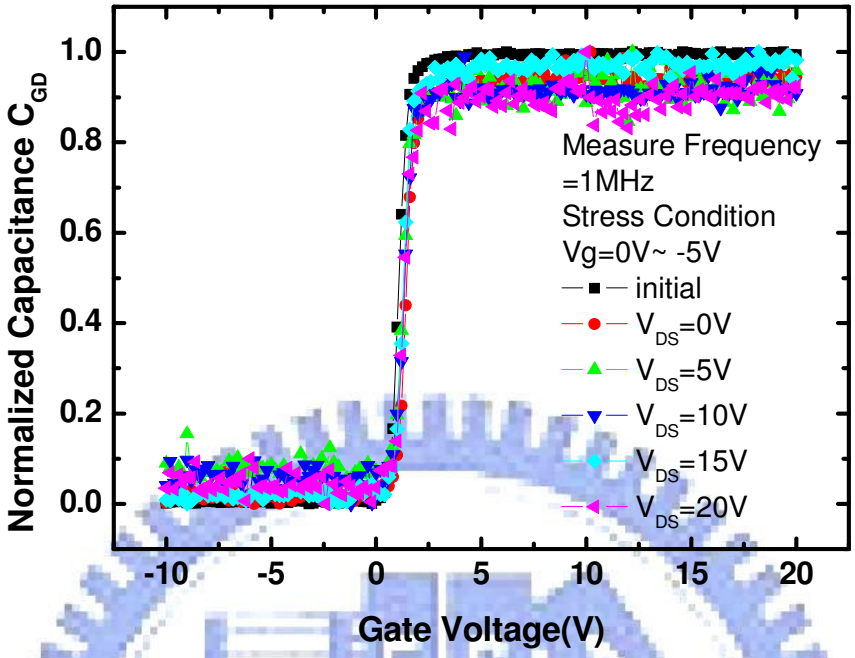


Fig. 4-14(b) Degradation of normalized C_{GD} curve in N-channel under Vg=-5V~0V with various V_{DS} at frequency=1MHz

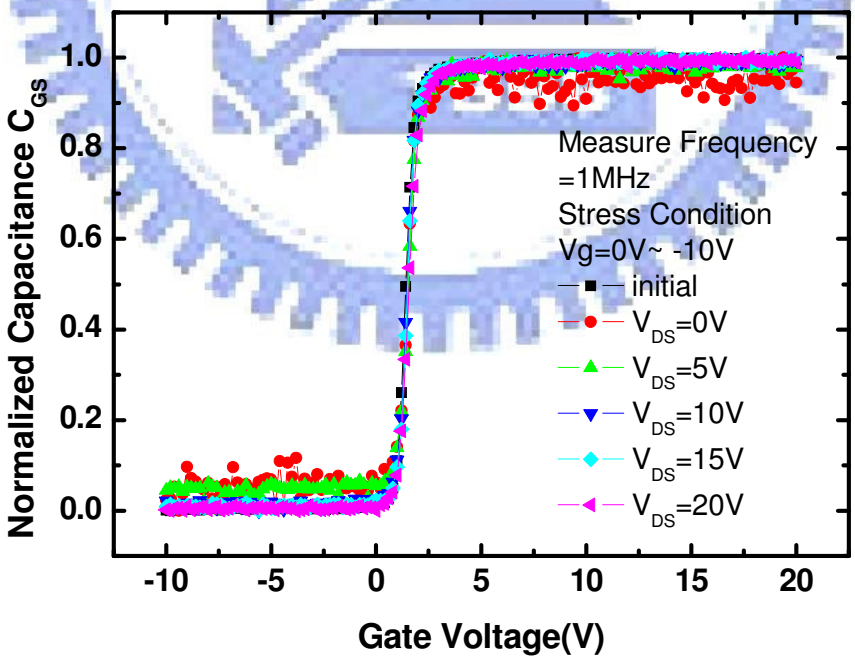


Fig. 4-15(a) Degradation of normalized C_{GS} curve in N-channel under Vg=-10V~0V with various V_{DS} at frequency=1MHz

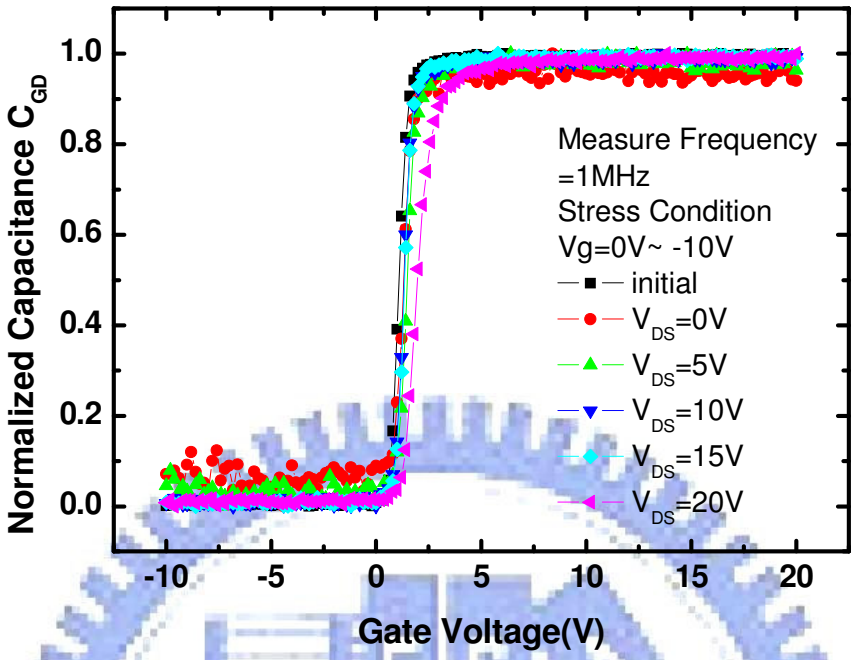


Fig. 4-15(b) Degradation of normalized C_{GD} curve in N-channel under Vg=-10V~0V with various V_{DS} at frequency=1MHz

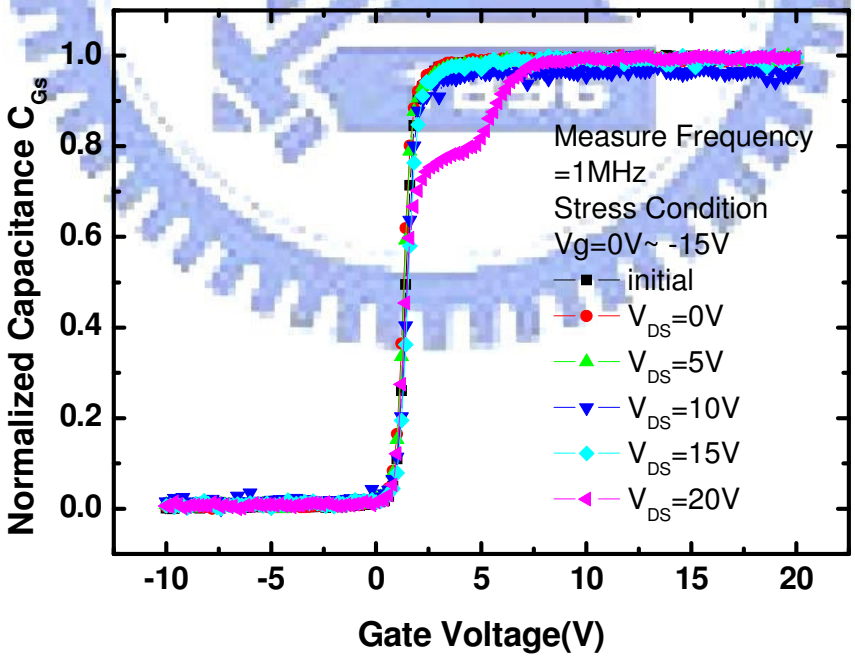


Fig. 4-16(a) Degradation of normalized C_{GS} curve in N-channel under Vg=-15V~0V with various V_{DS} at frequency=1MHz

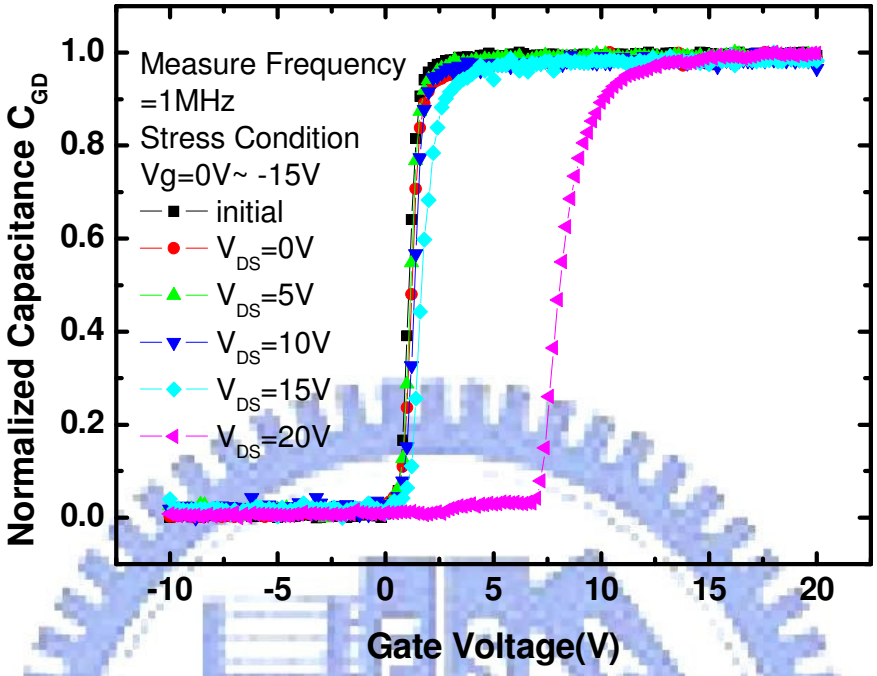


Fig. 4-16(b) Degradation of normalized C_{GD} curve in N-channel under Vg=-15V~0V with various V_{DS} at frequency=1MHz

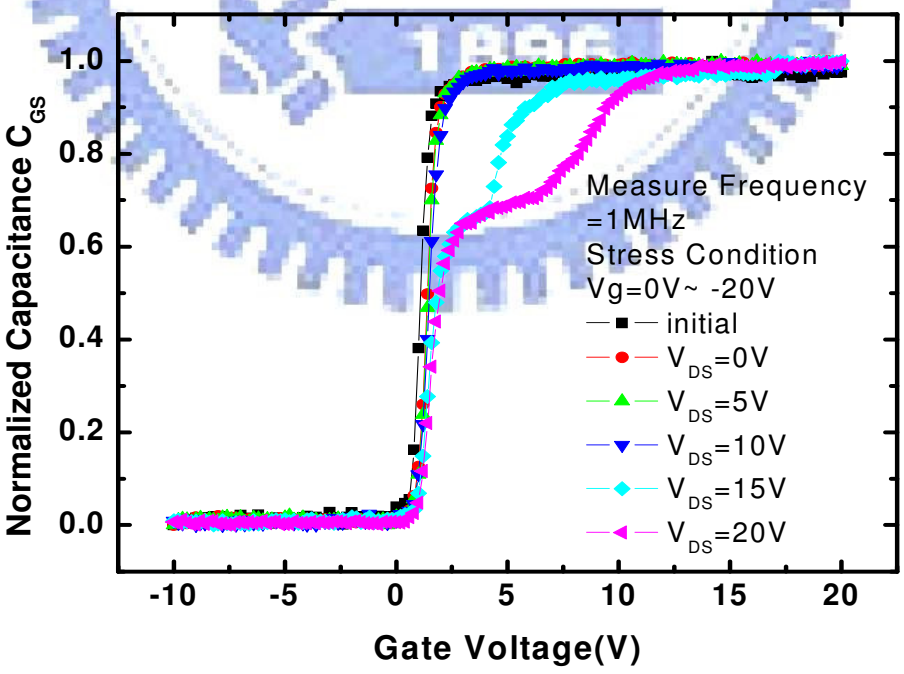


Fig. 4-17(a) Degradation of normalized C_{GS} curve in N-channel under Vg=-20V~0V with various V_{DS} at frequency=1MHz

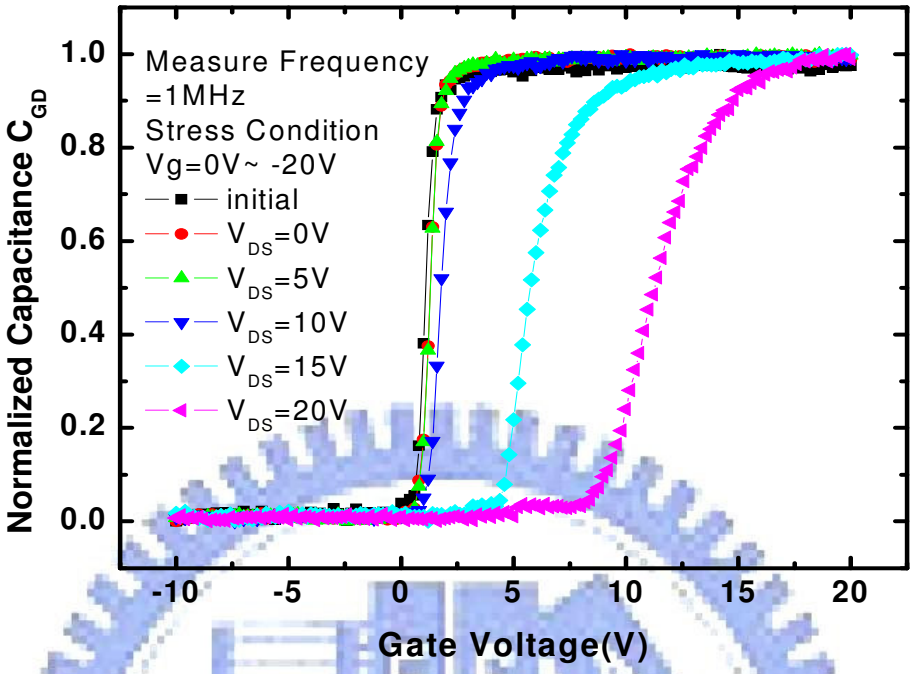


Fig. 4-17(b) Degradation of normalized C_{GD} curve in N-channel under Vg=-20V~0V with various V_{DS} at frequency=1MHz

4.4 Other Effects

4.4.1 Effect of Rising Time

4.4.1.1 Vg in ON and OFF Region

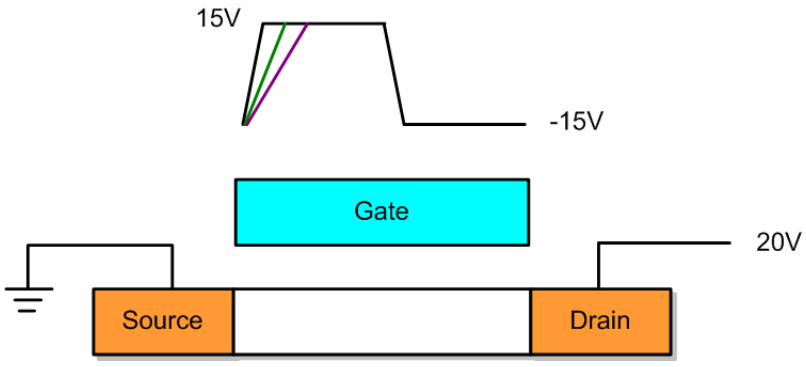


Fig. 4-18 TFT model in N-channel under Vg=-15V~15V with changed rising time Tr and fixed Tf

One of the stress configurations of the devices is examined in Fig. 4-18; the device is biased under Vg of ON/OFF region and drain voltage of 20V. The frequency of the stress voltage is 500 KHz and stress time is set to 60 seconds. There are various stress conditions with the variation of rising time Tr from 100ns to 700ns and a fixed falling time Tf of 700ns for the gate signal. After the different stress conditions applied on the device individually, the u/u0 is extracted and shown in Fig. 4-19(a). As the rising time getting longer, the mobility degrades worse. The sub-threshold swings also become worse as shown in Fig.4-19(b). This means that the degradation strongly depends on the rising time Tr. These results suggest that the degradation occur when the gate voltage is transited from low to high. In other words, the rising time of the gate voltage would dominate the degradation.

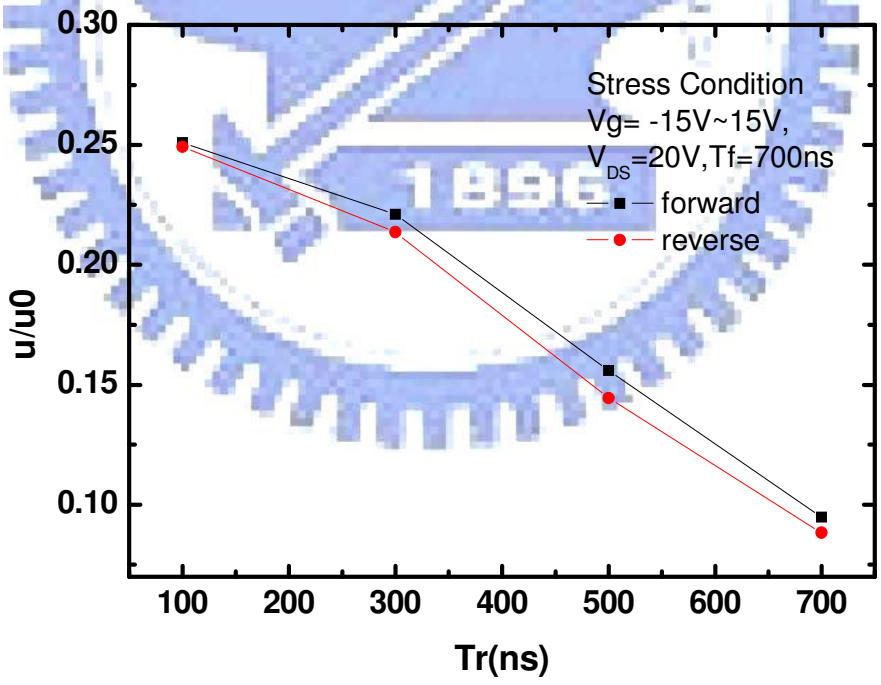


Fig. 4-19(a) Degradation of μ/μ_0 in N-channel TFT under AC stress with Vg = -15V to 15V measured for various rising times Tr and for Tf = 700ns

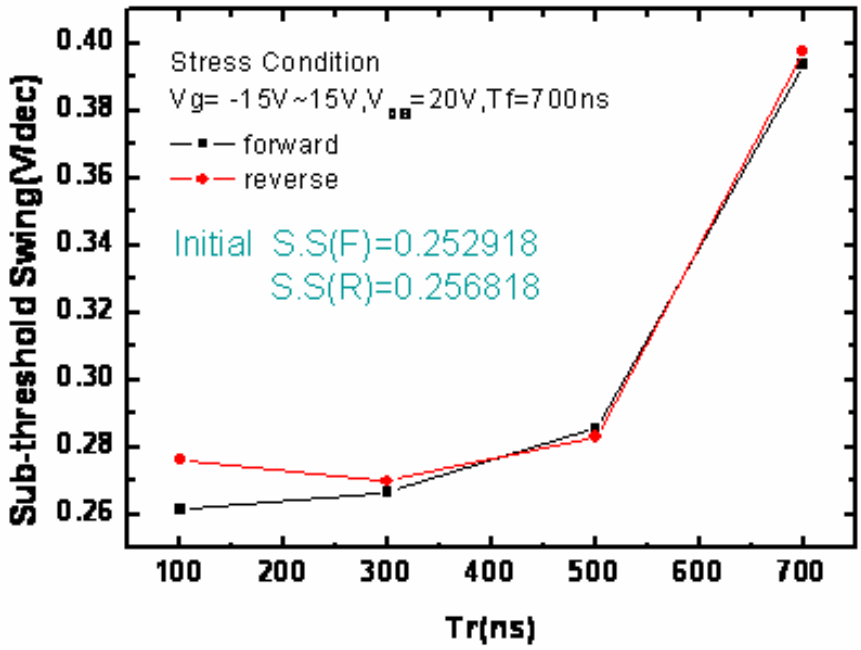


Fig. 4-19(b) Degradation of S.S in N-channel TFT under AC stress with Vg = -15V to 15V measured for various rising times Tr and for Tf = 700ns

Fig. 4-20 and Fig. 4-20(b) shows the C_{GS} and C_{GD} curves of the devices stressed with various rising time of the gate signal. It is observed that the C_{GS} curve seriously degrades under Tr of 700ns and Tf of 700ns. The other three C_{GS} curves under Tr from 100ns to 500ns with fixed Tf have almost no change. With increasing rising time Tr and a fixed falling time Tf, the C_{GD} curve stretches more.

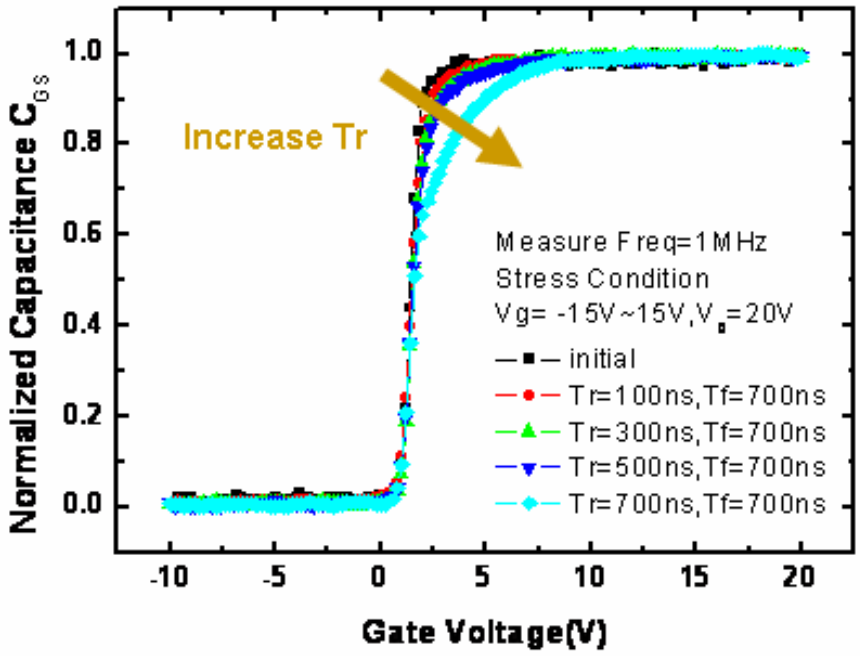


Fig. 4-20(a) Degradation of normalized C_{GS} curve in N-channel under Vg=-15V~15V measured for various Tr and for Tf = 700ns at freq=1MHz

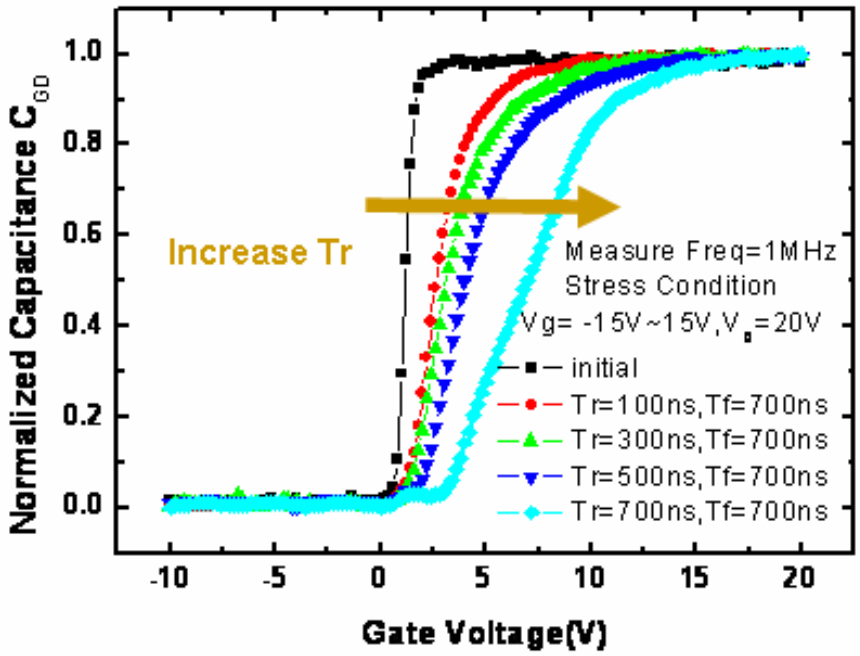


Fig. 4-20(b) Degradation of normalized C_{GD} curve in N-channel under Vg=-15V~15V measured for various Tr and for Tf = 700ns at freq=1MHz

4.4.1.2 Vg in the OFF Region

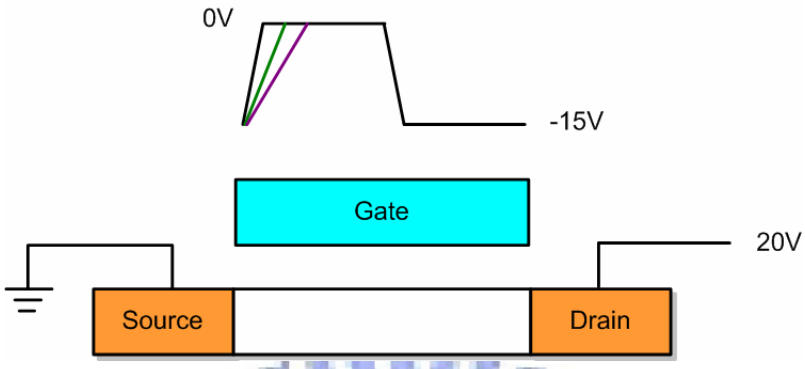


Fig. 4-21 TFT model in N-channel under Vg=-15V~0V with changed rising time Tr and fixed Tf

The other of the stress configurations of the devices with different rising time is examined in Fig. 4-21; the device is biased under Vg in the OFF region and drain voltage of 20V. The stress conditions of frequency and stress time are the same as the previous section. There are various stress conditions with the variation of rising time Tr from 100ns to 700ns and fixed falling time Tf of 700ns. After the different stress conditions applied on the device, the u/u0 is extracted and shown in Fig. 4-22(a). It is distinct cases from Vg in ON/OFF region. As the rising time is set to an appropriate value, the stress results would show that the mobility degraded slightly and the sub-threshold swing also became lower, as shown in Fig. 4-22(b). However, if the rising time is set to a value which is higher or lower than the same appropriate value, the mobility would degrade seriously. Therefore, the dependence for the Tr would exhibit a turn-around behavior, which can both be observed in the u/u0 and S.S dependence.

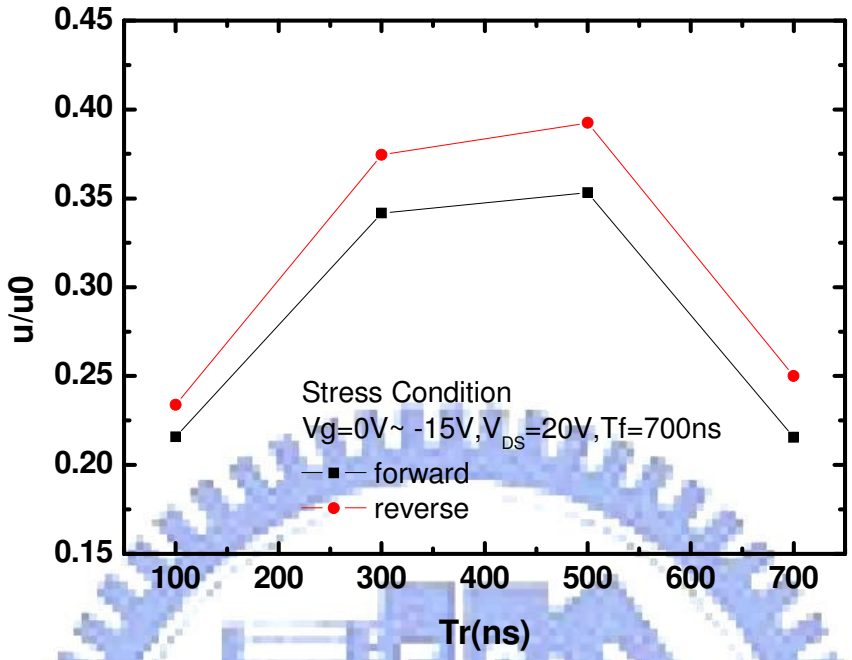


Fig. 4-22(a) Degradation of μ/μ_0 in N-channel TFT under AC stress with Vg = -15V to 0V measured for various rising times Tr and for Tf = 700ns

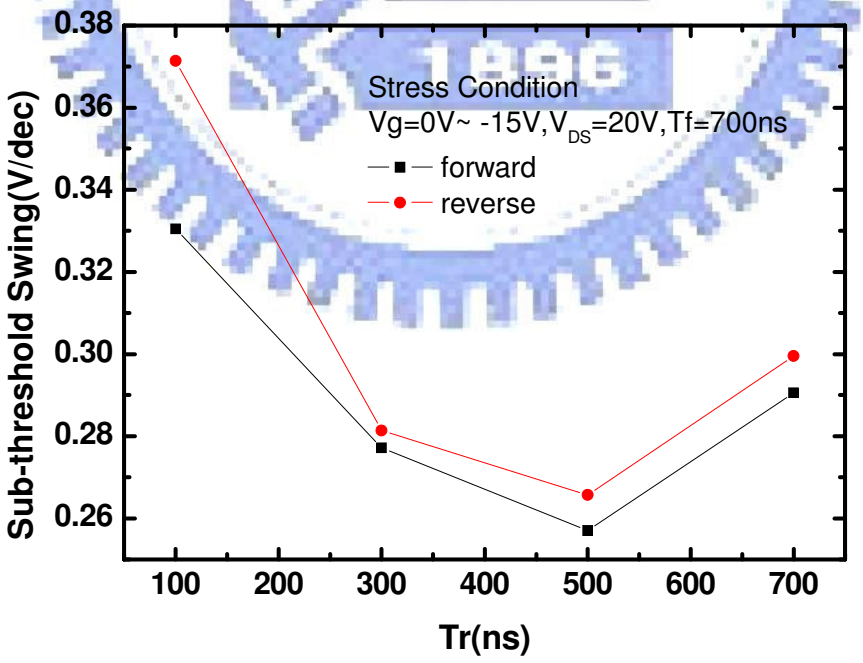


Fig. 4-22(b) Degradation of S.S in N-channel TFT under AC stress with Vg = -15V to 0V measured for various rising times Tr and for Tf = 700ns

Fig. 4-23(a) and Fig. 4-23(b) shows the C_{GS} and C_{GD} curves of the devices stressed with various rising time in the OFF region. It is observed that the C_{GS} curve also degrades seriously under identical stress conditions. The other two C_{GS} curves under Tr from 100ns to 300ns with fixed Tf are almost no change. As the rising time Tr of 700ns and falling time Tf of 700ns, the C_{GD} curve stretches worst.

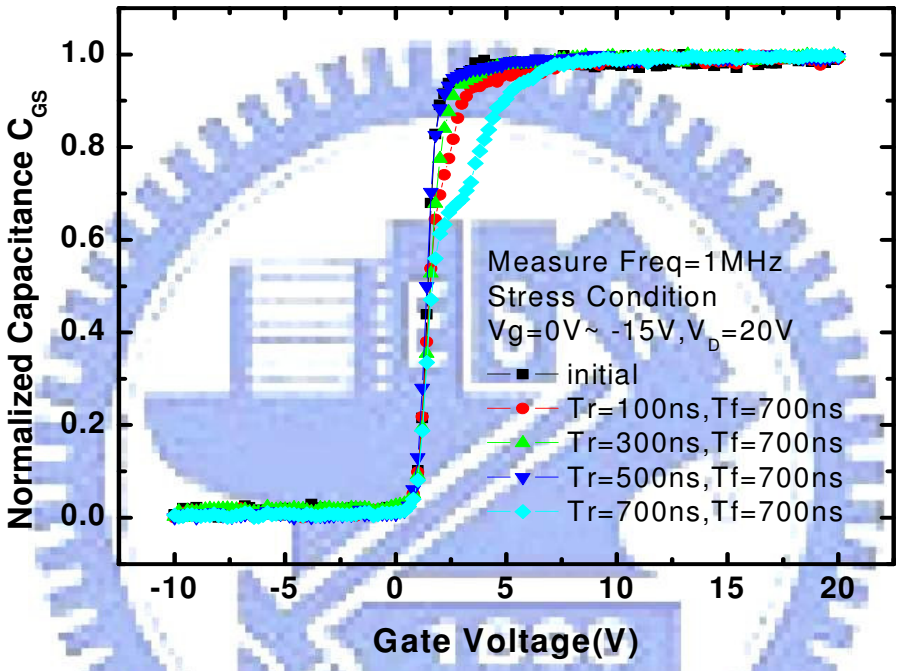


Fig. 4-23(a) Degradation of normalized C_{GS} curve in N-channel under Vg=-15V~0V measured for various rising times Tr and for Tf = 700ns at freq=1MHz

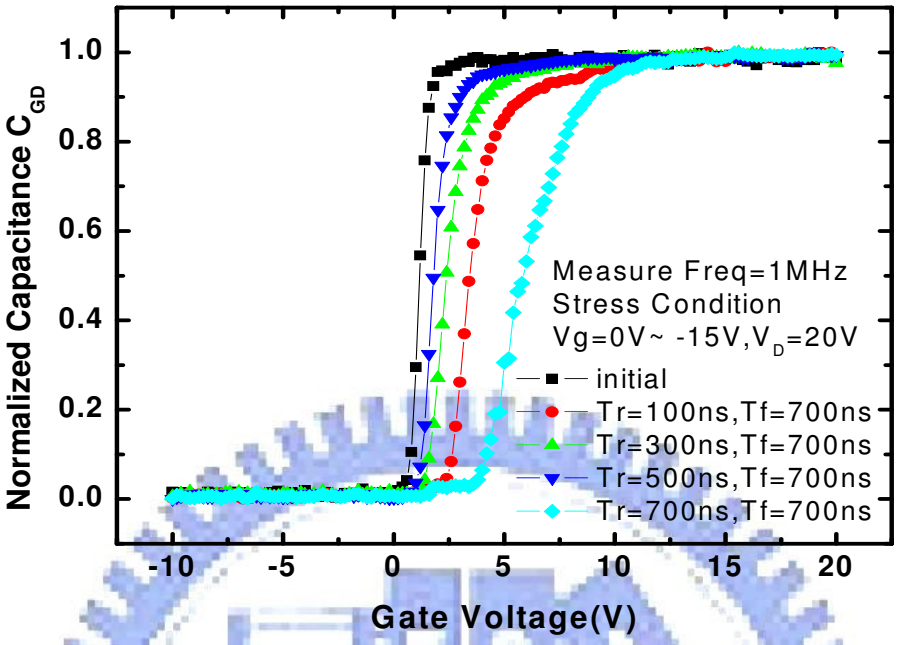


Fig. 4-23(b) Degradation of normalized C_{GD} curve in N-channel under Vg=-15V~0V measured for various rising times Tr and for Tf = 700ns at freq=1MHz

4.4.2 Effect of Falling Time

4.4.2.1 Vg in ON and OFF Region

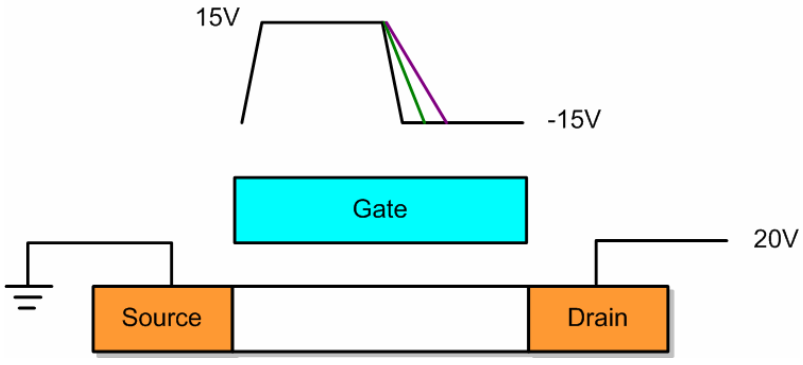


Fig. 4-24 TFT model in N-channel under Vg=-15V~15V with changed falling time Tf and fixed Tr

One of the stress arrangements with different falling time is examined in Fig. 4-24; the

device is biased under Vg of ON/OFF region and drain voltage of 20V. The frequency is equal to 500 KHz, and stress time is set to 60 seconds. There are various stress conditions with the variation of falling time Tf from 100ns to 700ns and fixed rising time Tr of 700ns. After the different stress conditions are applied on the devices individually, the u/u0 is extracted and shown in Fig. 4-25. As the falling time is set to an appropriate value, the stress results would show that the mobility degrades seriously. Nevertheless, if the falling time is set to a value which is higher or lower than the above mentioned, the mobility would degrade slightly.

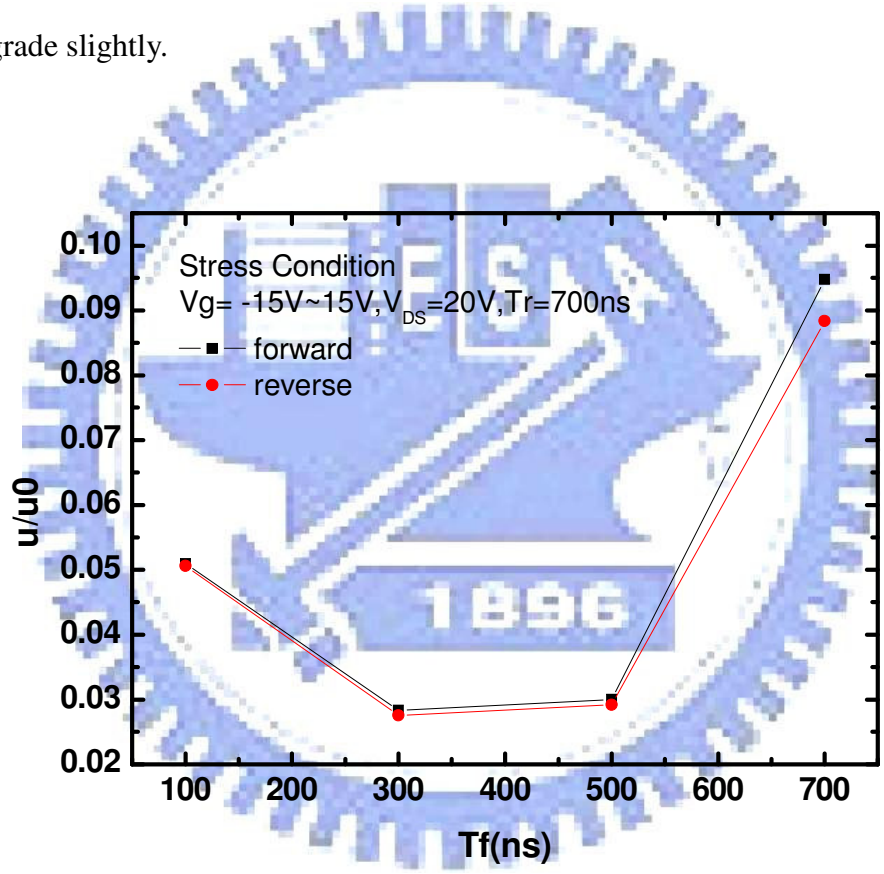


Fig. 4-25 Degradation of μ/μ_0 in N-channel TFT under AC stress with Vg = -15V to 0V measured for various falling times Tf and for Tr = 700ns

Fig. 4-26(a) and Fig. 4-26(b) shows the C_{GS} and C_{GD} curves of the devices stressed with various falling time. Among the different stress conditions with falling time Tf from 100ns to 500ns and fixed Tr 700ns, it is observed that the C_{GS} curve seriously degraded

under falling time of 300ns with fixed rising time of 700ns. We also could find that the C_{GD} curve with the falling time 300ns degrades most. It would cause that higher gate bias needed to be applied to the gate to transit the C_{GD} curve from off to on. If the stress condition is set with rising time Tr 700ns and falling time Tf 700ns, it shows another degradation mechanism. It only requires fewer applied gate voltage to turn the C_{GD} on. However, the degree of the stretch-out of the curve becomes more seriously. Briefly, there is another degradation mechanism when the stress condition is set under rising time Tr 700ns with falling time Tf 700ns.

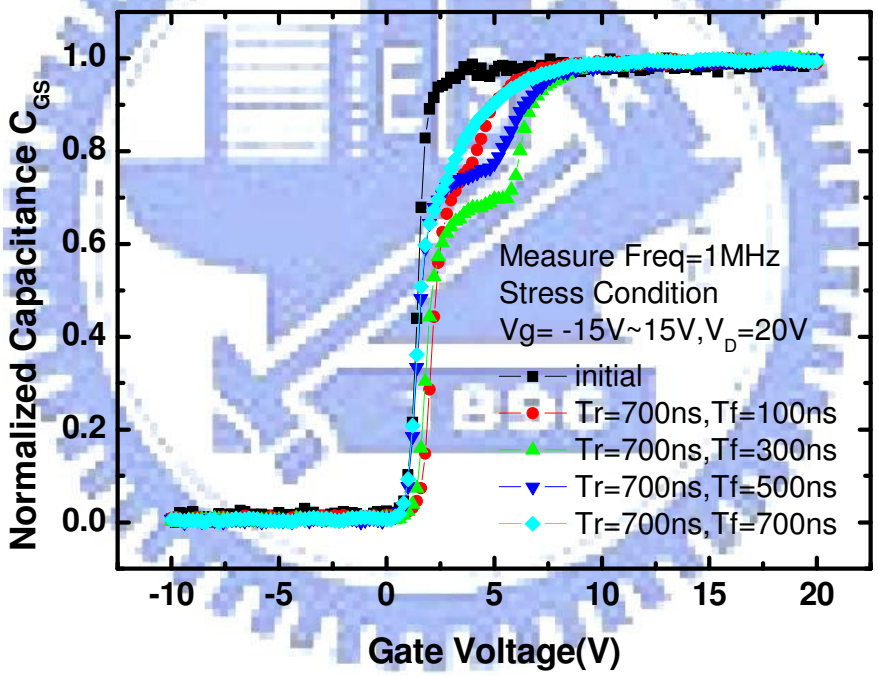


Fig. 4-26(a) Degradation of normalized C_{GS} curve in N-channel under Vg=-15V~15V measured for various Tf and for Tr = 700ns at freq=1MHz

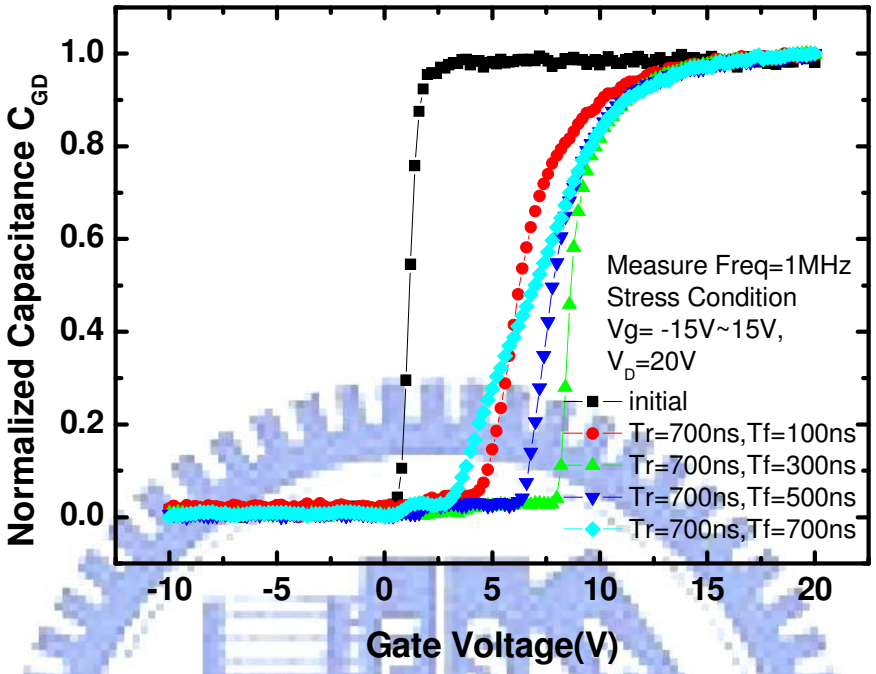


Fig. 4-26(b) Degradation of normalized C_{GD} curve in N-channel under Vg=-15V~15V measured for various Tf and for Tr = 700ns at freq=1MHz

4.4.2.2 Vg in the OFF Region

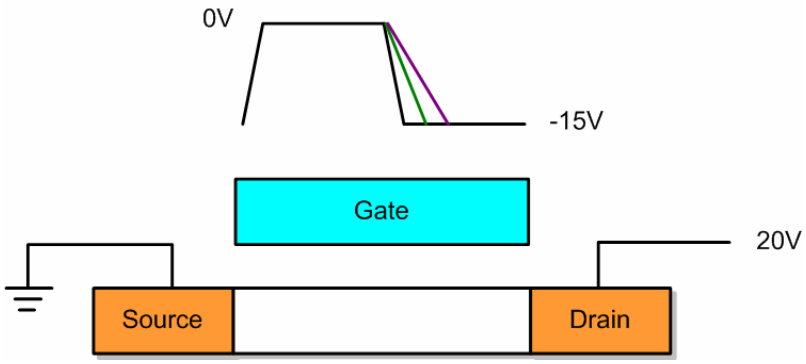


Fig. 4-27 TFT model in N-channel under Vg=-15V~0V with changed falling time Tf and fixed Tr

The stress arrangement for different falling time is examined in Fig. 4-27; the device is biased that Vg is in the off region and drain voltage is 20V. The stress conditions of

frequency and stress time are the same as above. There are various stress conditions with the variation of falling time Tf from 100ns to 700ns and fixed rising time Tr of 700ns. After the different stress conditions are applied on the devices individually, the u/u0 is extracted and shown in Fig. 4-28. As the falling time is set to an appropriate value, the stress results would show that the mobility degraded slightly. However, if the falling time is set to a value which is higher or lower than the above mentioned, the mobility would degrade more. We should notice that the degree of the degradation between the worst and the most slightly cases, there is no large difference. Consequently, the degradation is not related to falling time Tf.

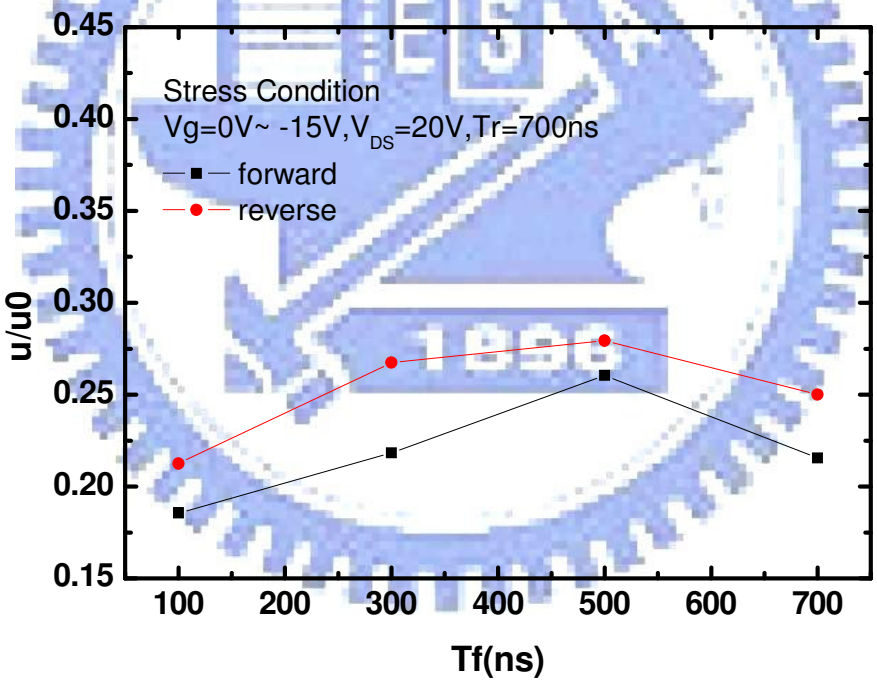


Fig. 4-28 Degradation of μ/μ_0 in N-channel TFT under AC stress with Vg = -15V to 0V measured for various falling times Tf and for Tr = 700ns

Fig. 4-29(a) and Fig. 4-29(b) shows the C_{GS} and C_{GD} curves of the devices stressed with various falling time. It was observed that for increasing falling time Tf with fixed

rising time Tr, the damage region of C_{GS} curve locates at the Vg near V_{FB}. The C_{GS} curve under Tr of 300ns and Tf of 700ns was almost no change. The C_{GD} curve also degraded seriously in the same way, and it stretched to positively. It stretched mostly under Tr of 700ns and Tf of 500ns.

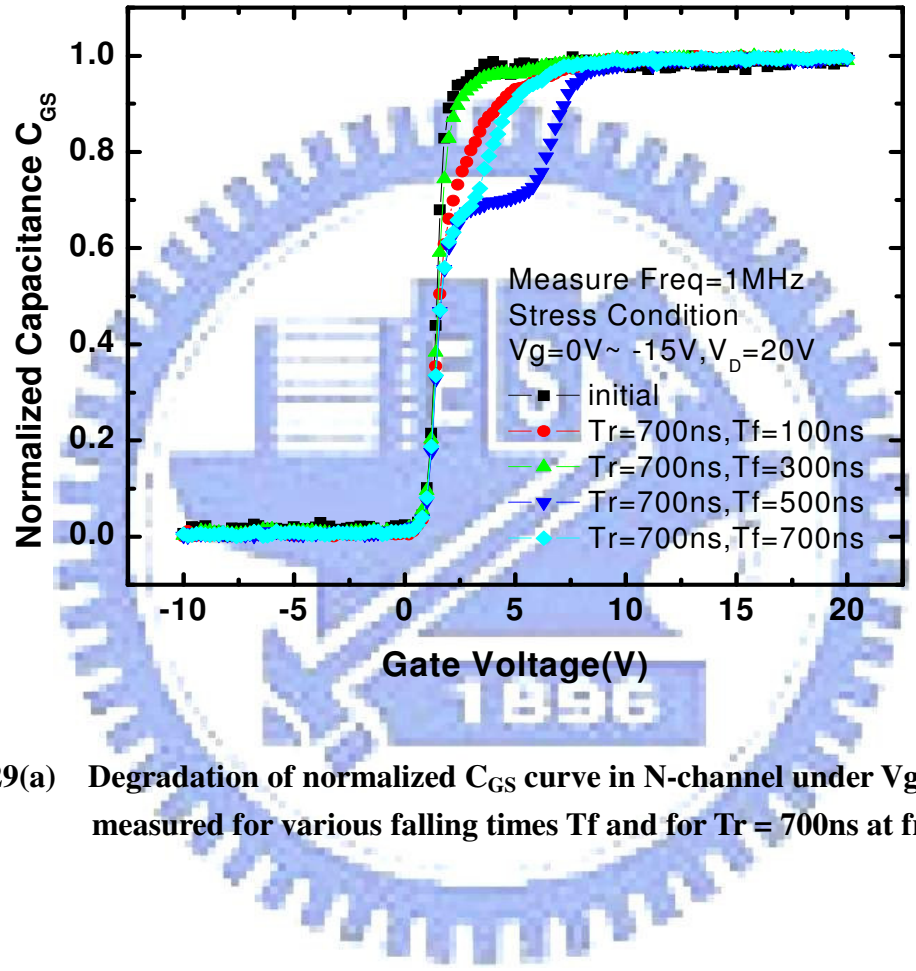


Fig. 4-29(a) Degradation of normalized C_{GS} curve in N-channel under Vg=-15V~0V measured for various falling times Tf and for Tr = 700ns at freq=1MHz

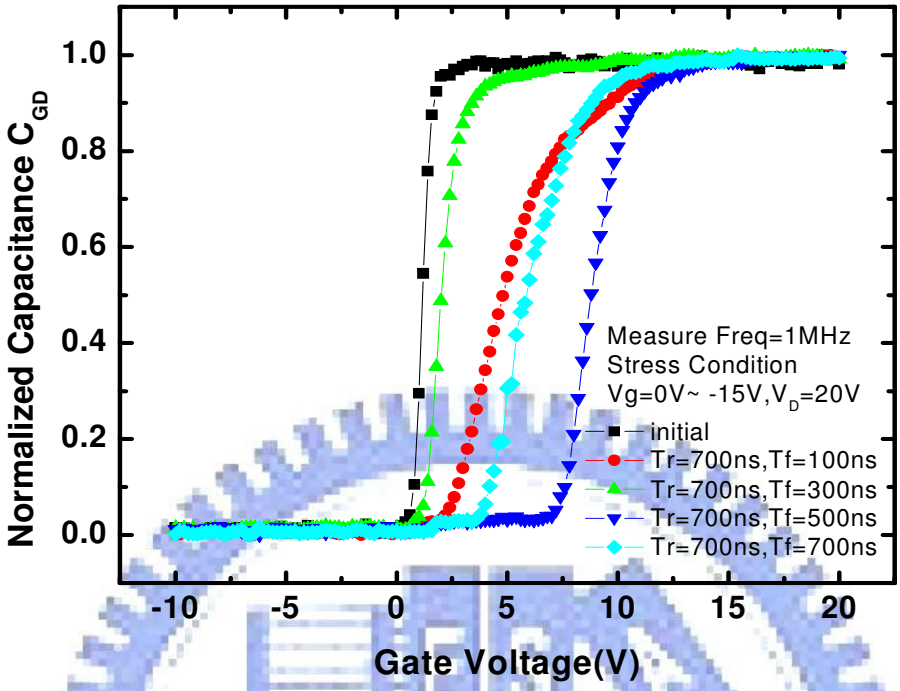


Fig. 4-29(b) Degradation of normalized C_{GD} curve in N-channel under Vg=-15V~0V measured for various falling times Tf and for Tr = 700ns at freq=1MHz

4.5 Results and Discussions

In prior studies, the case of the degradation under DC stress usually was attributed to the generation of traps at deep states in poly-Si grains, as well as the threshold voltage shift caused by charge trapping in the gate oxide and at the interface states. For the mechanism of degradtion under gate AC stress, the mechanism is similar to hot carrier effect. Channel electrons gain energy in the high-field region from drain and are accelerated towards the drain junction, where the impact ionization may occur and electron-hole pairs may be generated. This causes the charge to be injected into the gate oxide and creates a fixed charge in the oxide.

As the gate voltage swings between the on and off region, carriers are gathered to the

oxide/poly-Si interface. When the gate voltage swings from high to low, the induced electrons in the channel would rush to the source and drain region. These carriers exposed to the high electric field move rapidly to the source and drain. They become hot carriers and cause the device degradation. The flow of the carriers reflects the displacement current induced by the AC gate pulses. With the rising time and the falling time increases, the time differential of Vg decreases, making the displacement current also decreases.

Fig. 4-30(a) shows the carrier flow under the stress of gate voltage swing from -15V to 0V. Electrons would flow from source to channel. Since the device is applied with a large drain bias, some electrons may flow from channel to drain. When the rising time increases, meaning that the larger voltage drop Vgd would stay longer, the electrons flow to high electric field near drain would result in more hot carriers. Under this stress condition, the time of high electric field is longer, as shown in Fig. 4-30(b). It might the reason why there are turning points in mobility and S.S of rising time.

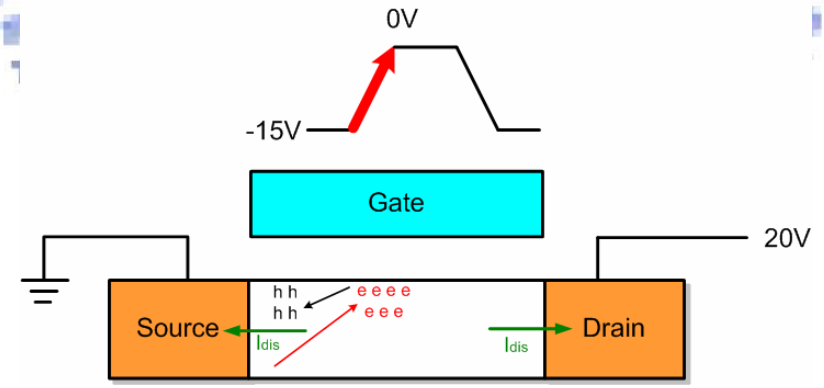


Fig. 4-30(a) The proposed AC stress degradation N-channel model under V_D=20V for various rising time Tr

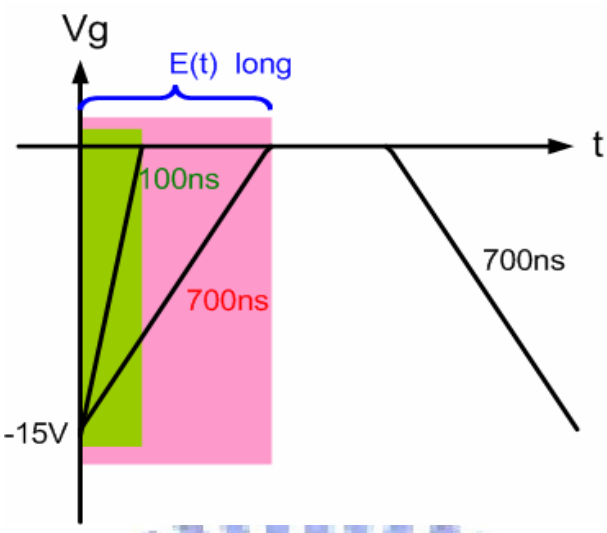


Fig. 4-30(b) The time of electric field AC stress degradation N-channel under V_D=20V for various rising time Tr

Fig. 4-31(a) shows the carrier flow under the stress of gate voltage swing from 0V to -15V. Electrons are discharged from channel to drain. Because a large Vds is applied, more electrons may flow to drain. When the falling time increases, the electrons would gain more energy to become hot carriers. Under this stress condition, the time of low electric field is longer, as shown in Fig. 4-31(b). It might be also the reason why there are turning points in mobility and S.S of falling time, too.

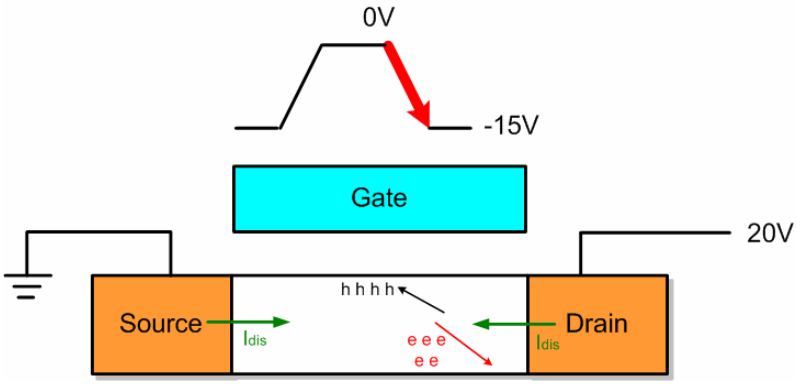


Fig. 4-31(a) The proposed AC stress degradation N-channel model under V_D=20V for various falling time Tf

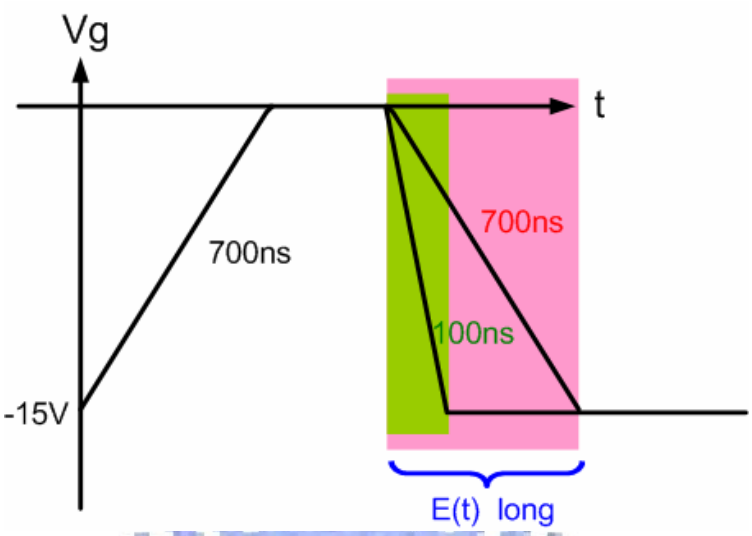


Fig. 4-31(b) The time of electric field AC stress degradation N-channel under V_D=20V for various falling time Tf

4.6 Summary

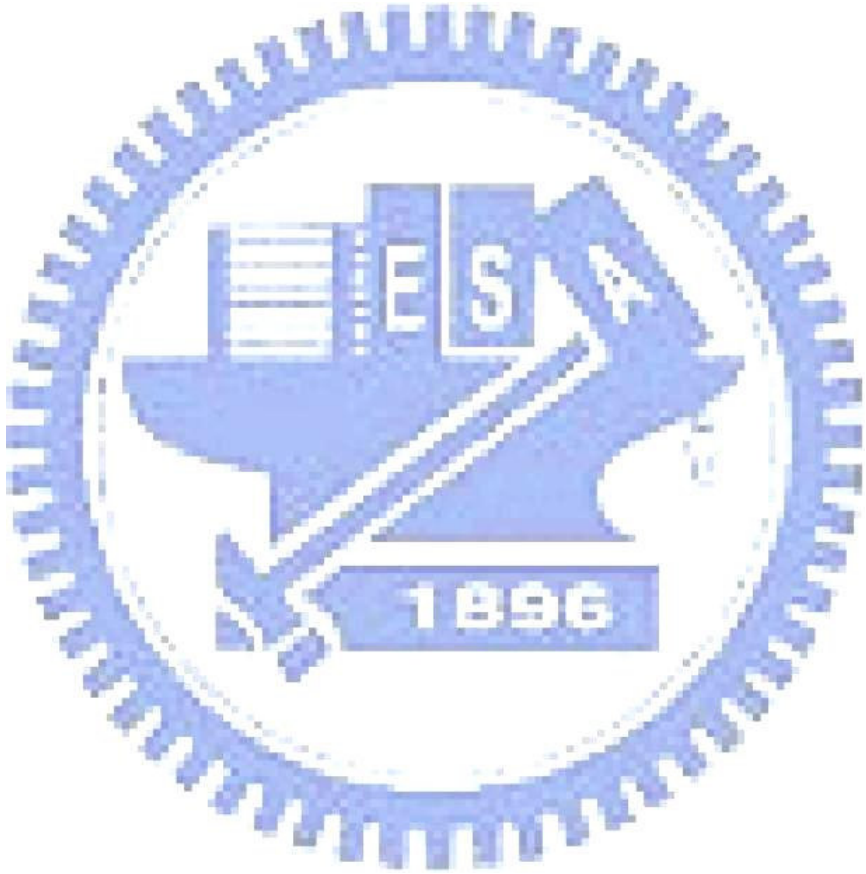
The effect of drain bias which the gate voltage stressed in the on/off region and in the off region is obvious. The higher threshold voltage, lower mobility and higher sub-threshold swing are observed. C_{GS} curves degrade slightly in the on/off region, and the phenomenon of C_{GS} curves degrades like hot carrier. However, C_{GD} curve stretches with increasing stress V_{DS}.

The effect of gate voltage range with various drain bias shows the degraded mobility and sub-threshold swing after stress. When V_{DS} is higher than 15V and Vg ranges beyond 10V, the sub-threshold swing is seriously degraded. C-V curve distorts when V_{DS} is higher than 15V.

For the rising time of gate voltage toggling with on/off region or off region, electrons are induced from source to channel. When the rising time increases, the time of high electric field is longer. It causes turning points in mobility and S.S.

The same as the falling time of gate voltage toggling with the above-mentioned region,

electrons are discharged from channel to drain. When the falling time increases, the electrons would gain more energy to become hot carriers, which may explain turning points in mobility and S.S, too.



Chapter 5

Degradation for P-type Poly-Si TFT under Gate Pulse Stress with Drain Bias

5.1 Effect of Drain Bias

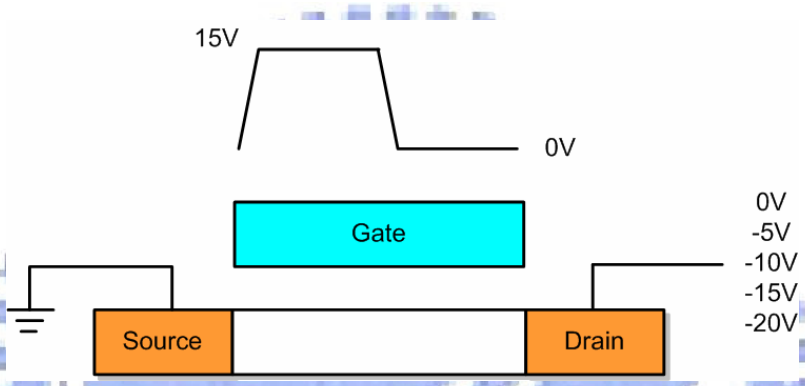


Fig. 5-1 TFT model in P-channel under various drain bias in off region

Fig. 5-1 shows the structure of the P-type poly-Si TFT under various negative drain bias in off region. The frequency is equal to 500KHz, and the stress time is set as 60 seconds. The degradation is not obvious in Id-Vg curves, and the device parameters are extracted for the following discussion. The higher stress drain bias, the higher mobility is observed after stress. Compared with the degradation of the forward and the reverse mobility, the reverse mobility is larger than the forward. The degree of mobility increase is 0.07 with the stress drain bias of -5V, as shown in Fig. 5-2(a). The initial sub-threshold swing is 0.21 V/dec. After the AC stress it moves to 0.20 V/dec, as shown in Fig. 5-2(b). Fig. 5-2(c) shows the relation of threshold voltage shift (ΔVth) after stress. As the drain voltage increases, the threshold voltage shift (ΔVth) drifts more. This part is not observed in Id-Vg curves. In addition, they depend on the stress drain bias.

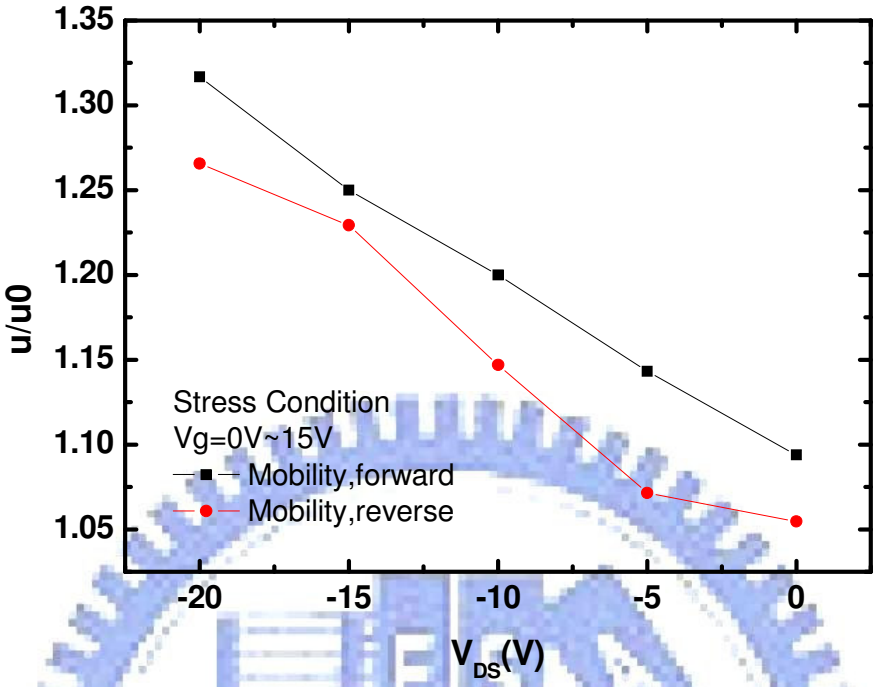


Fig. 5-2(a) Dependence of the mobility on V_{DS} with gate AC stress in off region

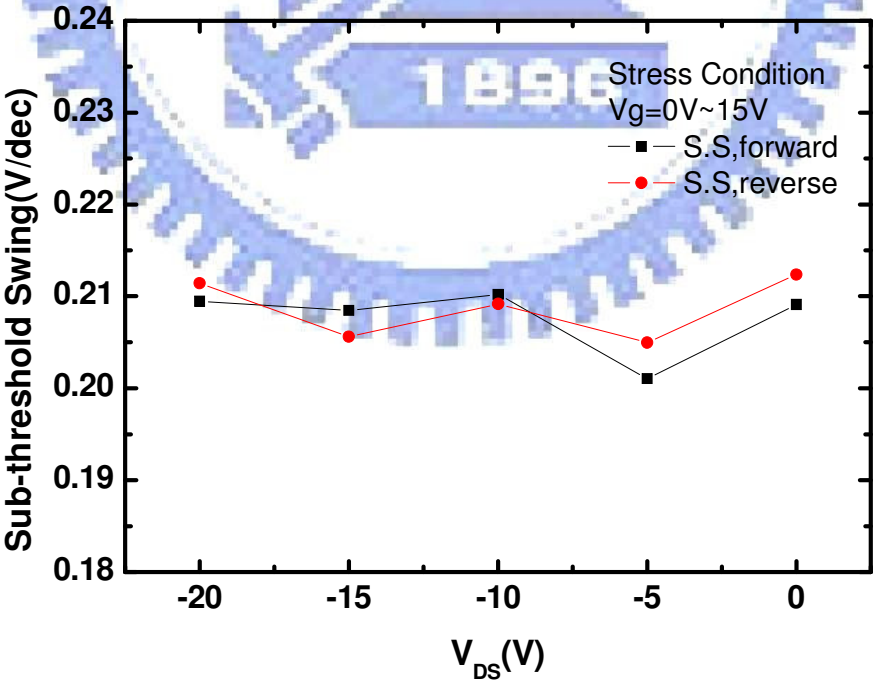


Fig. 5-2(b) Dependence of the Sub-threshold Swing on V_{DS} with gate AC stress in off region

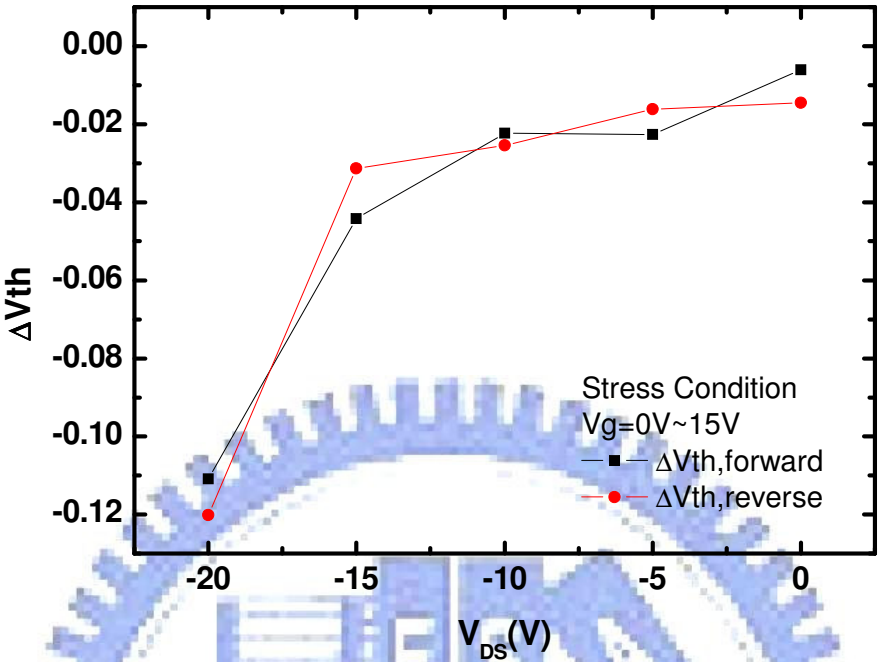


Fig. 5-2(c) Dependence of the threshold voltage shift on V_{DS} with gate AC stress in off region

By the same token, the Id-Vg transfer characteristics could not distinguish the dominant degradation region; C-V measurement is therefore employed. They could also help to investigate the asymmetry electric field near source and drain of TFTs during stress. Fig. 5-3(a) shows the normalized gate-to-source capacitance (C_{GS}) curves before and after stress with different drain voltage. Fig. 5-3(b) shows the normalized gate-to-drain capacitance (C_{GD}) curves under the same stress conditions.

Observed from Fig. 5-3(a) and Fig. 5-3(b), C_{GS} and C_{GD} curves remain almost the same and show no obvious differences as the gate voltage is smaller than the flat band voltage V_{FB}. C_{GS} curves and C_{GD} curves rise in the off region after stress. With the negative stress drain bias increases, C_{GD} curves raise more. However, the degree of C_{GS} curves raises less than that in the C_{GD} curves. The increase of the C_{GS} and C_{GD} curves for

the lower gate voltage and its degree of increase just corresponds the mobility increase of the Id-Vg curves, as shown in Fig. 5-2(a).

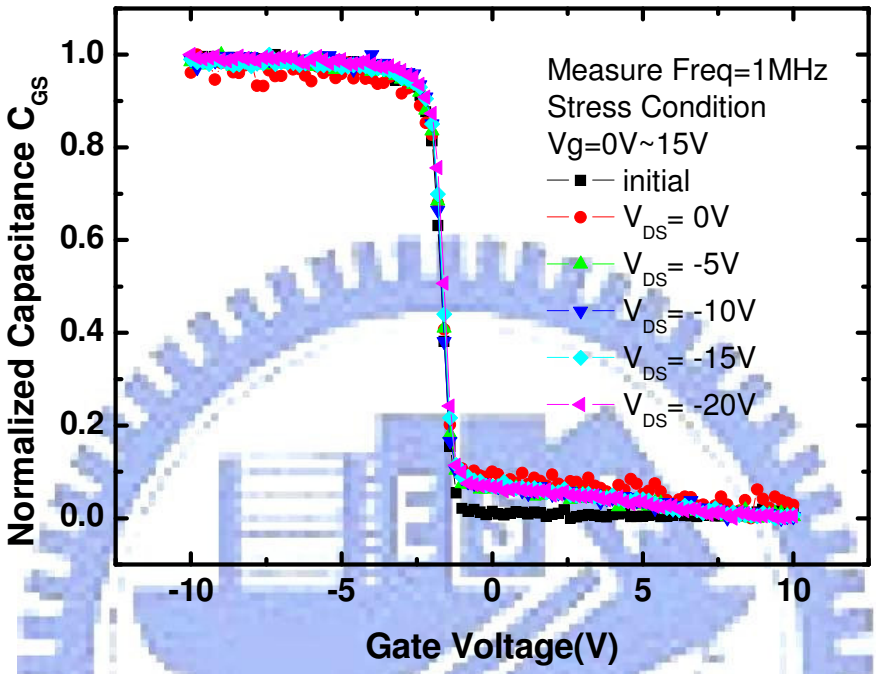


Fig. 5-3(a) Degradation of normalized C_{GS} curve in P-channel under various stress V_{DS} in off region at frequency=1MHz

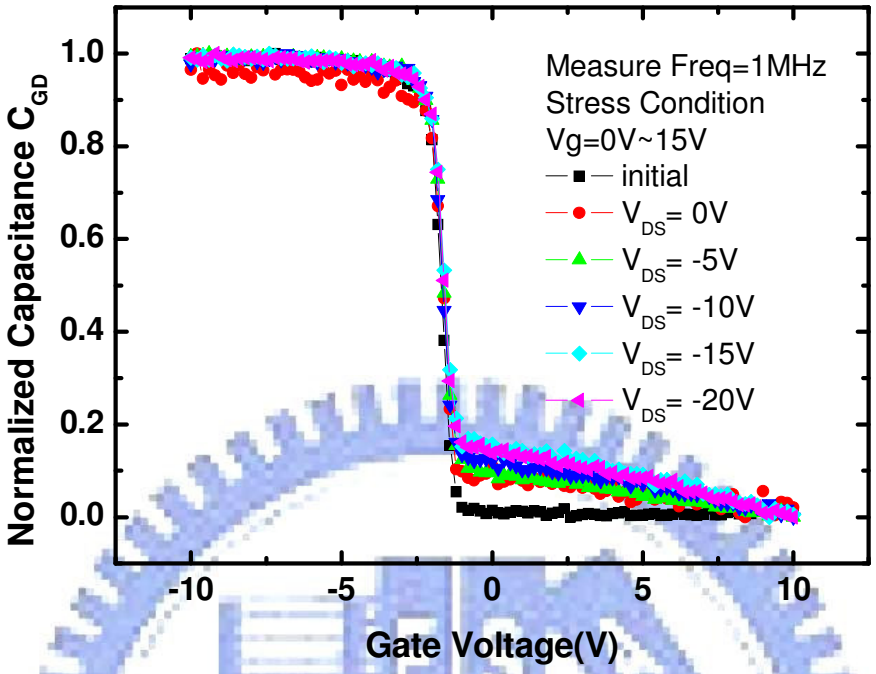


Fig. 5-3(b) Degradation of normalized C_{GD} curve in P-channel under various stress V_{DS} in off region at frequency=1MHz

5.2 Effect of Gate Voltage Range

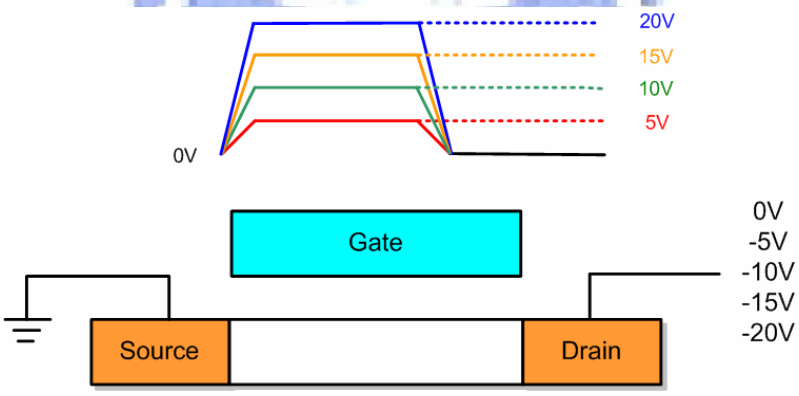


Fig. 5-4 TFT model in P-channel under various V_{DS} and range of gate voltage

Fig. 5-4 shows the structure for stressing the device for the 60s dynamic gate stress

with different negative drain voltage V_D and different gate voltage ranges. The frequency is equal to 500KHz. The pulse signals of Vgh ranges from 5V to 20V and Vgl of 0V to the gate electrode of TFTs. Moreover, the various negative DC voltages are applied to the drain.

The larger gate voltage range and negative drain bias, the high increase of the mobility is observed as shown in Fig. 5-5. It is observed that when V_{DS} is 0V or -5V and Vg range is smaller than 10V, the mobility exhibits almost no difference. When negative drain bias is higher than -15V and Vg range beyond 10V, the mobility seriously increases.

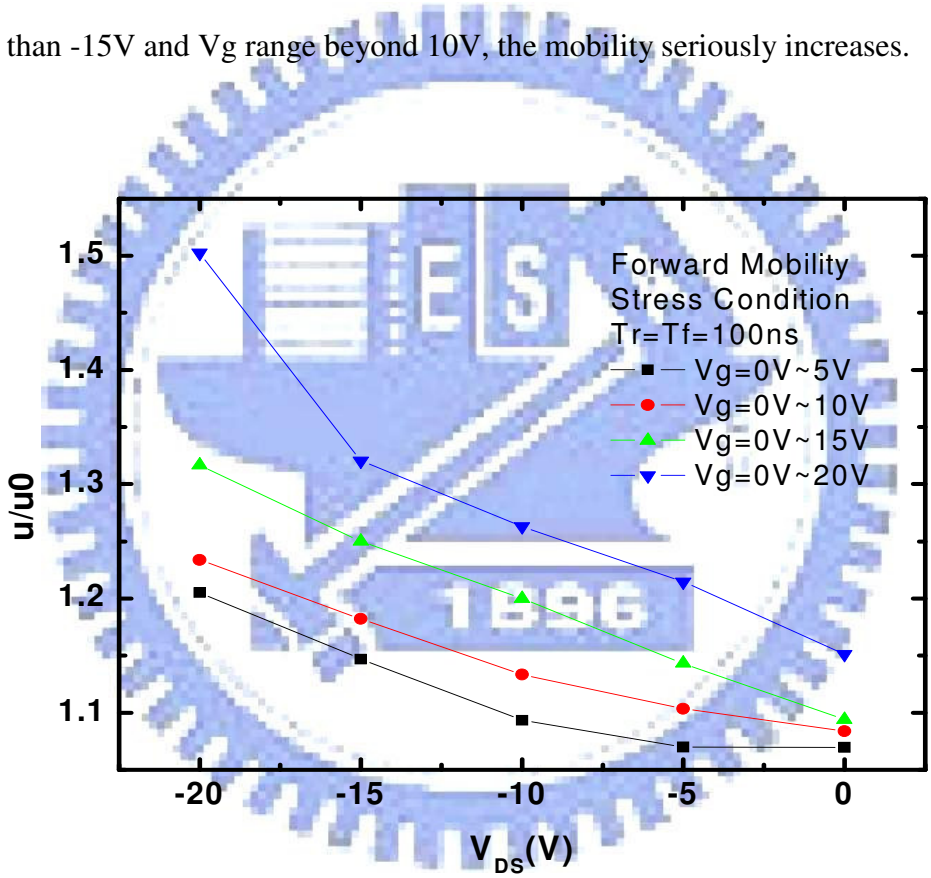


Fig. 5-5 Degradation of u/u0 in P-channel under various V_{DS} and range of gate voltage

Fig. 5-6(a) and Fig. 5-6(b) shows the C_{GS} and C_{GD} curves of the devices stressed by Vg=0V~5V and various drain bias voltages. Fig. 5-7(a) and Fig. 5-7(b) shows the curves of the devices stressed by Vg=0V~10V, while Fig. 5-8, Fig. 5-9 respectively show the

stress Vg=0V~15V and Vg=0V~20V. It is observed the C_{GS} and C_{GD} curves rise in Vg of the off region after stress. When V_D increases, C_{GD} curves have larger increase. However, the degree of increase in C_{GS} curves is not much as C_{GD} curves. In the same way, C_{GS} curves raise the range more with negative drain bias increases. The C-V increase in the off region also corresponds to the mobility increase in the Id-Vg curves.

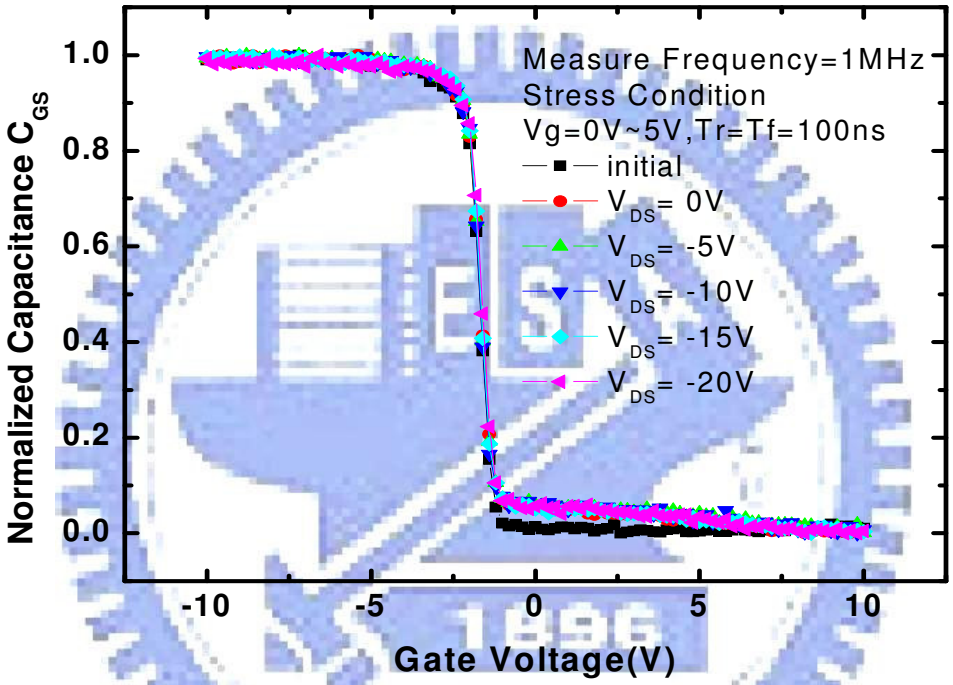


Fig. 5-6(a) Degradation of normalized C_{GS} curve in P-channel under Vg=0V~5V with various V_{DS} at frequency=1MHz

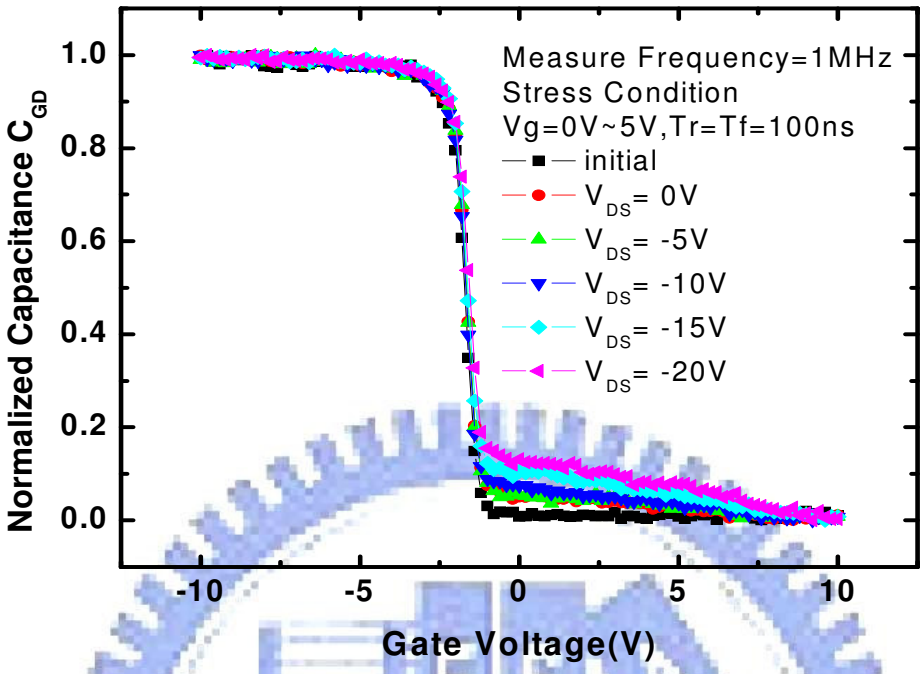


Fig. 5-6(b) Degradation of normalized C_{GD} curve in P-channel under Vg=0V~5V with various V_{DS} at frequency=1MHz

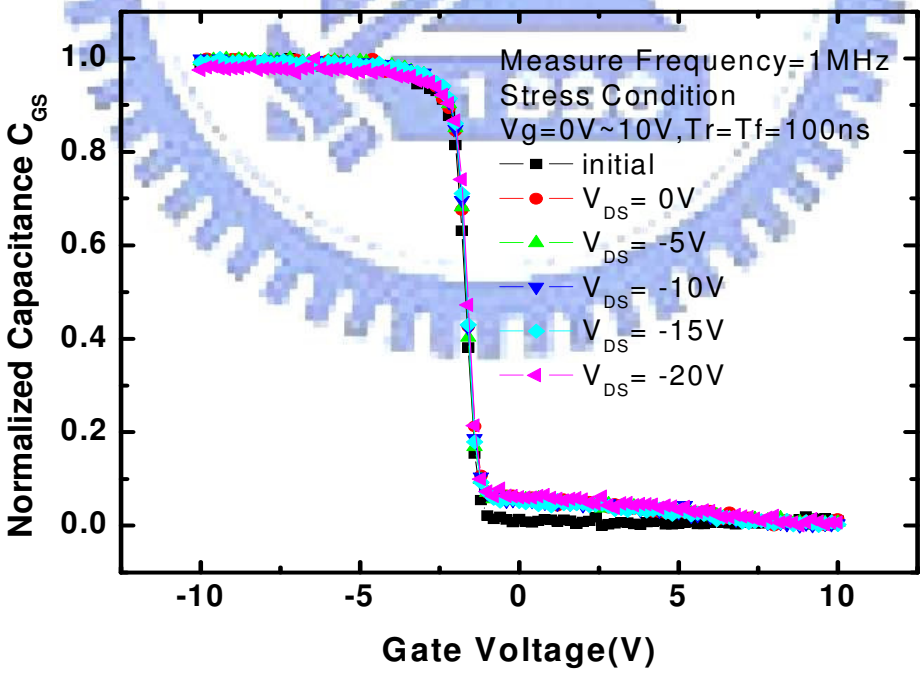


Fig. 5-7(a) Degradation of normalized C_{GS} curve in P-channel under Vg=0V~10V with various V_{DS} at frequency=1MHz

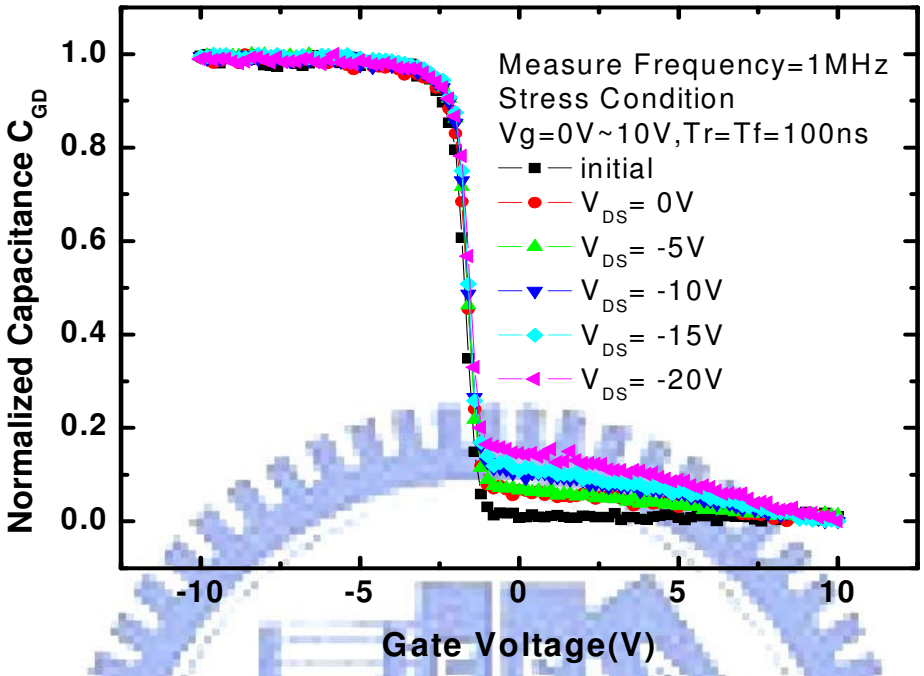


Fig. 5-7(b) Degradation of normalized C_{GD} curve in P-channel under Vg=0V~10V with various V_{DS} at frequency=1MHz

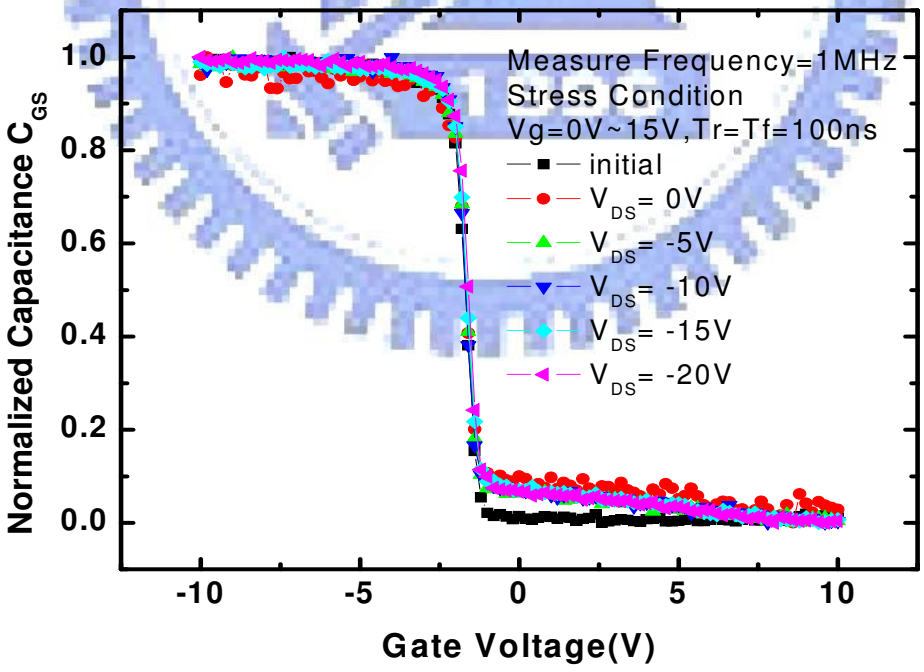


Fig. 5-8(a) Degradation of normalized C_{GS} curve in P-channel under Vg=0V~15V with various V_{DS} at frequency=1MHz

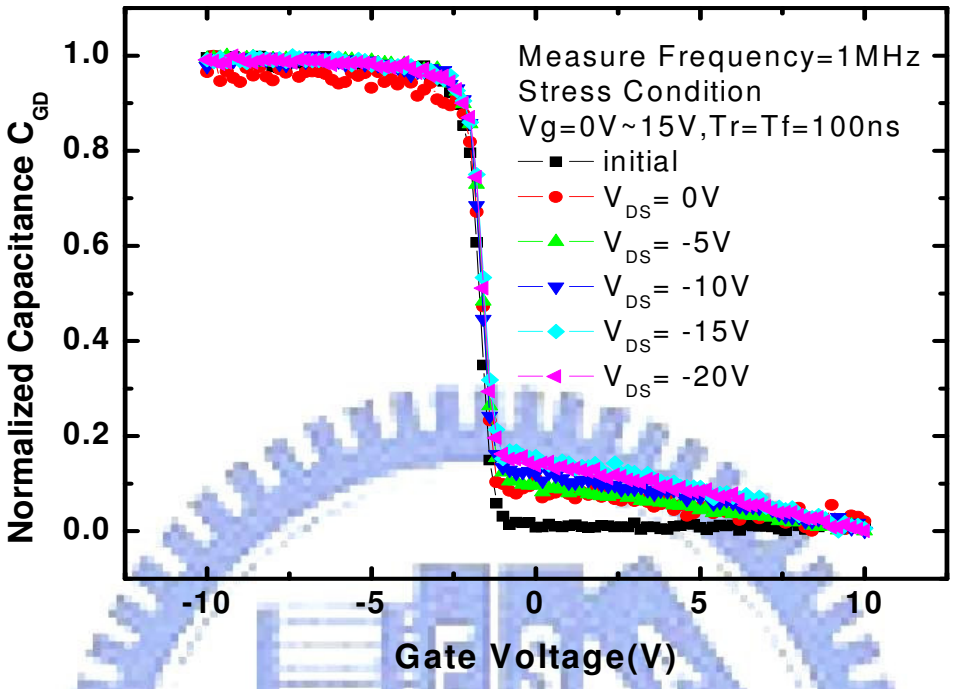


Fig. 5-8(b) Degradation of normalized C_{GD} curve in P-channel under Vg=0V~15V with various V_{DS} at frequency=1MHz

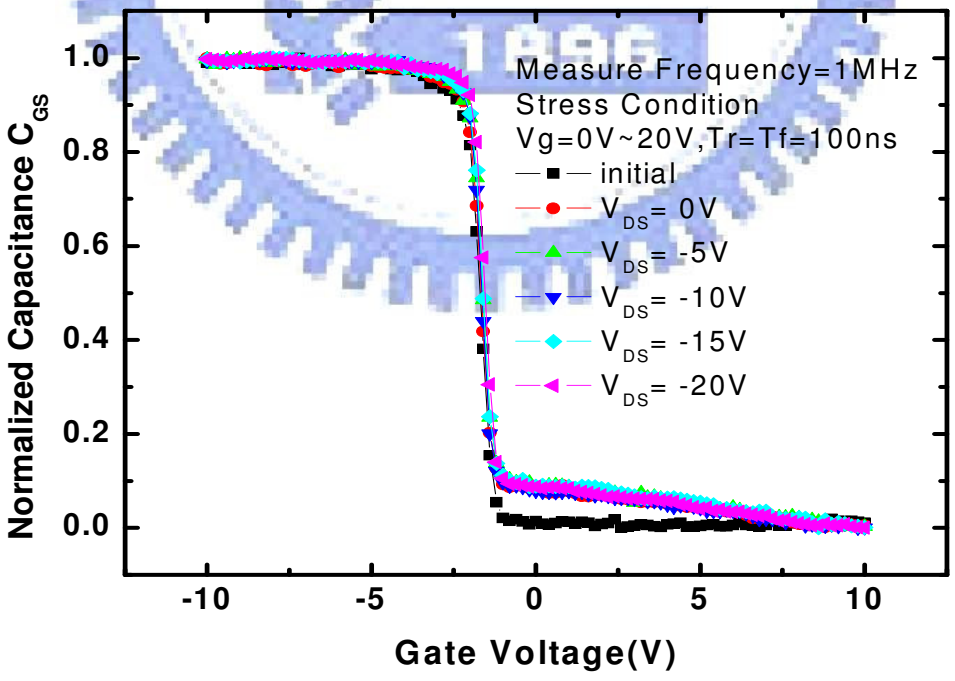


Fig. 5-9(a) Degradation of normalized C_{GS} curve in P-channel under Vg=0V~20V with various V_{DS} at frequency=1MHz

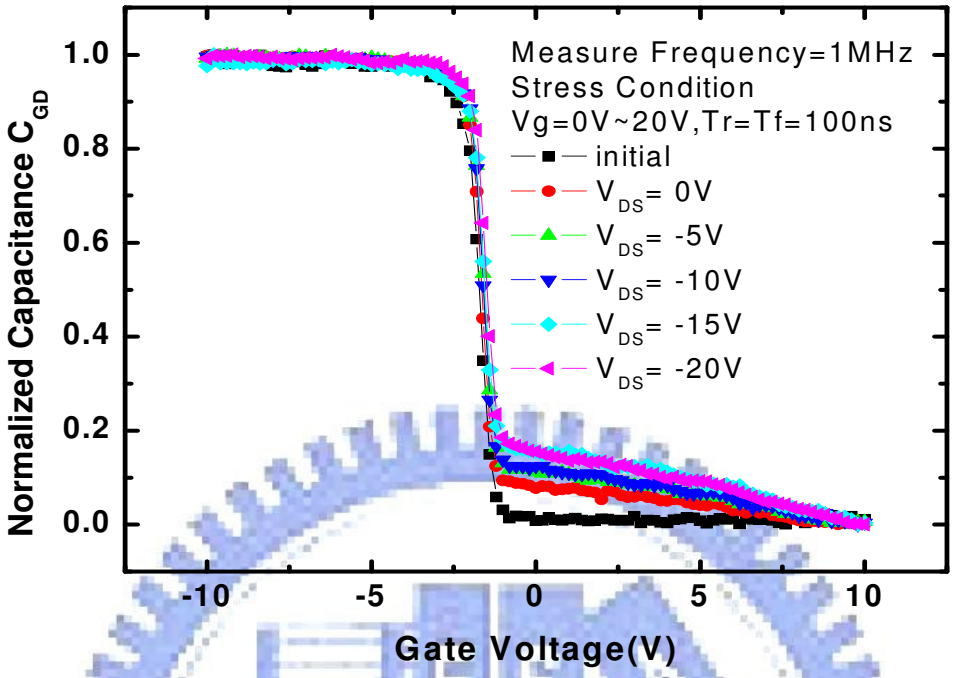


Fig. 5-9(b) **Degradation of normalized C_{GD} curve in P-channel under Vg=0V~20V with various V_{DS} at frequency=1MHz**

5.3 Other Effects

5.3.1 Effect of Rising Time

5.3.1.1 Vg in ON and OFF Region

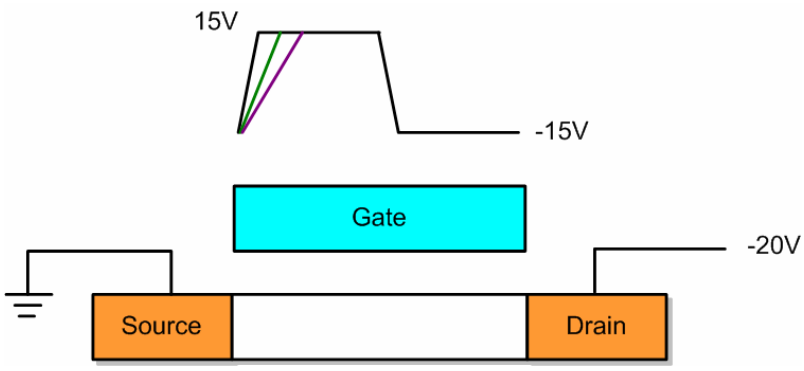


Fig. 5-10 **TFT model in P-channel under Vg=-15V~15V with changed rising time Tr and fixed Tf**

One of the degradation arrangements of the devices shows in Fig. 5-10; the device is biased under Vg of ON/OFF region and drain voltage of -20V. The frequency of the gate signal is 500 KHz and stress time is set to 60 seconds. There are various stress conditions with the variation of rising time Tr from 100ns to 700ns and a fixed falling time Tf of 700ns. After the different stress conditions applied on the devices, the u/u0 was extracted and shown in Fig. 5-11. As the rising time is 300ns, the stress would cause less mobility increase. However, if the rising time is set to a value which is higher or lower than the above mentioned value, the mobility would increase seriously.

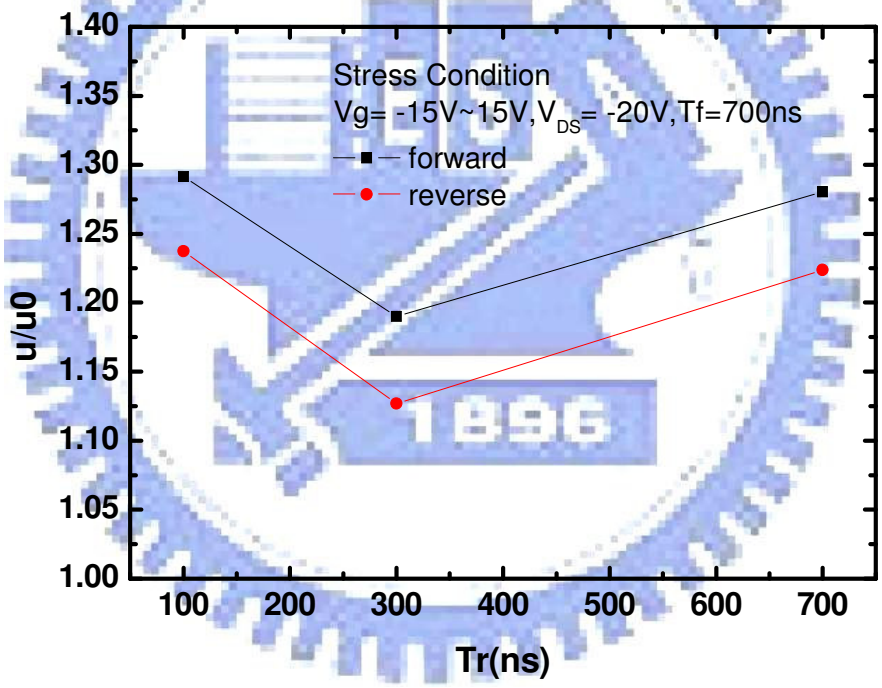


Fig. 5-11 Degradation of μ/μ_0 in P-channel TFT under AC stress with Vg = -15V to 15V measured for various rising times Tr and for Tf = 700ns

Fig. 5-12(a) and Fig. 5-12(b) show the C_{GS} and C_{GD} curves of the devices stressed with various rising time. It is observed that the C_{GS} curves and C_{GD} curves rise in Vg of the off region after stress. The increase in the C_{GS} and C_{GD} curves does not exhibit apparent

dependence on Tr. However, the degree of C_{GS} curves is not as much as that of C_{GD} curves.

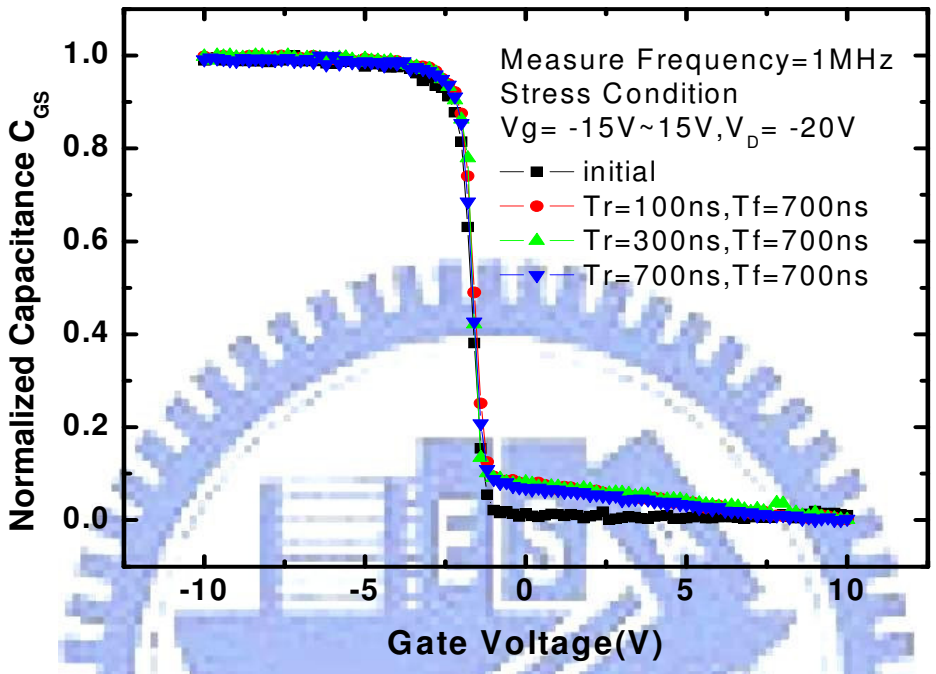


Fig. 5-12(a) Degradation of normalized C_{GS} curve in P-channel under Vg=-15V~15V measured for various Tr and for Tf = 700ns at freq=1MHz

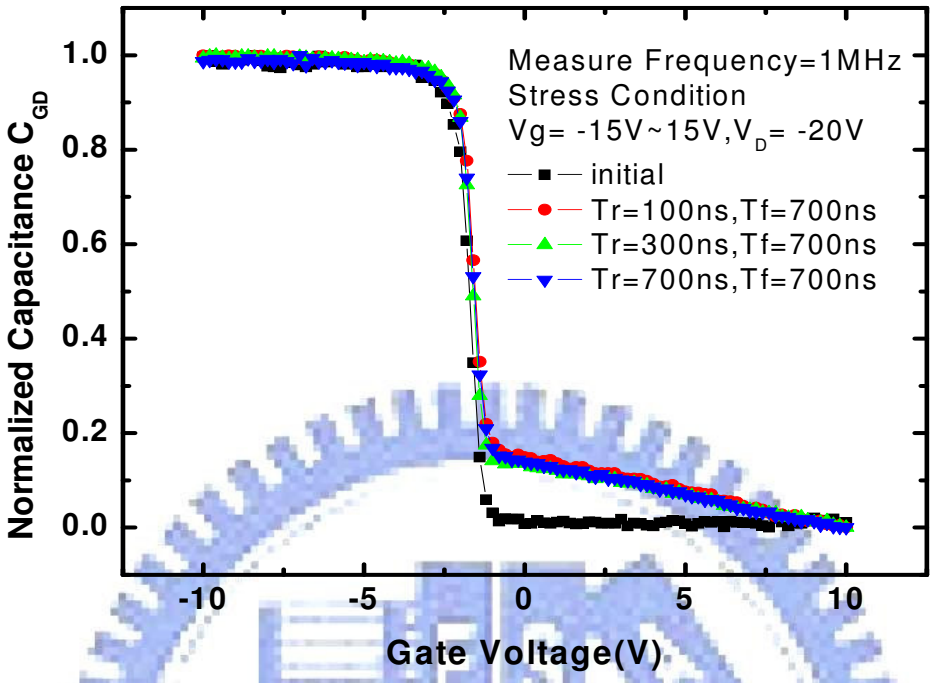


Fig. 5-12(b) Degradation of normalized C_{GD} curve in P-channel under Vg=-15V~15V measured for various Tr and for Tf = 700ns at freq=1MHz

5.3.1.2 Vg in the OFF Region

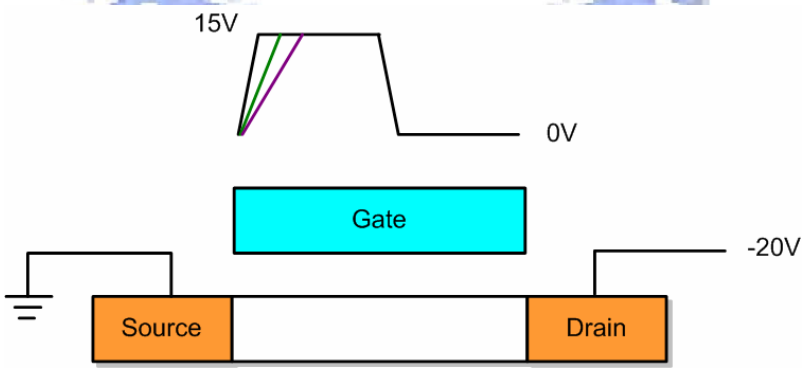


Fig. 5-13 TFT model in P-channel under Vg=0V~15V with changed rising time Tr and fixed Tf

The experiment structure of the device for varying the dependence of rising time is

shown in Fig. 5-13; the device is biased the Vg in the off region and drain voltage of -20V. The stress conditions of frequency and stress time are the same in the previous sections. There are various stress conditions with the changing of rising time Tr ranging from 100ns to 700ns and fixed falling time Tf of 700ns. After the different stress conditions applied on the devices individually, the u/u0 is extracted and shown in Fig. 5-14. As the rising time getting shorter, the mobility increases seriously after stress. The degradation is strongly depended on the rising time Tr. This result suggests that the degradation occur when the gate voltage is transited from low to high.

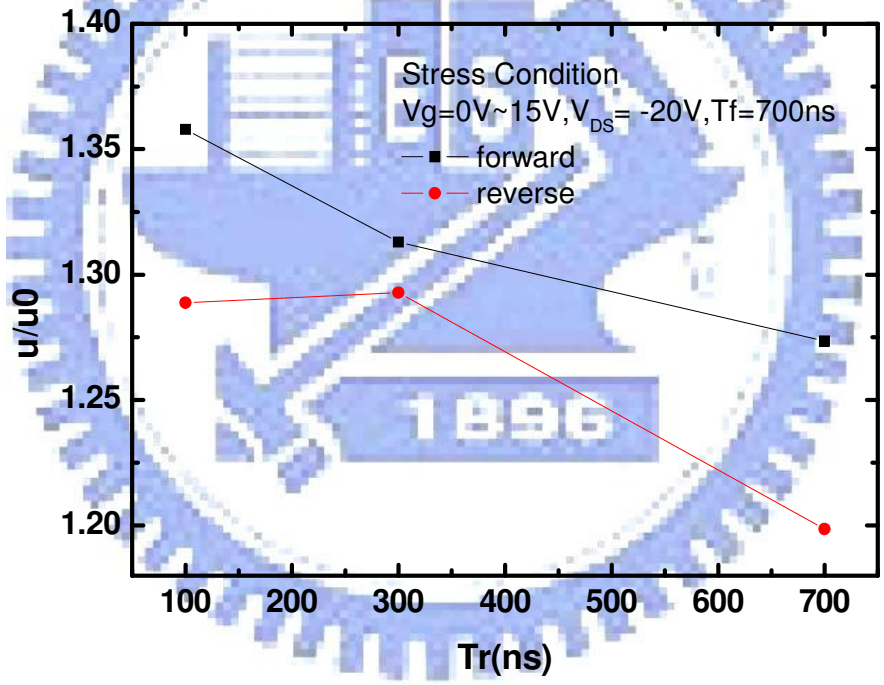


Fig. 5-14 Degradation of μ/μ_0 in P-channel TFT under AC stress with Vg = 0V to 15V measured for various rising times Tr and for Tf = 700ns

Fig. 5-15(a) and Fig. 5-15(b) shows the C_{GS} and C_{GD} curves of the devices stressed with various rising time. It is observed that the C_{GS} and C_{GD} curves rise in the off region after stress. The increase of the C-V curves for the voltage lower than V_{FB} shows no

apparent dependence with Tr. However, the degree of C_{GS} curves is smaller than that in C_{GD} curves.

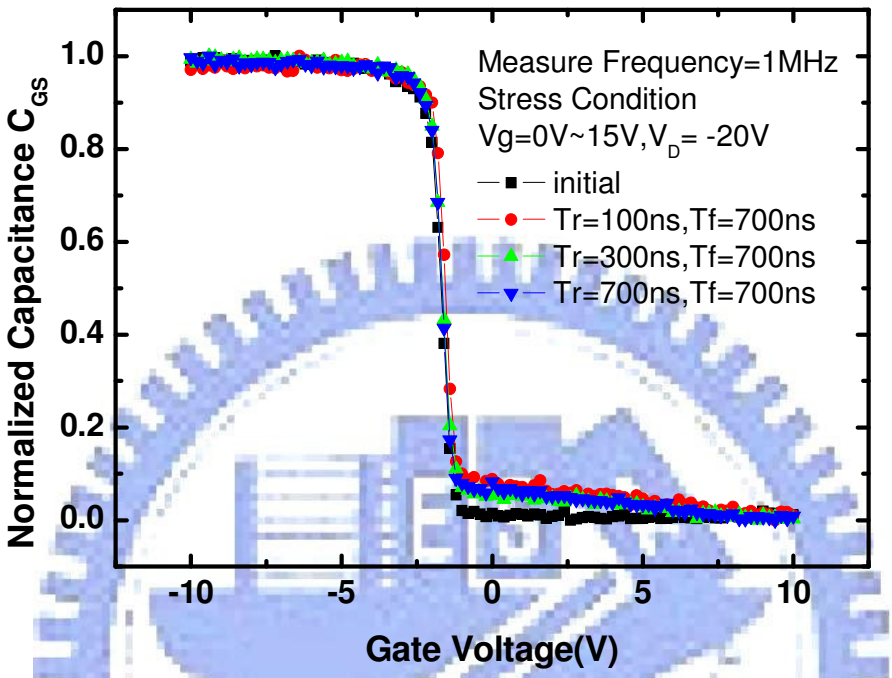


Fig. 5-15(a) Degradation of normalized C_{GS} curve in P-channel under Vg=0V~15V measured for various Tr and for Tf = 700ns at measuring freq=1MHz

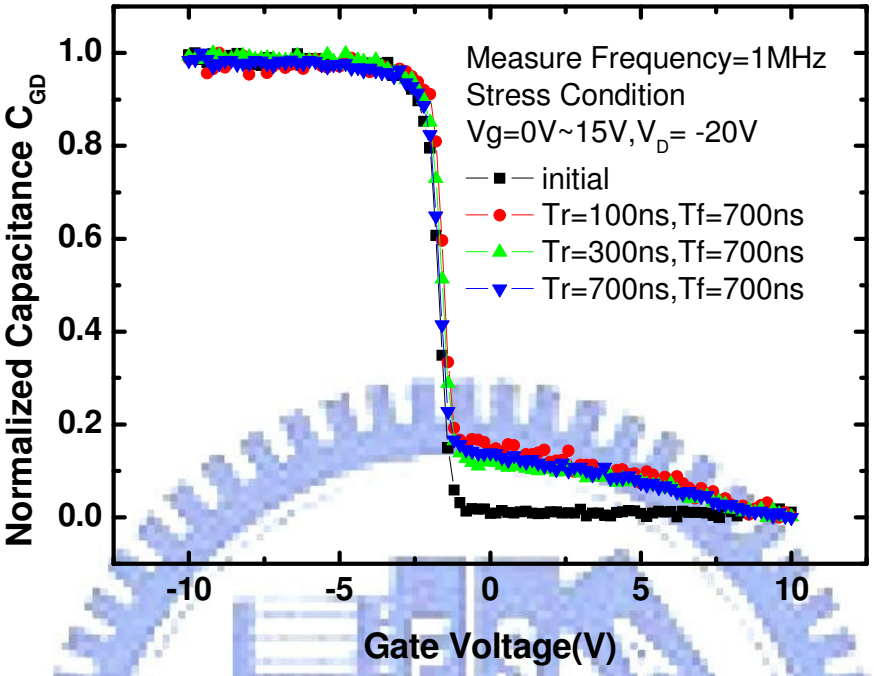


Fig. 5-15(b) Degradation of normalized C_{GD} curve in P-channel under Vg=0V~15V measured for various Tr and for Tf = 700ns at measuring freq=1MHz

5.3.2 Effect of Falling Time

5.3.2.1 Vg in ON and OFF Region

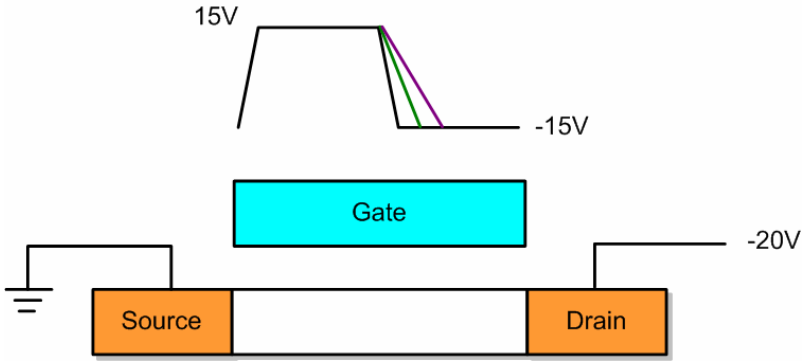


Fig. 5-16 TFT model in P-channel under Vg=-15V~15V with changed falling time Tf and fixed Tr

The stress structure for examining the falling time dependence is shown in Fig. 5-16;

the device is stressed between that the Vg ON/OFF region and drain voltage is -20V. The frequency is equal to 500 KHz, and stress time is 60 seconds. The stress conditions with are falling time Tf varies from 100ns to 700ns and fixed rising time Tr of 700ns. After the different stress conditions applied on the devices individually, the u/u0 is extracted and shown in Fig. 5-17. As the falling time getting longer, the mobility increases larger after stress. The increase is strongly depended on the falling time Tr. This result suggests that the degradation occur when the gate voltage is transited from high to low. In other words, the falling time of the gate voltage would dominate the degradation.

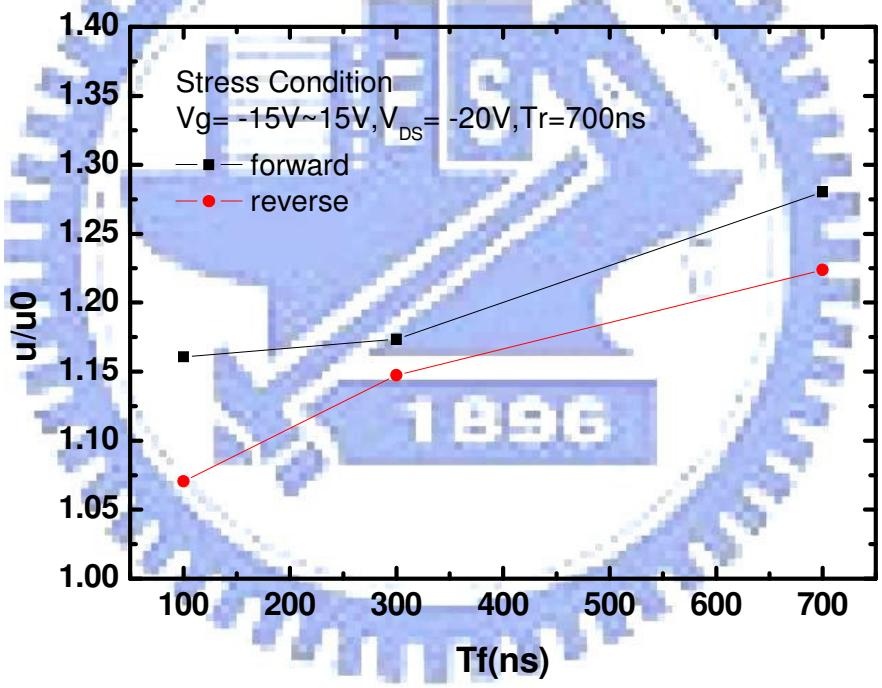


Fig. 5-17 Degradation of μ/μ_0 in P-channel TFT under AC stress with Vg = -15V to 15V measured for various falling times Tf and for Tr = 700ns

Fig. 5-18(a) and 5-18(b) shows the C_{GS} and C_{GD} curves of the devices stressed by various rising time. It is observed the C_{GS} curves and C_{GD} curves rise i the off region after stress. With the rising time Tr increases, C_{GD} curves raise the range more. However, the

degree of C_{GS} curves is less than C_{GD} curves. C_{GS} curves are not obvious changed with increasing the rising time Tr.

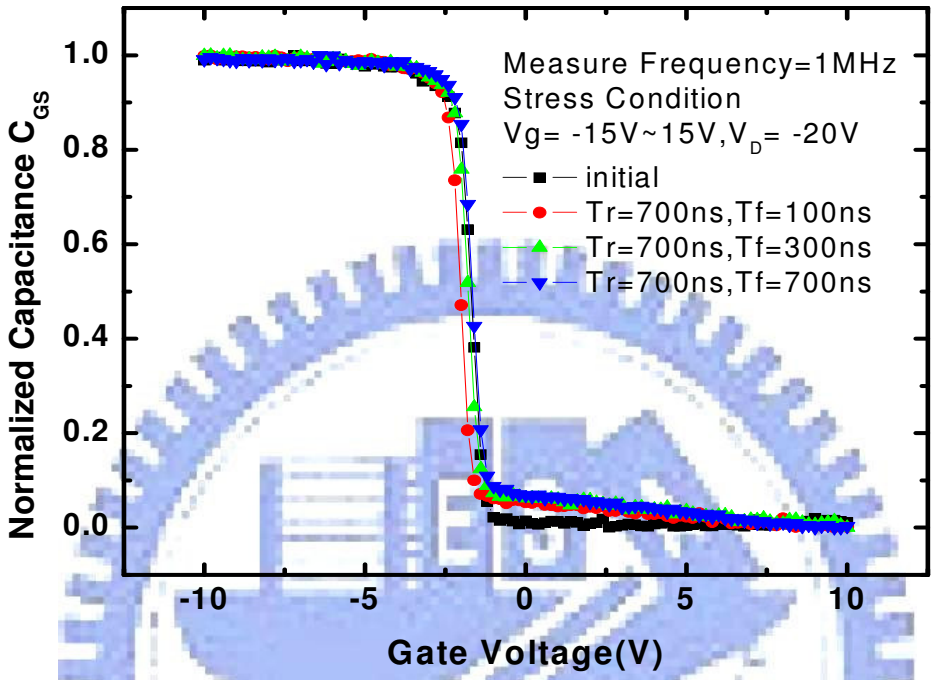


Fig. 5-18(a) Degradation of normalized C_{GS} curve in P-channel under Vg=-15V~15V measured for various Tf and for Tr = 700ns at freq=1MHz

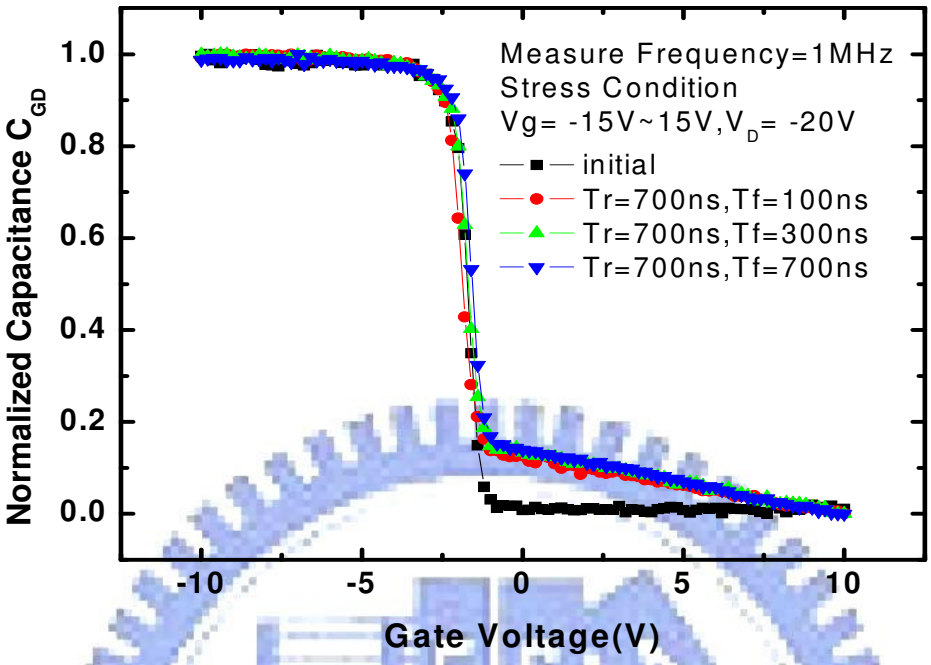


Fig. 5-18(b) Degradation of normalized C_{GD} curve in P-channel under Vg=-15V~15V measured for various Tf and for Tr = 700ns at freq=1MHz

5.3.2.2 Vg in the OFF Region

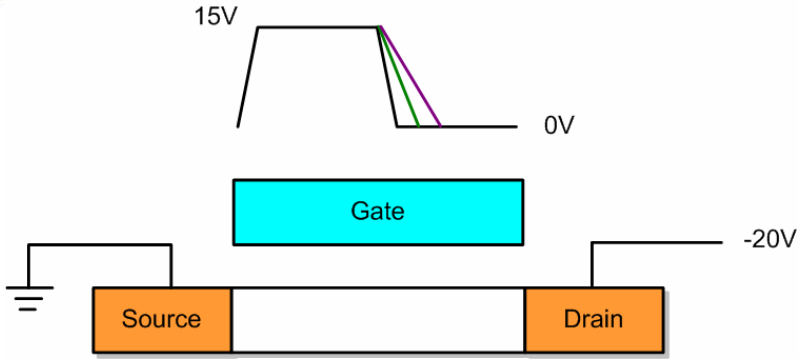


Fig. 5-19 TFT model in P-channel under Vg=0V~15V with changed falling time Tf and fixed Tr

The examination of dependence of the falling time of gate pulse is shown in Fig. 5-19; the device is biased in the off region and drain voltage of -20V. The stress conditions of frequency and stress time are the same as above. There are various stress conditions that

falling time Tf ranging from 100ns to 700ns and fixed rising time Tr of 700ns. After the different stress conditions are applied on the devices, the u/u0 is extracted and shown in Fig. 5-20. As the falling time is 700ns, the stress result would show that the mobility increases slightly. However, if the falling time is set to a value which is higher than the above mentioned, the mobility would degrade seriously. The degree of the degradation between the worst and the most slightly cases shows not much difference. Consequently, the degradation is not related to falling time Tf.

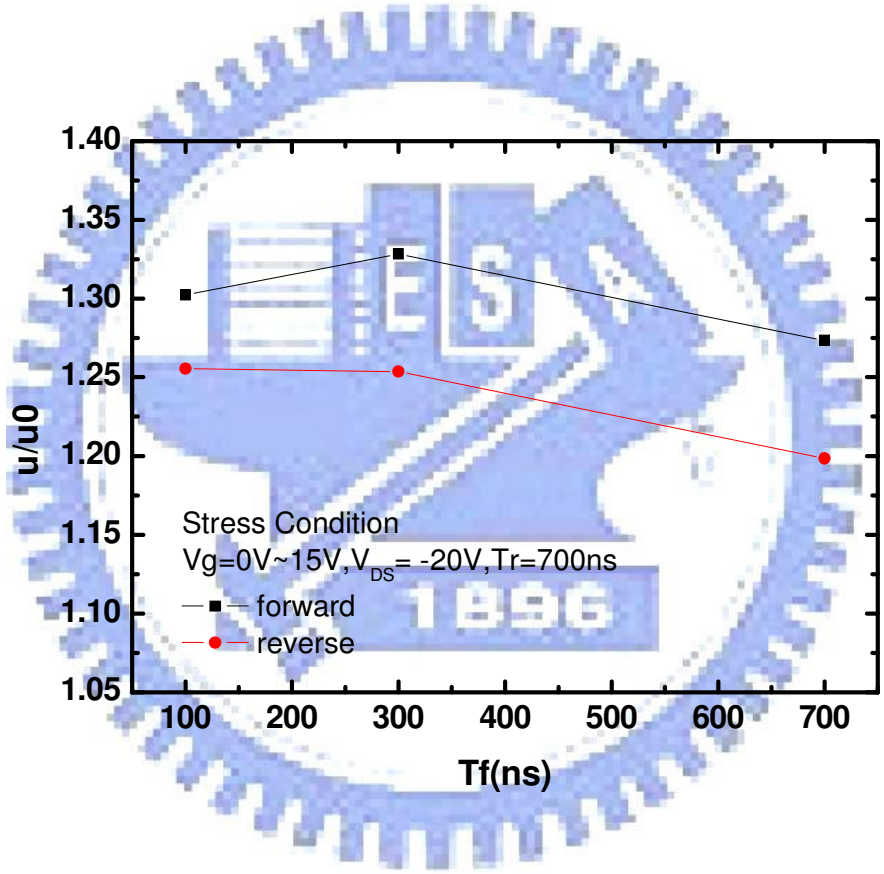


Fig. 5-20 Degradation of μ/μ_0 in P-channel TFT under AC stress with Vg = 0V to 15V measured for various falling times Tf and for Tr = 700ns

Fig. 5-21(a) and 5-21(b) shows the C_{GS} and C_{GD} curves of the devices stressed by various rising time. It is observed the C_{GS} curves and C_{GD} curves rise in the off region after stress. The degree of degradation of C_{GS} curves and C_{GD} curves are not obvious with increasing the rising time Tr.

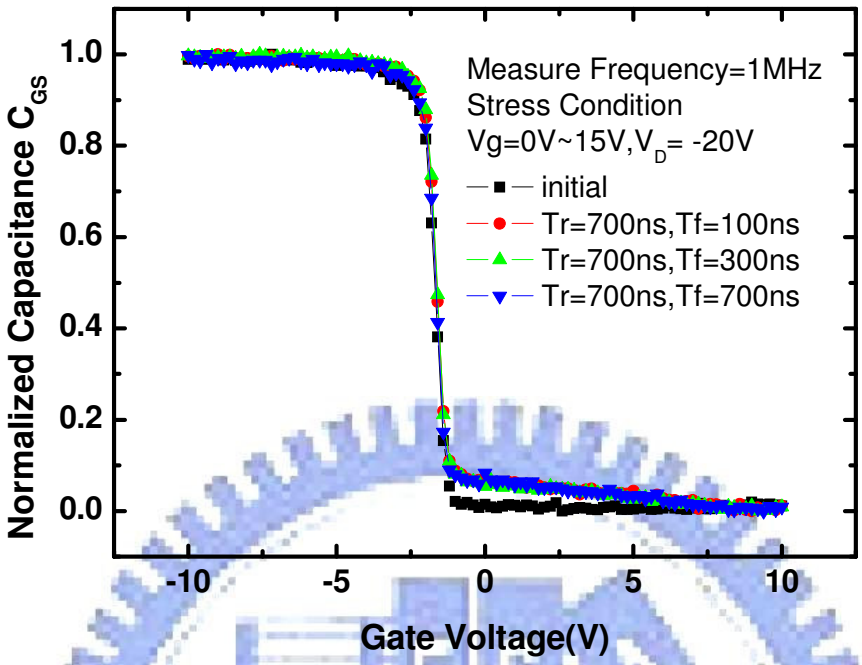


Fig. 5-21(a) Degradation of normalized C_{GS} curve in P-channel under Vg=0V~15V measured for various Tf and for Tr = 700ns at freq=1MHz

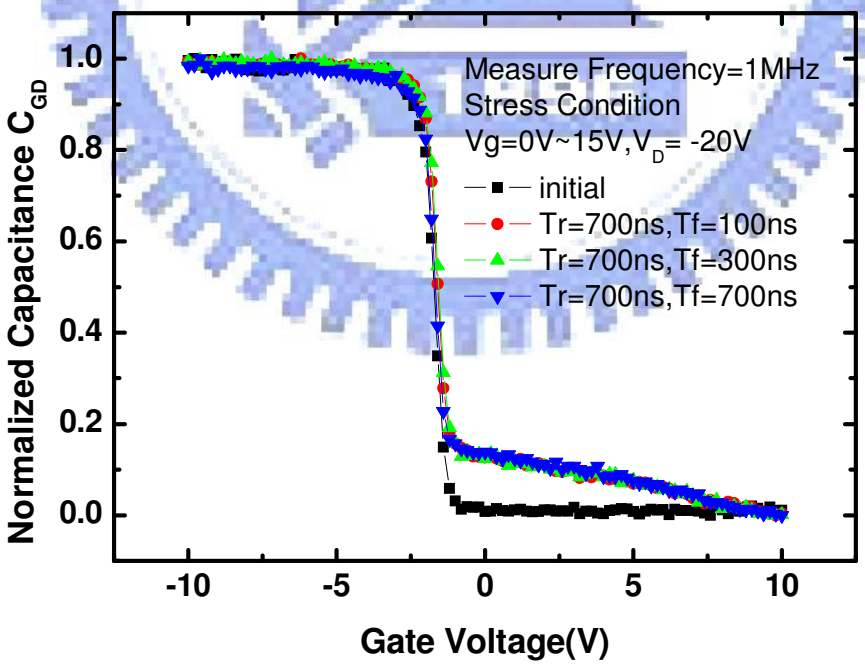


Fig. 5-21(b) Degradation of normalized C_{GD} curve in P-channel under Vg=0V~15V measured for various Tf and for Tr = 700ns at freq=1MHz

5.4 Results and Discussions

The degradation of P-channel TFT devices is due to a different mechanism rather than that of the N-channel TFT devices. The mechanism is triggered by the electrons in the inversion region of the channel that are injected into the gate oxide. The trapped electrons cause the surface of the channel to invert, which effectively extends the p^+ region of the drain into the channel. Fig. 5-22 shows this mechanism and indicates the charged area effectively extending the drain. Extending the drain reduces the effective channel length of the transistor and actually increases the transconductance as a function of the time the device is operated at a high voltage. The mechanism is called hot-electron-induced punchthrough (HEIP). This is the dominant cause of P-channel TFT device degradation.

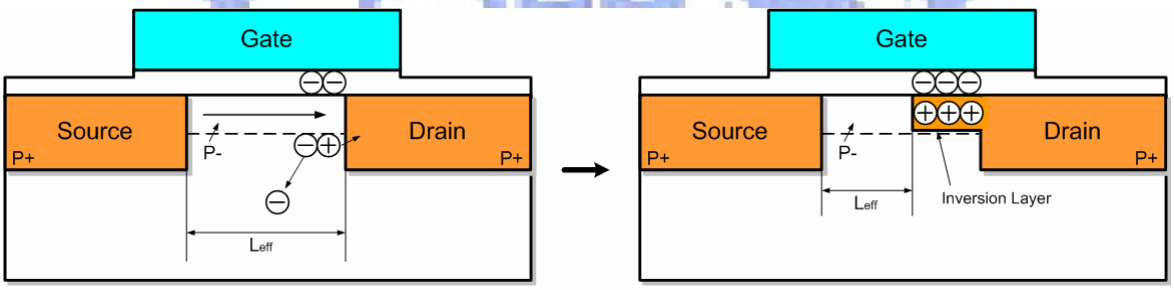


Fig. 5-22 Schematic illustration of the mechanism causing the hot-electron-induced-punchthrough effect

More carriers are induced from channel to the drain region during the stress with the larger drain voltage. These carriers may gain high energy because of the large drain bias and result in impact ionization, causing electron-hole pairs. Generated holes flow to drain and electrons flow to the source or gate direction. However, the generated electrons are so far away from the source. More electrons flow to the gate direction. And, carriers locate in the interface and become charges. Charges near the drain are more than near the source. Thus, the drain region degrades seriously.

Fig. 5-23(a) shows the degradation model of the forward measurement under a large drain voltage. There are interface trapped charges in drain depletion region. These charges make the depletion region extend. Fig. 5-23(b) shows the reverse measurement. Charges could not form the depletion region alone. The mobility in reverse connection increases less. However, C_{GD} curves which are corresponded to the reverse connection in Id-Vg raise more than that in C_{GS} curves which are corresponded to the forward connection. After stress, trap charges would increase and would be near the drain region because of the large V_D during stress, as shown in Fig. 5-24. It is because that the forward mobility and C_{GD} curve degrades seriously.

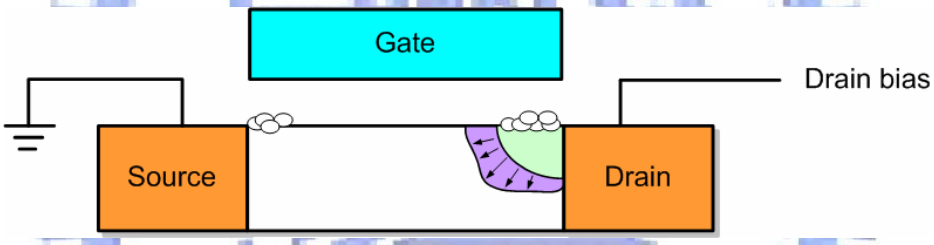


Fig. 5-23(a) The degradation model in the forward Id-Vg measurement

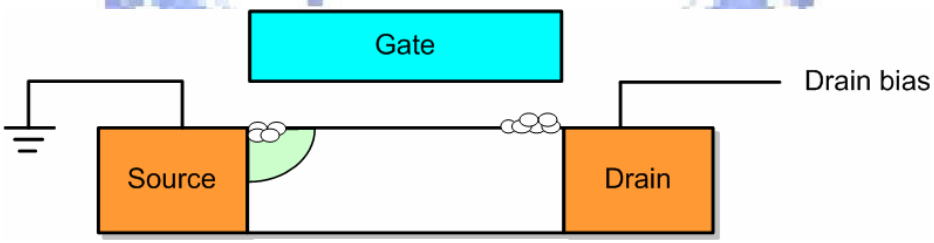


Fig. 5-23(b) The degradation model in the reverse Id-Vg measurement

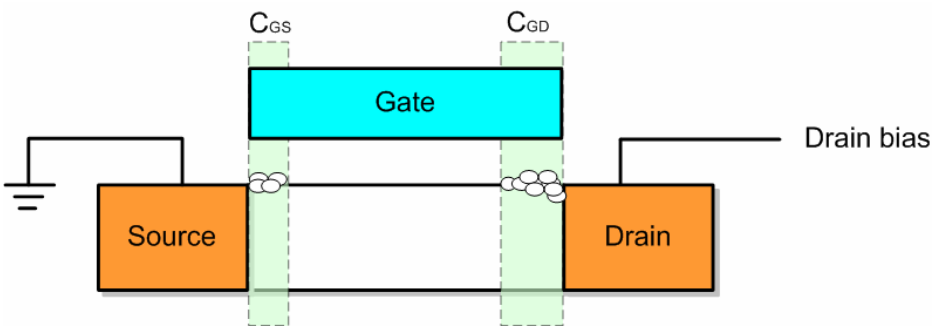


Fig. 5-24 The C-V degradation model under a large drain bias

5.5 Summary

The effect of negative drain bias with the AC gate voltage stressed in the off region of the P-type TFTs is observed in the device parameters. With the higher stress drain bias, the mobility increases and the threshold voltage shift (ΔVth) drifts more. C_{GD} and C_{GS} curves both raise in the off region. For the larger gate voltage range and negative drain bias, the high increase of the mobility is observed.

For the rising time and falling time of gate voltage toggling with on/off or off region, the effect is not obvious. The interfacial trapped charge is found to be responsible for the mobility increase and Cmin raise.

Chapter 6

Conclusions

For the gate voltage toggling between -15V~15V of N-channel TFT devices with source and drain grounded, it is observed that the degradation depends on the falling time Tf but does not depend on the rising time Tr. However, for the gate voltage toggling between -15V~0V, it is observed that the degradation is dependent on both Tr and Tf.

For the stressed Vg=-15V~15V of P-channel TFT devices, it is observed that the degradation depends on the rising time Tr but does not depend on the falling time Tf. The degradation is both independent of Tr and Tf for Vg=0V~15V stressed.

For N-channel TFTs applied with gate AC ranging between ±15V with drain bias, the mobility and sub-threshold swing are influenced on stress V_{DS}. The degradation in the C-V behavior is the stretched-out curves, which correspond to the Id-Vg curves. For the effect of gate voltage range with various drain bias, curves degrade seriously with both increasing Vg range and V_{DS}. As for the effect of rising time and the falling time of the gate voltage, electrons would flow from source to channel and may flow from channel to drain. It would explain turning points.

Nevertheless, for the case of P-channel TFTs, the degradation is not as clear as that in N-channel TFTs. The mobility and the threshold voltage are also influenced on increased drain voltage. The degradation of C-V curves is raised for the lower gate voltage. With both increasing Vg range and V_{DS}, curves would degrade more. Last, with the drain electron given a large voltage, the rising time and falling time dependence of gate pulse would not be clear.

Table 6-1 and Table 6-2 are the relationship of rising time and falling time for N-type TFTs and P-type TFTs.

Table 6-1 Summary statement of rising time and falling time dependence of gate AC signal for N-type

N-type	V_{DS}=0V		V_{DS}=20V	
Vg= -15V~ +15V	Tr	x	Tr	○
	Tf	○	Tf	x
Vg=-15V~ 0V	Tr	○	Tr	x
	Tf	○	Tf	x

Table 6-2 Summary statement of rising time and falling time dependence of gate AC signal for P-type

P-type	V_{DS}=0V		V_{DS}= -20V	
Vg= -15V~ +15V	Tr	○	Tr	x
	Tf	x	Tf	○
Vg=-0V~ 15V	Tr	x	Tr	○
	Tf	x	Tf	x

In this thesis, we have discussed various gate AC stress conditions with both N-channel and P-channel TFTs with biased drain. It would be helpful in the understanding and evaluation of the device degradation mechanism to design for the reliability of poly-Si TFT circuit.

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論文題目：

低溫複晶矽薄膜電晶體在閘極關閉區脈衝電壓及汲極直流偏壓下的劣化研究

Study of LTPS TFTs Degradation under Gate Pulse Stress in OFF Region with Drain Bias