Effect of Back-Gate Bias on Tunneling Leakage in a Gated p^+-n Diode

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***Abstract*—On a thin-oxide gate-controlled p^+-n diode, this work first exhibits experimentally not only the substrate-bias-dependent characteristics of the tunneling leakage current but also the tunneling leakage characteristics independent of the substrate bias. This observation can be reasonably explained by the nature of the modulation of the surface space-charge region over the heavily doped p^+ region as well as over the n-type substrate. Based on this work, the original understanding of such tunneling leakage has been improved.**

I. Introduction

In 1965, Grove and Fitzgerald [1] presented experimentally the back-gate bias dependence of the leakage current through a gated p^+-n diode whose oxide was intentionally contaminated with sodium ions. For such a diode having a highly doped p^+ region, they proposed empirically a tunneling mechanism involved in an induced junction formed between an inversion layer over the p^+ region and the underlying p^+ region. Recently, a new tunneling leakage occurring in the gate-to-drain overlap region for scaled-down thin oxide MOSFET's has been extensively studied [2], [3]. Chang and Lien [2] and Chan *et al.* [3] have shown this leakage current experimentally to be independent of back-gate bias or substrate bias. To interpret this relationship, they together proposed the deep-depletion approximation theory by not forming an inversion layer over the heavily doped region. On a thin-oxide PMOSFET or, equivalently, a thin-oxide gate-controlled p^+-n diode, however, we will present experimentally a new phenomenon that the previous theories [1]-[3] fail to interpret.

II. Experiment

The structure under test consists of 864 gated p^+-n diodes in parallel. Fig. 1 shows the cross section of one such diode where the simulated potential contours are superimposed and will be discussed later. This structure has been fabricated using the conventional n-well CMOS process. The gate oxide thickness is about 250 Å and the total peripheral length is 124 416 μm. The junction depth and surface doping concentration of the p^+ region are about 0.44 μm and 4×10^{19} cm^{-3}, respectively. The temperature measurements have been performed to identify the band-to-band tunneling mechanism responsible for the measured leakage characteristics.

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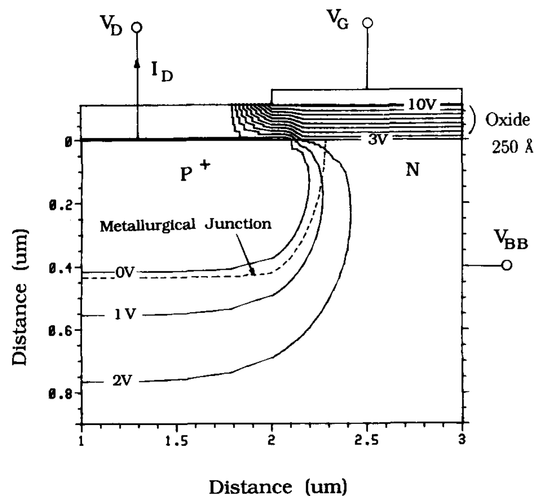

Fig. 1. Cross section of a gate-controlled p^+-n diode. Also shown are the simulated potential contours corresponding to $V_D = 0$ V, $V_G = 10$ V, and $V_{BB} = 2$ V.

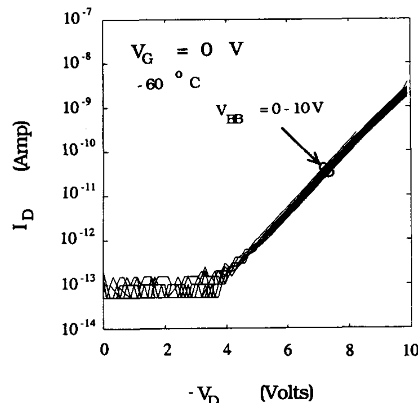

Fig. 2. Measured leakage characteristics at −60°C with back-gate bias ranged from 0 to 10 V in 1-V steps for all the gates grounded.

At −60°C and with all of the gates grounded, Fig. 2 shows the measurement results of the leakage current I_D versus the drain voltage V_D with the back-gate bias V_{BB} as a parameter. From Fig. 2, it can be observed that the leakage current is nearly independent of the back-gate bias. By changing the test condition from the gates grounded to the p^+ regions grounded, however, a great difference in the resulting leakage characteristics occurs. For all of the p^+ regions grounded, Fig. 3 shows the measurement results of the leakage current I_D versus the gate voltage V_G with $V_{BB} = 2$

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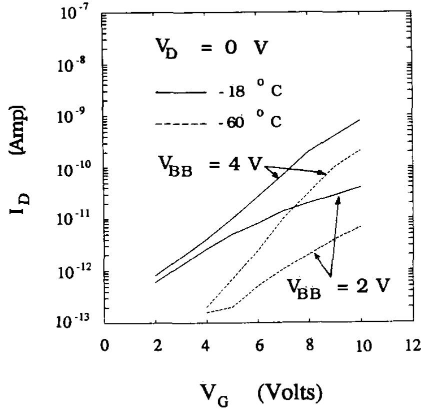

Fig. 3. Measured leakage characteristics at two temperatures of −18 and −60°C with two back-gate biases of 2 and 4 V for all the p^+ regions grounded.

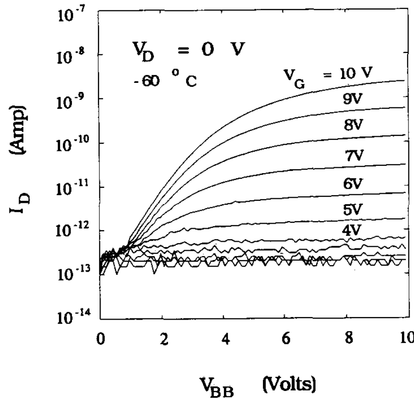

Fig. 4. Measured leakage current versus back-gate bias at −60°C with gate voltage as a parameter for all the p^+ regions grounded. The gate voltage ranges from 0 to 10 V in 1-V steps.

and 4 V for two different temperatures of −18 and −60°C. The corresponding characteristics of the leakage current versus the back-gate bias at −60°C with the gate voltage as a parameter are shown in Fig. 4. The measured leakage current shown in Fig. 3 exhibits a positive temperature coefficient, i.e., the leakage current increases as the temperature increases, indicating the band-to-band tunneling mechanism dominating the measured leakage characteristics in our work. As we increase V_D negatively to a large value (−10 V, for example), we have found a negative temperature coefficient of not only the drain leakage current occurring in the gate–p^+ overlap region but also the gate leakage current through the gate–p^+ overlap oxide, indicating the dominance of the surface avalanche impact ionization [4]. Note that the I_D versus V_G curves for large value of V_{BB} deduced from Fig. 4 are nearly identical to the I_D versus $-V_D$ curves shown in Fig. 2. We can observe from Fig. 4 that for both small values of V_{BB} and large values of V_G the leakage current is modulated over a very large range by the application of a back-gate bias; however, as the V_{BB} value increases, the leakage current tends to saturation and thus becomes considerably independent of the back-gate bias. Therefore, we have shown experimentally both the back-gate bias dependence and the back-gate bias independence of such leakage current. The previous theories [1]–[3] fail to explain this new phenomenon and should be considerably improved.

III. Discussion

To account for the above experimental results, the two-dimensional potential distributions in a gated p^+-n diode as a function of V_G and V_{BB} under $V_D = 0$ V are of concern. Based on the measured doping profile, a two-dimensional device simulator PISCES II-B [5] has been utilized to offer the corresponding potential distributions. Fig. 1 shows such potential contours under $V_G = 10$ V, $V_{BB} = 2$ V, and $V_D = 0$ V. From Fig. 1, it can be clearly observed that the surface of the p^+ region near the corner is inverted. Moreover, the simulation has shown that an increase in V_{BB} can cause a decrease in the regime located by such an inversion layer until the p^+ surface is completely depleted. For example, the inversion region in Fig. 1 completely disappears as V_{BB} exceeds about 5 V. Also, the simulation has shown that the corresponding surface electric field strength near the corner increases and then tends to saturation. Based on this simulation work, we present the following new mechanism in order to better interpret the experimental results.

According to Fig. 1, for the formation of an inversion layer over the p^+ surface, the following two conditions must be satisfied simultaneously:

$$V_G - V_{BB} \geq V_{FB,n} \tag{1}$$

and

$$V_G \geq V_{T,p} \tag{2}$$

where $V_{FB,n}$ is the flat-band voltage for the MOS system on the substrate and $V_{T,p}$ is the threshold voltage to induce an inversion layer near the corner over the p^+ surface. The voltage $V_{T,p}$ can be expressed as [6]

$$V_{T,p} = V_{FB,p} + V_{BB} + \frac{2kT}{q}\ln\frac{N_A}{n_i} + t_{ox}\sqrt{18\frac{1}{\epsilon_s}qN_A\left(\frac{2kT}{q}\ln\frac{N_A}{n_i} + V_{BB} - V_D\right)} \tag{3}$$

where $V_{FB,p}$ is the flat-band voltage for the MOS system on the p^+ region, t_{ox} is the gate oxide thickness, ϵ_s is the silicon permittivity, n_i is the effective intrinsic concentration, and N_A is the position-dependent surface doping concentration of the diffused p^+ region. Note that $V_{T,p}$ is a position-dependent parameter along the surface of the p^+ region. Equation (1) reveals the condition for the accumulation layer appearing over the substrate and (2) gives the condition for the formation of an inversion layer over the p^+ surface. Note that (2) is valid only when (1) has been satisfied. This is because the accumulation layer itself acts as a conductive path via which the back-gate bias V_{BB} is electrically connected to the possibly formed inversion layer over the p^+ region. Therefore, any condition (1) or (2) not satisfied will make the tunneling leakage characteristics independent of the back-gate bias.

The experimental I_D versus V_D curves shown in Fig. 2 can be interpreted by noting that (1) is not satisfied since the measured value of $V_{FB,n}(= 0.3 \text{ V})$ is greater than $(V_G - V_{BB})$. Depending on the values of V_{BB} and V_G, the part of the curves shown in Fig. 4 where the leakage currents are about independent of V_{BB} can be divided into two regimes: the left-side regime, where (1) is satisfied while (2) is not, and the right-side regime, where (1) is not satisfied. Only for the case of small V_{BB} and large V_G values can (1) and (2) be satisfied simultaneously. Under this condition, the p^+ surface near the corner is inverted. The formation of such an inversion layer provides the path for the back-gate bias to reduce the effective electrical field strength, leading to the back-gate bias dependence mentioned above.

IV. Conclusion

This work has demonstrated that for a thin-oxide gated p^+-n diode, not only back-gate bias dependence but also back-gate bias independence of the tunneling leakage current have been observed. The nature of the modulation of the surface space-charge region over each side of the junction has been proposed for this observation.

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