金屬誘發側向結晶複晶矽薄膜電晶體

可靠度課題及元件特性之研究

研究生：洪文強　　指導教授：　林鴻志　博士

黃調元　博士

國立交通大學

電子工程學系　　電子研究所

中文摘要

在本論文中，我們首先利用金屬誘發側向結晶的方式，製作薄膜電晶體的通道層，且整體製程也都符合低溫薄膜電晶體的製作。同時，我們也應用本實驗室所研發的特殊結構，來探討元件的結晶特性以及可靠度。

利用金屬誘發側向結晶來製作複晶矽，其成長有方向性，因此不同區域的成長時間不同，特性也不一樣，利用此特殊結構的四個通道，可以直接由量測電性圖，觀察其不同成長特性，較傳統方法需要剝除通道層以上結構，並拍攝掃描式電子顯微鏡照片方便許多。另外為了進一步改善元件特性，我們也將元件加以氨電漿處理，除了其一般電特性有所改善之外，在閘極氧化層測試時，經過電漿處理後，也有較好的效果。

可靠度量測係在兩種不同偏壓下進行，$V_G=0.5V_D$ 以及 $V_G=V_D$。在 $V_G=0.5V_D$ 偏壓下，利用改變量測電流的新方法，可以偵測到小區塊($10\,\mu m \times 0.2\,\mu m$)熱載子引發的傷害，配合上特殊結構子通道的量測，可以更精準敏感的感測出通道內不同區域的傷害。

在 V_G=V_D 偏壓下，則可能有兩種機制，分別是碰撞電離產生電子電洞對，其電洞注入閘極氧化層，以及閘極氧化層內鍵結不完全的矽原子，在高電壓下，被抽離電子而帶正電，導致臨界電壓(threshold voltage)在高偏壓測試後偏移。

Device Characteristics and Reliability of Metal Induced Laterally Crystallized Polysilicon Thin Film Transistors

Student: Wen-Chiang Hong

Advisors: Dr. Horng-Chih Lin

Dr. Tiao-Yuan Huang

Department of Electronics Engineering & Institute of Electronics

National Chiao-Tung University

Abstract

In this study, we have fabricated a special TFT structure which includes four pairs of channels and analyzed its basic characteristics and reliability issues. The devices are fabricated under low temperature and the active channel was made by metal induced lateral crystallization (MILC). Using the special structure, the channel crystallinity can be monitored by electrical measurement instead of pain-taking scanning electron microscope (SEM) pictures. In order to improve the device performance, the devices were also treated under NH_3 plasma to passivate defects and enhance the quality of devices. In addition, NH_3 plasma also enhances the quality of gate oxide which can resist higher gate voltage stressing.

For reliability study, two kinds of hot-carrier effects were studied. In the first place, we study the stress condition under $V_G=0.5V_D$. In this case, the special structure can provide better sensitivity in localized region of the channel. Furthermore, by changing the current path of measurement we are able to study hot-carrier effect in depth. Our data show that the small

damage region has only edge dimensions of 10 μm/0.2 μm. In the second place, we study the stress condition under V_G=V_D. Threshold voltage shifting and degradation of subthreshold swing are observed in this case. There are two responsible mechanisms. The first mechanism is pertaining to holes which are induced by impact ionization and injected into the gate oxide. The second mechanism is pertaining to electrons being extracted from Si in gate oxide under higher gate voltage.

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洪文強

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Chapter 1

Introduction

1.1 Introduction to Poly-Si Thin-Film Transistors: Trends in the Development

The fabrication of thin-film transistors (TFTs) on an insulating substrate (typically glass) is similar to MOSFETs process on a Si wafer. Process temperature is the biggest difference between TFTs and MOSFETs. While the highest temperature approaches the melting points of Si in the fabrication of MOSFETs, TFTs are usually fabricated at lower temperature owing to the use of glass substrates, and amorphous silicon (α-Si) and poly silicon (poly-Si) are usually employed as the channel materials. Low temperature poly silicon (LTPS) has drawn lots of attention in the fabrication of TFTs. First, poly-Si film as an active layer has much higher mobility than α-Si (<1 cm^2 V^{-1} s^{-1}) film does[1]. As a result, incorporating the integrated peripheral driving circuitry and switching transistors on the same substrate for active-matrix liquid crystal displays (AMLCD's) becomes possible. Second, fabrication at low temperature (less than 600-650℃) allows the use of cheap glass substrate instead of quartz substrate. LTPS reduces the assembly complication and cost dramatically [2]. Moreover, the dimension of poly-Si TFTs can be made smaller compared with that of α-Si TFTs, thus more suitable for high-density, high-resolution AMLCDs. Furthermore, poly-Si TFTs can be applied to the field of memory devices such as dynamic random access memories (DRAMs), static random access memories (SRAMs), electrically erasable programmable

read-only memories (EEPROMs), etc.[1, 2]

1.2 Formation of Polycrystalline Silicon

The quality of active layer affects the performance of TFTs tremendously, and the methods of poly-Si formation affect the quality directly. For this reason, the crystallization process is a very critical step in TFT fabrication process. Depositing poly-Si directly and crystallizing α-Si are two usual ways to attain poly-Si film. Crystallizing α-Si is the main stream because of higher mobility[3]. Solid phase crystallization (SPC), excimer laser crystallization (ELC), and metal induced lateral diffusion (MILC) are the most popular methods to transform α-Si into poly-Si. Followings are brief introduction of them.

1.2.1 Solid Phase Crystallization (SPC)

SPC is a common method to obtain poly-Si from α-Si. Since α-Si is a thermodynamically metastable phase, when α-Si is annealed at a suitable temperature which is high enough to surmount energy barrier, the phase transformation takes place by a thermodynamic driving force.

The precursor α-Si and heating methods affect the resultant poly-Si quality because both of them influence the nucleation rate in α-Si film[1, 4]. For the first factor, increasing disorder in the precursor (e.g., decreasing deposition temperature and increasing deposition rate) can slow the nucleation rate. Larger grain size relates to longer crystallization time, but

the crystallization time corresponding to grain size exceeding 0.5-1 μm is too long to be practical[4]. For the second factor, increasing temperature of SPC can make bigger grain size and lower defect density. However, when the heating temperature is too high, for example, higher than 750℃, the glass substrate cannot be used. As a result, a popular heating temperature in a furnace is around 600℃. These have ranged from a few hours for low temperature chemical vapor deposition (LPCVD) with precursor of SiH_4 at 550℃ to approximately 24h for both LPCVD with precursor of Si_2H_6 films deposited at 470℃ and plasma enhanced chemical vapor deposition (PECVD)[2].

Rapid thermal annealing (RTA) is another method to crystallize α-Si. The poly-Si crystallized by RTA has a smaller grain than poly-Si by furnace annealing, but the defect density is lower and the Hall mobility is higher [5].

1.2.2 Laser Crystallization

Laser crystallization is the most commonly reported technique on LTPS preparation. First, capping a SiO_2 layer on glass substrate can absorb excess heat to protect substrate. After capping an α-Si layer, a laser light source scans and melts the α-Si. After cooling the layer is transformed into poly-Si. The source of laser can be classified into two groups: excimer laser crystallization (ELC) and continuous waver (CW) lateral crystallization (CLC). Both of them

can achieve poly-Si with grain size bigger than the SPC method. Note that the heating process is short and occurs only in the Si layer. Therefore, this approach is compatible with the low temperature requirement while the mobility can be enhanced to several hundred (>200 cm^2 V^{-1} s^{-1})[1]. Especially, laser annealing with some auxiliary methods can produce localized single-crystal silicon (c-Si) which has mobility of 430 cm^2 V^{-1} s^{-1}[6, 7]. Usually, ELC uses XeCl as gas source and operates in pulse mode, at frequencies around 300Hz, with pulse duration in the range of 10-50ns [4]. On the other hand, CLC uses a stable high power diode pumped solid state laser (DPSS) with Nd: YVO4 (671nm) as source.

In ELC methods, melting condition is the key that decides the recrystallization grain size, and it can be divided into three conditions: partially melting, nearly completely melting, and completely melting[1]. As the melting silicon region increases, less nucleation sites are formed, and thus bigger grain size can be attained. However, if the whole film melts, amorphization or microcrystallization occurs, resulting in a very fine grain size [1]. Figure 1-1 is the diagram. After heating the α-Si layer, some grains have to merge and protrusive grain boundaries are formed, as shown in Fig. 1-2.

CLC scans the α-Si films along a specific direction. As a result, grain merging phenomenon encountered in ELC method is unlikely to occur, so a larger grain size can be obtained. Otherwise, grain boundary can be controlled parallel to the scanning direction and the numbers of grain boundary are also reduced. The main disadvantage associated with CLC

is its higher power consumption.

1.2.3 Metal Induced Lateral Crystallization (MILC)

High temperature (~600℃) and small grain size restrict the application of SPC method. Using metal as catalyst can effectively address these issues. Metal can lower the energy barrier of transformation between α-Si and poly-Si. Therefore, the temperature of crystallization can be lower[1]. Metals of different catalytic mechanisms can be classified into two groups. Metals of the first group, such as Al [8], Au [9], Sb[10], form eutectics with Si and the eutectic temperature is often lower than the temperature of crystallization for α-Si. Metals of the second group, such as Ti[11], Pd[12] , Ni[13] , form Si-rich silicides with α-Si that then serve as the nucleation center for crystallization.

There are several factors which affect the choice of metal catalysts in TFTs fabrication process. First the metal-Si reaction temperature must be lower than the temperature that the glass substrates can tolerate, so certain metals like Ti that reacts with Si at high temperature are not suitable. Second, serious contaminations in Si fabrication should be avoided, so several metals like Au and Cu that are known to result in serious contamination cannot be used. Third, some metals like Al form alloys with Si are also unsuitable. Fourth, the metal diffusion speed in α-Si must be sufficiently fast for efficient crystallization. Concerning all

factors stated above, Ni is a suitable metal because of its lower crystallization temperature and high diffusion speed in α-Si. Besides, the dislocation density is expected to be low because the lattice constant between $NiSi_2$ (0.5406nm) and c-Si (0.5430nm) is only 0.44%.

Adding an ultra-thin Ni on Si surface is the first step of MILC. Afterwards, annealing of the wafer at a temperature around 525℃ is applied to induce crystallization. The mechanism of MILC using Ni has two main stages [14]. First, the α-Si which contacts with Ni or contains Ni initially would form a region called metal-induced-crystallization (MIC), as shown in the Fig. 1-3. The grain size in MIC region is very small and lots of grain boundaries are formed. A nickel silicide is formed at the MIC/α-Si interface, the so-called Reactive Grain Boundary (RGB), with the following equation:

$$Ni + \alpha - Si \in Nickel\ Silicide(at\ RGB) \quad (1).$$

RGB is responsible for the Si grain growth in the second stage. The equation (1) will take place when Ni impurities lower the activation energy of the α-Si crystallization.

As Ni diffuses to α-Si region continuously, Si atoms are dissociated from the rear-edge of the nickel silicides RGB and bound to the poly-Si, as indicated in equation (2).

$$Nickel\ Silicide(at\ RGB) \in Ni + poly - Si \quad (2)$$

As the reaction goes through the film, a crystallized region called MILC is formed, as shown in Fig. 1-4. The whole process is sketched in Fig. 1-5.

Many methods are used to incorporate Ni into process. Three techniques are introduced here. In the first technique, physical vapor deposition (PVD) methods; like sputtering and electron-beam evaporation [15, 16], are used to deposit a Ni film on α-Si film directly. In the second technique, ion implantation is employed to put Ni into α-Si film [17]. In the third technique, an aqueous solution of $Ni(NO_3)_2/NH_4OH$ is used for formation of Ni media on α-Si [18].

Annealing temperature is another important factor in MILC process. Direct SPC will be occurred in the α-Si layer when annealing temperature is too high, and disturb the process of MILC [19]. As a result, the grain size will be as small as that of SPC films. At a higher temperature, the incubation time of SPC decreases and MILC will be seriously retarded seriously, as shown in Fig. 1-6. Some groups used pulsed rapid thermal annealing (RTA) to carry out MILC process at higher temperature [19] by taking advantage of the fact that the heating time of each pulse is too short for SPC to take place.

1.2.4 Advantage of MILC

MILC is a modified method of SPC, so it also has advantages of SPC. In comparison with ELA film, MILC film has smoother surfaces, better uniformity, and can take advantage of the batch process in a furnace to improve the throughput. Moreover, the tools used in

MILC process are much cheaper than those in ELA process [20].

Metal contamination is the main problem in MILC techniques. It makes the fabricated devices suffer from severe leakage current, which is directly related to the lateral electrical field in the drain depletion region [14, 15, 21]. Through the implementation of a buffer layer and the design of an asymmetric structure, the leakage issue is improved [15]. Other techniques, such as the use of P as Ni gettering centers [22] and multi-gated structure [21, 23], were also proposed to reduce the leakage.

1.3 Reliability Issues

Performance of TFTs devices improves with increased crystallinity. TFTs formed by ELA, CW-laser lateral crystallization (CLC), and MILC, can have much larger grain size than those formed by conventional SPC and α-Si, so they depict better electrical characteristics such as higher mobility, lower threshold voltage, sharper subthreshold swing. As a result, poly-Si TFTs is expected to be applied to high-performance displays. Besides basic electrical characteristics, reliability is another important factor which affects the feasibility of practical applications. Therefore, careful attention needs to be paid on such issue.[24]

1.3.1 Conventional Reliability Issues in MOSFETs.

Drain avalanche hot carrier (DAHC) and channel hot electron injections (CHEI) are the usual topics which are widely addressed in investigating the hot-carrier effects (HCEs) of MOSFETs. CHEI is generated when electrons are accelerated by lateral electric field across the channel, and gain energy to become hot [25]. The voltage biases around $V_G=V_D$ has been reported to be the optimum condition for CHEI [26, 27]. Unlike CHEI, DAHC is mainly induced by impact ionization which originates from the high electric field near the drain[28, 29]. The generated energetic electrons will then cause avalanche multiplication and substantially increase the amount of energetic carriers. Experiments show the optimum condition to observe DAHC under the biasing conditions of $V_D>V_G>$Threshold voltage. [28, 29] Schematics of CHEI and DAHC are illustrated in Fig. 1-7 (a) and Fig. 1-7 (b), respectively.

The major outcomes of HCE can be roughly classified into the following events. In the first place, hot carriers may be injected into gate dielectric and form fixed charges or oxide traps. In the second place, hot carriers may overcome the barriers at Si/SiO_2 interface to reach the gate and become excess gate leakage current. In the third place, hot carriers may lose their energy at Si/SiO_2 interface, so the property of interface is degraded and interface states (N_{it}) also increases. This will contribute to the performance degradation in field-effect mobility and subthreshold swing.

1.3.2 Reliability Issues in Poly-Si TFTs

In contrast with single-crystal silicon, grain boundaries (GBs) may contribute additional factors for reliability analysis of poly-Si TFTs. The GBs contain dangling bonds and strain bonds which may potentially act as carrier traps. Hot carriers also easily cause damage in GBs and generate more defects and induce electrical degradation. As a result, degradation mechanisms of poly-Si TFTs strongly depend on the granular structure of the channel film which is related to the fabrication method. For example, T. Yoshida, et al[30] reported lower degradation would occur in devices with lower GBs density. And it also reported that directional GBs may affect reliability tremendously. In our study, poly-Si TFTs were fabricated by the MILC method. It was reported that MILC films have directional GBs[31], and it affects reliability[31]. It is also important to analyze spatially the degradation within the transistor because the damage caused by the HCE is non-uniform.

Furthermore, unlike conventional MOSFETs, typically TFTs have no substrate contact, leaving another difficulty for reliability characterization of TFTs. In MOSFETs, measurement of substrate current is an important method to monitor the impact ionization in DAHC[27]. Moreover, in TFTs the damage creation itself may affect the temporal potential distribution during stressing, and therefore subsequent degradation characteristics [32]. This further complicates the local damage mechanisms.

1.4 Motivation of this Study

As mentioned above, poly-Si TFTs with high performance are potential technology in AMLCD's application. In this regard, electronic devices like displays are usually expected to operate for a long period. So it is clear that reliability should be a very essential issue in this application. MILC is a potential method to produce high-performance devices with low cost, so it is worth the reliability characterization. Based on two factors mentioned in Section. 1.3.2, it is desirable to resolve and understand the detailed mechanisms at different portions of the stressed channel. Furthermore, the unique granular structure of the MILC films is also spatially dependent, so it is also desirable to realize the situation of different parts of the channel which are formed in different periods of MILC process. In this work, a special structure called Hot-Carrier TFT (HCTFT) was employed to analyze related issues [33], so it becomes possible to get a clear picture in the reliability issues of MILC TFTs. Besides, the MILC crystallization can be spatially analyzed through HCTFT and other conventional devices.

1.5 Organization of the Thesis

In this study, five chapters are presented to analyze aforementioned issues. In Chapter 1, an overview of poly-Si TFTs and related reliability issues is described. In Chapter 2, the processes of fabrication are introduced and how the devices are measured is also included. In Chapter 3, basic characteristics are presented, including material analysis, electrical characteristics, and post-metal plasma treatment. Different crystallization situation in different period of MILC process is analyzed directly through the electrical method. In Chapter 4,

HCTFT devices are used to analyze related reliability issues. The conditions of different stress biases are related to DAHC and CHEI which are the two major reliability issues in MOSFETs. A new method which can monitor offset region between gate and S/D junction is also addressed. Finally, the summaries, conclusions, and some future work are given in Chapter 7. References are organized and listed at the end of this thesis.

Chapter 2

Device Fabrication and Material Characterization

2.1 Device Fabrication

The top view of the test structure of HCTFT is shown in Fig.2-1. In horizontal direction, HCTFT has one pair of n^+ contacts to form a lateral channel (the test transistor (TT), shown in Fig. 2-2) which is similar to conventional devices. In vertical direction, HCTFT has three pairs of n^+ contacts to form three perpendicular channels (the monitor transistor (MTs), shown in Fig. 2-3) which are used to monitor the local channel details of the TT. A normal gate electrode covers the whole channel and is used for TT and MTs. The three MTs are called D-MT (drain-side MT), C-MT (central MT), and S-MT (source-side MT), respectively, according to their relative position in the channel of the TT.

The main fabrication steps are described in Figs. 2-4~2-7. First, a 100nm-thick thermal oxide was grown in a furnace on six-inch silicon wafers to simulate the glass substrate. Then, a 100nm-thick α-Si were deposited by LPCVD at respective pressure and temperature of 300mtorr and 550℃, and a 100nm-thick oxide subsequently was deposited by PECVD. The oxide layer deposited by PECVD is used as blocking layer which isolates most part of active layer from Ni metal. After patterning the MILC contact windows as shown in Fig. 2-4, the 5nm-thick Ni layer was deposited by PVD. Afterwards, wafers were heated at 550℃ to finish

MILC process. After removing Ni layer and blocking oxide layer, poly-Si layer which was formed by MILC was patterned as active islands. Next, all four pairs of source and drain regions were doped by phosphorus implantation at a dose of $5\times15/cm^2$ and energy of 15keV with the masking of a photo resist layer. Dopant activation was then performed at 600℃ for 24 hours, as shown in Fig. 2-6. After the source/drain formation, a 100nm-thick oxide gate insulator deposited by PECVD and a 150nm-thick TiN gate deposited by PVD were successively formed over the device surface, as shown in Fig. 2-7. Finally, a 500nm-thick oxide passivation layer was placed on all wafers. After patterning contact holes, Al-Si-Cu alloy was deposited by sputtering and patterned to form the metal pads.

In order to perform an in-depth analysis, devices with different dimensions were designed and fabricated. The test structures can be divided into two major categories. Devices of the first group are conventional TFTs with only one pair of source and drain. This group contains many devices with different widths and lengths. Devices of the second group are HCTFTs which have different offsets of MILC open windows (Dc in Fig. 2-1). In addition, HCTFTs having different monitor channels with different widths (W_S, W_M, and W_D in Fig. 2-1), as well as different widths and lengths in TT, were also fabricated. Furthermore, some devices are intentionally designed to contain two D-MTs, so local situation can be analyzed more thoroughly.

2.2 Material Characteristics

The MILC seeding window is a 5 μm×30 μm rectangle. To ensure that the active layer has been effectively crystallized by the MILC method, it is necessary to observe the layer. In this work, optical microscope (OM) was used to observe how the crystallization proceeds. An example is shown in Fig. 2-8, in which the lighter region near the open window is the MILC region. After averaging data of several test regions on the wafer, the total MILC length is estimated to be 43 μm. The variance of the MILC length is small as shown in Fig. 2-9, implying good process uniformity among different dice.

2.3 Measurement Setup

Current-voltage (I-V) characteristics were evaluated by an HP4156A precision semiconductor parameter analyzer. Temperature-regulated hot chuck was used to control the temperature of test environment at a fixed 25℃.

In consideration of special structure of HCTFTs, it is important to clarify how the measurements are executed. As shown in Fig. 2-2, the drain side of TT is located in the side where the MILC window is located. In the case of MTs, the source and drain arrangement are shown in Fig. 2-3.

In normal measurement, gate and drain are positively biased with respective to the source for n-channel TFTs. In order to analyze devices in details, reverse measurements (it's

denoted SDRev in the thesis) that have gate and source positively biased with respective to drain are also executed.

Below are the definitions of electrical parameters in transistors' I-V characteristics. First, threshold voltage has two different ways to extract. In the first method, threshold voltage is the gate voltage where transconductance (Gm) reaches maximum with V_D of 0.1V. Gm is defined as follows:

$$Gm = \frac{\partial I_D}{\partial V_G}|_{V_D=const} \qquad (2\text{-}1)$$

Threshold voltage which is extracted from Gm method is denoted as Vth. In the other method, threshold voltage is defined as the value of V_G at where drain-current (Ids) equals 100nA×L÷W with VD of 0.1V. The extracted value with this method is donated as Vthc.

Subthreshold swing (SS) is calculated from the subthreshold current,

$$SS = \frac{\partial I_G}{\partial \log I_D} \qquad (2\text{-}2).$$

Mobility is extracted from Gm at V_D of 0.1V as follows:

$$Gm = \left(\frac{W}{L}\right)\mu C_{OX}(Vg - Vth)$$

$$\mu = \frac{Gm}{\left(\frac{W}{L}\right)C_{OX}(Vg - Vth)} \qquad (2\text{-}3)$$

Chapter 3

Results and Discussion of Basic Characteristics

3.1 Basic Electrical Characteristics

The device parameters studied in this study are listed in Table 3-1. In this study, all processes were done at low temperature (less than 600 ℃), including the gate oxidation which was performed by PECVD instead of LPCVD. It is expected that the quality of oxide/channel interface and gate oxide is not as good as that in bulk CMOS devices. As a result, post-metal plasma treatments are used to improve the device characteristics. Traditionally hydrogen is commonly used for plasma treatment, although ammonia (NH_3) has also been employed. Diffused hydrogen and nitrogen species have been reported to effectively passivate the dangling bonds, traps, and defects at grain boundaries and oxide/channel interface[34].

Figure 3-1 shows the effects of plasma treatment on subthreshold swing of the transistors contained in HCTFTs. The subthreshold swing is related to deep states which are mainly associated with dangling bonds, and the deep states would be modified in the early period of plasma treatment [35]. The figure indicates that the three MTs depict negligible changes on SS after plasma treatment, and TT shows only a slight enhancement on SS. From the results we can state that the plasma treatment has little effect on the subthreshold characteristics. This

is attributed to the relatively large grain size of the MILC films.

Figure 3-2 shows the effects of plasma treatment on mobility of the four transistors in HCTFTs. The four transistors show similar increase in mobility. The sizes of the three MTs in the BE1-1 split are nominally identical (see Table 3-1), but the mobility of D-MT and S-MT is higher than that of the C-MT both before and after the plasma treatment, as shown in Fig. 3-2. The disparity may come from two possible factors, namely, the local film crystallinity and geometry of the HCTFTs. The first factor may be related to the characteristics of MILC. To confirm this point, reference samples with active channels prepared by SPC method were also fabricated and characterized. The reference samples were fabricated with the same process as the MILC devices except the crystallization step which was performed with SPC treatment in N_2 at 600 for 24 hours. After device fabrication, the SPC samples also received identical plasma treatment. The results of SPC samples are shown in Fig. 3-3. It is clear that the mobility of D-MT and S-MT is still higher than that of C-MT. Since the SPC films should have a spatially uniform grain size distribution throughout the channel, we can infer that the difference in film crystallinity should not be the main factor responsible for the results shown in Fig. 3-2. The other factor is about geometry design of the HCTFT. Note that D-MT and S-MT are near the drain and source side of TT, respectively. The offset between D-MT and drain of TT is only 0.2 μm. When the channel is turned on, the offset region is also inverted. As a result, portion of the current in D-MT may flow and bypass to the drain of TT, so the

effective channel width is actually bigger than the original design. The situation of S-MT is similar. But C-MT is far away from either drain or source of TT, the situation of S-MT and D-MT will not happen in C-MT. As a result, the extraction of mobility of D-MT and C-MT will be overestimated.

Another supportive evidence comes from the electrical characteristics of a unique test device shown in Fig. 3-4 (detailed structural parameters are listed in the attached Table). The structure is denoted as BC1. The device has two monitor transistors, denoted as S-MT-1 and S-MT-2, which have the same dimensions and are arranged side by side and separated by a small offset of 0.6 m. So supposedly the film crystallinity of the channel of the two transistors should have negligible difference. Moreover, the S-MT-1 device has its other side adjacent to the source of the main transistor, similar to the D-MT and S-MT shown in Fig. 2-1. Fig. 3-5 shows the comparison of transfer characteristics of S-MT-1 and S-MT-2 with SPC channel, and the extracted electrical parameters also are shown in the table under the picture. S-MT-1 has higher mobility than S-MT-2, consistent with our former ratiocination.

3.2 Enhancement of Oxide Reliability with Plasma Treatment

In LTPS process, it is not so easy to form high-quality gate insulators as bulk MOSFETs do because of the lower process temperature. For application of liquid crystals displays[1], a high operation voltage of 10 Voltage or higher is used. Assessment of gate oxide reliability is

thus essential. In this study, the effects of plasma treatment with NH_3 on reliability of oxide layer are investigated and discussed.

In a former dissertation [36], TFTs depicted negative threshold voltage shift after applying stress of V_G/V_D=13V/13V for 1000 seconds. It implied that the generation of positive charge is mainly responsible for the degradations. It was explained that such high field (i.e., with an oxide thickness of 35nm, the oxide field~3.7MV/cm) developed in the oxide near the source side may lead to the generation of positive charges in the oxide. The process is illustrated in Fig. 3-6 [36]. This reminds us that, in addition to the HC degradation, attentions should also be paid to the reliability issues associated with high oxide field strength. Next we explore the effect of plasma treatment on the related issues.

Figure 3-7 shows transfer curves of a device without receiving plasma treatment before and after subjecting to a stress test under V_G of 15 V (V_D=V_S=0) for 1000seconds. Gate oxide thickness is 105nm. It is seen that all four transistors contained in the test device depict negative threshold voltage shift as mentioned above, although the oxide field is relatively low (estimated to be around 1.5MV/cm). In this study the oxide was deposited by PECVD, and the oxide quality is expected to be inferior to the LPCVD-deposited oxide layer employed in the previous work [35]. As a result, the defect generation rate is higher.

After plasma treatment, Vth of the test device decreases by 2V. To maintain the same stressing field across oxide, the stress voltage V_G is decreased to 13V. The results for the

device receiving plasma treatment before and after the stress for 1000secondes are shown in Fig. 3-8. It is clear that the degradation caused by the stress becomes negligible. This implies that the oxide quality has been fortified.

To investigate the effect of high oxide field, a higher V_G of 30V is applied to the device, and the results are shown in Fig. 3-9 and 3-10. In this case, the voltage drops from channel to gate is quite large. Although the gate oxide breakdown didn't occur, electrons injected from channel to gate can attain high enough energy to become hot. As a result, these electrons may damage the oxide if they release their energy inside the oxide film. When this happened, devices would suffer damage events such as electron trapping and interface-state generation, resulting in Vth increase. The situation is depicted in Fig. 3-9, showing the occurrence during the first 1000 sec of stressing, As the stress period is sufficiently long, (e.g., 2000sec in Fig.3-10), TFTs depict negative threshold voltage shift similar to what was observed is the previous work [35].

3.3 Spatially Resolving the Electrical Characteristics of MILC Devices

As mentioned in Section 1.2.3, MILC process starts from MIC region. As a result, crystallization process in different parts of channel occurs at different time. In other words, the channel crystallinity of monitor transistors may depend on the distance of the channel to

the Ni seeding window, as shown in Fig. 3-11, as well as the MILC time. In Figs. 3-11 and 3-12, points A and C represent the positions of D-MT and S-MT, respectively. This means that D-MT receives the MILC treatment earlier than the S-MT does. It should be noted that, although at 550℃ the growth rate of SPC is very slow, it still occurs and may dominate the crystallization process as the film location is far away from the seeding window [37]. Moreover, because of needle-like grain growth in MILC process, some regions far from Ni seeding window are unlikely to form MILC poly-Si. This could be understood with the aid of Fig. 3.12, in which in the regions around point C the situation may occur. . The direct way to verify this phenomenon is to take scanning electron microscope (SEM) picture on the channel surface after removing all films above the channel. It is an effective, albeit a little complex method.

The novel HCTFT structure developed in our group presents another way to probe the location-dependent MILC characteristics. For this purpose, the three types of HCTFT structures, namely, BE1-1, BE1-2, and BE1-3, with their structural parameters listed in Table 3-1, are employed. The three structures have the same dimensions except the distant between Ni seeding window and the channel edge of the D-MT (Dc). The longest length in the channels to the Ni seeding windows (i.e., the distance between the left edge of the source of the test transistor and the right edge of the seeding window, see Fig. 2-1), is 26.4μm, 34.4μm, and 42.4μm for BE1-1, BE1-2, and BE1-3, respectively, as tabulated in Table 3-1. Based on

Fig. 2-9, the shortest MILC length on the wafer is about 42.5μm. This means that the whole channel should be transformed into poly-Si by the MILC process. But as mentioned above, there would be SPC granular structure inside the MILC channel, especially in regions which are farther from the seeding window. As a result, BE1-3 is expected to show the worst electrical characteristics among the three splits since its channel contains the region with the longest distance from seeding window.

The measured results are shown in Fig.13. Fig. 3-13(a) is the characteristics of the TTs, where we can see that BE1-3 has the lowest on-current and the worst SS, as expected. In Fig. 3-13(b), the characteristics of the D-MTs are shown, and the differences among the three I-V curves are not significant. Fig. 3-13(d) shows the characteristics of the C-MTs. We can see that among the three devices, BE1-3 shows the worst performance. In Fig. 3-13(c) the characteristics of the S-MTs are shown. Obviously, the electrical characteristics of the S-MT depend on its distance to the seeding window: the farter, the worse. Table 3-2 summarizes the main performance parameters of the results shown in Fig.3-13. It is seen that the TT and D-MT of BE1-3 have the smallest mobility, the biggest Vth, and the worst SS.

As mentioned above, the D-MT in an HC-TFT is the closest to the seeding window so its channel is crystallized in the starting period of MILC. As a result, the SPC is unlikely to happen. This explains the small difference in the characteristics shown in Fig. 3-13(b). However, the C-MT and S-MT are farther away from the window, so the difference in

channel crystallization reflects on the electrical performance shown in Fig. 13(c) and (d). Since the TT of HCTFTs covers the whole channel region, dramatic differences in characteristics are also observed.

The direct evidence comes from SEM pictures. Figure 3-14, Fig. 3-15, and Fig. 3-16 are SEM pictures taken on the channel regions of D-MTs, C-MTs, and S-MTs, respectively. Before the inspection, the samples were treated in a Secco solution in order to elucidate the grain structure. In order to distinguish SPC grains from MILC grains, a typical SPC picture is shown in Fig. 3-17 as reference[38]. The grain structures are similar in the D-MT regions of BE1-1, BE1-2, and BE1-3, as shown in Fig. 3-14. Fig.3-15 shows the results of the C-MT regions of the test structures. The C-MT of BE1-3 has lots of SPC grains (circled in Fig. 3-15 (c)), while the C-MT of BE1-2 has less amount of SPC grains (circled in Fig. 3-15 (b)). On the contrary, C-MT of BE1-1 has few SPC grains, as shown in Fig. 3-15 (a). When it comes to the region of the S-MTs which are located far away from MILC seeding windows, the differences of crystallization condition of three devices become very obvious. Both the S-MTs of BE1-2 and BE1-3 have lots of SPC grains, while the S-MT of BE1-1 still has few SPC grains. These SEM pictures provide supportive evidences for the location-dependent electrical performance of the HCTFTs shown in Fig. 3-13.

Chapter 4

Investigations of Hot-carrier Degradations Using a Novel Test Structure

4.1 Damage Characteristics under Drain Avalanche Hot Carrier (DAHC) Stress

4.1.1 DAHC under Low Stress Bias

As described in a previous dissertation [36], HCTFTs with SPC channel have the capability of spatially resolving the reliability issue. In this study, the case of HCTFTs having 100nm PECVD oxide and channel formed by MILC method are analyzed. In order to be consistent with former stress condition [36], Stress condition of $V_G=0.5V_D$ is chosen. Before and after applying a hot-carrier stress with V_G/V_D=10V/20V for 1000seconds, the subthreshold characteristics of TT in device BE1-1 (Table 3-1) are shown in Fig. 4-1. As presented in Fig. 4-1(a), the device depicts degradation of SS and decrement of on-current after the stress. The degradation is much severe under V_D=0.1V than V_D=5V. This result is consistent with the well-known facts that the main damage region occurs near the drain side of the channel [36]. Hot-carrier stressing could induce extra interface states and/or

grain-boundary defects[39], and form a defect-rich and resistive region near the drain side of the channel[40]. Under higher V_D bias, the damage region near the drain is effectively screened out by an increase in the depletion region. Compared with Fig. 4-1(a), the results measured under the reverse mode (the source and drain biases are exchanged, denoted as SDRev) measurement are shown in Fig. 4-1(b). We can see that a high V_D of 5V (applied to the source) does not screen the damage region as the normal mode does. It is evident that the regions near the source side have little damage by the HC stressing.

The situation also can be illustrated in Fig. 4-2. Damage induced by hot carriers near the drain side can cause a potential energy hump as shown in Fig. 4-2(a). A high drain bias tends to modify the band diagram as that shown in Fig. 4-2(b) and the energy barrier is lowered, so the degradation in current-voltage characteristics is screened out. If the high bias is applied to the source, the situation changes to that shown in Fig. 4-2(c). As a result, the carriers still have to overcome the energy hump during transport, so the degradation is still presented. As has been demonstrated in the previous dissertation [36], the MTs contained in the HCTFT can show detailed degradation evolution and the associated mechanisms occurring at different parts of the channel. The results of MTs in the present case are shown in Fig. 4-3. In the three MTs, D-MT in Fig. 4-3(a) shows the most serious degradation. Not only decrement of on-current but also SS degradation is presented in D-MT. Moreover, the cases of V_D=0.1V and V_D=5V are similar condition at both case of measurement of normal and reverse bias, so

the resulted damage in the channel of the D-MT should be uniform instead of concentrating in any regions. In the C-MT, the damage induced by hot carriers is much smaller, and no visible damage seems to occur in S-MT. To summarize the above results, the unique design of the HCTFT can easily identify the major damage location.

4.1.2 DAHC under High Stress Bias

By increasing the stress voltage, the degradation worsens. Before and after applying V_G/V_D=15V/30V for 100 and 1000seconds, the electrical characteristics of TT are shown in Fig. 4-4. The on-current degradation is much bigger than that under the former case with V_G/V_D=10V/ 20V (Fig. 4-1), and the degradation of SS is significant. Screening effect by the high drain voltage is also seen. The characterization results of MTs are shown in Fig. 4-5. Again C-MT and S-MT show negligible differences between the initial and the post-stressed characteristics. D-MT still indicates degradation of SS, but the on-current degradation is obviously lighter than that shown in TT (Fig. 4-4). Moreover, on-current degradation in TT is significant during the stress period from 100 to 1000 seconds, but it shows little change in D-MT during the same period. As a result, the major damage locations in the channel can not be clearly revealed through the MTs.

In this section, we would propose a new method to locate the damage region precisely. In the BE1-1 Device, an offset region is located between the channel of D-MT and drain of TT.

The region is supposed to have the highest electrical field when the device is stressed, so it is presumed to be the main damage region. Unfortunately, as shown in Fig. 4-6, the D-MT can not sense this region since the channel of D-MT doesn't contain this area. Even if the current flows to these regions as mentioned in the section 3.1, these current would reduce dramatically when the offset region has high resistivity due to stress. The new method is to change the current path of measurement, as shown in Fig. 4-7. Taking "Short D" mode as an example, the drain bias is applied to the drain of TT while the source bias is applied to one of the junctions of the D-MT, and the measurement configurations of the other modes are shown in the figure. Executing this method can sense the damage result in the offset region. The results of "Short D" are shown in Fig. 4-8. A large on-current degradation occurs in Short D just as what is observed in the TT. Moreover, Short D shows the evolution of degradation in the time period from 100 seconds to 1000 seconds. It even shows more severe on-current degradation than the TT does, indicating that in the measurement the current conduction flows through the major damage region.

Other evidences are shown in Fig. 4-9. The current paths of Long D and Long S are similar to the path of TT except for the offset region, so their fresh electrical characteristics are alike, as shown in Fig. 4-9(a). After applying V_G/V_D=15V/30V for 100 and 1000 seconds, Long S maintains its original characteristics since the current wouldn't flow through offset region near the drain side. Long D and TT show similar current degradation at V_D =0.1V

because the two modes have the current flow through the damaged offset region. When a high drain bias is applied, the damaged region is effectively screened with the results shown in Fig. 4-9(b). Results of reverse modes of measurements are shown in Figs. 4-9(c) and (d) at V_D =0.1V and 5V, respectively. Since the aforementioned screening effect could be lifted with such measurement configuration, significant degradation could be seen in the transfer curves of TT and short-D regardless of the drain bias applied. Based on the above observation, it clearly reveals that the main damage region is indeed located in the offset region with edge dimensions of 10 μm/0.2 μm.

A previously proposed model used to explain the on-current degradation of the test devices is the generation of a large amount of negative charges in the damage region after the stress [30]. The change in SS of Short D is small, so the generation of interface traps between the gate oxide and the poly-Si body or the generation of gate oxide fixed charges is not the dominant factor in the offset region. Instead, a possible model to explain these results is the presence of a potential barrier at the damage site due to excessive amount of electron trapping at the GBs [30]. This implies that during the stress the hot carriers tend to damage the GBs in this site and generate a large amount of trapping sites at the GBs. As a result, a hot-carrier-induced resistance (R_I) is introduced in the offset region. Using a similar technique used in [30] to extract the channel resistance and the results are shown in Fig. 4-10. It can be seen that R_I of TT and Short D values show exponential decay with the increase in V_G after

stress of 1000sec, which imply lowering of a potential barrier. R_I also decreases when V_D increases. The above situations can be explained in Fig. 4-11. Both increments of V_G and V_D decrease the potential barrier induced by hot-carriers. The high value of R_I also means that the grain structure in the offset region near the drain suffers serious damage.

Besides, the different degradation situations observed in D-MT and Short D in the period from stress time 100 seconds to 1000 seconds are consistent. In the initial 100 seconds of stressing, the damage would take place both in the D-MT channel and offset region. But after 100 sec, the degradation is likely to occur solely in the offset region. Based on the simulation results [41, 42], the distribution of lateral field in the channel would change with stress time due to the modification of channel potential by the generated defects. As more band-tail acceptor-type states and interface states are generated, the electrical field would concentrate more near the drain, as shown in Fig. 4-12. As a result, the local electrical field strength increases with increasing stress time and further worsens the situation. In addition, the damage region would move closer to drain in the latter period of the $V_G=0.5V_D$ stress. The simulations[41, 42] also pointed out that the generation of interface states only couldn't account for the on-current degradation. Only when both band-tail acceptor-type states and interface states are considered could the experimental data be justified, so the negative charge trapped in the acceptor-type band-tail states in grain boundaries should be the main reason for on-current degradation, as proposed in a previous reference [30].

In D-MT, the on-current degradation is small, but the degradation of SS is the dominant event, and the damage is done in the initial period (Fig. 4-5). This is because the strength of the local electrical field in the channel region of the D-MT decreases with increasing stress time due to the generation of band-tail acceptor-type states and interface states, and the generation of additional defects in the region is limited. The degradation of SS suggests that interface states are dominant in the D-MT region, but the small on-current degradation suggests that a small amount of band-tail acceptor-type states is formed. On the contrary, the offset region near the drain side, where a higher electrical field, compared with that of the channel of D-MT exists, shows severe on-current degradation. This indicates that a large amount of band-tail acceptor-type states are generated during the entire stress period. The whole picture of this HCE is illustrated in Fig. 4-13.

Fig. 4-14 shows the shift in on-current (ΔIon) and threshold voltage (ΔVth), respectively, as a function of stress V_D with V_G=0.5V_D for 1000 seconds. The definitions of ΔIon and ΔVth are defined in the following equations.

$$\Delta I_{on}(\%) = \frac{I_{on,stress} - I_{on,fresh}}{I_{on,fresh}} \qquad (4.1)$$

(Ion is measured at V_G=10V and V_D=0.1V)

$$\Delta Vth(V) = Vth_{stress} - Vth_{fresh} \qquad (4.2)$$

When V_D is less than 20 volts, both D-MT and Short D much severe on-current degradation than TT does, as shown in Fig.4-14 (a). In this area, D-MT and Short D can

detect details of the main damage in the drain side of TT. When V_D is higher than 20 volts, the major damage site shifts to the offset region near the drain and the D-MT fails to faithfully indicate the situation of degradation, but with the help of Short D measurement, the damage characteristics in the offset region could still be probed.

In Fig. 4-14 (b), Vth increase due to device degradation also indicates that the Short D depicts the most apparent change. To Sum up, Short D has a high sensitivity to reveal stress damage under the $V_G=0.5V_D$ stress. Moreover, the main advantage of the Short D measurement technique is the ability to detect the situation in the offset region. In corporation with the measurement of D-MT, it can reveal the local details in the channel through electrical characteristics directly.

4.2 Damage Characteristics under High Gate- and Drain-Voltage Stress

The subthreshold characteristics of a tester before and after stress at V_G/V_D=30V/30V for 100 and 1000 seconds, are shown in Fig. 4-15. For the first 100 seconds, TT reveals little information about the degradation. D-MT has degradation of SS. A shift in the electrical characteristics occurs in S-MT, while C-MT remains almost unchanged. After stressing for 1000 seconds, only the S-MT shows visible shift in the electrical characteristics with respect to characteristics after stressing 100 seconds. To analyze the degradation further, time

evolution of SS and Vth are shown in Fig. 4-16. During the stress the four transistors show degradation in SS, especially in the D-MT, as shown in Fig. 4-16 (a). In MOSFETs, the stress condition with high and equal V_G and V_D usually causes CHEI, and it doesn't cause serious impact ionization. But in poly-Si TFTs, the presence of granular structure in the poly-Si contains a lot of weak bonds. As a result generation of additional defects caused by the breaking of these weak bonds due to the impact of energetic electrons together with the generated interface states would affect the subthreshold swing. .

Vth shift of the four transistors is shown as a function of stress time in Fig. 4-16 (b). In the figure the S-MT shows the biggest negative shift. This implies that some holes are injected into and trapped in the gate oxide. The source of holes needs to be confirmed. Figure 4-17 shows changes in threshold voltage of TT and MTs after 1000 seconds stress at V_G of 30 V and various V_D. It can be seen clearly that the shift of threshold voltage in ST only occurs at V_D=30 V. Under such high drain bias, the occurrence of impact ionization is possible. Holes induced from impact ionization may flow toward the source owing to the grounded bias, and some holes with sufficiently high energy may overcome barrier between the channel and oxide, and will be injected and trapped in the oxide, as shown in Fig. 4-18. As result, threshold voltage shifts negatively in S-MT. Figure 4-19 shows the drain current of the S-MTs as a function of the stress time. It clearly shows that a higher drain current is resulted under a higher drain bias. Note that the hole trapping caused by the channel hole injection is not the

only origin for the negative Vth shift. As mentioned in Section 3.1.2, similar negative threshold voltage shift in S-MT also occurs when a gate bias of 30V is applied, albeit a long stress time (about 2000 seconds) is needed.

Chapter 5

Conclusions and Future Prospects

5.1 Conclusion

In this study, we have studied the special devices called HCTFTs which were fabricated with MILC methods under low temperature (LTPS TFTs). In Chapter 2, in order to give the basic background of this study, we introduce the process flow and present material analysis and measurement condition.

In Chapter 3, HCTFTs is used to analyze the crystalline conditions of MILC. In conventional methods of analyzing the crystallization, we have to handle devices with various steps to remove films above channels and use Secco solution to display the grain structure, followed by taking SEM pictures which are not only expensive but also cumbersome. In this study, measuring the four pairs of channels in HCTFTs allows us to analyze the different crystalline situations in different positions of channel only by the basic electrical characteristics, which is much easier and quicker. Compared with the SEM results, our methods can reveal the real situation which is consistent with SEM pictures.

Because of low temperature process, the quality of oxide in TFTs is not as good as that in bulk COMS. The effects of plasma treatment on gate oxide are also studied in Chapter 3. High

gate voltage stress was used to test the oxide. After plasma treatment, the negative Vth shift occurs at higher gate voltage than the counterparts without plasma treatment. This indicates that plasma treatment can enhance the quality of oxide in our devices.

In Chapter 4, two types of stresses were studied. The first case is $V_G=0.5V_D$ which is related to DAHC stress. Under lower stress bias, four channels of HCTFTs can reveal clear and in-depth information than the traditional measurements. This method has high sensitivity to damage and the capability of resolving the damage characteristics in different parts of channel. Under higher stress bias, a new method which changed the path of measure current was proposed and demonstrated. With this new method, we can sense the details in an offset region which only has dimensions of 10 μm/0.2 μm. Furthermore, combining this new method with original measurement of four monitor channels in HCTFTs can help us to realize the situation of damage in different parts of channel in different periods of stress.

The second case is $V_G=V_D$ which is related to CHEI stress. The damage is also studied in different parts of channel during different stress period. In this case, two degradation mechanisms are responsible for the negative threshold voltage shift detected by the monitor transistors. Unlike CHEI in CMOS, impact ionization also takes part in this stress condition.

5.2 Future Prospects

5.2.1 Hot-carrier Degradation in the Films of Different Crystallizations

In this study, we only applied stress voltage on the drain side of test transistors which is near MILC seeding windows. And only BE1-1 which has the nearest MILC seeding windows is studied. By applying stress voltage on source side of test transistor and studying BE1-2 and BE1-3 can help us to understand the relationship between crystallization of MILC process and degradation situation.

5.2.2 Hot-carrier Degradation in P-channel TFTs

It has been shown that hot-carrier degradation in p-channel TFTs is different from that in n-channel TFTs[43-45]. In this study, only n-channel TFTs are included. Therefore, further study on p-channel is necessary for us to understand the hot-carrier effects.

5.2.3 Hot-carrier Degradation in AC Stressing Modes

In former dissertation[36], AC stressing modes shows different degradation situation in TFTs formed by SPC methods from DC stressing modes. Furthermore, most circuits are operated under AC bias instead of DC bias. Since the trend of building circuits on panels is

future trend, studying hot-carrier degradation in AC stressing modes is an important issue.

Figures

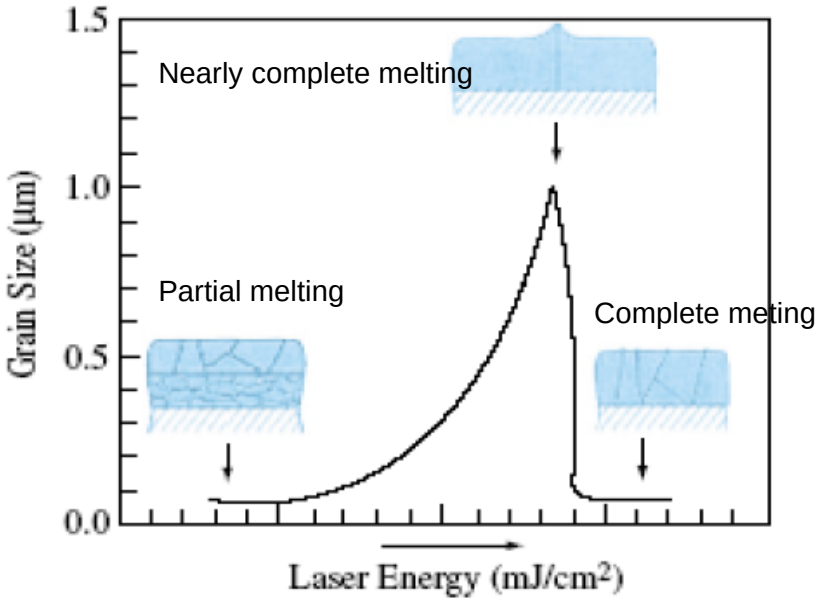


Fig. 1-1 Three condition of grain size which different laser energy can induce[46]

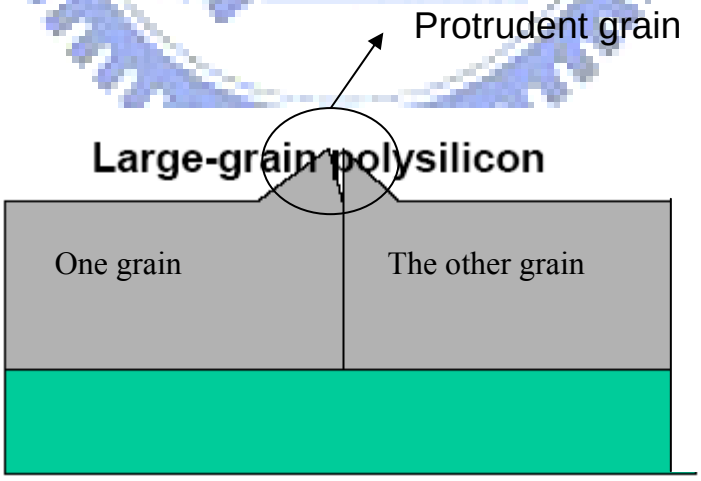


Fig. 1-2 Protrudent grains formed when grains merged [46]

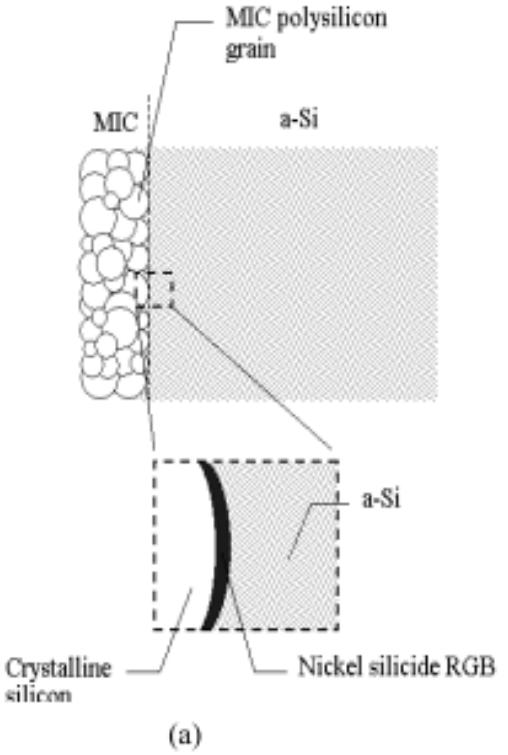


Fig. 1-3 MIC region formed at first stage of MILC process. [14]

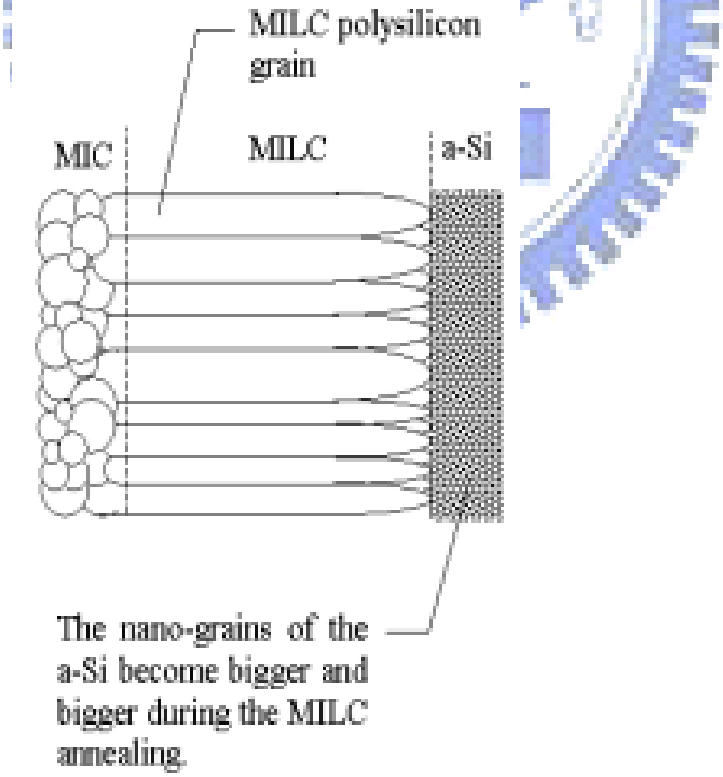


Fig. 1-4 MILC region formed after the reaction goes through the films[14]

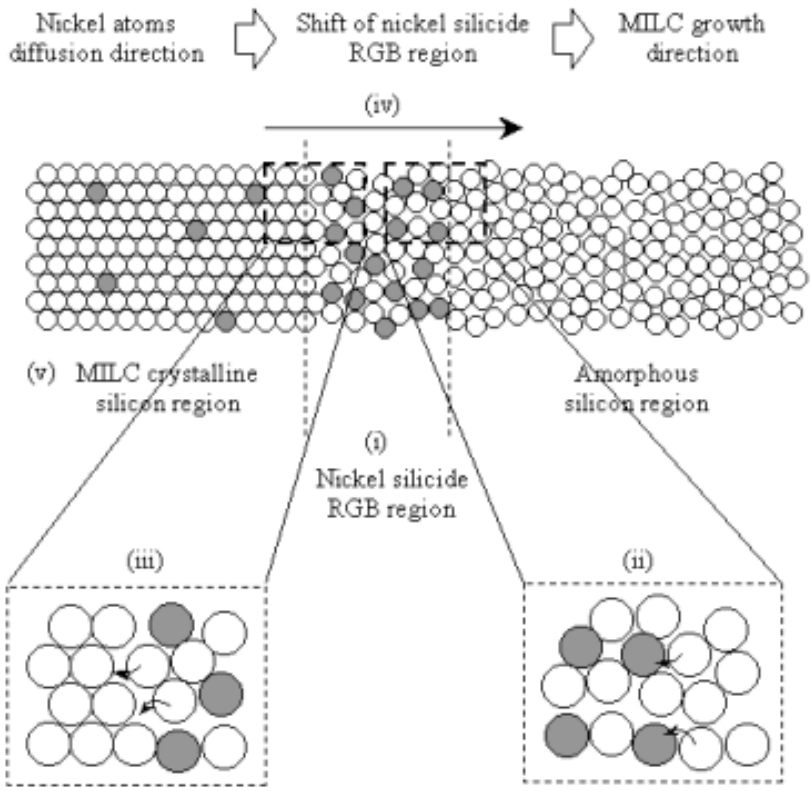


Fig. 1-5 The whole picture of MILC process [14]

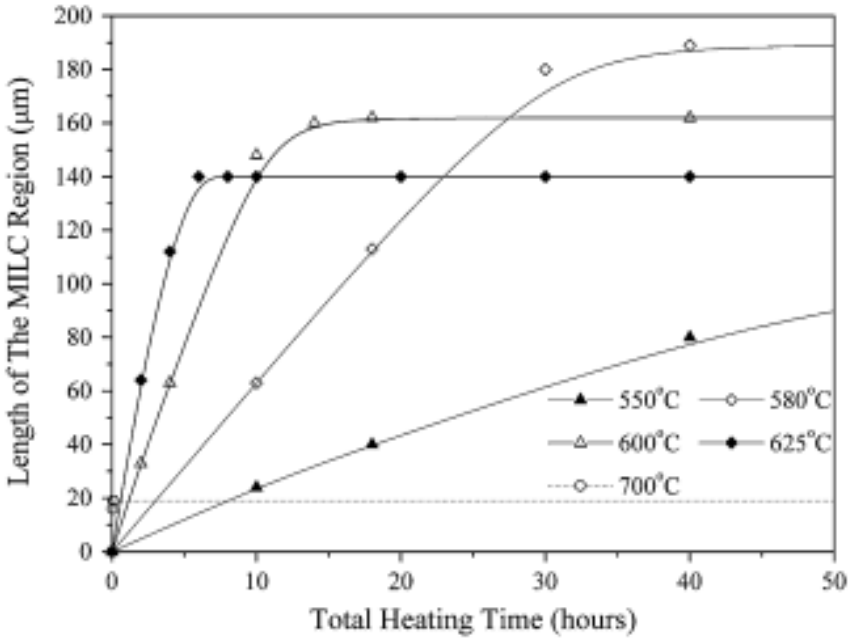
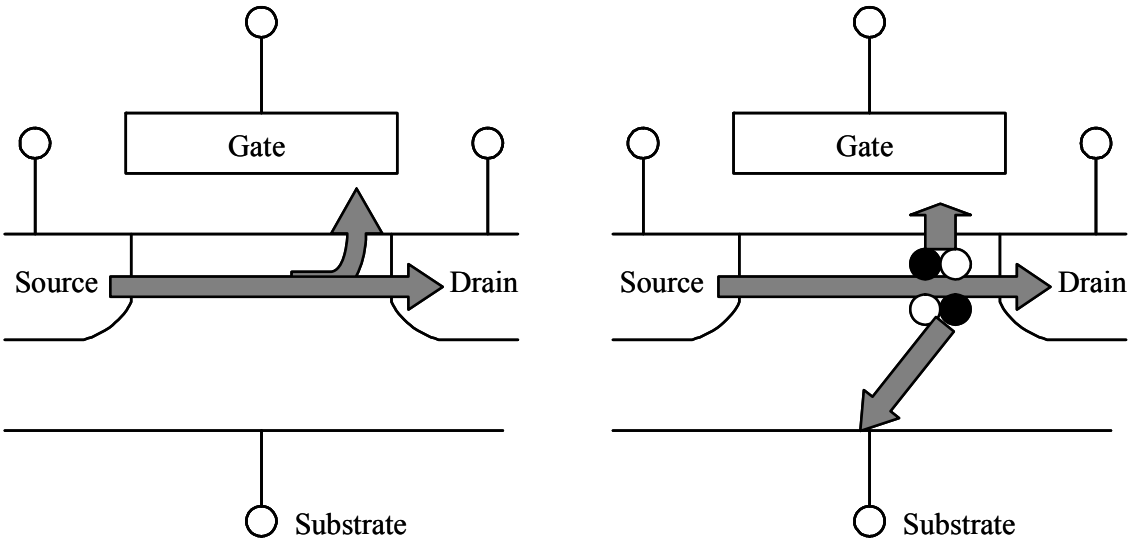


Fig. 1-6 The temperature and time dependence of the length of MILC Region[19].



(a) (b)

Fig. 1-7 Schematic illustration of (a) CHEI and (b) DAHC in hot-carrier generation.

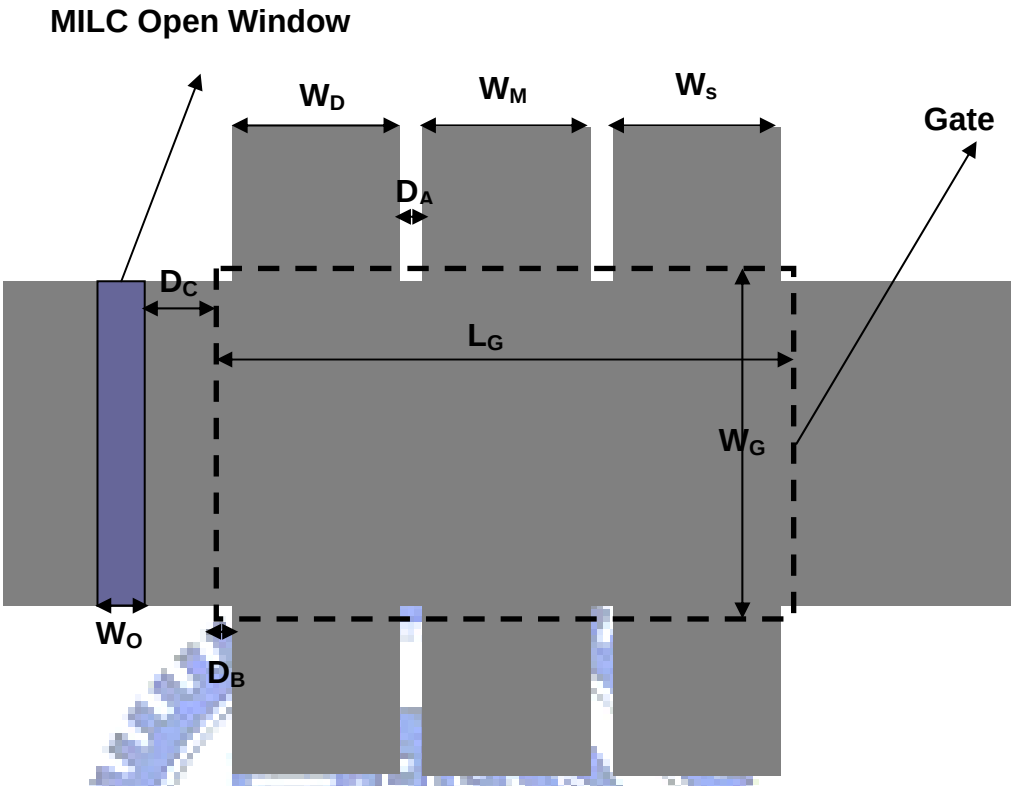


Fig. 2-1 Top view of HCTFT devices

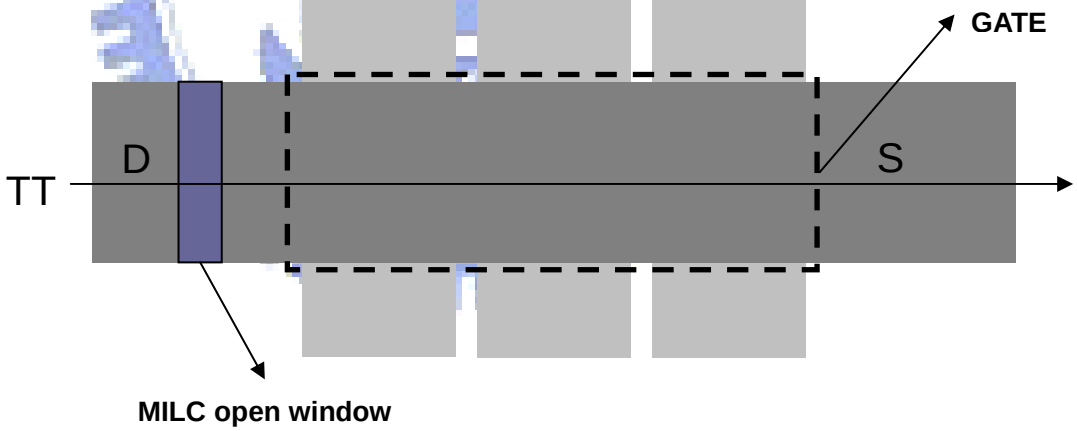


Fig. 2-2 The definition of test transistor (TT)

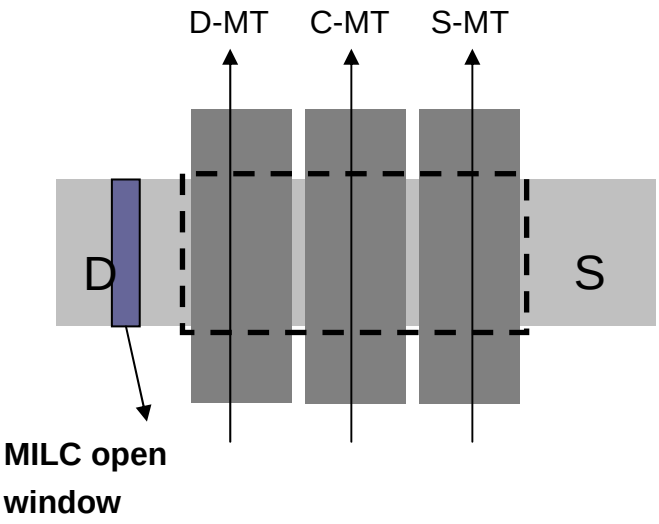


Fig. 2-3 The definition of monitor transistors (MTs)

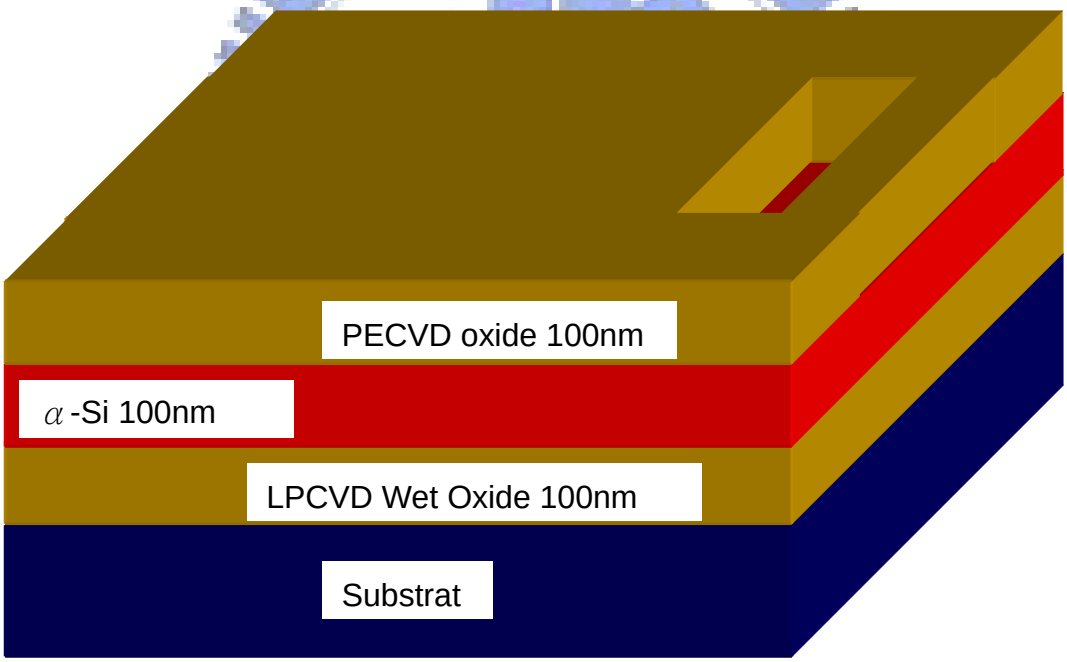


Fig. 2-4 Device process: MILC seeding window

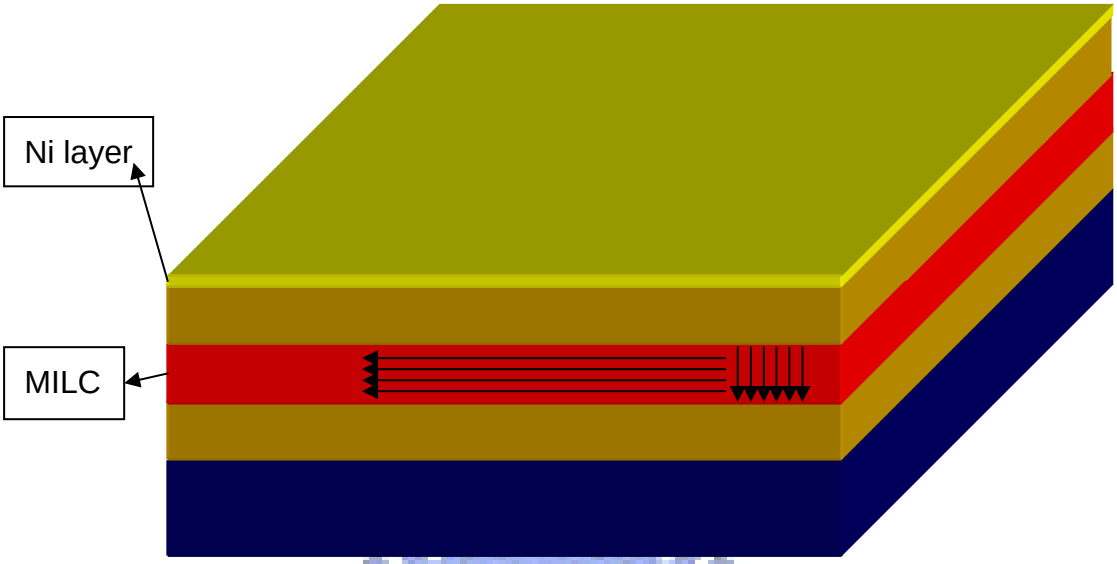


Fig. 2-5 Device process: wafer is heated at 550℃ for MILC process

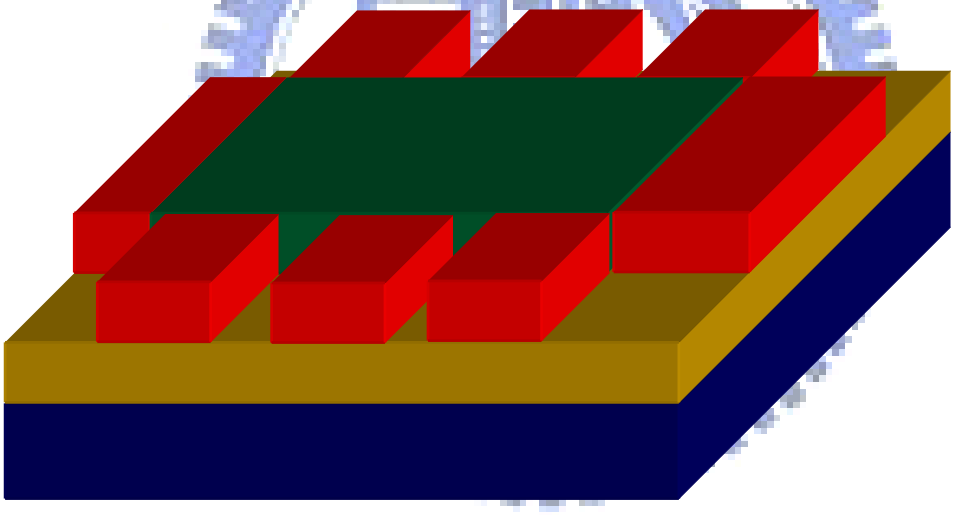


Fig. 2-6 Device process: channel formation, dopant implantation, and dopant activation

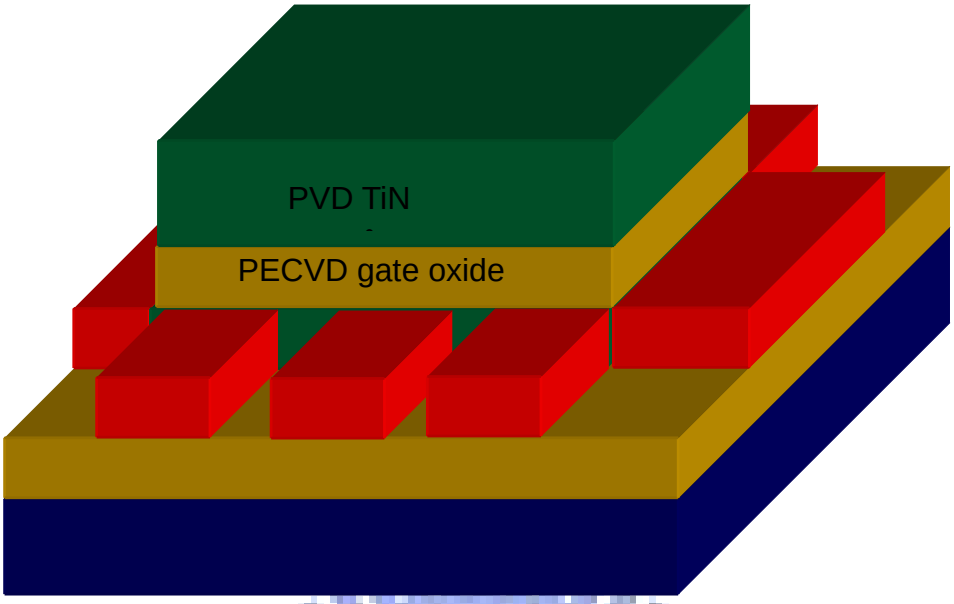


Fig. 2-7 Device process: gate oxide and gate deposition

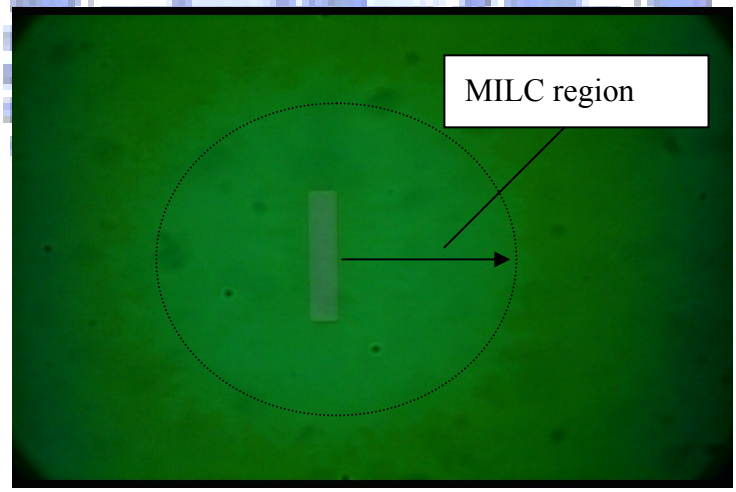


Fig. 2-8 A photo of the MILC region under OM.

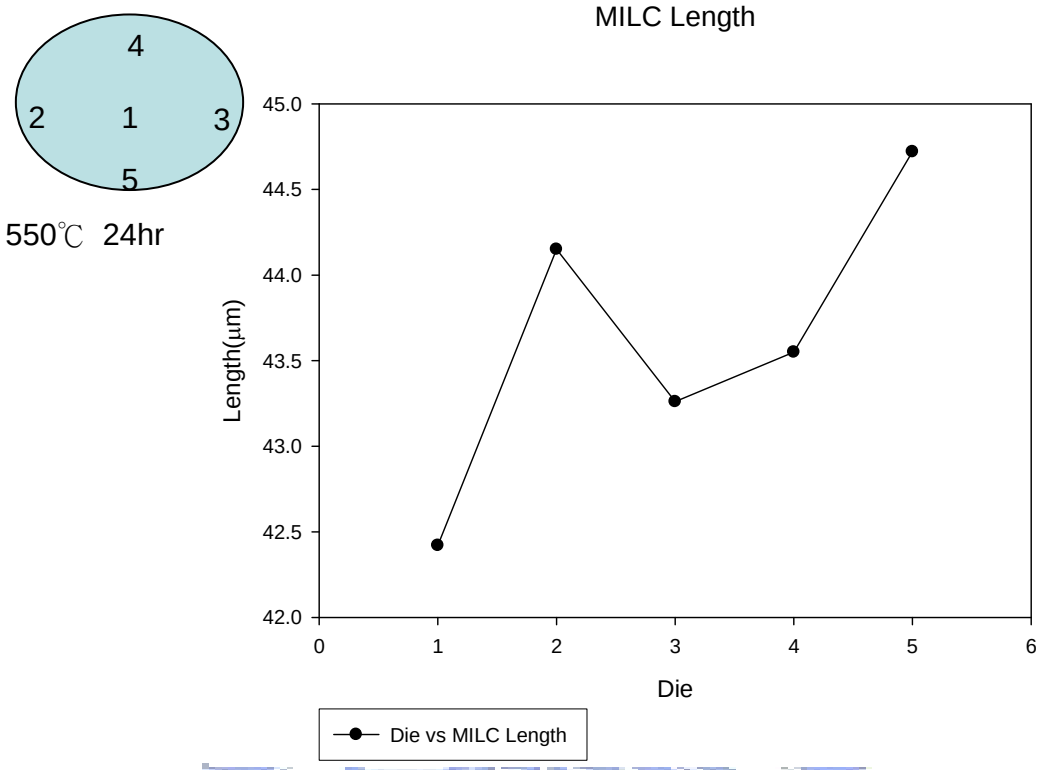


Fig. 2-9 Analysis of MILC length

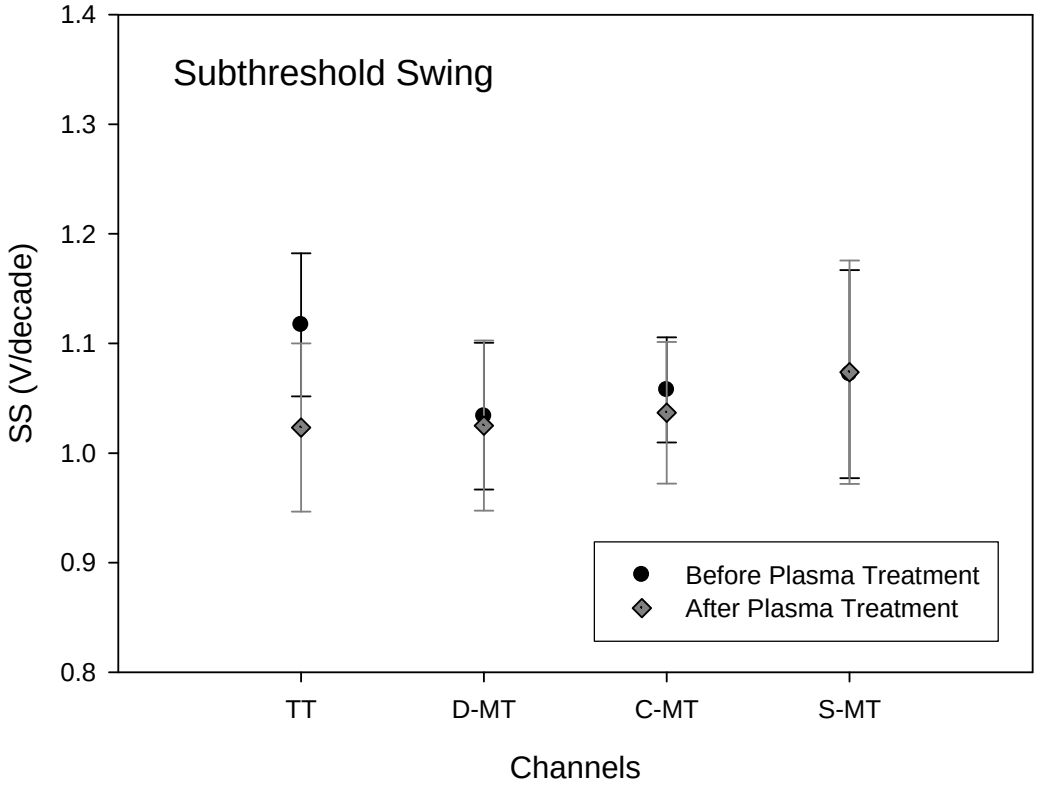
Table 3-1 Parameters of different devices

BE1 series: Splits of three devices with different offset

(All units are in micro meter, μm)

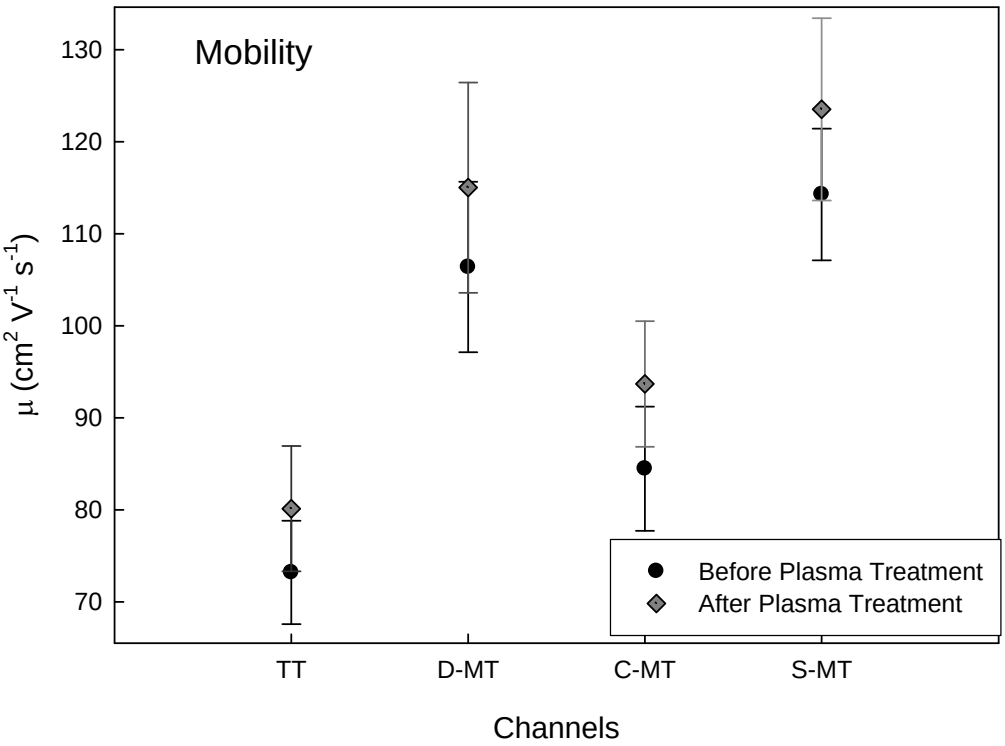
Denotation	L_G	W_G	W_S	W_M	W_D	W_O	D_A	D_B	D_C
BE1-1	21.4	10	5	5	5	5	3	0.2	5
BE1-2	21.4	10	5	5	5	5	3	0.2	13
BE1-3	21.4	10	5	5	5	5	3	0.2	21

(Details about the structural parameters can be found in Fig. 2-1. D_C represents the offset length between the seeding window and the channel region.)



Mean value of SS (V/decade)	TT	D-MT	C-MT	S-MT
Before Plasma treatment	1.117	1.034	1.058	1.072
After Plasma treatment	1.023	1.025	1.037	1.074
Delta Value	-0.094	-0.009	-0.021	0.002
%	-8.390	-0.838	-1.978	0.160

Fig. 3-1 Mean subthreshold swing of the four transistors in BE1-1 devices fabricated by MILC method.



Mean value of Mobility ($cm^2V^{-1}S^{-1}$)	TT	D-MT	C-MT	S-MT
Before Plasma treatment	73.20	106.39	84.47	114.27
After Plasma treatment	80.13	115.02	93.68	123.52
Delta Value	6.93	8.63	9.21	9.25
%	9.46	8.11	10.90	8.09

Fig. 3-2 Mean mobility of the four transistors in BE1-1 devices fabricated by MILC method.

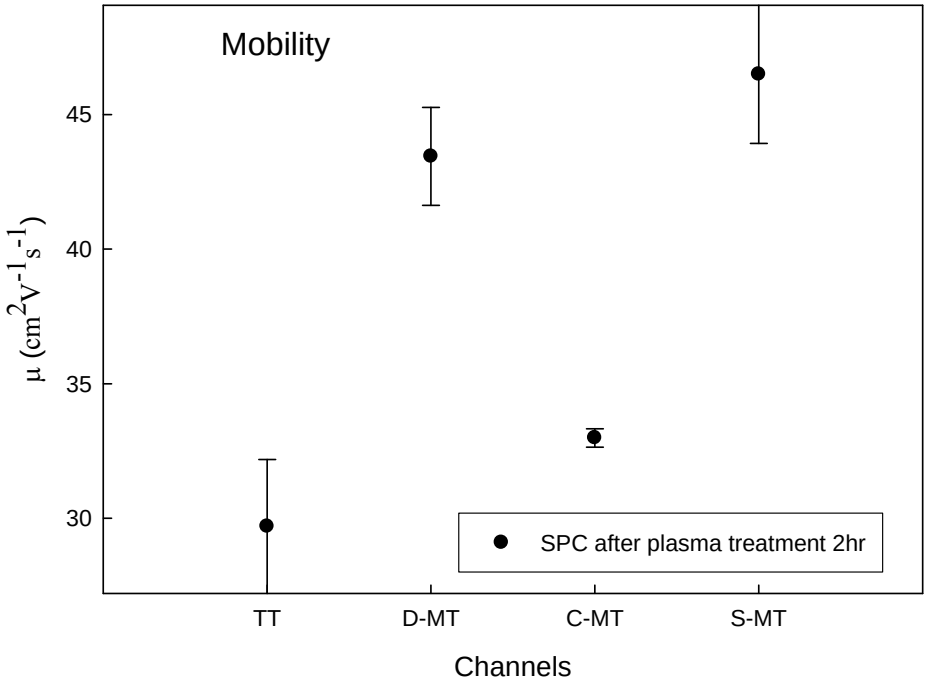
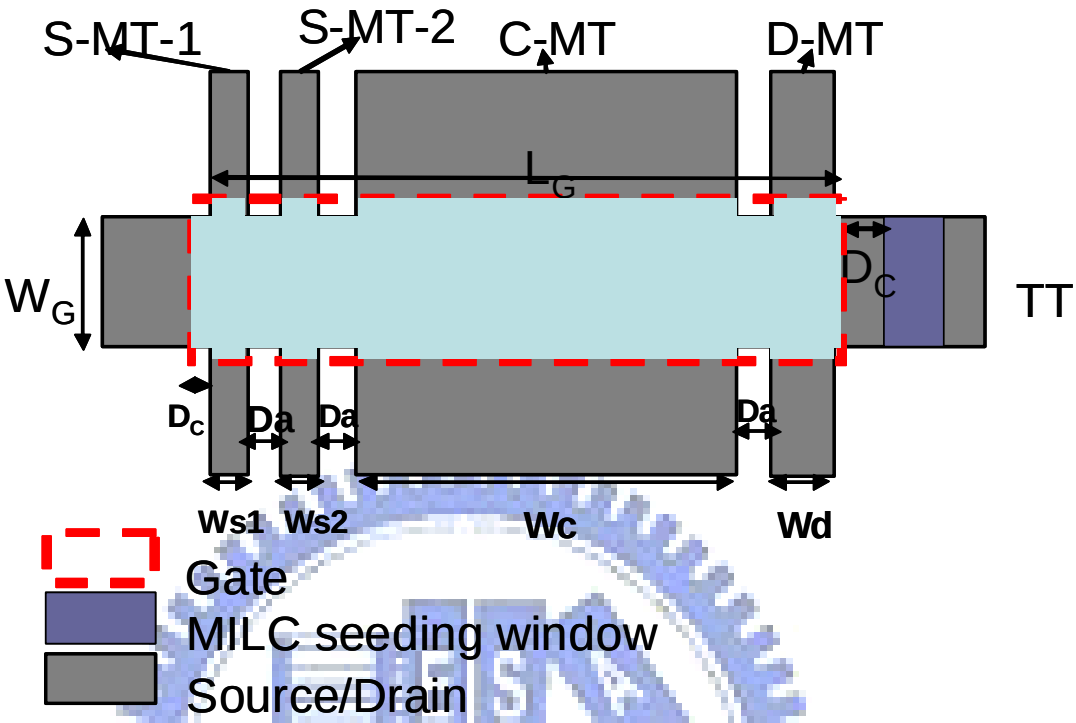


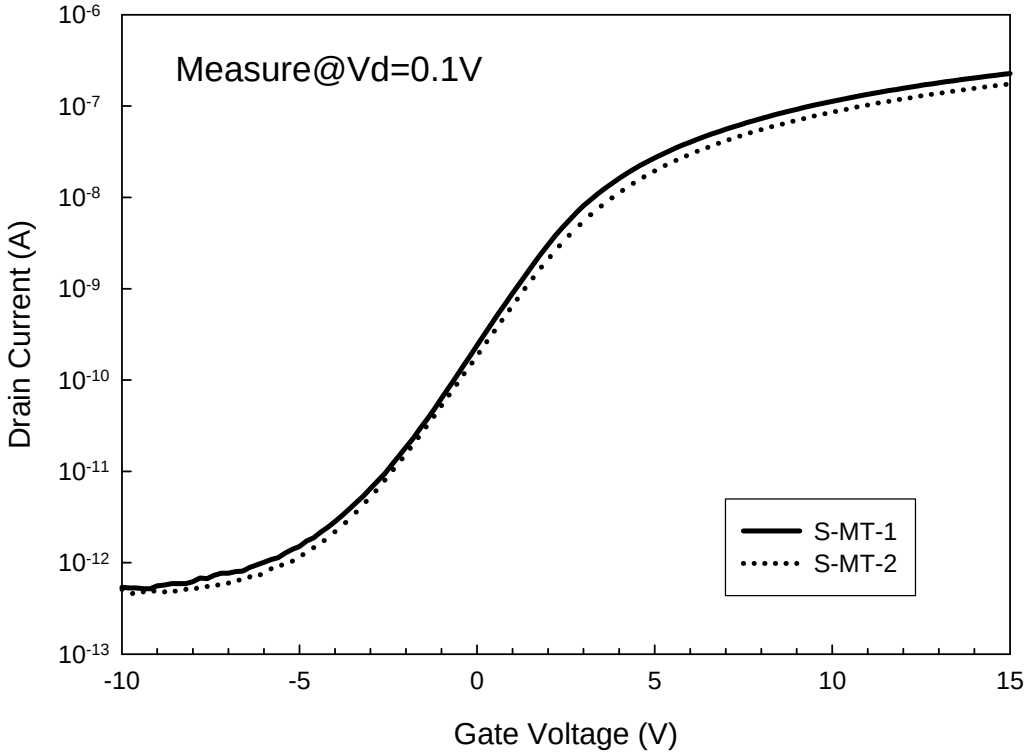
Fig. 3-3 Mobility of the four transistors in BE1-1 devices fabricated by SPC method.



Denotation	L_G	W_G	W_{S1}	W_{S2}	W_C	W_d	D_a	D_B	D_C
BC1	10.4	7	0.6	0.6	6	1	0.6	0.2	6.2

(unit: μm)

Fig. 3-4Top view of the test structure which has two monitor transistors, S-MT-1 and S-MT-2, near source side of the TT.



	mobility($cm^2V^{-1}s^{-1}$)	VTH(V)	SS(V/decade)	Ion(A)
S-MT-1	65.22	5.92	1.732	2.27E-07
S-MT-2	52.98	6.49	1.823	1.74E-07

Fig. 3-5 Comparisons of transfer characteristics and mobility of S-MT-1 and S-MT-2 in the BC1 devices fabricated by SPC method.

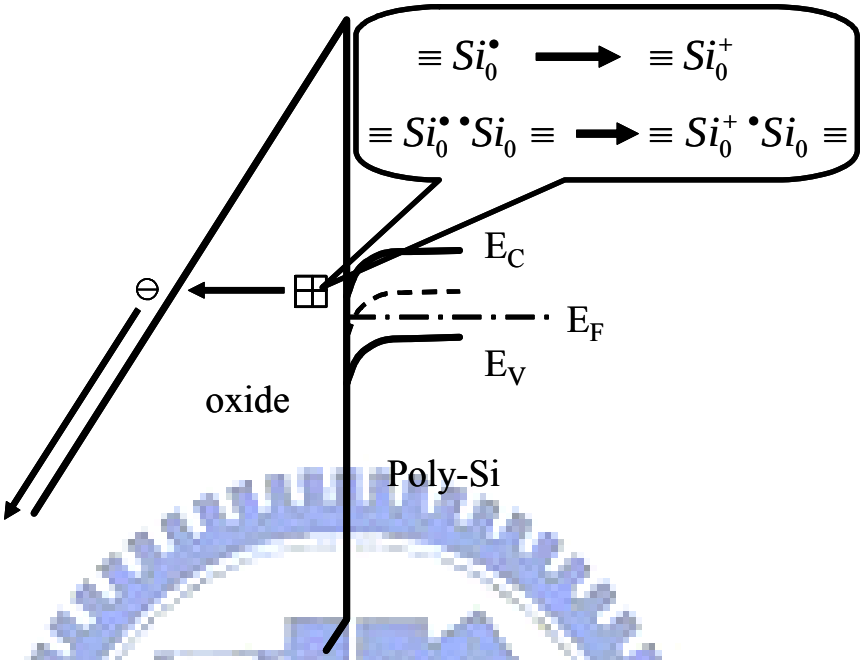


Fig. 3-6 Schematic illustration of the degradation mechanisms under V_G/V_D=13V/13V. The band diagram is taken near the source [36].

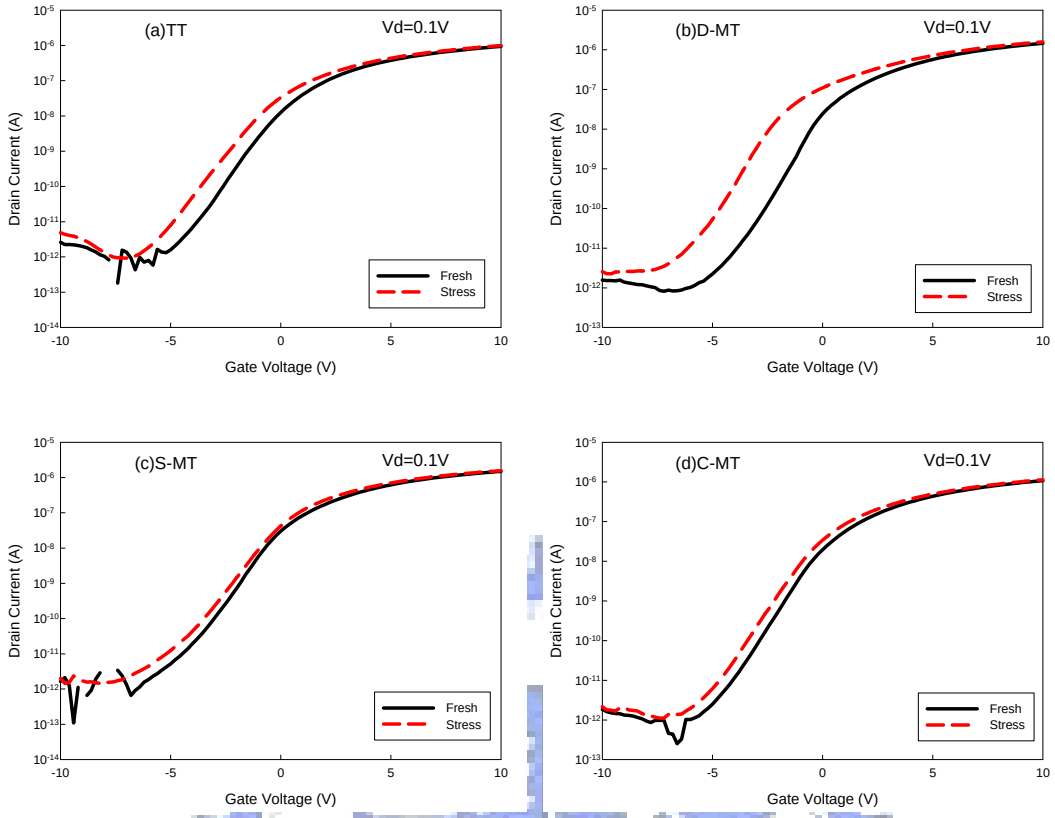


Fig. 3-7 Subthreshold characteristics of (a) TT, (b) D-MT, (c) S-MT, and (d) C-MT in a test structure with a MILC poly-Si channel before and after a stress test under V_G =15V and V_D=V_S=0V for 1000 sec.

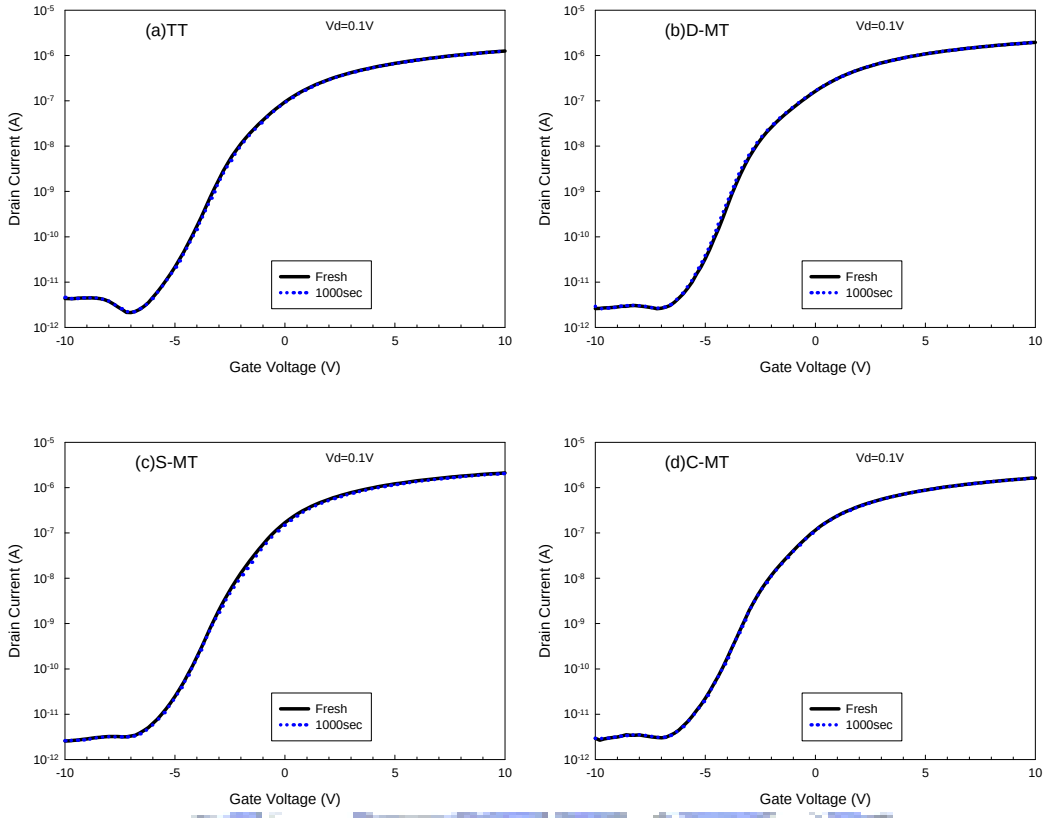


Fig. 3-8 Evolution of subthreshold characteristics of (a) TT, (b) D-MT, (c) S-MT, and (d) C-MT in a test structure with a MILC poly-Si channel before and after a stress test under V_G =13V and V_D=V_S=0V for 1000 sec.

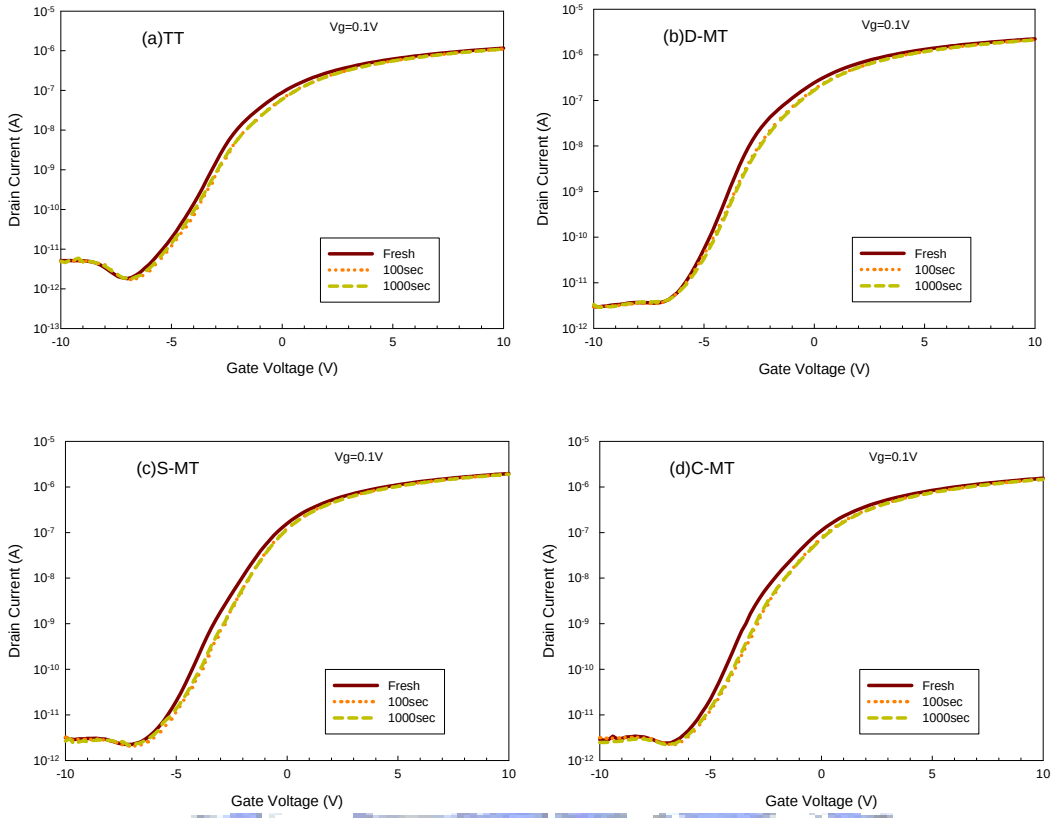


Fig. 3-9 (Fresh to 1000sec) Evolution of subthreshold characteristics of (a) TT, (b) D-MT, (c) S-MT, and (d) C-MT in a test structure with a MILC poly-Si channel before and after a stress test under V_G =30V and V_D=V_S=0V for 100 sec and 1000 sec.

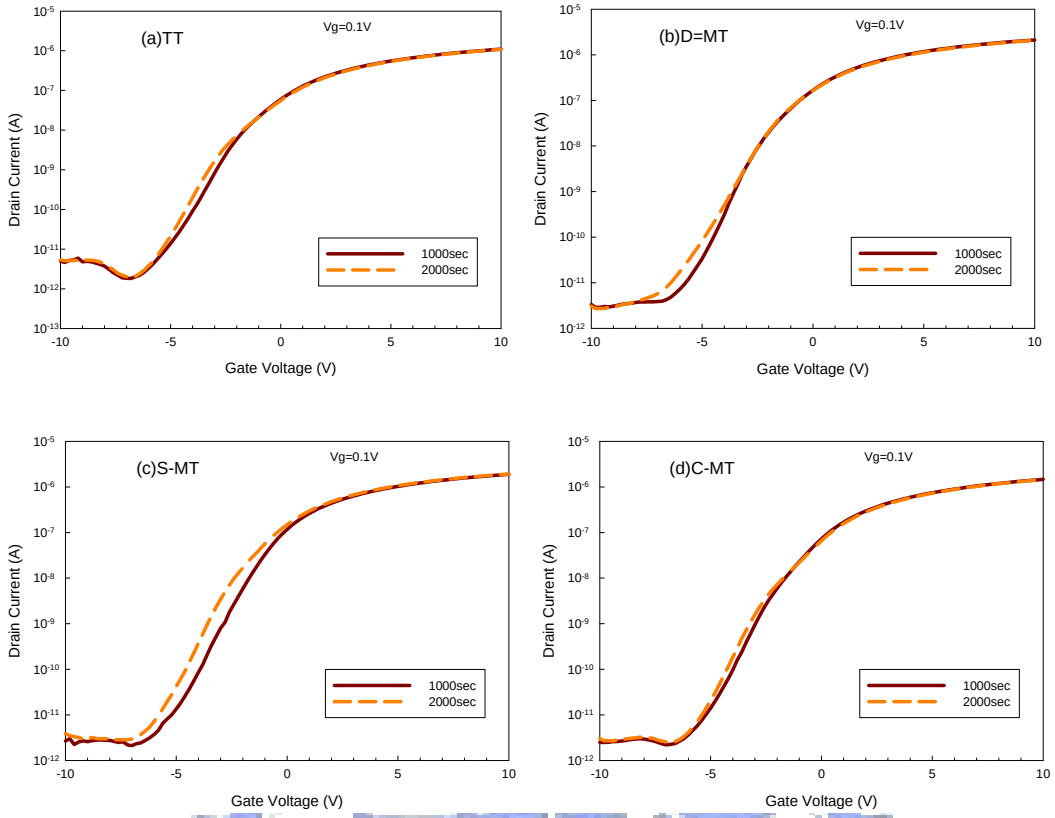


Fig. 3-10 Evolution of subthreshold characteristics of (a) TT, (b) D-MT, (c) S-MT, and (d) C-MT in a test structure with a MILC poly-Si channel after stress test under V_G =30V and V_D=V_S=0V for 1000 sec and 2000 sec.

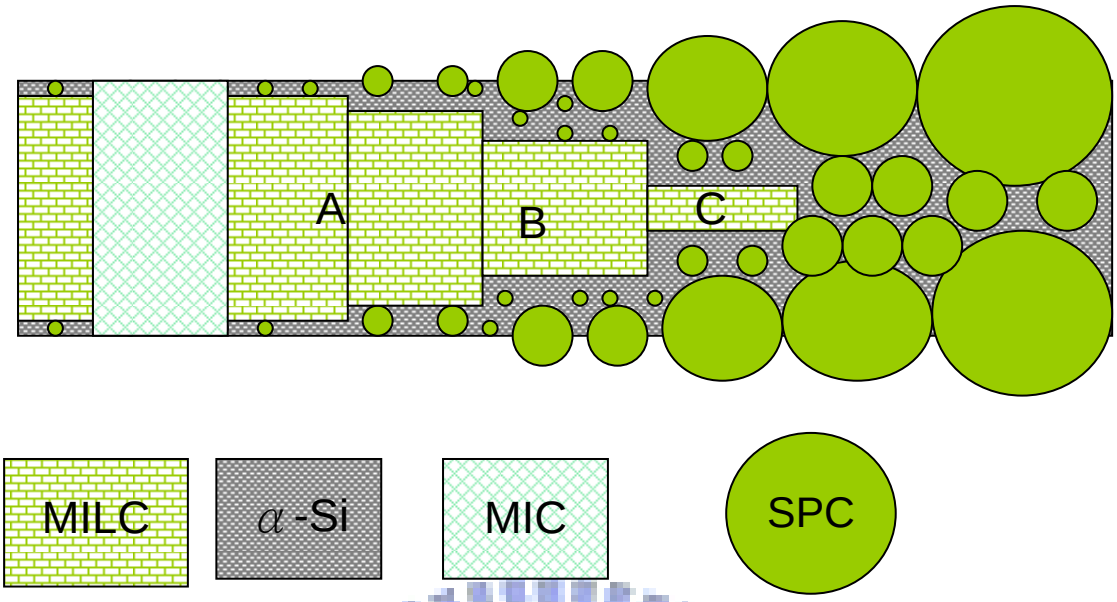


Fig. 3-11 Illustration of the location-dependant crystal structures in the MILC process.

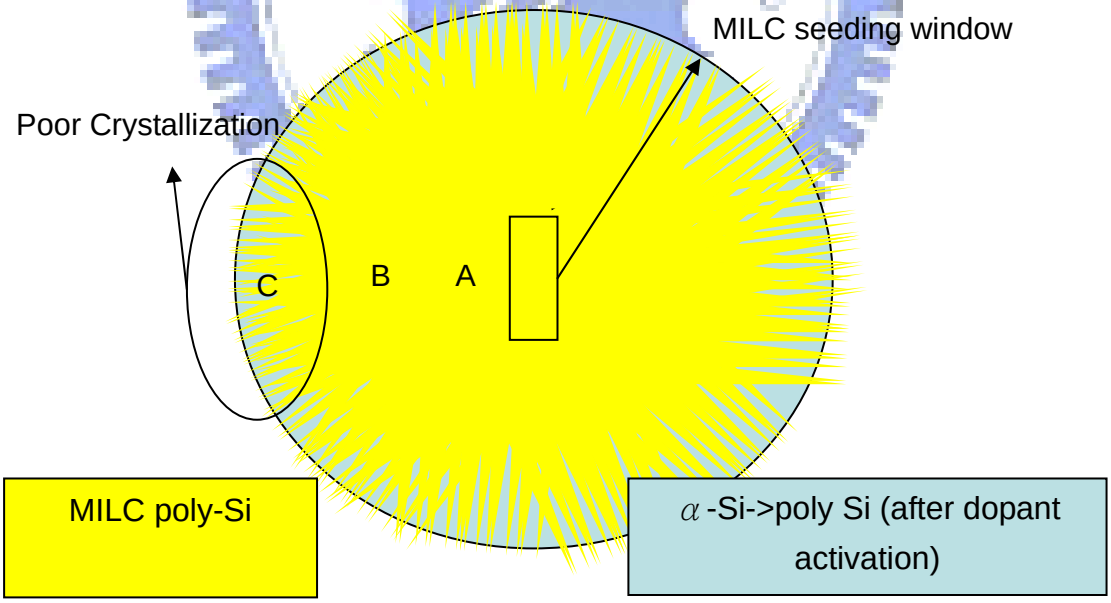


Fig. 3-12 Illustrations showing the radial development of the needle-like grains.

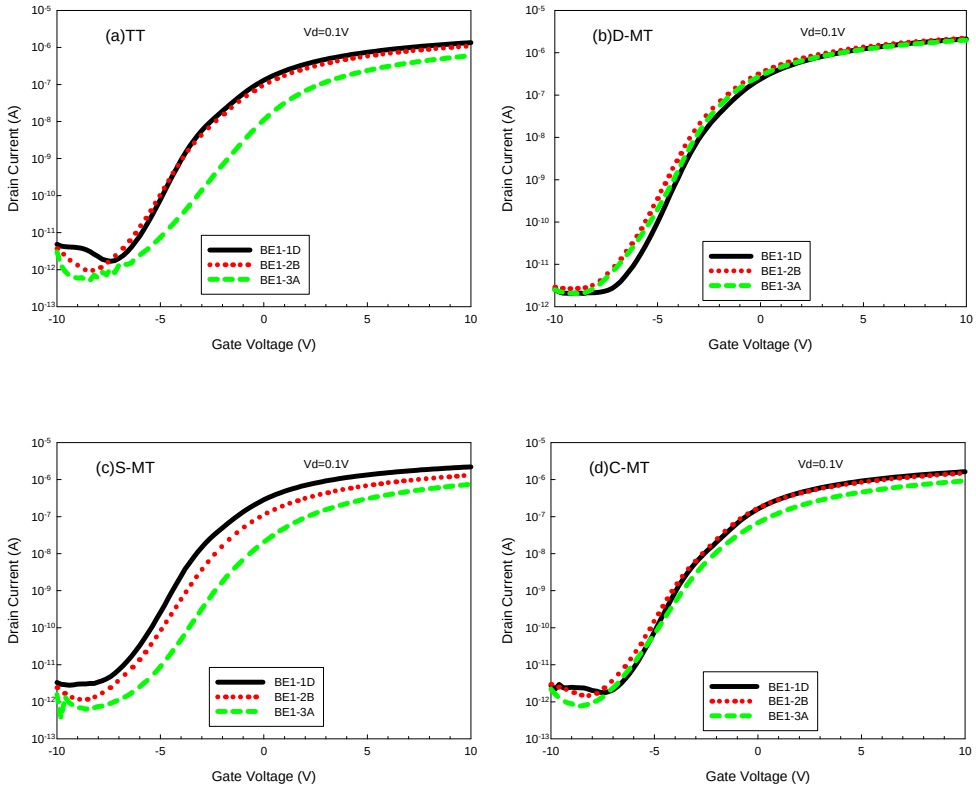


Fig. 3-13 Electrical characteristics of the four transistors contained in the three BE1- test structures (Table 3-1) with different Dc.

Table 3-2 Electrical parameters the four transistors contained in the three BE-1 test structures (Table 3-1) with different Dc.

TT	mobility($cm^2V^{-1}S^{-1}$)	VTH(V)	SS(V/decade)	Ion(A)
BE1-1	85.90	-0.68	0.968	1.35E-06
BE1-2	69.96	-0.48	1.108	1.09E-06
BE1-3	48.68	1.9	1.471	6.01E-07
D-MT	mobility(cm2V-1S-2)	VTH(V)	SS(V/decade)	Ion(A)
BE1-1	126.57	-0.99	0.990	2.11E-06
BE1-2	130.21	-1.5	1.080	2.24E-06
BE1-3	115.50	-1.42	1.090	1.98E-06
S-MT	mobility(cm2V-1S-2)	VTH(V)	SS(V/decade)	Ion(A)
BE1-1	135.57	-1.18	1.047	2.21E-06
BE1-2	80.40	-0.29	1.196	1.31E-06
BE1-3	57.16	1.95	1.254	7.48E-07
C-MT	mobility(cm2V-1S-2)	VTH(V)	SS(V/decade)	Ion(A)
BE1-1	97.10	-0.78	0.969	1.63E-06
BE1-2	86.45	-1.02	1.078	1.49E-06
BE1-3	57.98	0.16	1.196	9.25E-07

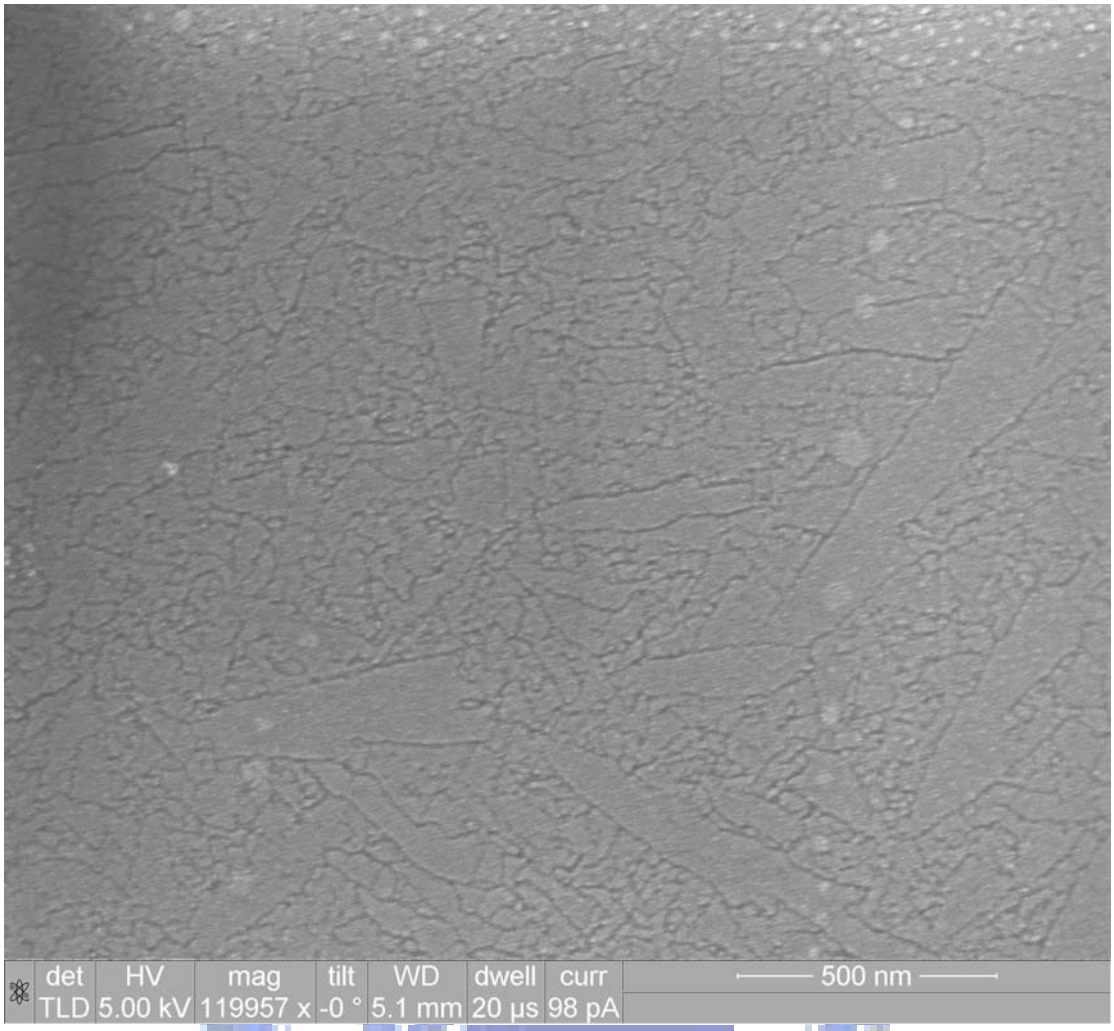


Fig. 3-14(a) SEM pictures of the D-MT channel regions in BE1-1

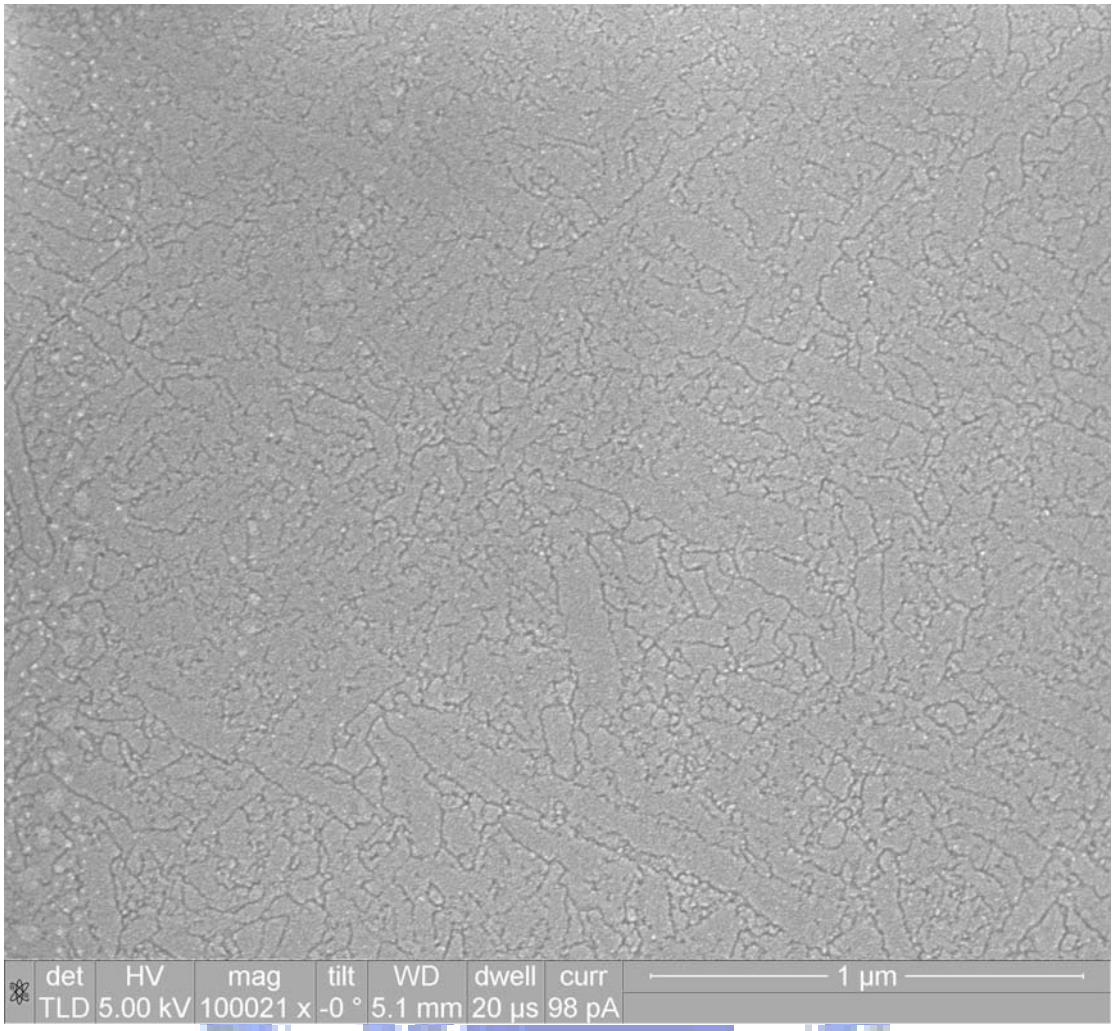


Fig. 3-14(b) SEM pictures of the D-MT channel regions in BE1-2

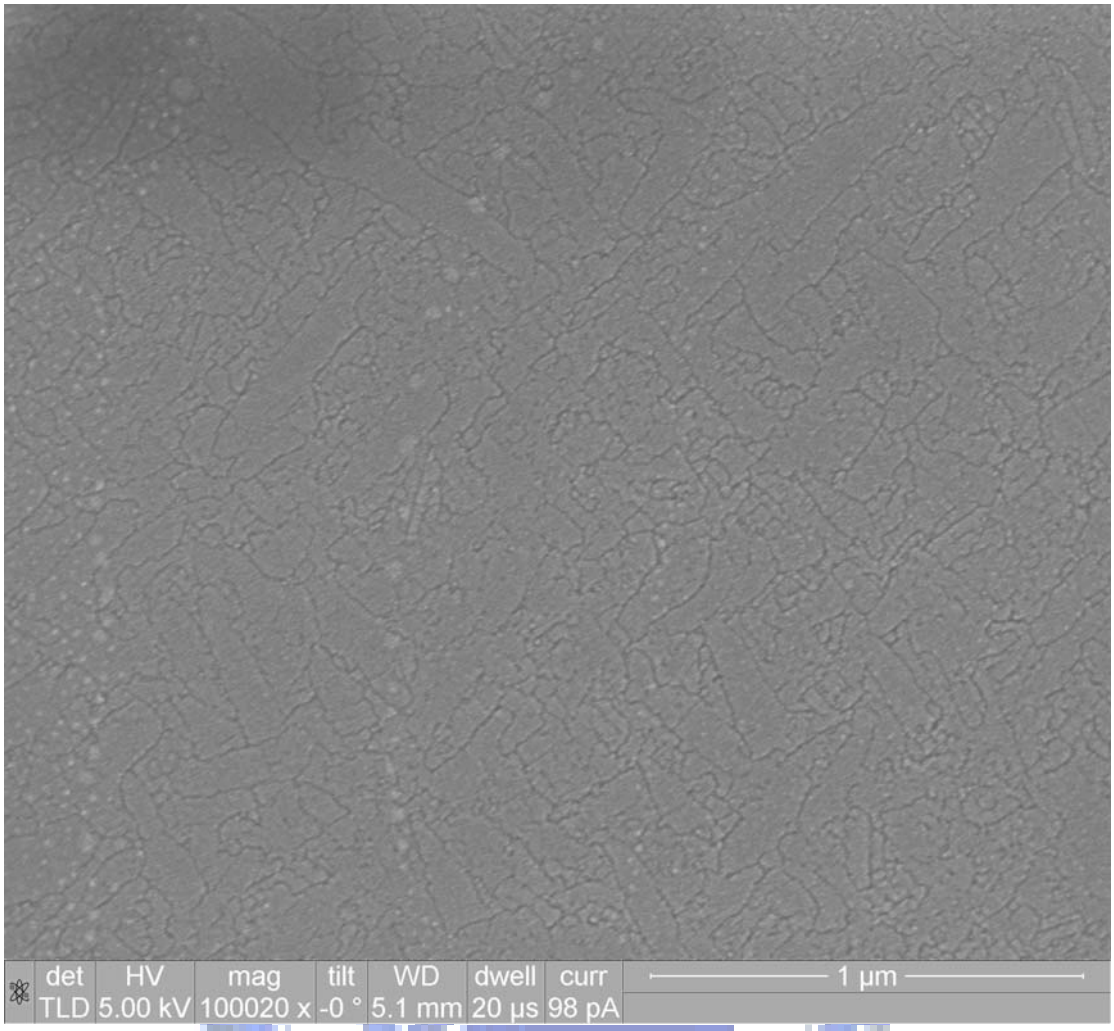


Fig. 3-14(c) SEM pictures of the D-MT channel regions in BE1-3

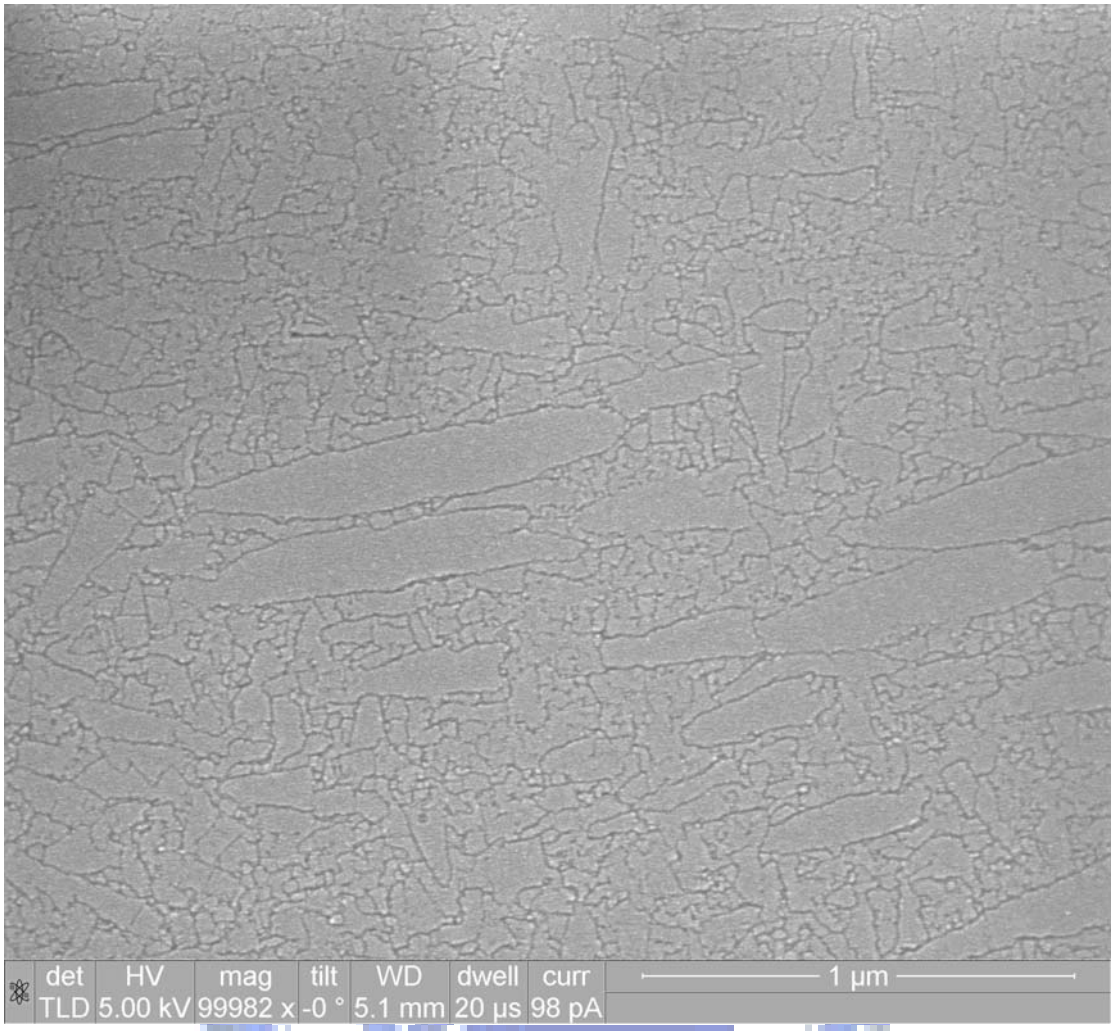


Fig. 3-15(a) SEM pictures of the C-MT channel regions in BE1-1

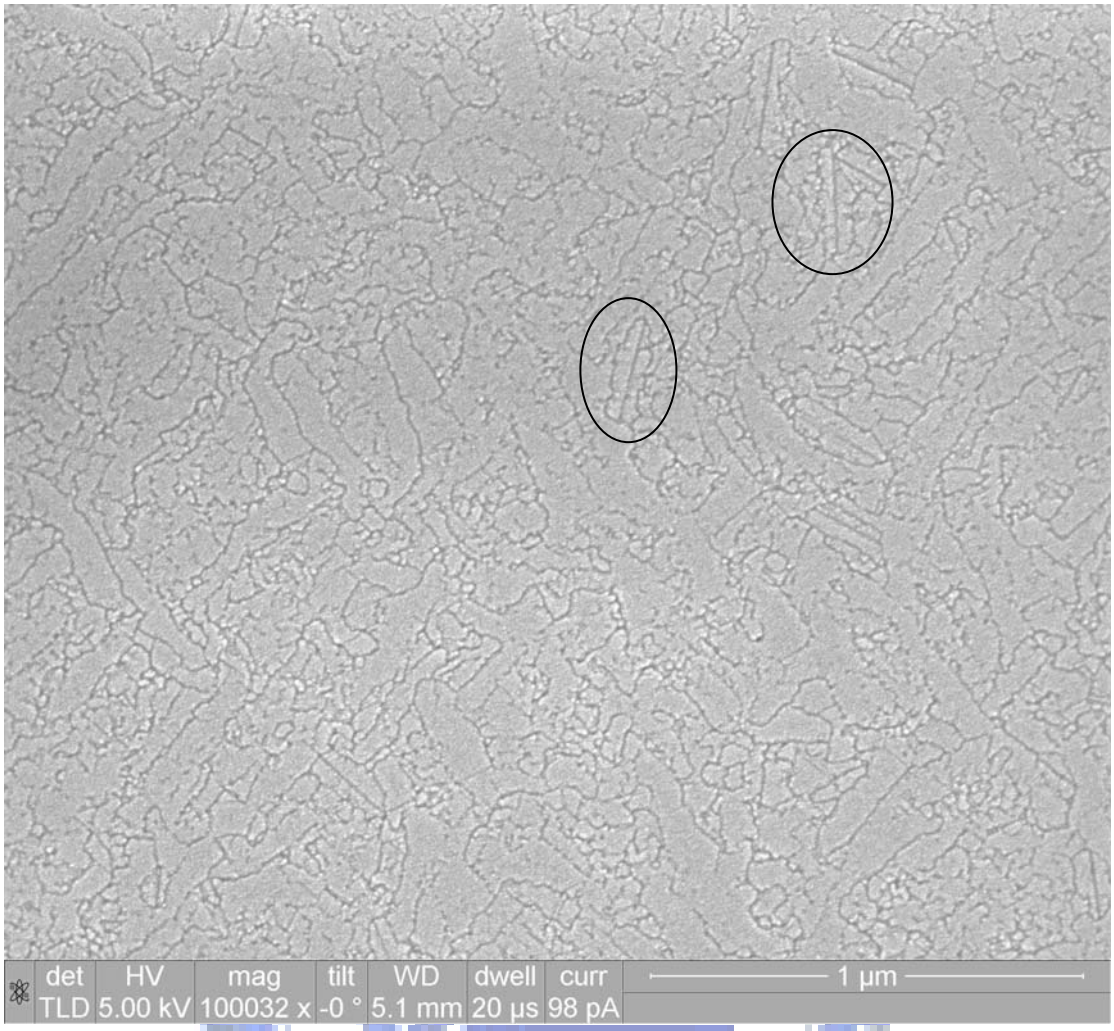


Fig. 3-15(b) SEM pictures of the C-MT channel regions in BE1-2

Fig. 3-15(c) SEM pictures of the C-MT channel regions in BE1-3

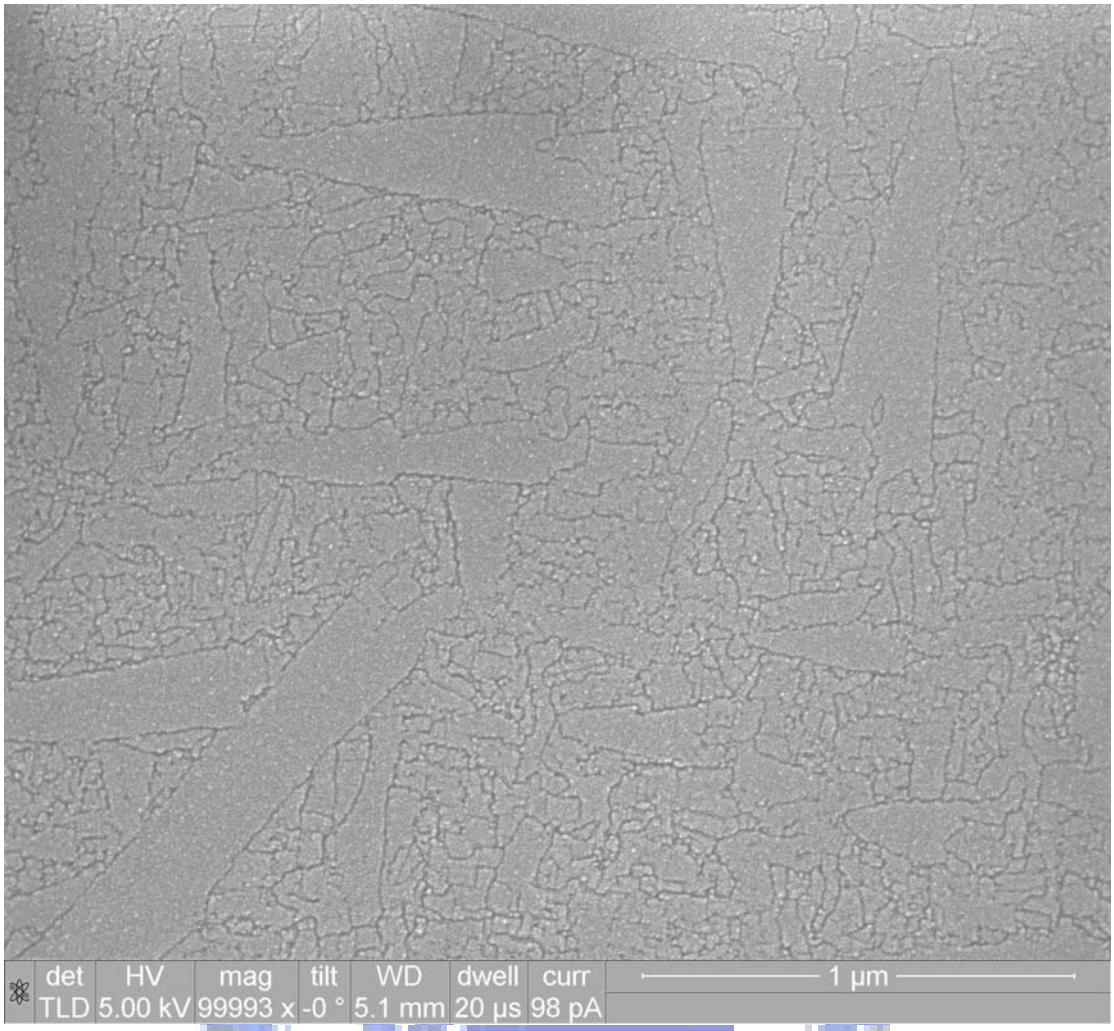


Fig. 3-16(a) SEM pictures of the S-MT channel regions in BE1-1

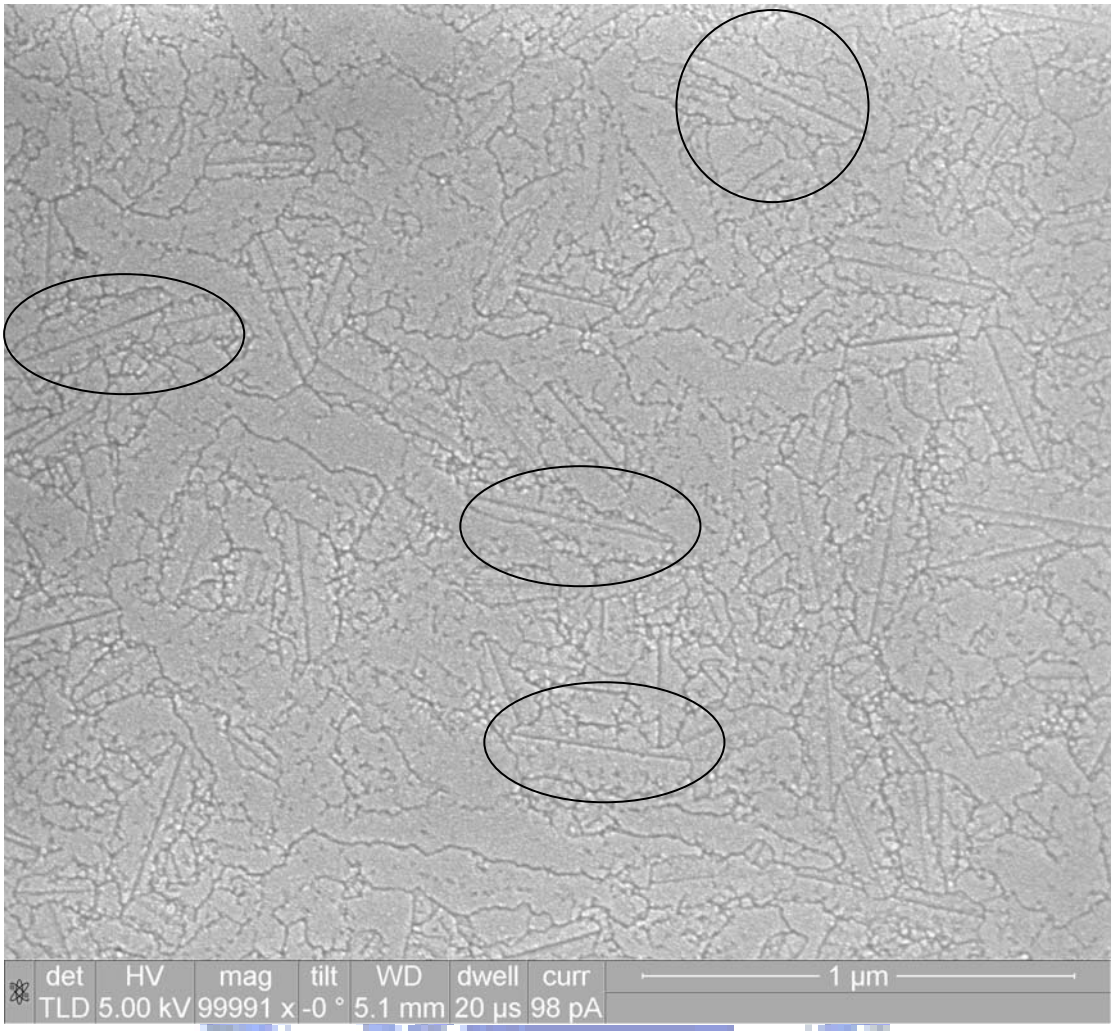


Fig. 3-16(b) SEM pictures of the S-MT channel regions in BE1-2

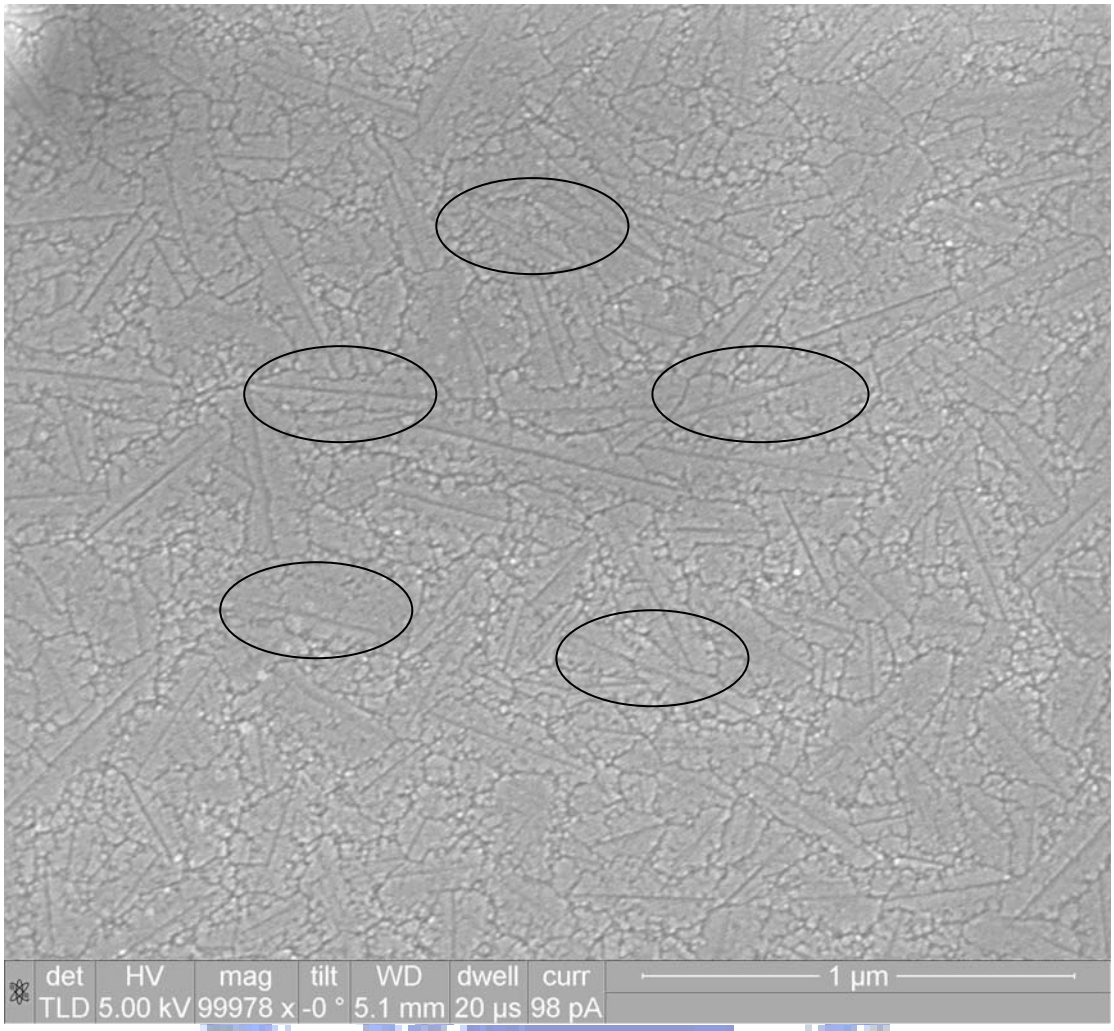


Fig. 3-16(c) SEM pictures of the S-MT channel regions in BE1-3

Fig. 3-17 A twin boundary observed in a grain of poly-Si formed by SPC method[38]. This feature is unique to SPC grains and thus can be used as an indicator of the occurrence of SPC mechanism.

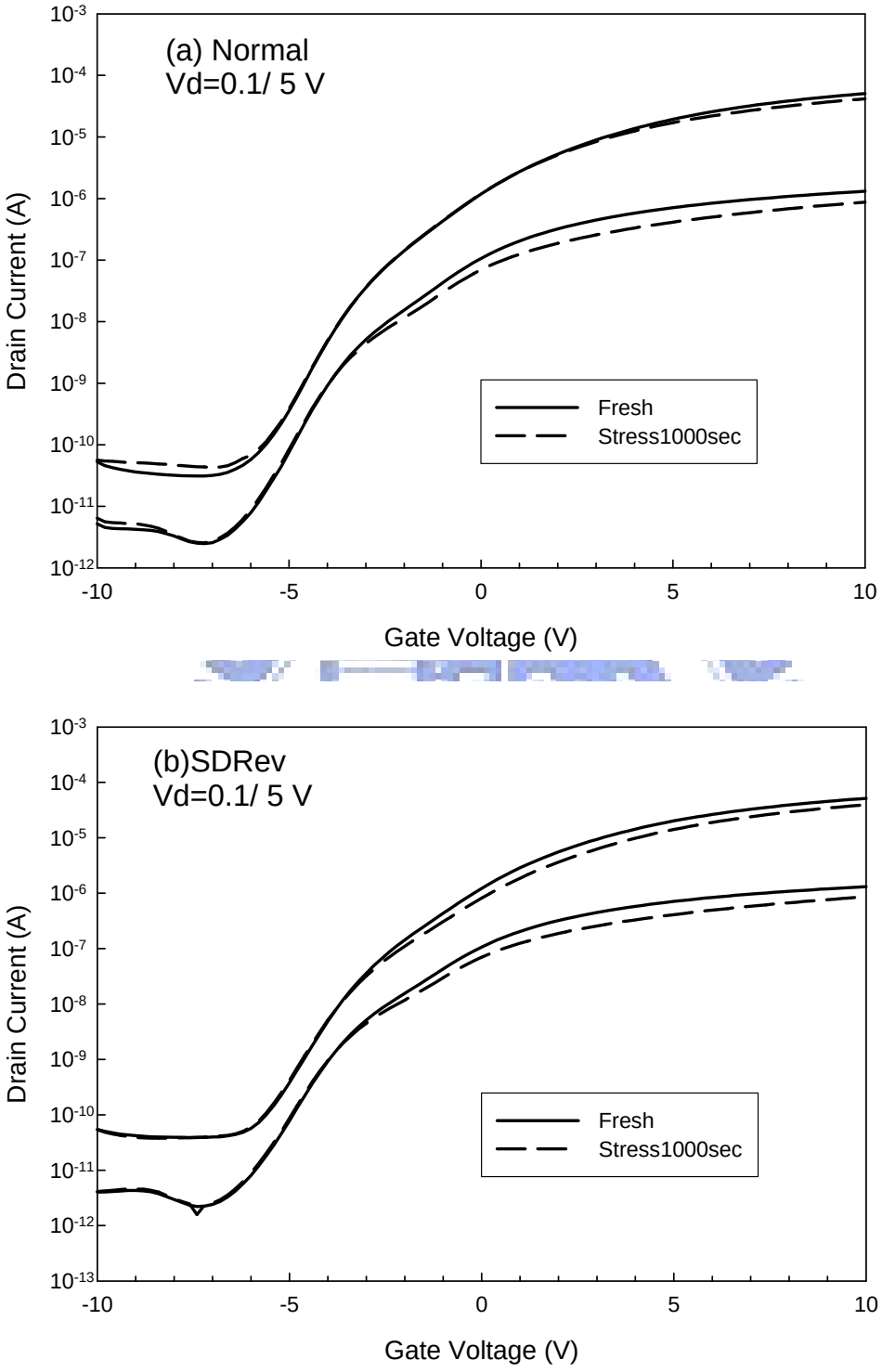
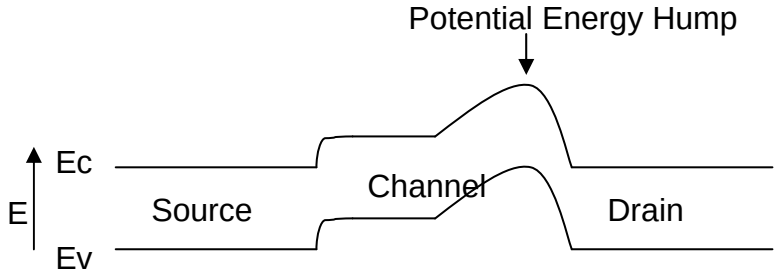
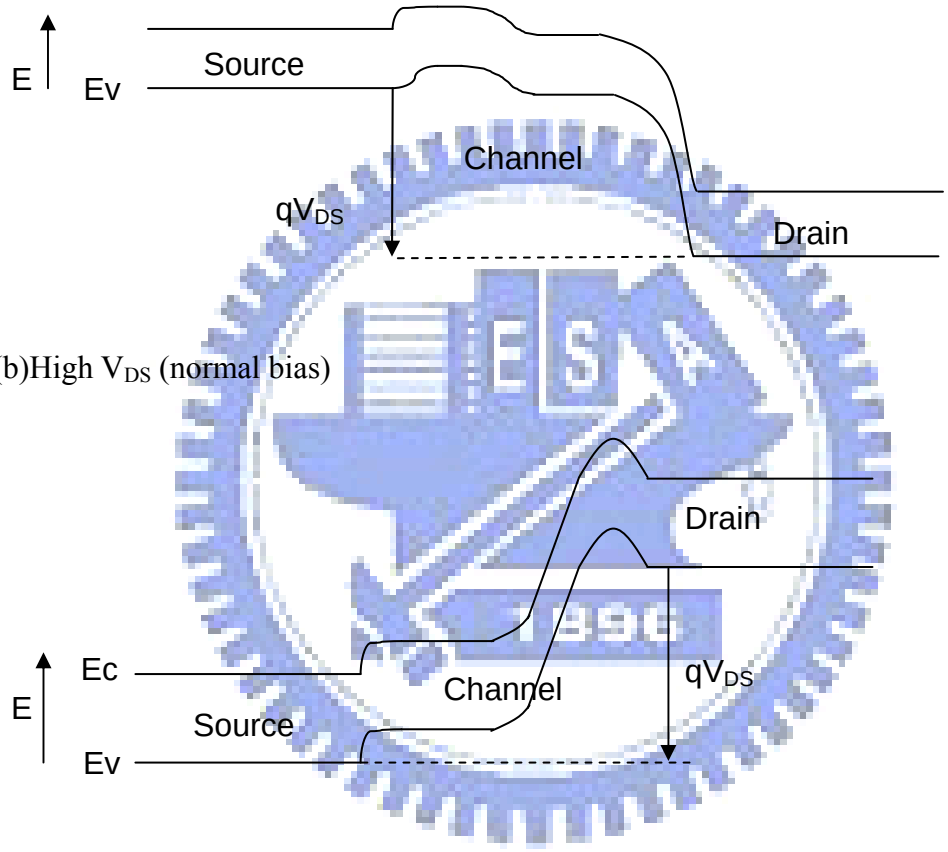


Fig. 4-1 Evolutions of subthreshold characteristics of TT before and after hot-carrier stressing at V_G/V_D=10V/20V measured under (a) normal, and (b) SDRev configuration in a test structure with MILC poly-Si channel.



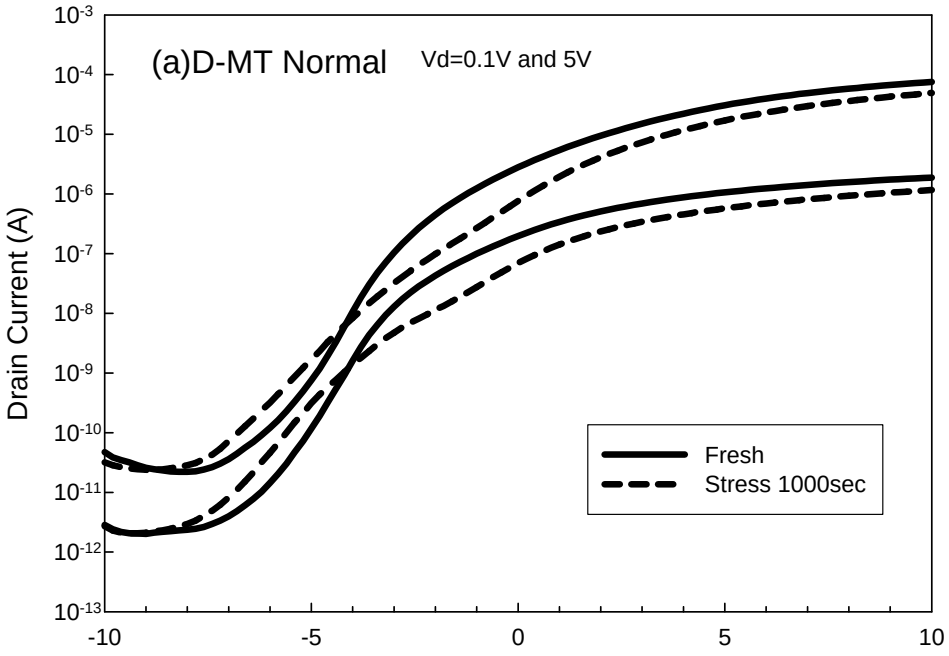
(a)After hot-carrier-induced degradation

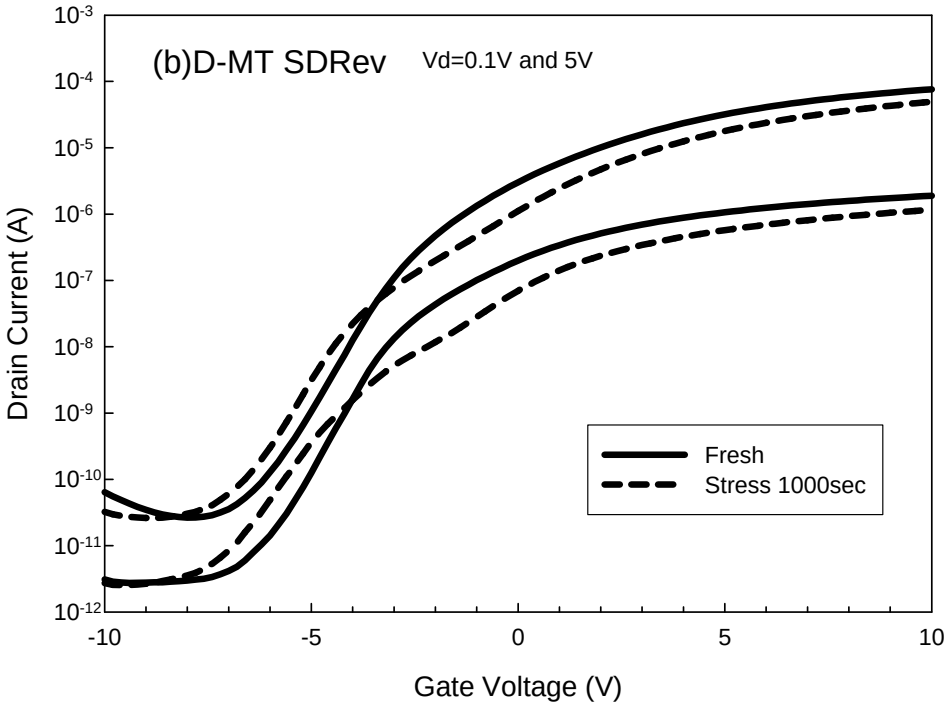


(b)High V_{DS} (normal bias)

(c) High V_{DS} (reverse bias)

Fig. 4-2 Energy band diagrams under different bias configurations [47].


(a)D-MT Normal
Vd=0.1V and 5V
Drain Current (A)
Gate Voltage (V)
Fresh
Stress 1000sec


(b)D-MT SDRev
Vd=0.1V and 5V
Drain Current (A)
Gate Voltage (V)
Fresh
Stress 1000sec

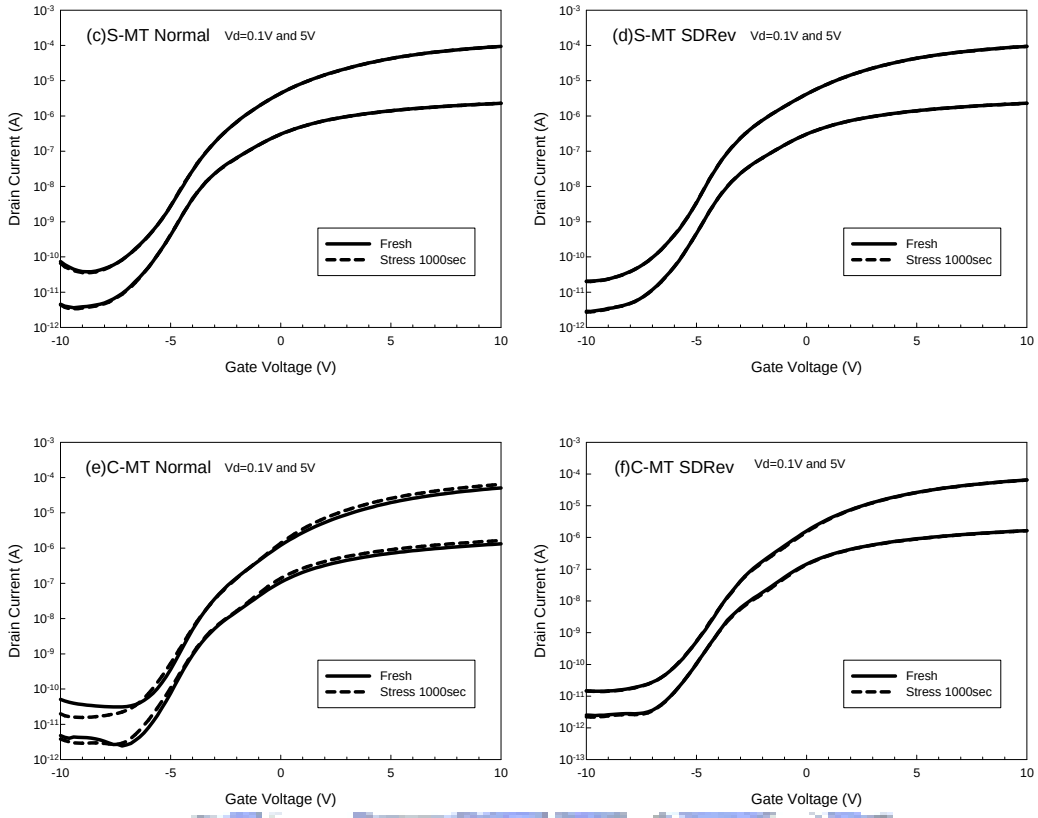


Fig. 4-3 Evolutions of subthreshold characteristics before and after hot-carrier stressing at V_G/V_D=10V/20V for 1000seconds: (a) normal mode of D-MT, (b) SDRev mode of D-MT (c) normal mode of S-MT, (d) SDRev mode of S-MT, (e) normal mode of C-MT, and (f) SDRev mode of C-MT in a test structure with MILC poly-Si channel.

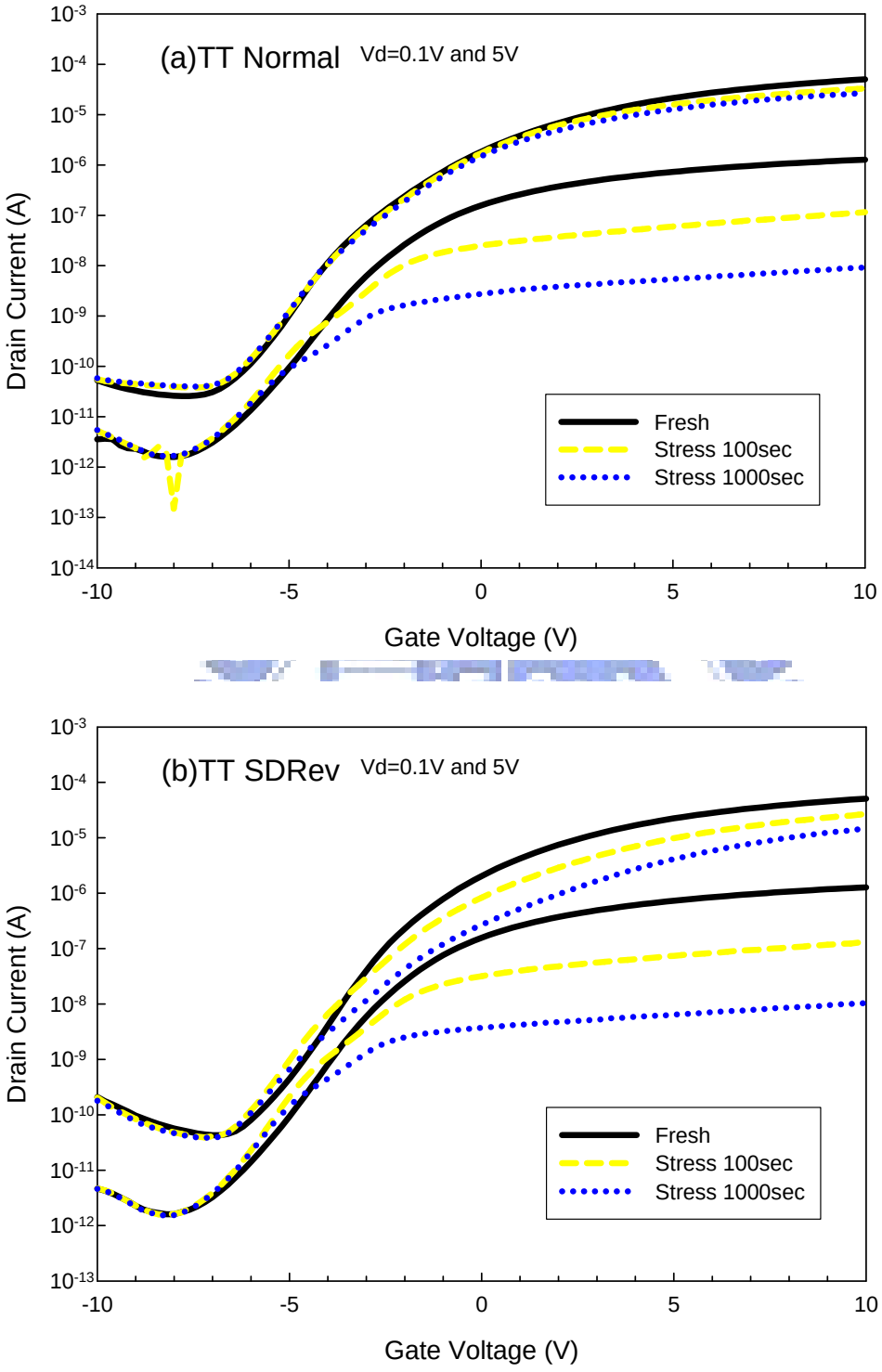


Fig. 4-4 Evolutions of subthreshold characteristics of TT before and after hot-carrier stressing at V_G/V_D=15V/30V measured under (a) normal, and (b) SDRev modes in a test structure with MILC poly-Si channel.

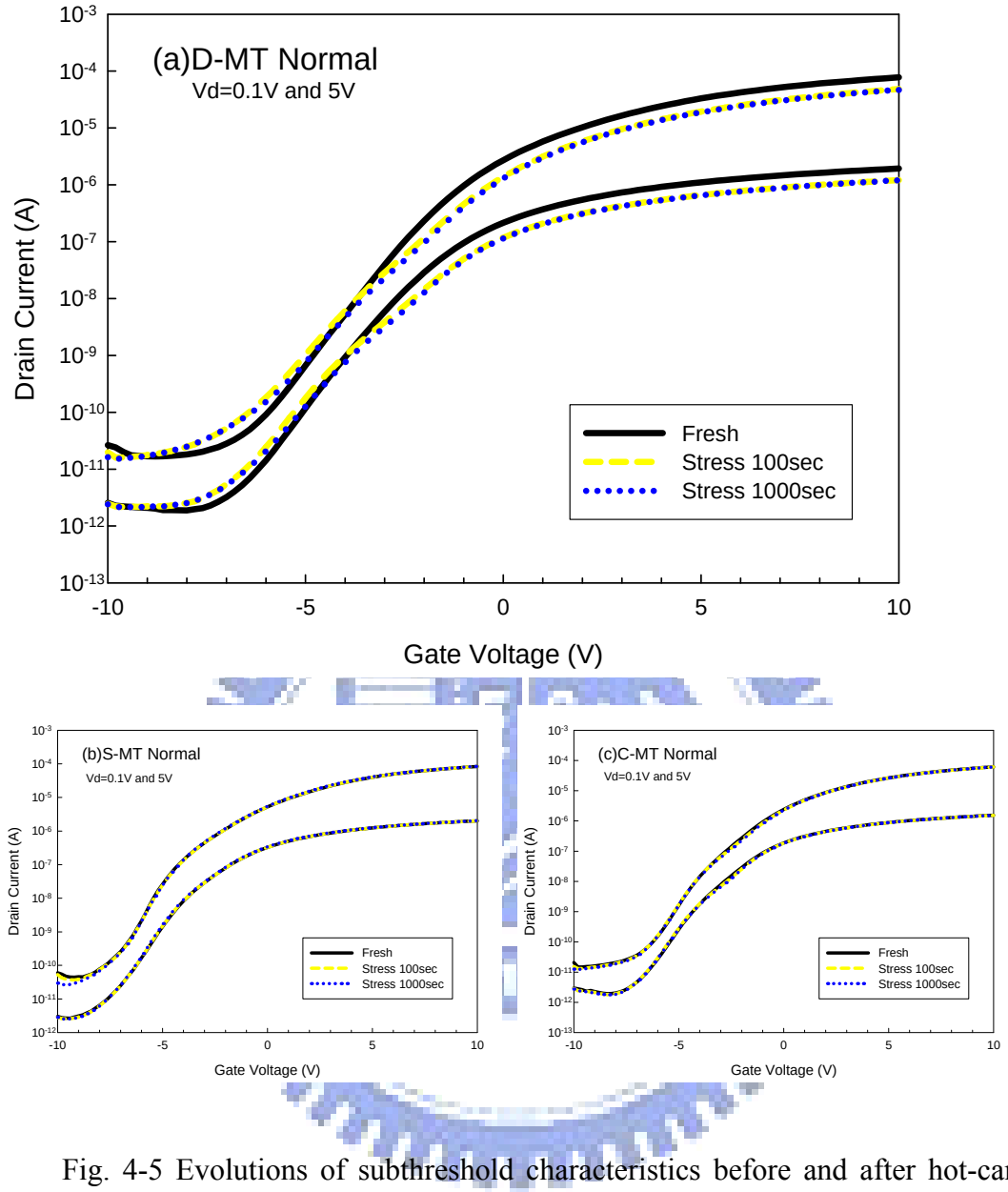


Fig. 4-5 Evolutions of subthreshold characteristics before and after hot-carrier stressing at V_G/V_D=15V/30V for 100 and 1000 sec: (a) D-MT, (b) S-MT, and (c) C-MT in a test structure with MILC poly-Si channel.

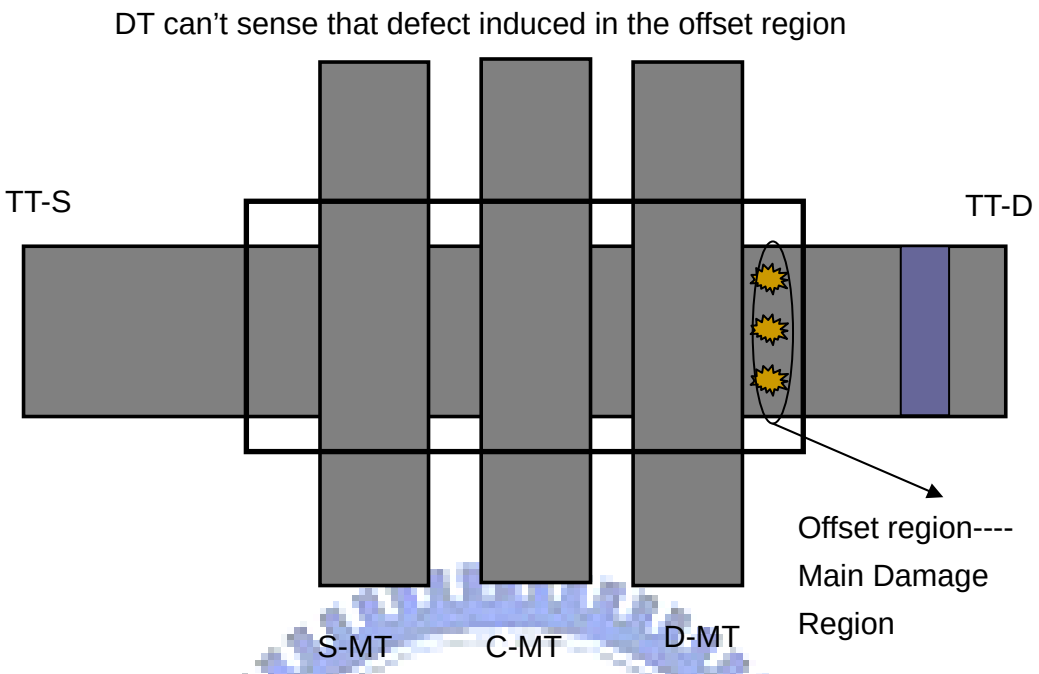


Fig. 4-6 Illustration of the major damage region in the HCTFT under a high voltage of V_G=0.5V_D stress condition.

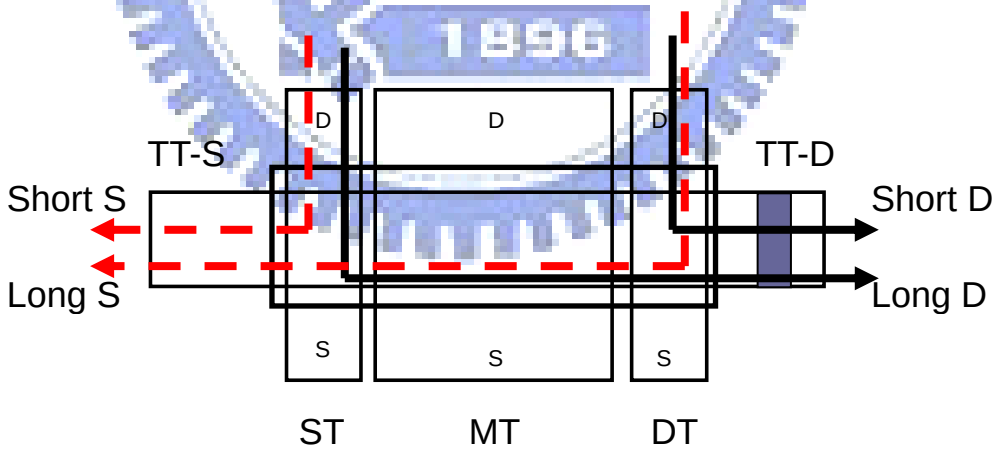


Fig. 4-7 Denotations of the proposed schemes for probing the offset regions in HCTFTs

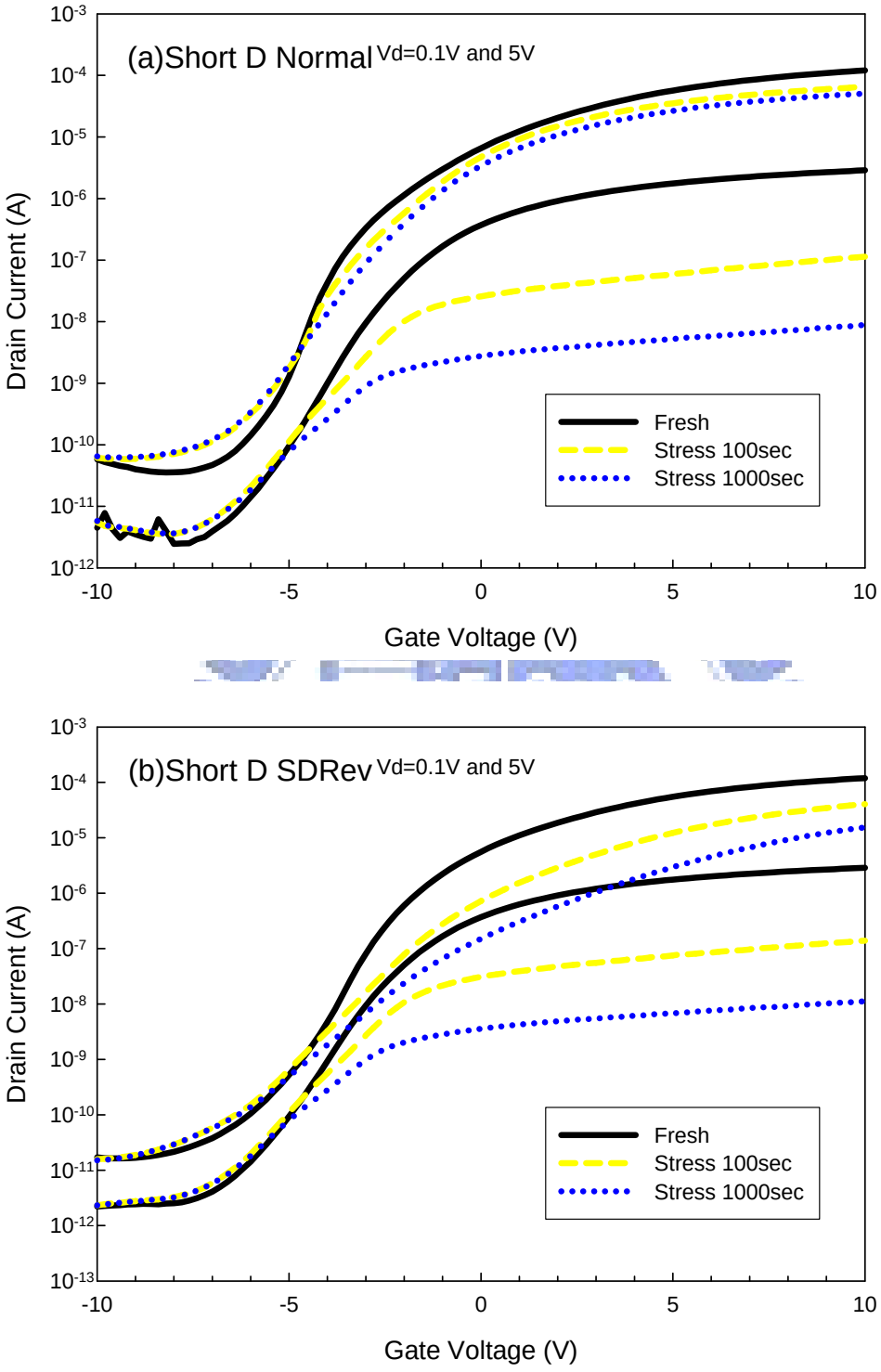
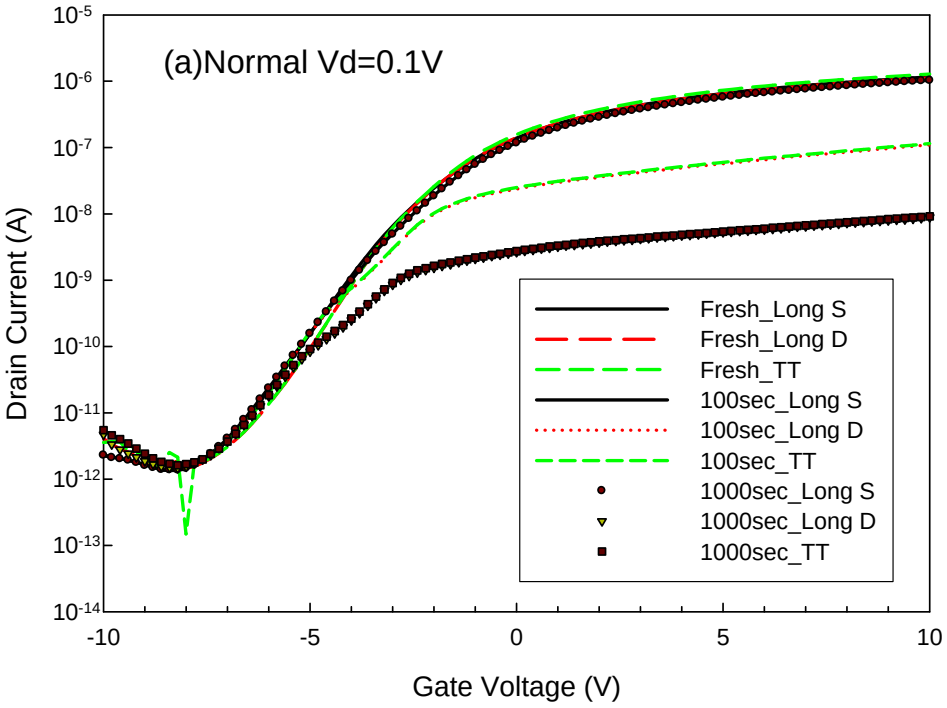
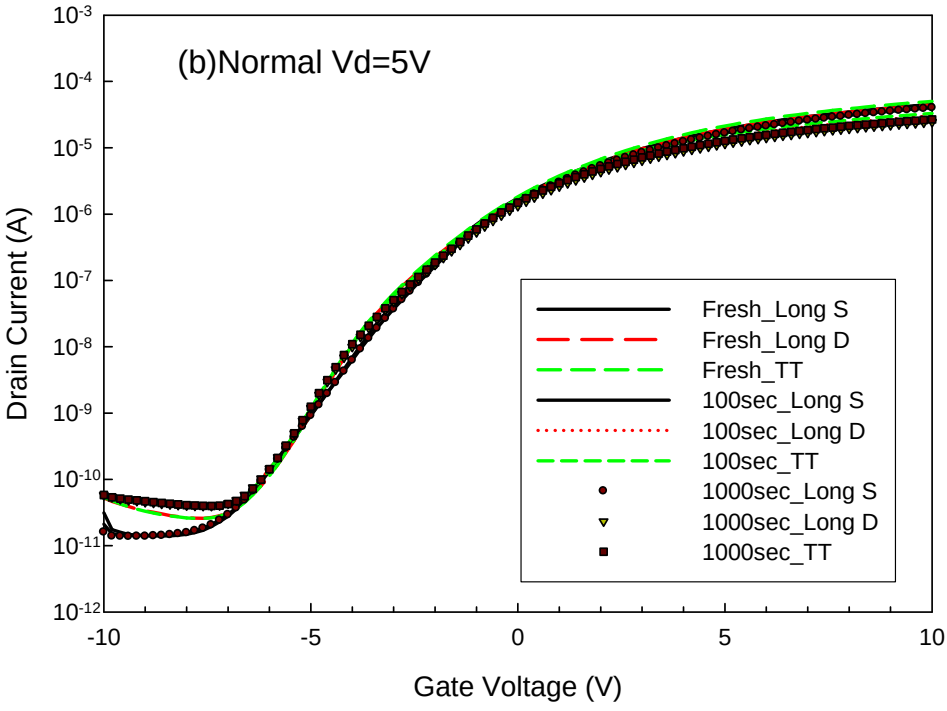


Fig. 4–8 Evolutions of subthreshold characteristics of short D before and after hot-carrier stressing at V_G/V_D=15V/30V for 100 sec and 1000 sec: (a) normal mode, and (b) SDRev mode.


(a)Normal Vd=0.1V
Drain Current (A)
Gate Voltage (V)
Fresh_Long S
Fresh_Long D
Fresh_TT
100sec_Long S
100sec_Long D
100sec_TT
1000sec_Long S
1000sec_Long D
1000sec_TT


(b)Normal Vd=5V
Drain Current (A)
Gate Voltage (V)
Fresh_Long S
Fresh_Long D
Fresh_TT
100sec_Long S
100sec_Long D
100sec_TT
1000sec_Long S
1000sec_Long D
1000sec_TT

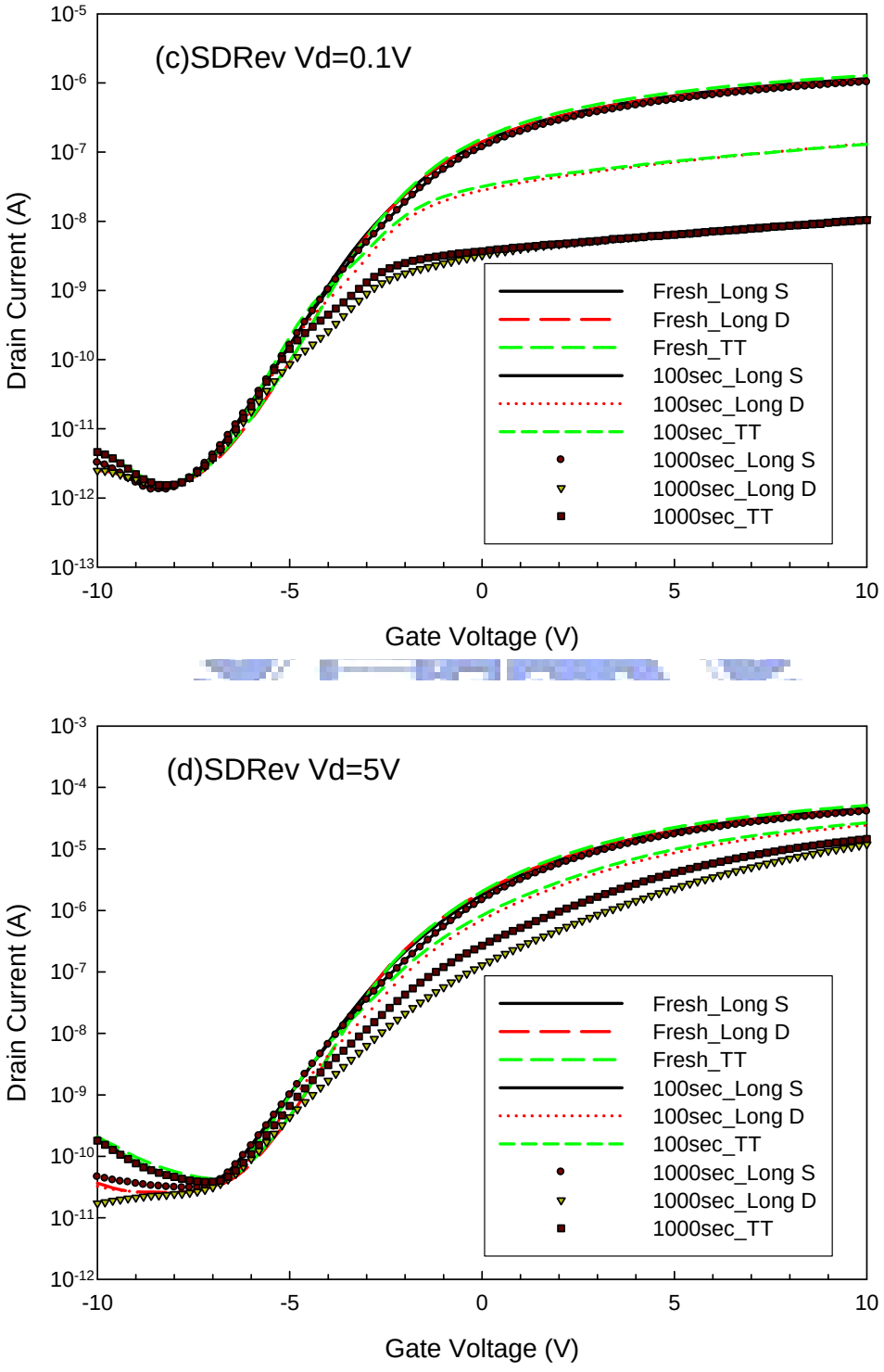


Fig. 4-9 Evolutions of subthreshold characteristics of Long S, Long D, and TT as a function of stress time: (a, b) Normal mode (at V_D=0.1V, 5V), (c, d) SDRev mode (measure at V_D=0.1V, 5V) under stress condition of V_G/V_D=15V/30V.

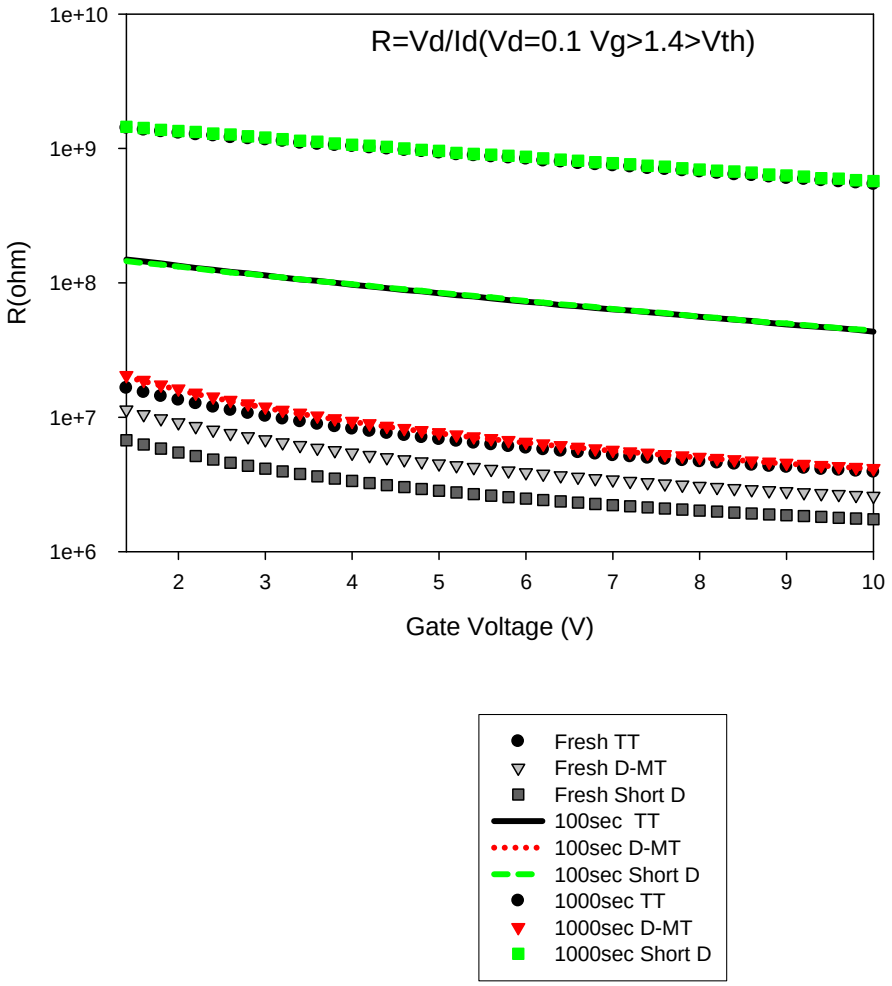


Fig. 4-10 Characteristics of hot-carrier-induced resistance (R_I) in the test transistor at different stress stages.

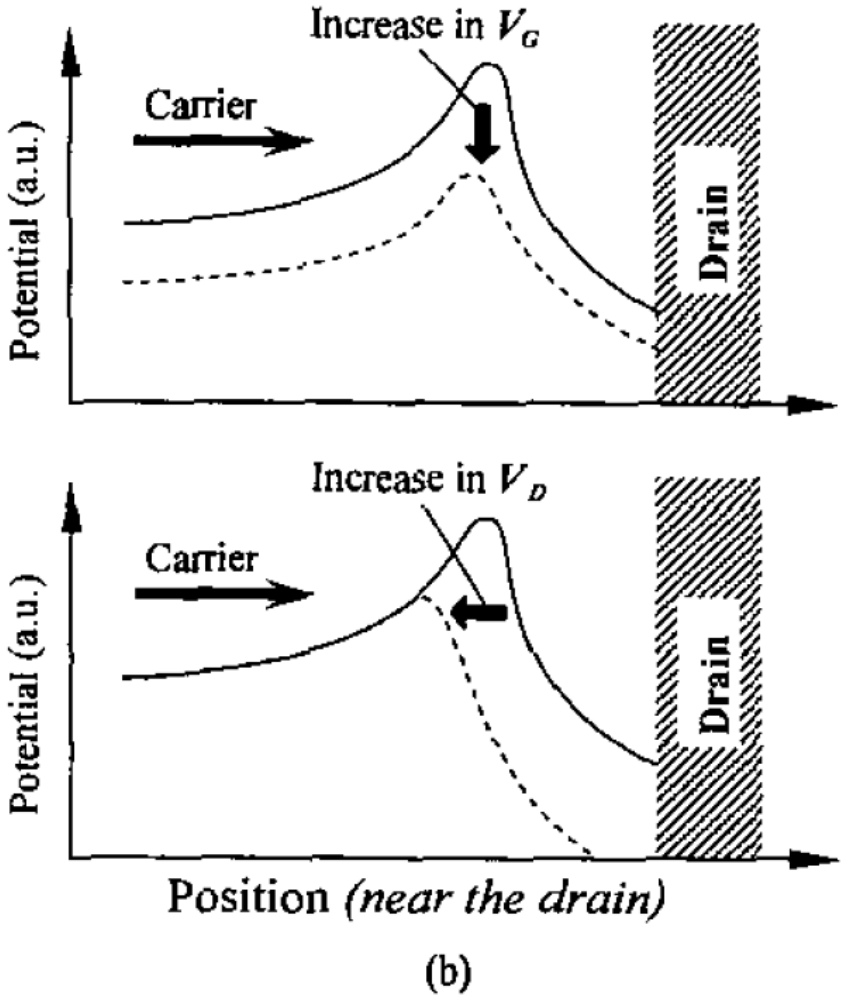


Fig. 4-11 The effects of different drain and gate bias on energy band bending [30]

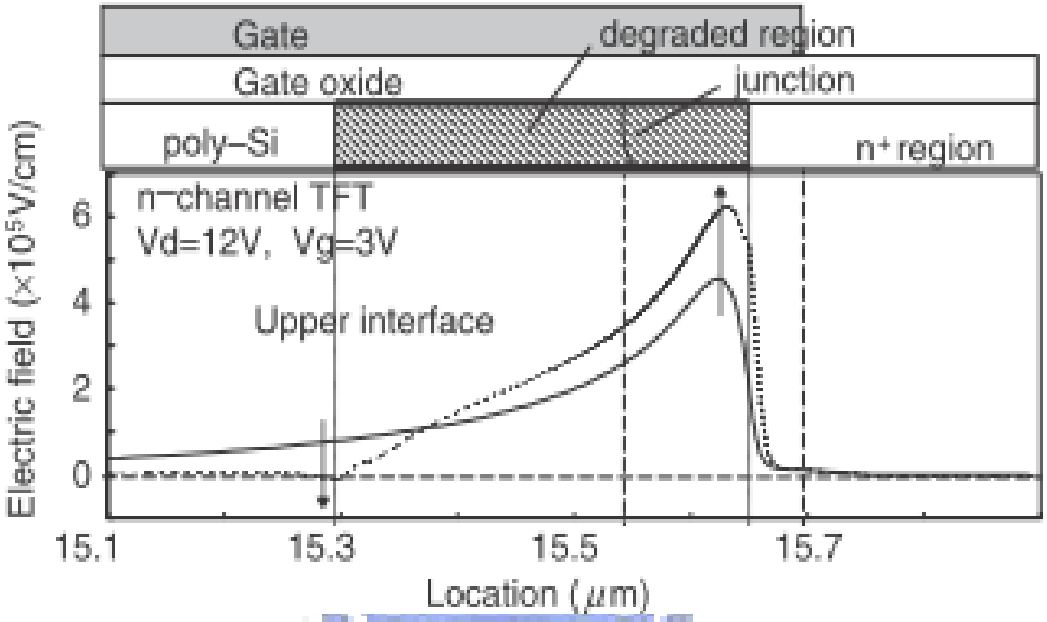


Fig. 4-12 Simulated lateral-field distributions at upper interfaces near the drain junction with (dotted line) and without (solid line) placing band-tail states and interface states[42]

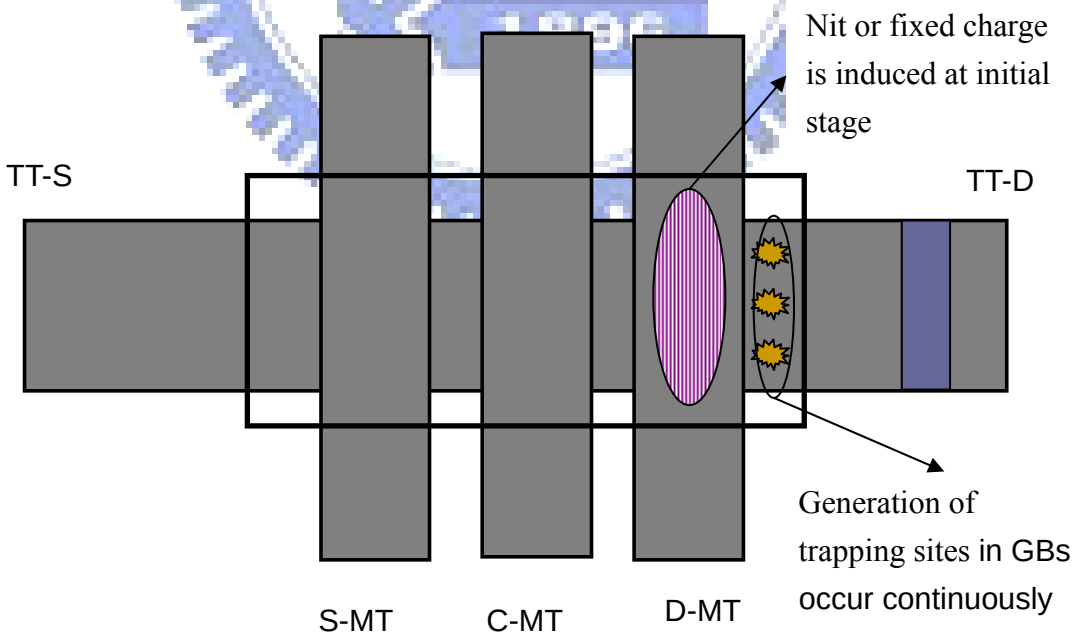
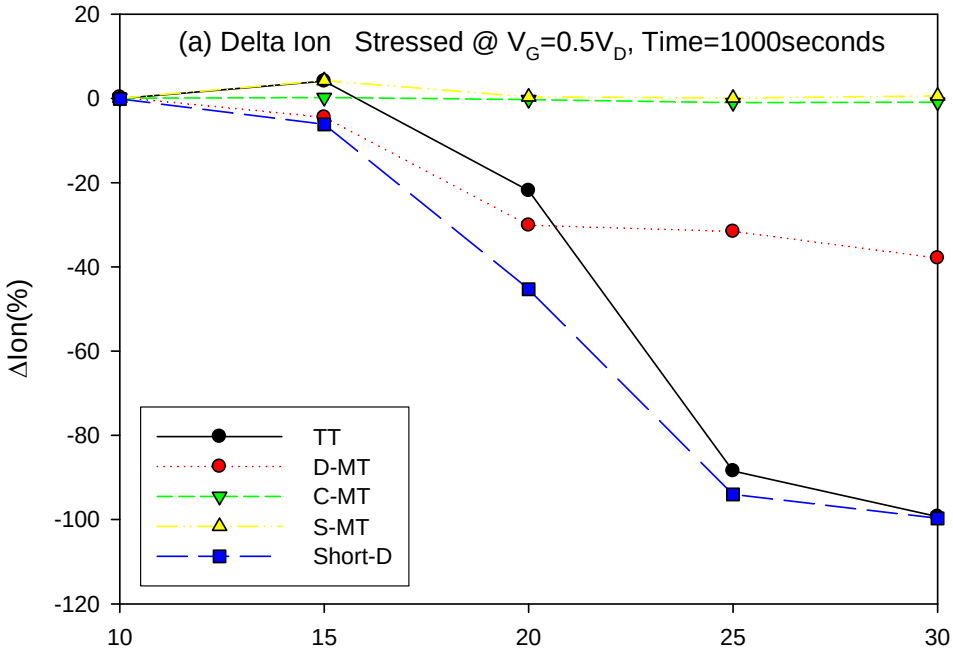


Fig. 4-13 Illustration of the major damage locations and defect types.



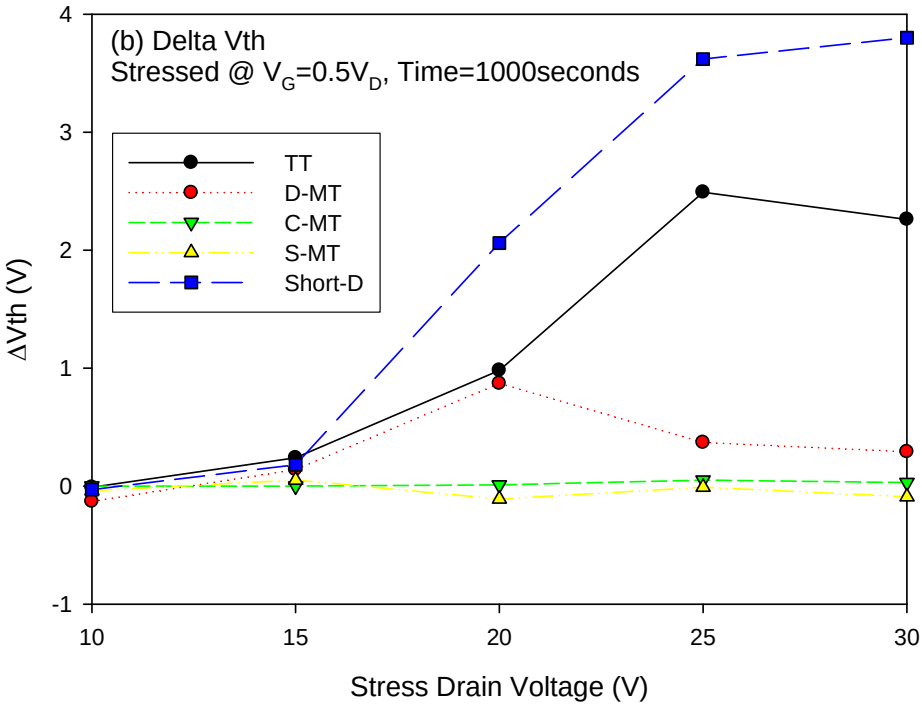
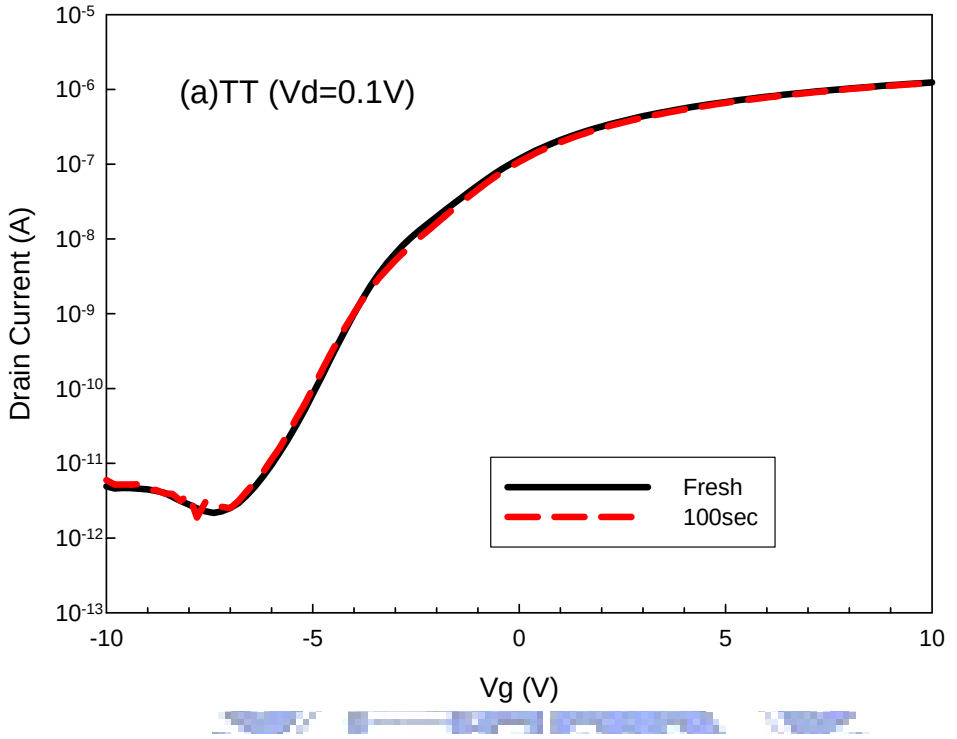
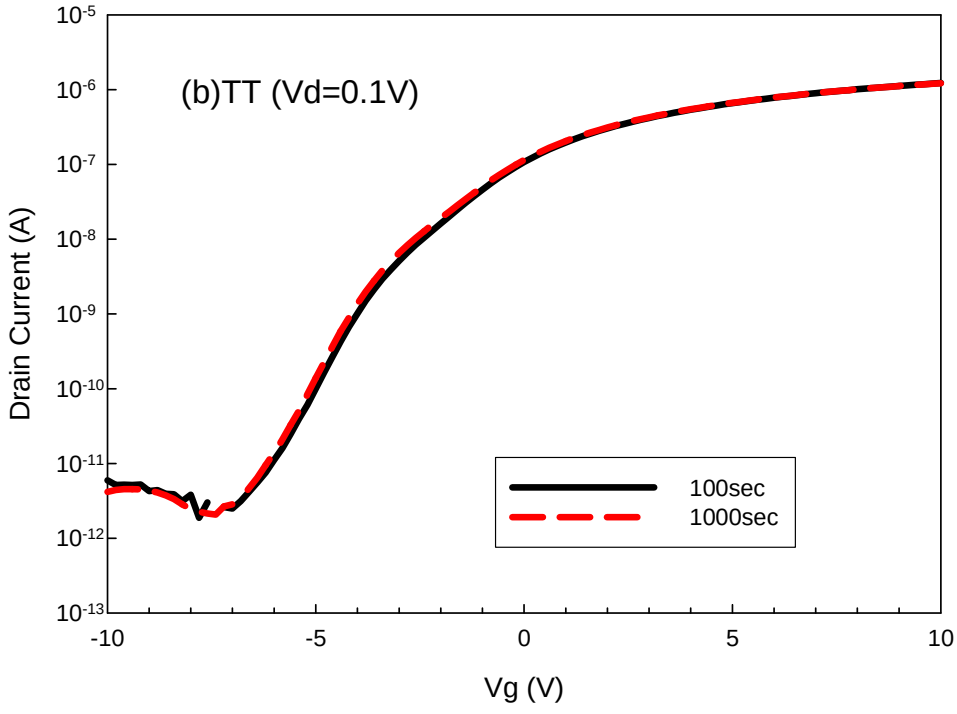


Fig. 4-14 (a) on-current (b) threshold voltage degradation of different test configurations under various hot-carrier stress conditions with constant V_G/V_D ratio of 0.5.


(a)TT (Vd=0.1V)
Drain Current (A)
Vg (V)
Fresh
100sec


(b)TT (Vd=0.1V)
Drain Current (A)
Vg (V)
100sec
1000sec

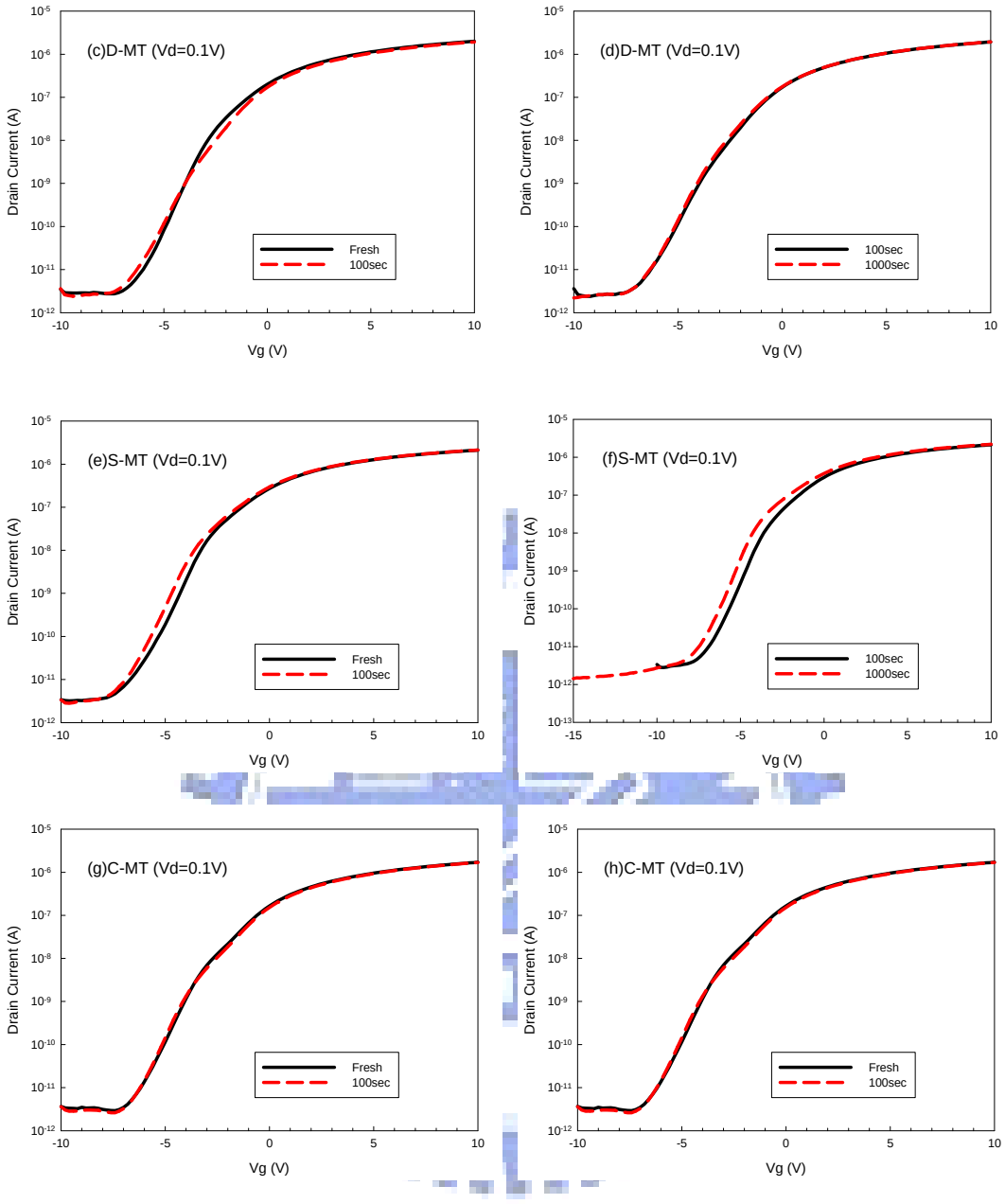


Fig. 4-15 Comparisons of electrical characteristics (a, c, e, and g) before and after 100sec, and (b, d, f, and h) from 100sec to 1000sec for the four transistors under V_G/V_D=30V/30V.

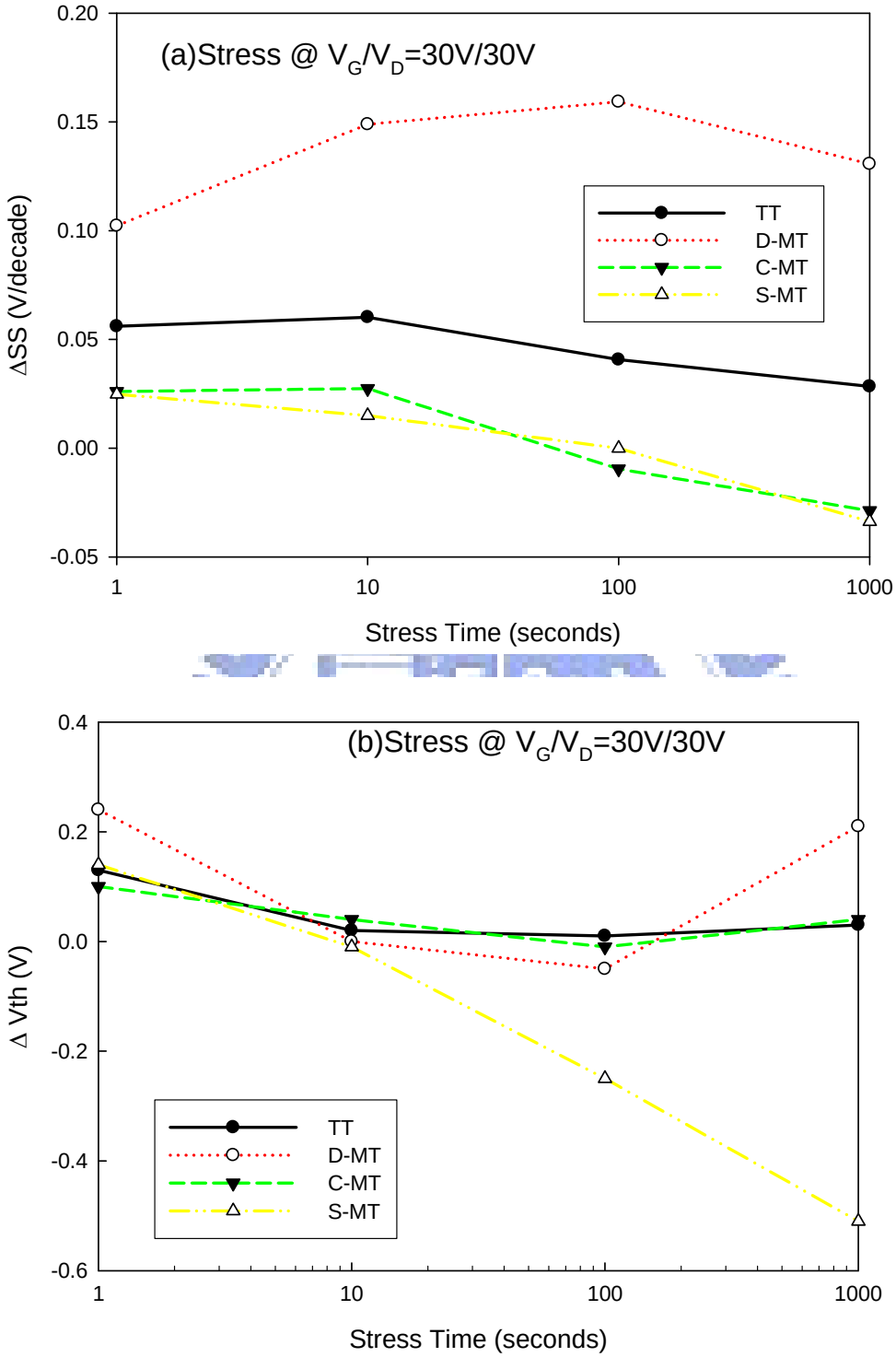


Fig. 4-16 Evolutions of (a) SS and (b) Vth of the four transistors during stressing under V_G/V_D=30V/30V.

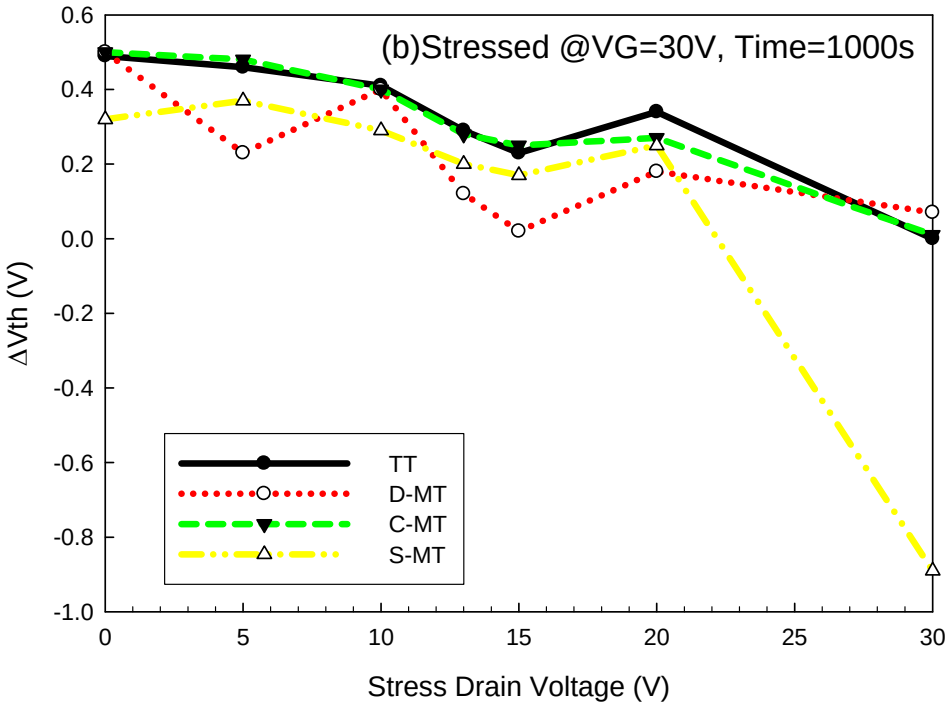


Fig. 4-17 Threshold voltage shift of the four transistors under V_G of 30 V and various V_D for 1000 sec.

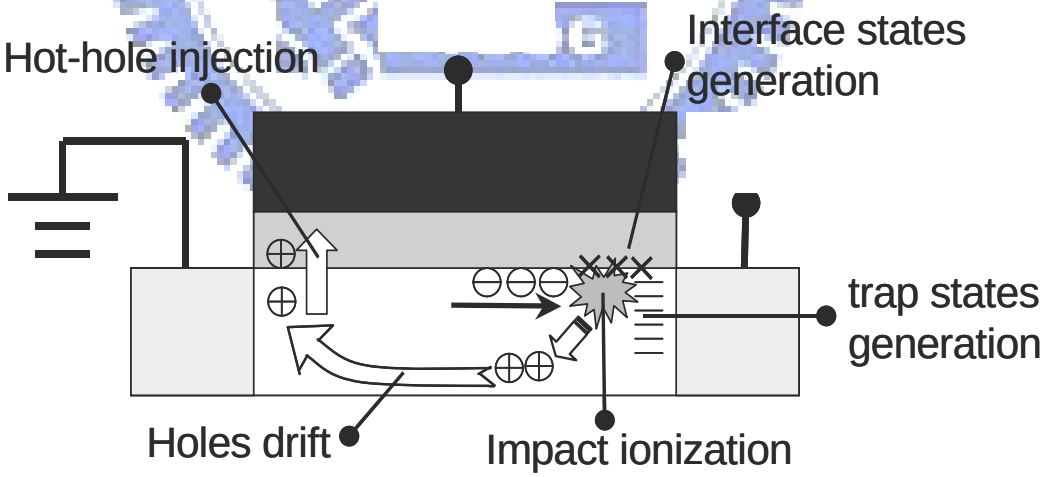


Fig. 4-18 Schematic illustration of the injection of holes into the gate oxide. The holes are generated by the impact ionization process.

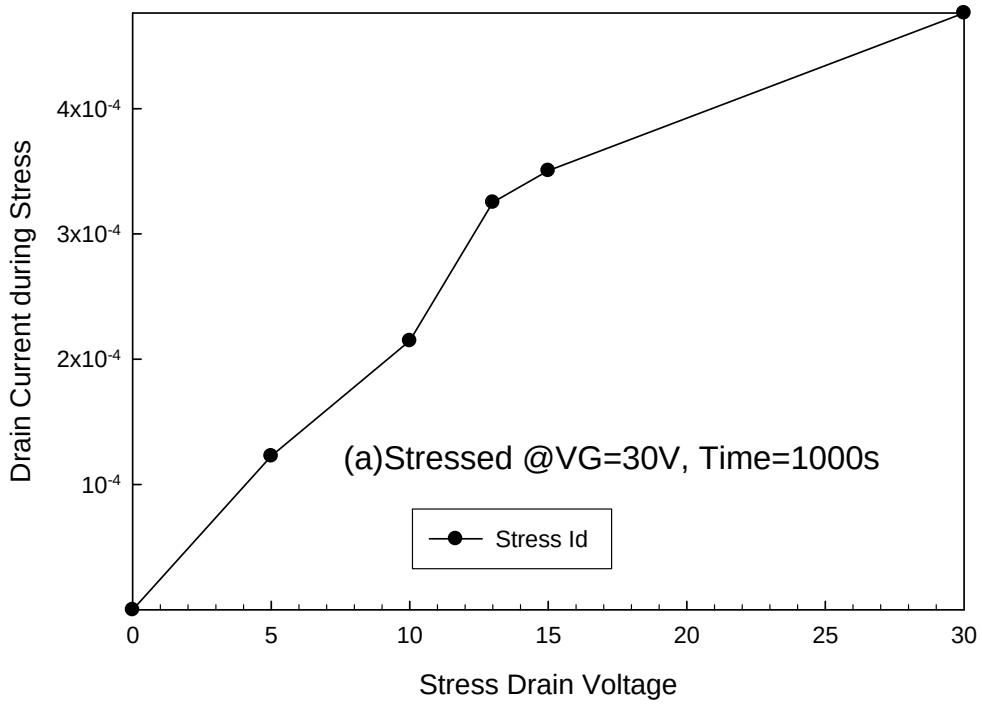


Fig. 4-19 Drain current of the S-MT under stress condition of V_G=30 V and various drain voltage for 1000 sec.

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