Chapter 1
Introduction

1.1 Background and Development of OTFTs

The Nobel Prize in chemistry in 2000 was awarded to Alan J. Heeger, Alan G. MacDiarmid and Hideki Shirakawa for the development of conducting polymers. After Shirakawa began the research on the conducting property of polymers in late 1970's [1.1], the first demonstration of organic thin film transistors (OTFTs) based on polyacetylene was reported in 1983 [1.2], but the mobility is quite low (about 10^{-5} cm^2/Vs) . The conductivity of the polymer can be altered from insulator to conductor through the method of doping. The possibility of fabricating OTFTs with small conjugated molecules was shown in 1989 [1.3] with sex thiophene rings linked at alpha positions, showed mobility on the order of 10^{-1} cm^2/Vs, which has reached the requirement for displays and is comparable to that of amorphous-Si TFTs. The comparisons between amorphous-Si TFTs, poly-Si TFTs and OTFTs are listed in *Table 1-1* [1.4].

Now days, a large number of conjugated molecules and polymers have been used to be the active material of OTFTs. The most significant parameter distinguishing those devices is the technique used for deposition. Organic semiconductors are potentially soluble in organic solvent and are therefore amenable to deposit at low temperatures on plastic substrates. Using low cost fabrication techniques such as spin-coating and inkjet-printing can avoid the complex vacuum evaporation system.

Since organic semiconductors can be processed at low temperatures and are compatible with plastic substrates, OTFTs may be used in applications requiring structural flexibility, large-area coverage, and especially low cost in fabrication. Such applications include

active-matrix liquid crystal displays (AMLCDs), active-matrix organic light-emitting diodes (AMOLEDs), and electronic paper-like displays. Additionally, organic sensors, textile like clothes, weaponry, digital watches, soft cell phones, low-end smart cards, radio-frequency identification (RFID) tags, and other electronic elements consisting of organic integrated circuits have been proposed.

The bonding between organic semiconductors is by Van Der Waals force between the hydrogen atoms, which are dangling on the ends of the fused rings. It is much weaker than that of the covalent force in inorganic materials, which is the reason for small mobility. In *fig. 1-1* [1.5], we can compare the increase of mobility in the past years for different organic semiconductors. If we want to exceed the limitation of the materials, there are several points we have to notice. First, the carrier injection from the contact electrode has to be optimized. Second, the fabrication parameters such as the deposition conditions have to be optimized to get the best molecular ordering and morphology. And third, synthesis of new materials provides more opportunities to various kinds of applications. While currently researches on OTFTs still focus on p-type semiconductors, the development of n-type semiconductors is expected and under investigation, shown in *fig. 1-2* [1.6]. The reliability, stability, and reproducibility are also important. There is still room for the fabrication technique to improve, and the choices of materials for the electrode, the insulator layer, even the substrate are also important issues. Finally, the interface treatment is an effective method for improving the characteristics of the device.

1.2 Device Fabrication Methods

The deposition of the semiconductor is the determining step of the OTFT fabrication. Today, the most common techniques that are used to deposit organic thin films are vacuum evaporation and solution processing methods such as solution cast, spin coating, spray coating,

and printing. So far, OTFTs fabricated by vacuum deposition remain having the best performance because very well-ordered structures can be obtained from the use of highly controllable deposition conditions. Although this technique is somewhat costly due to expensive equipment and low deposition throughput, it is appropriate for the deposition of molecular materials because a great number of which are not soluble. Solution processing methods such as solution-casting, spin-coating, and printing attract much attention because of their cost effectiveness. Soluble organic polymers and oligomers can be deposited by solution processing techniques. In such techniques, film formation takes place by evaporation of the solvent from a polymer solution. The thickness of films as small as 5~10 nm can be obtained by using dilute and low viscous solution. However, these solution processing methods have problems with film thickness and compositional uniformity. But when the solution processing technique is well handled, it will allow the production of homogeneous and good thickness-controlled films over large areas. What follows are the descriptions of deposition techniques.

Vacuum evaporation (including sublimation) is a technique to deposit high-purity films, and it belongs to physical vapor deposition (PVD). A schematic of a simple vacuum evaporator is shown in *fig. 1-3*, and a photograph of which is shown in *fig. 1-4*, Primordial material is placed on a tungsten boat which heats up when current passes through it. Individual atoms or molecules are produced by either sublimation of solid or evaporation of molten source. Since the evaporated molecules are transported through a high-vacuum environment, very little gas-phase scattering occurs. Therefore the mean free path of the vaporized molecules is very long, and they travel in essentially straight lines all the way from the source to the substrate surface without collisions in the space between the source and substrate. This process reduces gas-phase contaminants, and results in the high purity of the deposited film. The base pressure of the deposition system is an important deposition parameter because it determines the mean free path of the vaporized organic semiconductor

molecules and the presence of unwanted atoms and molecules in the vicinity of the substrate surface during the film formation. Typically, vacuum evaporation takes place in a gas pressure range of 10^{-5} to 10^{-9}Torr, depending on the level of contamination that can be tolerated in the deposited film. Deposition rate monitoring and control are relatively easy in vacuum deposition compared to the other techniques. Thin film morphology and the transport properties of OTFTs are influenced by substrate temperature, deposition rate, purity of the organic source material and substrate cleanliness. Organic thin films are intolerant to the various chemicals used in a typical lithographic process, so shadow masking is generally used to pattern the organic layer.

Spin-coating involves the acceleration of a small liquid droplet on a rotating substrate. *Fig. 1-5* shows a schematic of the spin coating process, and a photograph of a spin-coater is shown in *fig. 1-6*. The coating material (in solution form) is dropped on the center of the substrate. Then the substrate is spinning at a low speed to spread the solution over the substrate. It follows by a higher spinning speed to thin out the film and remove thick edge. Finally, the substrate is heated to remove the solvent and the film is therefore deposited. However, a requirement for this technique is a good solubility of the organic semiconductor.

1.3 Solution Processed Organic Semiconductor Films

The key feature that makes organic semiconductors attractive for low-cost manufacturing is the possibility for them to be deposited from spin coating, enabling very homogeneous films with perfect control of their thickness over a large area. Two methods have been usually used to fabricate OTFT devices. In the first method involves the use of a soluble material, either a conjugated polymer such as poly(3-alkylthiophene) (P3AT) [1.7] or precursor materials that can undergo subsequent chemical reactions to give the desired compounds, such as pentacene and poly(thienylene vinylene) [1.8-1.9]. In this method, low field effect

mobilities have been reported due to poor ordering and the amorphous nature of the semiconductor thin films. The second technique uses vacuum deposition of oligomers and organic materials of low molecular weights. High mobility of greater than 0.01 cm^2/Vs can be obtained with materials such as oligothiophenes, [1.10-1.13] copper phthalocyanine, [1.14] bis(benzodithiophene) [1.15], and pentacene,[1.16-1.17] which can form highly ordered and self-assembled films. It is clear that good ordering is necessary to achieve better transistor performance.

However, the technology that is believed to have the potential to produce the highest impact on manufacturing costs is the use of soluble organic semiconductors, both polymers and oligomers, combined with large area spin-coating or printing techniques that could eliminate lithography.

1.4 Motivations

Here we choose Poly(3-hexylthiophene) (P3HT) as the semiconducting layer in our research of OTFTs, because of the P3HT has many merits to act as the semiconducting layer in thin film transistors : (1) P3HT is solution processed, therefore can be processed by spin coating. (2) The addition of alkyl side-chains of P3HT enhanced the solubility of the polymer chains, [1.18] so that we can use different solvent such as toluene, xylene, and chloroform to fabricate our devices. (3) P3HT is a well-known polymer as an organic semiconductor and has shown the field-effect mobility from 10^{-4} cm^2/Vs in 1988 to 0.2 cm^2/Vs in 2003. [1.19-1.21]

In order to improve the large leakage current, we use a novel method called self-organized deposition process to reduce it. This method will not damage organic thin film. It's simply to define the active region through drop casting or spin coating, so we obtain the highest on/off current ratio (10^7) by suppressing leakage current. And we can manufacture this device at low temperature, and then we can apply this method on the plastic substrate as low

as 140^{O}C. There is potential on large area and low cost via this method, with drop casting or spin coating. The drop casting doesn't need the expensive equipments and is compatible with the roll-to-roll process which has advantages of large area, faster process, and low cost.

The other one of our motivation of this method is applied on other materials that can be dissolved or dispersed in solvent, such as the ZnO、F8T2、small molecules…etc. We could use this materials to manufacture sensors、organic/inorganic C-TFT, and ring oscillator via this novel self-organized process.

1.5 Organization of This Thesis

In chapter 1, we described our background and motivation of our research.

In chapter 2, we showed our experimental method to fabricate OTFT with RIE-Patterned method and Self-Organized Method on the plastic substrate in the first time.

In chapter 3, we fabricatied the structures including non-patterned OTFT, patterned active region OTFTs. In order to perform series experiments to optimize the dielectric parameter this was applied in our devices.

In chapter 4, Fabrication devices based on the self-organized patterned method. This method was applied on the other semiconductor materials like the pentance precursor, F8T2 and ZnO.

In chapter 5, we made some conclusions to this thesis.

Chapter 2
Novel Patterned Method of Soluble Materials for Fabricating OTFTs

2.1 Background

There are two kinds of contemporary OTFT structures. One is the called top-source-drain contact (TP) *[Fig. 2-1]* or top-electrode OTFT in which both source and drain contact pads are deposited on top of the active layer through a shadow mask. The other one is named bottom-source-drain contact (BC) *[Fig. 2-2]* or bottom-electrode OTFT in which drain and source contact metal is deposited and patterned on the gate dielectric prior to the active layer deposition. In general, the field effect mobility of top-source-drain contact (TP) OTFT is one order larger than bottom-source-drain contact OTFT. It attributes to the morphologies of active layer that is more disorder when the active layer is deposited on metal. The advantage of BC structure is the patterning process through conventional lithography technique. So we choose the bottom-source-drain contact structure in our experiment. An heavily doped n^+ type silicon wafer or metal is acted as the common gate electrode. Then source and drain metals are patterned by lift-off method via conventional lithography technique after forming the insulator. Finally the device is finished fabricating after depositing the P3HT active semiconductor layer.

How to pattern the organic semiconductor active layer in organic devices is very critical till to now. It is required in applications on flexible electronics [1-2]. Patterning the active layer not only can reduce the cross-talk between adjacent devices, but also can reduce the parasitic resistance and leakage current of the devices. As a result, the devices have better electrical performance than un-patterned ones. Leakage current is more obvious when OTFTs

share a common gate, in which case the leakage current goes through the gate dielectric and is collected by the whole P3HT layer to the drain electrode[3].

In this work, there are two ways for patterning the organic semiconductor films. One is the photolithographic patterning method *[Fig. 2-3]* which has been used by several groups [4-6]. It is a well established method that uses existing tools and processes what are commonly used within the inorganic semiconductor industry. A large area, high resolution lithography system that may be used for high volume, roll-to-roll production of organic electronic devices has been demonstrated [7]. Photolithographic patterning allows relatively complex circuits in which need multiple layers processes and modest alignment tolerances that are required to approach performance goals.

Another promising method is self-organized method *[Fig. 2-4]* for patterning the active region. In this method, the semiconductor solution is deposited by drop- casting or spin-coating and self-organized only in the desired area, therefore excludes material wasting and the subsequent active region patterning. Self-organized process for organic materials, such as certain regionregular polymers, and liquid- crystals polymers leads to superior performance in organic field effect transistors, photovoltaic cells, etc. which are candidates for the next generation of cost-effective optoelectronic materials. Molecular self-organization in soft condensed phases enables creation of novel functional materials with unique properties. Furthemorer, self-assembly process of organic nanostructures in solution leads to novel architectural concepts in optoelectronic applications. In this method, we chose two Self-Assembled Monolayers (SAMs) to modify the active region surface step by step. At first, we deposited the hexmethyldisilane (HMDS) SAMs, then deposited the second octadecyltrichlorosilane (OTS) SAMs. Here we also chose the different second SAMs , if the surface energy is different from the first one.

We need to consider about source/drain metals for obtaining an ohmic contact with P3HT that is an important issue for our devices due to the contact resistance between the

source/drain electrodes and the organic semiconductor. It also becomes increasingly important to device performance as the channel length decreases. Pt is a well-known material applied in OTFTs as the contact material because it is pretty stable in the air and its work function is match with P3HT. Therefore, we just change the material of adhesion layer and adjust its thickness to check its effect to the contact resistance and the drain current. However, Pt is hard to deposit on SiO_2 surface so that we needed to add an adhesion layer between Pt and SiO_2 interface, for example Cr or Ti adhesion layer because these two kinds of metal are not only noted for good adhesion to SiO_2 but also have similar work function.

Oxide surfaces are treated with some modification layer to improve the performance and adhesion between the polymer and the oxide surface, because the modification of the substrate surface prior to depose the regular P3HT has also been found to influence the film morphology so that we use different kinds of modification layer to discuss effect of this thin layer.

2.2 Device Fabrication of RIE-Patterned OTFTs

2.2.1 Device Structures

P3HT OTFTs are usually fabricated in either the coplanar or staggered geometry for bottom gate devices as shown in *fig. 2-2*. The staggered geometry called top contact device, is generally less susceptible to high contact resistance than the coplanar one (bottom contact device), because the effective contact area of which is much larger. However, there might be some physical damage when using sputtering system to deposit metal contact, or even some metal–semiconductor reactions to influence the contact resistance. The coplanar structure is desirable for its ease of fabrication and compatible with conventional lithography technique, so it is valuable to study the resistance properties of the different types of contact and

understand their role in the device performance.

Due to the reason mentioned above, so we fabricated our device with coplanar structure. The schematic diagram of the device in this chapter is shown in *fig. 2-5*. First, a thermal oxide layer with a thickness 1000 nm was grown in a furnace on an n+ type low-resistance wafer which acts as a common gate electrode. Afterwards, source/drain regions were defined using photolithography process. There are two kinds of layout for source/drain electrode, strip type and finger type as shown in *Fig. 2-6*. Finger geometry for the source/drain contacts is to minimize the device area and the associated gate to source/drain leakage current. The linear type: the channel length (L) is in a range of 10~50μm and the channel width is in a range of 300~1000μm. The finger type: the channel length (L) is in a range of 10~50μm and the channel width is in a range of 500~5000μm. Finally, the device is finished after spinning-coating the P3HT for active layer.

2.2.2 Process Flow of RIE-Patterned OTFTs

2.2.2.1 Process Flow of Non-Patterned OTFTs

1. Initial RCA cleaning
2. 100 nm field-oxide layer: furnace wet oxidation at 980 ℃
3. Mask #1: Source/Drain electrodes definition
4. Ti / Pt = 2 nm / 20 nm as the adhesion/electrode layer: Sputter system at base pressure = 2 × 10^{-6} torr; metals were deposited continuously without breaking vacuum
5. Photo Resistor (P. R.) lift-off to form source/drain electrodes: in acetone (ACE) with ultrasonic agitation
6. ACE + Isopropyl Alcohol (IPA) cleaning
7. Surface modification layer deposition

8. Spin-on P3HT: 0.5 wt. % P3HT in chloroform, 500 ~ 2000 rpm for 40 seconds, and then baking in a vacuum chamber at 120^{o}C for 45 minutes.

The descriptions above is shown in *fig. 2-7*

2.2.2.2 Process Flow of Non-Patterned Gate and Patterned Active Region OTFTs

1. Initial RCA cleaning
2. 100 nm field-oxide layer: furnace wet oxidation at 980 C
3. Mask #1: Source/Drain electrodes definition
4. Ti / Pt = 2 nm / 20 nm as the adhesion/electrode layer: Sputter system at base pressure = 2 × 10^{-6} torr; metals were deposited continuously without breaking vacuum
5. P. R. lift-off to form source/drain electrodes: in ACE with ultrasonic agitation
6. ACE + IPA cleaning
7. HMDS layer deposition
8. Spin-on P3HT: 0.5 wt. % P3HT in chloroform, 1000 rpm for 40 seconds, and then baking in a vacuum chamber under 120 ^{o}C for 45 minutes.
9. Spin-on passivation layer (PVP liquid : 2.67% PVP, 1.33% PMF, 0.8% PAG in three kinds of solvent: PGMEA, BuOH, and IPA), 1500 rpm for 30 seconds, exposing under 365nm UV light for 1 minute to make PVP cross linked and then baking in a vacuum chamber at 120 ^{o}C for 10 minutes.
10. Spin-on thick PR (AZ-4620) and patterned the active region as a hard mask.
11. HDP-RIE in an O_2 plasma etcher for the dry etching of PR, PVP and P3HT. (ICP RF Power: 500 W, bias RF Power: 100 W, process Pressure: 10 m Torr, O_2 : 40 sccm for 200 s)

The descriptions mentioned above is shown in *fig. 2-8*

2.2.2.3 Process Flow of Patterned Gate and Patterned Active Region OTFTs

1. Si-Wafer with 1000nm thermal oxide as buffer oxide
2. Ti / Pt = 2 nm / 20 nm as the gate adhesion/ electrode layer: Sputter system at base pressure = 2×10^{-6} torr; metals were deposited continuously without breaking vacuum
3. Depositing 100nm PECVD oxide.
4. Ti / Pt = 2 nm / 20 nm as the adhesion/electrode layer: Sputter system at base pressure = 2×10^{-6} torr; metals were deposited continuously without breaking vacuum
5. P. R. lift-off to form source/drain electrodes: in acetone (ACE) with ultrasonic agitation
6. ACE + IPA cleaning
7. HMDS layer deposition
8. Spin-on P3HT: 0.5 wt. % P3HT in chloroform, 1000 rpm for 40 seconds, and then baking in a vacuum chamber at 120 ^{o}C for 45 minutes.
9. Spin-on passivation layer (PVP liquid : 2.67% PVP, 1.33% PMF, 0.8% PAG in BuOH), 1500 rpm for 30 seconds, exposing under 365nm UV light for 1 minute to make PVP cross linked and then baking in a vacuum chamber at 120 ^{o}C for 10 minutes.
10. Spin-on thick PR (AZ-4620) and patterned the active region as a hard mask.
11. HDP-RIE in an O2 plasma etcher for the dry etching of PR, PVP and P3HT.
    (ICP RF Power: 500 W, Bias RF Power: 100 W, Process Pressure: 10 m Torr,
    O_2 : 40 sccm for 200 s)

The structure of patterned gate & patterned active region OTFTs is shown in *fig. 2-9*

2.2.3 Scanning Electron Microscope (SEM) Analysis

Fig. 2-10, *Fig. 2-11*, and *Fig. 2.12* showed OTFTs with patterned P3HT. In graph of *fig. 2-10*, we found that the position of channel was so far away from the edge of the residual polymer. The channel damage from sidewall was low influence. But it's too thick that can't

fabricate electrical circuit [*Fig. 2-11*], and there was likely merge with cross-linked PVP and P3HT. Even if after RIE etching, the cross-linked PVP was still on the P3HT film. The photo resist thickness is about 3.88um, PVP-PMF thickness is about 1.62um, and P3HT thickness is about 227nm.

2.2.4 Electrical Characteristics of OTFTs

2.2.4.1 Measurement

Current-voltage characteristics of OTFTs was measured under ambient with a semiconductor parameter analyzer HP4156C. All measurements were carried out in an electrically shielded box. The drain-source current, I_{DS}, was measured as a function of the drain-source voltage, V_{DS}, to observe FET-like characteristics. And I_{DS} was measured as a function of the gate voltage, V_G, at small drain-source voltage, which was constructed to determine the gate bias modulation of the FET conductive channel. Three parameters were extracted from the experimental I-V curves: (1) the threshold voltage (V_{th}), (2) the current modulation (the ratio of the current in the accumulation mode over the current in the depletion mode, also referred to as on/off current ratio), and (3) the field effect mobility (μ). The detailed extraction method will be discussed in the following section.

2.2.4.2 Extraction of On/Off Current Ratio, Mobility and Threshold Voltage

Devices with high on/off current ratio represent large turn-on current and small off current. It determines the gray-level switching of the displays. High on/off current ratio means that there are enough turn-on current to drive the pixel and sufficiently low off current when the device is turned off.

Mobility is an important parameter for carrier transport because it describes how strongly the motion of an electron or hole is influenced by an applied gate electric field. OTFTs are adequately modeled by standard field-effect transistor equations and the P3HT used in the present devices behave as a p-type semiconductor. When the gate electrode is biased negatively with respect to the source electrode (ground), OTFTs operate in the accumulation mode and the accumulated carriers are holes. Mobility could be extracted from the maximum transconductor (g_m) at V_D = - 40 V in our experiment.

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=\text{const}} = \frac{WC_i}{L}\mu V_D \qquad \text{..... [Equation 2-1]}$$

where L is the channel length, W is the channel width, Ci is the capacitance per unit area of the insulating layer, and μ is the field effect mobility.

The threshold voltage of an organic thin film transistor is also a very vital device parameter, since it is directly related to the power supply requirements. The interface between the dielectric and organic-semiconductor controls the transistor I-V characteristics. The density of charges trapped in the bulk and at the interface, as well as the mobile and fixed charges in the dielectric directly affects the threshold voltage. For a given dielectric thickness, the presence of higher charge results in a higher threshold voltage. This because the charge carriers get trapped and larger voltage is required to invert the semiconductor surface. Threshold voltage V_{th} can be extracted from the following equation.

$$I_D^{1/2} = \sqrt{\frac{1}{2}\mu C_i \frac{W}{L}}(V_G - V_{th}) \qquad \text{..... [Equation 2-2]}$$

Using linear fitting of the plot $I_D^{1/2}$ vs. V_G in saturation region to from the slope and the horizontal axis intercept at point A, which was the extracted threshold voltage (V_{th} = V_G at $I_D^{1/2}$ =0)

2.2.4.3 The Electrical Characteristics Comparison of All Kinds' Structures

The distortion of the I–V curves in the linear region because of the I_D offset can be clearly seen. The gate induced leakage (i.e. the gate current) (I_G) increases with gate bias and is much higher at lower V_{DS} and peaks at V_{DS} = 0 V *[Fig. 2-13 (a) and (b)]*. These kinds of OTFTs share a common gate and a common active layer so that there were many current paths from drain to gate that result in large gate leakage current. The I_D-V_D curve of patterned active layer OTFT was shown in *fig. 2-13 (c) (d)*. The electrical characteristics of the patterned P3HT device was represented in the *fig. 2-14(a)* show an OTFT with low gate induced leakage current. While the I_D offset is reduced significantly, the drive current for the transistor is comparable to the non-patterned devices.

We suggest that the major source of I_D offset is the effective expansion of source/drain electrodes from the un-patterned P3HT conducting accumulation layer. By patterning the P3HT film, I_D offset in OTFT can be reduced significantly. Patterning the P3HT film and limiting the film to the channel area eliminates a large source of I_D offset.

We measured the I_{ON}/I_{OFF} ratio, mobility and threshold voltage of conventional, patterned P3HT device without patterned gate and patterned P3HT device with patterned gate shown in *table 2-1*. Patterned Gate & Patterned Active Layer OTFT electrical characteristics were degraded compared to the non-patterned gate with patterned active layer one. The possible reason was that there was very rough surface before P3HT coating, leading to P3HT could not arrange well on the surface. Several reports have indicated that P3HT polymer is sensitive to the presence of oxygen [8-9]. It has been shown that oxygen is a kind of doping for P3HT polymer. Moreover, if there are oxygen atoms in P3HT polymer, carriers scattering would occur and the field-effect mobility would decrease. Since our P3HT OTFTs were not fabricated in vacuum, the influence of oxygen to the characteristics of organic transistors is inevitable.

Fig. 2-14(b) shows the decrease in accumulation capacitance with an increase in frequency for an undoped material. This is believed to be at least partly associated with the

transit time for a majority carrier to the interface from either the back of the film or along the accumulated interface. Of particular importance in these plots is the value of flat band voltage, which is in all cases close to zero.

High oxide leakage currents have been observed in MOS capacitors as a result of polymer deposition. The current increased further with an increase in polymer film thickness and also with increase in percentages of 3 times. This oxide current is believed to be due to the displacement of dopant ions or impurities present in the polymer film. [20]

2.3 Critical Issues for Fabrication OTFTs on Plastic Substrates

2.3.1 Mask Alignment

A conventional plastic substrate has high thermal expansion coefficient that is about one order of magnitude larger than silicon and glass substrates. This feature makes mask alignment and thin-film patterning very difficult in layer by layer during the pre-baking and post baking processes of photolithography. In addition, the difference between expansion and contraction of the conventional plastic substrate due to water absorption becomes more than 3000ppm. *Fig. 2-15* depicts variations of substrate length during the actual OTFT process [10]. By controlling the temperature and humidity of the OTFT process, the maximum allowance of the mask alignment can decrease to 1000ppm. However, a conventional OTFT array structure requires alignment allowance within ±15ppm. Thus, mask alignment in each layer is one of the most serious problems to fabricate precise OTFT structure on the plastic substrate.

2.3.2 Thermal-Mechanical Problems with Plastics

If the thermal expansion coefficient α_s of a substrate differs from the thermal expansion α_l of a layer on that substrate, then the overall tension α_{tot} in the layer, including its intrinsic tension α_i at room temperature T_R, changes for a process temperature T_P to [11]:

$$\alpha_{tot} = \alpha_i + (\alpha_l - \alpha_s)(T_P - T_R)E_l/(1-\nu_l) \quad \text{[Equation 2-3]}$$

where E_l stands for the modulus of elasticity and ν_l for the Poisson's ratio of the layer. As a rule, when $\alpha_l < \alpha_s$ and $T_R < T_P$, result in a decrease in α_{tot}, indicating an additional compressive stress. This stress may lead to crack or delaminate in the layer and also result in a curvature of the substrate with the radius R valid for $E_s d_s$ much larger than $E_l d_l$.

$$R = \frac{E_s d_s^2}{6 d_l \sigma_{tot}(1-\nu_s)} \quad \text{[Equation 2-4]}$$

In Equation 2-4, *Es* is the modulus of substrate elasticity, d_s *is* the thickness of the substrate, ν_s *is* the Poisson's ratio of the substrate, d_l *is* the thickness of the layer, and is α_{tot} taken from equation 2-3. For silicon wafer, $E_s d_s >> E_l d_l$, the radius is so large that the substrate remains planar. However, for flexible plastic substrate with thickness is only 100 ~ 200 μm and with a relatively low Young's modulus, serious bending of the substrate may occur after multiple thin-film deposition, such as P3HT, ZnO ,and F8T2 dip casting curing in the process temperature of 140~200 ^{o}C. General manufacturing equipments could not handle the wrapped substrate, much less fabricating the OTFT.

2.3.3 Plastic Substrate and Their Properties

Direct fabricating OTFTs on plastic substrate has many problems. These problems mostly arise from the unique physical and chemical properties of plastics. Polymeric substrates applied in displays are polycarbonate (PC), polyarylate (PAR), polyimide (PI), poly(ethylenterephtalate) (PET), poly(estersulfone) (PES), and polyolefin, etc. *Tables 2-2* lists general requirements of plastic substrate for LCDs [12] and *Table 2-3* summaries substrate

properties for organic polymeric backplanes specially synthesized for display fabrication [13]. From these tables, one can find that the major differences between plastics are the Young's modulus, melting/glass-transition temperature, thermal expansion coefficient and thermal conductivity; some plastics even have native color. Since the strain is inversely proportional to the Young's modulus of the substrate, deformation for these flexible plastic materials could be easily observed and requires delicate post treatments.

2.3.4 The Choice of the Plastic Substrate

Some of the important features of PET film were listed below:

1. High total light transmittance above 89%
2. Coefficient of thermal expansion about 15ppm /℃
3. Very low water absorption of 0.14%
4. Good adhesion to layers such as hard coating, printing inks and ITO, etc.

Moreover, the transmittance and reflectance of glass, PC, PET and ARTONTM films were illustrated in *fig. 2-16*. The thicknesses of these plastics were all about 200μm.One can find the transmittance of PET is good while the reflectance was the lowest among those plastic substrates, and its performance is even better than glass. Additionally, the PET film has good resistance to most chemicals used in the semiconductor fabrication such as ACE, IPA, TMAH (developer), KOH, HF, etc .and moderate resistance to HNO3 (becoming slightly yellowish after immersion in it for a long time). Although the requirements for plastic substrates in the process are not strictly constrained, we still chose PET film as the substrate in this work.

2.3.5 Polymer Dielectric

The dielectric systems discussed above have all been part of bottom gate devices. Deposition of inorganic dielectrics would be difficult on top of the organic active layer. The

surface treatments employed on inorganic would be practically impossible to use in top gate devices. Organic dielectrics, however, offer the freedom to build both top and bottom gate devices by the use of solution coating techniques and printing.

Solution-process enable easiness for applications in electronics, the resulting films exhibit good characteristics simply by spin-coating, printing, or dip casting at room temperature under ambient conditions. Of course, gate dielectrics are not an exception. Furthermore, this capability has practical merits when couple with low-cost patterning techniques for dielectric and for other materials needed for TFT fabrication. From this point of view, polymer dielectrics really have great application potential.

However OTFTs with both the semiconductor and the insulator are polymers have shown limited success in contrast. An inherent problem in the fabrication of these polymer TFTs is that the polymer semiconductor layer on an insulating layer can get damaged when the other layer is spin-coated onto the existing, underlying layer for the fabrication of the transistor.

Poly (4-vinylphenol) (PVP), as shown in *fig. 2-17*, is one of the most popular gate insulator materials. OTFTs with PVP gate dielectric and opaque noble-metal source/drain contacts showed a pretty good performance. However, the gate dielectric capacities of the polymer gate dielectric are still inferior to those of inorganic dielectric materials. Moreover, sensitivity to gate bias stress in OTFTs with the polymer dielectric, resulting in threshold voltage shift depending on the direction of gate voltage sweeping, has been often found and reported[14]. Cross-linked PVP is that PVP blends with some cross-linking agent and then treats with UV light or thermal curing to make PVP cross-linked. Cross-linked PVP is insoluble in common solvents, and it could be patterned using standard microelectronic etching methodologies, moreover, it has a pretty good mechanical strength and flexibility so that it is one of the prospective materials as gate dielectric. Few studies reported the reasons of the threshold voltage shift and the unreliable behavior of OTFTs with organic dielectrics

[15]. Hence, no report has mentioned about optimum PVP curing conditions for cross-linked of polymer chains, which may substantially influence the electrical properties of polymer gate dielectric films and further influence the reliability of the OTFTs with polymer gates.

2.4 Device Fabrication of Self-Organized TFTs on the PET Substrate

2.4.1 Process Flow of Self-Organized TFTs

1. PET substrate adhesion on the silicon wafer with vacuum tape.
2. Substrate cleaning with deionized (DI) water
3. Deposition Ti / Pt = 2 nm / 20 nm as the gate adhesion/ electrode layer: Sputter system at base pressure = 2×10^{-6}torr; metals were deposited continuously without breaking vacuum
4. Spin-on dielectric layer (PVP liquid : 8 wt% PVP, 4 wt% PMF, 2.4 wt% PAG in the solvent of PGMEA), 1000 rpm for 60 seconds, exposing under 365nm UV light for 1 minute and then baking in a vacuum chamber under 120 ^{o}C for 10 minutes to make PVP cross linked.
5. Ti / Pt = 2 nm / 20 nm as the adhesion/electrode layer: Sputter system at base pressure = 2×10^{-6}torr; metals were deposited continuously without breaking vacuum
6. P. R. lift-off to define source/drain electrodes: in ACE with ultrasonic agitation
7. ACE + IPA cleaning the surface.
8. The first HMDS SAMs growth in a high temperature (150^{o}C) and low pressure (lower than 20 torr) in oven which was full of HMDS steam.
9. Spin-on photo resist (FH6400), 1000 rpm for 10 seconds, then 4000rpm for 30 seconds (uniformity and thickness consideration) and lithography (with active region mask)
10. HMDS removing from surface excluding active region with PDC-3XG O_2 plasma, the

power about 5.4 Walt.

11. Growth the second OTS SAMs: putting the sample and 1 ml OTS liquid in a negative-pressure box in R.T for 45 minutes and then baking in vacuum chamber (100 ^{o}C for 1 hour).
12. P.R removing by A.C.E with wet striping.
13. Dip casting P3HT: 0.5 wt. % P3HT in DCB solvent, and then baking in a vacuum chamber under 120 ^{o}C for 1 hour.

We can simply present this process with diagrammatic process flow in *fig. 2-18*

2.4.2 Physical Properties of TFTs

2.4.2.1 Optical Microscopy Images

In the optical microscopy, we took four pictures shown in *fig. 2-19*, *fig. 2-20* *fig. 2-21*, and *fig.s 2-22(a)(b)* which proved some obvious phenomenon in these images. *In fig. 2-19*, the device was fabricated on the PET substrate plastered on silicon wafer by vacuum tape. The silicon wafer (holder) could be re-used, if we want to manufacture the device again. This is for cost down and environmental consciousness. *Fig. 2-20* shows the PET substrate which was bended 180 degree. The curvature is an important parameter for flexible substrates. The flexible PET substrate can be applied on the tech. clothes, RFID card and flexible electronic newspapers. *Fig. 2-21* shows the image of P3HT OTFT device clearly with self-organized method. The P3HT polymer was deposited self-organizingly where the active region was with lower surface energy. The reason for self organization will be discussed physically with surface energy later.

2.4.2.2 AFM and SEM Analyses

In the AFM images, *fig. 2-23* showed that the polymer were assembled at the edge of the active region. The possible direction of self-organization is from center to the edge. The vertical distance of green dot is 90.726 nm and red dot is 66.742 nm. The gap of two dots is 23.258 nm. We could also analysis the phenomenon from SEM images. The tilt view and top view of the device (*fig. 2-25, fig. 2-24)* show that the P3HT film on the cross-linked PVP dielectric was confined at the edge of active region.

2.4.2.3 The Thickness and Roughness of PVP and P3HT

The thickness of PVP and P3HT are 635nm and 81nm *[Fig.s 2-26 (a), (b)]*. Cross-linked PVP dielectric constant is 4.1, so that the dielectric capacitance is calculated by the formula: $C_{PVP} = \varepsilon x \varepsilon_0 x t_{pvp}$ (f/cm^2). It is believed that the conducting channel in OTFTs is confined to a few monolayers at the organic dielectric interface [16]. Studies on pentacene-based devices showed 0.9 and 2–3 nm accumulation layers depending on the dielectric and the applied gate bias [17-18]. Even though working OTFTs have been made with a monolayer of P3HT, the semiconductor layer in most OTFTs has a thickness ranging from a few tens of nanometers to hundreds of nanometers which is much larger than the accumulation layer thickness [19]. The roughness of PVP and P3HT are few nanometers *[Fig. 2-27, 2-28]*. It is obviously to be observed that film deposited on the PET substrate leads to a rough surface. It might be the adhesion of the adhesion titanium metal gate layer is not as well as that on the silicon wafer.

2.4.3 Electrical Characteristics of OTFTs on PET Substrate

According to these measurements, the Self-Organized TFTs exhibited superior electrical characteristics to those of other active layer patterned OTFTs on the plastic substrate *[Fig.s 2-29, 2-30]*. The measured device's width (W) is 1000um and channel length (L) is 25μm, This Self-Organized device's is about 5.73×10^{-3} cm^2/V-s. The threshold voltage is about

2.66V (V_{DS}=40V). The V_{th} is low and could be applied in the some low power consumption electronic products. The I_{ON}/I_{OFF} ratio is $2.04x10^4$ (A/A). And organic polymer is easier doped by oxygen molecules under ambient. The I_{ON}/I_{OFF} ratio of all recent cross-linked PVP dielectric OTFTs researches is from 10^3 to 10^4, and our results could be compared with other ones.

2.4.4 Energy Dispersive Spectrometer (EDS) Mapping Analysis

In order to observe whether the P3HT molecule deposited self-organizingly only in active region corresponds to the previous report or not. The EDS mapping was used to confirm it. *Fig. 2-32*, *Fig. 2-33* showed the EDS mapping result of self-organized method. The chemical structure of the P3HT had been shown in *Fig. 2-34*. In P3HT skeleton, it shows the chemical formula with $C_{10}H_{14}S$.

Because of PVP and P3HT molecules also contain carbon and hydrogen atoms. The P3HT molecules contain sulfur atoms, but the PVP molecules don't contain it. That is the difference between the P3HT and PVP molecules. So the EDS spectroscopy was used to detect the sulfur(S) distribution among the PET substrate. *Fig. 2-31* showed the SEM image of the Self-Organized TFTs. Two reference blocks region were selected, one was inside the active region *Fig. 2-31(a)* and the other one was outside the active region *[Fig. 2-31(b)]*, and then EDS analysis was performed to reveal the component of the element within the block region. The signal of sulfur(S) atom was detected inside the active region and fitted automatically by computer program, *Fig. 2-32* showed the relative abundance of sulfur distribution. *Fig. 2-33* showed the EDS analysis outside the active region. The result indicated that no sulfur atoms existed outside the active region.

Chapter 3
Different Structures of Self-Organized Organic/Inorganic TFTs

3.1 Background

Patterning of liquid films using nonlithographic techniques has attracted interest due to lower cost and better suitability to devices made of organic or inorganic which can be dissolved in the solvent [3.1]. Liquid patterning is essential for fabrication of electronic devices, optical storage media and mechanical devices [3.2]. Additionally, liquid patterning is important for improving the practical performance of micro-nanomechanical devices.

In this chapter, we discussed the different kinds and thickness of thermal oxides to see what do they affect the performance of the P3HT OTFTs. Then we optimized the dielectric deposition parameters to obtain the better electric characteristics for further electrical circuit application.

3.2 Non-Patterned Gate and Patterned Active Region Self-Organized OTFTs

How to pattern the organic semiconductor active layer in organic devices is a really critical issue. It is required in applications such as flexible color displays or polymer/organic light emitting diode displays or backlight [3.3-3.4]. The purpose of patterning the active layer is to reduce the leakage currents, crosstalk between adjacent devices, and unwanted parasitic capacitance, these led to not only a higher circuit operating speed but also better performance characteristics (I_{ON}/I_{OFF} ratio, for instance). Patterning the active region is even more

important to self-organized OTFTs when they shared a common gate, in which case the leakage through the gate dielectric is more significant [3.5]. Several methods of patterning small molecules can be seen in the literature, ex, deposition through a shadow mask [3.6], integrated shadow mask [3.7], or patterned growth [3.8]. However, these kinds of patterning methods could not be applied to polymer semiconductor OTFTs because the polymer semiconductor's un-evaporation physical quality under vacuum. Here we used the spin-coating technique to deposit the active layer of Self-Organized OTFTs instead of vacuum deposition which was comparable with the patterned technology through shadow mask. Furthermore, one of the most common methods for patterning OTFTs consisted of either a water-soluble resist or a protective parylene layer followed by a regular photoresist on top of the polymer, which was acted as an etch mask. Subsequently the polymer layer is etched by oxygen plasma. [3.9-3.10]

In this thesis, we employed a self-organized patterning process for P3HT OTFTs. The process described in this thesis could also apply to other organic semiconductors and we discussed in Chap. 4. One of the handicaps of this process was the observed degradation of the photolithographically patterned transistor performance. Recent reports showed a mobility of 6.1 x 10^{-3} cm^2/V s and 10^{-5} cm^2/V s for the photolithographically active layer patterned pentacene and P3HT OTFTs, respectively [3.11-3.12]. Considering a typical mobility of 0.1 cm^2/V s and 0.01 cm^2/V s for un-patterned pentacene and P3HT OTFTs, respectively [3.13–3.16], there were more than two orders of mobility degradation after the patterning process. Therefore, we focused on not only how to develop a low cost and convenient process that is compatible with inexpensive plastic substrates but also the electrical characteristic enhancement of OTFT devices such as mobility, I_{ON}/I_{OFF} ratio, and operating frequency etc.

3.2.1 Process Flow

1. Initial RCA cleaning
2. 100 nm thermal-oxide layer: furnace wet oxidation at 980 C
3. Ti / Pt = 2 nm / 20 nm as the adhesion/electrode layer: Sputter system at base pressure = 2 $\times 10^{-6}$ torr; metals were deposited continuously without breaking vacuum
4. P. R. lift-off to form source/drain electrodes: in ACE with ultrasonic agitation
5. ACE + IPA cleaning
6. HMDS modification layer growth in a high temperature (150^{o}C) and low pressure (lower than 20 torr) oven which was full of HMDS steam.
7. Spin-on passivation layer for active region with lithography (active region mask) via photo resistance FH6400, 1000 rpm for 10 seconds to be uniform and 4000rpm for 30 second to control thickness about 1 μ m.
8. HMDS removing from surface excluding active region with PDC-3XG O_2 plasma with power of 5.4 Walt.
9. To grow OTS modification layer, we put the sample and 1 ml OTS liquid in a negative-pressure box in R.T for 45 minutes and then baking in vacuum chamber (100^{o}C for 1 hour).
10. P.R removing by A.C.E with wet striping.
11. Dip casting of P3HT with 0.5 wt. % P3HT in DCB solvent, and then baking in a vacuum chamber under 120 ℃ for 1 hour.

We can simplify this process to diagrammatic process flow in *fig. 3-1.*

3.2.2 Scanning Electron Microscope Analysis

Here showed the images of devices with the patterned active regions via this self-organized method on the thermal oxide. The channel length is about 10um *[Fig.3-2]*. The evaporation mechanism of the solution is from center to sidewall. And the average P3HT

thickness on the channel is about 80nm *[Fig. 3-3 (a)]*. Even if the scale is to 200nm, the thickness outside the active region is to be close to zero. *[Fig. 3-3 (b)]*

3.2.3 Electrical Characteristics Analysis

Fig. 3-4 showed the transfer characteristics of two P3HT OTFTs, one was without active region patterning and the other was with active region patterning. The non-patterned P3HT device showed the I_{ON}/I_{OFF} ratio of 10^3. After patterning the active region, the I_{ON}/I_{OFF} ratio was dramatically improved from 10^3 to about 10^7 because of the reduction of the P3HT film coverage, which was confined only between the source/drain electrodes. The mobility of patterned Self-Organized OTFT was slightly increase from 0.00038 to 0.00279 (cm^2/V-s) compared with non-patterned one. The characteristic of these two OTFTs was listed in *table 3-1*.

3.2.4 Modification of Oxide Surface

The SAM modification on the SiO_2 gate dielectric surface improved the molecular ordering of semiconducting layer in OTFTs, leaded to a significant improvement in transistor performance. Similarly, the mobility of P3HT TFTs has also been reported to improve by orders of magnitude upon modification of the SiO_2 gate dielectric substrate by hydrophobic SAM, possibly through lowering of the surface energy of the gate dielectric and removal of residual surface water and other polar groups prior to deposition of the polymer [3.17], or by inducing microstructure changes through specific interactions with functional groups of the polymer [3.18]. Molecular ordering in semiconductors can be manipulated to vary degrees through controlled solvent evaporation [3.19], post-deposition annealing [3.20], and substrate surface chemistry [3.21–3.24]. For example, modification of the gate dielectric surface with HMDS, as shown in *fig. 3-5(a)*, led to improved OTFT performance [3.25]. The nature of

these groups apparently attracts the hexyls side chains of P3HT heat to tail (HT) in electrical structure and transport. Similarly, a significantly higher mobility of F8T2-TFTs was obtained using a dielectric surface modified with OTS, as shown in *fig. 3-5(b)* [3.26]. Because of these reasons, in our research, we discuss two conditions of different modification layers as below: 1. HMDS layer; 2. O_2 plasma treatment add OTS layer. There are HMDS layer on oxide surface after source/drain deposition duo to the process of lithography, so the purpose of O_2 plasma treatment is to destroy the HMDS layer and remove other chemicals on the oxide surface.

The detail experimental method was described below: HMDS molecules were chemically bonded with the hydroxyl groups on the oxide surface in a high temperature (150 ^oC) and low pressure (lower than 20 torr) oven which was full of HMDS steam. In order to remove the HMDS from the process of lithography, we employed O_2 plasma for ten minutes to make the surface of SiO_2 clean and without any organic chemicals. To grow OTS modification layer, we put the sample and 1 ml OTs liquid in a negative-pressure box in R.T for 60 minutes and then baking in vacuum chamber (100 ^oC for 30 mins).

Fig. 3-6 showed that the I_D-V_G curves of OTFT with different modification layer. We found that if we treat the surface with O_2 plasma, V_{th} shifted to positive apparently. We thought that if we did with O_2 plasma treatment, P3HT not only arrange well on the channel region but on the top of source and drain, leading to larger leakage current from the bulk. In order to get lower leakage current, we only treated with HMDS to improve adhesion and regioregularity between the polymer chain and the oxide surface [3.27]. After treating SiO_2 surface with HMDS, the hydroxyl groups at the oxide surface would be replaced by methyl groups and the polar nature of these groups apparently attracts the hexyls side chains of P3HT, favoring lamellae with an edge-on orientation.

The modification OTS molecules with long alkane chains provided the higher driving current, [3.28] which allowed them to interact with similar features in the structure of P3HT

via induced dipole dispersion forces. The alkane chains in OTS extend perpendicularly to the SiO_2 surface. However, there must be HMDS layer on oxide surface after S/D deposition duo to the process of lithography. So the OTs layer had to be deposited after O_2 plasma treatment to destroy the HMDS layer. This process causes higher leakage current and also suppresses the I_{ON}/I_{OFF} ratio. If we deposit OTS layer on HMDS layer, the I_D-V_G curves showed two steps of increasing current because of the different modification layer on the oxide surface.

3.3 Patterned Gate and Patterned Active Region Self-Organized OTFTs

3.3.1 Process Flow

1. Silicon Wafer with 500nm thermal oxide as buffer oxide
2. Deposition Ti / Pt = 2 nm / 20 nm as the gate adhesion/ electrode layer: Sputter system at base pressure = 2×10^{-6} torr; metals were deposited continuously without breaking vacuum
3. Depositing 100 nm PECVD oxide.
4. Deposition Ti / Pt = 2 nm / 20 nm as the S/D adhesion/ electrode layer: Sputter system at base pressure = 2×10^{-6} torr; metals were deposited continuously without breaking vacuum
5. P. R. lift-off in ACE with ultrasonic agitation and then the residual Pt metal formed the source/drain electrodes.
6. ACE + IPA cleaning
7. HMDS molecules growth in a high temperature (150 ^{o}C) and low pressure (lower than 20 torr) oven which was full of HMDS steam.
8. Spin-on passivation layer for active region with lithography used photo resistance FH6400, 1000 rpm for 10 seconds to be uniform and 4000 rpm for 30 second to control thickness

about 1 μ m.

9. HMDS removed from surface excluding active region with PDC-3XG O_2 plasma, the power about 5.4 Walt.
10. To grow OTS modification layer, we put the sample and 1 ml OTS liquid in a negative-pressure box in R.T for 45 minutes and then baking in vacuum chamber (100 ^oC for 1 hour).
11. P.R removing by A.C.E with wet striping.
12. Dip casting P3HT with 0.5 wt. % P3HT in DCB solvent, and then baking in a vacuum chamber under 120 ^oC for 1 hour.

We can simplify the step process to diagrammatic process flow in *fig. 3-7*

3.3.2 Scanning Electron Microscope and Energy Dispersive Spectrometer Mapping Analyses

Here showed the images of active layer and gate patterned self-organized OTFTs on the PECVD oxide. The evaporation mechanism of solution is from center to sidewall, and sidewall was thicker than the middle *[Fig. 3-8]*. P3HT thickness on the channel is about 87nm *[Fig. 3-9]*.

In order to determine whether the P3HT film was confined in active region corresponds to the previous report or not, function of EDS mapping was used to confirm it. *Fig. 3-11*, *Fig. 3-12* showed the EDS mapping result of self-organized method. The chemical structure of the P3HT was shown in *fig. 2-34*. In this fig., the P3HT chemical formula is $C_{10}H_{14}S$.

The function of EDS was used to detect the sulfur(S) and carbon(C) distribution on the SiO_2 surface. *Fig. 3-10(a)* showed the SEM image of the self-organized TFTs. A reference block region was selected to across the active region and outside active region *[Fig. 3-10(b)]*, and then EDS analysis was performed to reveal the element component inside the block

region. The signal of sulfur(S) and carbon(C) elements was detected and fitted automatically by computer program. *Fig. 3-11* showed the relative amount of sulfur distribution. *Fig. 3-12* showed the EDS analysis outside active region. The result indicated that no sulfur atom existed.

3.3.3 Electrical Characteristics Analysis

Fig. 3-13 showed the transfer characteristics of two OTFTs. Both of OTFTs W/L was 1000um/10um, one was patterned with RIE system and the other one was with this self-organized method. We had been discussed about the oxygen influence for P3HT lifetime with RIE etching by oxygen plasma. And the leakage current of the RIE patterned device will be serious increased. The I_{ON}/I_{OFF} ratio of the device was both about 2×10^4. But the mobility of Self-Organized OTFTs was increase from 0.00014 to 0.00075 (cm^2/V-s). The characteristic of these two OTFTs was listed in *Table 3-2*. In this electrical characteristic analysis, there is an issue of OTFTs dielectric. The dielectric can't afford high voltage. We will discuss and optimize in the next section.

3.4 Dielectric Optimized for OTFTs Applications

The experiment for dielectric optimization was to realize electrical circuit application. We have four oxide deposition parameters. There were different PECVD (SiH_4+N_2O at 300 ^OC) oxide thicknesses with 100nm, 200nm and 300nm. *[Fig. 3-13 ~ Fig. 3-15]*

3.4.1 Breakdown Mechanism

The breakdown phenomenon determines the highest applicable voltage and limits the power-handling capacity of the devices. Therefore, breakdown voltage is as important as

transconductance or threshold voltage in OTFTs. A briefly introduction will be made to the mechanisms of avalanche breakdown, gate oxide breakdown and punch-through breakdown.

Avalanche breakdown: when the drain of an OTFT is biased at high voltage (negative voltage for V_D), a high electric field is built up in the depletion region at the junction between channel and P3HT bulk drift region. Carriers in the depletion region, either thermally generated or drift current from channel region, gain kinetic energy from the electric field. If the field is sufficiently high, these energetic carriers can create new electron-hole pairs by impact ionization. The newly created electrons and holes also gain kinetic energy from the electric field and create additional electron-hole pairs. These electrons and holes in turn create other electron-hole pairs through the same way. This carrier-creating process is called avalanche multiplication. Eventually, device breakdown occurs due to the high current result from this avalanche multiplication. *Fig. 3-18* shows an OTFT transistor operated at V_G= -25, V_D=0V, which is a near breakdown condition. The maximum impact ionization generation rate is taking place near the silicon surface under bird's beak.

Gate oxide breakdown: Gate oxide breakdown is possible if the gate bias is pushed beyond the supply voltage limit. The typical value of electric field that gate oxide can withstand is around 10 MV/cm. If the electric field in the gate oxide exceeds this value, a leakage path may appear and cause device breakdown. Gate oxide breakdown is a destructive process. Once it occurs, device is destroyed.

Punch-through breakdown: punch-through is a phenomenon associated with the merging of the source and drain depletion regions in the OTFT. Once punch-through occurs, any increase in the applied drain voltage will lower the potential energy barrier for majority carriers in the source. With the lowering of the barrier, carriers can be easily injected in to the channel region and collected by the drain. Thus, an increase in drain current with increasing drain voltage is observed. Device under this condition referred as punch-through breakdown.

3.4.2 Electrical Characteristics Analysis with Different Oxide

The gate bias applied to an OTFT can vary from -40V to 40V or more depending on its various applications. With this wide range of applied voltages, it is obvious that a single gate oxide thickness may not equally meet the requirement of all these applications. For this reason, OTFT with different gate oxide thickness are fabricated for different levels of gate bias. All measurements were performed on OTFTs with W/L=1000/10 under room temperature. *Fig. 3-17* and *Fig. 3-18* showed the breakdown characteristics of devices with different gate oxide thickness. An approximate expression for the breakdown voltage is given by [29], which can be used to qualitatively understand the correlation between breakdown voltage and gate oxide thickness:

$$V_{BD} = \varepsilon_s E_{cr} \left[\frac{E_{cr}}{2qN_d} + \frac{1}{C_{ox}} \right] \quad \text{[Equation 3-1]}$$

E_{cr} is as critical electric field of avalanche breakdown. V_{BD}: V_G of the point at which I_D reaches 50uA when V_D= -25V. The only term related to gate oxide thickness is Cox. As discussed earlier, Cox decreases with thicker gate oxide thickness. Thus, as depicted in the equation, device with thicker gate oxide has higher breakdown voltage. As gate oxide thickness increases, gate capacitance per unit area (Cox= ε_{ox}/t_{ox}) decreases. *Fig. 3-19* shows the I_D-V_G characteristics of different gate oxide thickness measured at V_D = -40V. The decrease in transconductance is caused by the same mechanism that degrades drain current in thicker gate oxide. Also shown in the fig. is a shift in the characteristic curves. This implies a different threshold voltage in different gate oxide thickness. As mentioned earlier, the threshold voltage of an OTFT can be expressed as:

$$V_{th} = \phi_{ms} + 2\phi_f + \frac{\sqrt{2\varepsilon N_A \cdot 2\phi_f}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \quad \text{[Equation 3-2]}$$

ϕ_{ms}：Work function difference between metal and silicon

$q\phi_f$：Energy difference between Fermi level & intrinsic Fermi level

As gate oxide thickness increases, gate capacitance per unit area ($Cox= \varepsilon_{ox}/t_{ox}$) decreases. Consequently, V_{th} increases with increasing gate oxide thickness. *Table 3-3* shows measured V_{th} increases with gate oxide thickness.

3.4.3 Atomic Force Microscope (AFM) Analysis

The AFM graphs with different thicknesses of oxides were shown in *fig. 3-20 (a) (b) (c)*. As gate oxide thickness differed, the variation in the vertical electric field was responsible for all the changes in parameters. The edge of 100nm thick gate oxide was 121.03nm high, so that there will induce to a large electric field in the edge protrusion region. That led to an easier oxide breakdown source when applied gate bias. Finally, the optimum oxide thickness for application was a critical issue. The gate oxide thickness of 300nm can be employed in driver circuits where the high stability was obtained with applying high gate bias.

3.5 The Surface Energy Calculating Via Contact Angle Measurements

The sessile drop contact angle method with two different probe liquids *[Table 3-4]* was used to measure the surface energy of HMDS and OTS SAMs treatment oxide surface. Probe liquids (10 µl, 0.010 ml) were transferred with a micropipette onto the oxide and Pt electrode surfaces with different SAMs treatment. Two seconds after placement of the liquid droplet, a digital (pseudo static) image of the droplet was captured utilizing a computer-based digital image acquisition card (frame grabber) and a charge-coupled device (CCD) camera. Using the digitally recorded images, the contact angles of the drops on both sides (left and right) were measured and averaged with digital image analysis software *[Fig. 3-21]*. Each drop was placed on a wafer portion of a growth ring on the tangential surface for HMDS and on the other surface for OTS. After each drop, the experimental strips were moved to obtain a new

surface under the pipette tip for repetitive measurements (Shen et al. 1998). The Good-Girifalco (geometric mean) and Chang equations were used to calculate the surface energy of HMDS and OTS treatment composite surface (Gardner et al. 1999).

$$W = (1+\cos\theta)\gamma_L = 2[(\gamma_L^D \times \gamma_S^D)^{1/2} + (\gamma_L^P \times \gamma_S^P)^{1/2})] \ldots\ldots \text{[Equation 3-3]}$$

where: θ = contact angle,

γ_L = surface tension of the liquid (mJ/m^2),

γ_s = surface energy of the solid (mJ/m^2),

d = non-polar (dispersive) component of surface energy,

P = polar component of surface energy.

The average measured contact angles obtained from different HMDS and OTS SAMs treatment surfaces utilizing a series of probe liquids were summarized in *Table 3-5*. In general, the HMDS treatment surface, an organometallic preservative, resulted in an increase in contact angles of water (74.8 ^{0}) and diodomethane (59.4 ^{0}) compared with the bared oxide surface ((water (61.5 ^{0}) and diodomethane (53.9 ^{0})). This was expected due to the different physical and chemical characteristics of both surfaces tested. In the OTS treatment surface, however, both water and diodomethane contact angles were increased even more than that of of HMDS treatment surface. The increase in contact angle on surfaces tested represents a reduction of surface energy (Pocius 1997).

Known values of γ_L, γ_L^D, γ_L^P for the probe liquids (water and diodomethane) shown in *[Table 3-4]* and their actual measured contact angles on HMDS and OTS treatment surfaces *[Table 3-5]* were used to calculate the total surface energy (γ_s^{tal}) of the different SAMs modificated solid surfaces including polar (γ_s^P) and the dispersive (γ_s^D) components *[Table 3-5]*, as described by Gardner et al. (1999). The dispersive energy was elevated using the geometric mean formula [Equation 3-4]. At first, the diiodomethane contact angle was used to determine the γ_s^D *value*. Assuming $(\gamma_L^p\ \gamma_s^p)^{1/2} = 0$, simplifies as:

$$(1+\cos\theta)\gamma_L = 2(\gamma_L^D \times \gamma_S^D)^{1/2} \quad \text{[Equation 3-4]}$$

Rearranging term results in:

$$\gamma_S^D = \frac{1}{4}\gamma_L(1+\cos\theta)^2 \quad \text{[Equation 3-5]}$$

Where: $\gamma_L = \gamma_L^D$ for non-polar liquids.

So we can obtain the the dispersive (γ_s^D) component in equation 3-5. Then the water contact angle was used to elevate the polar (γ_s^P) component with the known γ_s^D, γ_L^D , γ_L^P , γ_L.

Total surface energy results after γ_s^P calculation with the dispersive (γ_s^D) component:

$$\gamma_S^{Total} = \gamma_S^D + \gamma_S^P \quad \text{[Equation 3-6]}$$

The surface energy values in the OTFT device were listed in *Fig. 3-22*. The surface energy of active region (HMDS region: SiO_2, 37.4 nJ/cm^2 and Pt, 40.7 nJ/cm^2) in P3HT OTFT was higher than that of the non-active region (OTS region: SiO_2, 24.5 nJ/cm^2 and Pt, 31.9 nJ/cm^2). The surface energy is related to the wettability of the surface with different chemically SAMs modifying, ex. HMDS and OTS. The surface with higher surface energy is easy to wet with the contact liquid. It means that the contact liquid easily adheres to the substrate surface with higher surface energy than that with lower surface energy. When P3HT solution flowed across the device substrate surface, it selectively wetted the active region (HMDS modified surface, higher surface energy) and dewetted the non-active region (OTS modified surface, lower surface energy). The P3HT solution was trapped (wetted) in the higher surface energy area, it was difficult to escape because the lower surface energy (dewetted) area was around it. So the P3HT active region was confined after this self-organized process. The PEDOT:PSS water solutions were also compatible with this method. Because the HMDS and OTS modified surfaces both are hydrophobic. Water solution cannot stay at their surfaces any more. So the simple hydrophilic and hydrophobic theory can't explain the self-organized phenomenon well. Here, this surface theory is better to explain this self-organized phenomenon and makes

someone understand clearly. Despite the difference of surface energy values with different chemical modifications, the solution will wet the surface with higher surface energy when it has choice. We had demonstrated a unique, novel patterning plat-form for dissolved/well-dispersed solutions via two-step chemical modification layer growth.

Chapter 4
Novel Self-Organized Method Applied on Different Organic/Inorganic Materials

A novel double gate structure of P3HT OTFT was also fabricated, the purpose of this structure to control the threshold voltage by biasing the top gate voltage. Moreover, several other active materials were also applied, such F8T2, ZnO and Pentacene Precursor. Those intentions let us manufacture the N-type TFT and P-type TFT and combine them to act as the complementary TFTs.

4.1 Double Gate Organic Thin Film Transistor

4.1.1 Background

Recent advances in material development and processing techniques [4.1] have resulted in significant performance gains of solution-processed OTFTs. Throughout this progress, despite proposed new geometries, such as vertical channel OTFTs, [4.2] the standard planar devices remained basically unchanged, with TFT structures, implemented in bottom gate (BG) or top gate (TG), as the most common configurations. New structures and geometries, such as the double-gate-OTFT (DG-OTFT), which is already used in the inorganic metal-oxide-semiconductor field-effect transistor (MOSFET) research field, [4.3] could help to achieve further performance improvements without significantly affecting the process complexity. The main application for OTFTs are switches, [4.4] which require high values of I_{ON}/I_{OFF} ratio (10^6) and reduced power dissipation in the off state. However, the leakage

currents through solution-processed polymeric insulators and processing issues often limit the minimum insulator thickness and consequently the dielectric capacitance Ci. High values of V_G and V_D are then required to achieve the desired drain current level, which is intrinsically limited by the low carrier mobility of conjugated polymers. We demonstrated the DG-OTFT structures, an increased drain current can be achieved as a consequence of two effects: The accumulation of carriers at the second semiconductor-insulator interface; and under specific conditions, the capacitive coupling between one of the two channels and the opposite gate. Furthermore, since the electrostatic potential and the carrier density in the whole film became a function of the second gate bias, to a certain extent the threshold voltage V_{th} and the off-state current can be tuned.

The DG-OTFTs with simplified geometry was described in *fig. 4-1(a)*, with a combination of a TG stacked on a BG OTFT; the two devices shared the source and drain electrodes and the semiconductor layer, while the two gates can be designed to be independent or electrically connected. In our case, the DG-OFET structure was strongly asymmetric, due to differences between the production processes of bottom and top gate OTFT structures. Two different insulators with different dielectric constants and thicknesses have been used in this study, led to different capacitances and different insulator-semiconductor interfaces. The gate controlled the metal-insulator-semiconductor structure with the higher capacitance (Ci), which will be responsible for the higher contribution to the drain current, and be referred to as the primary gate. In our study the primary gate was the bottom gate. The top gate in our study therefore was referred to as the secondary gate. The ratio between the top and bottom capacitances C_{Ti} /C_{Bi} significantly affectsedthe device operation. The various operation modes for the device can be separated into single-gate and double-gate (DG) modes. For single gate operation, either a TG or BG was obtained when the corresponding gate was biased while the other gate was connected to ground. The DG bias modes for the p-type DG-OFET were described in *fig. 4-2*. Applying simultaneously different independent bias levels to the TG and BG (V_{TG}, V_{BG})

drove the device in an asymmetric bias mode (AB). If both gates were connected to the same voltage source, the DG-OTFT was operated in the symmetric bias mode (SB). In both cases, the double accumulation regime (V_{TG}<0, V_{BG}<0) or the double depletion regime (V_{TG}>0, V_{BG}>0) were obtained, respectively, when both gates were biased with the same polarity; the application of opposite bias polarities to the gates allowed one to operate a depletion OTFT, where the device (on) were switched off by biasing one of the gates positively; we called this the mixed mode.

4.1.2 Process Flow

The DG-OTFT structure was based on the Non-Patterned gate OTFT.

1. Initial RCA cleaning
2. 100 nm gate-oxide layer: furnace wet oxidation at 980 ℃
3. Ti / Pt = 2 nm / 20 nm as the adhesion/electrode layer: Sputter system at base pressure = 2 × 10^{-6}torr; metals were deposited continuously without breaking vacuum
4. P. R. lift-off to form source/drain electrodes: in ACE with ultrasonic agitation
5. ACE + IPA cleaning
6. HMDS molecules growth in a high temperature (150^{o}C) and low pressure (lower than 20torr) oven which was full of HMDS steam.
7. Spin-on passivation layer for active region with lithography used photo resistance FH6400, 1000 rpm for 10 seconds to be uniform and 4000rpm for 30 second to control thickness about 1μm.
8. HMDS removing to from surface excluding active region with PDC-3XG O_2 plasma with power of 5.4 Walt.
9. To grow OTS modification layer, we put the sample and 1 ml OTS liquid in a negative-pressure box in R.T for 45 minutes and then baking in vacuum chamber (100^{o}C

for 1 hour).

10. P.R removing by A.C.E with wet striping.
11. Dip casting P3HT with 0.5 wt. % P3HT in DCB solvent, and then baking in a vacuum chamber under 120^{o}C for 1 hour.
12. Spin coating PMMA with EA as the solvent as dielectric buffer layer, then baking in a vacuum chamber under 100^{o}C for 0.5 hour.
13. Sp coating the PVP dielectric layer (PVP liquid : 8 wt% PVP, 4 wt% PMF, 2.4 wt% PAG in cyclohexanol), 1000 rpm for 60 seconds, exposing under 365nm UV light for 1 minute and then baking in a vacuum chamber under 120^{o}C for 10 minutes to make PVP cross linked.
14. Ti / Au = 2 nm / 20 nm as the adhesion/electrode layer: Sputter system at base pressure = 2×10^{-6}torr; metals were deposited continuously without breaking vacuum
15. P. R. lift-off to form source/drain electrodes: in ACE with ultrasonic agitation.

We can simplified the step process flow to a diagrammatic process flow shown in *fig. 4-3*

4.1.3 Result and Discussion

A set of output curves measured for a p-type DG-OTFT were shown in *fig. 4-4* and *fig. 4-5*, where the bias of the TG is floating and the BG was used as “control” electrode. The threshold voltage was 2.6V, mobility is 0.002 cm^2/Vs, current on and off ratio were 3.5x10^5. The output curves showed in *fig. 4-6* and *fig. 4-7* when BG was floating and TG was used as “control” electrode. The threshold voltage is 3.4V, mobility is 0.01 cm^2/Vs, current on and off ratio is 1.2x10^5. We have got high mobility in this biased voltage. The contact resistance of source and drain was lower than first biased mode. The cross-linked PVP dielectric will trap a lot of carriers. With respect to the case where the BG electrode was floating diamonds, the output curves, measured with the BG negatively biased squares were shifted toward higher

current values.

The transfer characteristics of the DG-OTFT wasshown in *Fig. 4-8*, where the $I_D^{1/2}$ was plotted, respectively, for the asymmetric bias mode (AB) and symmetric bias mode (SB) (inset) accumulation bias modes. For asymmetric biasing, the BG voltage was swept from +40V to −40V, while the TG was biased with different constant negative and positive voltage. The field effect mobility was estimated from the curves with V_{TG}= 0 V in the saturation region (V_{DS}= −40 V) by inverting *Equation 4-1*: [4.5]

$$I_D = (W/2L) \cdot \mu Ci(V_g - V_{th})^2 \quad \text{..... [Equation 4-1]}$$

Where W=1000 um, L=10 um, and C_{Ti}=6.4 X 10^{-9} f/cm^2, was the measured capacitance per unit area; the field effect mobility was about 3X10^{-3} cm^2 /Vs. The transconductance in saturation, defined as:

$$g_m = (\frac{\partial I_D}{\partial V_G})_{V_D = const} = (W/L) \times \mu \times C_i \times (V_G - V_{TH}) \text{..... [Equation 4-2]}$$

It remained the similar slopes of the curves in the quadratic region. From *fig. 4-9*, it was clear that the set of curves was shifted “up and left” when increased negative V_{TG} voltages. Consequently, the threshold voltage, indicated by the intercepts of the dashed lines with the V_{BG} axis, moved from a value of 32.8 V to a value of −3.7 V for V_D=−40 V. We interpreted this shift of V_{th} as the result of an increasing hole carrier density through the whole P3HT film, including the top interface, resulting in the filling of traps at lower TG voltages. This is confirmed by the off current shift in *fig. 4-9* which was dependent on the BG bias. In this case, no significant improvement of the on/off ratio can be expected, due to the increase of the off current. Here we had successfully modulated the threshold voltage from 32,8 V to -3.7 V by biasing different top gate voltages. Moreover, this simple DG-OTFT structure has a great potential in circuit applications which need a low threshold voltage.

4.2 Other Soluble Active Materials fabricated by Self-Organized Methods

4.2.1 [9,9]-Dioctylfluorene-*Co*-Bithiophene Copolymer (F8T2) Deposition

We deposited the F8T2 active material with 1 wt% F8T2 in $CHCl_3$ solvent, then cured at 280 ℃ for 1 hour. Polymer thin film transistors based on the polyfluorene F8T2 exhibit a nonohmic contact resistance, particularly when in the coplanar device geometry. We showed F8T2-TFT I_D–V_G transfer curve in *[Fig. 4-13]* with W/L is 1000um/10um. The diode-type relation was attributed to the contact injection properties of the metal Schottky barrier. No significant increase in mobility with gate or drain field was observed. *Fig. 4-10* showed image of F8T2-TFT with self-organized method.

4.2.2 Pentacene Precursor Deposition

We deposited the Pentance precursor active material with 10mg precursor in $CHCl_3$ solvent, then cured device 130 ℃ for 1 hour. Recent research reported the fabrication of pentacene-TFTs via such a precursor route. [4.6] The maximum charge-carrier mobilities were about 10^{-2} cm^2/Vs. Here we presented a synthetic concept toward a soluble pentacene precursor, which might also be applied to the synthesis of even higher acenes. Furthermore, we showed the optimum the conditions for the conversion of the precursor into pentacene leading to a moderate value of the charge-carrier mobility. *Fig. 4-11* showed the good image with this self-organized method.

4.2.3 ZnO Deposition

We deposited the ZnO active material with 1 wt% in ethoxyethanol solvent, and cured at 300^{O}C for 1 hour. Recently research has focused on TFTs with substituting traditional amorphous silicon by a popular TCO material – ZnO. ZnO film deposited at room temperature reveals polycrystalline with a hexagonal wurtize structure and has a preferred orientation with the c-axis perpendicular to the substrate. Un-doped ZnO film behaves as an n-type transparent semiconductor due to the defects such as zinc interstitials and oxygen vacancies. It has a wide band gap (~-3.37eV) with optical transmission about 75% in the visible portion of the electromagnetic spectrum [4.7]. The main advantage of using ZnO deals with the fact that it is possible to growth high quality polycrystalline ZnO films at room temperature [4.8]. Besides that, thin films based on ZnO have been studied for several years for their low cost, low photo sensitivity, no environmental concern, and especially the high mobility [4.9]. TFTs using ZnO as channel layer usually exhibit normally-on state, because the excess carries are over 10^{17} cm^{-3} in as deposited states [4.10]. We got the moderate mobility (0.316 cm^2/Vs) of the ZnO device shown in *[Fig. 4-15]* and the image of it shown in *fig. 4-12.*

Chapter 5
Summary and Conclusions

In this research, the novel and unique self-organized organic/inorganic TFT devices were proposed. At first, we fabricated the P3HT OTFT device on the PET plastic substrate with this method. The patterned active layer is without any physical damages and the manufacturing process is very easy and low cost under low curing temperature with 120 ^{O}C. The current On/Off ratio approached 10^4, and it might not be used in the LCD display transistors. The OTFTs on the PET substrate showed the threshold voltage and mobility with 2.66V and 5.75× 10^{-3} cm^2/Vs. This moderate threshold voltage could be applied in the RFIDs, displays or some application which needn't high current on/off ratio.

Furthermore, we optimized the thickness of thermal oxide with patterned active layer and patterned metal gate OTFT devices on the silicon wafer. The optimum 300nm thickness of thermal oxide exhibited the lowest leakage current under operating that leaded to a high breakdown voltage. Gate patterning is necessary for further application in complicated circuit. The inverter and ring oscillator is our further plan. And high current on/off ratio about 10^6 is usefully to apply to our future electrical circuit.

Threshold voltage control is also an interesting project in OTFT research field. Among the OTFT devices, the high threshold voltage is a big issue for further application. We also fabricated the DG-OTFT devices with this simply self-organized process, we can modulate the threshold voltage from 32.8V to –3.7V. With this excellent controlling of the threshold voltages, the complementary OTFT (C-OTFT) could act as an inverter which was mostly applied in many electric circuits.

This novel self-organized method showed an important flat-top building with inorganic/organic active materials. The organic (P3HT, F8T2 and pentance precursor) and inorganic (ZnO) have been deposited and confined within the active region. This ZnO TFT

showed the high mobility 0.316 cm^2/Vs.

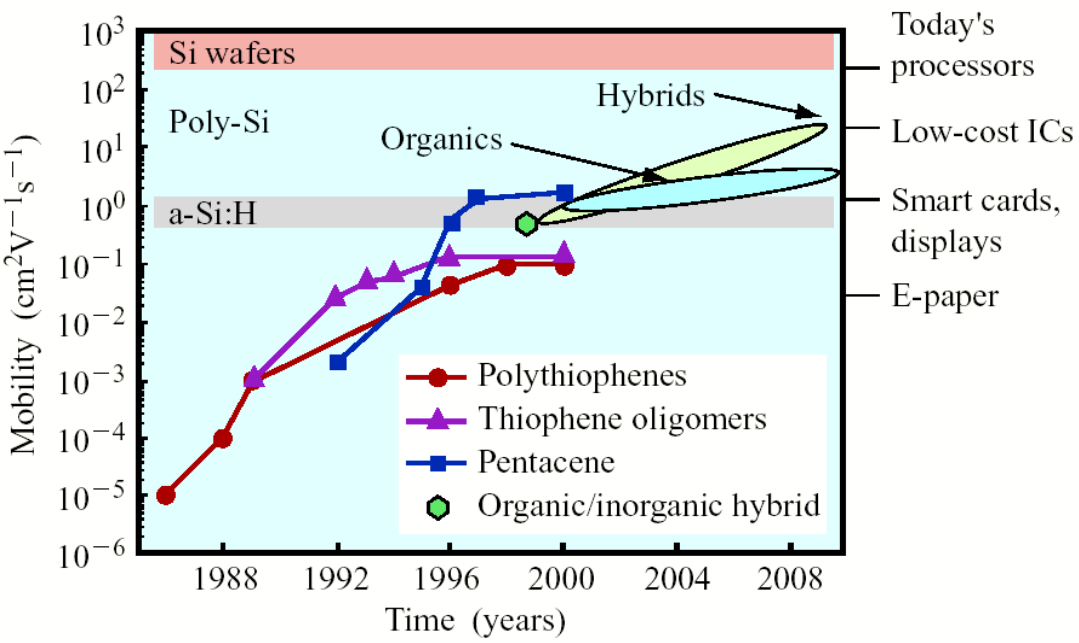


Fig. 1-1 The progress of mobility on organic materials in recent decades.

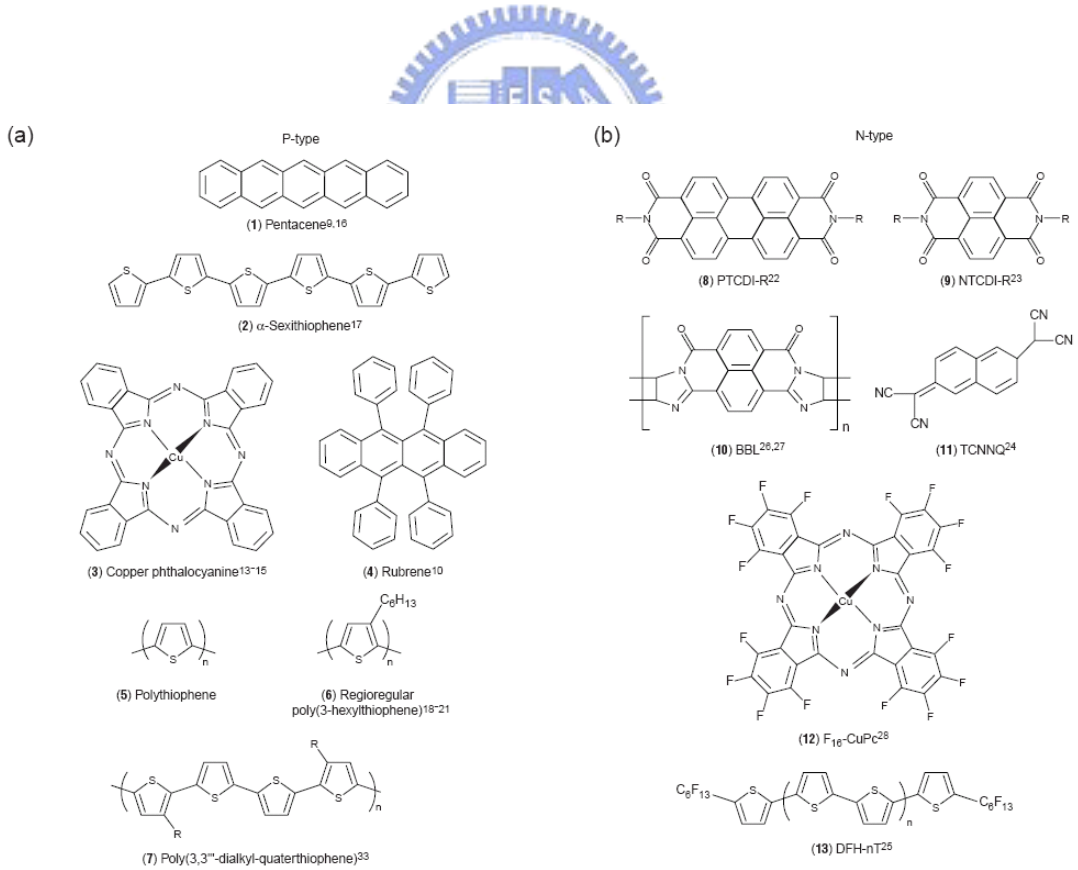


Fig. 1-2 Prominent (a) p-type and (b) n-type organic semiconductor materials.

Fig. 1-3 Photograph of a vacuum evaporator.

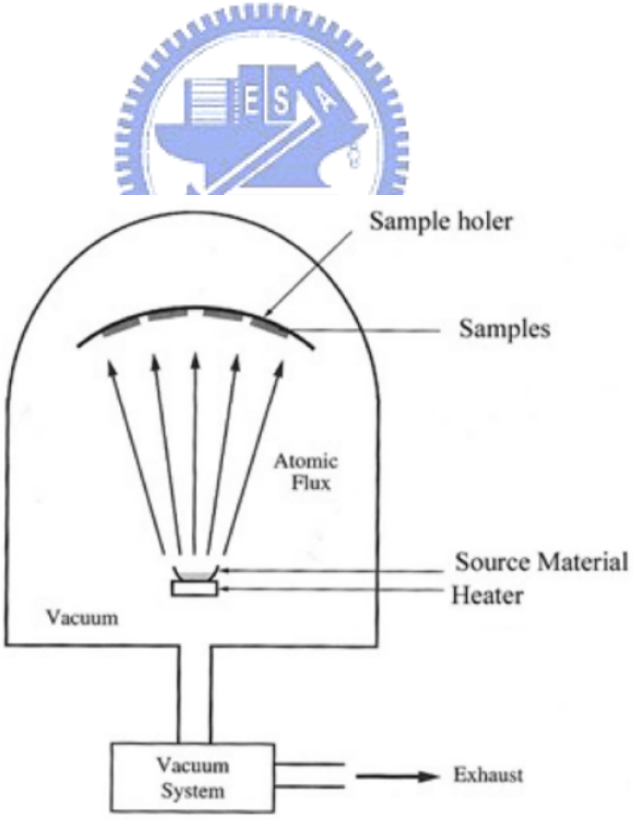


Fig. 1-4 The schematic of vacuum evaporator.

Fig. 1-5 A photograph of a spin-coater.

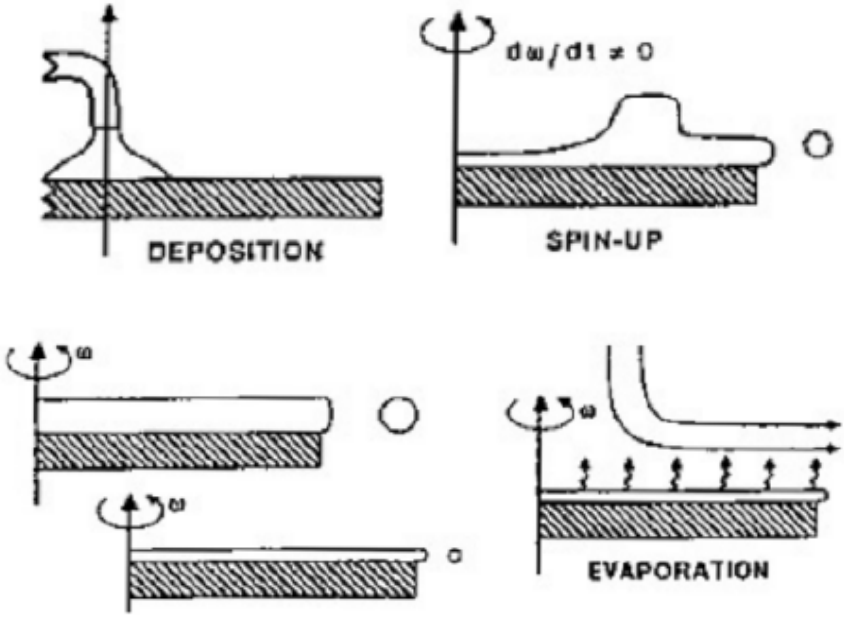


Fig. 1-6 The schematic of spinning coating.

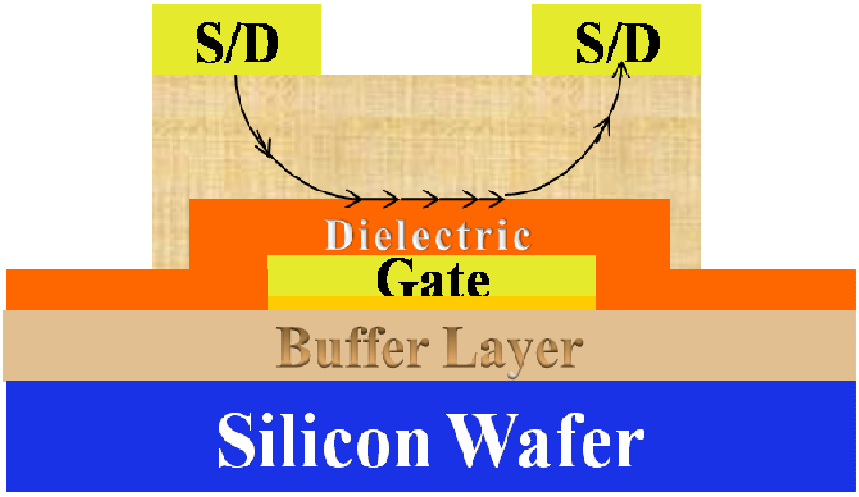


Fig. 2-1 The top contact structure, where both source and drain contact pads are deposited on top of an active layer through a shadow mask.

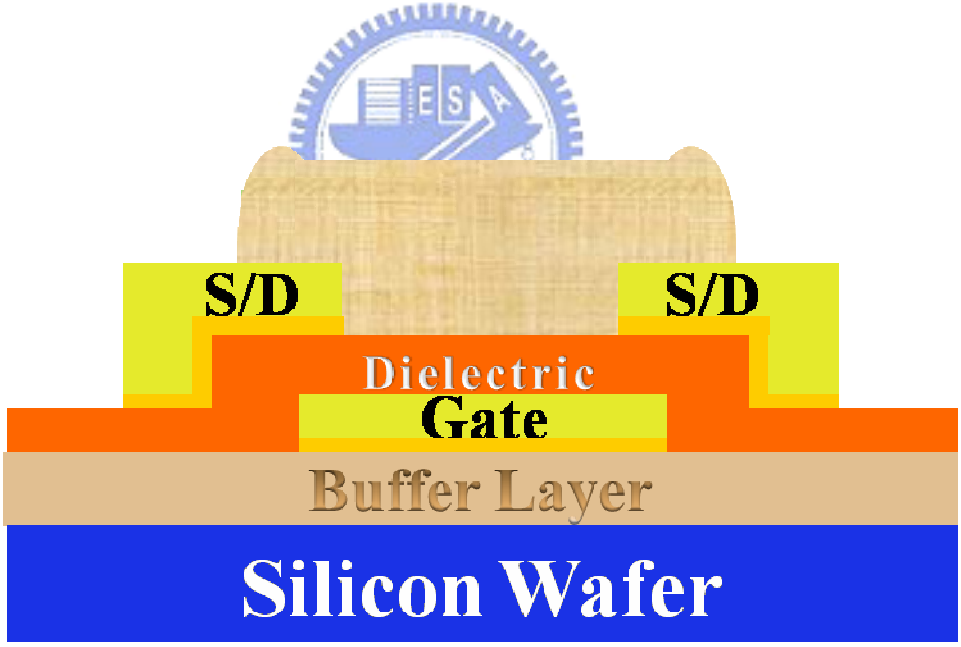


Fig. 2-2 The bottom contact structure, where drain and source contact metal is patterned on the gate dielectric prior to the active layer deposition.

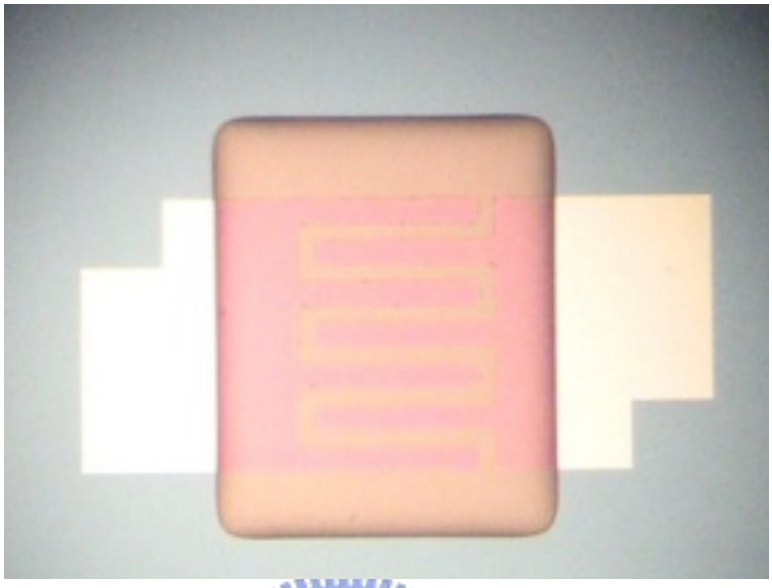


Fig. 2-3 The OM graph of RIE-Patterned active region.

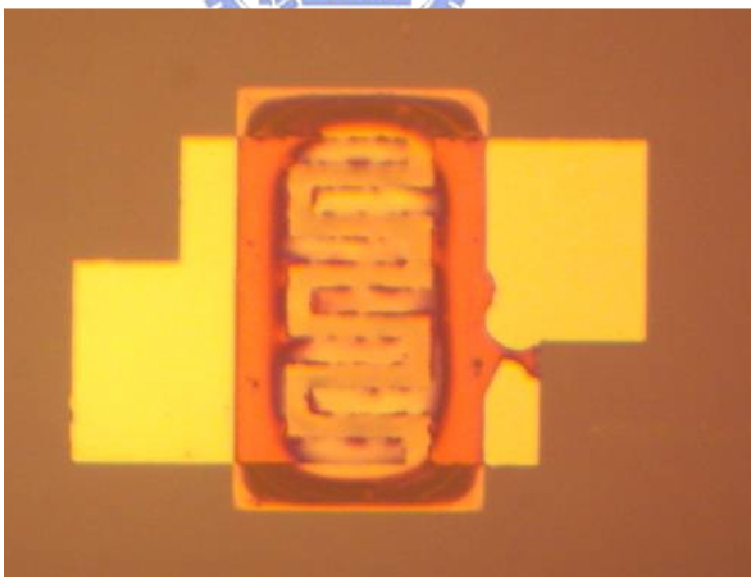


Fig. 2-4 The OM graph of Self-Organized active region.

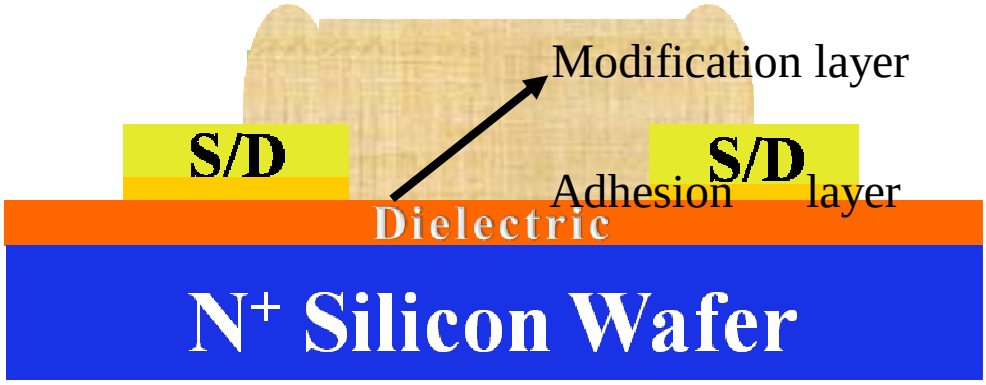


Fig. 2-5 The structure of coplanar OTFT.

(a) (b)

Fig. 2-6 The (a) finger type and (b) Stripe type source and drain with width/length is equal to 1000um/10um

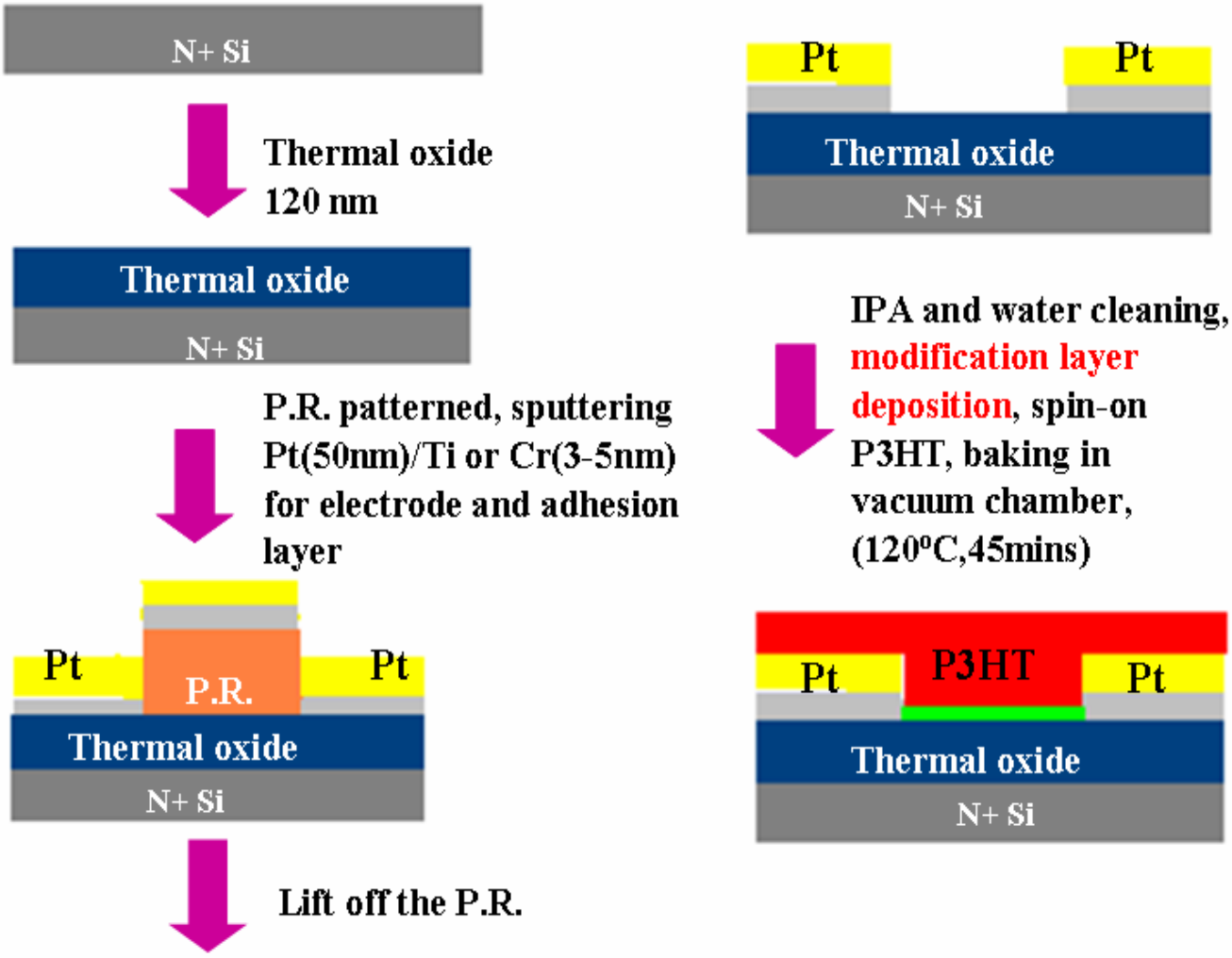


Fig. 2-7 The process flow of conventional OTFTs.

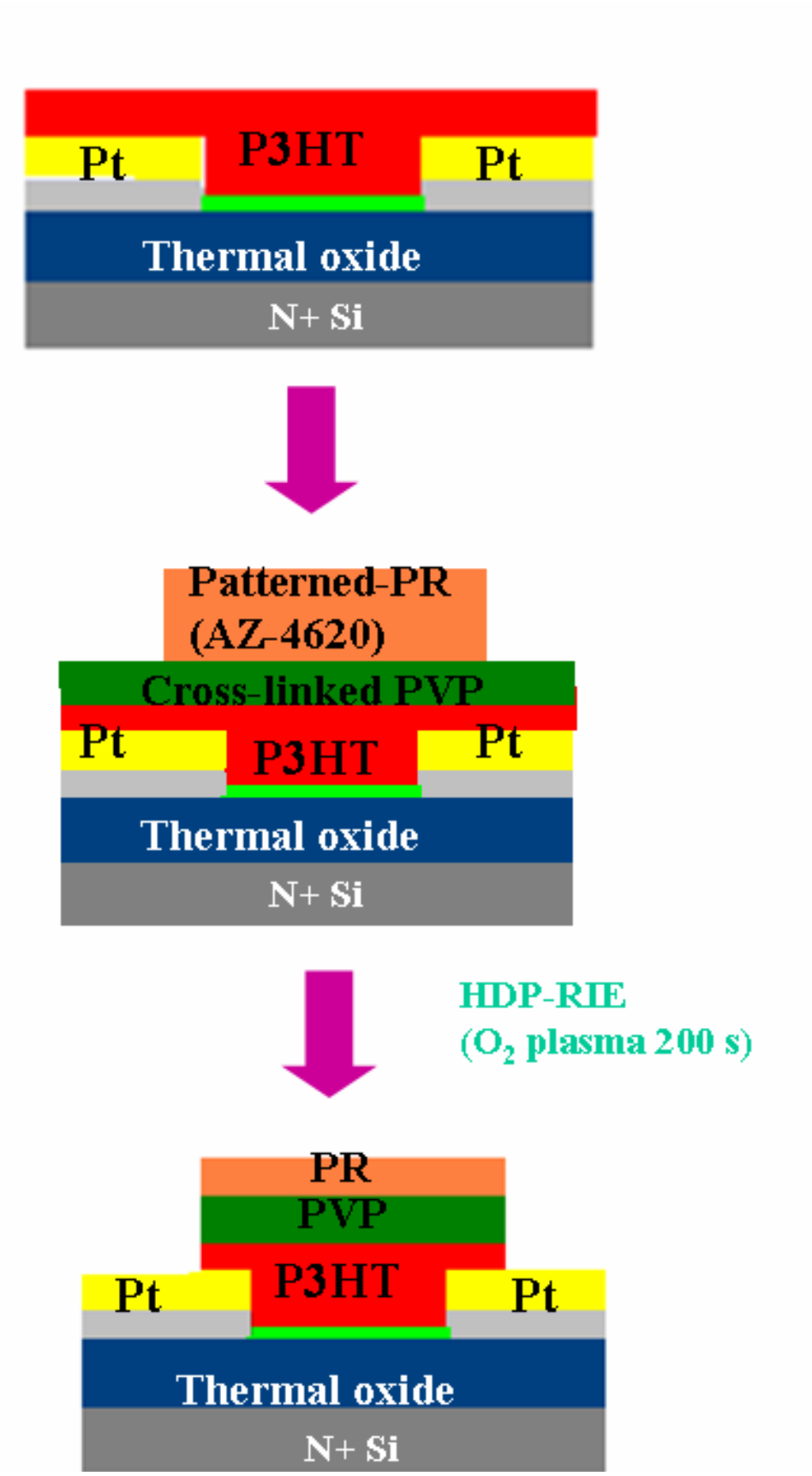


Fig. 2-8 The process flow of RIE-patterned OTFT with non-patterned gate

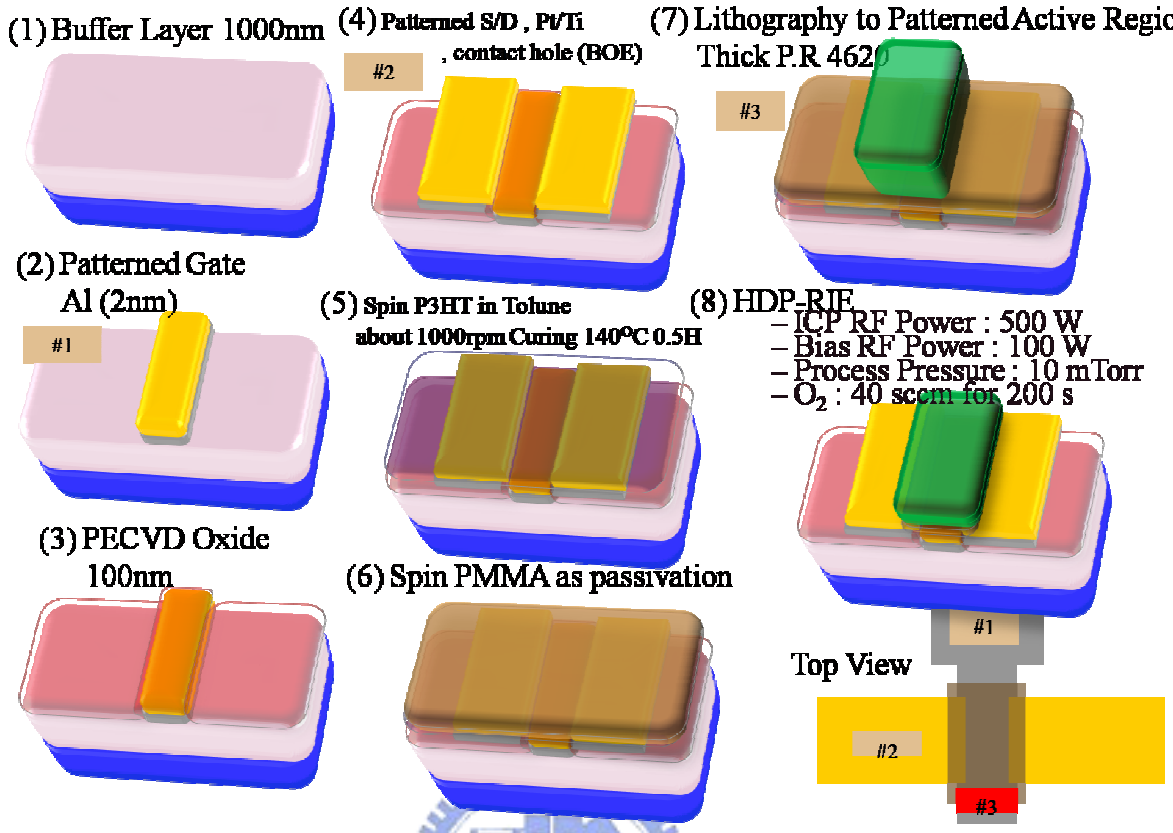


Fig. 2-9 The process flow of RIE-patterned TFT with patterned gate.

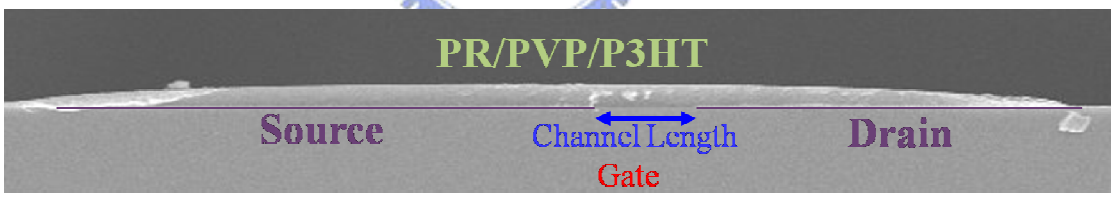


Fig. 2-10 The SEM image of RIE-Patterned OTFT.

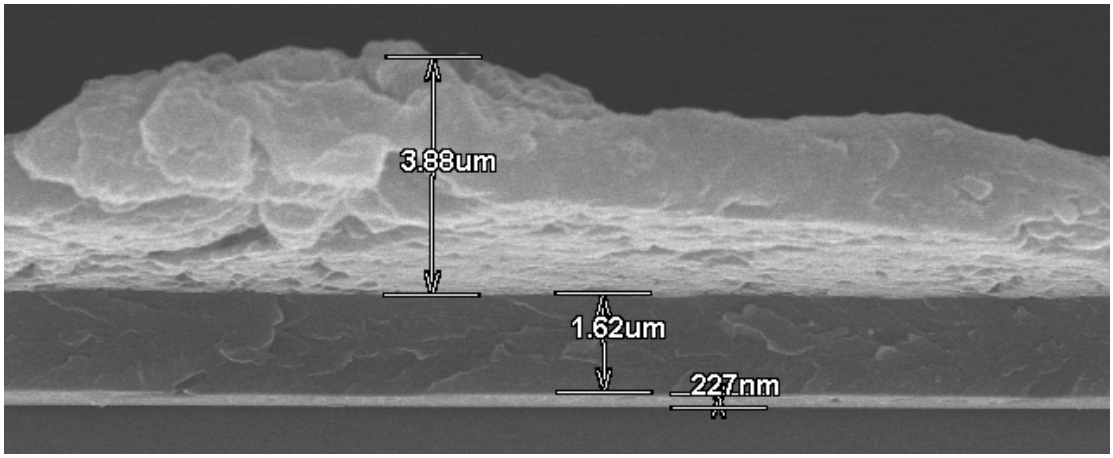


Fig. 2-11 The SEM image of PR stacking on OTFT.

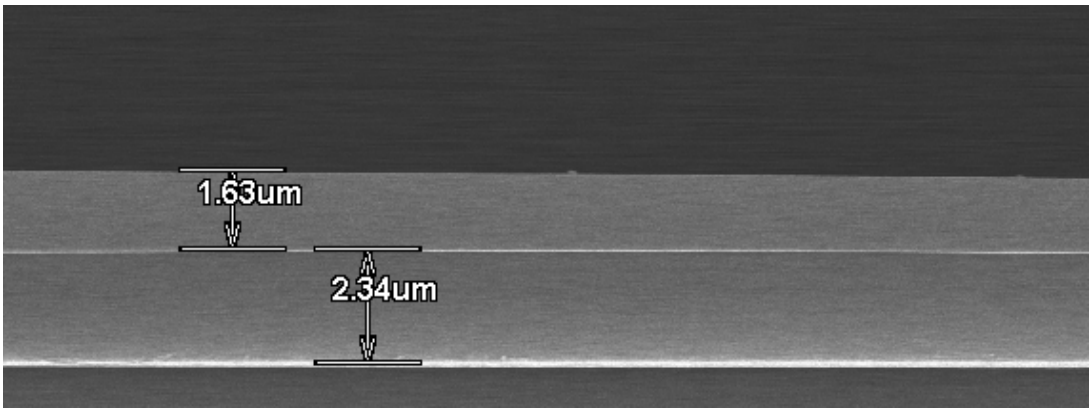


Fig. 2-12 The SEM image of RIE-patterned on the P3HT film.

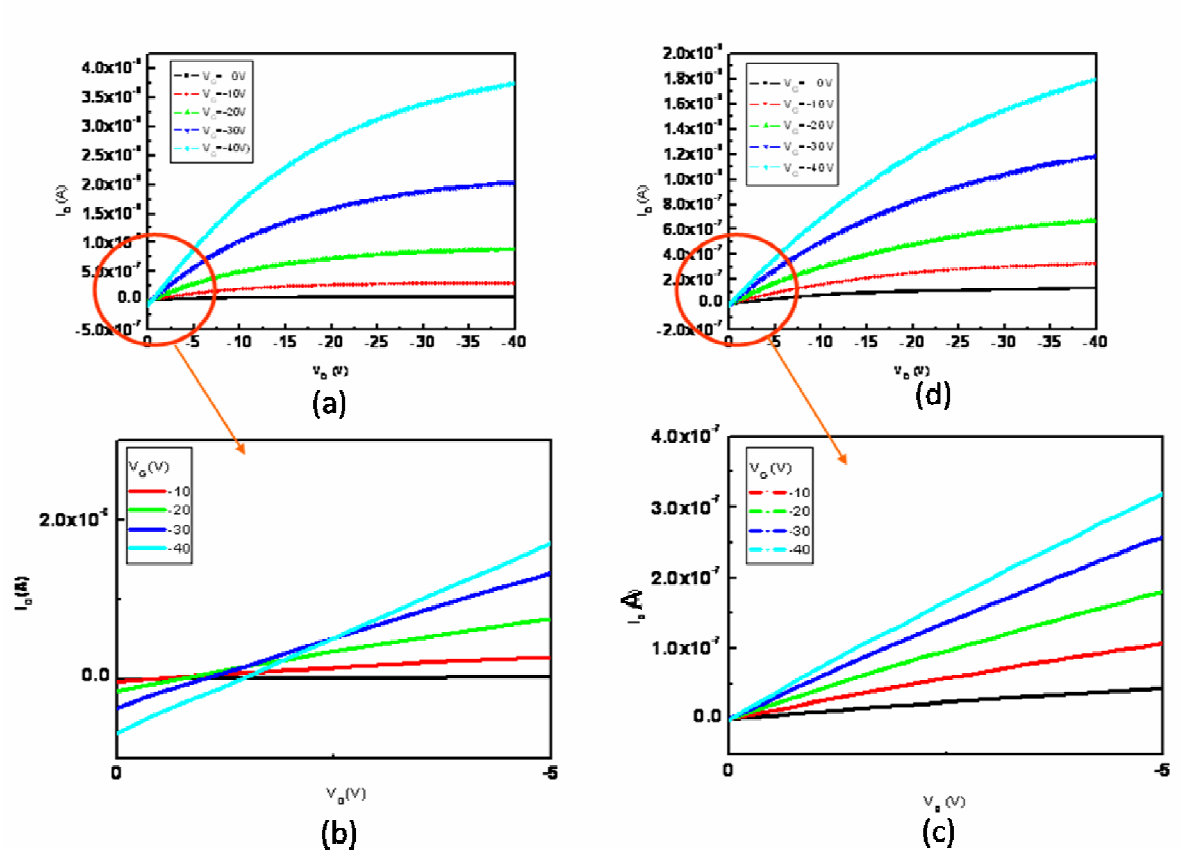
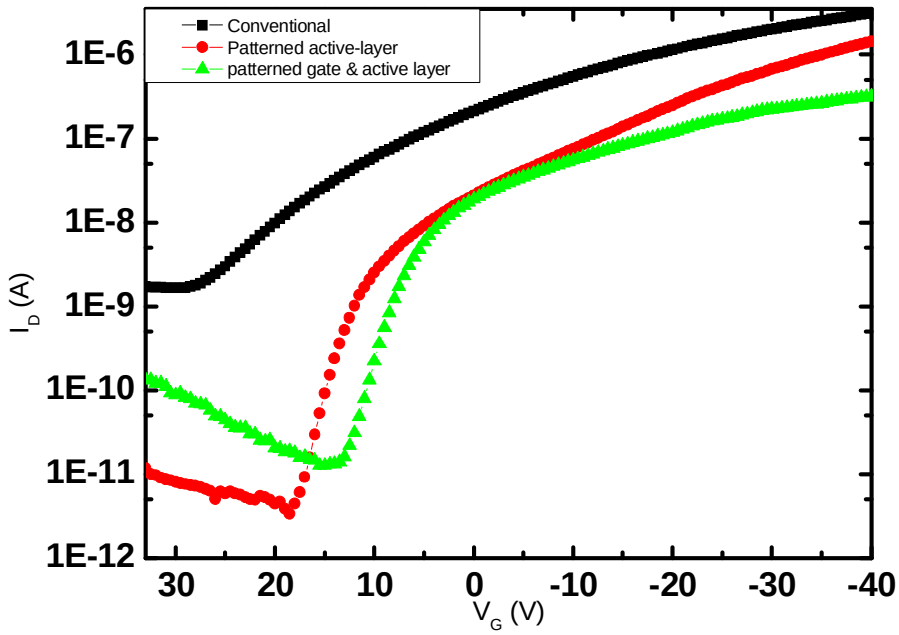


Fig. 2-13 (a)~(d) The gate induced leakage (i.e. the gate current) (I_G) increased with gate bias and was much higher at lower V_{DS} and peaks at V_{DS} = 0 V.

I_D-V_D curve of patterned active layer OTFT was shown in this fig..



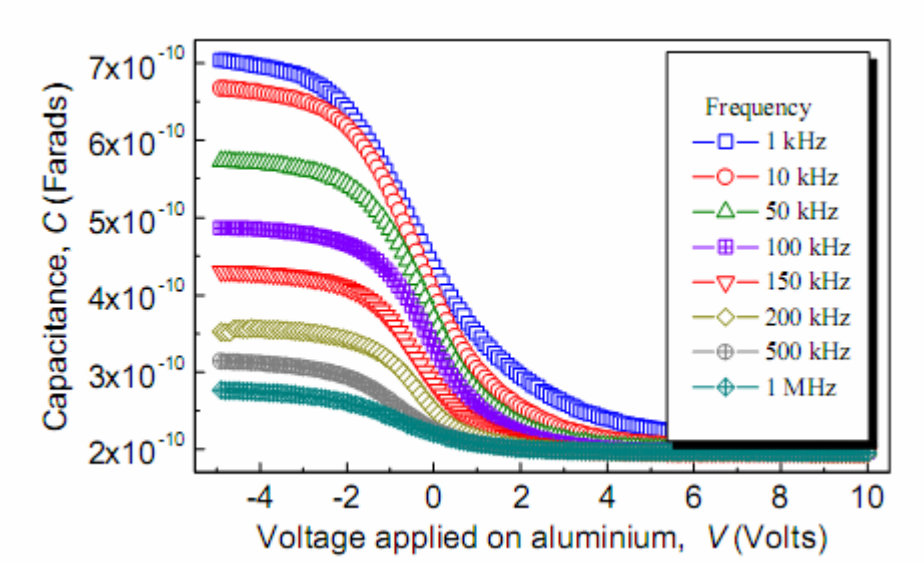


Fig. 2-14 (a) The I_D-V_G curve. This showed an OTFT with low gate induced leakage current. While the I_D offset was reduced significantly, the drive current for the transistor was comparable to the non-patterned devices. (b) The C-V curve. CV plots of Al/Al2O3/P3HT/Au (MOS) capacitor with undoped spun P3HT film at different frequencies. The oxide thickness was nearly 82 nm.

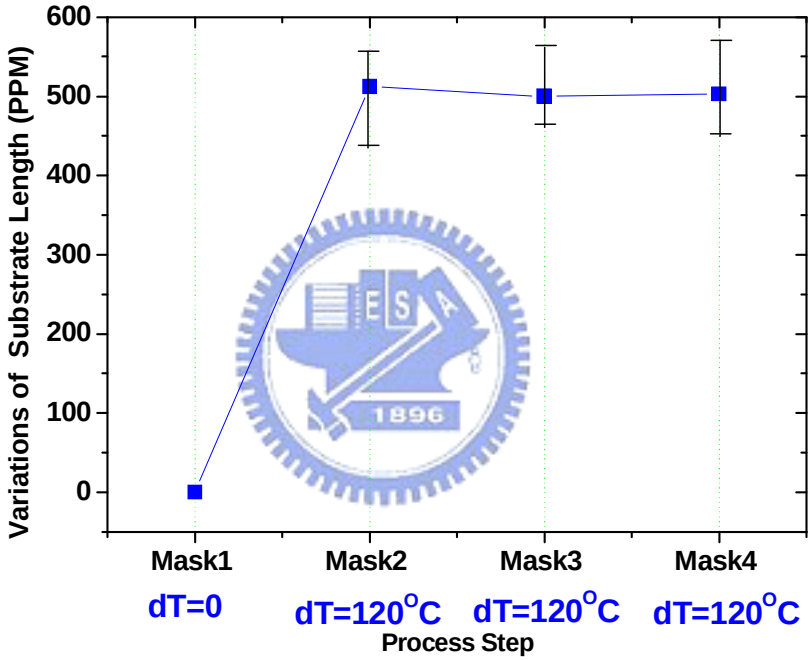


Fig. 2-15 The fig. depicted variations of substrate length during the actual OTFT process.

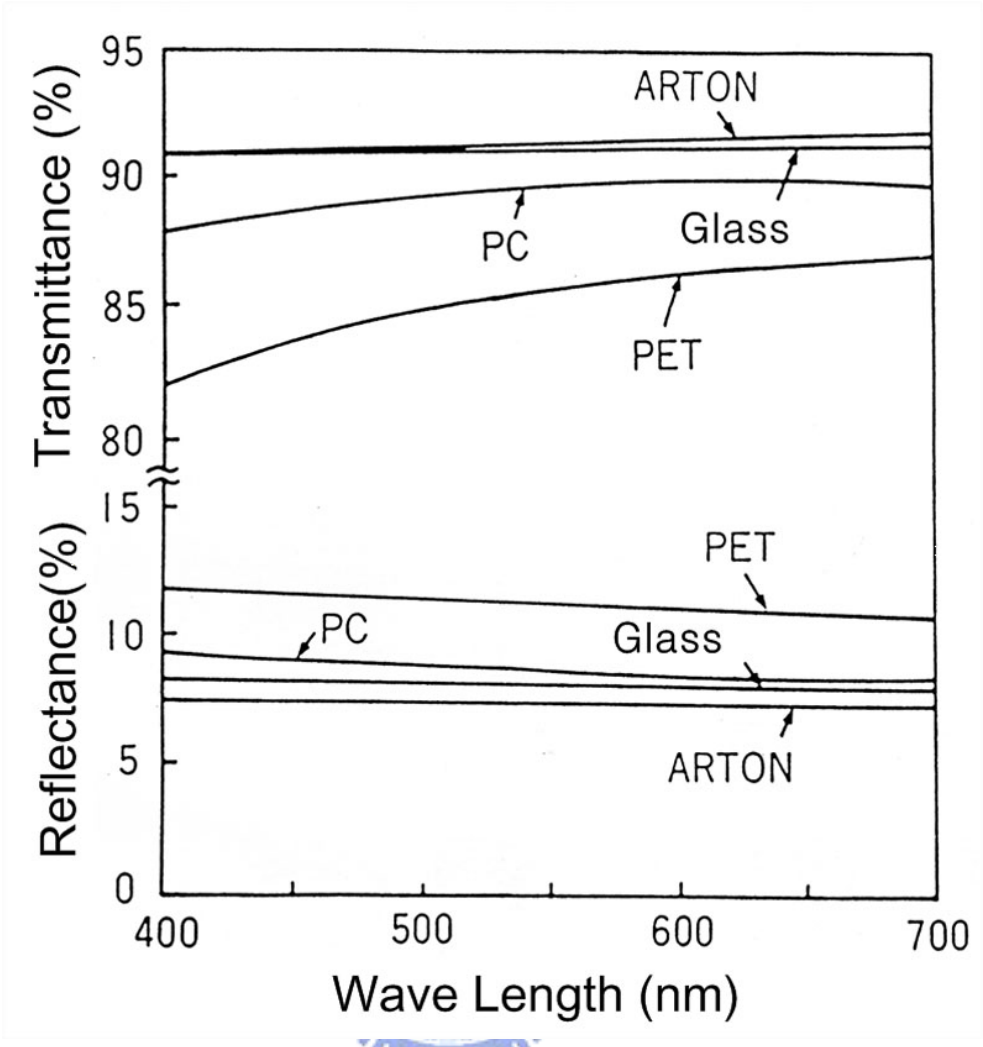
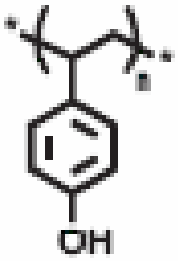


Fig. 2-16 PET film offers superior optical properties in comparison with PC, ARTON and glass substrates.



PVP

Fig. 2-17 Poly (4-vinylphenol) (PVP) is one of the most popular gate materials.

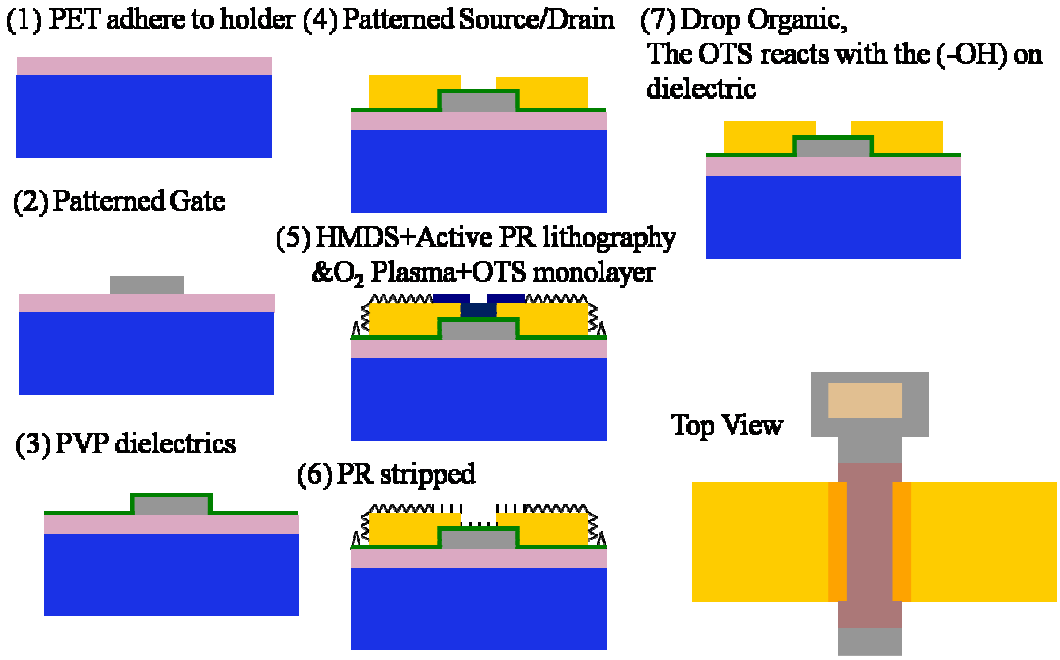


Fig. 2-18 The step process flow was shown into a diagrammatic process flow.

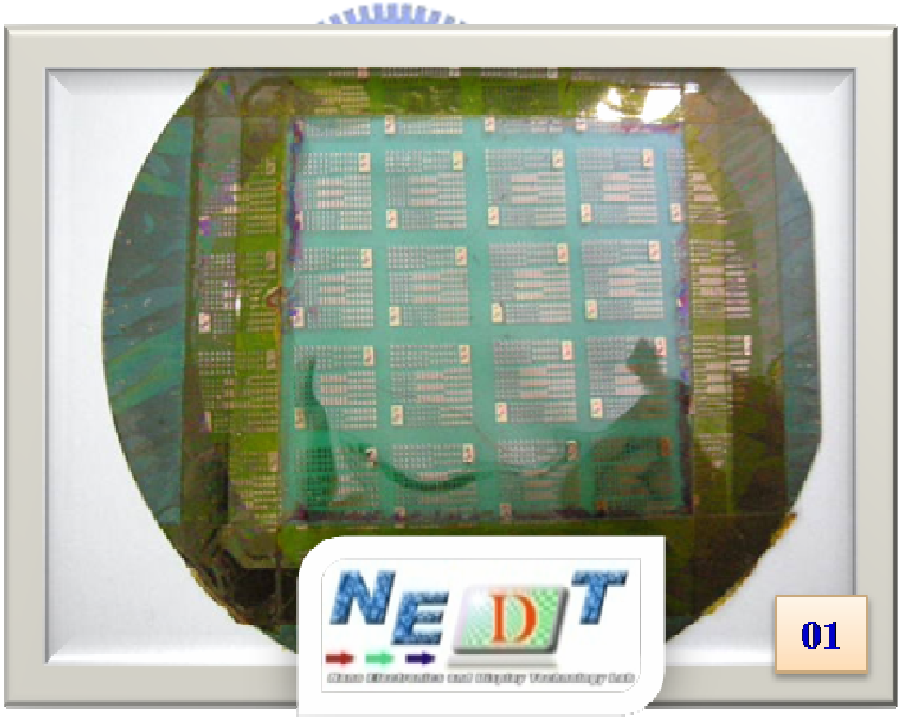


Fig. 2-19 Device was fabricated on the PET substrate with to plaster on silicon wafer by vacuum tape. Holder could be re-used, if we manufacture the device again.

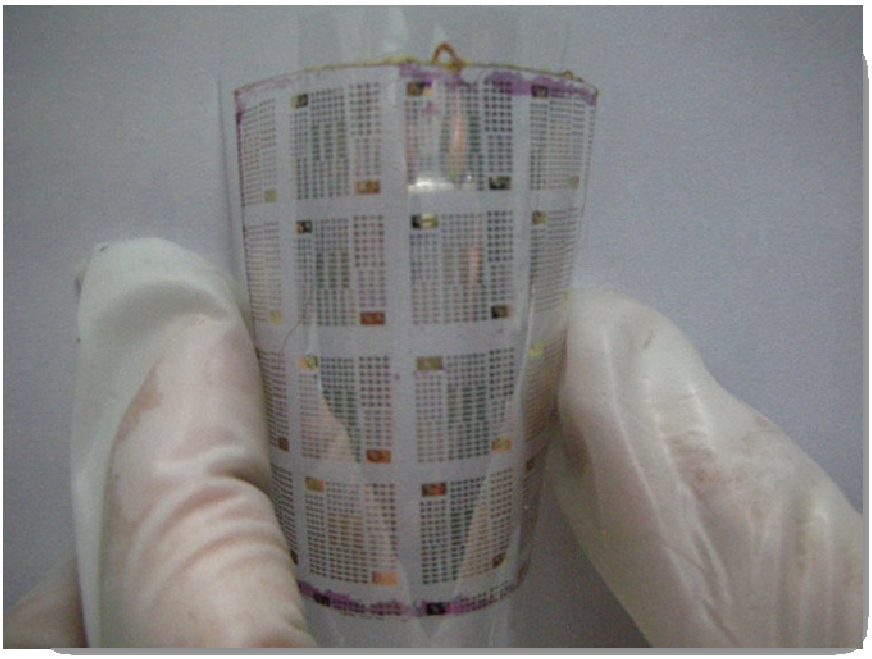


Fig. 2-20 The fig. shows the PET substrate could be curved 180 degree. If we called flexible substrate, the curved angle is vital factor.

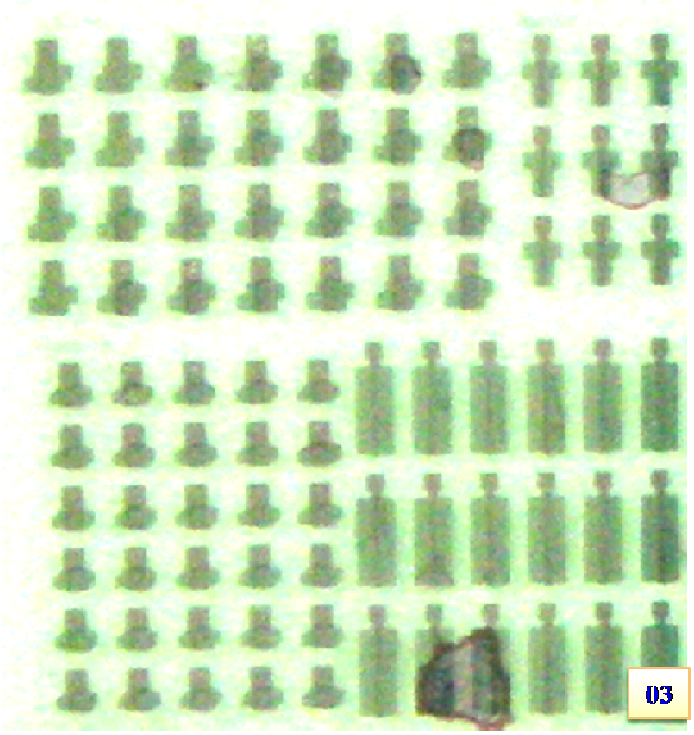
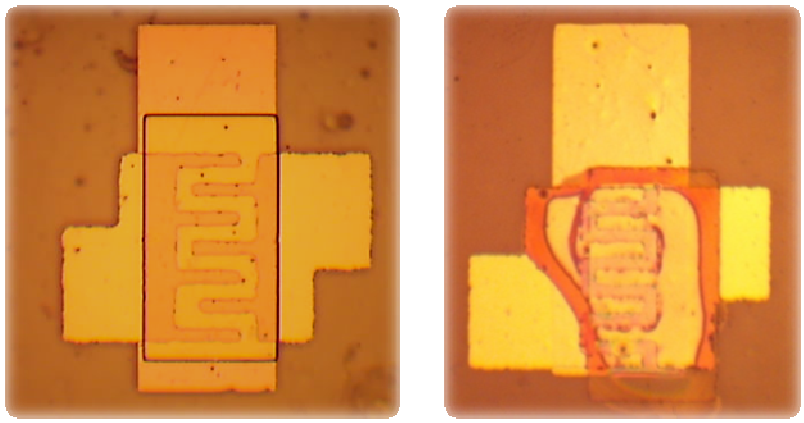


Fig. 2-21 This number shows the method called self-organized with P3HT clearly. P3HT was flow into active region, where this region was with lower surface energy.



(a) (b)

Fig. 2-22 (a) The active layer etched by RIE-patterned (b) The active layer patterned by self-organized.

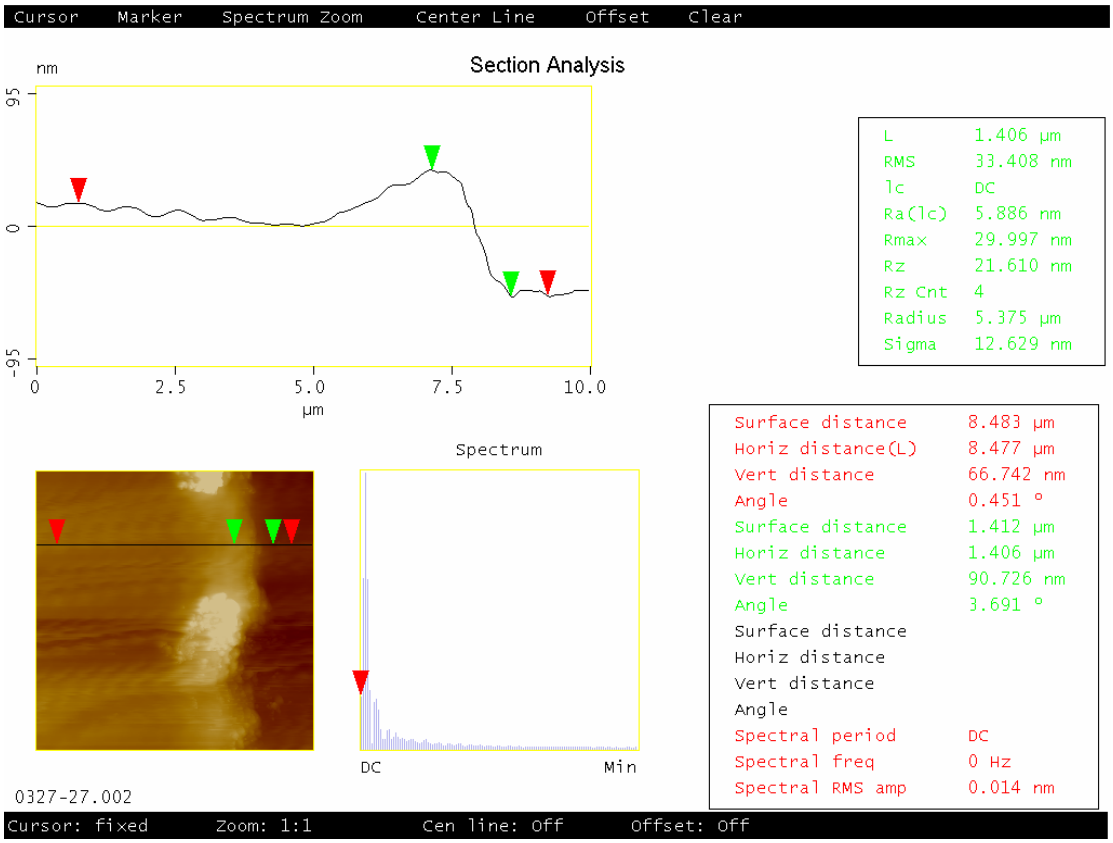


Fig. 2-23 The fig. showed that the polymer was assembled at the active edge of active region. Its might be the mechanism of self-organized is from center to edge. The vertical distance of green was 90.726nm and red is 66.742nm. The variation of two was 23.258nm.

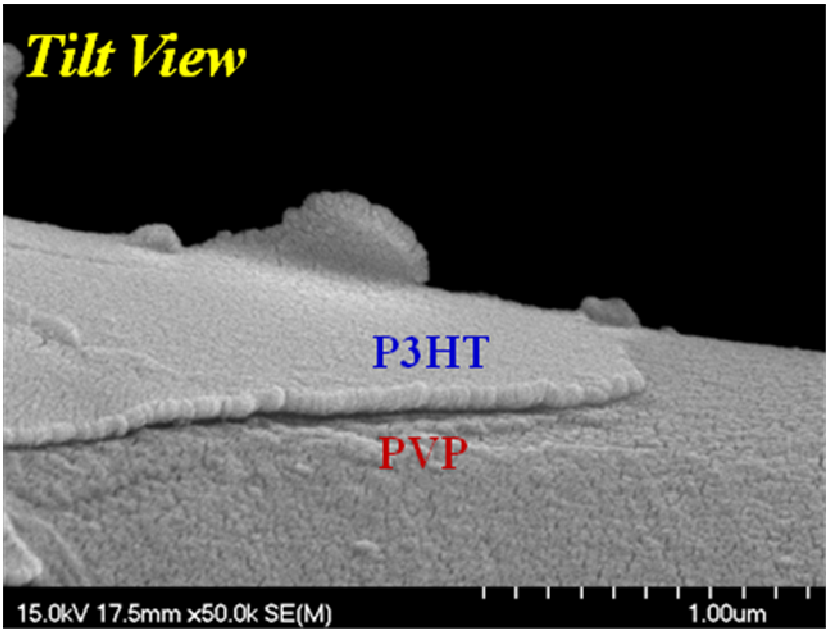


Fig. 2-24 The tilt view SEM image.

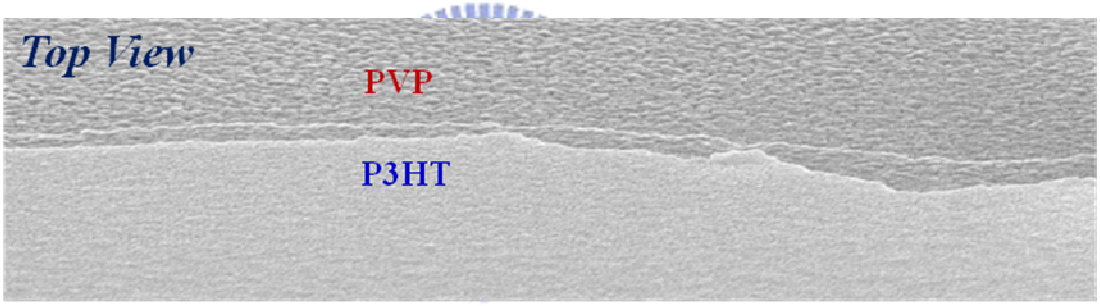


Fig. 2-25 The top view SEM image.

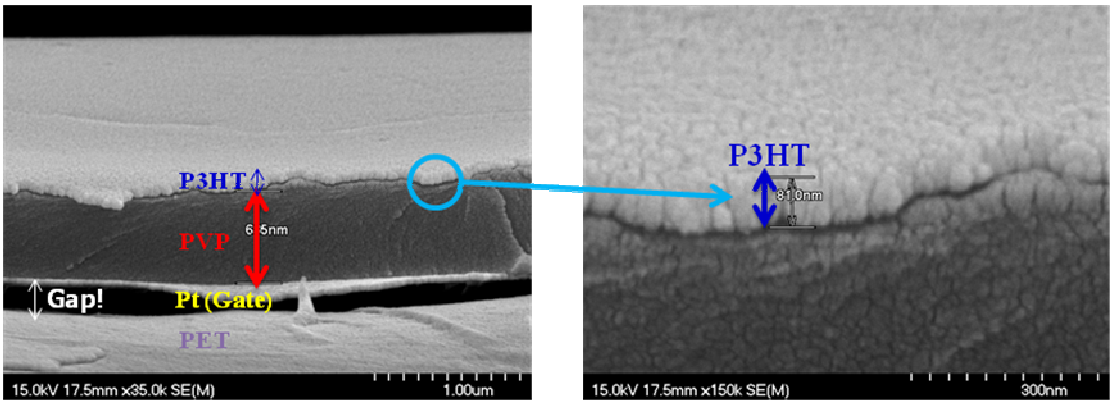


Fig. 2-26 The thickness of PVP and P3HT were 635nm and 81nm.

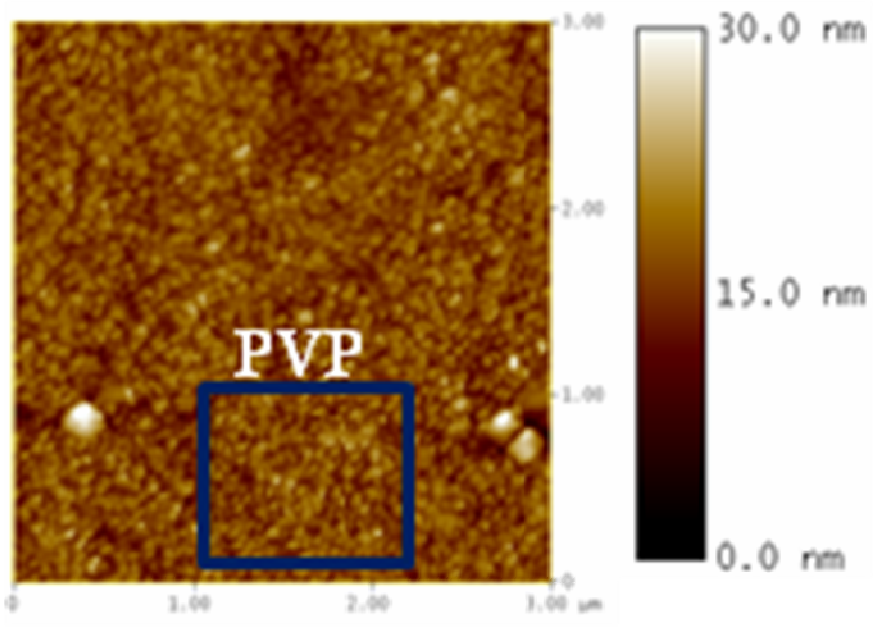


Fig. 2-27 AFM image of PVP film.

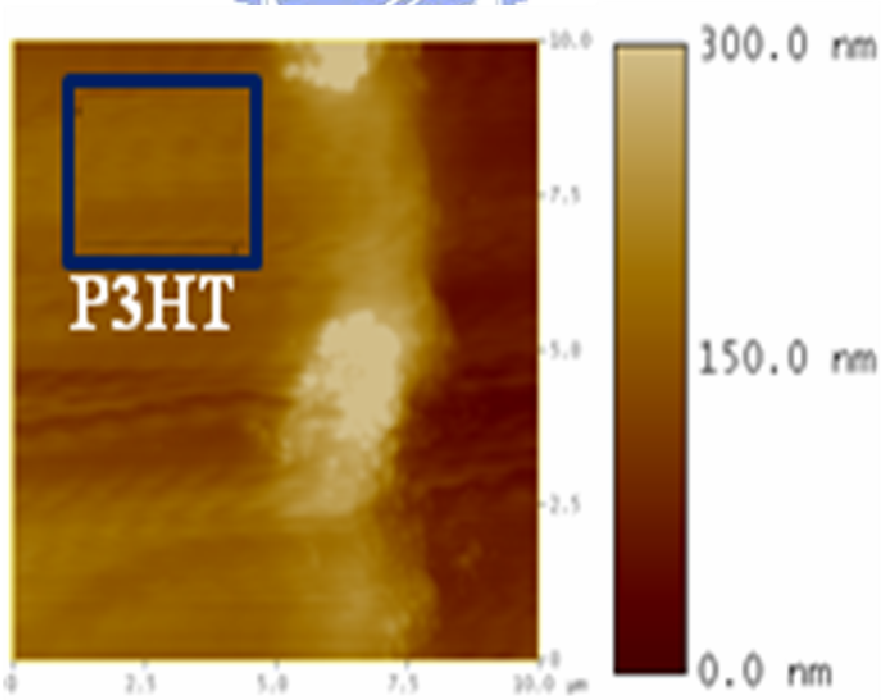


Fig. 2-28 AFM image of P3HT film.

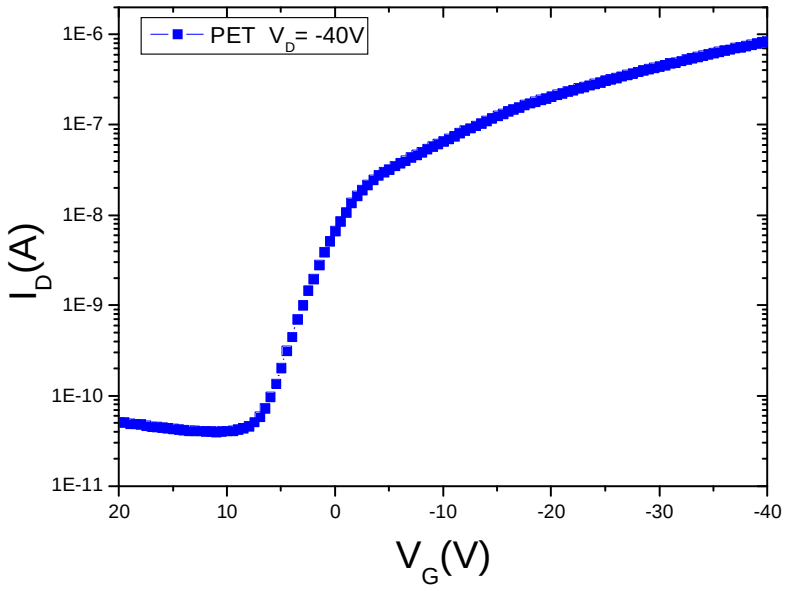


Fig. 2-29 The I_D-V_G curve of OTFT on PET substrate with V_D=40V, W=1000um L=25um.

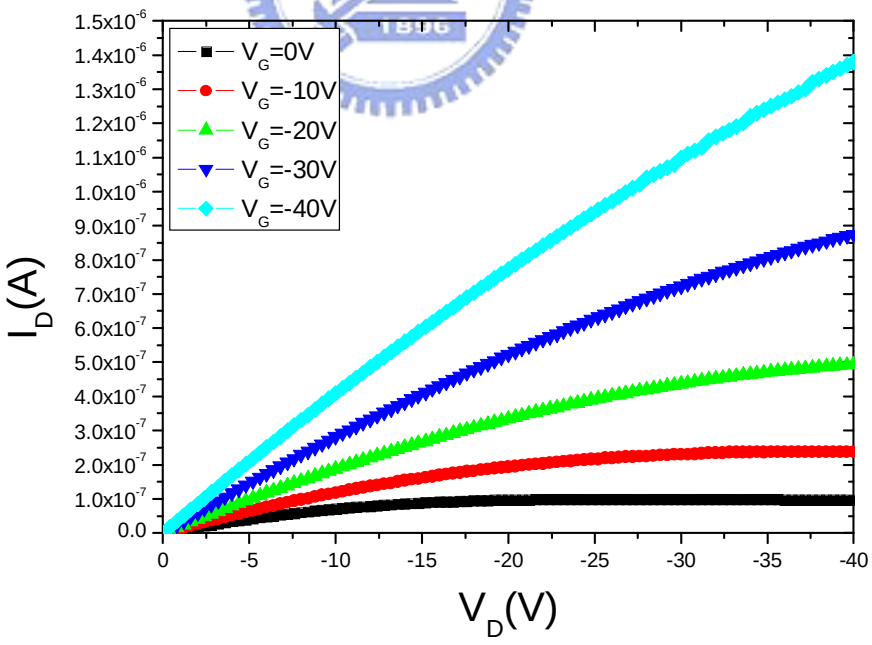
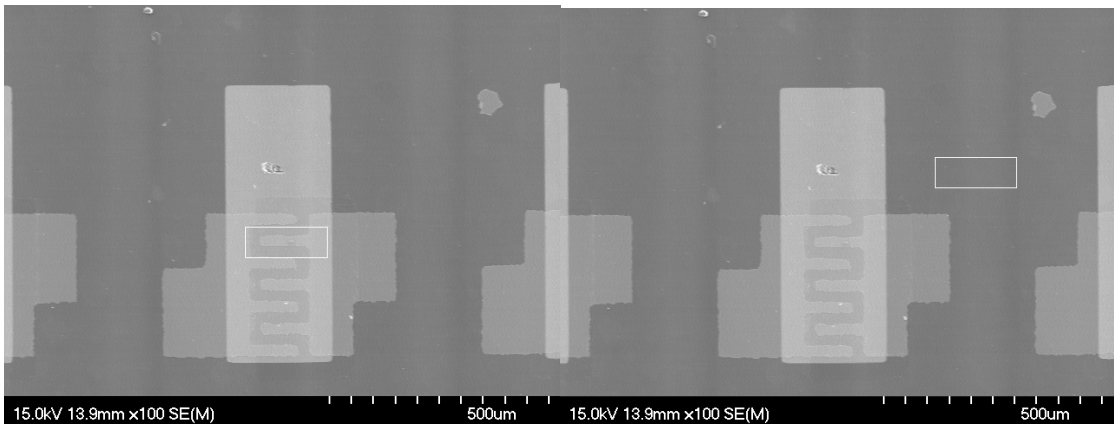


Fig. 2-30 The I_D-V_D curve of OTFT on PET substrate, W=1000um L=25um.



(a) (b)

Fig. 2-31 (a) showed the SEM image of the Self-Organized TFTs. A reference block region was selected inside the active region and (b) outside the active region.

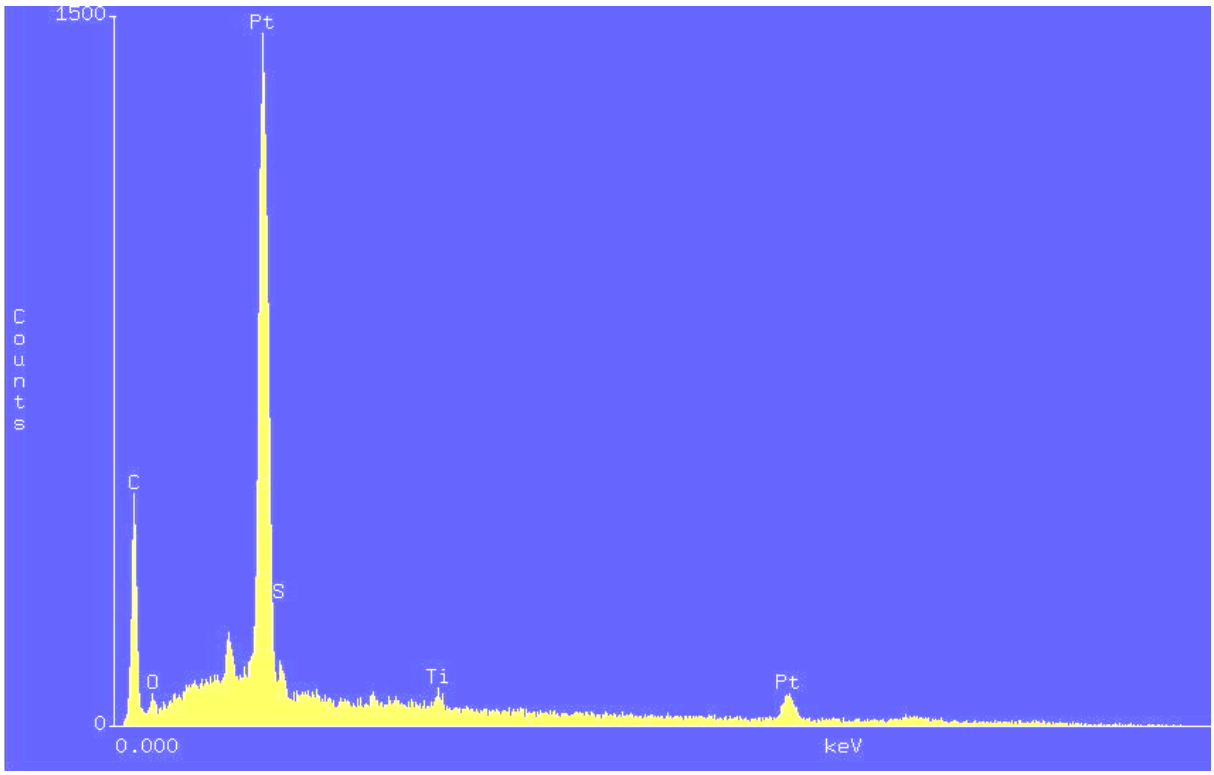


Fig. 2-32 The fig. showed the relative counts of sulfur distribution.

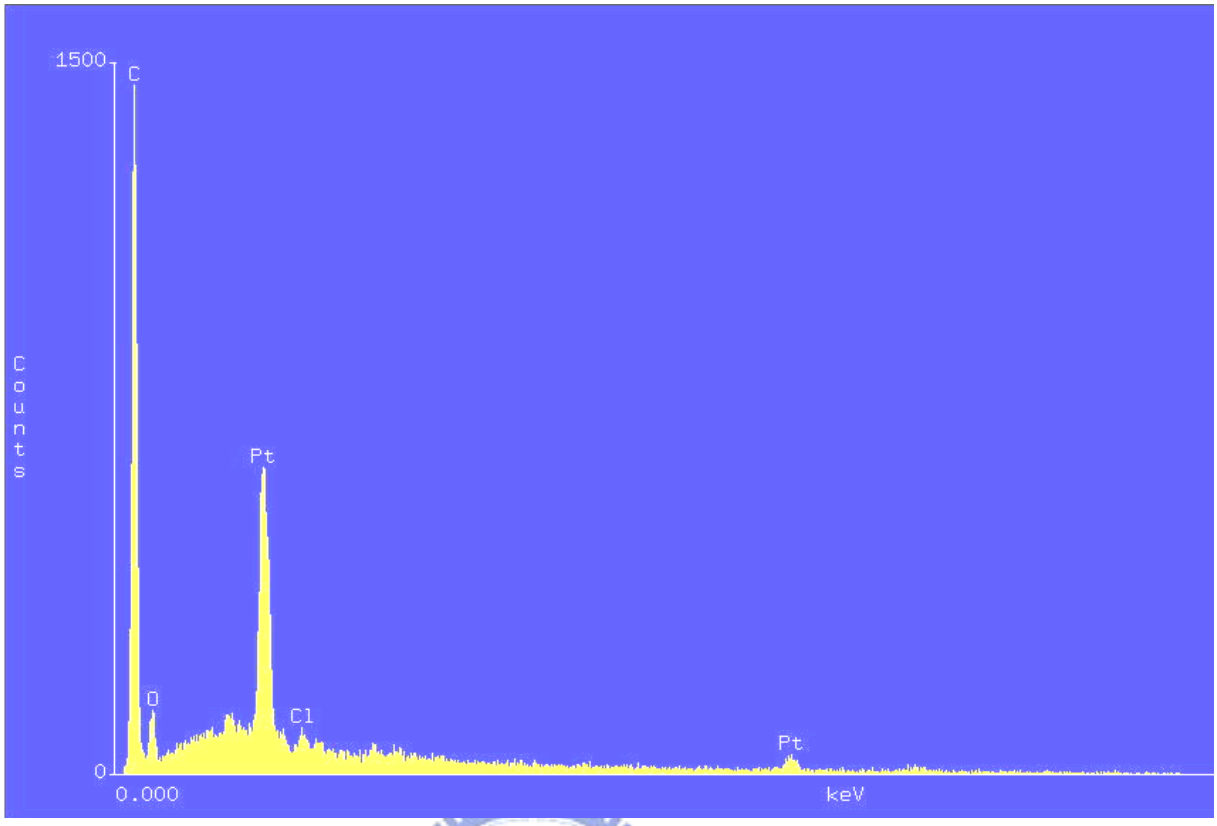


Fig. 2-33 The fig. showed the EDS analyses with non-patterned active region.

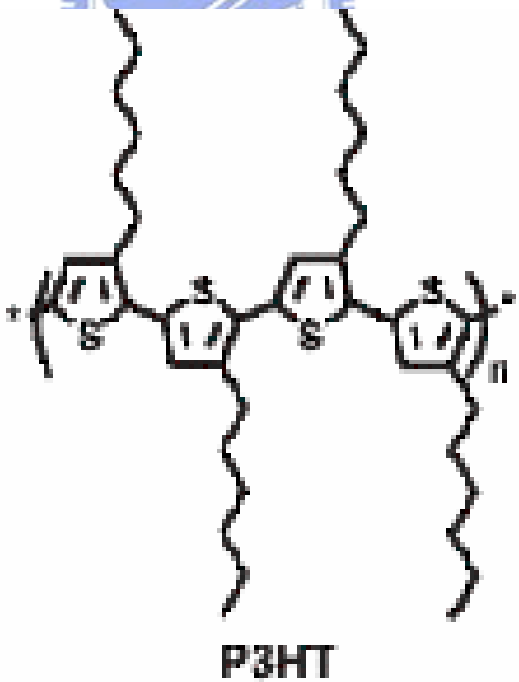


Fig. 2-34 The chemical structure of the P3HT.

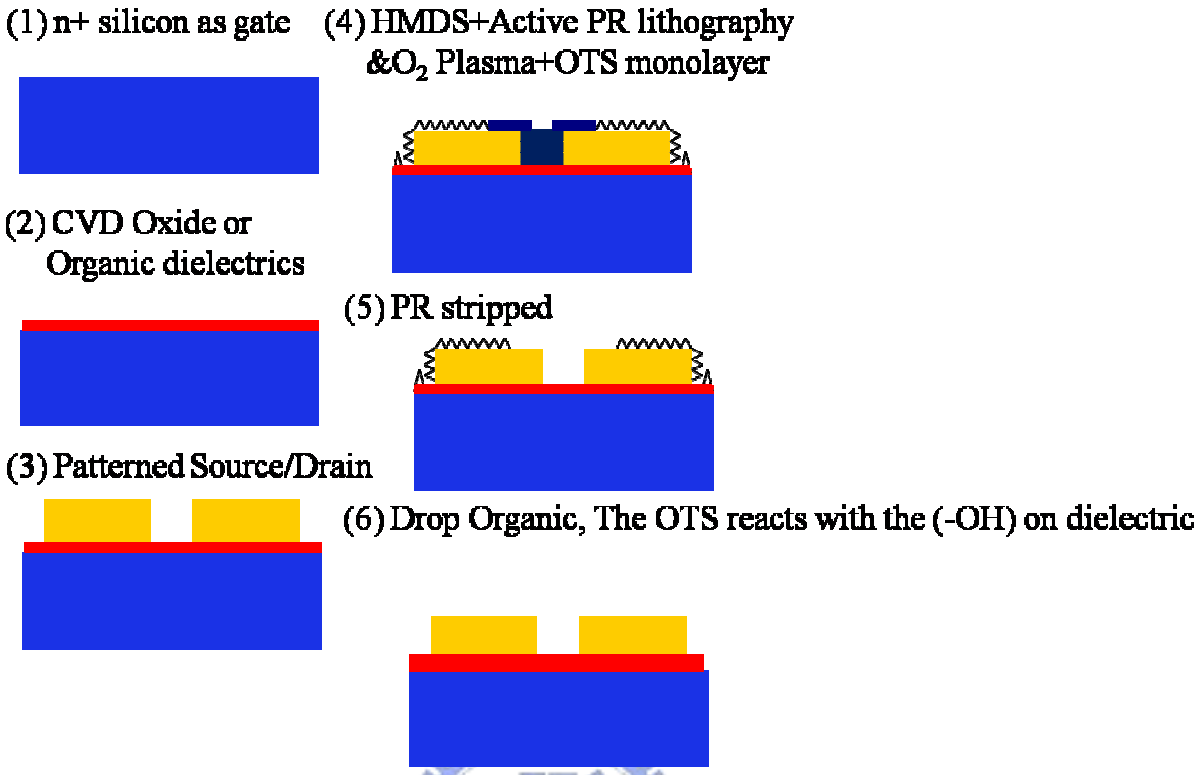


Fig. 3-1 The step process flow was shown to a diagrammatic process flow.

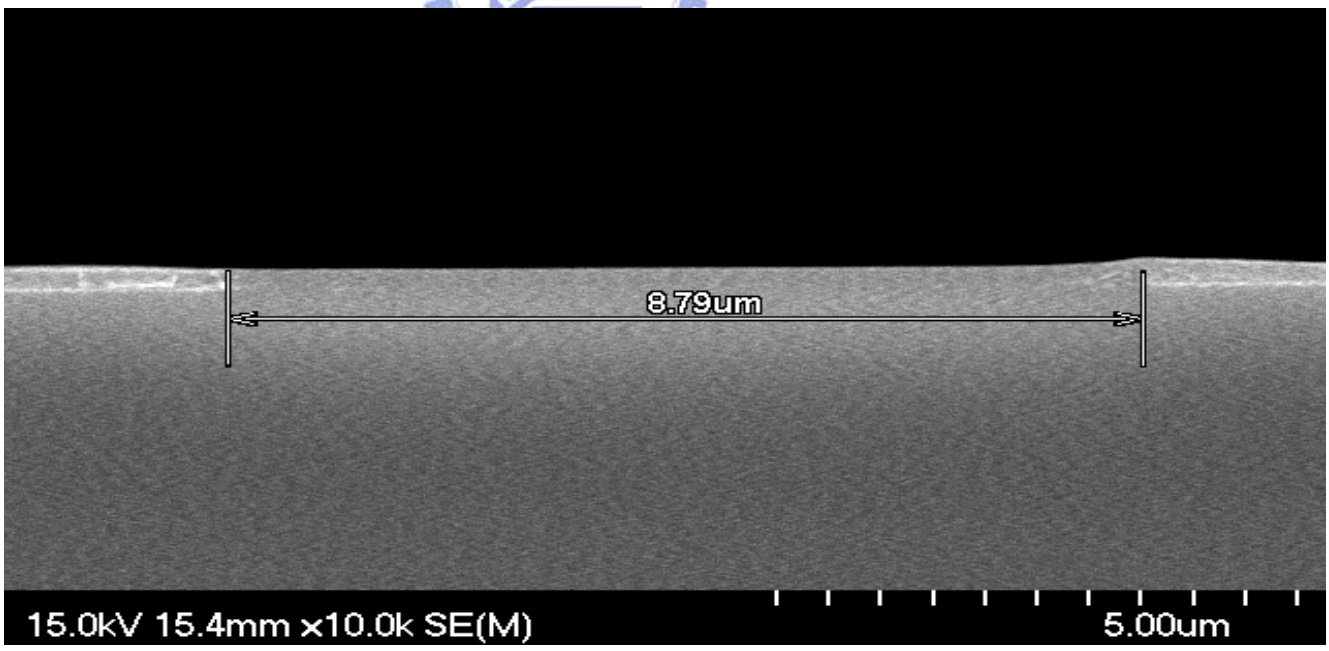
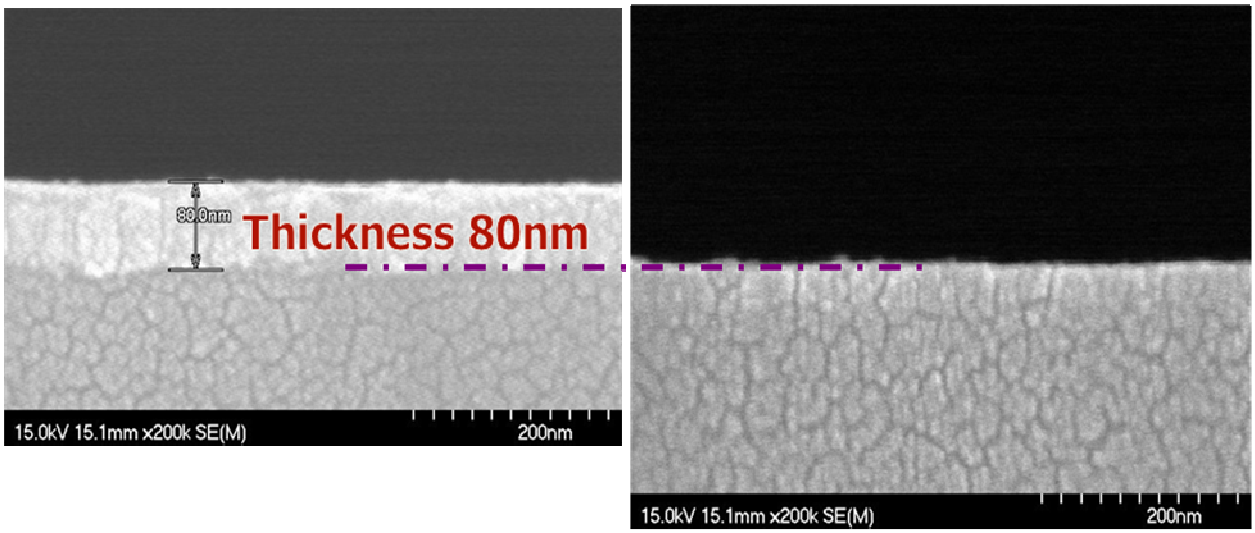


Fig. 3-2 Self-Organized method on the thermal oxide was allowed patterned active region. The channel length was about 10um.



(a) (b)

Fig. 3-3 P3HT thickness on the channel is about 80nm (a). This showed that even if the scale is up to 200nm, the thickness outside the active region was to be close to zero (b).

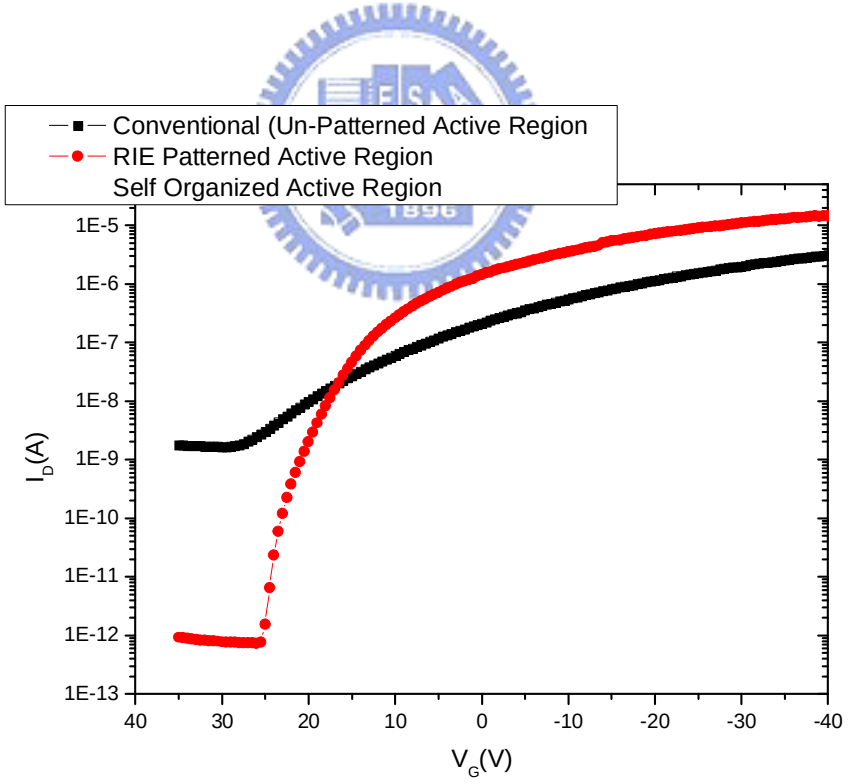
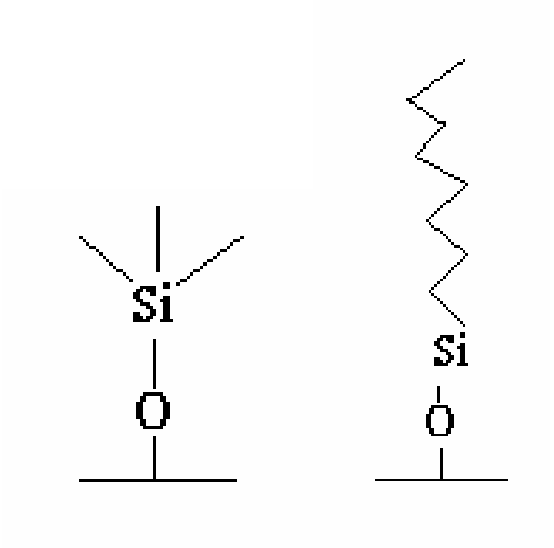


Fig. 3-4 The fig. showed the transfer characteristics of two Self-Organized OTFTs, one without and the other with the patterned P3HT.



(a) (b)

Fig. 3-5 The monolayer of (a) HMDS (b) OTS

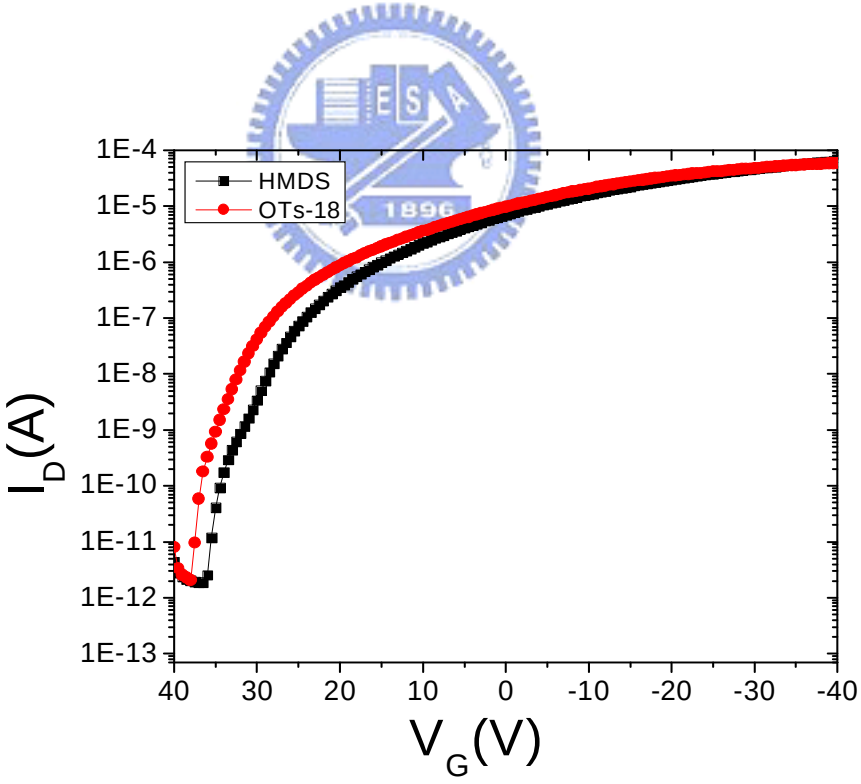


Fig. 3-6 This fig. showed that the I_D-V_G curves of OTFT with different modification layer.

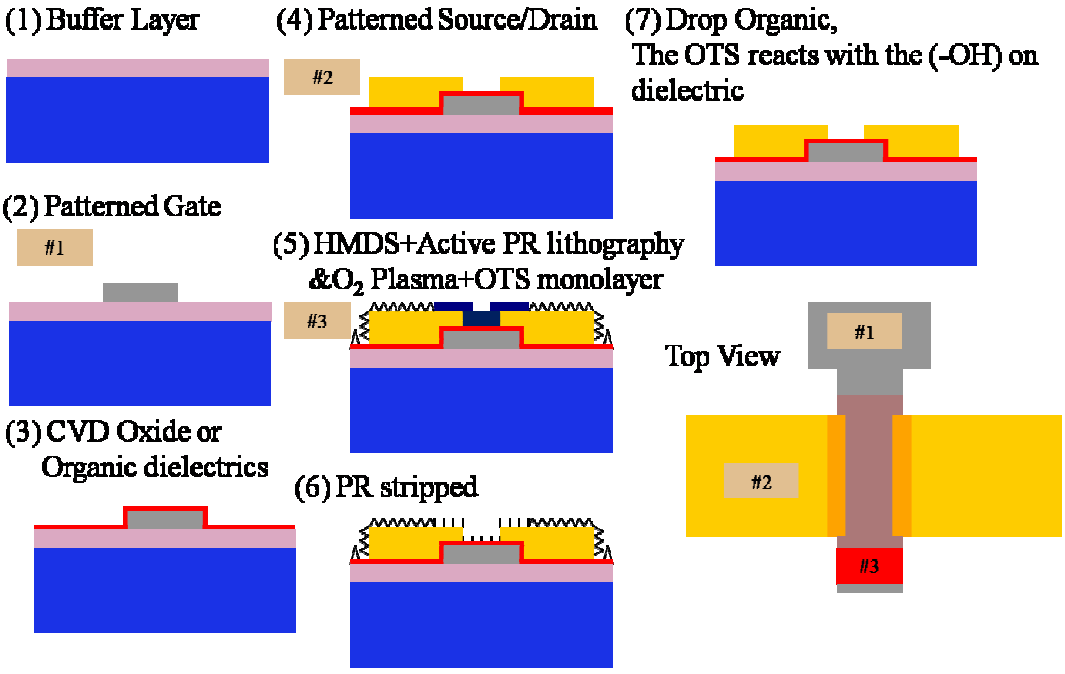


Fig. 3-7 The step process flow of patterned gate and patterned active layer with self-organized was shown to a diagrammatic process flow.

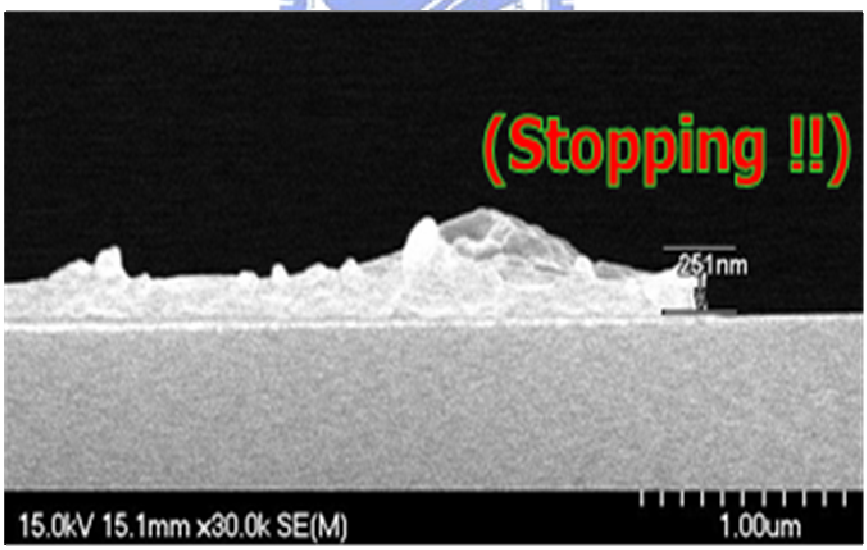


Fig. 3-8 The fig. showed evaporating mechanism of solution which is from center to edge sidewall.

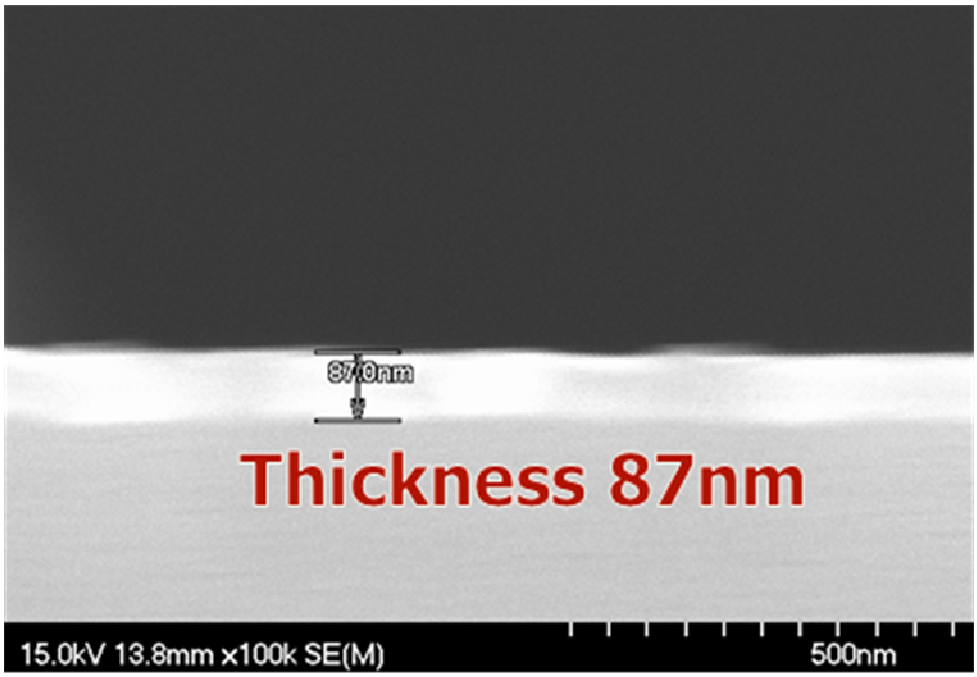
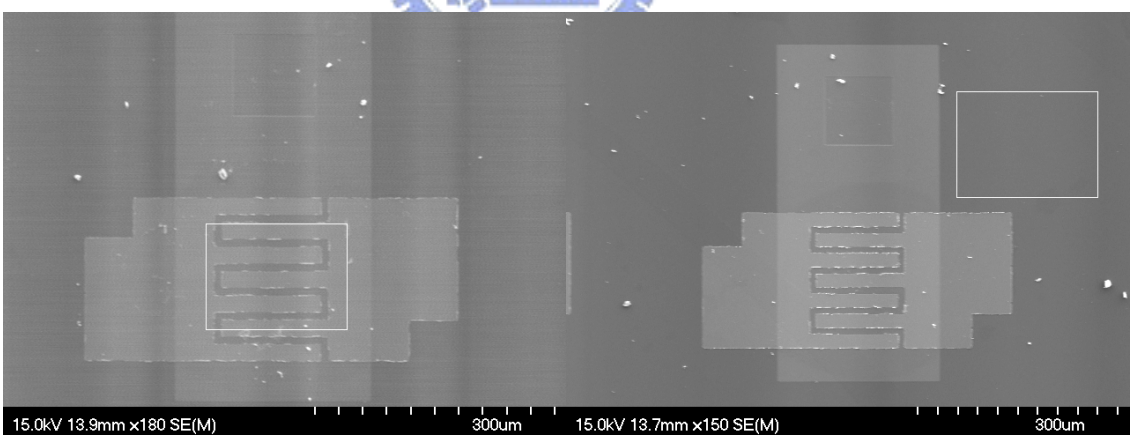


Fig. 3-9 P3HT thickness on the channel was about 87nm.



(a) (b)

Fig. 3-10 The (a) showed the SEM image of the self-organized TFTs. A reference block region was selected inside the active region and outside the active region in (b).

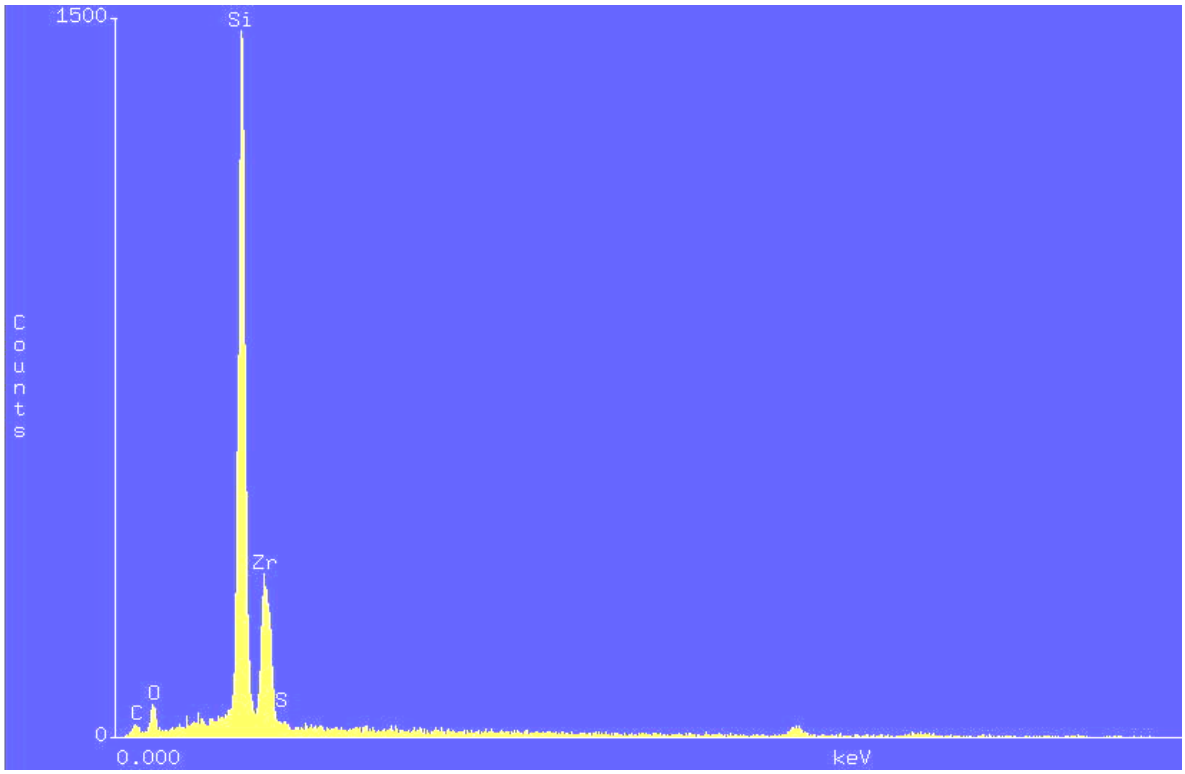


Fig. 3-11 The fig. showed the relative counts of sulfur distribution.

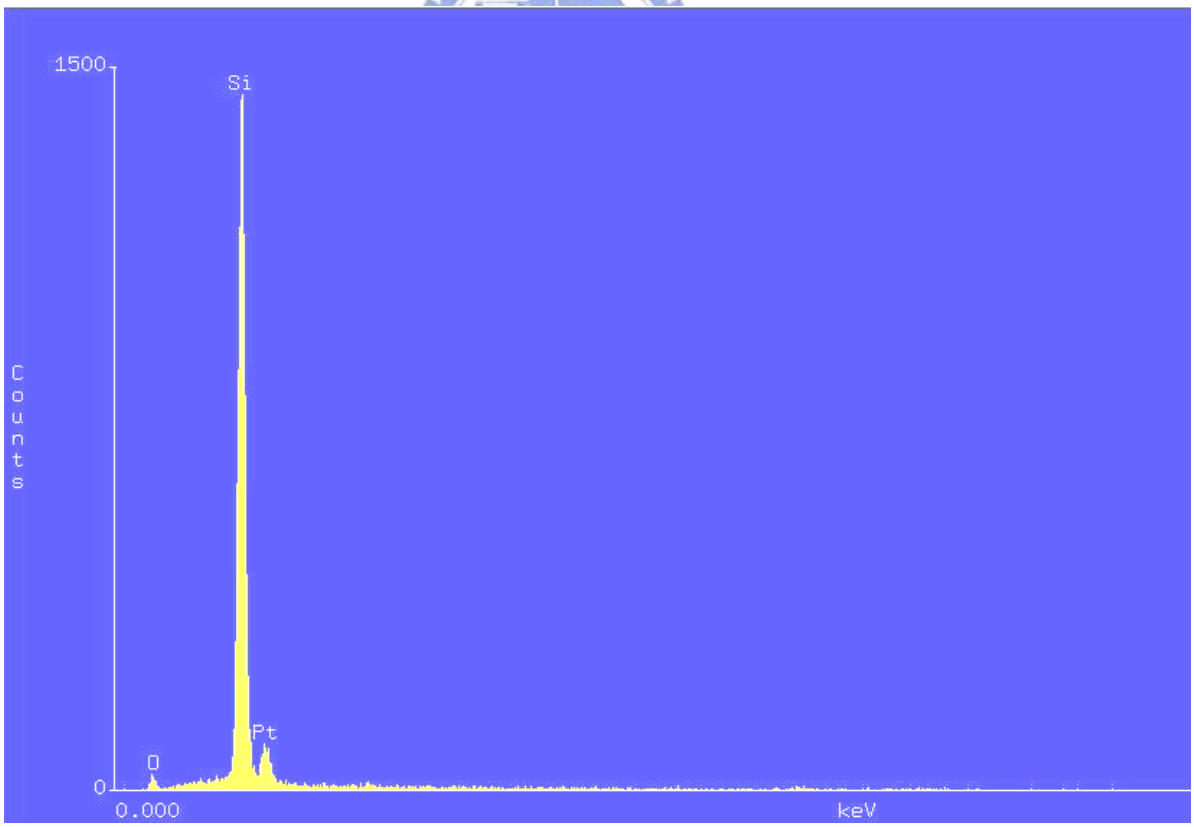


Fig. 3-12 The fig. showed the EDS analyses outside the active region.

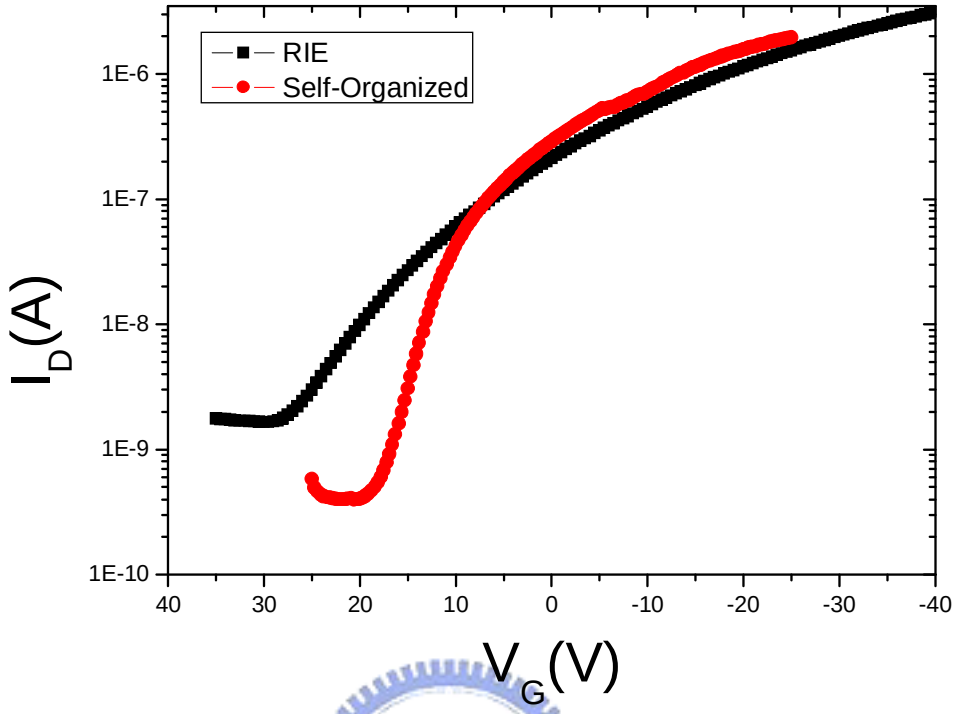


Fig. 3-13 The fig. showed the transfer characteristics of two OTFTs.

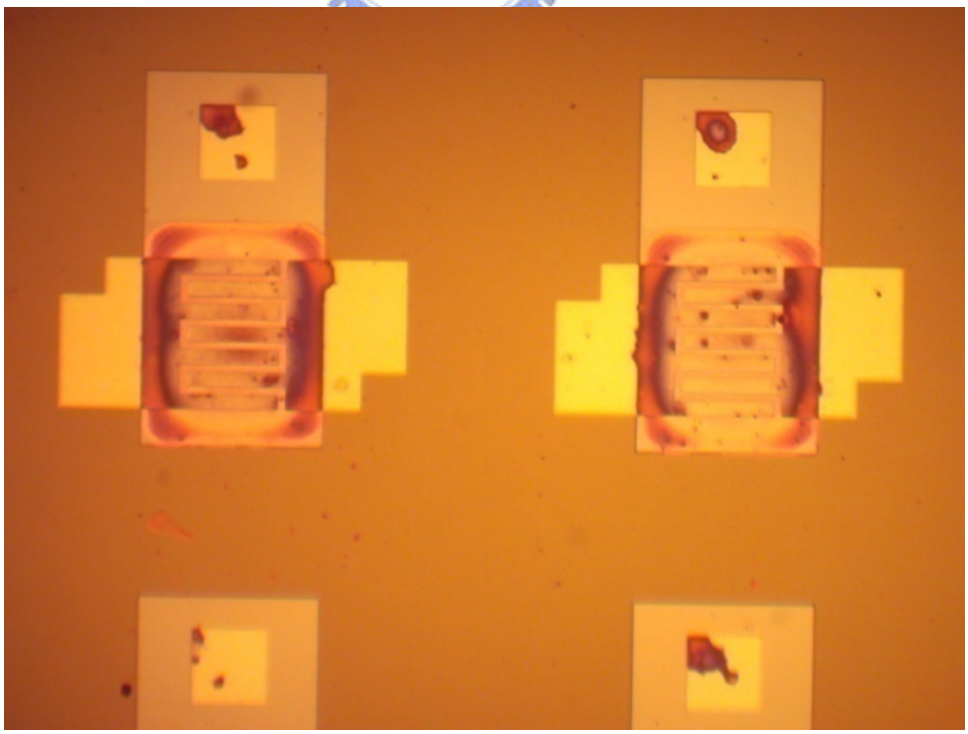


Fig. 3-14 The OM image of PECVD (SiH_4+N_2O@300 ℃) oxide thickness with 100nm.

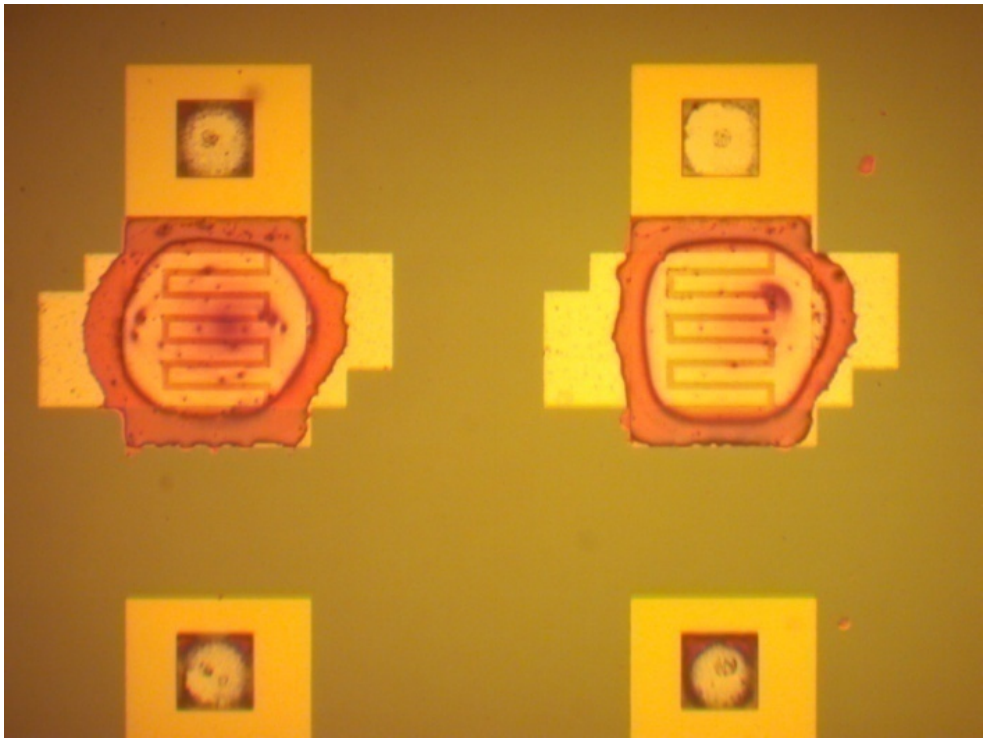


Fig. 3-15 The OM image of PECVD (SiH_4+N_2O@300^{O}C) oxide thickness of200nm.

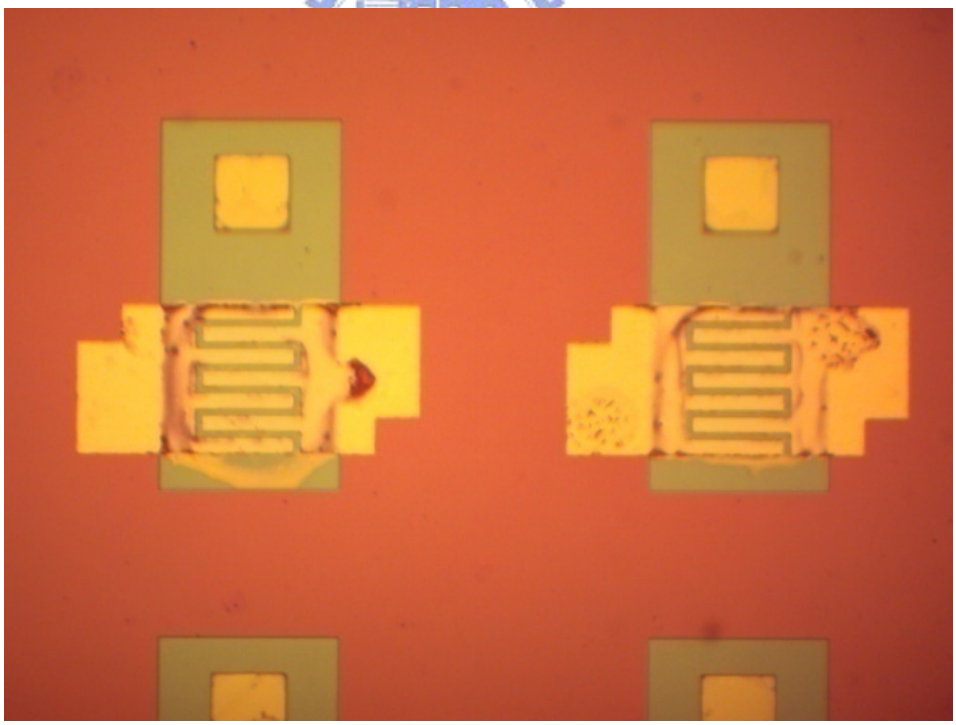


Fig. 3-16 The OM image of PECVD (SiH_4+N_2O@300^{O}C) oxide thicknessof 300nm.

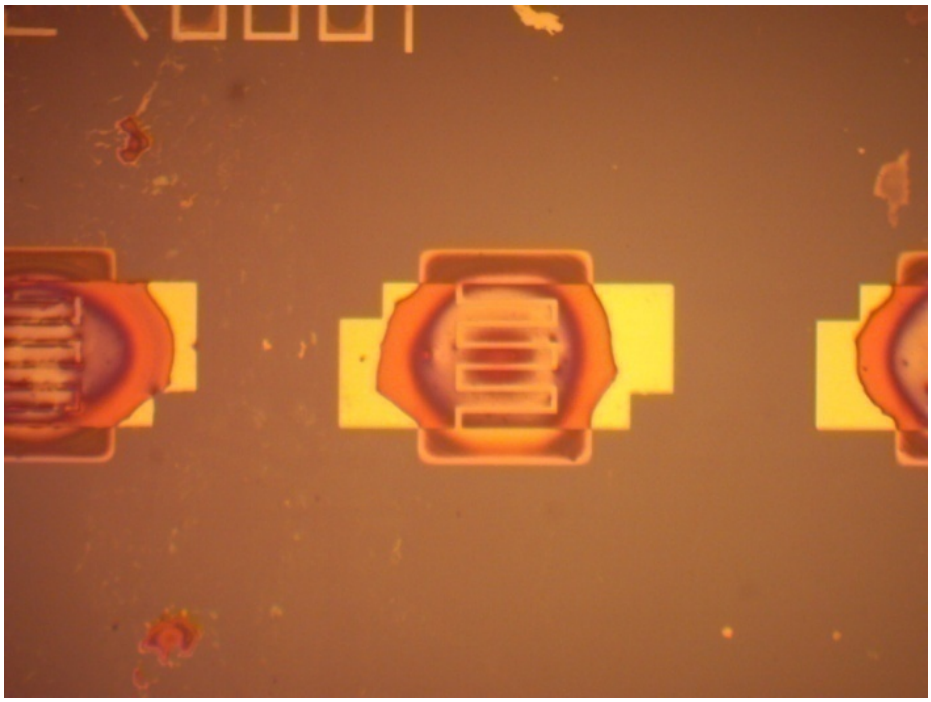


Fig. 3-17 The OM image of Thermal (TEOS@700^{O}C) oxide thickness of 100nm.

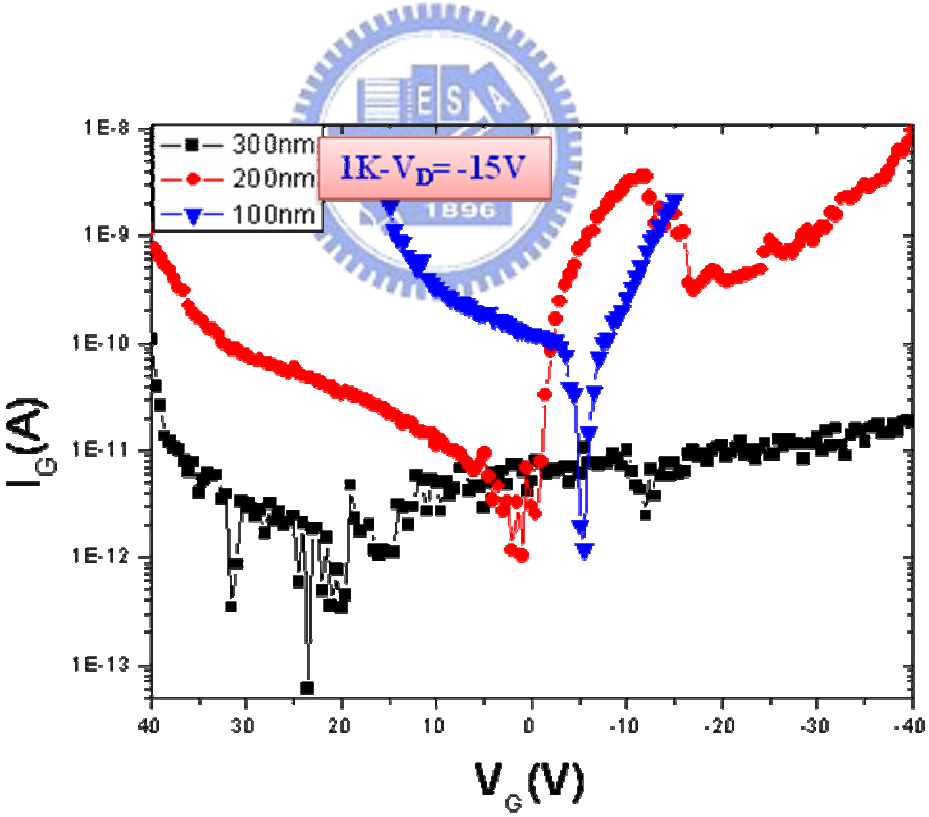


Fig. 3-18 The showed the I_G-V_G characteristics of devices with different gate oxide thickness.

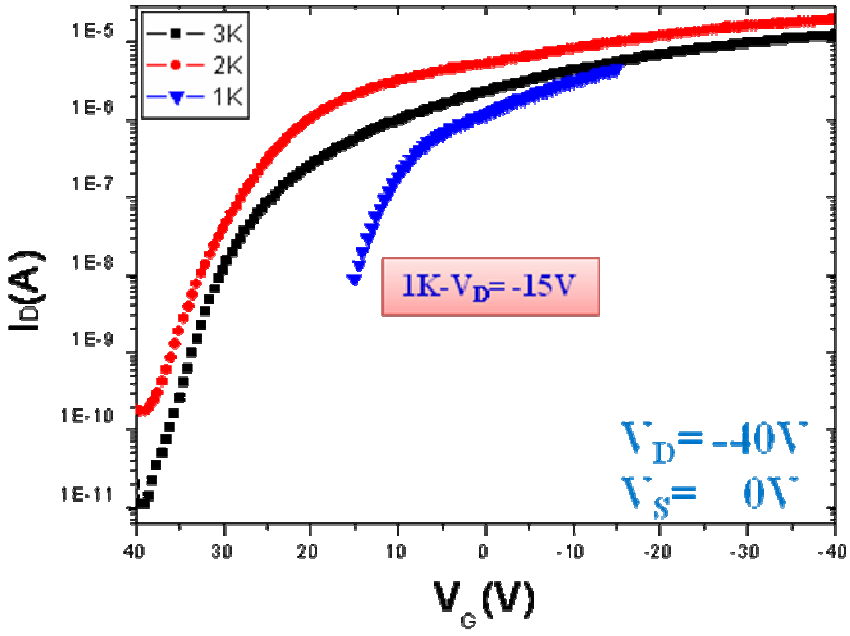
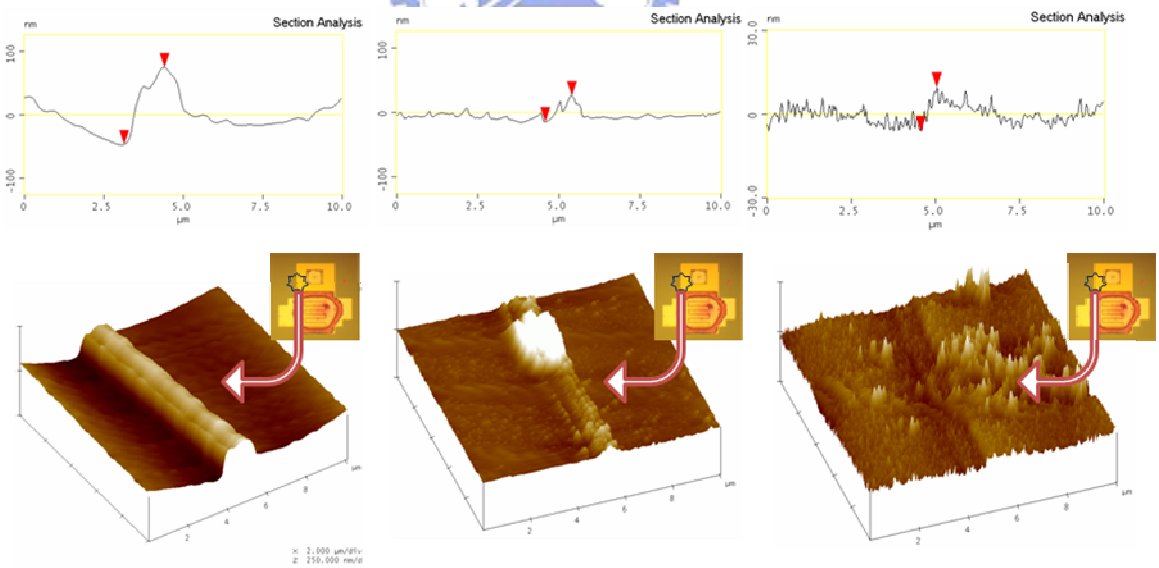


Fig. 3-19 This fig. showed the I_D-V_G characteristics of different gate oxide thickness measured at V_D = -40V.



(a) (b) (c)

Fig. 3-20 The AFM graphs which different thickness oxides were shown in this fig.s (a) 100nm, (b) 200nm and (c) 300nm.

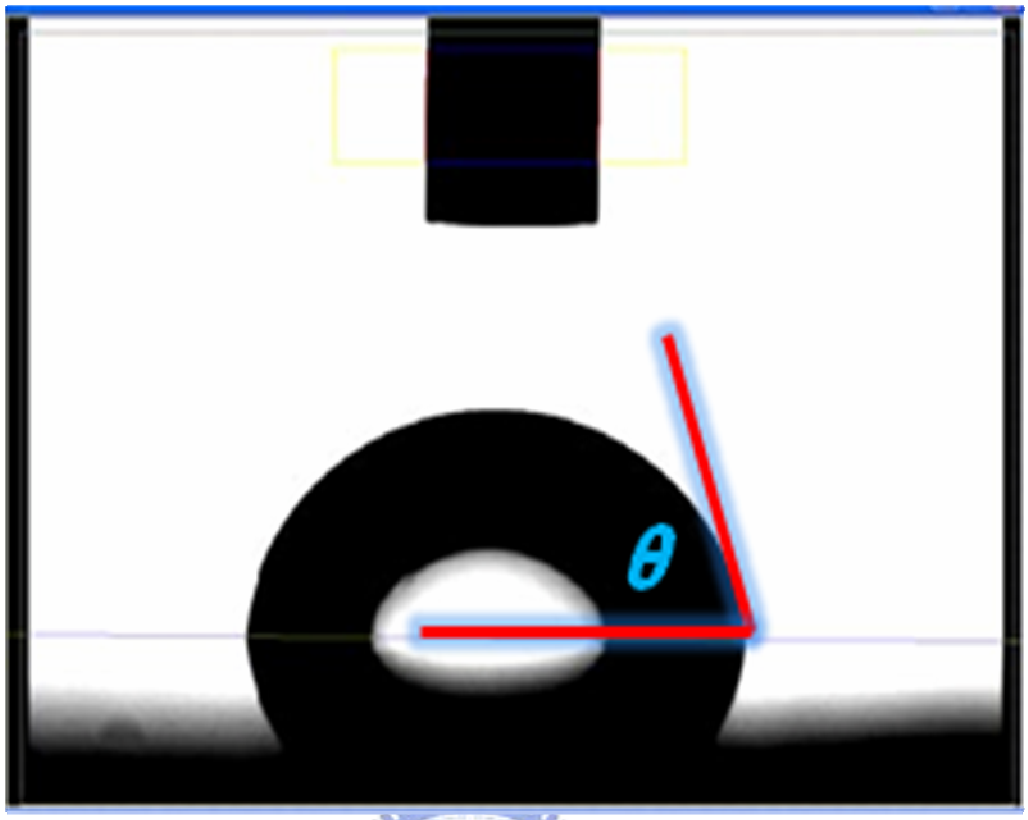


Fig. 3-21 The digitally recorded images, the contact angles of the drops on both sides (left and right) were measured and averaged with digital image analysis software.

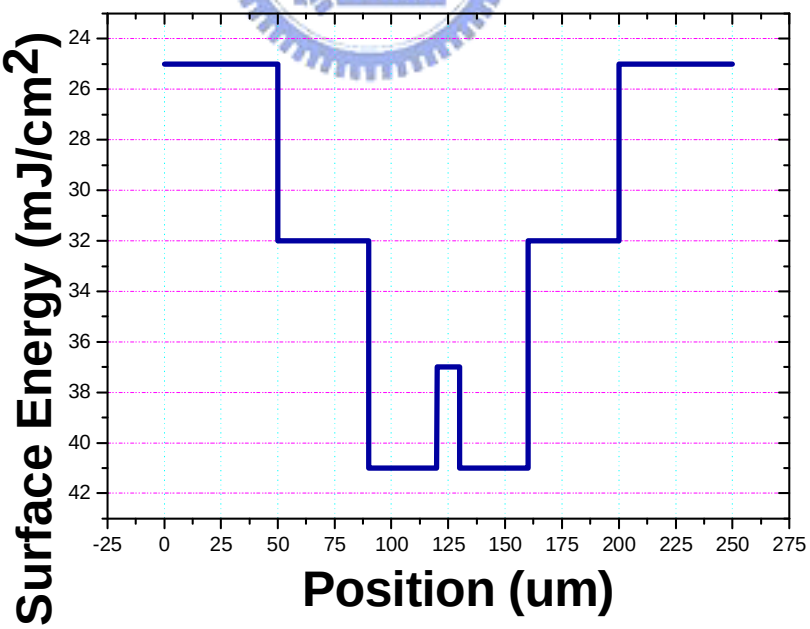


Fig. 3-22 The surface energy computed values in the OTFT device.

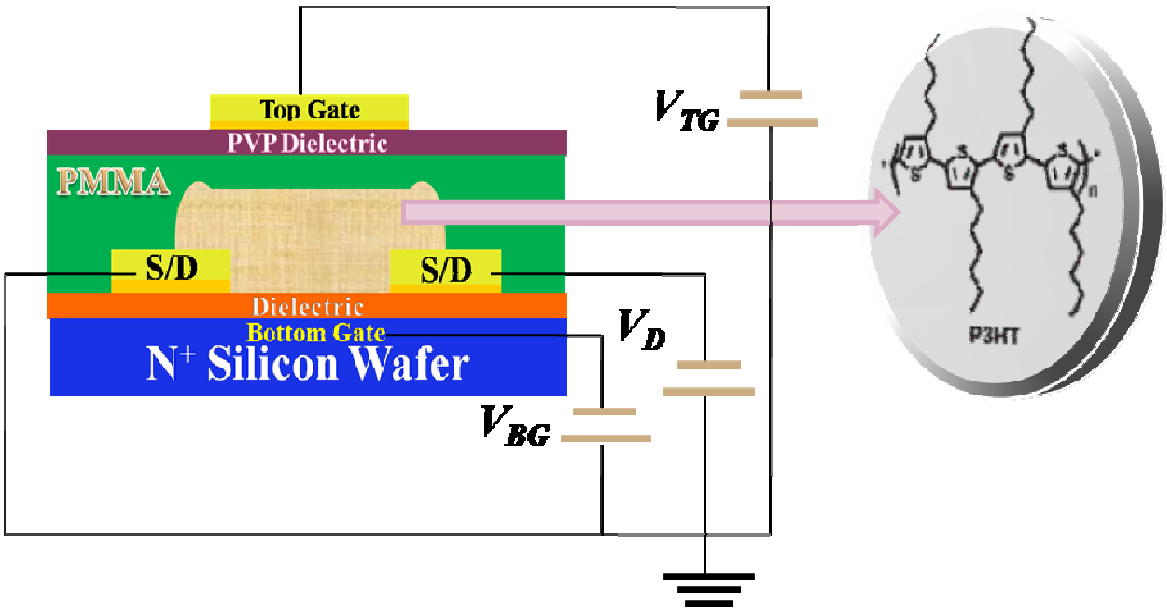


Fig. 4-1 The DG-OTFT, the simplified geometry was described in this fig..

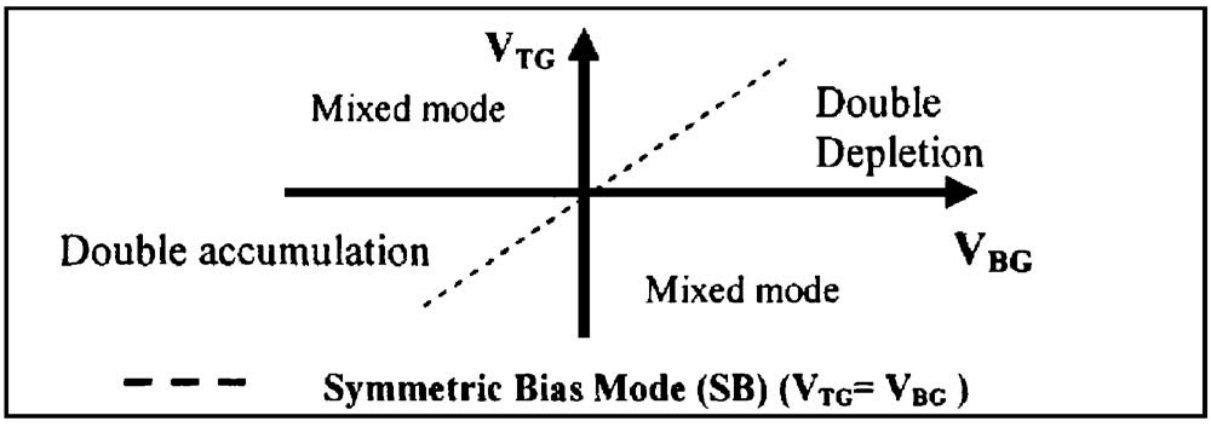


Fig. 4-2 The DG bias modes for the p-type DG-OFET was described in this fig..

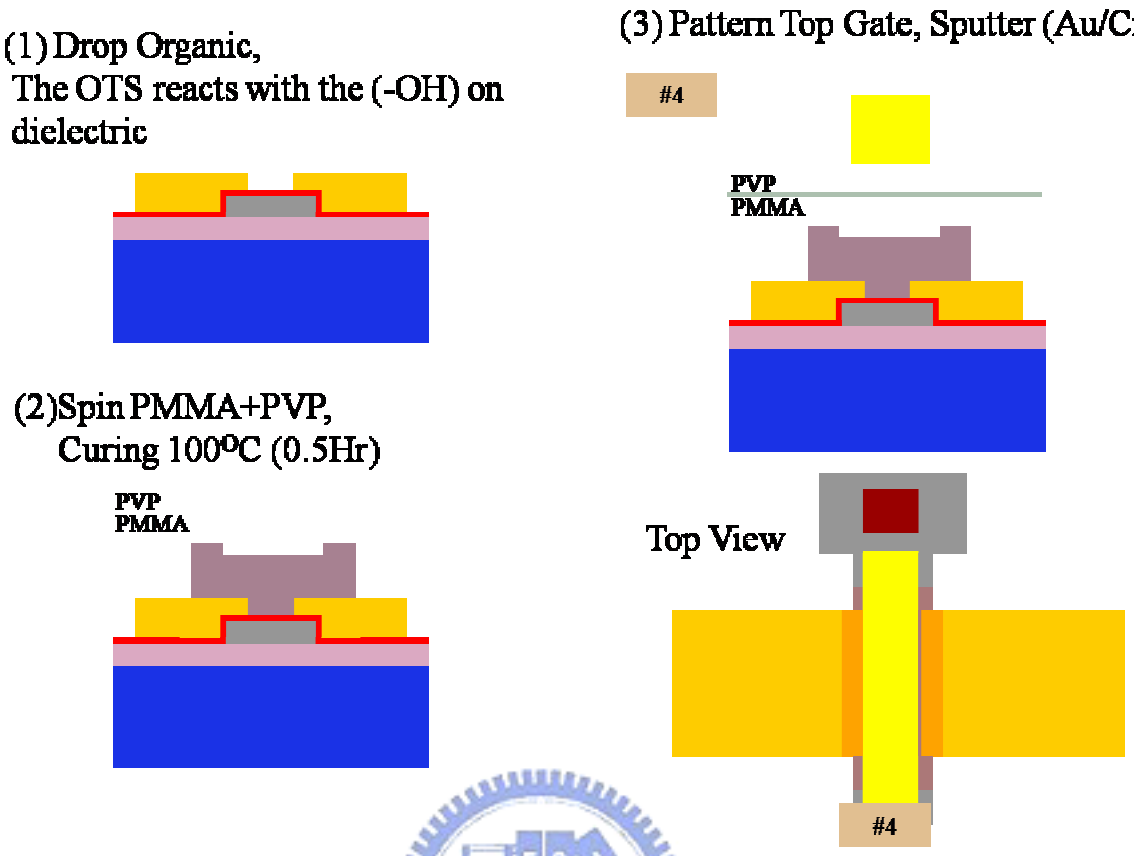


Fig. 4-3 The step process flow of DG-OTFT.

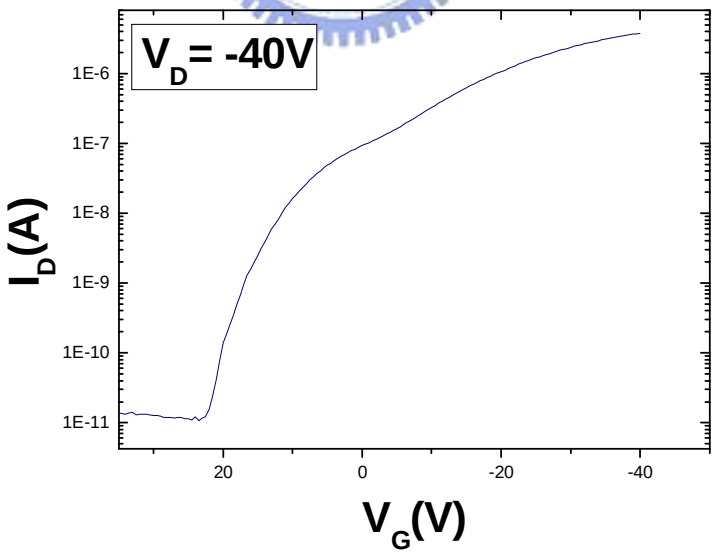


Fig. 4-4 The I_D-V_G electrical characteristics of TG floating and BG biased.

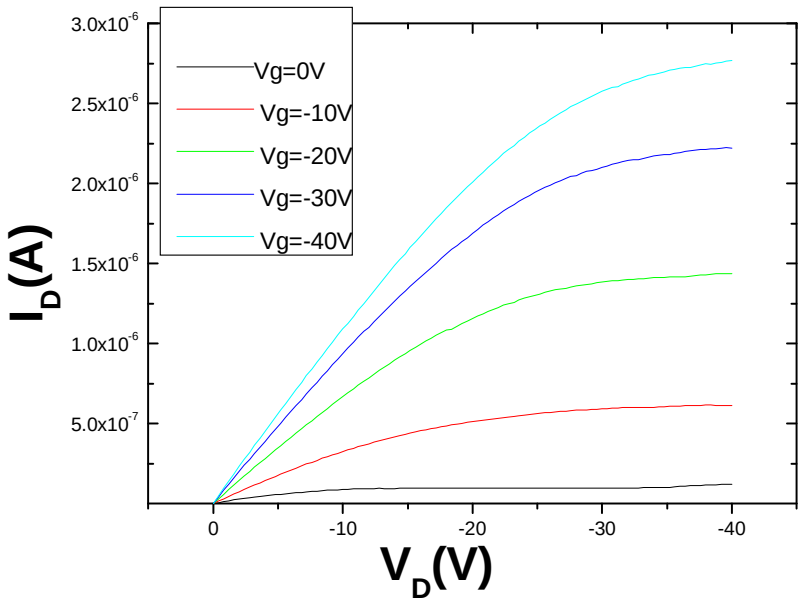


Fig. 4-5 The I_D-V_D electrical characteristics of TG floating and BG biased.

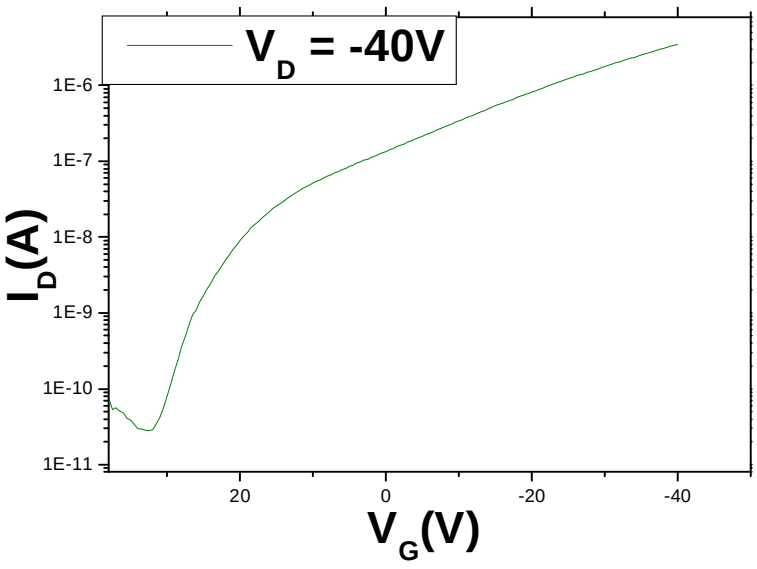


Fig. 4-6 The I_D-V_G electrical characteristics of BG floating and TG biased.

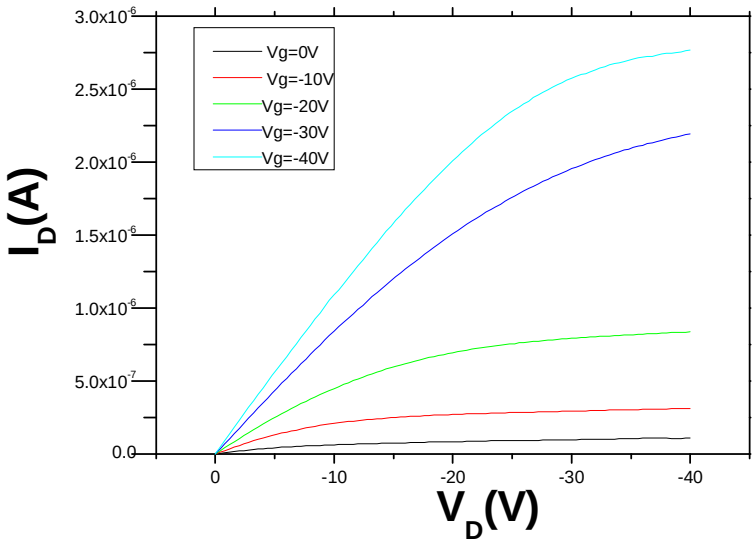


Fig. 4-7 The I_D-V_D electrical characteristics of BG floating and TG biased.

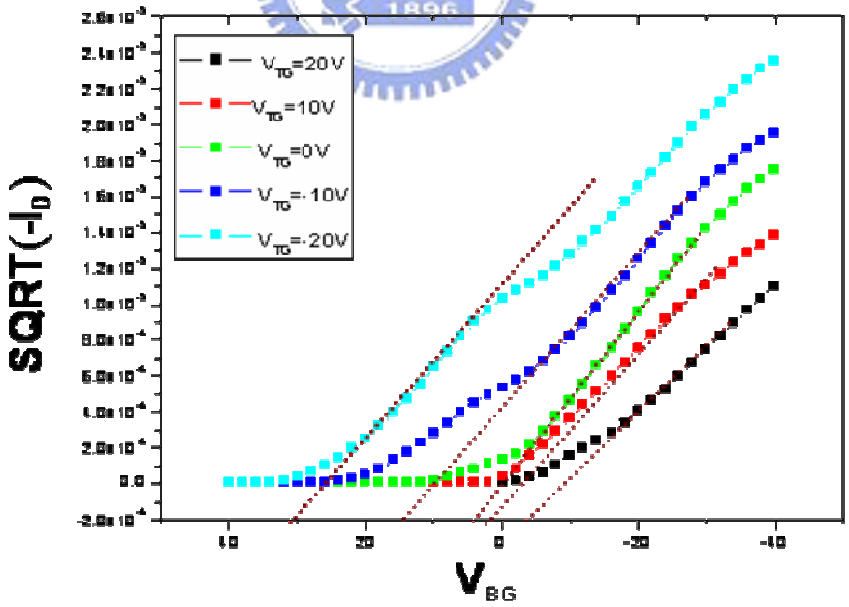


Fig. 4-8 The transfer characteristics of the DG-OTFT were shown in this fig., where the $I_D^{1/2}$ is plotted, respectively, for the asymmetric bias mode (AB).

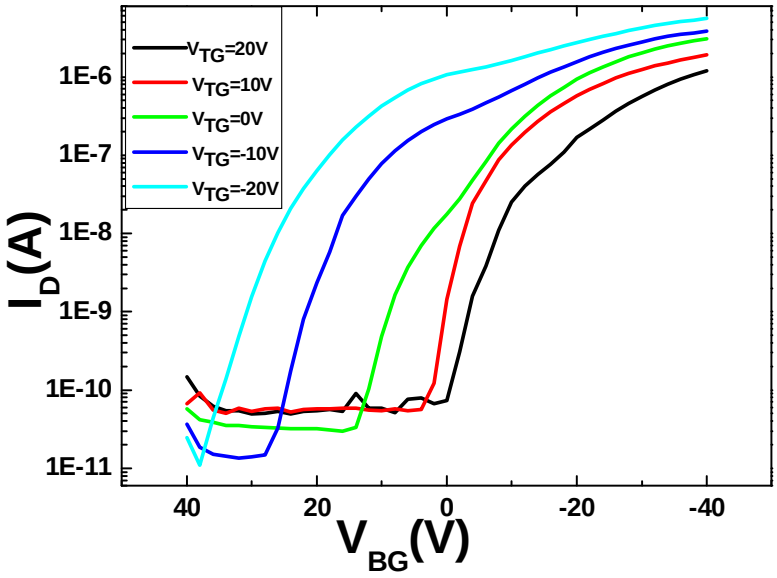


Fig. 4-9 From this fig., it was clear that the set of curves was shifted “up and left” when increased negative V_{TG} voltages.

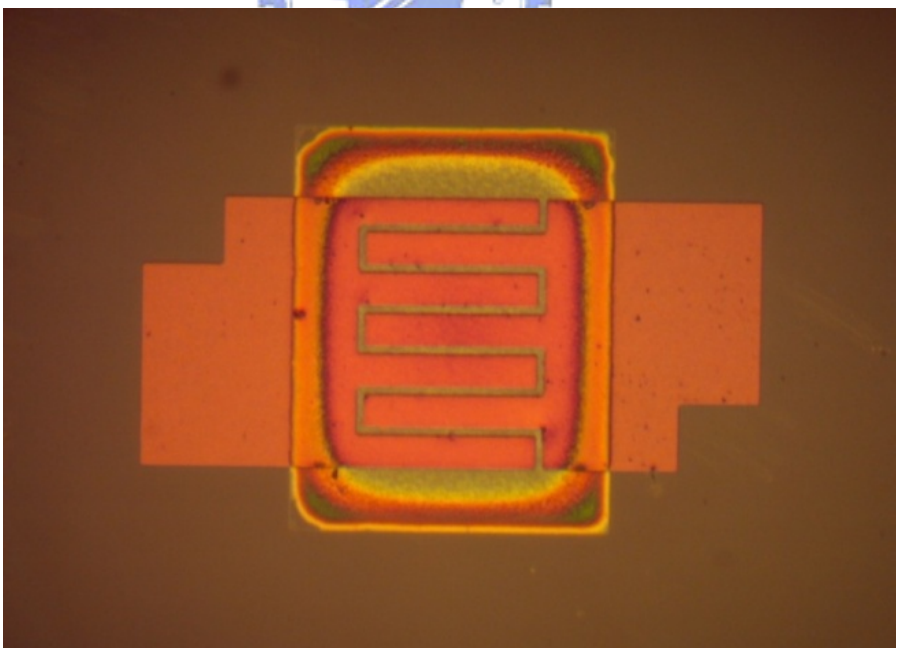


Fig. 4-10 This fig. showed the successful in fabrication F8T2-TFT with self-organized method.

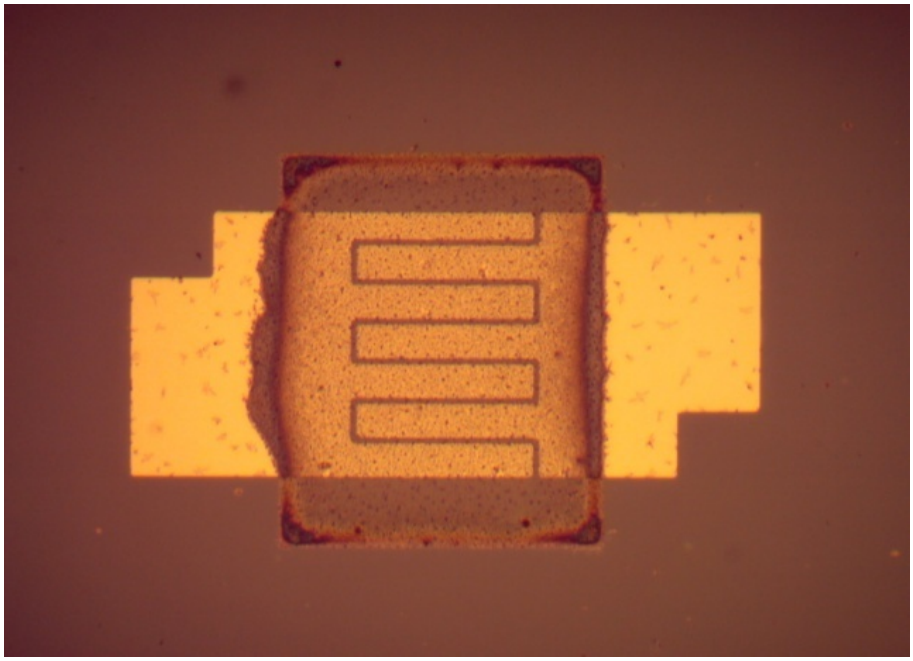


Fig. 4-11 This fig. showed successful in fabrication Pentance-TFT with self-organized method.

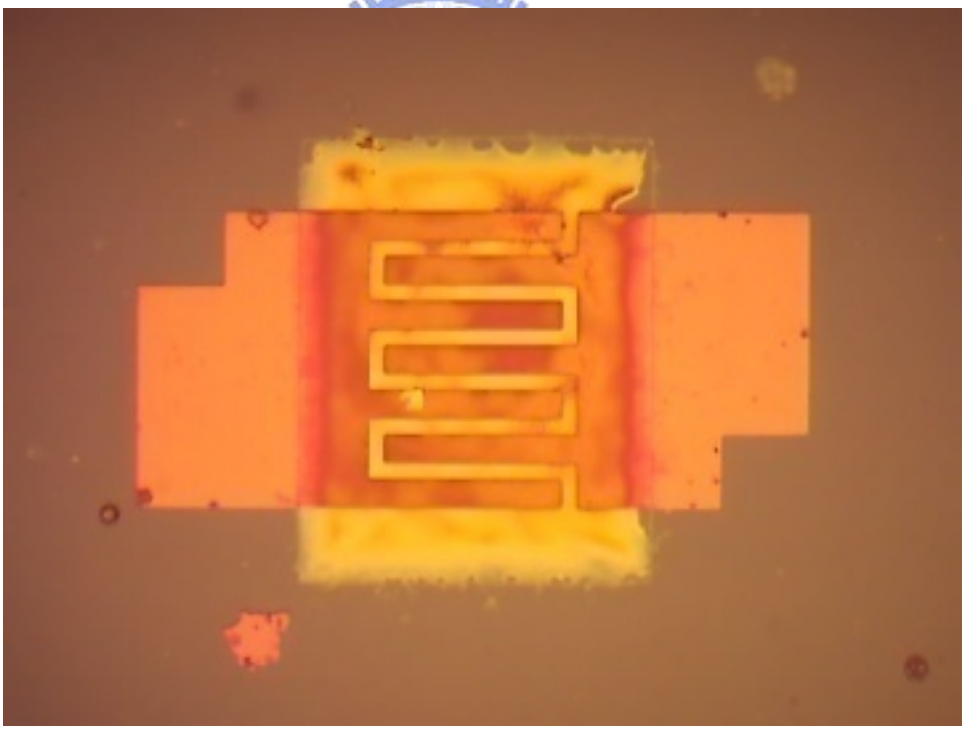


Fig. 4-12 This fig. showed successful in fabrication ZnO-TFT with self-organized method.

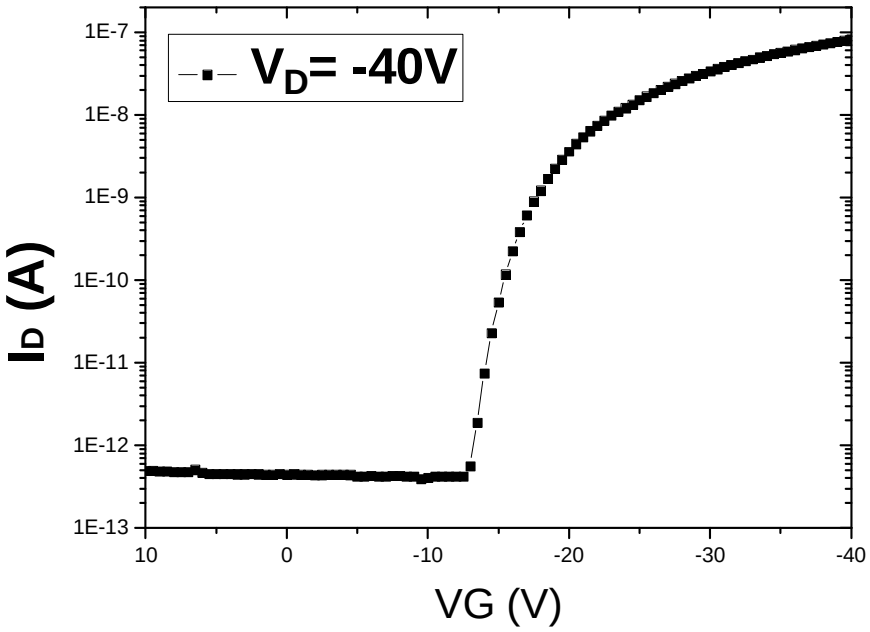


Fig. 4-13 The fig. showed F8T2-TFT I_D–V_G curve.

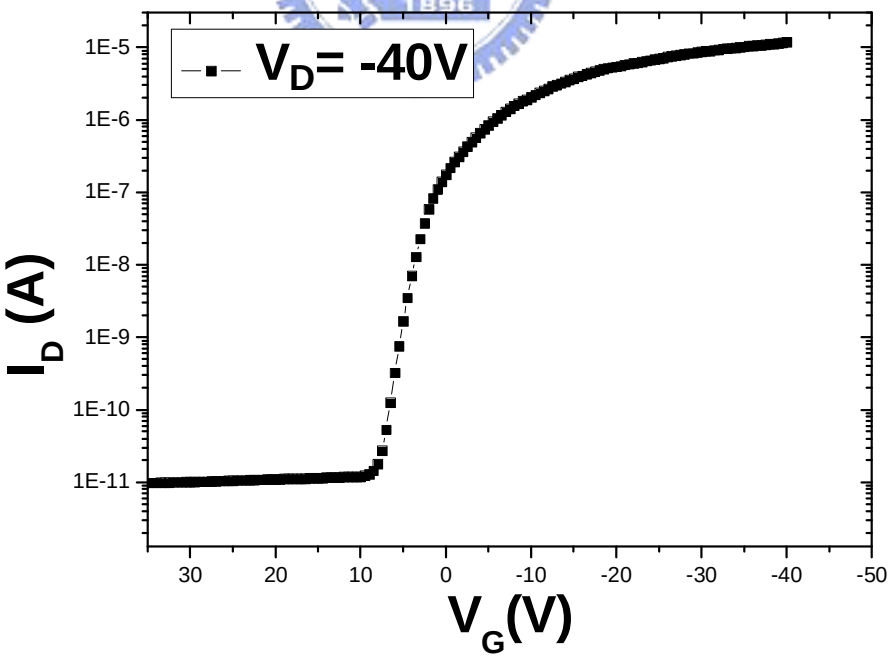


Fig. 4-14 The fig. showed Pentance-TFT to obtain the I_D–V_G curve.

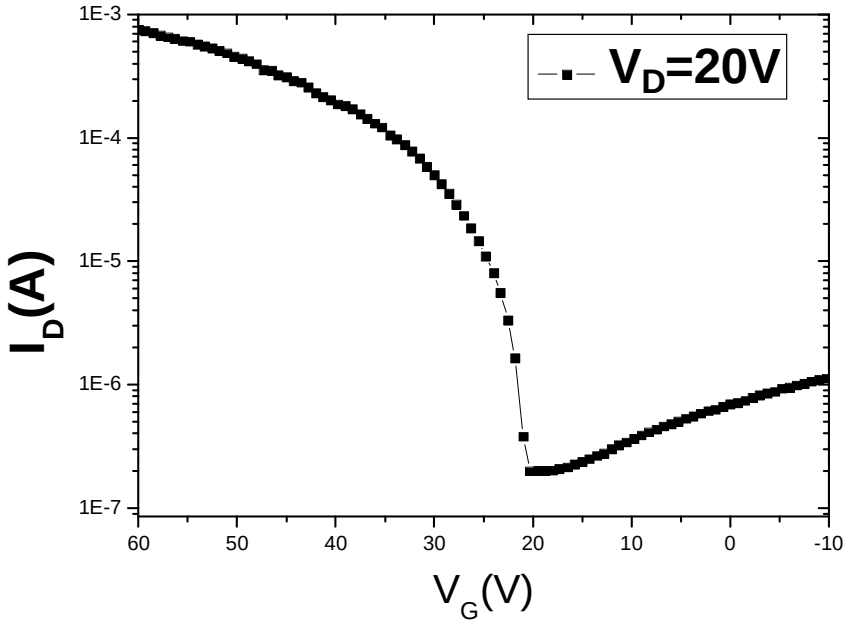


Fig. 4-15 The fig. showed ZnO-TFT to obtain the I_D–V_G curve.

Table 1-1: Comparisons of TFTs with different materials for the channel region.

	Amorphous Si	Poly-Si	Organic
Status	Mature	Development	Result
Mobility(cm^2/Vs)	0.1-1.0	50-200	0.0001-1
Uniformity	Good	Poor	Good
Stability	Poor	Good	Very Poor
Cost	Low	High	Very low
Ion/Ioff	$>10^6$	$>10^6$	10^3-10^8

Table 2-1: The I_{ON}/I_{OFF}, mobility and threshold voltage of conventional, patterned P3HT without patterned gate and patterned P3HT with patterned gate .

	(a) Conventional	**(b) Patterned P3HT**	**(c) Patterned P3HT and Patterned Gate**
Mobility (cm^2/V-s)	**$1.2X10^{-3}$**	**$9.0X10^{-4}$**	**$1.4X10^{-4}$**
I_{ON}/I_{OFF}	**10^3**	**5×10^5**	**2×10^4**
Threshold Voltage (V)	**26.6**	**20.12**	**18.73**

Table 2-2: General requirements of plastic substrates for LCDs.

Parameter	**Require Standards**
Temperature stability	As high as possible
Thermal expansion coefficient	≦ 50 ppm/K
Irreversible shrinking	< 1/20 of pixel pitch
Surface roughness	≦ 10 nm
Transparency	≧ 90%
Permeation of H_2O	< 0.15 g/m^2 24 hr at 40^oC and 90% relative humidity
Permeation of O_2	< 0.1 cm^3/m^2 24 hr
Chemical resistance	etchants, solvents and other chemicals used in display manufacture

Table 2-3: This table summaries substrate properties four organic polymeric backplanes specially synthesized for display fabrication.

PROPERTIES	UNIT	PET	PC	PEN	PI
Density	g/cm^3	1.4	1.2	1.36	1.43
Total Light Transmittance	%	**89**	90	87	<30
Tg	℃	78	150	121	410
Using Temp.	℃	105	125	**180**	240
Heat Shrinkage (150℃/30min)	% (Machine Direction) %(Transverse Direction)	1.5 0.2	0.7 0.5	0.03 0.02	0.2 0.1
CTE	ppm/℃	**15**	70	**13**	20
Moisture Absorption	%	**0.14**	0.4	**0.14**	1.3

Table 3-1: The characteristic of these two OTFTs was listed in this table.

W/L=1k/10	***u*** **(cm^2/V.s)**	**on/off**	**V_t(V)**
Self-Organized Active Region	**$2.79x10^{-3}$**	**$1.96x10^{7}$**	**17.44**
Conventional (Un-Patterned)	**$3.8x10^{-4}$**	**$2.1x10^{3}$**	**26.6**

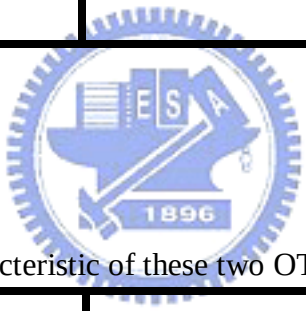


Table 3-2: The characteristic of these two OTFTs was listed in this table.

W/L=1k/10	***u*** **(cm^2/V.s)**	**on/off**	**V_t(V)**
RIE-Patterned Active Region	**$1.4x10^{-4}$**	**$2x10^{4}$**	**20.12**
Self-Organized Active Region	**$7.5x10^{-4}$**	**$1.95x10^{4}$**	**14.85**

Table 3-3: The table showed measured V_{th} increases with gate oxide thickness.

W/L= 1000um/10um	***u*** **(cm^2/V.s)**	**on/off**	**V_{TH} (V)**
100nm	**$2.90x10^{-3}$**	**$5.14x10^{2}$**	**16.43**
200nm	**$4.69x10^{-3}$**	**$1.30x10^{5}$**	**27.62**
300nm	**$4.24x10^{-3}$**	**$\underline{1.18x10^{6}}$**	**33.35**

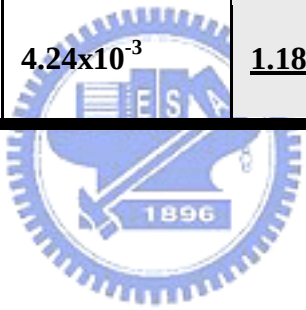


Table 3-4: The sessile drop contact angle method with two probe liquids, there was used to measure the surface energy of treated HMDS and OTS surfaces treatment.

Probe liquid	γ_L (mJ/m^2)	γ_L^d (mJ/m^2)	γ_L^d (mJ/m^2)
Diiodomethane	50.8	50.8	0
Water	72.8	21.8	51

Table 3-5: The average measured contact angles obtained from differentially treated HMDS and OTS composite surfaces utilizing a series of probe liquids.

$r_s^{Total} = r_L^D \times r_S^P$	**Diod' angle**	**H_2O angle**	r_S^D	r_S^P	**Surface Energy**
SiO_2 bare	53.9	61.5	32.074	14.641	46.715
SiO_2 HMDS	59.46	74.8	28.886	8.524	37.409
SiO_2 plasma	43.15	25.76	37.991	32.009	70.001
SiO_2 plasma OTS	69.67	98.2	23.058	1.514	24.572
Pt bare	40.87	86.96	39.170	1.627	40.797
Pt HMDS	41.9	85.2	38.641	2.129	40.771
Pt Plasma	35.8	87.62	41.655	1.185	42.841
Pt Plasma OTS	56	95.07	30.875	1.027	31.902

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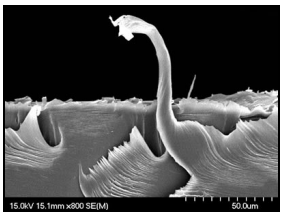
Image in Focus 國際特殊發表：

[1] **Cheng-Chin Liu** "Chinese mystical bird? ", *Materials Research Society :Materials360*, Issue 2, January 2008



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（88 年 9 月~92 年 6 月）

國立交通大學電子工程研究所碩士班

（95 年 9 月~97 年 6 月）

論文題目:新穎自我定位有機/無機薄膜電晶體於軟性電子應用之研究

Study on the Novel Self-Organized Organic /Inorganic Thin Film Transistors for the Flexible Electronics Applications