新式複晶矽奈米線元件製作與特性分析

Fabrication and Characterization of Novel Poly-Si Nanowire Devices

研 究 生:劉大偉　　　　Student: Ta-Wei Liu
指導教授:林鴻志 博士　　Advisors: Dr. Horng-Chih Lin
　　　　 黃調元 博士　　　　　　 Dr. Tiao-Yuan Huang

國立交通大學
電子工程學系 電子研究所碩士班

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摘　要

在本篇論文中，我們利用簡單、低成本而且富變化性的方法製作數種具有相同奈米線型狀，但是不同閘極組態的複晶矽奈米線元件，這些元件有助於我們探討多閘極對於奈米線元件的基本電性和特性變異度的影響。相較於平面結構元件，實驗結果證明奈米線具有較好的次臨界擺幅(subthreshold swing)、較低的漏電流，以及較大的開關電流比(on/off current ratio)。我們實驗的數據也顯示，當奈米線的通道表面被閘極覆蓋的比例愈大時，由於具有較高的表面體積比(surface-to-volume ratio)，會展現出更好的特性。我們也藉由臨界電壓(threshold voltage)的標準差和閘極寬度、長度乘積開根號($\sqrt{WL}$)的關係來探討不同元件之間特性的變異度，發現環繞全閘極(gate-all-around)結構的奈米線元件呈現出最穩定的臨界電壓控制能力，而平面元件由於有較大的空乏區以及較差的電漿修補效果，因此不同元件之間的臨界電壓差異性較大。

此外，我們也製作三閘極(tri-gate)奈米線結構的 SONOS 元件。相較於平面結構，奈米線元件的寫入和抹除速度有很明顯的改善；在可靠度議題方面，奈米線元件擁有不錯的電荷儲存能力(retention)和忍耐力(endurance)，它可以承受超過 10000 次的重複寫入/抹除，並且在十年後仍然維持大於 0.5V 的記憶窗(memory window)。

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Dr. Tiao-Yuan Huang

Department of Electronics Engineering and Institute of Electronics
National Chiao Tung University, Hsinchu, Taiwan

ABSTRACT

In this thesis, several multiple-gated (MG) poly-Si nanowire (NW) devices were fabricated and characterized. Our fabrication process is simple, low cot, and flexible for fabricating devices with identical NW structure but different gate configuration. It thus allows us to investigate the impacts of MG on the basic electrical characteristics as well as the variation of devices. The experimental results show that, as compared with devices with planar structure, much improved device characteristics in terms of better subthreshold swing, lower leakage, and higher on/off ratio are obtained. Among all NW structures, superior device performance is achieved as the gated portion of NW channel surface increases, owing to the higher surface-to-volume ratio. We also study the device variation issue by plotting the standard deviation of V_{TH} as a function of $\sqrt{WL}$. We found that the device with gate-all-around configuration exhibits the

best control in terms of the variation. Besides, the deviation of planar devices is evidently higher than the NW ones because of wider depletion width and worse plasma treatment efficiency.

Tri-gated SONOS devices were also fabricated and characterized with a process flow modified from the aforementioned one. It is confirmed that the NW devices have higher P/E speed than planar ones. For reliability issue, NW SONOS devices possess good retention and endurance characteristics. The memory window is larger than 0.5V after 10 years for a device after subjecting to 10^4 times of P/E cycles.

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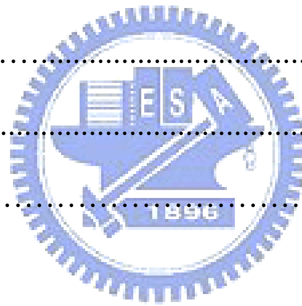

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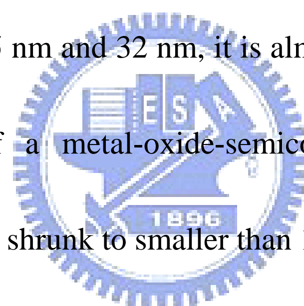
CHAPTER 1

Introduction

1-1 Overview of Nanowire and Multiple-Gate Structures

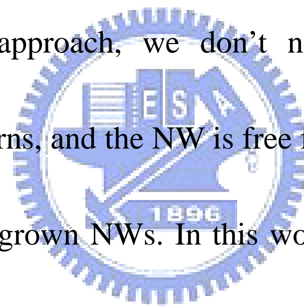
Since the invention of the transistor by Bell laboratory in 1947 and the integrated circuit (IC) in 1958, the semiconductor industry has grown explosively. Sixty years ago, While the state-of-the-art technology is now firmly at 65 nm technology node and rapidly moving toward 45 nm and 32 nm, it is almost impossible to imagine sixty years ago that the size of a metal-oxide-semiconductor field-effect transistor (MOSFET) could someday be shrunk to smaller than 1 micrometer.



As device dimensions shrink into nano-scale, gate control ability is weakened by drain due to high lateral electrical field penetration from drain to source [1], known as short channel effects (SCEs). To cope with this issue, multiple-gate (MG) configurations, such as double gate [2], FinFET [3], tri-gate [4], Ω-gate [5] and gate-all-around (GAA) [6], are very promising for 32nm node and beyond. Channel potential of these devices is controlled by the MG configuration, and a better capability is expected [7]-[9]. In the same planar width, MG devices have additional vertical direction channels to increase the effective channel width and thus the drive

current.

On the other hand, nanowires (NWs) possess high surface-to-volume ratio, making it attractive for a number of applications, including memory [10], thin-film transistors (TFTs) [11], light-emitting diodes (LEDs) [12], and sensors of biological or chemical species [13][14]. However, the formation of NWs usually needs complicated process flow or costly process and/or tools, hindering their further development. To address the issue, we have recently developed a simple and low-cost method to fabricate the MG NWs, which is different from conventional top-down or bottom-up methods [15]-[17]. In our approach, we don't need any costly and advanced equipment to form NWs patterns, and the NW is free from metal contamination which may occur in metal-catalytic grown NWs. In this work a modified process has been developed to fabricate MG NW devices, and details of the process flow will be described in Chapter 2.



1-2 Overview of Variation in Device Characteristics

For IC technology, scaling is not only in accordance with shrinkage of device dimensions, but also the lowering of operation voltage in order to reduce power consumption and maintain good reliability [18]. In early generations with large dimensions, operation voltage was high and the fluctuation of device characteristics

was negligible. However, when the device size becomes small and the operation voltage is reduced, variation in device parameters becomes a major issue and may disturb normal function of circuit operation [19].

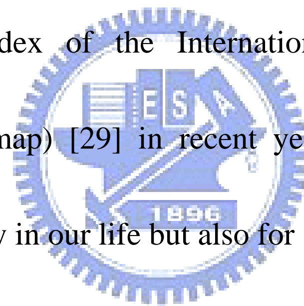
There are various fluctuation sources with regard to threshold voltage (V_{TH}), such as grains in poly-Si gate [20], oxide thickness [21], edge roughness [22], dopants [23]-[25], and so forth. Random dopant placement is considered to have significant weight to cause V_{TH} fluctuation in small-geometry MOSFET. In general, the number of dopants in the channel depletion region is merely a few hundreds for a 0.1μm-scale device. For instance, a MOSFET with gate length/width (W/L) = 65/200nm and substrate doping concentration=1×10^{18} cm^{-3}, the total number of dopant is only 454. If device shrinks into 32nm and beyond, dopant number would be less than 100. As a result, a small variation in dopant number in the depletion region may lead to a significant V_{TH} difference. Unfortunately, doping profile in the channel is difficult to control in either vertical or horizontal direction when device is scaled down.

To overcome this aggravated problem, there have been several proposals for reducing V_{TH} variation. One possible way is to change the gate material from poly silicon to metal or silicide [26]. By this manner, gate depletion can be suppressed and thus reduce one deviation origin in V_{TH}. Another possible way is to use silicon-on-insulator (SOI) structure [27][28]. By adopting a gate material with

appropriate work function to adjust the V_{TH} of the device, the channel can be undoped to avoid the aforementioned issue associated with the random dopant fluctuation.

1-3 Overview of SONOS Flash Memory

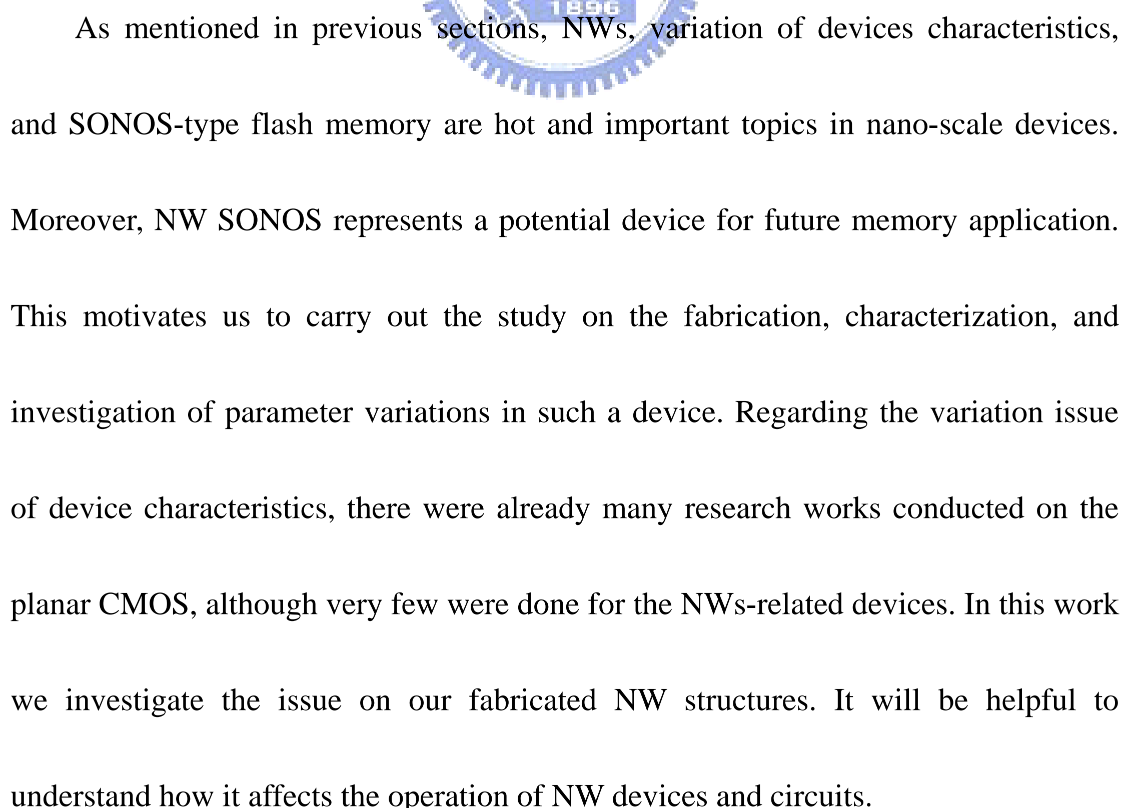
Nowadays, the market of flash memory has dramatically increased, and the relating products, such as mobile phones, digital cameras, MP3, personal digital assistants (PDAs), and other storage medium for personal appliances, have become part of many persons' life. Moreover, the technology node of flash memory has become an authoritative index of the International Technology Roadmap for Semiconductors (ITRS roadmap) [29] in recent years. Hence, the status of flash memory is substantial not only in our life but also for semiconductor industry.



In contemporary market, high density and low cost are the basic requirements for flash memory. Unfortunately, conventional floating-gate flash memory has been facing fierce challenges in device scaling. For example, as the distance between two floating gates is shortened, coupling inference may cause the data disturbance [30]. Floating gate also suffers from the large stress-induced leakage current (SILC) as tunneling oxide is thinner than 8 nm, which would result in unacceptable data retention [31][32]. With these limits, it is generally believed that the floating-gate structure may fall out of use at 32 nm and beyond. Development of a feasible

technology to succeed the floating-gate flash memory becomes necessary and urgent.

Among miscellaneous techniques, silicon-oxide-nitride-oxide-silicon (SONOS) is widely viewed as the most potential one for next-generation flash memory [33]-[35]. Because the storage layer of SONOS is nitride, electrons are stored spatially isolated within insulator, ingeniously skipping the issues of coupling effect and SILC pertaining to the floating-gate flash memory. For an aggressively scaled structure, excellent data retention with high programming/erasing (P/E) speed is more possible in SONOS.



1-4 Motivation of this Study

As mentioned in previous sections, NWs, variation of devices characteristics, and SONOS-type flash memory are hot and important topics in nano-scale devices. Moreover, NW SONOS represents a potential device for future memory application. This motivates us to carry out the study on the fabrication, characterization, and investigation of parameter variations in such a device. Regarding the variation issue of device characteristics, there were already many research works conducted on the planar CMOS, although very few were done for the NWs-related devices. In this work we investigate the issue on our fabricated NW structures. It will be helpful to understand how it affects the operation of NW devices and circuits.

It had also been proved that NW devices may exhibit performance better than planar devices, such as lower subthreshold swing and leakage current. So we also apply MG NWs to fabricate SONOS flash memory. Because of good gate controllability of NWs, it is believed that performance improvements such as faster programming and erasing speed can be achieved.

1-5 Organization of the Thesis

We divide this thesis into five chapters. In Chapter 1, the related backgrounds and motivation of this study are described briefly. Detail process flows and structures for different kinds of MG NW devices as characterized in this thesis are depicted and described in Chapter 2. Basic theories on the variations of device characteristics are then discussed in Chapter 3. In Chapter 4, operation mechanisms about SONOS and comparisons in P/E characteristics between NWs and planar devices are presented. Finally, we summarize all findings and fruitful results in this study and suggest the schemes of future work in Chapter 5.

CHAPTER 2

Device Fabrication

Two structures, one with NW channels and the other with planar channel, were fabricated and studied in this thesis. For each structure, it was further divided into two types of devices, namely, conventional MOS type and SONOS type. In this chapter, process flows for fabricating these devices are described.

2-1 Fabrication and Structure of Nanowire Devices

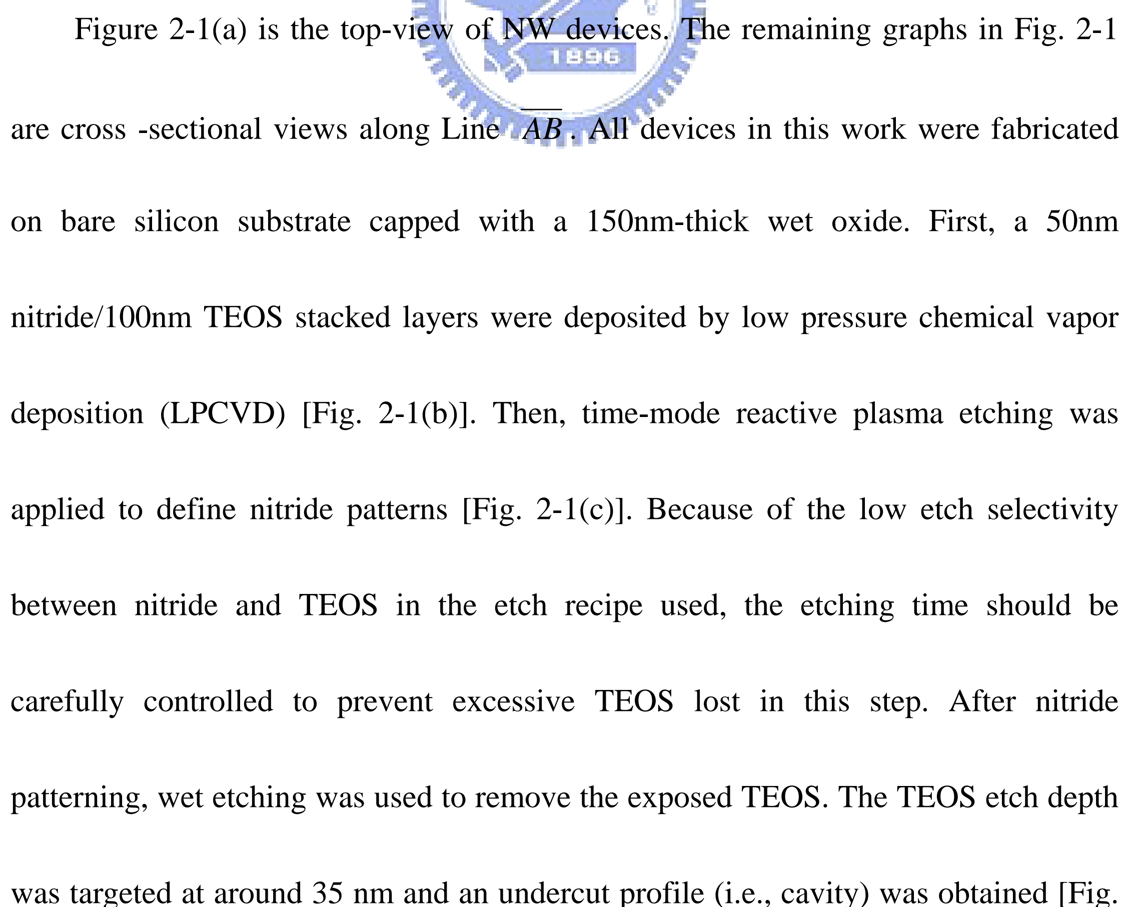
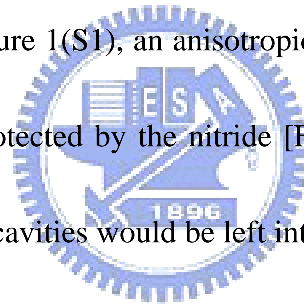


Figure 2-1(a) is the top-view of NW devices. The remaining graphs in Fig. 2-1 are cross -sectional views along Line $\overline{AB}$. All devices in this work were fabricated on bare silicon substrate capped with a 150nm-thick wet oxide. First, a 50nm nitride/100nm TEOS stacked layers were deposited by low pressure chemical vapor deposition (LPCVD) [Fig. 2-1(b)]. Then, time-mode reactive plasma etching was applied to define nitride patterns [Fig. 2-1(c)]. Because of the low etch selectivity between nitride and TEOS in the etch recipe used, the etching time should be carefully controlled to prevent excessive TEOS lost in this step. After nitride patterning, wet etching was used to remove the exposed TEOS. The TEOS etch depth was targeted at around 35 nm and an undercut profile (i.e., cavity) was obtained [Fig.

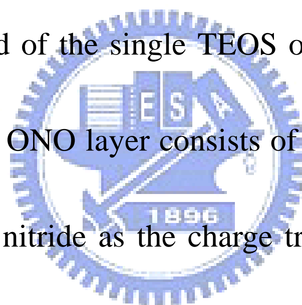
2-1(d)]. Next, a 100nm undoped amorphous silicon (a-Si) was deposited [Fig. 2-1(e)]. By taking advantage of the excellent filling capacity of LPCVD process, the cavities formed in last step could be refilled by the deposited a-Si. Afterwards, an annealing step was performed at $600^{o}C$ in N_2 ambient for 24 hours to transform the a-Si into polycrystalline phase. Subsequently, source/drain (S/D) implant was carried out by P^{+} implantation with an energy of 30 keV and a dose of $1x10^{15}$ cm^{-2}. Note that the S/D photoresist patterns were generated by a standard I-line lithography step. The main split conditions of this work were determined by the following steps. For the first type of structure, denoted as structure 1(S1), an anisotropic plasma etching was performed to remove the poly-Si not protected by the nitride [Fig. 2-1(f-1)]. Poly-Si films that filled the previously-existing cavities would be left intact since they were protected by the nitride in the dry etching step. Hence, nanowire channels were simultaneously formed at this step in a self-aligned manner. Note that for the S1 devices, the nitride layer was kept after the etching step, so that only one side of the NW channel is modulated by the gate, as shown in Fig.2-1(g-1). For the second type of structure, denoted as structure 2 (S2), the remaining nitride hard mask was subsequently removed by hot H_3PO_4 after the poly-Si etching [Fig. 2-1(f-2)]. By continuously etching TEOS by a diluted HF (DHF) solution with controlled etching time, the third type of structure denoted as structure 3 (S3) was formed [Fig. 2-1(f-3)]. Afterwards,



all structures were combined and capped with a 20nm TEOS gate oxide and a 100nm in-situ-doped poly-Si gate [Fig. 2-1(g-1) to (g-3)]. It is worth noting that the resultant S2 and S3 devices have two and three surfaces of the NW channel, respectively, modulated by the gate. Also note that no additional S/D dopant activation step was necessary. This is because the depositions of TEOS and poly-Si films were performed at temperatures higher than 700°C and the process time was sufficiently long to for dopant activation purpose. After the n^{+} poly-Si gate patterning, all devices were passivated with a 250nm-thick TEOS layer. Contact holes and test pads were formed by standard metallization steps. Finally, the fabrication was completed by a NH_3 plasma treatment for 2 hours.

Figures 2-2 and 2-3 show the cross-sectional-view TEM picture of an S2 and S3 device along Line $\overline{AB}$. It can be seen that the shape of NWs is nearly a quarter circle and the dimensions and shapes of S2 and S3 are similar to each other even though different etch steps were performed to them. The channel width of S1, or the gated vertical edge of the nanowire, is about 35nm for each nanowire channel. For S2 and S3 devices, the channel width is increased to 55 and 100nm, respectively, owing to the fact that additional nanowire edges are incorporated as the conductive channel. Since there are two NWs in one device, the effective channel width is doubled to 70, 110, 200nm for S1, S2, and S3, respectively.

In this study, we also modified the fabrication of S3 devices to fabricate SONOS-type devices, as shown in Fig. 2-4. First, a nitride(50nm)/TEOS(40nm) stacked layers were capped on the thermal oxide layer [Fig. 2-4(b)]. Then we defined dummy nitride/TEOS patterns by anisotropic plasma etching [Fig. 2-4(c)]. DHF etching was carried out in subsequent step to remove the TEOS layer with high selectivity to both nitride and thermal oxide, and rectangular recessed cavities were formed at sides of the dummy patterns [Fig. 2-4(d)]. Following steps were the same as that in the fabrication of S3 devices [Figs. 2-4(e) to (g)] except for the use of an ONO stacked gate dielectric, instead of the single TEOS oxide layer [Fig. 2-4(h)] and the skip of plasma treatment. The ONO layer consists of a 4nm-thick TEOS oxide as the tunneling oxide, a 7nm-thick nitride as the charge trapping layer, and a 13nm-thick TEOS oxide as the blocking oxide. Figure 2-5 shows the cross-sectional TEM picture of an NW SONOS device along Line $\overline{AB}$ of the top layout shown in the same figure. It can be seen that the shape of NWs is nearly rectangular with rounding curvature corner and the dimensions are around 25 and 40nm for the NW width and height, respectively.



2-2 Fabrication and Structure of Planar Devices

For comparison, planar devices were also fabricated and characterized in this

study. The fabrication process was similar to that of conventional TFTs, so the process would be described only briefly. Figure 2-6(a) is the top view of a planar device. Briefly, the fabrication began with the deposition of a 60nm-thick undoped a-Si film on the surface of a thermal oxide capping on a Si wafer. An anneal step was performed at 600°C in N_2 ambient for 24 hours to transform the a-Si into poly-Si [Fig. 2-6(b)]. After S/D and channel region were defined [Fig. 2-6 (c)], a 20nm-thick TEOS gate oxide and an in-situ-doped poly-gate were deposited [Fig. 2-6(d)]. Afterwards, gate electrode formation and self-aligned S/D implant were carried out [Fig. 2-6(e)]. Finally, the deposition of passivation layer [Fig. 2-6(f)], the formation of test pads, and NH_3 plasma treatment were performed, similar to the NW devices.

For SONOS-type planar devices, the gate dielectric consists of an ONO layer of 4/7/13 nm. Other steps were nominally identical to MOS-type devices except for the skipping of the plasma treatment.

CHAPTER 3

Characteristics of MOS-Type Devices

One the most important criteria to weigh the characteristic variation of MOSFETs is the threshold voltage (V_{TH}). So to begin with, we will present the fundamental notion about standard deviation of V_{TH} in this chapter. Then our observations on NWs fluctuation will be examined and compared with the developed models.

3-1 Theory about the Standard Deviation of Threshold Voltage

Just as specified in Section 1-2, dopant counts in channel region unceasingly decrease with device scaling, and may fall less than few hundreds in nano-scale CMOS devices. Discrete random dopant distribution in depletion region is regarded as the primary source to induce V_{TH} deviation especially in scaled MOSFETs [23]-[25]. To simplify the model, we assume that all parameters are kept constant in the deduction, other than the dopant distribution. As usual, V_{TH} can be expressed as

$$V_{TH} = V_{FB} + \phi_S - \frac{Q_{DEP}}{C_{OX}}, \qquad \text{(Eq. 3-1)}$$

where V_{FB} is the flat band voltage, ϕ_S is the surface potential between oxide and

channel, Q_{DEP} is the charge within the depletion region, and C_{OX} is the capacitance of gate oxide. The last term is directly related to dopant distribution in the depletion region, which causes the essential variation in V_{TH}. According to Takeuchi's model [36], V_{TH} shift (ΔV_{TH}) can be described as

$$\Delta V_{TH} = \frac{\Delta Q_{DEP}}{C_{OX}} \times (1 - \frac{x_0}{W_{DEP}}). \qquad \text{(Eq. 3-2)}$$

This model is based on Fig. 3-1(a), which assumes that additional charge sheet (ΔQ_{DEP}) at position "x_0" within maximum depletion width (W_{DEP}) would cause surface potential shift and hence V_{TH} change. In Fig. 3-1(b), solid line means original electrical field in the depletion region induced by substrate doping (N_{SUB}) without any extra charge and the original surface electrical field is E_0. When ΔQ_{DEP} is added, the electrical field is converted into dash line in order to balance the voltage drop at "x_0" and the surface electrical field has an increment of ΔE. The surface potential difference caused by electrical field variation is the cause of V_{TH} shift.

To calculate standard deviation of V_{TH} (σV_{TH}), we should consider ΔQ_{DEP} first. Here we suppose that ΔQ_{DEP} in the depletion region is binomial distribution, and appearance percentage and probability are comparatively less as compared with N_{SUB}. Thus the standard deviation of ΔQ_{DEP} ($\sigma \Delta Q_{DEP}$) at "x_0" can be approximated by Poisson's statistics [37], which is approximated by

$$\sigma \Delta Q_{DEP} = \frac{q\sqrt{N_{SUB}(x) LW (dx)}}{LW}, \qquad \text{(Eq. 3-3)}$$

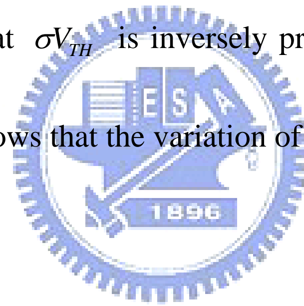
where W is the gate width and L is the gate length. σV_{TH} can be obtained by substituting Eq. 3-3 into Eq. 3-2 and integrating all the contribution of ΔQ_{DEP} in the depletion region from x=0 to x= W_{DEP}. The result is

$$\sigma V_{TH} = \frac{q}{C_{OX}} \times \sqrt{\frac{N_{EFF} W_{DEP}}{3LW}}\,, \qquad \text{(Eq. 3-4)}$$

where N_{EFF} is the average substrate doping concentration inside the depletion region, which is equal to

$$N_{EFF} = 3\int_{0}^{W_{DEP}} \frac{N_{SUB}(x)}{W_{DEP}}(1-\frac{x}{W_{DEP}})^{2}\,dx\,. \qquad \text{(Eq. 3-5)}$$

From Eq. 3-4, we can see that σV_{TH} is inversely proportional to the square root of the product *LW*. The result shows that the variation of V_{TH} is larger as device becomes smaller.



3-2 Comparisons of Basic Transfer Characteristics

Figure 3-2(a) shows the I_D-V_G curves of planar and the three kinds of NW devices. All measured devices have channel length of 2μm and gate oxide thickness of 20nm. It can be seen that all NW devices depict better subthreshold swing (SS) than planar devices. Among the three kinds of NW devices, the S3 split which has its NW channels surrounded by the gate exhibits the best SS and the highest on-current, while the S1 split which has only one of the NW surface under gate modulation has the

worst SS and the lowest on-current. The improvement of SS for the S3 device can be ascribed to the improved surface-to-volume ratio of its NW structures. S3 device also has the highest on-current because of its largest effective channel width. Furthermore, by normalizing the drain current to the channel width, we re-plot the I_D-V_G curves in Fig. 3-2(b). Clearly the NWs devices possess higher on-current and lower off-current than the planar one, hence the I_{on}/I_{off} ratio is higher for NW devices.

Figures 3-3 and 3-4 show the transfer characteristics of planar and S2 NW devices, respectively, with different channel length. The I_D-V_G curves of planar devices shift as channel length varies, indicating that V_{TH}, SS, and on/off currents are strongly related to the channel length. This condition is different for NWs as shown in Fig. 3-4, in which only on-current significantly increases with reduced channel length. The drain induced barrier lowing (DIBL) is obvious for planar device with channel length of 0.7μm. Figure 3-5 shows the transfer curves of S1 and S3 with channel length of 0.7μm. Unlike the planar counterpart, the DIBL phenomenon is negligible for the NW devices, which can be attributed to their ultra-thin channel body and much improved gate controllability.

3-3 Characteristic Variation of Nanowire Devices

3-3-1 Variation of Threshold Voltage

Before discussing the experimental results, several important parameters used in the coming content are revealed first. As shown in Figs. 2-2 and 2-3 and discussed in Section 2-1, the channel widths of measured devices are 70, 110, and 200nm for S1, S2, and S3, respectively. For every structure, the devices with three channel lengths of 0.7, 2, 5μm were characterized. In other words, we have investigated nine groups of devices with different channel width/length in this work. For the purpose of studying the fluctuation of device performance, we measured thirty devices for each split. Generally, we applied standard deviation (σ) to judge the variation of samples with the formula $\sigma = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(x_i - \bar{x})^2}$, where N is the total numbers of samples, x_i is the value of individual sample, and $\bar{x}$ is the mean value of all samples. Next, we have to settle on how to define V_{TH}. For MOSFETs, the V_{TH} is defined by $V_{TH} = V_A - \frac{V_D}{2}$, where V_A is the gate voltage coinciding with the maximum value of transconductance (g_m). Since the max g_m of poly-Si TFTs is sometimes not so easy to decide due to the low carrier mobility, here we instead determine V_{TH} by the constant drain current method with the following expression: $V_{TH} = V_G \Big|_{I_D = 10nA \times \frac{W}{L},\ V_D = 0.5V}$.

First, we select two series devices to show the I_D-V_G characteristics. Figures 3-6(a) and (b) are the I_D-V_G curves of thirty devices from S1 split with channel length of 0.7μm and S3 split with channel length of 5μm, respectively. Obviously, the

devices with the smallest width and length within our samples in Fig. 3-6(a) have more apparent fluctuations than the ones with the largest width and length in Fig. 3-6(b). Figure 3-7(a) shows the V_{TH} distribution of different NW structures with channel length of 2μm. It can be seen that S3 split depicts the narrowest V_{TH} distribution, while S1 has the widest distribution. Figure 3-7(b) shows V_{TH} distribution for S2 split with different channel length. We can see that the device with channel length of 0.7μm depicts wider distribution than devices with longer channel length (i.e., 2 and 5μm).

Next, we show all measured results of nine groups of devices by transparent graphic method with V_{TH} mean value and the standard deviation of V_{TH} (σV_{TH}). In Figures 3-8(a), (b), and (c), the mean value of V_{TH} of different structures are plotted for channel length of 0.7, 2, and 5μm, respectively. Note that the error bar represents σV_{TH}. While in Figures 3-9(a), (b), and (c), the mean value of V_{TH} versus channel length is plotted for S1, S2, and S3, respectively. All of the splits in Figs. 3-8 and 3-9 show the identical trend in σV_{TH}, i.e., when the channel width and/or length increases, σV_{TH} decreases. As described in Section 3-1, the discrete random dopant in depletion region is regarded as the main source to induce the V_{TH} fluctuation. In our study, no intentional channel doping was performed to the poly-Si. Nevertheless, the trapping sites located in the grain boundaries may play a similar role to that of random dopants

in the bulk CMOS devices [38] since their charge state is affected by the gate bias and may affect V_{TH}. To verify this assumption, we plot σV_{TH} versus $1/\sqrt{LW}$ in Fig. 3-10, in which the experimental data of nine groups of NW devices are fitted with one solid line, while the data of each NW structure (i.e., S1, S2, and S3) are fitted with the dashed lines. Note that full depletion of the channel is expected because of the sufficiently small dimension of our NWs. Figures 2-2 and 2-3 show that the three NW structures almost possess the same cross-sectional dimensions in the channel region, hence S1 with only one side of its NW channels gated has the thickest effective depletion width. On the other hand, the S3 device has a gate-all-around (GAA) configuration, thus has the thinnest effective depletion width. Therefore, the slope of the fitting lines for S1 is the highest, S2 falls in the middle, and S3 is the lowest. Such trend is consistent with the theory depicted by Eq. 3-4.

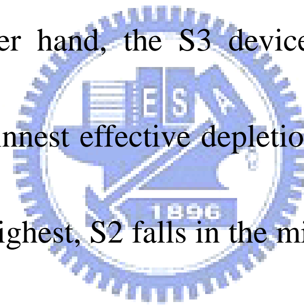


Figure 3-10 also shows the σV_{TH} of planar devices. The channel width/length of the measured planar devices is 5/0.7, 10/2, and 20/5μm. The σV_{TH} of planar devices is higher than that of NWs evidently, which may be ascribed to the much thicker depletion region of the planar device. The dashed line next to the fitting line for planar devices is constructed based on the assumption that the planar devices have channel thickness of 20 nm, similar to that for S1 according to TEM pictures [Figs. 2-2 and 2-3]. Note that the depletion width is 60nm for our planar devices [39]. The

result shows that the σV_{TH} of S1 split is still much smaller than that of planar devices with similar channel thickness. This might be caused by the insufficient plasma treatment for planar devices. Most defects in NW channel region can be passivated and become inactive during the two-hour NH_3 plasma treatment due to high surface-to-volume ratio of NWs. For planar devices, however, the two-hour duration is not sufficient for plasma to penetrate into entire channel region to repair the defects because the channel volume is relatively large. Hence the deviation of planar devices is higher than that of NWs.

3-3-2 Variation of Subthreshold Swing

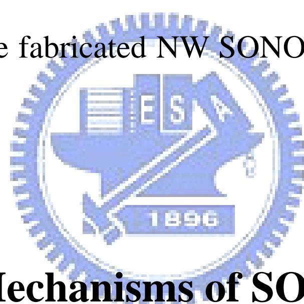
In addition to V_{TH}, we also plot the standard deviation of SS (σSS) for devices of different channel length and width. Figures 3-11(a), (b), and (c) show the mean value of SS and σSS of the three NW structures for channel length of 0.7, 2, and 5μm, respectively. It can be seen that SS and σSS decrease when effective channel width increases from S1 to S3 for a fixed channel length. However, as we plot SS and σSS versus channel length, as shown in Figs. 3-12(a), (b), (c), it can be seen that the mean values of SS and σSS seem not to strongly depend on the channel length. But we can see that the discrepancy of mean value of SS and σSS between different channel lengths is largest for S1 [Figs. 3-12(a)] and smallest for S3 [Figs. 3-12(c)]. This phenomenon can be attributed to the increasing gate coverage within finite

channel region, which promotes the control ability of gate and then reduces the deviations of SS mean value and σSS among different channel lengths. Hence the trend shown in Fig. 3-11 is also reasonable.

CHAPTER 4

Characteristics of SONOS-Type Devices

For non-volatile semiconductor devices such as electrically erasable programmable read only memories (EEPROMs), several important parameters including P/E speed, data retention, and endurance need to be carefully considered. In this chapter, we will first review the basic P/E mechanisms and reliability issues. Then the experimental results on the fabricated NW SONOS devices will be presented and discussed.



4-1 Program/Erase Mechanisms of SONOS Flash Memory

4-1-1 Channel Hot Electrons Injection

Several hot-carrier injection (HCI) mechanisms such as channel hot electrons injection (CHEI) [40], drain avalanche hot carrier (DAHC) [41] and substrate hot electrons injection (SHEI) [42] have been widely investigated for non-volatile memory applications. Among these mechanisms, CHEI is often applied to flash memory. Hence the fundamental theory of CHEI will be reviewed below.

As the device channel length is scaled down, the hot-carrier effects (HCE) [43] could become a serious reliability issue if the supply voltage is not proportionally

scaled down. It was considered that HCE would be disastrous for submicron MOSFETs when the hot-carrier effects were first discovered in the seventies. However, it was serendipitous that, if properly utilized, HCE could turn from disaster to asset. A case in point is that many flash memory were programmed by hot electrons from HCE.

As illustrated in Fig. 4-1(a), HCE occurs because of high lateral electrical field (E_L) in channel. While high gate voltage (V_G) and drain voltage (V_D) are applied, in general $V_D \geq V_{DSAT} = V_G - V_{TH}$, pinch-off occurs close to drain region. When gate length (L) shrinks into submicometer while maintaining the same V_{CC}, lateral electrical field in the pinch-off region increases dramatically for $E_L = \frac{V_D - V_{DSAT}}{L}$. High E_L will accelerate transport electrons in the pinch-off region. Electrons can obtain sufficient energy and become "hot carriers", known as channel hot electrons (CHE).

The CHEs with sufficient energy may cause impact ionization, and create extra electrons named secondary electrons (2nd e^-). The CHEs or 2nd e^- drift into drain will contribute to drain current. If these hot electrons overcome energy barrier and be injected into gate dielectric [Fig. 4-1(b)], they contribute to the gate current, which is well understood by "lucky electron model" [44]. On the other hand, holes injection is much more difficult due to heavier mass and higher valence barrier height. Therefore

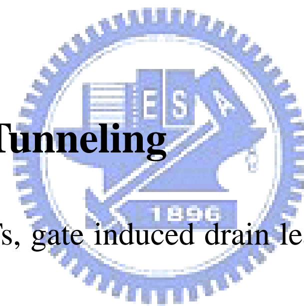
we can cleverly employ CHEI to achieve programming purpose for non-volatile memories.

4-1-2 Fowler-Nordheim Tunneling

In the classical theory, electrons in the channel region are forbidden to tunnel through gate dielectrics into gate electrodes or other states such as n-region of SONOS structures when carrier energy is lower than the barrier height [Fig. 4-2(a)]. However, as gate oxide thickness is sufficiently thin, the quantum tunneling phenomenon will occur easily, and can be categorized into the direct tunneling mode [45] and the Fowler-Nordheim tunneling (F-N tunneling) mode [46].

Electrical field built up across gate oxide (E_{OX}) can be represented by $E_{OX} = \frac{V_{OX}}{t_{OX}}$ where V_{OX} and t_{OX} represent voltage drop in oxide region and oxide thickness, respectively. If V_{OX} is higher than the band-offset ($q\phi$) of Si substrate and oxide, electrons in Si channel may tunnel into the conduction band of oxide through triangular barrier as illustrated in Fig. 4-2(b). Electrons in the conduction band of oxide will be accelerated by high field and injected into gate. This mechanism is called F-N tunneling, which was named after Fowler and Nordheim who first reported the phenomenon in 1928. The difference between direct tunneling and F-N tunneling is that in direct tunneling electrons pass through oxide and are injected into gate

"directly" when V_{OX} is lower than band-offset as show in Fig. 4-2(c). The damage on dielectric caused by direct tunneling is less sever than F-N tunneling due to the fact that the injecting electrons do not present in the conduction band of the gate dielectric. But in general, this mechanism leads to a leakage much higher than the F-N process at a fixed field strength and is therefore not preferred. Because direct tunneling dominates when oxide thickness is less than 3nm, such a thin oxide is not suitable for flash memory applications due to retention and reliability issues which will be discussed in the following section.



4-1-3 Band-to-Band Tunneling

For nano-scale MOSFETs, gate induced drain leakage (GIDL) is a major part of off-state leakage current. Similar to CHEI, we may take advantage of such phenomenon and turn it into a useful technique in the operation of flash memory.

As illustrated in Fig. 4-3(a), GIDL is attributed to band-to-band tunneling (BTBT) in n^+ drain region overlapped by the gate region [47]. When a highly negative voltage relative to n^+ region is applied to the gate, deep depletion will occur within n^+ area next to the interface of oxide and silicon substrate. Deep depletion with serious band bending will promote electron BTBT from valence band to the conduction band in the n^+ region. Other mechanisms like traps-assisted-tunneling and thermal emission also

promote BTBT. At the same time, holes will be left in the valence band and accelerated by the strong electrical field. Portion of these accelerated holes may be attracted by the negative gate voltage and injected into gate oxide contributing to the gate leakage current [Fig. 4-3(b)].

4-1-4 Program/Erase Principle of the NW Devices

Just as mentioned in previous sections, there are several approaches for P/E operation in flash memory based on the device configuration. For our devices, channel is formed with poly-Si and electrons transporting in channel may be scattered by grain boundaries of poly-Si. Hence it is difficult for electrons to obtain high energy during transportation and become "hot" enough. So CHEI is not appropriate for programming operation in the poly-Si NW devices. Hence we decide to employ the F-N tunneling for programming in this work. For erasing, both F-N and BTBT are employed and studied.

4-2 Reliability of SONOS Flash Memory

4-2-1 Retention

Retention is a measure of the sustained time for storage of charges in the trapping layer that different logic levels can be distinguished without blur due to any

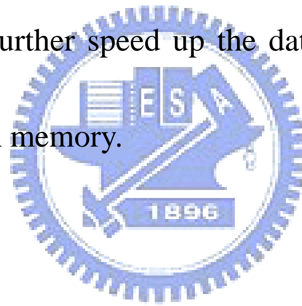
charge lost events. For commercial products, the standard retention time is 10 years with window larger than 0.5 V.

All possible data loss paths mentioned in this section are shown in Fig. 4-4. In general, two kinds of data loss mechanisms in SONOS flash memory can be categorized. The first one is Frenkel-Poole mechanism [48]. Frenkel-Poole emission can be explained by the movement of trapped charges from site to site with level inside the bandgap (symbol 1 in Fig. 4-4), especially when an electric field is applied. The injected electrons due to programming are trapped in the nitride, and will raise the potential of the trapping site. The build-up of local field may boost the movement of carriers toward the sites located at lower energy levels. As electrons are pushed to the edge of the nitride layer and near the nitride/oxide interface, the barrier width relative to the channel narrows as compared with the original position, and tunneling process may occur (see discussion in the next paragraph). This phenomenon frequently takes place when a material contains many defects acting as trapping and de-trapping centers.

The other data loss mechanism is tunneling effect. Electrons in nitride trapping states can tunnel into the conduction band of Si-substrate (trap-to-band, symbol 2 in Fig. 4-4) or inject into the interface traps between Si-substrate and tunneling oxide (trap-to-trap, symbol 3 in Fig. 4-4). As mentioned above, Frenkel-Poole mechanism

may push electrons to the edge of the nitride layer, which promotes the tunneling probability. Not only electrons lost blur data, but also holes in the valence band of Si-sub tunnel into trapping centers of nitride (band-to-trap, (symbol 4 in Fig. 4-4)) does. [49]

In general, the thickness and quality of tunneling oxide in SONOS devices has evident influence on data retention. Thin tunneling oxide will lead to a fast P/E rate, but data storage capacity will decrease due to the shorter tunneling length. With respect of oxide quality, if there are defects contained in the tunnel oxide, traps-assisted-tunneling will further speed up the data lost rate. These all challenge data retention of SONOS flash memory.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4-2-2 Endurance

Another reliability topic is endurance, which is a measure of cycle times that devices can endure will still retain acceptable P/E window to make devices work normally. In general, the basic requirement for endurance of flash memory is 10^6 P/E cycling times. Fortunately, the endurance requirement will be relaxed when devices are scaled along with the increase in memory density [50]. For high-density memory, every cell has less probability to receive P/E cycles because the cell in a memory array will be subjected to P/E stressing only if the particular memory block is

accessed. Hence, endurance standard can be lessened from 10^6 for 16MB to 10^4 for 4GB.

Programming and erasing operations of flash memory are performed with a very high electric field. Hence tunneling oxide and trapping layers must be durable to the operations. As described in Chapter 1 and last section [31][32], the SILC is a main issue associated with floating-gate flash memory. There are many defects generated in tunneling oxide region during P/E cycles. These defects act as the sites for traps-assisted-tunneling and data lost path. So all electrons stored in a "conductive" floating-gate will leak out through these defects. On the other hand, electrons are stored in discrete traps in the nitride layer of SONOS, so these electrons will not lose entirely due to the "insulating" storage layer. This is one important reason for the SONOS to be regarded as a promising candidate for next-generation flash memory.

In order to reduce stress-induced damage in the tunneling oxide, operation voltage must be reduced. However, there is a trade-off between P/E speed and applied voltage, so we have to optimize all related parameters such as the thickness of each composed layer in the ONO stack, P/E modes, tolerable operation time, etc.

4-3 Program/Erase Characteristics

4-3-1 Program/Erase Characteristics of Nanowire Devices

As mentioned in previous section, the SONOS devices in this work are programmed and erased by F-N tunneling. For programming, both source and drain of the fresh device are grounded, and the gate is applied a positive voltage to induced voltage dropped in ONO region to achieve F-N tunneling. For erasing, the device is programmed beforehand with 3V shift of V_{TH} relative to the fresh state [Fig. 4-5]. Then the gate of the programmed device is biased with a negative voltage, while source and drain are both grounded. As shown in Fig. 4-5, the I_D-V_G curve of a programmed NW SONOS device is nearly parallel to that of fresh state.

Figure 4-6 shows the V_{TH} shift versus programming time of NW SONOS with gate bias of 11V, 12V, 13V, and 14V, respectively. For simplicity, the V_{TH} is defined as the gate voltage at drain current of 1 nA. For a fixed period, the V_{TH} shift increases with increasing gate bias. It can be seen that memory window of 3V can be achieved within 1 millisecond (ms) with applied voltage of 14V. We utilize this operation condition to program fresh devices for investigation of erasing characteristics. Figure 4-7 is the result of V_{TH} shift as a function of erasing time with gate bias of -9V, -10V, -11V, respectively. The V_{TH} shift increases with increasing gate voltage and/or operation time. It can be seen that the rate of V_{TH} shift slows down when erasing time is longer than 100ms with gate bias of -11V. During the erasing process, the amount of trapping electrons in the nitride reduces. The electrical field across the tunneling

oxide also reduces. Therefore the erasing capability weakens and erasing speed is retarded accordingly.

4-3-2 Program/Erase Characteristics of Planar Devices

In Chapter 3, we have shown transfer characteristics of planar device and NWs. It is obvious that NW devices possess better gate control ability and stable reliability. Hence it is predictable that NWs will have better characteristics than planar SONOS. Figure 4-8 shows the programmed and erased states of both NWs and planar SONOS, which verifies our predictions. Here we define erased state as "on" state, programmed state as "off" state, and the reading voltage is set at 2.5V. With the same memory window of 2.5V, the I_{on}/I_{off} ratio of NW devices is higher than that of planar SONOS. This diversity can be attributed to better SS and less leakage current of NW devices.

Figure 4-9 compares the programming characteristics of planar and NW SONOS devices with identical ONO thickness. To compare the programming capability, we apply the same gate bias of 14V to both planar and NW devices. For NWs, V_{TH} shift is over 1V when the programming time is merely 1 microsecond (μs). On the contrary, V_{TH} shift of planar devices is less than 0.1V even when the programming time increases to 10ms. In order to have the same V_{TH} shift as the NW device at 10ms, a gate bias of 20V needs to be applied to the planar device. Similar situations also occur

in erasing characteristics, as shown in Fig. 4-10. If we apply gate voltage of -11V to the planar device for 1s, the programmed device only exhibits negligible shift. To attain comparable erasing speed to that of the NW device biased with gate voltage of -11V, the gate bias of planar devices must be raised to -20V.

Irrespective of programming or erasing operation, the above results show that the NWs devices exhibit better efficiency than planar counterparts. As shown in Fig. 2-5, the cross-sectional shape of the tri-gated NW channel is nearly rectangular configuration with rounding curvature corners. Here we consider the results of NW SONOS devices with round NW channel and GAA configuration reported in a recent publication [51]. The superiority of NW devices in P/E speed over the planar structure is also observed in that previous work, so we refer to their deduction based on the band diagrams shown in Fig. 4-11 to explain our experimental findings. Figure 4-11(a) shows the band diagrams of planar and NW SONOS devices with identical ONO thickness and gate bias under programming operation. The solid line and dash line represent the potential profile of NW and planar devices, respectively. It can be seen that the voltage dropped across tunneling oxide in GAA NWs is higher than planar devices due to its high curvature, hence the barrier width in tunneling oxide is thinner with respect to planar devices. Because the tunneling probability increases as tunneling length is reduced, the carrier injection speed of NW device is apparently

higher than that of the planar one when the applied gate bias is the same. Similar situation occurs for erasing operation, as shown in Fig. 4-11(b). Therefore, GAA NW devices exhibit much better P/E efficiency than planar devices. Although the shape of the NW cross-section characterized in this study is different from the round shape in the previous work, we believe the rounded corner region should behave similarly as that described in Fig. 4-11, and thus dramatically promote the P/E efficiency.

4-4 Reliability Characteristics of Nanowire Devices

4-4-1 Retention Characteristics

Before discussing the reliability topic of NW SONOS devices, we briefly explain the procedural rules used for retention and endurance measurements in this work. Figure 4-12 shows I_D-V_G curves of SONOS devices before and after a few cycles of P/E operation. The solid line in the left is the fresh-state characteristics. We apply gate voltage of 14 V for 1ms to perform the first-time programming to attain V_{TH} shift of 3V. Then in the second operation, the gate is biased at -11V for 50ms to erase the programmed device and cause the V_{TH} shift of -2.3V. In order to reach the same programmed state as the first operation, we apply gate bias of 13V instead of 14V for 1ms to program the device again. For the fourth and fifth operations and beyond, the P/E voltage and time are identical to the second and third operations, respectively.

Except for the first programming, the P/E specifications of other cycles make the SONOS in stable programmed and erased states, which are "real-life situations" in practical products. Hence the parameters employed in this section are according to the P/E specifications of "real-life situations."

The data retention characteristics of fresh devices are shown in Fig. 4-13. If we program the devices by gate bias of 13V for 1ms, and -11V with 50ms for erasing, the memory window can be larger than 0.5V after 10 years at room temperature. Figure 4-14 is the data retention measured at 25°C, 55°C, and 85°C, respectively. No matter in programmed or erased state, the data storage ability is stable and the temperature dependence of memory window at 10 years is weak. This phenomenon is reasonable. The data lost path of SONOS discussed in previous section is mainly through Frenkel-Poole emission and tunneling effect. Hence the temperature dependence is not evident.

4-4-2 Endurance Characteristics

There are two P/E specifications applied to endurance tests, as indicated in Fig. 4-15. The results show that the stressing cycles can be more than 10^4 with acceptable memory window. Nevertheless, window opening is observed in our measurement. The memory windows in the beginning are about 1.39V and 2.29V for individual P/E

specifications. As stressing cycles increasing, the windows extend from 1.39 and 2.29V to 1.98 and 2.96V respectively.

During the stressing process, electrons tunnel through bottom oxide between channel and nitride backwards and forwards. Hence tunneling oxide will directly affect the P/E efficiency, if there are any changes in its properties during stressing. Since the thickness of blocking oxide in this work is quite thick (13nm), electrons barely tunnel into the gate and thus we ignore the influence of this particular charge loss path.

First, we measured and inspected the evolution of subthreshold characteristics during P/E operations. If there are interface states created during the operation, V_{TH} shift may mainly come from the increase in subthreshold swing (SS). Figure 4-16 show I_D-V_G characteristics of the device coinciding with the measured points shown in Fig. 4-15 with P/E specification of 13V1ms/-11V50ms. It can be seen that in the programmed state, the SS other than the first time programming becomes worse. Because we define V_{TH} at I_D=1nA, the V_{TH} shift in programmed state comes from SS degradation. On the other hand, the change of SS in erased state is not significant, and thus the SS variation has a small effect on the V_{TH} shift in the erased state.

Next, we measured the retention characteristics again to examine the quality of tunneling oxide. Figures 4-17 show the data retention characteristics of a device after

subjecting to one (fresh) and 10^4 P/E cycles with P/E specification of 13V1ms/-11V50ms. Here we discuss the programmed and erased state separately. For programmed state, if the window opening is caused by additional electrons trapped in the tunneling oxide during P/E cycles, data loss will be more severe. Because the tunneling length of electrons trapped in tunneling oxide is shorter than that in nitride, electrons will escape more easily. Compared with fresh devices, the V_{TH} of stressed devices does not show apparent change in the rate of V_{TH} lowering in programmed state in Fig. 4-17. Therefore, we can confirm our contention in last paragraph that V_{TH} shift in programming retention characteristics come from SS degradation.

For erased state, Figure 4-17 shows that the erased device after stressing has evident positive shift in V_{TH} in seconds and then reaches a steady state. During stressing cycles, holes would inject into nitride to accomplish erasing operation and some holes may stay in tunneling oxide. These holes would result in V_{TH} decrease as with a fresh device without holes injection. This is the origin of window opening in erased state after stressing. When we stop applying negative bias for erasing operation, these holes stored in the tunneling oxide may escape easily and lead to recovery of V_{TH} as shown in Fig. 4-17.

CHAPTER 5

Conclusion and Future Work

5-1 Conclusion

In this thesis, without resorting to advanced lithographical tools like e-beam direct writers, we propose a simple and flexible way to successfully fabricate NW devices with three different types of MG configurations. Furthermore, we also modified the fabrication to fabricate tri-gated SONOS devices with nearly rectangular configuration.

Compared with planar devices, the improvements in SS, leakage, DIBL, and on/off ratio for NWs are verified in our experimental results. These excellent NW characteristics can retain even with shrunk channel length. Among our three NW structures, the S3 split which has a gate-all-around configuration exhibits the best gate controllability, hence it possesses the most prominent performance in nearly all aspects of device characteristics. For device variation issue, the standard deviation of V_{TH} is shown to be inversely proportioned to $\sqrt{WL}$, which is consistent with the planar CMOS theory. Moreover, the fluctuation of planar devices is higher than that of NW ones, which may be caused by the insufficient plasma treatment duo to the

relatively wider channel and thus larger channel volume that needs a longer time to effectively passivate the defects.

Regarding the SONOS devices, NW structures have apparent improvement on P/E efficiency as compared with planar devices, which can be attributed to the increase of curvature of the NWs. Though the P/E speed of NWs is better than that of planar devices, the erasing speed is somewhat slower owing to the rather thick blocking oxide. The retention measurements show that the memory window can be larger than 0.5V after 10 years at 85°C. For endurance test, the devices can sustain P/E cycles for more than 10^4 times and maintain acceptable memory window in retention test.

5-2 Future Work

When the channel length reduces, our NWs still possess good gate control abilities. Therefore, if we can design a layout with increased NW count in a unit area to provide sufficient current drive, it is believed that NW-TFTs will become a promising candidate for future applications.

The fabricated S3 device is a GAA NW, but its shape is not preferred for electrical characteristics because of the sharp corners. Hence we have to improve the NW structure and make it close to a circle, which is suitable for the applications of both MOS-type and SONOS-type devices. Besides, we should deposit thinner

blocking oxide for our SONOS devices to reduce the operation voltage and/or to increase the P/E speed.

. In this study, we have demonstrated many important and interesting results about NW characteristics. Nevertheless, it is a pity that we don't have a complete model to explain the characteristics of the NW devices. Therefore, performing more simulation work to justify our findings is another urgent work in the future.

REFERENCES

[1] Ran-Hong Yan, Abbas Ourmazd, and Kwing F. Lee. **"Scaling the Si MOSFET: From Bulk to SOI to Bulk,"** *IEEE Transactionss on Electron Devices,* vol. 39, no. 7, pp. 1704-1710, 1992.

[2] Tetsu Tanaka, Hirishi Horie, Satoshi Ando, and Shinpei Hijiya. "**Analysis of p^+ Poly Si Double-Gate Thin-Film SOI MOSFETs**," *IEDM*, pp.683-686, 1991.

[3] Digh Hisamoto, Wen-Chin Lee, Jakub Kedzierski, Erik Anderson, Hideki Takeuchi, Kazuya Asano, Tsu-Jae King, Jeffrey Bokor, and Chenming Hu. "**A Folded-Channel MOSFET for Deep-Sub-Tenth Micron Era**," *IEDM,* pp. 1032-1034, 1998.

[4] B.S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios, and R. Chau. **"High Performance Fully-Depleted Tri-Gate CMOS Transistors,"** *IEEE Electron Device Letters,* vol. 24, no. 4, pp. 263–265, 2003.

[5] Fu-Lian Yang, Hau-Yu Chen, Fang-Cneng Chen, Cheng-Chuan Huang, Chang-Yun Chang, Hsien-Kuang Chiu, Chi-Chung Li, Chi-Chun Chen, Huan-Tsung Huang, Chih-Jian Chen, Hun-Jan Tao, Yee-Chia Yeo, Mong-Song Lian, and Chenming Hu. **"25 nm CMOS Omega FETs,"** *IEDM,* pp. 255–258, 2002.

[6] J.P. Colinge, M.H.Gao, A. Romano-Rodrigeuz, H. Maes, and C. Claeys. "**Silicon-On-Insulator Gate-All-Around Device,"** *IEDM,* pp. 595-598, 1990.

[7] T. Poiroux, M. Vinet, O. Faynot, J. Widiez, J. Lolivier, T. Ernst, B. Previtali and

S. Deleonibus. "**Multiple Gate Devices: Advantages and Challenges,**" *Microelectronic Engineering*, vol. 80, pp. 378-385, 2005.

[8] Jean-Pierre Raskin, Tsung Ming Chung, Valeria Kilchytska, Dimitri Ledere, and Denis Flandre. "**Analog/RF Performance of Multiple Gate SOI Devices: Wideband Simulations and Characterization,**" *IEEE Transactionss on Electron Devices,* vol. 53, no. 5, pp. 1088-1095, 2006.

[9] J. Saint-Martin, A. Bournel, and P. Dollfus. **"Comparison of Multiple-Gate MOSFET Architectures Using Monte Carlo Simulation,"** *Solid-State Electronics,* vol. 50, no. 1, pp. 94-101, 2006.

[10] Xiangfeng Duan, Yu Huang, and Charles M. Lieber. **"Nonvolatile Memory and Programmable Logic from Molecule-Gated Nanowires,"** *Nano letters*, vol. 2, no. 5, pp. 487-490, 2002.

[11] Xiangfeng Duan, Chunming Niu, Vijendra Sahi, Jian Chen, J. Wallace Parce, Stephen Empedocles and Jay L. Goldman. "**High-Performance Thin-Film Transistors Using Semiconductor Nanowires and Nanoribbons,**" *Nature*, vol. 425, pp. 274-278, 2003.

[12] Xiandfeng Duan, Yu Huang, Yi Cui, Jianfang Wang, and Charles M. Lieber. **"Indium Phosphide Nanowires as Building Blocks for Nanoscale Electronic and Optoelectronic Devices,"** *Nature*, vol. 409, pp. 66-69, 2001.

[13] Fernando Patolsky and Charles M. Lieber. **"Nanowire Nanosensors."** *Materials today*, vol. 8, pp. 20-28, 2005.

[14] Jong-in Hahm and Charles M. Lieber. **"Direct Ultrasensitive Electrical Detection of DNA and DNA Sequence Variations Using Nanowire**

Nanosensors," *Nano Letters,* vol. 4, no. 1, pp. 51-54, 2004.

[15] D. Mijatovic, J. C. T. Eijkel and A. van den Berg. **"Technologies for Nanofluidic Systems: Top-Down vs. Bottom-Up — a review,"** *Lab Chip*, vol. 5, pp. 492-500, 2005.

[16] O. H. Elibol, D. Morisette, D. Akin, J. P. Denton, and R. Bashir. **"Integrated Nanoscale Silicon Sensors Using Top-Down Fabrication,"** *Applied Physics Letters,* vol. 83, no. 22, pp.4613-4615, 2003.

[17] Mingwei Li, Rustom B. Bhiladvala, Thomas J. Morrow, James A. Sioss, Kok-Keong Lew, Joan M. Redwing, Christine D. Keating and Theresa S. Mayer. **"Bottom-Up Assembly of Large-Area Nanowire Resonator Arrays,"** *Nature Nanotechnology,* vol. 3, pp. 88-92, 2008.

[18] W. Haensch, E. J. Nowak, R. H. Dennard, P. M. Solomon, A. Bryant, O. H. Dokumaci, A. Kumar, X. Wang, J. B. Johnson, and M. V. Fischetti. **"Silicon CMOS Devices Beyond Scaling,"** *IBM Journal of Research and Development,* vol. 50, no. 4/5, pp.339-361, 2006.

[19] Siva G. Narendra. **"Effect of MOSFET Threshold Voltage Variation on High-Performance Circuit,"** *PH. D. Dissertation, Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology,* 2002.

[20] Asen Asenov, and Subhash Saini. "**Polysilicon Gate Enhancement of the Random Dopant Induced Threshold Voltage Fluctuations in Sub-100 nm MOSFETs with Ultrathin Gate Oxide**," *IEEE Transactionss on Electron Devices,* vol. 47, no. 4, pp. 805-812, 2000.

[21] Asen Asenov, Savas Kaya, and John H. Davies. "**Intrinsic Threshold Voltage Fluctuations in Decanano MOSFETs Due to Local Oxide Thickness Variations,**" *IEEE Transactionss on Electron Devices,* vol. 49, no. 1, pp. 112-119, 2002.

[22] Asen Asenov, Savas Kaya, and Andrew R. Brown. "**Intrinsic Parameter Fluctuations in Decananometer MOSFETs Introduced by Gate Line Edge Roughness,"** *IEEE Transactionss on Electron Devices,* vol. 50, no. 5, pp. 1254-1260, 2003.

[23] P.A Stolk, and D.B.M. Klaassen. "**The effect of Statistical Dopant Fluctuations on MOS Device Performance,"** *IEDM,* pp. 627-630, 1996.

[24] Robert W. Keyes. **"Effect of Randomness in the Distribution of Impurity Ions on FET Thresholds in Integrated Electronics,"** *IEEE Journal of Solid-State Circuits,* vol. 10, no. 4, pp. 245-247, 1975.

[25] Kazumi Nishinohara, Naoyuki Shigyo, and Tetsunori Wada. "**Effects of Microscopic Fluctuations in Dopant Distributions on MOSFET Threshold Voltage,"** *IEEE Transactionss on Electron Devices,* vol. 39, no. 3, pp. 634-369, 1992.

[26] Yun Heub Song, Jeong Ho Park, Sang Eun Lee, Jun Young Lee, and Joong Shik Shin. **"Highly Manufacturable 90 nm NOR Flash Multi-Level Cell Technology with WSi_x Gate,"** *Japanese Journal of Applied Physics,* vol. 46, no. 6, pp. L120-L122, 2007.

[27] Xinghai Tang, Vivek K De, Lihui Wang, and James D. Meindl. "**SOI MOSFET Fluctuation Limits on Gigascale Integration (GSI),"** *IEEE International SOI Conference,* pp.42-43, 1999.

[28] Toshinori Numata, Mitsuhiro Noguchi, and Shin-ichi Takagi. **"Reduction in Threshold Voltage Fluctuation in Fully-Depleted SOI MOSFETs with Back Gate Control,"** *Solid-State Electronics,* vol. 48, no.6, pp979-984, 2004.

[29] http://www.itrs.net/home.html

[30] Masashi Wada, Shouichi Mimura, Hiroyuki Nihira, and Hisakazu Iizuka. "**Limiting Factors for Programming EPROM of Reduced Dimensions**," *IEDM,* pp. 38-41, 1980.

[31] R.S. Scott and David J. Dumin. "**The Charging and Discharging of High-Voltage Stress-Generated Traps in Thin Silicon Oxide**," *IEEE Transactionss on Electron Devices,* vol. 43, no. 1, pp. 130-136, 1996.

[32] R.S. Scott, N.A. Dumin, T.W. Hughes, D.J. Dumin and B.T. Moore. **"Properties of High-Voltage Stress Generated Traps in Thin Silicon Oxide,"** *IEEE Transactionss on Electron Devices,* vol. 43, no. 7, pp. 1133-1143, 1996.

[33] Eiichi Suzuki, Hisato Hiraishi, Kenichi Ishii, and Yutaka Hayashi."**A Low Voltage Alterable EEPROM with Metal Oxide Nitride Oxide Semiconductor (MONOS) Structures,"** *IEEE Transactionss on Electron Devices,* vol. 30, no. 2, pp. 122-128, 1983.

[34] Marvin H. White, Dannis A. Adams, and Jiankang Bu. **"On the go with SONOS,"** *IEEE Circuits and Devices Magazine,* vol. 16, pp. 22-31, 2000.

[35] Jiankang Bu and Marvin H. White. **"Design Considerations in Scaled SONOS Nonvolatile Memory Devices,"** *Solid-State Electronics*, vol. 45, no. 1, pp. 113-120, 2001.

[36] Kiyoshi Takeuchi, Toru Tatsumi, and Akio Furukawa. **"Channel Engineering**

for the Reduction of Random-Dopant-Placement-Induced Threshold Voltage Fluctuation," *IEDM,* pp. 841-844, 1997.

[37] Nobuyuki Sano, Kazuya Matsuzawa, Akira Hiroki, and Noriaki Nakayama. "**Probability Distribution of Threshold Voltage Fluctuations in Metal Oxide Semiconductor Field-Effect-Transistors,"** *Japanese Journal of Applied Physics,* vol. 41, no. 6, pp. L552-L554, 2002.

[38] Yoshiaki Fukuzumi, Ryota Katsumata, Masaru Kito, Mitsuru Sato, Hiroyasu Tanaka, Yuzo Nagata, Yasuyuki Matsuoka, Yashihisa Iwata, Hideaki Aochi, and Akihira Nitayama. **"Optimal Integration and Characteristics of Vertical Array Devices for Ultra-High Density, Bit-Cost Scalable Flash Memory,"** *IEDM,* pp. 449-452, 2007.

[39] K. L. Yeh **"The Fabrication and Characterization of Schttoky Barrier Thin Film Transistor with Field-Induced Drain,"** *PH. D. Dissertation, Institute of Electronics, National Chiao Tung University,* pp. 93-95, 2004.

[40] Boaz Eitan and Dov Frohman-Bentchkowsky. **"Hot-Electron Injection into the Oxide in n-Channel MOS Devices,"** *IEEE Transactionss on Electron Devices,* vol. 28, no. 3, pp. 328-340, 1981.

[41] E. Takeda, A. Shimizu, and T. Hagiwara. **"Role of Hot-Hole Injection in Hot-Carrier Effects and the Small Degraded Channel Region in MOSFET's**," *IEEE Electron Device Letters,* vol. 4, no. 9, pp. 329–331, 1983.

[42] Felicia E. Pagaduan, Cary Y. Yang, Toru Toyabe, Yashhiro Nishioka, Akemi Hamada, Yasho Igura, and Eiji Takeda. "**Simulation of Substrate Hot-Electron Injection,"** *IEEE Transactionss on Electron Devices,* vol. 37, no. 4, pp. 994-998, 1990.

[43] Ben G. Streetman and Sabjay Banerjee. **"MOSFET Scaling and Hot Electron Effects,"** *Solid State Electron Devices (Fifth Edition)*, pp. 307-311.

[44] Simon Tam, Ping-Keung Ko, and Chenming Hu. **"Lucky-Electron Model of Channel Hot-Electron Injection in MOSFET's,"** *IEEE Transactionss on Electron Devices,* vol. 31, no. 9, pp. 1116-1125, 1984.

[45] Chang-Hoon Choi, Kwang-Hoon Oh, Jung-Suk Goo, Zhiping Yu, and Bobert W. Dutton. "**Direct Tunneling Current Model for Circuit Simulation,"** *IEDM,* pp. 735-738, 1999.

[46] M. Lenzlinger and E.H. Snow."**Fowler-Nordheim Tunneling into Thermally Grown SiO_2,"** *Journal of Applied Physics*, vol. 40, pp. 278-283, 1969.

[47] J. Chen, T.Y. Chan, I.C. Chen, P.K. Ko, and Chenming Hu. **"Subbreakdown Drain Leakage Current in MOSFET,"** *IEEE Electron Device Letters,* vol. 8, no. 11, pp. 515-517, 1987.

[48] K. Lehovec and A. Fedotowsku. "**Charge Retention of MNOS Devices Limited by Frenkel-Poole Detrapping,"** *Applied Physics Letters,* vol. 32, no. 5, pp. 335-338, 1987.

[49] Yang (Larr) Yang and Marvin H. White**. "Charge Retention of Scaled SONOS Nonvolatile Memory Devices at Elevated Temperatures,"** *Solid-State Electronics,* vol 44, no 6, pp. 949-958, 2000.

[50] Kinam Kim and Jungdal Choi. **"Future Outlook of NAND Flash Technology for 40nm Node and Beyond,"** *Non-Volatile Semiconductor Memory Workshop,* pp. 9-11, 2006.

[51] J. Fu, N. Singh, K. D. Buddharaju, S. H. G. Teo, C. Shen, Y. Jiang, C. X. Zhu, M.

B. Yu, G. Q. Lo, N. Balasubramanian, D. L. Kwong, E. Gnani, and G. Baccarani.

"Si-Nanowire Based Gate-All-Around Nonvolatile SONOS Memory Cell,"

IEEE Electron Device Letters, vol. 29, no. 5, pp. 518-521, 2008.

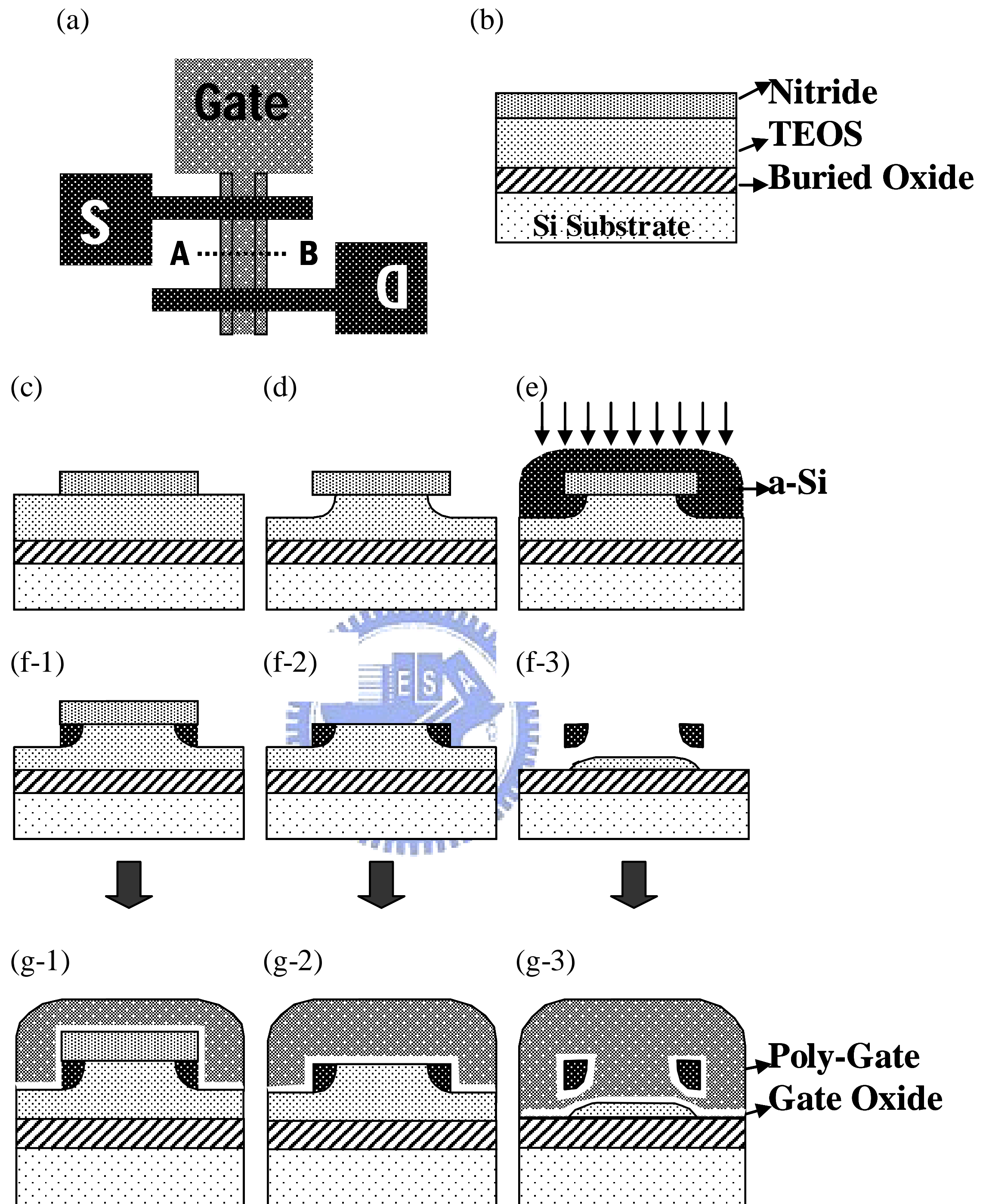
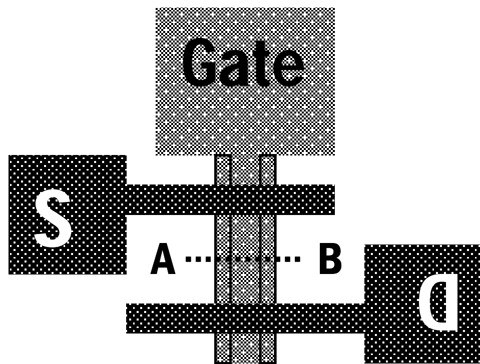


Fig. 2-1 Key steps of NW devices fabrication (a) Top-view of the NW device. (b) Nitride and TEOS formed on Si-substrate capped with a buried oxide. (c) Nitride patterned by anisotropic reactive plasma etching. (d) Undercut formed by isotropic DHF wet etching. (e) a-Si deposition and annealing, and S/D implant. (f-1) Si removal with anisotropic dry etching. (f-2) Nitride removal with hot H_3PO_4. (f-3) Portion of TEOS removed by DHF. (g-1 to g-3) gate oxide and poly gate deposition.



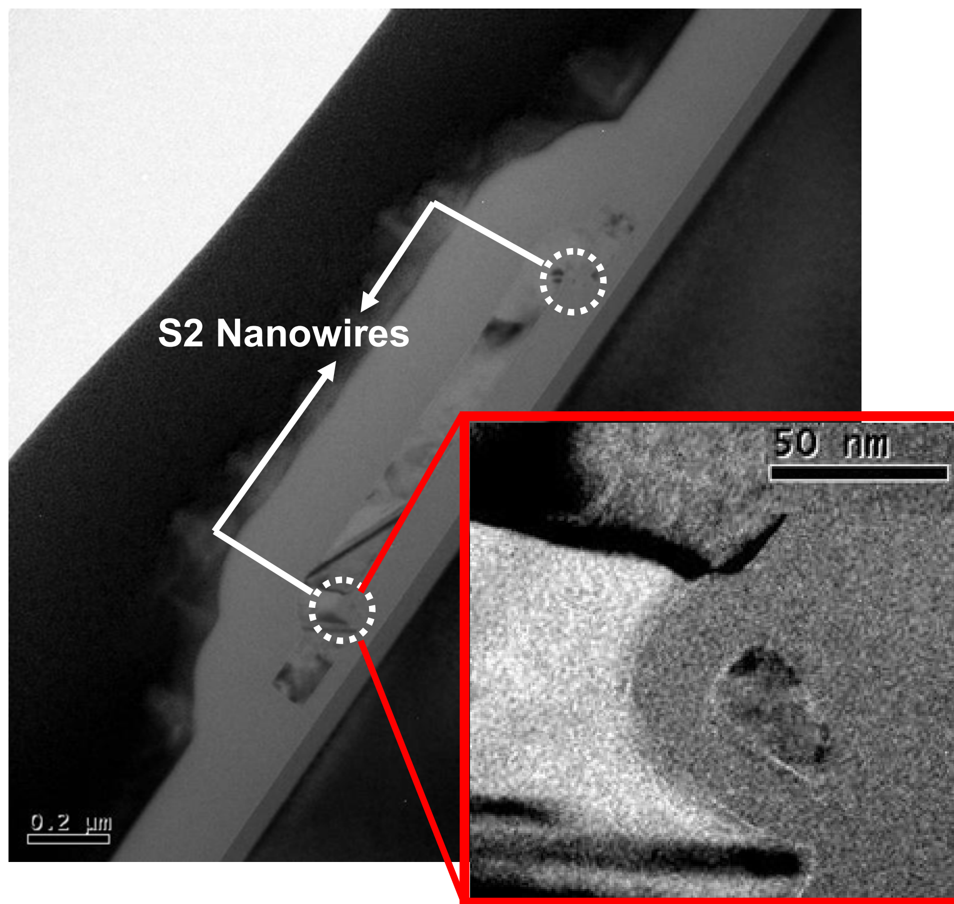


Fig. 2-2 Cross-sectional-view TEM picture of an S2 device along Line $\overline{AB}$ of the top layout.

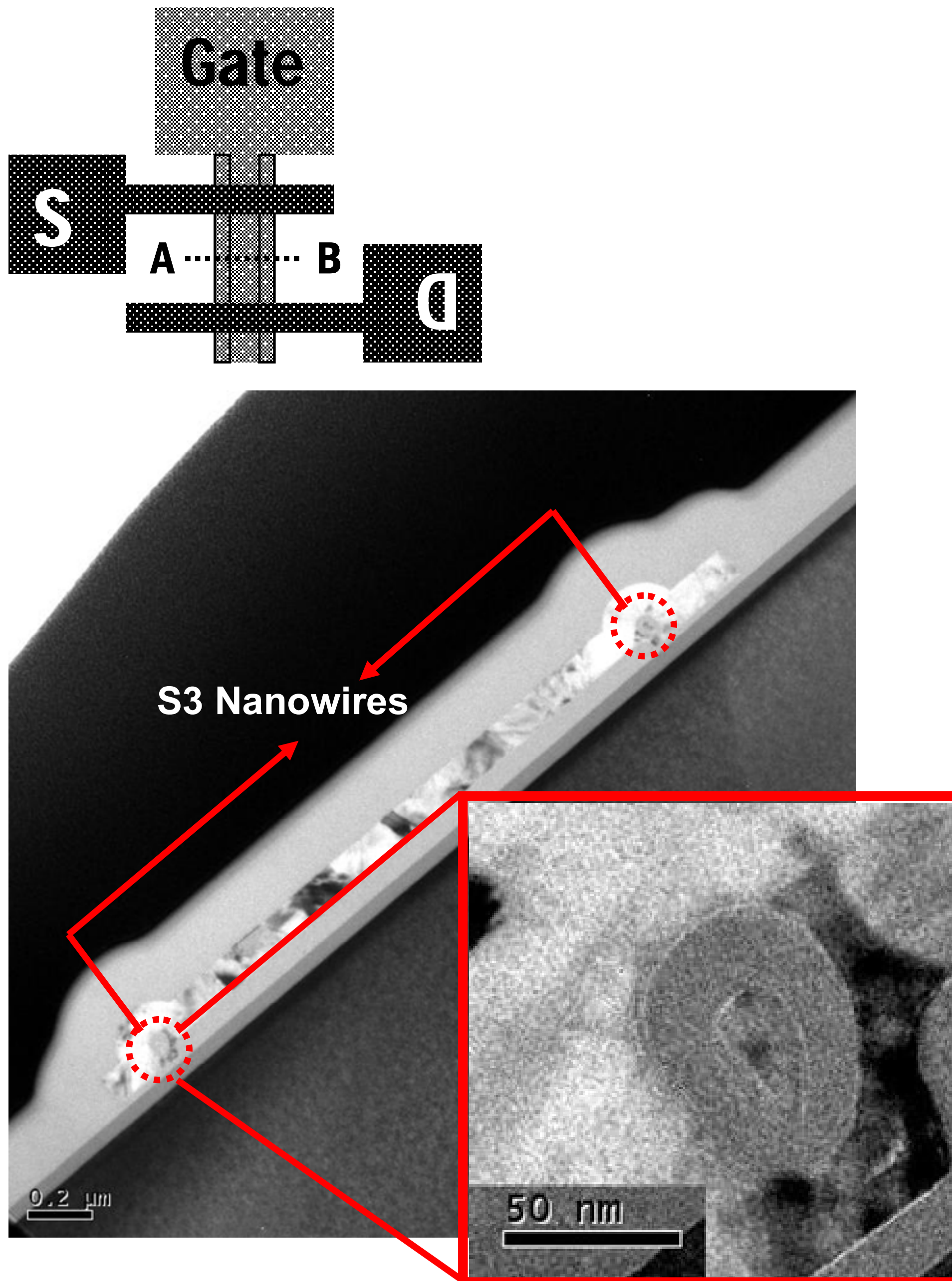


Fig. 2-3 Cross-sectional-view TEM picture of an S3 device along Line $\overline{AB}$ of the top layout.

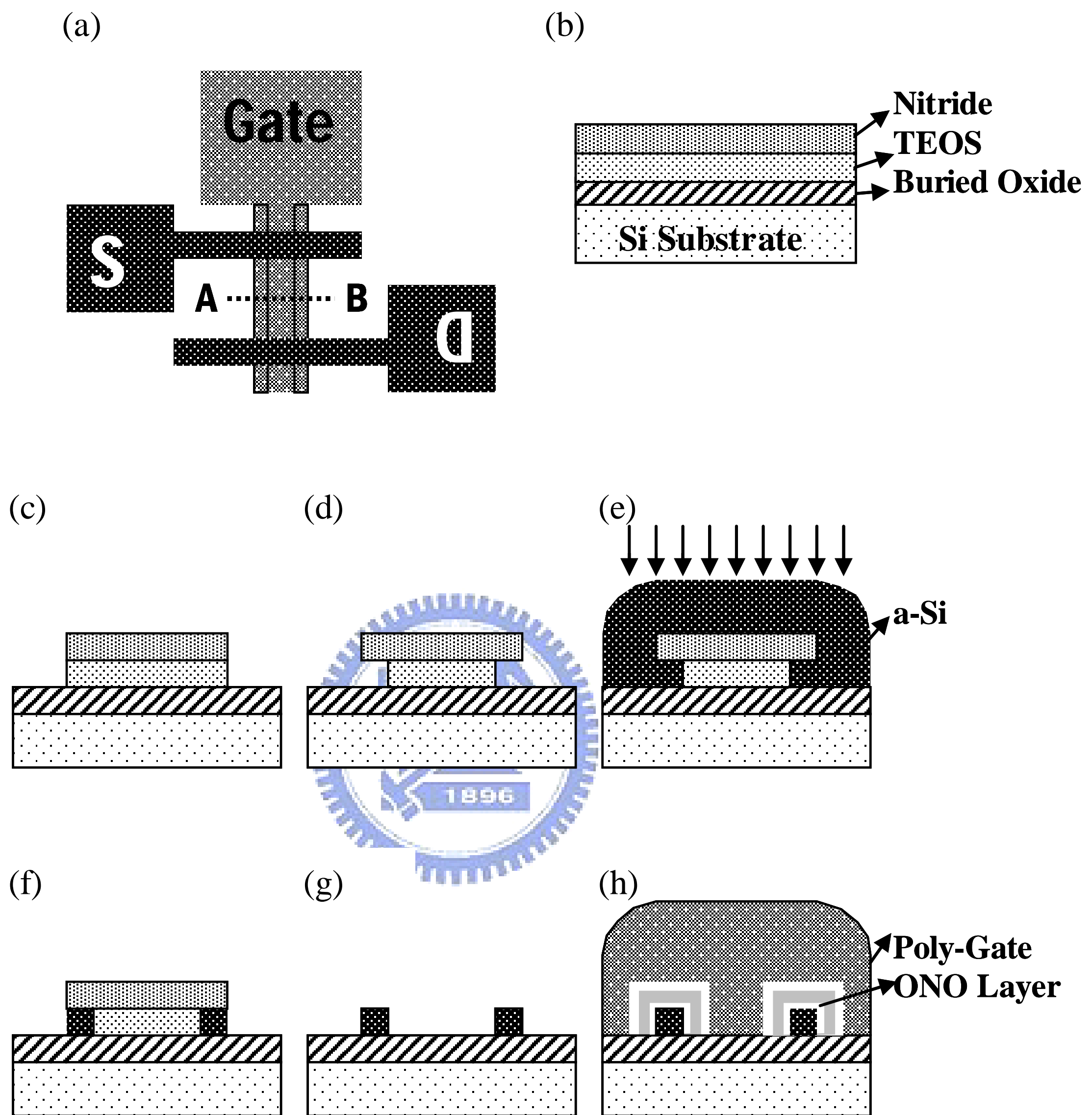


Fig. 2-4 Key steps of NW SONOS devices fabrication (a) Top-view of the NW device. (b) Nitride and TEOS formed on Si-substrate capped with a buried oxide. (c) Nitride and TEOS patterned by anisotropic reactive plasma etching. (d) Recessed cavities formed by DHF wet etching. (e) a-Si deposition and annealing, and S/D implant. (f) Si removal with anisotropic dry etching. (g) Nitride removal with hot H_3PO_4 and TEOS removed by DHF. (h) ONO stacked layer and poly gate deposition.

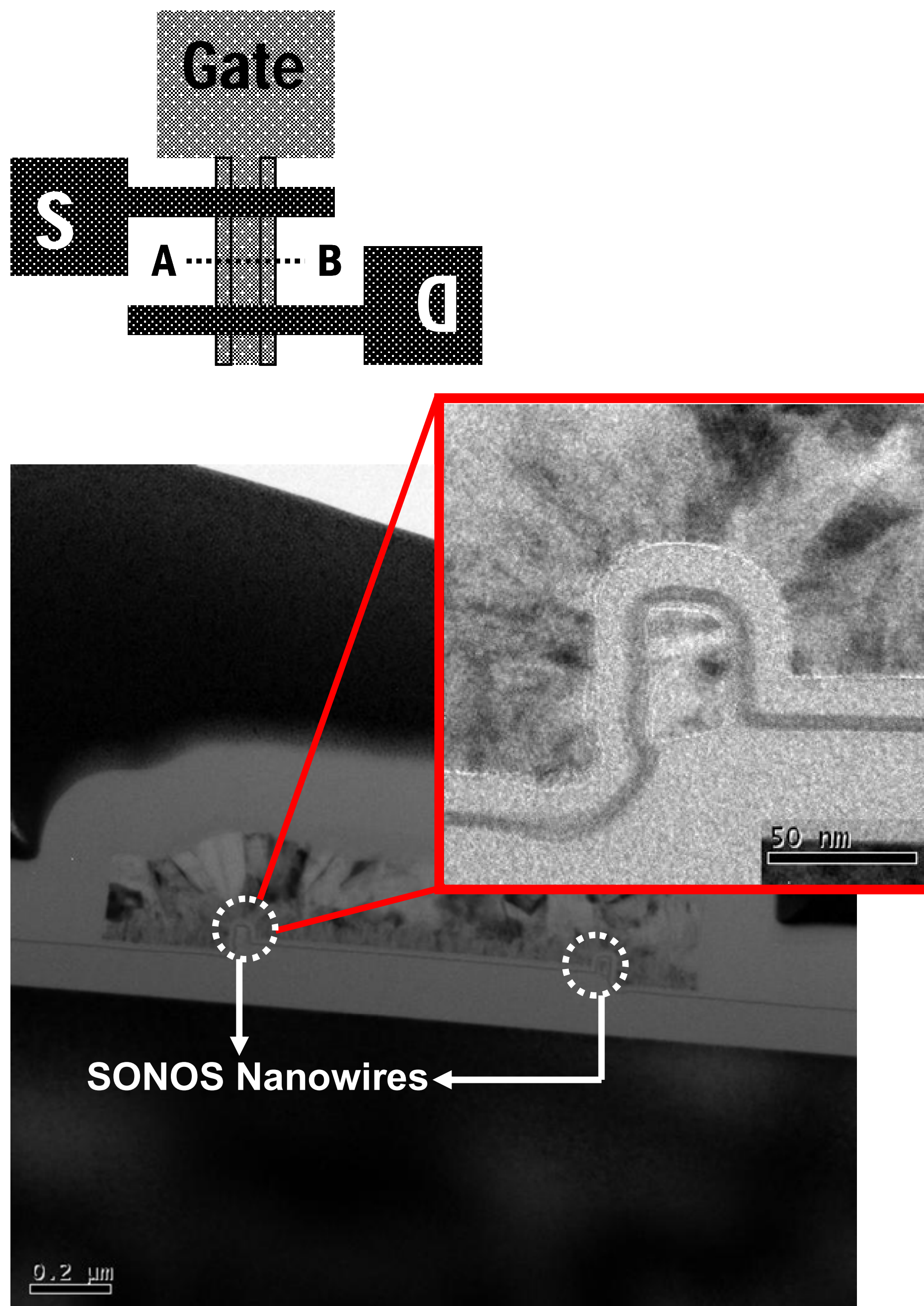


Fig. 2-5 Cross-sectional-view TEM picture of an NW SONOS device along Line $\overline{AB}$ of the top layout.

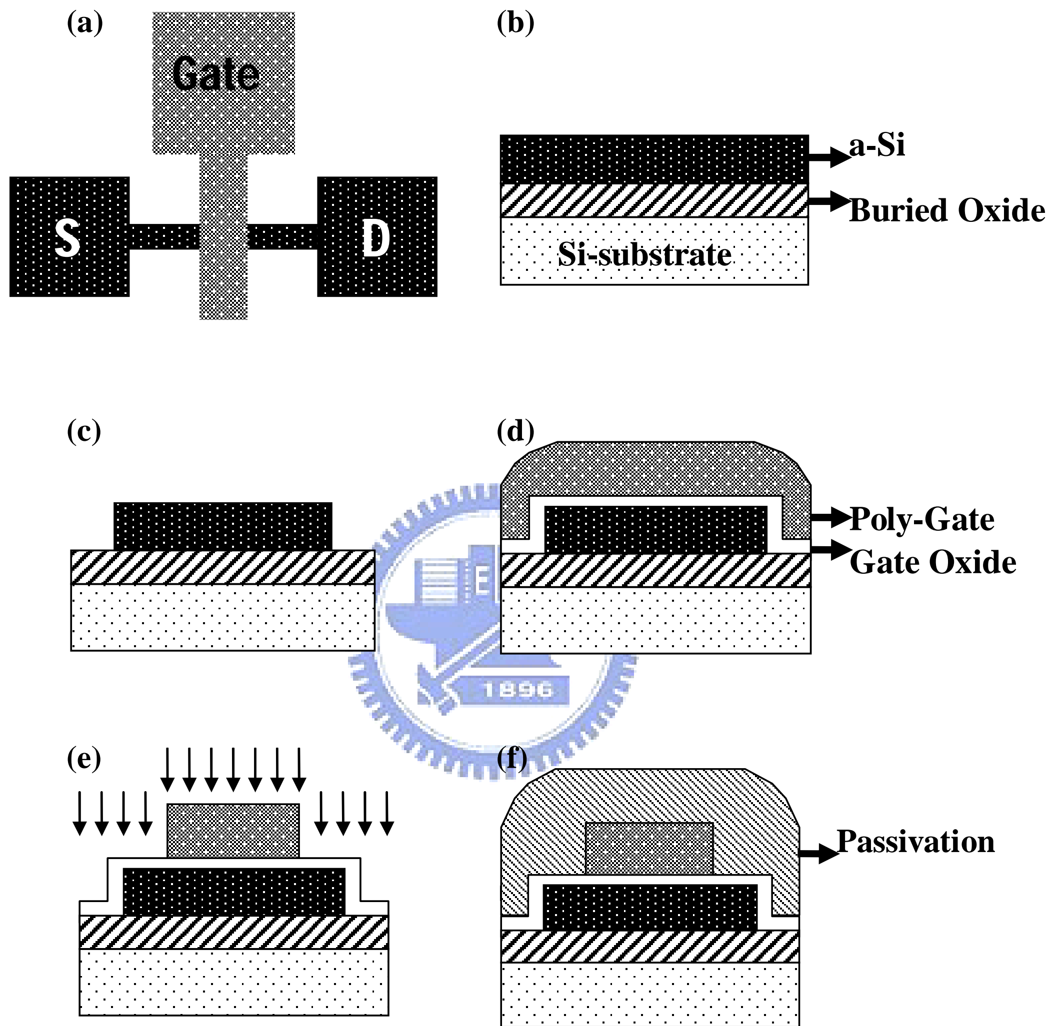


Fig. 2-6 Key steps of planar device fabrication. (a) Top view layout of the planar device. (b) a-Si formed on Si substrates capped with a buried oxide. (c) Active region definition. (d) Deposition of 20nm-thick gate oxide and n^+ poly-Si gate. (e) Gate electrode formation and subsequent S/D implant. (f) Passivation layer deposition.

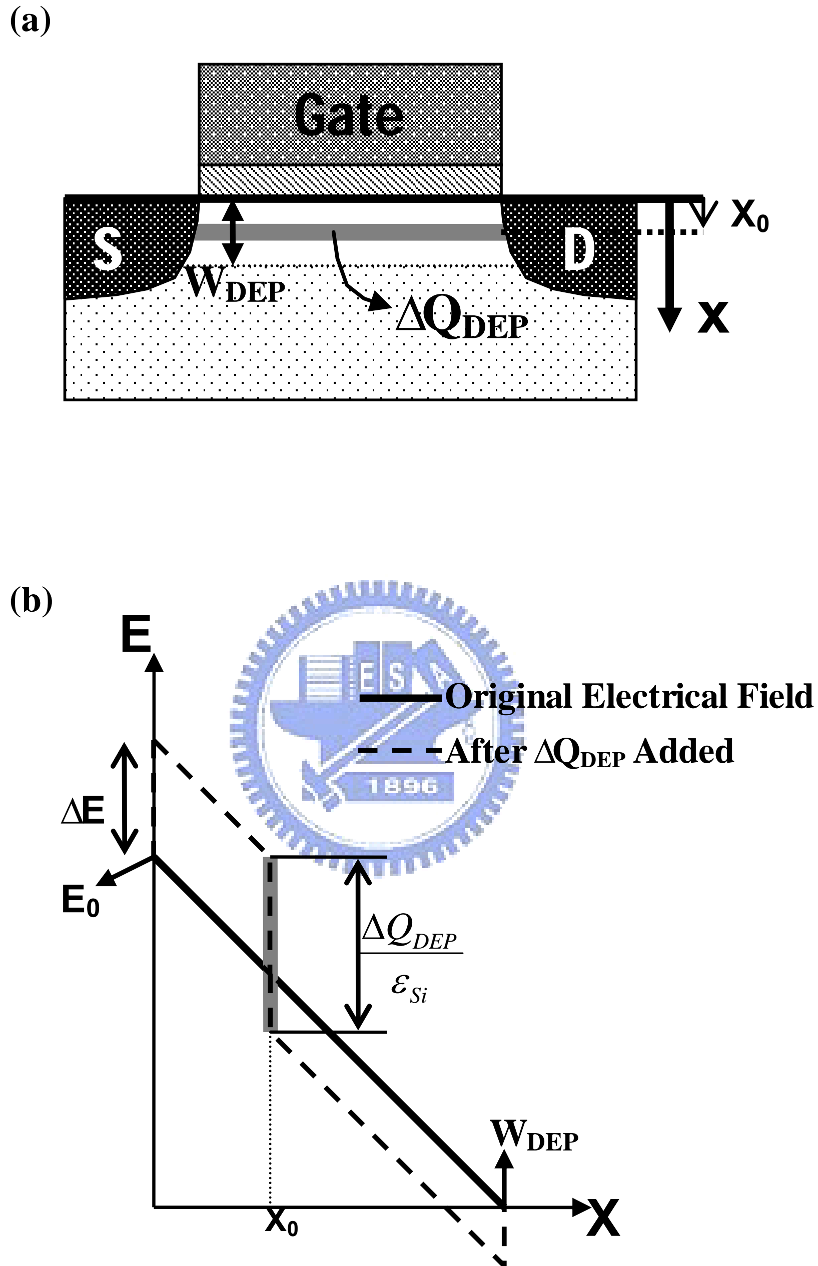


Fig. 3-1 Surface electrical field difference caused by the insertion of a sheet charge ΔQ_{DEP} . (a) Diagram of ΔQ_{DEP} within depletion region. (b) Electrical field change in depletion region induced by ΔQ_{DEP} .

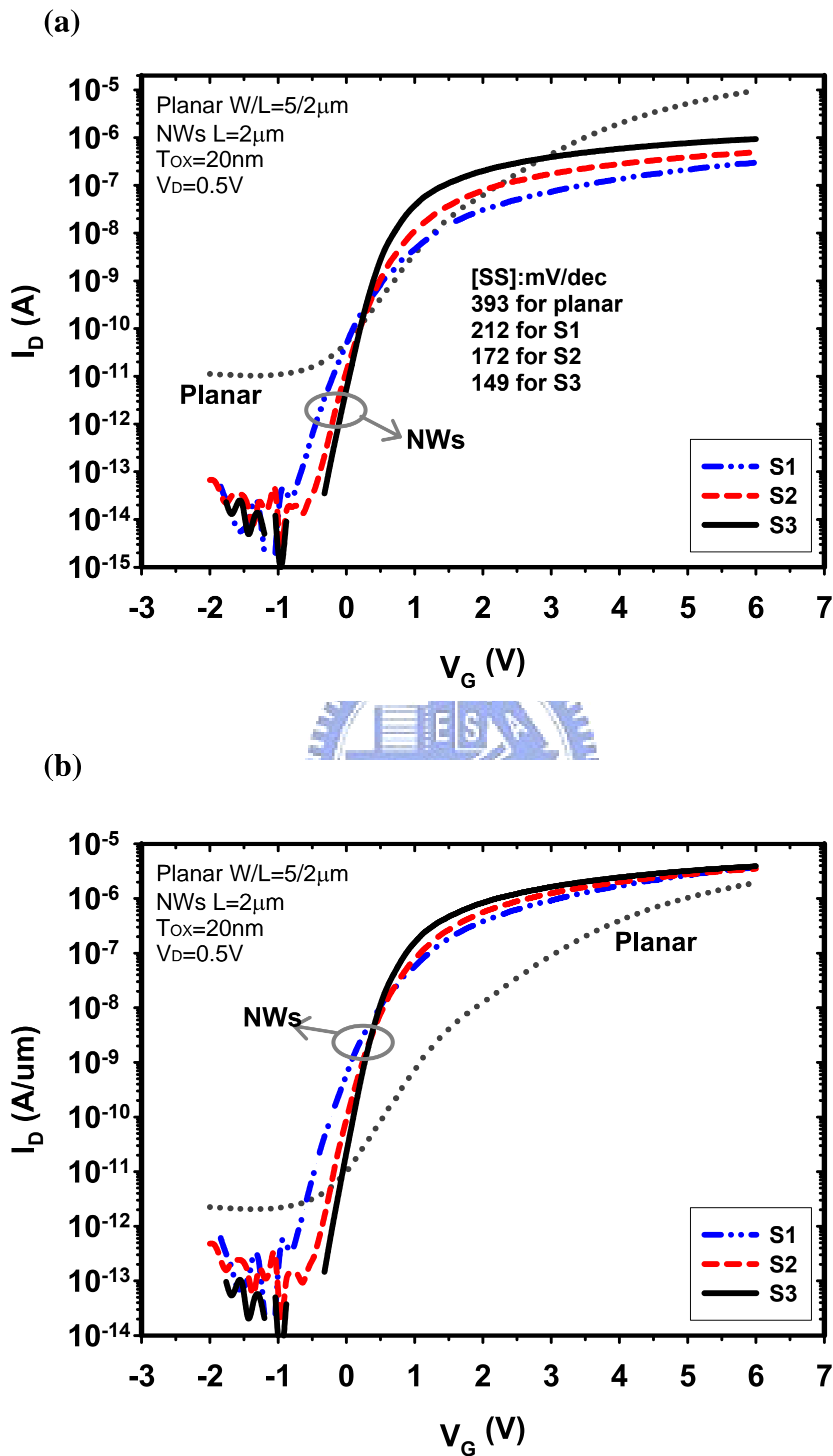


Fig. 3-2 Transfer characteristics of MOS-type devices with channel length of 2μm (a) before (b) after normalizing to channel width.

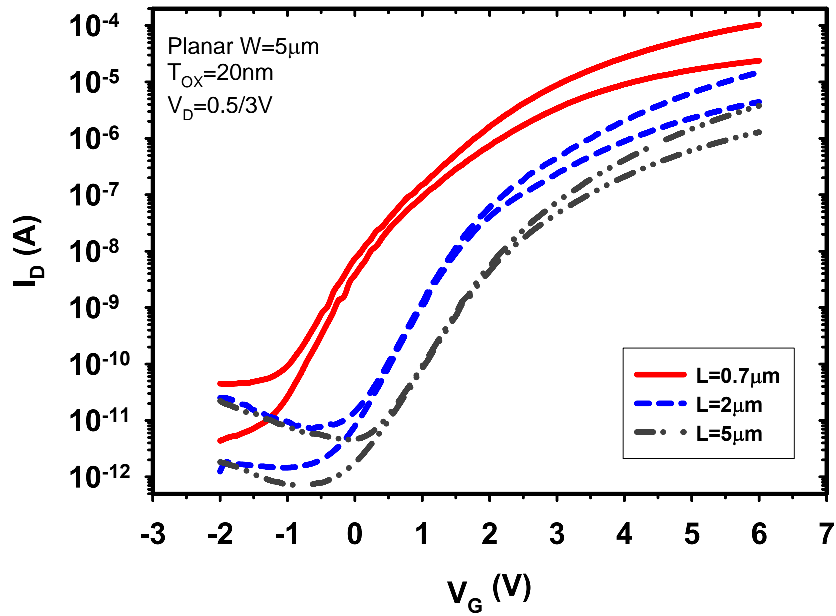


Fig. 3-3 Transfer characteristics of planar devices with different channel length.

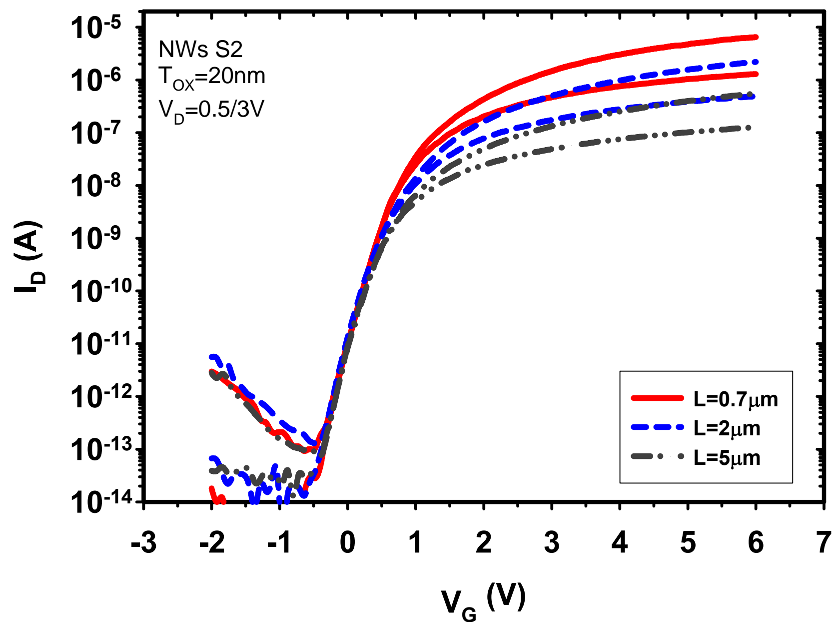


Fig. 3-4 Transfer characteristics of NW devices with different channel length.

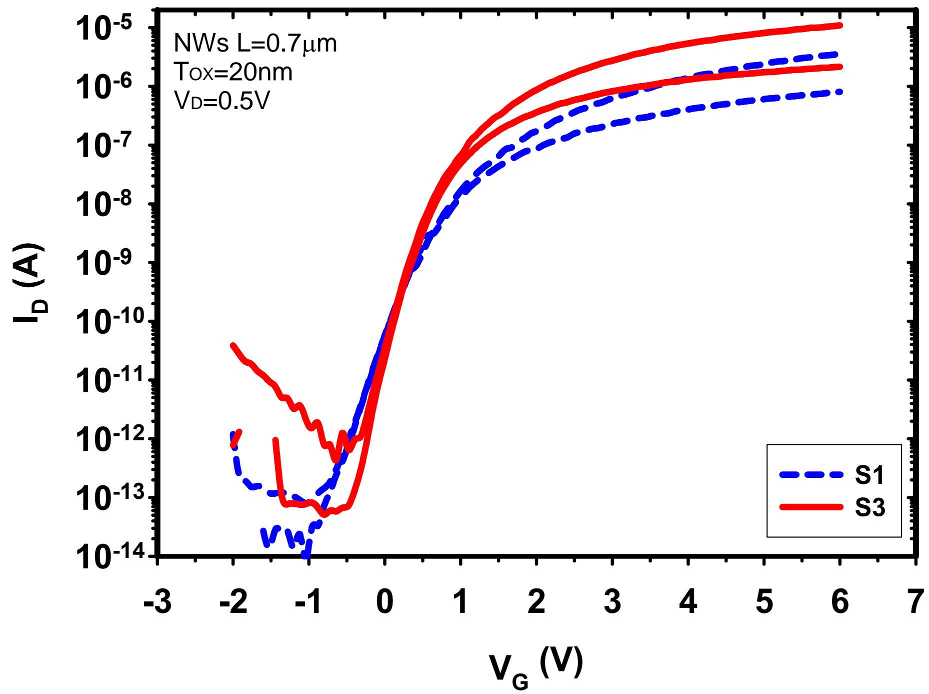


Fig. 3-5 Transfer characteristics of NW devices with channel length of 0.7μm for S1 and S3 splits.

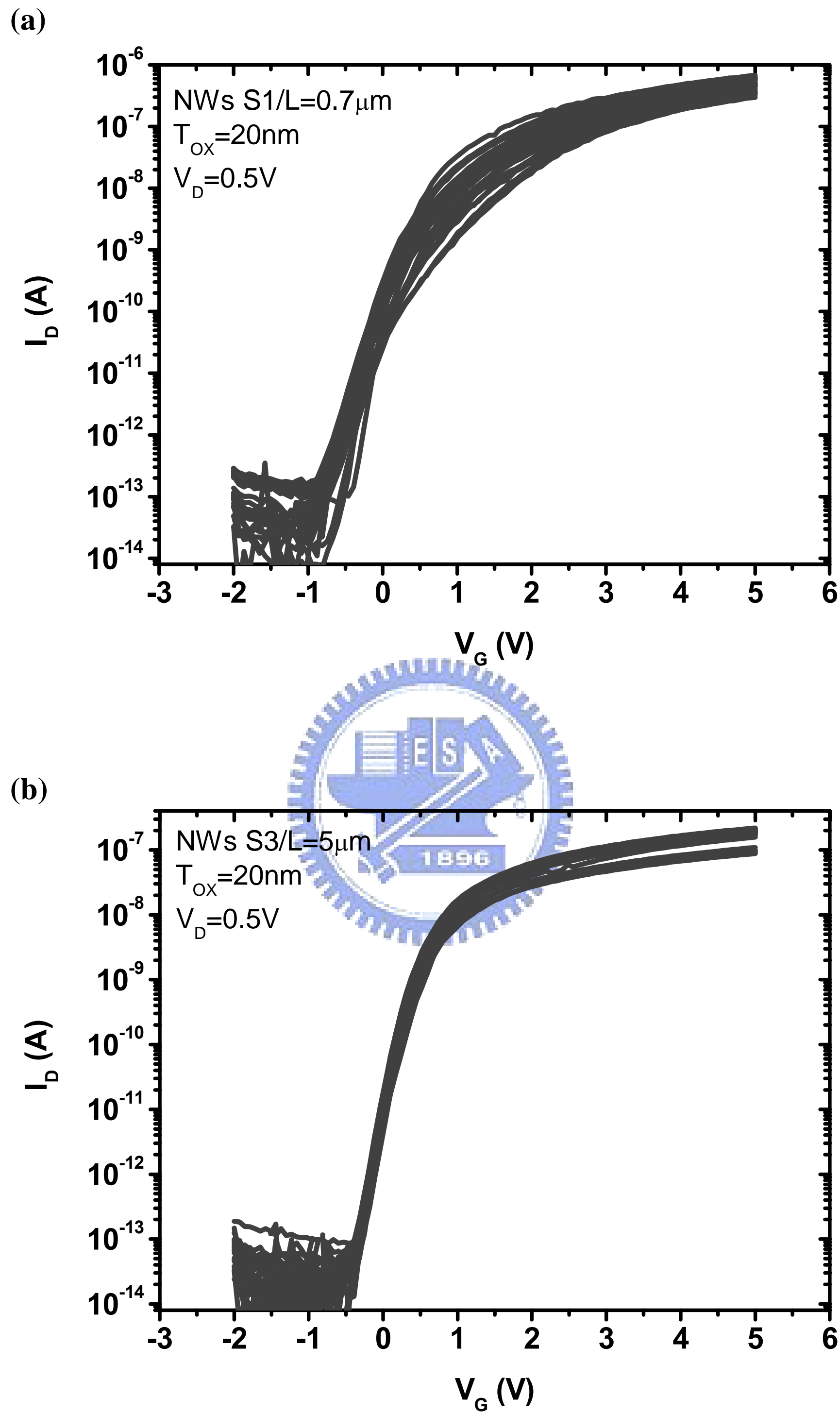


Fig. 3-6 I_D-V_G curves of thirty NW devices. (a) S1 with channel length of 0.7μm. (b) S3 with channel length of 5μm.

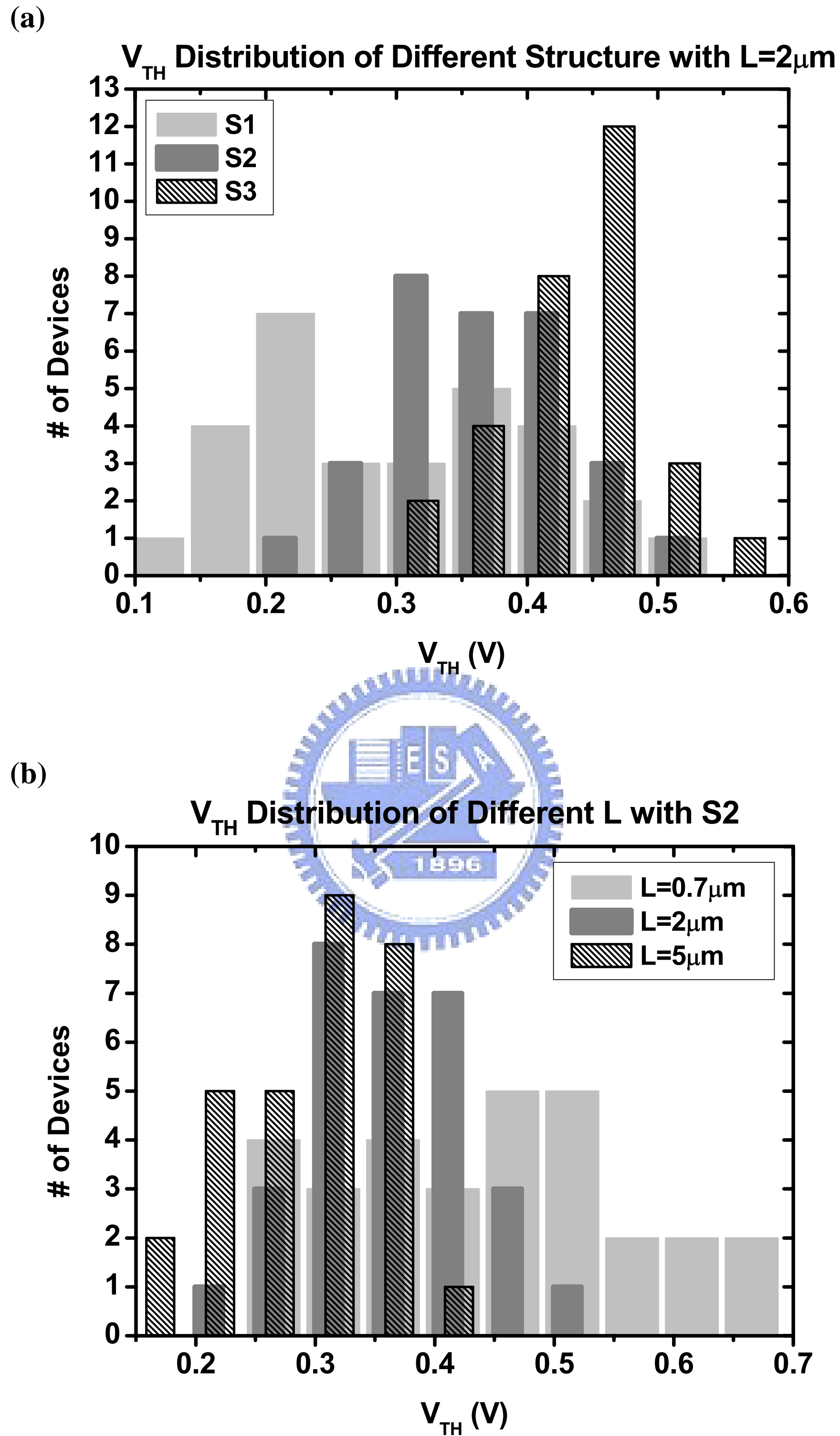


Fig. 3-7 V_{TH} distribution. (a) Different NW structures with channel length of 2μm. (b) S2 devices with different channel lengths for S2.

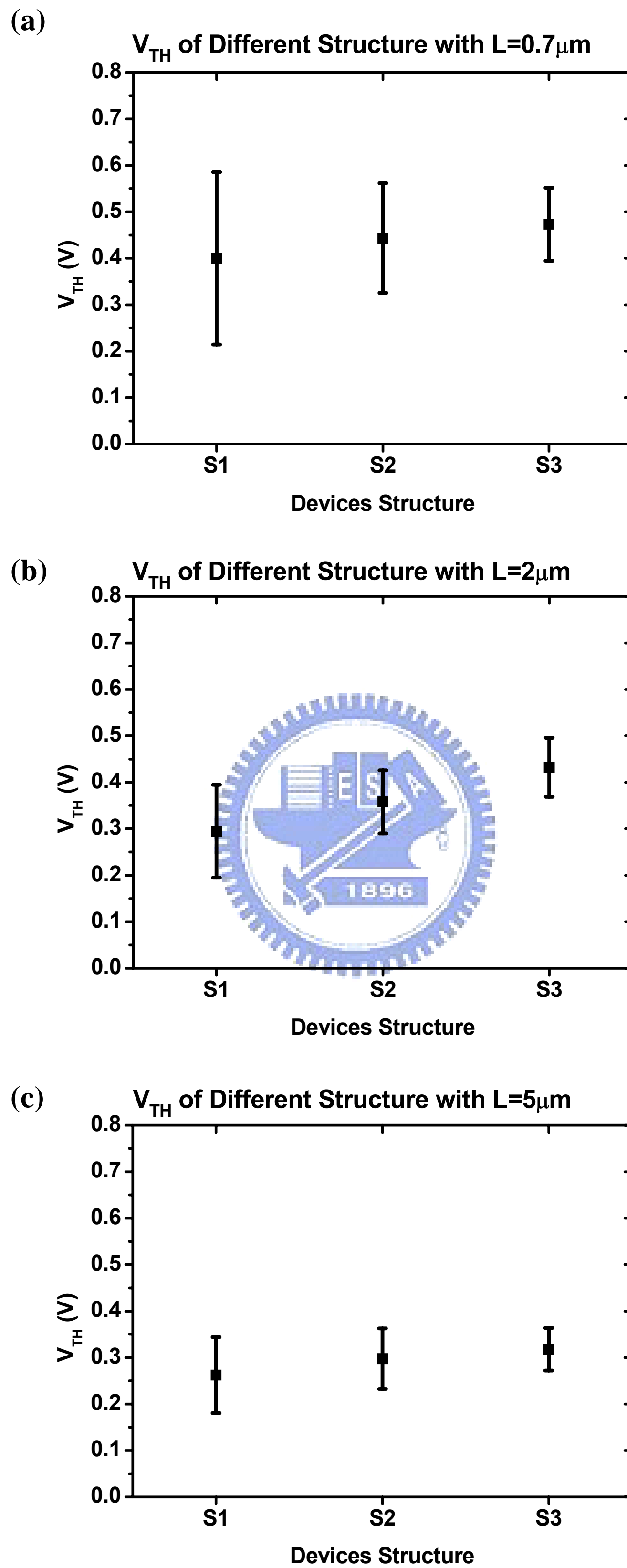


Fig. 3-8 Mean values of V_{TH} for different structures with (a) L=0.7μm, (b) L=2μm, and (c) L=5μm. Error bars represent standard deviations.

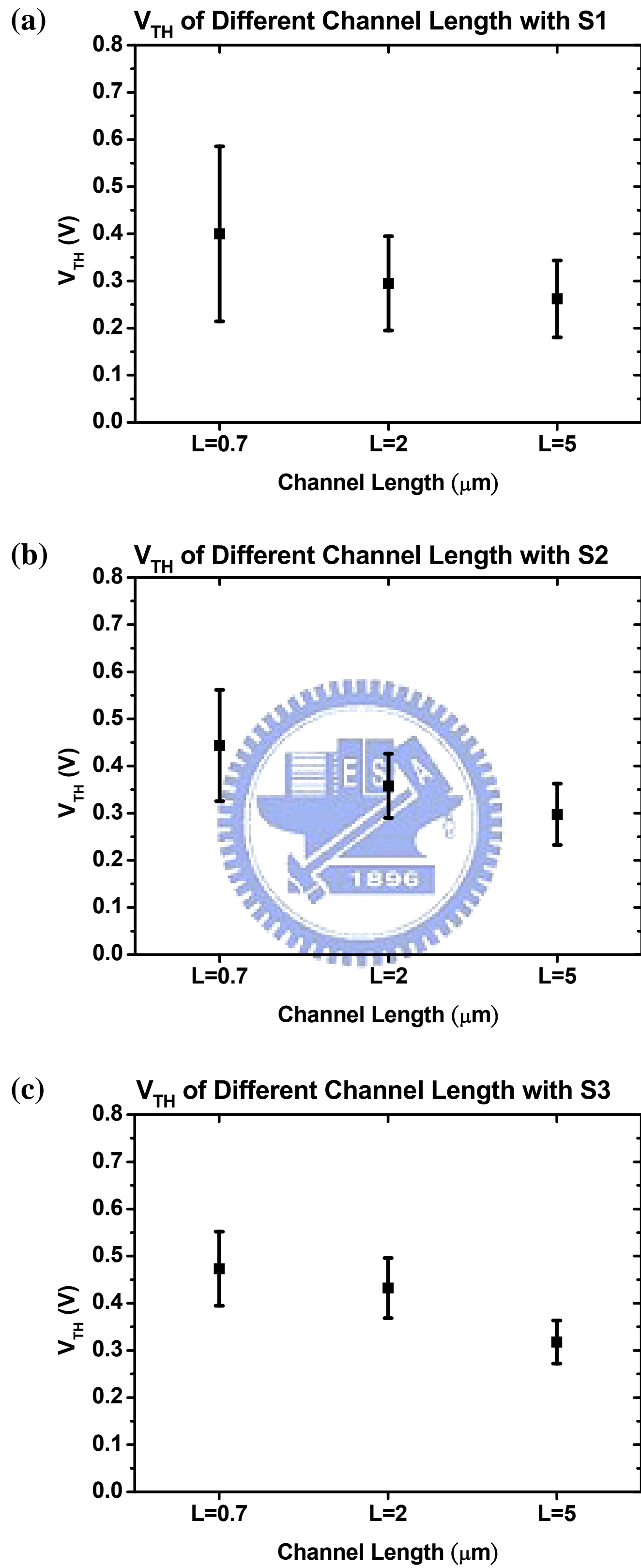


Fig. 3-9 Mean value of V_{TH} versus channel length for (a) S1, (b) S2, and (c) S3 splits. Error bars represent standard deviations.

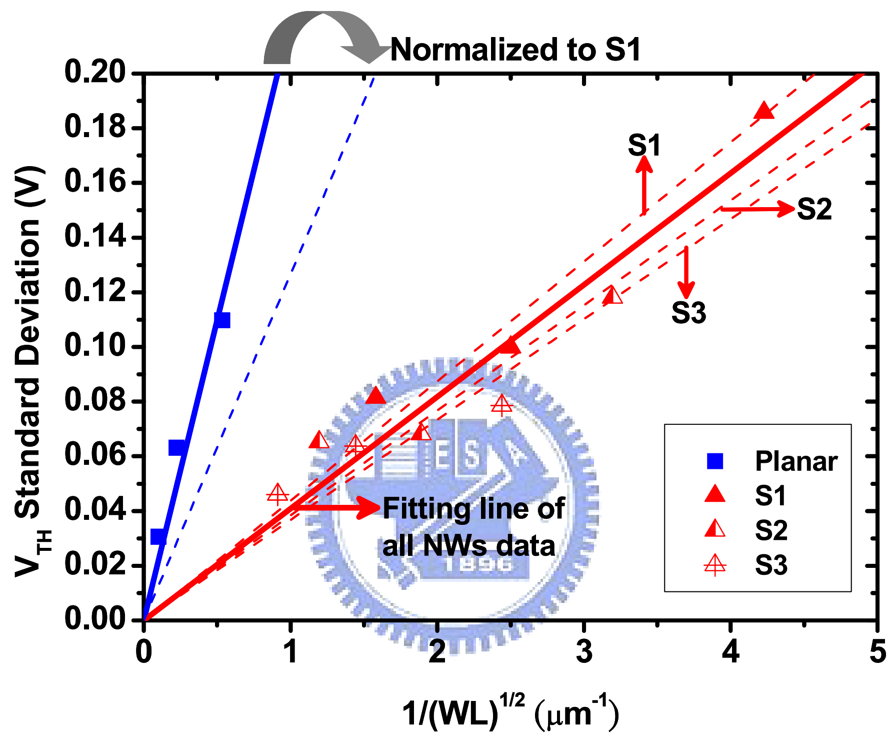


Fig. 3-10 Standard deviation of V_{TH} versus $1/\sqrt{WL}$ for planar and NW devices.

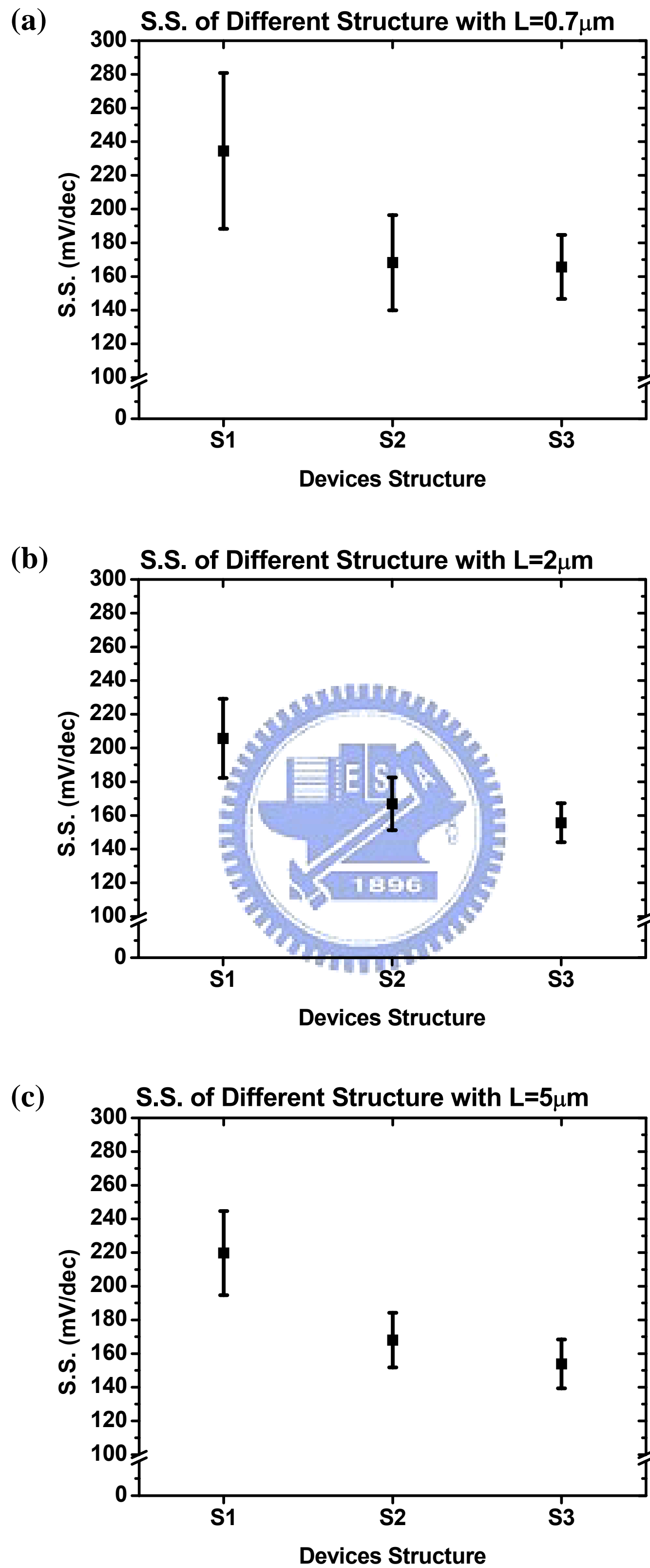


Fig. 3-11 Mean values of SS for different structures with (a) L=0.7μm, (b) L=2μm, and (c) L=5μm. Error bars represent standard deviations.

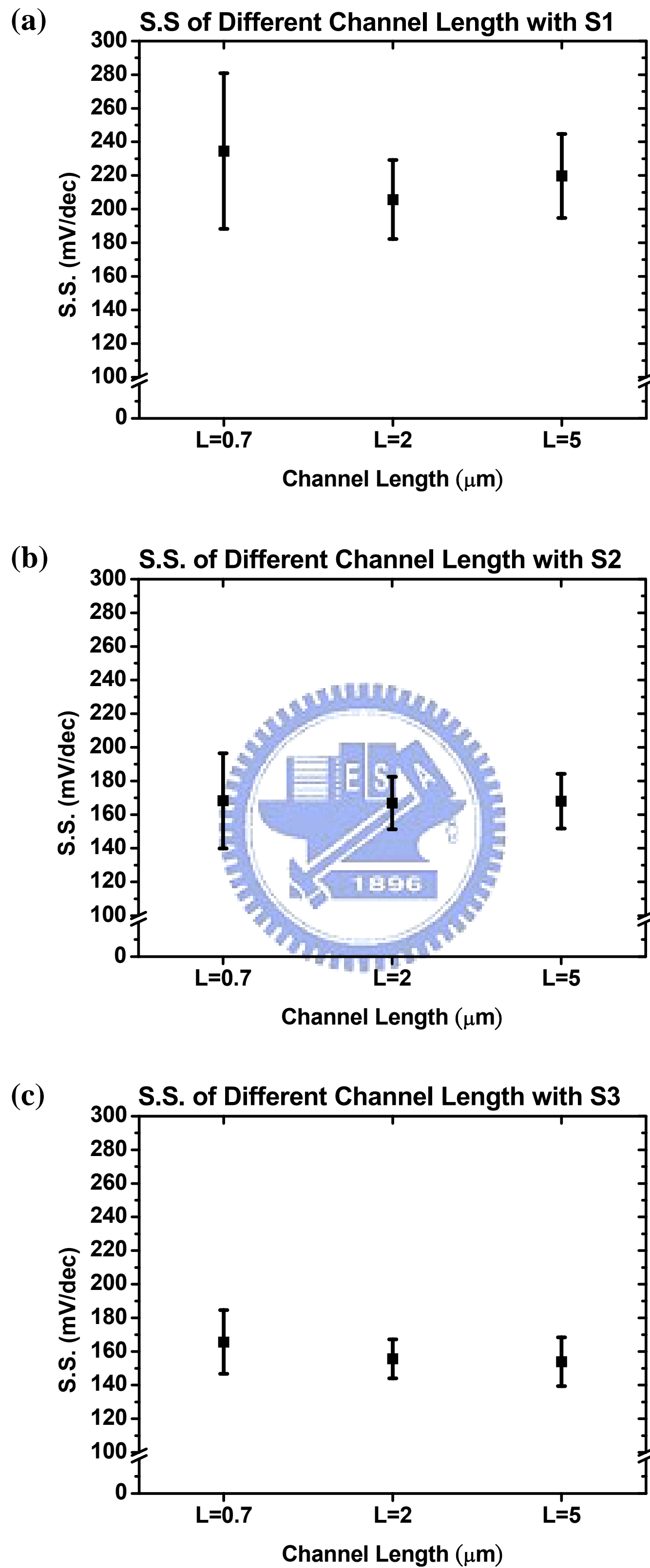


Fig. 3-12 Mean value of SS versus channel length for (a) S1, (b) S2, and (c) S3. Error bars represent standard deviations.

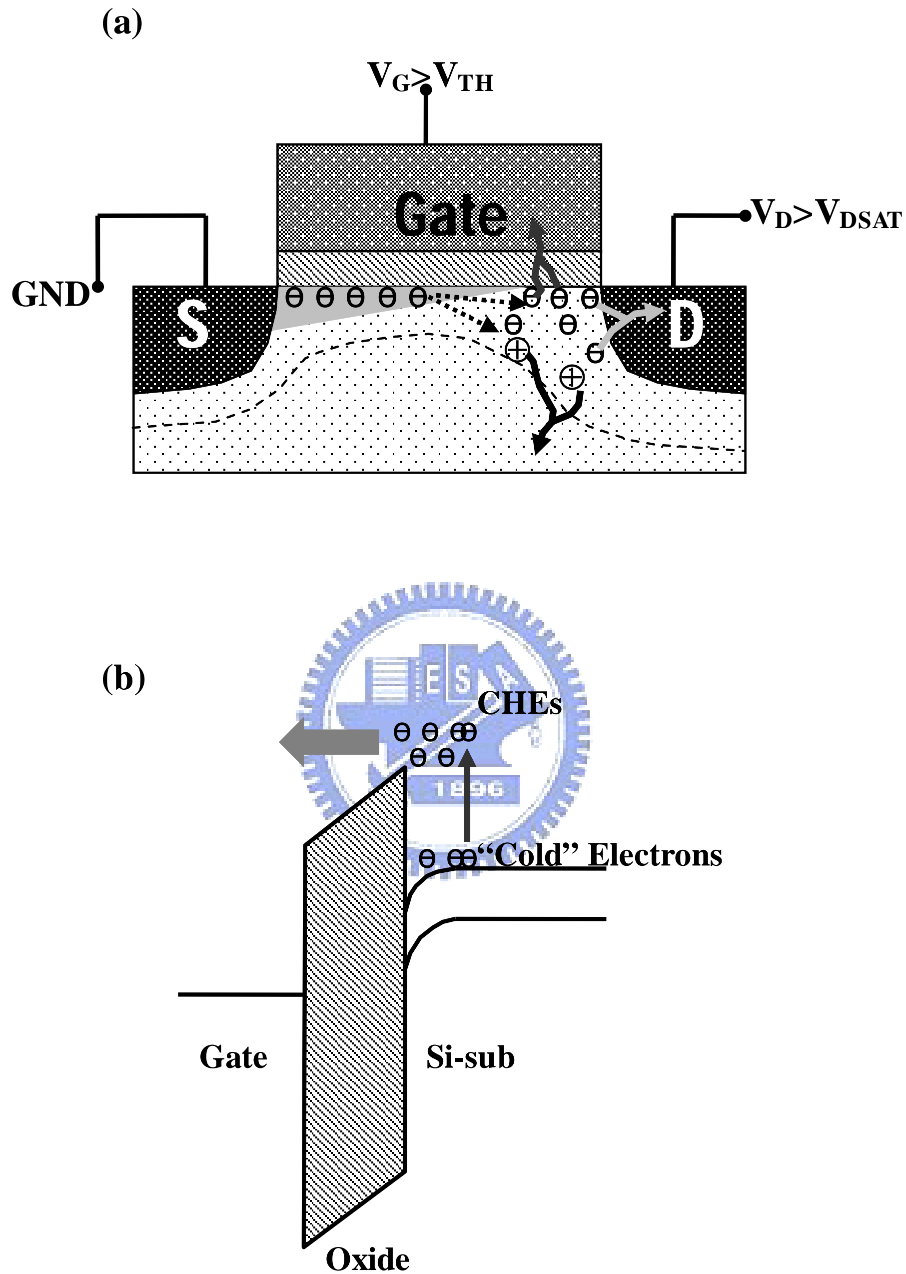


Fig. 4-1 Channel Hot Electron Injection (CHEI). (a) Channel hot electrons (CHEs) caused by strong lateral electrical field in pinch-off region. (b) Hot electrons gain sufficient energy and are injected into gate.

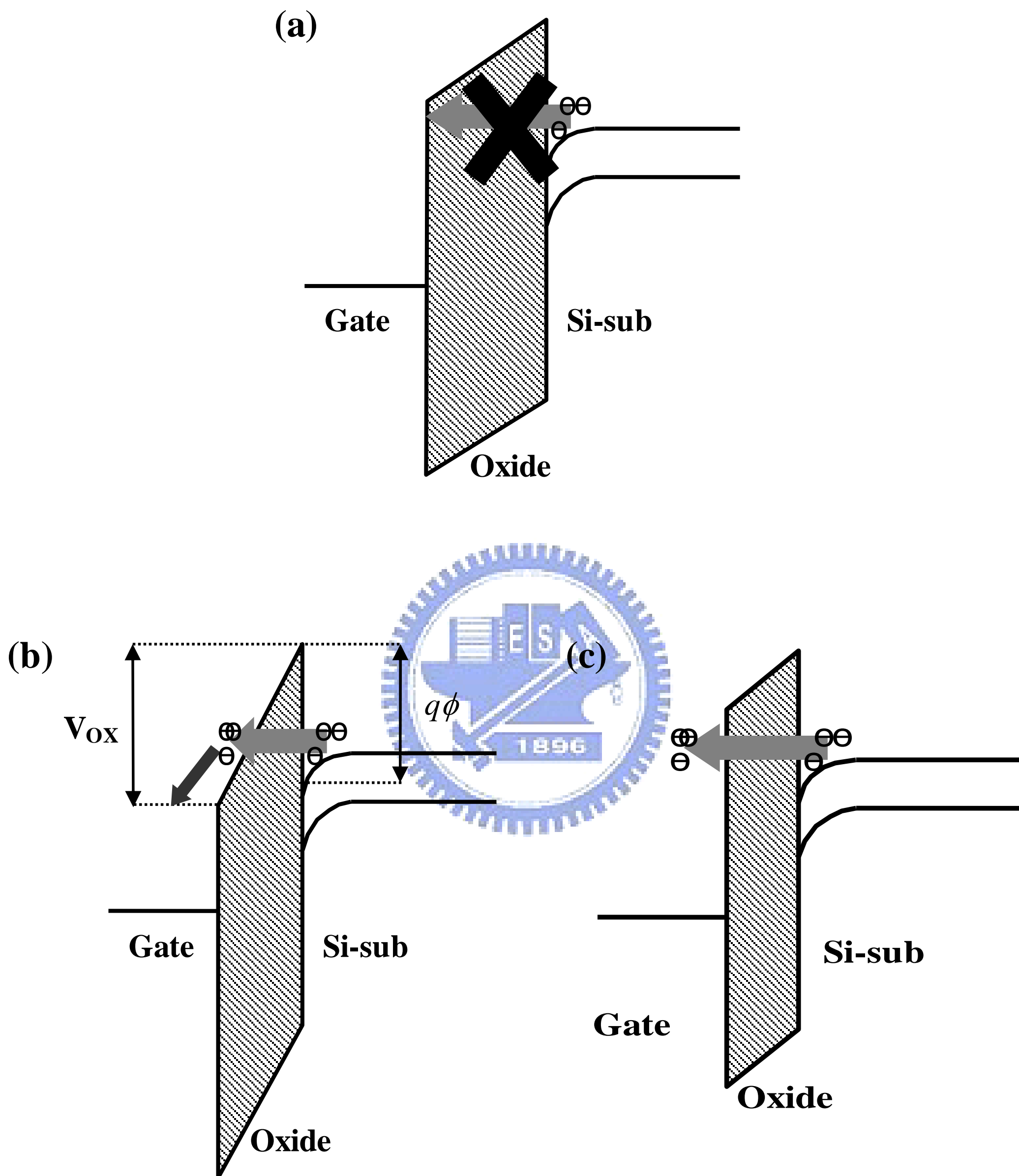


Fig. 4-2 (a) Carrier with energy lower than barrier height can't tunnel into gate in classical theory. (b) Fowler-Nordheim tunneling occurs when V_{OX} is higher than band-offset ($q\phi$). (c) Direct tunneling occurs when oxide is thin enough.

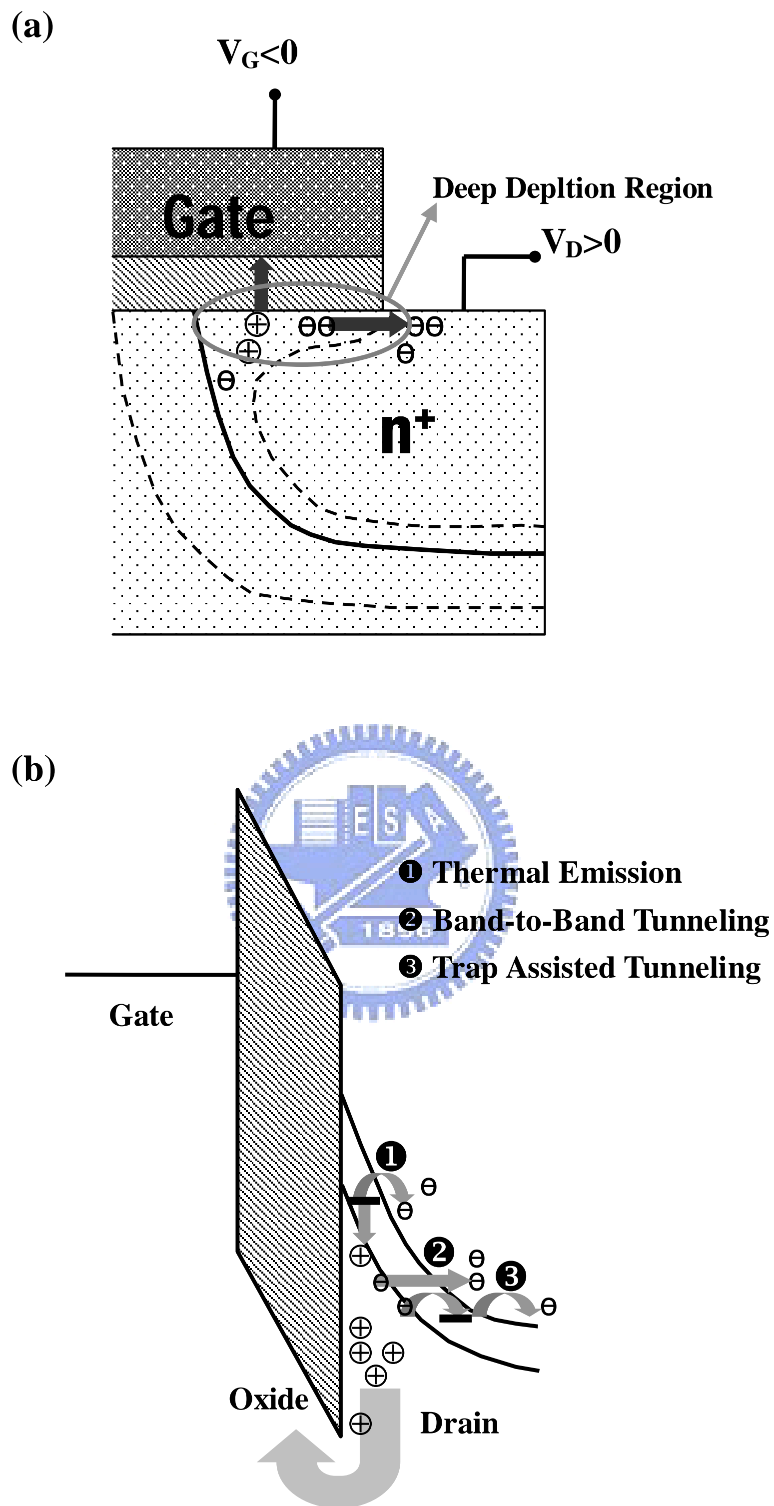


Fig. 4-3 Band-to-Band Tunneling (BTBT). (a) Deep depletion appears in n^+ drain region overlapped by gate. (b) Main tunneling mechanism occurs in deep depletion region.

❶ **Frenkel-Poole Emission**
❷ **Trap to Band Tunneling**
❸ **Trap to Trap Tunneling**
❹ **Band to Trap Tunneling**

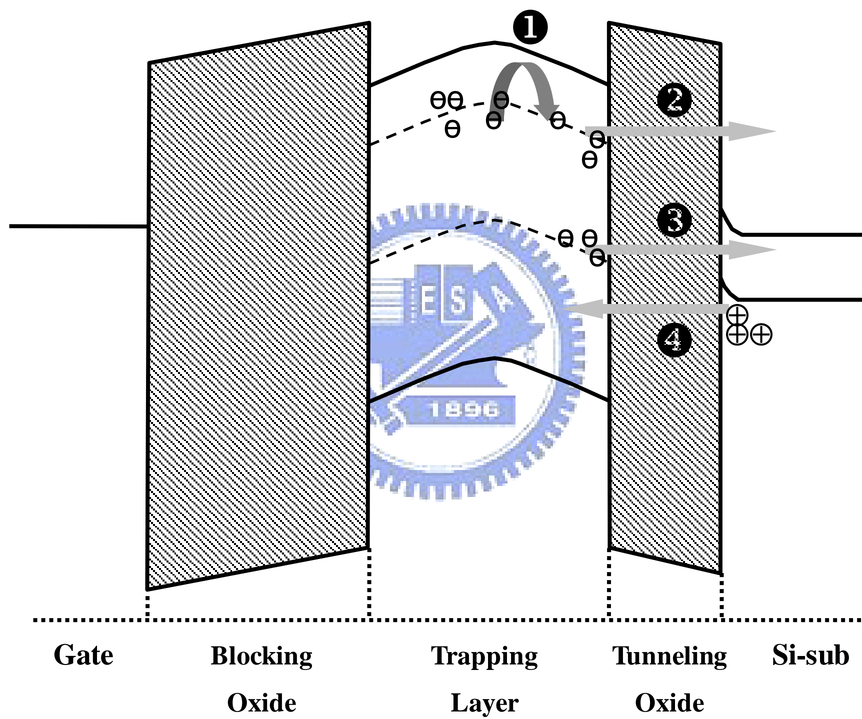


Fig. 4-4 Data lost paths in SONOS flash memory.

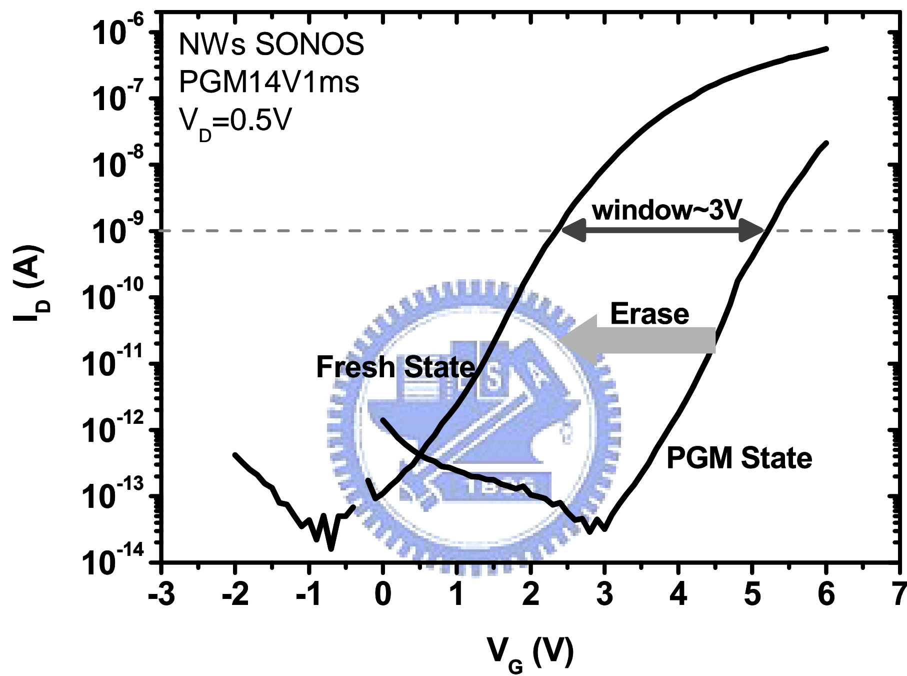


Fig. 4-5 Transfer characteristics for an NW SONOS-Device programmed with V_{TH} shift of 3V before erasing operation.

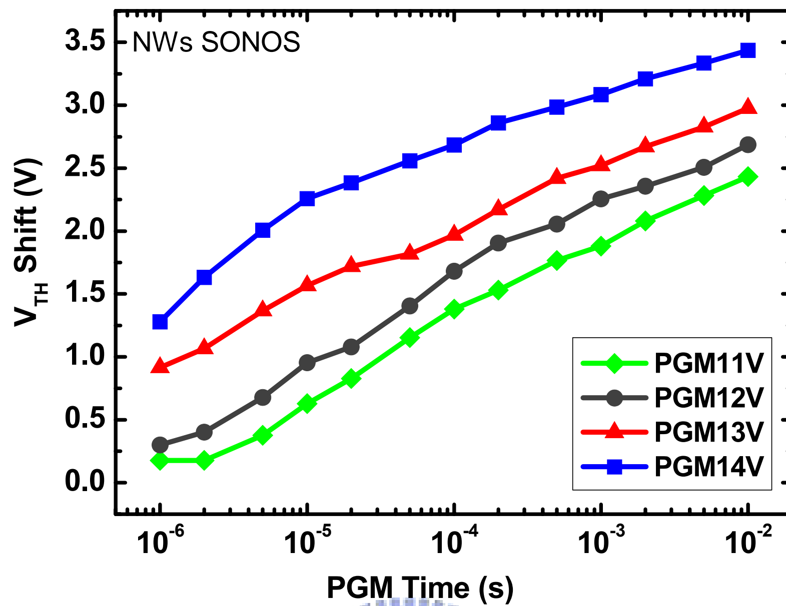


Fig. 4-6 Programming characteristics of NW SONOS-devices.

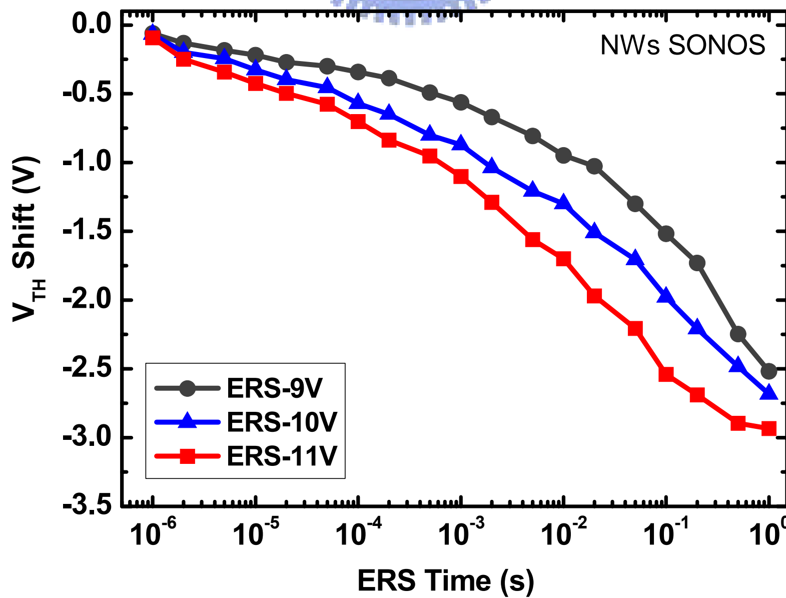


Fig. 4-7 Erasing characteristics of NW SONOS-devices.

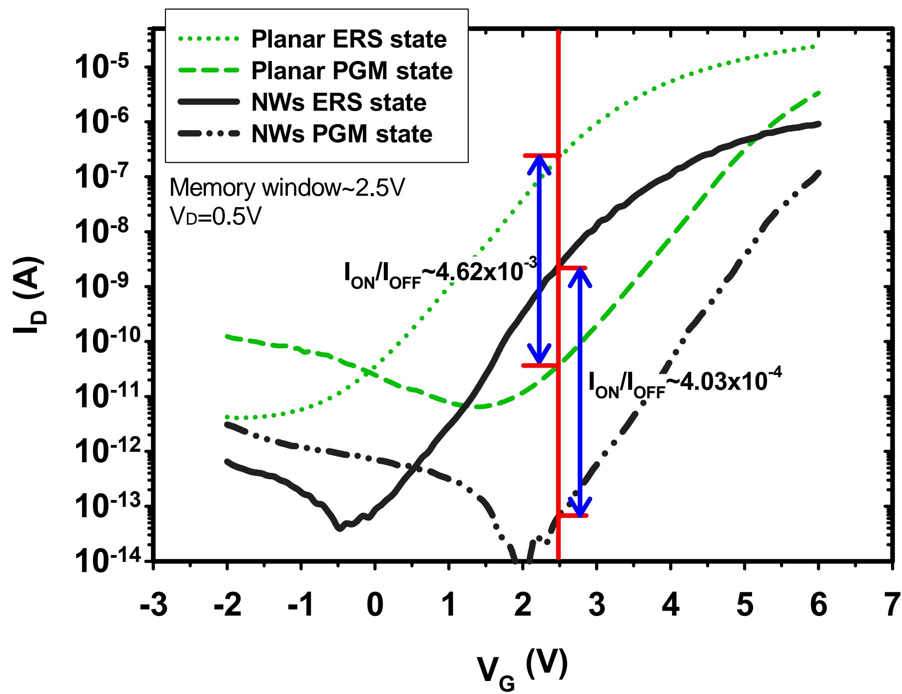


Fig. 4-8 I_{on}/I_{off} ratio of planar and NWs SONOS-devices with memory window of 2.5V.

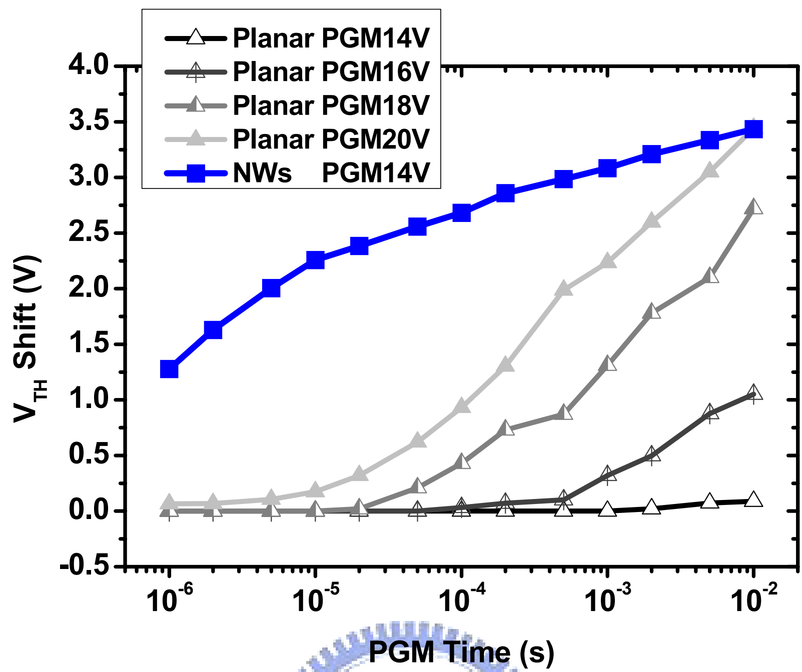


Fig. 4-9 Programming characteristics of planar SONOS-devices.

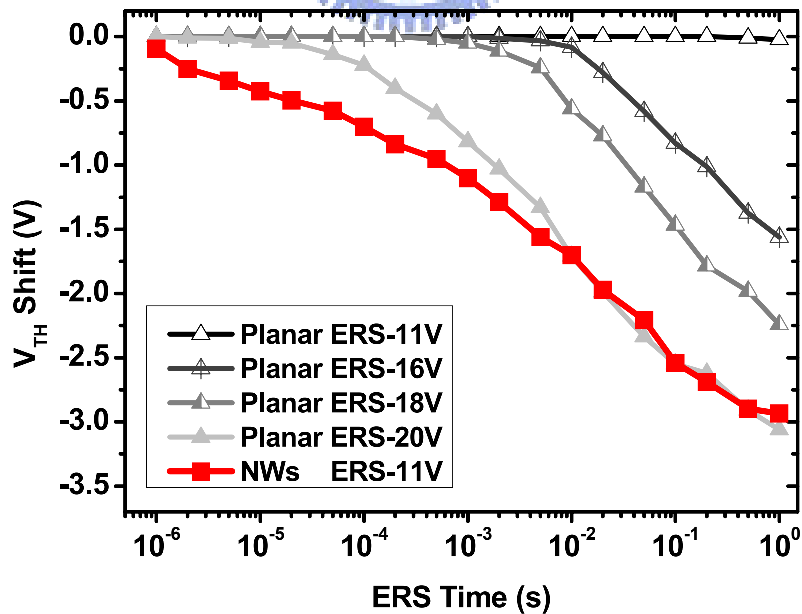
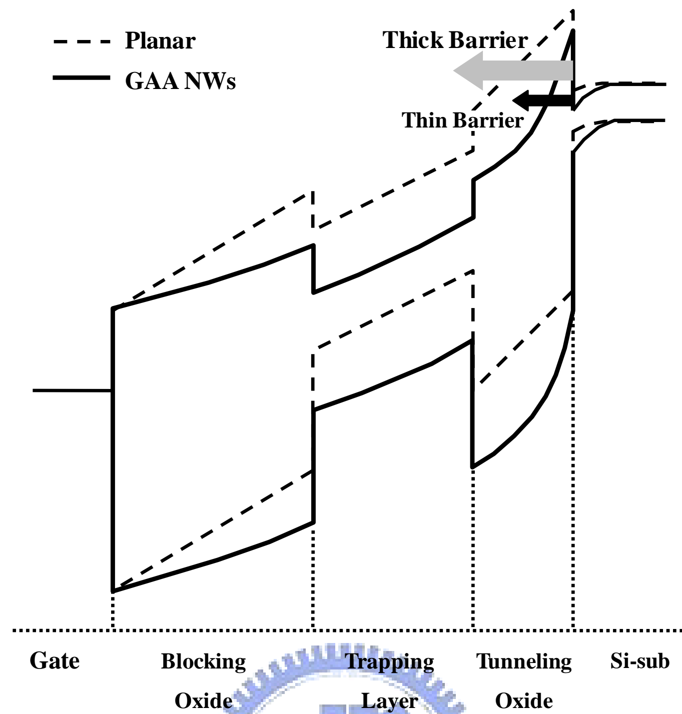


Fig. 4-10 Erasing characteristics of planar SONOS-devices.

(a)



(b)

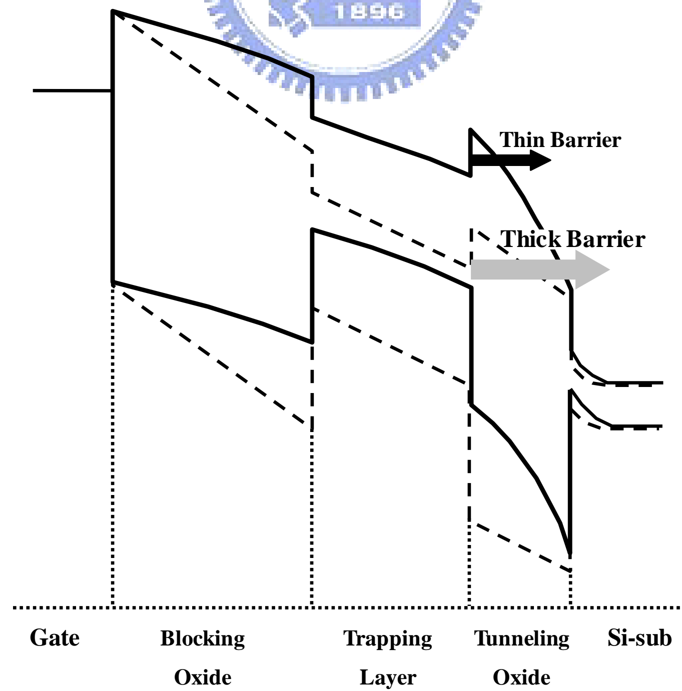


Fig. 4-11 V Voltage dropped across ONO region of planar and GAA NWs devices for (a) programming (b) erasing operations.

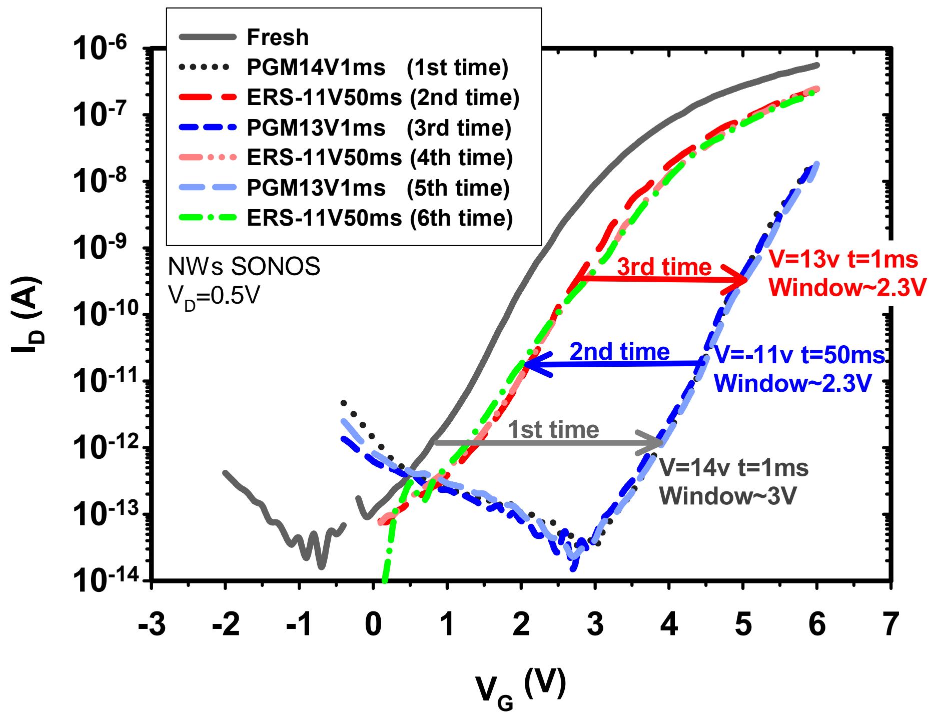


Fig. 4-12 I_D-V_G characteristics of programmed and erased states with different P/E specifications.

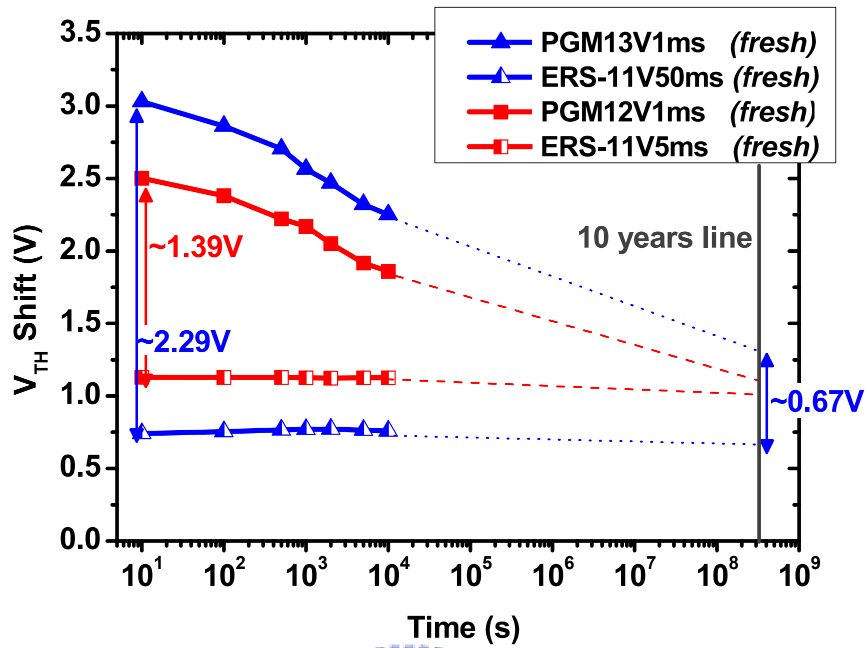


Fig. 4-13 Retention characteristics of NW SONOS-devices at room temperature.

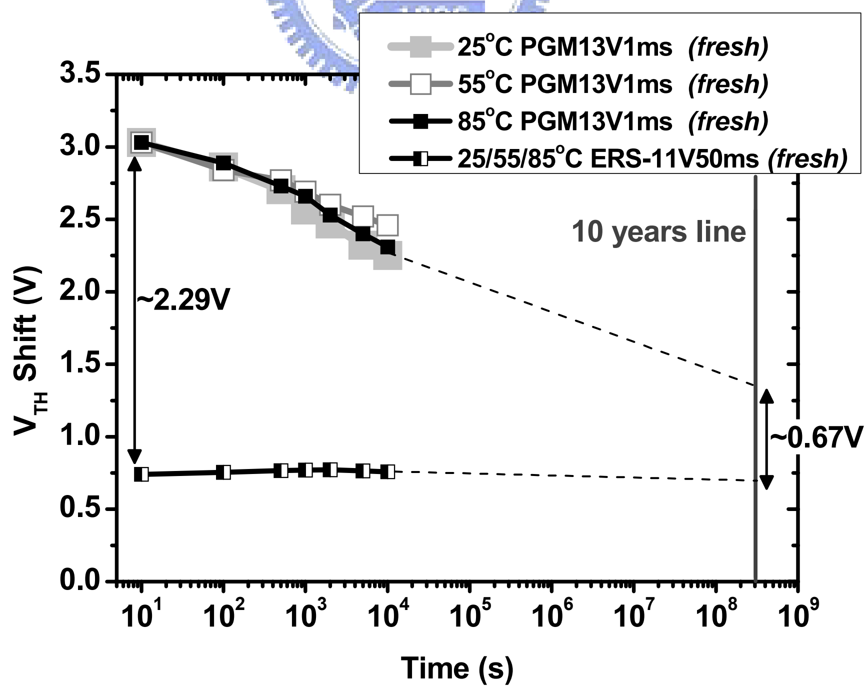


Fig. 4-14 Retention characteristics of NW SONOS-devices at different temperatures.

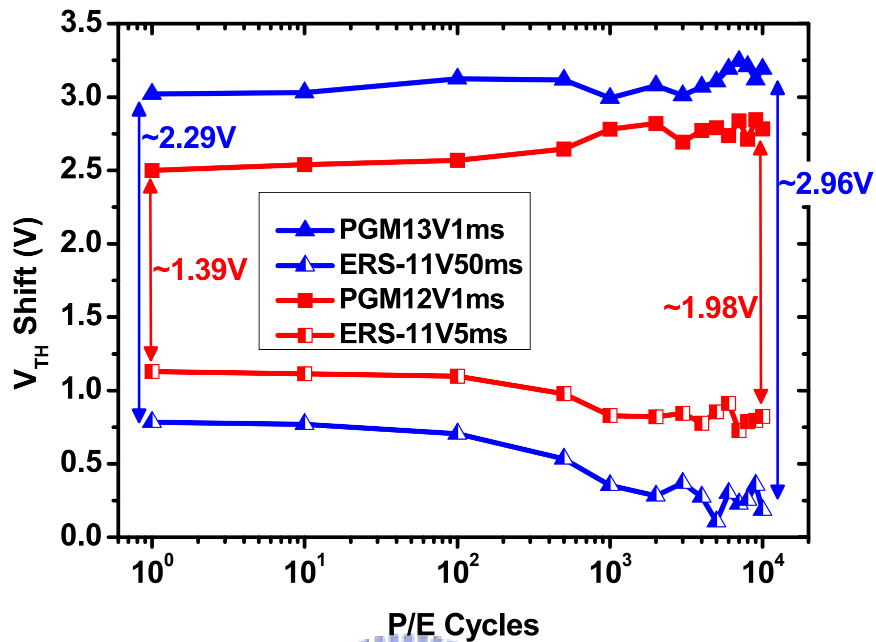


Fig. 4-15 Endurance characteristics of NW SONOS devices.

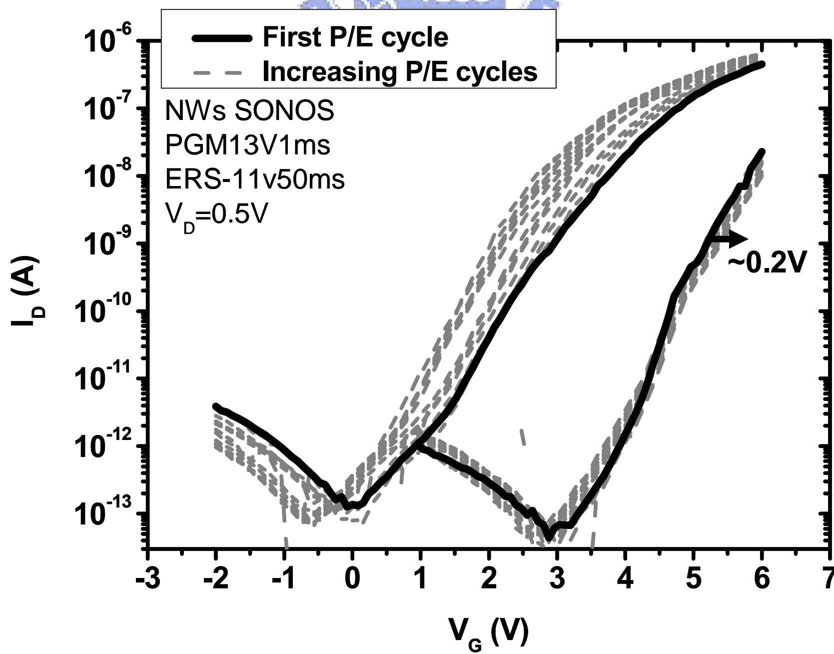


Fig. 4-16 I_D-V_G characteristics of the measured points in Fig. 4-15 with P/E specification of 13V1ms/-11V50ms.

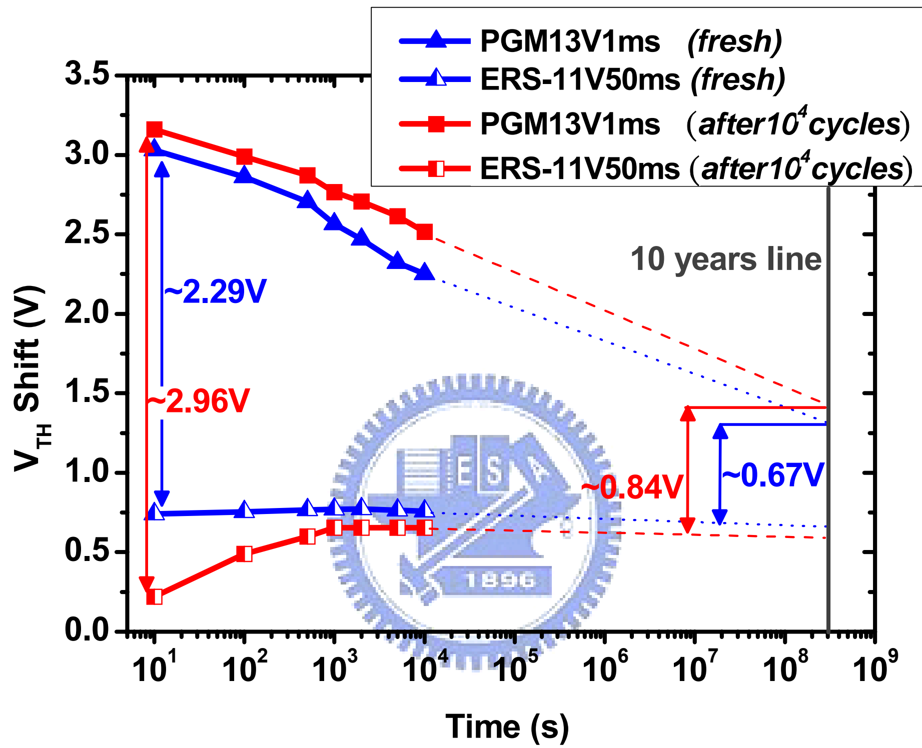


Fig. 4-17 Retention characteristics of NW SONOS-devices before and after stressing with P/E specification of 13V1ms/-11V50ms.

VITA

姓名:劉大偉

性別:男

生日:1984/03/23

籍貫:台灣省 彰化縣

住址:彰化縣溪州鄉舊眉村劉厝巷 26 號

電子郵件:**asdfghdavid@yahoo.com.tw**

求學歷程:	國立交通大學 電子研究所	2006/09~2008/06
	國立交通大學 材料科學與工程學系	2002/09~2006/09
	國立彰化高級中學	1999/09~2002/06
	彰化縣立溪州國民中學	1996/09~1999/06
	彰化縣立溪州國民小學	1990/09~1996/06

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Fabrication and Characterization of Novel Poly-Si Nanowire Devices

PUBLICATION LIST

- ✓ **<u>Ta-Wei Liu</u>**, Hsin-Hwei Hsu, Zerming Lin, Raymond Lin, Horng-Chih Lin, and Tiao-Yuan Huang, **"Multiple-Gated Poly-Si Nanowire Thin-Film Transistors,"** *SSDM, 2008.*

- ✓ Hsing-Hui Hsu, **<u>Ta-Wei Liu</u>**, Lin Chen, Raymond Lin, Tiao-Yuan Huang, **"Fabrication and Characterization of Multiple-Gated Poly-Si Nanowire Thin-Film Transistors and Impacts of Multiple-Gate Structures on Device Fluctuations,"** *IEEE Transactionss on Electron Devices, 2008.*

- ✓ **"Tri-Gated Poly-Si Nanowire SONOS Devices for Flat-Panel Applications,"** *IEDM, 2008.*