國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

修正蕭基位障電晶體之源極/汲極阻抗分析

Analysis of Source/Drain Resistance of Modified Schottky Barrier (MSB) FETs

研究生：劉筱函

指導教授：崔秉鉞 教授

中華民國九十七年七月

修正蕭基位障電晶體之源極/汲極阻抗分析

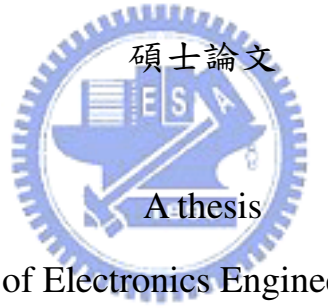
Analysis of Source/Drain Resistance of Modified Schottky Barrier (MSB) FETs

研究生： 劉筱函　　Student: Hsiao-Han Liu

指導教授：崔秉鉞　　Advisor: Bing-Yue Tsui

國立交通大學

電子工程學系 電子研究所



碩士論文

A thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical and Computer Engineering

National Chiao Tung University

in Partial Fulfillment of the Requirement

for the Degree of Master

in

Electronic Engineering

2008

Hsinchu, Taiwan, Republic of China

中華民國九十七年七月

修正蕭基位障電晶體之源極/汲極阻抗分析

研究生：劉筱函　　指導教授：崔秉鉞

國立交通大學電子工程系　電子研究所碩士班

摘要

隨著電晶體持續微縮至奈米等級，傳統式電晶體面臨許多挑戰，而蕭基位障電晶體具有較為優異的微縮表現，但蕭基位障電晶體受限於其蕭基位障而降低導通電流，修正蕭基位障電晶體可有效的改善其問題。本論文利用元件模擬軟體研究修正蕭基位障電晶體其參數對於元件特性之影響，並且對於源極/汲極阻抗進行最佳化之討論。

本論文利用元件模擬分析修正蕭基位障參數對於修正蕭基位障電晶體之影響。結果發現修正蕭基位障電晶體可分為兩類：一為偏向傳統電晶體之特性，另一為偏向蕭基位障電晶體之特性。偏向傳統電晶體特性之元件具有高濃度或較厚的修正蕭基位障區域，可有效的縮小源極端的蕭基位障之厚度進而增加電子穿隧機率，故元件特性由通道阻抗主導。另一偏向蕭基位障電晶體特性之元件具有較低濃度或較薄的修正蕭基位障區域，故當閘極電壓增加時，此區域容易被閘極電壓空乏而無法達到其作用，故其特性仍受限於源極端的蕭基位障。而當元件持續微縮之下，過厚的修正蕭基位障區域會造成等效元件通道降低的效應，反而造成較嚴重的短通道效應。故當元件微縮後，修正蕭基位障區域必須朝著高濃度薄厚度以達到較好的元件特性。另一所需考慮之特性為 DIBL（Drain induced barrier lowering），當修正蕭基位障區域濃度增加時，DIBL 現象也會隨之增加。對於通道長度為 32 nm 之元件，所得到最適當的條件為當修正蕭基位障區域之濃度為 $3\times10^{19}cm^{-3}$、厚度為 3 nm。

源極/汲極阻抗中，接觸阻抗佔了最重要的部份，利用修正蕭基位障區域提高接觸面之介面濃度，並改變不同的金屬矽化物厚度以增加接觸面積來達到降低阻抗之作用。對於偏向傳統電晶體之元件，其最佳化條件是約金屬矽化物佔矽晶層厚度一半；而偏向蕭基位障電晶體之元件，金屬矽化物愈薄其阻抗愈小，由於其側接面幾乎只有通道表面會有電子穿隧電流，故隨著金屬矽化物厚度增加並不會增加側面之穿隧電流。對於三閘極 (Tri-gate) 電晶體的接觸阻抗，包含兩種源極/汲極金屬矽化物接面：一為平面式，另一為包覆式接觸。平面式最佳化條件趨近於完全金屬矽化之源極/汲極結構，主要受到側面通道之影響。另一包覆式結構最佳化在鰭狀結構寬度為四分之一處。然而，導通電流與及次臨界擺幅的趨勢相同，故元件設計時，必須考慮兩者的權衡關係以得到最適當的元件特性。

本論文採用外部阻抗粹取串聯阻抗之方法（external loading method）於模擬與實際製作的 SOI 元件。結果發現，對於偏向傳統元件特性之元件可適用此方法，但對於偏向蕭基位障電晶體則無法適用。模擬元件所得到的外部阻抗為 160.01 Ω-μm 且其接觸阻抗約為 5.5×10^{-8} Ω-cm^2（可達到 ITRS 標準）。然而，在實際元件中，外部阻抗約為 1～3 kΩ-μm，接觸阻抗約為 6×10^{-7} Ω-cm^2, 相較於模擬結果約大了 10 倍，主要原因應為其修正蕭基位障區域之濃度並不如預期之高，但元件特性仍是呈現偏向於傳統電晶體之特性，推測為其修正蕭基位障區域之厚度約至 10 nm 所致。藉由實際元件與模擬元件之結果可相互比較以推測實際元件之修正蕭基位障區域參數，並且可藉此探討後續實驗之改善條件。

Analysis of Source/Drain Resistance of Modified Schottky Barrier (MSB) FETs

Student: Hsiao-han Liu Advisor: Bing-Yu Tsui

Department of Electronics Engineering

Institute of Electrons

National Chiao Tung University

Abstract

As CMOS device scaling to nanometer regime, the conventional device would meet many challenges to scaling. The Schottky barrier (SB) FET becomes one of the promising structures and has better scalability. However, the on-current of SB FETs is limited by the Schottky barrier at source side. The Modified-Schottky-Barrier (MSB) FETs have been proposed to improve the SB FETs performance. Therefore, the effects of the parameters of the MSB region on device performance and series resistance optimization were simulated by TCAD tools.

According to the simulation results, the MSB FETs can be classified into two groups. One is conventional-like devices, and the other one is SB-like devices. For the conventional-likes devices, the high doping concentration and thick thickness of the MSB region would thinner the Schottky barrier thickness at the source side and increase the tunneling current. Therefore, the total conductance is dominated by the gate field induced channel potential barrier lowering. In contrast, for the SB-like devices, the MSB region with lower doping concentration and thin thickness is easily depleted by gate bias. Therefore, the Schottky barrier resistance dominates the total conductance. However, as the device scaling down, the thick MSB thickness would

degrade the device performance due to the reduction of effective channel length. Thus, the MSB region with thinner thickness and high doping concentration is needed. On the other hand, the drain-induced-barrier-lowering (DIBL) has to be considered for short channel device. According to the simulation results, the DIBL increases as the MSB doping concentration increases. The optimized conditions for tri-gate MSB FETs with channel length = 32 nm are the MSB thickness = 3 nm and the MSB doping concentration = 3×10^{19} cm^{-3}.

The contact resistance is the major part in total resistance. The MSB FETs utilize the high doping concentration at the silicon and silcide interface to reduce the contact resistance. Various silicide thickness structures were used to increase the contact area and reduce the contact resistance. For the conventional-like devices, the optimized silicide thickness is about half of the silicon thickness. For the SB-like devices, the optimized value is about 10 nm due to the tunneling current is concentrated at the Si surface; therefore, the increase of silicide thickenss would not provide additional tunneling current. For tri-gate MSB FETs, the optimized value of planar contact is about 30~35 nm (nearly fully-silicided structure) due to the sidewall channel effect. The optimized value of wrapped contact is quarter of the fin width. However, the on-current and subthreshold swing shows the same silicide thickness dependence. The tradeoff between on-current and subthreshold swing has to be considered.

The external loading method was used to extract the series resistance of simulated and real devices. For the conventional-like device, this extraction method is suitable. But for the SB-like devices, this method can not be applied. The extracted series resistance from simulation devices is 160.01 Ω-μm and the specific contact resistivity is lower than 5.5×10^{-8} Ω-cm^2 (meet the requirement of ITRS roadmap). The extracted series resistance from contact resistance test structures is about 1~3 kΩ-μm and the specific contact resistivity is 6×10^{-7} Ω-cm^2. The contact resistivity of

real devices is one order higher than that of the simulatresulted device. The reason may be that the MSB doping concentration is not high enough as expected. The real devices still exhibits a very conventional-like property due to the thicker thickness. It is estimated to be about 10nm. The MSB region of the real devices can be conjectured by the comparison of simulation results and then to improve the process condition to optimize the device performance.

誌謝

兩年的研究生活很快的過去，隨著論文的完成也慢慢的感受出在這兩年中所學習的、所獲得的、以及所成長的經歷，在這兩年的學習中，受到了許多人的幫助才得以順利完成論文，在此僅以此文感謝。

首先感謝在這兩年中對我影響最大的指導教授-崔秉鉞老師，在老師身上，我深刻的體會到老師對於研究投入的熱情，在專業知識上的探究，對於追求真相的認真專注，讓我了解到對於知識所追尋的正確方向，並且老師在指導學生投入了相當大的心力，每每與老師討論過後，皆會有豁然開朗的念頭。不僅僅在專業知識上，老師的學術態度與為人處事也提供了我相當好的身教典範。

感謝實驗室的夥伴們，在實驗製程與讨論中提供我相當多過來人經驗的謝志民與盧季霈學長，常常為了我的實驗提供我許多可行的方案與想法。上一屆的振欽、振銘、玉仁學長，感謝你們帶領我學習交通大學奈米中心與國家奈米元件實驗室的機台與操作環境，也提供了許多你們自身實驗的情形與經驗，讓我可以更快速進入狀況，匀珮與旭茹學姐可以一起談女生話題並且互相加油打氣。同屆的孝瑜、曉萱、雨蓁更感謝有妳們的陪伴，讓我的碩士生活充滿歡樂與笑聲，女孩們之間的相互支持、照顧成為很大助力。正愷與嘉文在實驗上或生活上也有許多相互幫助的地方。另外，感謝依成學弟擔任實驗室負責人的角色，辛苦囉。很開心的在這樣的實驗室中度過，有著相互幫助的大家，謝謝你們！

還要感謝義璿學長與蘇彬實驗室的育昇學長、銘隆、昆諺，感謝你們在模體軟體中對於我的幫助，提供了我很多模擬上的解決方法讓我順利進行實驗。感謝我的大學同學與社團夥伴，雖然不常相聚，但總是知道你們的關心，也讓我在沮喪的時候可以得到妳們的加油鼓勵，支持著我繼續努力。

最後，感謝我最重要的家人，我的爺爺奶奶、外公外婆以及我的爸媽-劉日定與林貴美，感謝你們對於我的信賴與鼓勵，家永遠有著滿滿的愛使我充滿元氣，僅用此篇論文與你們一起分享這份喜悅。

Content

Table Captions

Chapter 3

Chapter 4

Figure Captions

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter1

Introduction

1-1 FinFETs

To achieve the benefits such as high performance, high device density, low operation voltage, and low cost, the dimensions of CMOS devices are continued to scale down for several decades. As devices scaling down, the short channel effect (SCE) becomes the major issue to influence device performance. There are several methods to alleviate SCE such as raising the substrate doping concentration, forming ultra-shallow source/drain junction, and reducing the gate dielectric thickness [1]. However, the SCE of conventional planar CMOS is still a significant limitation in the sub-45nm technology node. It is clearly claimed that new device structures and new materials will be needed to satisfy the device and circuit requirements [2]. Several non-classical structures such as ultra-thin body (UTB) silicon-on-insulator (SOI) MOSFETs [3-4], double-gate (DG) FETs [5], tri-gate FETs [6], Ω-gate FETs [7], and gate-all-around FETs [8] have been invented to increase the gate controllability and to suppress the SCE. On the other hand, high-dielectric constant (high-k) dielectrics have been employed to reduce effective oxide thickness (EOT) and gate leakage current [9-10]. Fig.1-1 presents these new device structures as the promising structures for device scaling.

Most of the non-classical structures use silicon-on-insulator (SOI) substrate to improve SCE. The bottom oxide layer (BOX) can also reduce the parasitic capacitance [11]. Using the thin-Si film results in reduction of drain-induced barrier lowering (DIBL), nearly ideal subthreshold swing, lower off-state leakage current, and higher driving current on short channel device. However, for the UTB SOI

MOSFETs, as the silicon layer thickness (t_{Si}) becomes less than the inversion-layer thickness of bulk MOSFETs, the device performance would be restricted because of quantum effects such as mobility degradation, threshold voltage increase, and inversion layer capacitance increase [12]. In addition, the channel length has to be three times larger than the t_{Si} in order to maintain fully depletion of the Si layer under gate control [13]. As the t_{Si} scaling down, the fabrication and the uniformity of ultra-thin SOI wafer would be challenges.

Multi-gate FETs (MuGFETs) have better gate-controllability than conventional planar MOSFETs. In this case the t_{Si} can be thicker than that of the UTB SOI MOSFETs at the same channel length. For DG FinFETs, the silicon body thickness would be scaled down to ~ $L_{eff}/2$ [14]. Fig.1-2 presents the required silicon body thickness versus gate length for different structure [7], [15]. Moreover, MuGFETs may have higher driving current, for example, tri-gate FETs have the top and sidewall gates to increase the effective channel width without increasing the layout area. Therefore, MuGFETs become the most potential structure beyond the 45nm technology node.

1-2 Modified-Schottky-Barrier MSB FETs

Although MuGFET is expected to be the most promising structure beyond 45nm technology node, some technical challenges such as source/drain shallow junction formation, reduction of source/drain and gate electrode resistance, and the source/drain lateral diffusion still exist [16]. Schottky-barrier (SB) MOSFETs have some advantages such as a superior scaling ability due to the abrupt source/drain junctions and low extrinsic parasitic resistance and process compatibility with current CMOS technology [17-18]. The Schottky barrier at source side can also improve the

drain induced barrier lowering (DIBL) and SCE [19]. In SB MOSFETs, the source/drain regions have been replaced by metal silicides typically. The on-current depends on the schottky-barrier height (SBH) at source-side. Therefore, silicides with low SBH were preffered such as PtSi for p-type MOSFETs and $ErSi_2$ or YbSi for n-type MOSFETs [20-22]. However, the complementary silicides for n-type and p-type MOSFETs suffers from the complex fabrication process. It has been reported that the SBH must below 0.1eV in order to compare with conventional MOSFETs [23]. In addition, the low SBH at drain side results in high off-state leakage current due to carrier tunneling [24]. Therefore, the on/off states for SB MOSFETs are both inferior to those for conventional MOSFETs.

In order to reduce the effective SBH, dopant-segregation (DS) technique [25-27] and implant-to-silicide (ITS) technique [28-29] have been proposed to form modified Schottky barrier (MSB) FETs. Using these methods, the silicon and silicide interface would have a dopant segregation layer which could lower the SBH effectively. It has been approved that the MSB not only reduce the effective SBH at source side but also reduce of the tunneling leakage current form drain side [30]. Therefore, MSB FETs have attracted more attention in recent years.

1-3 Parasitic resistance

As CMOS device scaleing down, channel resistance decreases as gate length reducing. Therefore, parasitic resistance becomes more considerable and even limits device performance. In 1986, K. K. Ng and W. T. Lynch reported that parasitic resistance includes contact resistance, source/drain sheet resistance, spreading resistance, and accumulation resistance; besides they calculated the relationship between device structure and parasitic resistance [31]. In 2002, S. D. Kim reported

that analysis of series resistance for CMOS scaling to nanometer regime [32]. Sheet resistance would reduce dramatically by using silicide technology at source/drain regions; therefore, it can be ignored. The overlap and contact resistance would dominate the total resistance as device scaling to nanometer, as shown in Fig.1-3. The overlap resistance includes the accumulation resistance and spreading resistance (at gate to source/drain overlap region). Fig.1-3 presents that the contribution of overlap resistance would be the same as gate length decreasing. However, the contribution of contact resistance would increase because of the contact area shrinking. Therefore, the contact resistance would the major part to total series resistance in deep submicron devices.

Beyond 45nm node, MuGFETs are the most promising structure to suppress SCE. MuGFETs use the sidewall to increase the effective channel width and to improve the gate-controllability. However, the shrinkage of channel width leads to a smaller contact area which will cause higher contact resistance. If the contact resistance is larger than channel resistance, the CMOS scaling down is meaningless. Therefore, how to reduce the parasitic resistance effectively is an important issue. The optimization of parasitic resistance for the UTB SOI MOSFETs has been proposed. It depended on the extension length and the doping profile of source/drain junction [33]. However, it is difficult to achieve the optimized doping profile with current CMOS technology.

Reducing barrier height and increasing contact area are direct and effective methods to decline contact resistance. Recently, elevated source/drain structure by selective epitaxial-growth has been proposed to reduce the series resistance by increasing the thickness of the source/drain region after spacer formation [34-35]; nevertheless, this method results in higher gate-source/drain capacitance and influences the signal delay time. On the other hand, recessed source/drain structure

have the same advantage of increasing source/drain thickness but without increasing gate-source/drain capacitance [36-37]. The recessed source/drain structure showed good SCE immunity than the raised source/drain, but the process is more complex and harder to scale down.

Mehmet C. Ozturk used SiGe source/drain junction by selective epitaxial-growth, the SiGe source/drain reduced the parasitic resistance dramatically due to the smaller bangap and higher solid solubility in SiGe [38-39]. Besides, SiGe source/drain also provided the channel stress to enhance the device performance [40]. It should be noted that NiSi/SiGe system has poor thermal stability, so the thermal process after Ni-silicidaiton should be careful.

The parasitic resistance issue also exists at MSB FETs. Hence, in this thesis, we focus on the parasitic resistance of tri-gate MSB FETs. The effect of Schottky barrier height, MSB thickness, MSB doping concentration as well as the source/drain contact structure on the parasitic resistance will be investigated.

1-4 Thesis Organization

In the first chapter of this thesis, we briefly review the challenges as device scaling such as SCE, parasitic resistance, and shallow junction. Accordingly, we choose MSB FETs as the research target to study the device performance by varying the parameters related to the parasitic resistance.

In chapter 2, the device structure parameters and physical models used in numerical simulation are shown clearly. The fabrication process of tri-gate MSB FETs and Quasi-Vertical Kelvin structure for MSB contact resistance measurement are described.

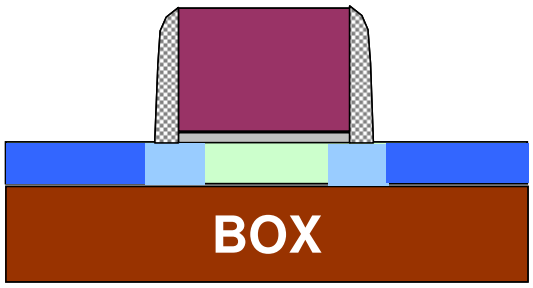
In chapter 3, we use the simulation tool of Sentaurus-TCAD to study the effect of

MSB junction on device performance [41]. In order to keep the benefits of SB FETs, the MSB junction can be not too conventional-like. Thus, the device optimized with respect to various parameters such as MSB thickness, MSB doping concentration, silicide thickness, silicide work-function, and source/drain contact structure.

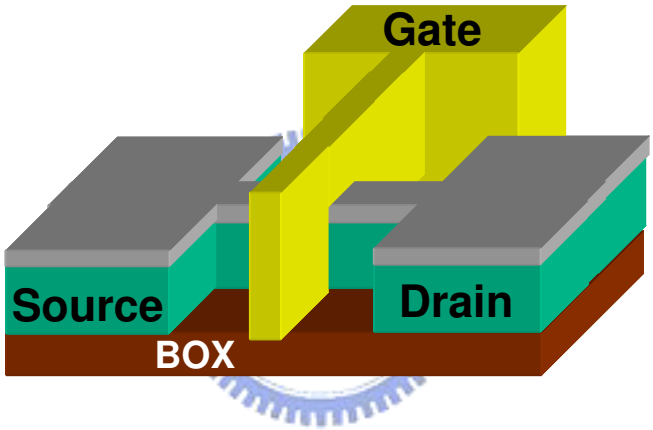
In chapter 4, the external loading method is used to extract the series resistance of MSB FETs [42]. The validity of this method is evaluated by numerical analysis at first. The MSB MOSFETs with different process conditions are then used to verify the numerical simulation performed in chapter 3.

Finally, in chapter 5, we summarize the importance observation and make conclusions of this thesis. Some future works worthy to study continuously are recommended.

(a)



(b)



(c)

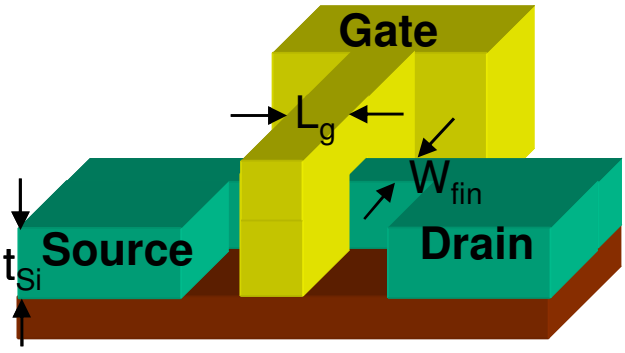
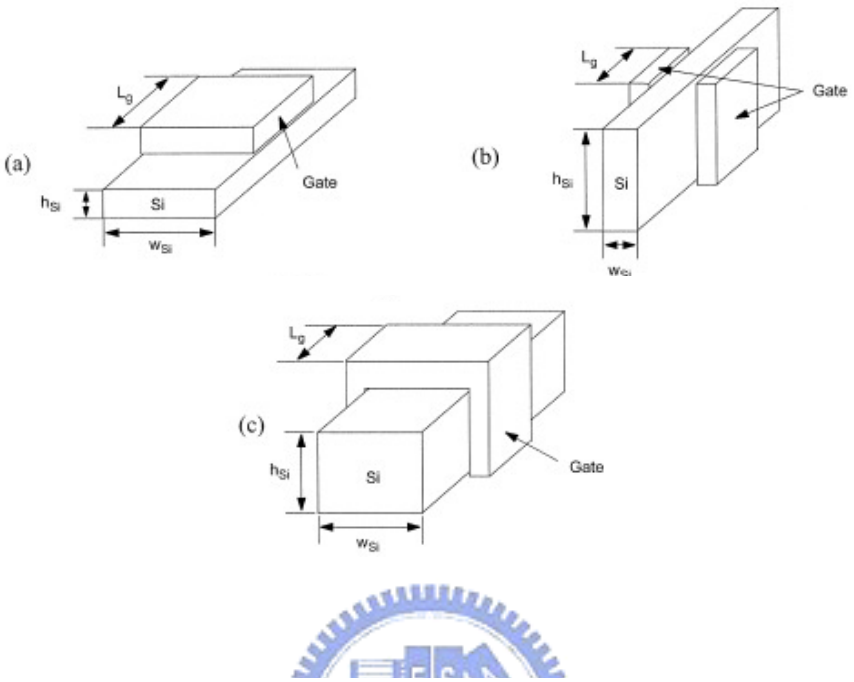


Fig.1-1 Schematic figures of (a) UTB SOI FETs, (b) DGFETs, and (c) Tri-gate FETs.



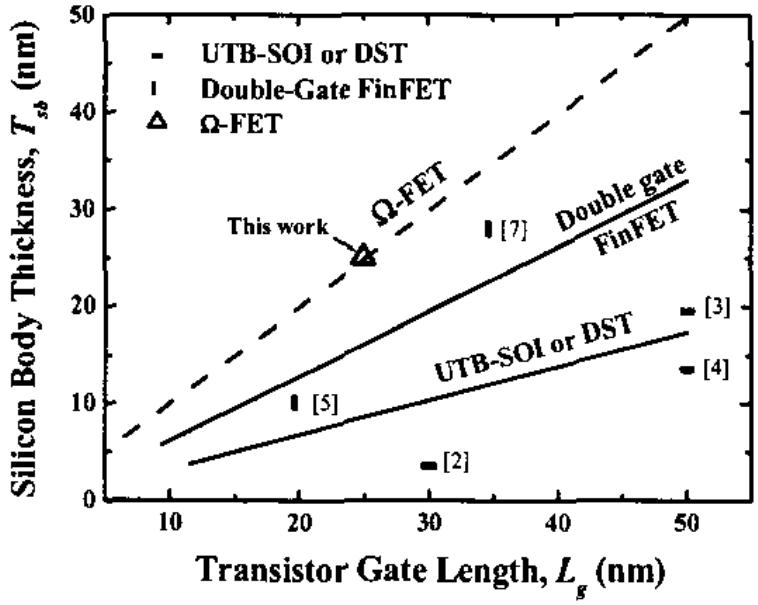
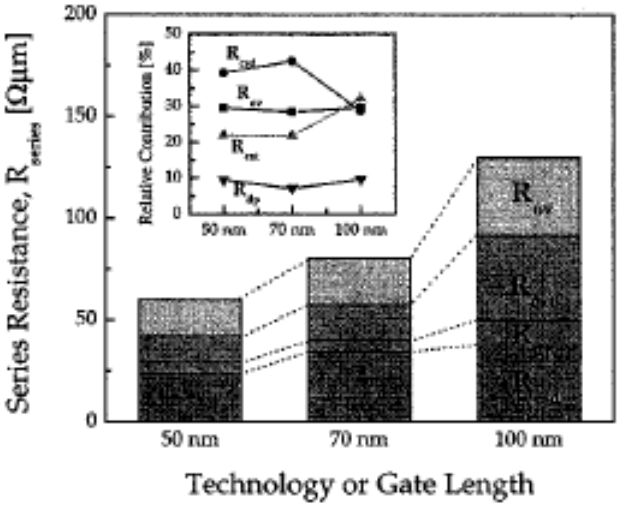


Fig.1-2 Silicon body thickness versus transistor gate length [7],[15].

(a)



(b)

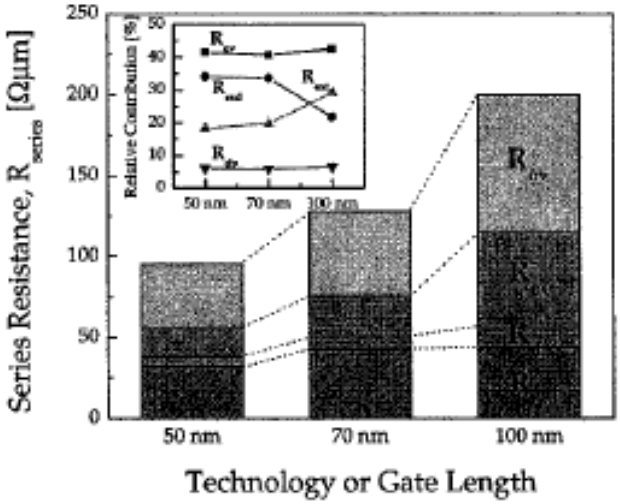


Fig.1-3 Series resistance components relation as the CMOS scaling [32]. (a) NMOS and (b) PMOS

Chapter 2

Experimental Procedure

2-1 Numerical Analysis on Modified-Schottky-Barrier (MSB) FETs

2-1-1 Device Structure

To study the effect of MSB junction on device performance, Sentaurus-TCAD tool was used to simulate. The device structure was defined by DEVISE. In this thesis, fully-depleted MSB-SOI FETs and Tri-gate MSB-SOI FETs were studied. For fully-depleted MSB-SOI FETs, 2-D structures were used, as shown in Fig.2-1. The fixed device parameters includes silicon thickness t_{si} = 50 nm, gate oxide thickness t_{ox} = 5 nm, channel length L_g = 0.35 μm, substrate doping concentration $N_{sub} = 10^{17}$ cm^{-3}. The variable device parameters are MSB doping concentration N_{MSB}, MSB thickness t_{MSB}, silicide work-function WF_M, and silicide thickness t_M. For tri-gate MSB-SOI FETs, 3-D structures were used, as shown in Fig.2-2. For tri-gate MSB structure, the device parameters are similar to those for the fully-depleted MSB-SOI FETs. In additional to those parameters, two kinds of contact schemes at source/drain region were studied to optimize the series resistance. One is the top contact, and the other one is the wrapped contact, as shown in Fig.2-3. The tri-gate MSB-SOI FETs device was also used to evaluate the scalability and device optimization.

2-1-2 Physical Model on Numerical Analysis

DESSIS in Sentaurus-TCAD is used for electrical simulation, and declares physical models and physical parameters. Bandgap narrowing model, recombination

model, quantum mechanics model, and mobility model are included [41]. The QCVanDort model was selected to consider the quantum effect of the inverted channel. For mobility model, three components were considered. The first one is "Doping Dependence," which means the mobility would degrade as doping concentration increasing. The second one is "High Field Saturation," which means the mobility would be saturated at high electrical field. The last one is "Enormal," which means the mobility would be affected by the vertical electrical field.

At silicide and silicon interface region, the nonlocal tunneling model was used. This model can be applied to contacts and interfaces [41]. In this thesis, silicide sheet resistance can be ignored because it contributes very low percentages of the total series resistance. Thus, silicide contacts were used to study the effect of silicide work-function on device performance. In this nonlocal tunneling model, tunneling current includes thermionic current over the Schottky barrier and tunneling current through the Schottky barrier. The tunneling current depends on gate voltage by modulating the tunneling width at source-side, as shown in Fig.2-4.

2-2 Device Fabrication

2-2-1 MSB FETs

Device fabrication started on boron-doped 6-inch SOI wafer with low doping concentration around 1×10^{15} cm^{-3}. The nominal Si layer and buried oxide layer thicknesses were 50 nm and 150 nm, respectively. The active regions (including S/D region and Si fins) were defined by i-line stepper lithography and plasma etching. A 5 nm thick SiO_2 was grown by thermal oxidation as the gate dielectric, and a 150 nm thick undoped poly-Si was deposited as the gate electrode. For p-FET, poly-Si gate was doped by BF_2^+ at 50 keV to a dose of 5×10^{15} cm^{-2} and dopant activation was

performed by rapid thermal anneal at 900 ℃ for 20 seconds. For n-FET, poly-Si gate was doped by P_{31}^{+} at 45 keV to the same dosage and dopant activation was performed by rapid thermal anneal at 1020 ℃ for 15 seconds. Once again, gate regions were defined by i-line stepper lithography and plasma etching as shown in Fig.2-5(a). After 800 ℃ gate re-oxidation, a 40nm thick nitride was deposited to form the spacer, as shown in Fig.2-5(b). In order to avoid the serious lateral growth of nickel silicide, 2-step Ni silicidation method was used [28]. After 30 nm thick Ni deposition by a dual E-gun system, Ni reacted with Si to form Ni-rich silicide at 300 ℃ for 45 min. The unreacted Ni can be selectively removed by H_2SO_4+H_2O_2 mixture. The 2nd step anneal at 600 ℃ transformed Ni-rich silicide to NiSi. After the self-aligned silicide formation process, the devices became Schottky-barrier FETs as shown in Fig.2-5(c). The MSB junction was formed using the implant-to-silicde (ITS) method, and the silicide region was doped by BF_2^{+} at 10 keV to a dose of 5×10^{15} cm^{-2} for p-type device and by P_{31}^{+} at 45 keV to the same dosage for n-type device. Finally, a psot-ITS annealing at 600℃ for 30 min was performed to let dopants pile-up at silicon and silicide interface to form the MSB junction.

2-2-2 Contact Resistance Test Structures

It has been reported that the MSB FETs with a high doping concentration region at the silicide and silicon interface can improve device performance significantly than that of SB FETs. But the actual doping concentration of this MSB layer can not be analyzed by secondary ion mass spectroscopy (SIMS). The contact resistivity of the silicide/silicon interface with MSB layer also can not be extracted by the conventional test structures. Therefore, two kinds of test structure were designed and fabricated to extract the contact resistivity.

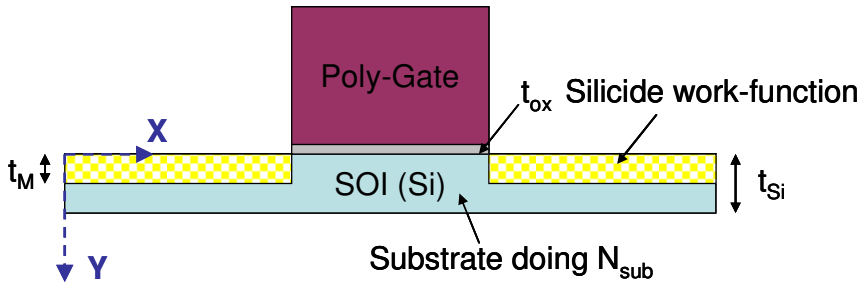
The first one is the multi-junction structure as shown in Fig.2-6. It can be

fabricated simultaneously with the MSB FETs. Silicon wires were defined during the definition of the active regions. The width and height of silicon wires are 0.4/0.5/0.8 μm and 40~50 nm, respectively. Then, p-type silicon wire was doped by BF_2^+ at 25 keV to a dose of 1×10^{13} cm^{-2} and n-type silicon wire was doped by P_{31}^+ at 15 keV to the same dosage. The dopant concentration of the doped Si wires is about $1x10^{18}$ cm^{-3}. The purpose of this doping process is to reduce the silicon sheet resistance. However, the doping concentration should not be too high to affect the MSB doping concentration. The poly-Si gate pattern was used to define the un-silicided silicon regions with various lengths. The nickel silicide regions were separated by the poly-Si gate pattern after Ni-salicide process. After ITS process, the 600℃/30 minutes annealing let dopants pile-up at the silicon and silicide interface to form the MSB junction. The total resistance of the test structure includes silicide resistance, silicon resistance, and silicide/silicon contact resistance. $R_{total} = R_{silicon} + 2 \times R_C$. The silicide sheet resistance can be ignored. By varying the length of the silicon regions, the total contact resistance can be extracted.

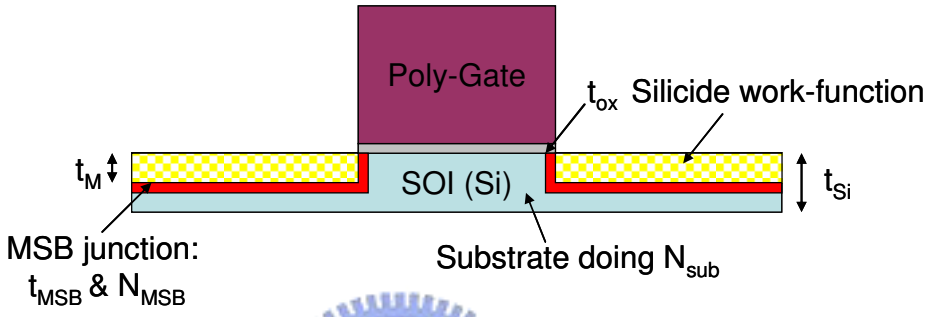
The second test structure is Quasi-vertical Kelvin structure and the layout is shown in Fig.2-7. The fabrication process is identical to that of the multi-junction structure. The structure parameters include silicon wire width **a** (0.4/0.5/0.8 μm), voltage sensing electrode width **b** and **c** (0.5 μm). The parameters **d** and **e** should be as small as possible and they depend on the process capability. They are 0.1μm in this thesis. The parameters of **f** and **g** are two times of **b** and **c,** respectively. Because of the SOI substrate, the current flow in this planar structure is identical to that of the Vertical Kelvin Structure developed in 1986 [43]. During measurement, the current flows from electrode I_1 to I_4 and measures the voltage different between electrode V_2 and V_3. As a result, the contact resistance can be derived by V_{23}/I_{14}. The parasitic error depends on parameters **d** and **e**. The **e** value should be 0 for ideal structure; however,

it is limited by the process error. In this test structure, **e** = 0.1μm and the error from n^- region resistance (the doping concentration of n^- region ~ 10^{18} cm^{-3}) is about 900Ω. In order to verify the real contact resistance, the n^- region resistance should be excluded.

(a)



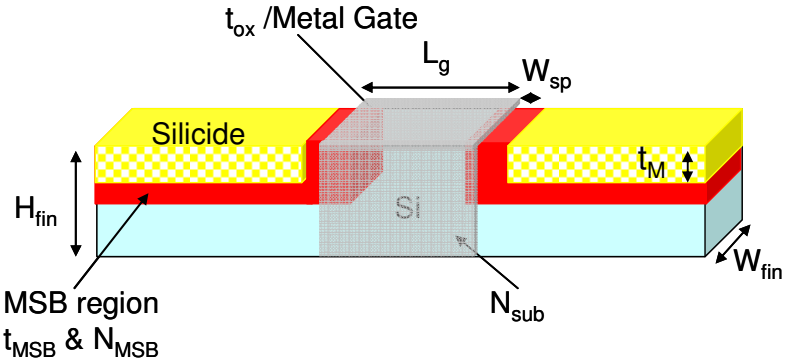
(b)



(c)

	n-MOS SB-SOI	n-MOS MSB-SOI
Gate length (μm)	0.35	0.35
S/D architecture	Shocttky barrier contact	with a n^+ region at Silicide/silicon interface
N_{Gate} (cm^{-3})	1×10^{20}	1×10^{20}
N_{sub} (cm^{-3})	1×10^{17}	1×10^{17}
N_{MSB} (cm^{-3})	-	$5\times 10^{18} \rightarrow 5\times 10^{19}$
t_{ox} (nm)	5	5
t_{Si} (nm)	50	50
t_M (nm)	0→ 50	0→ 50
t_{MSB} (nm)	-	1→ 5

Fig.2-1 (a) SB-SOI FETs (b) MSB-SOI FETs (c) Structural parameters of Fully-depleted device used in device simulation.



n-MOS tri-gate MSB FETs

Gate length (nm)	32
S/D architecture	with a n^+ region
N_{sub} (cm^{-3})	1×10^{15}
t_{ox} (nm)	1
H_{fin} (nm)	40
W_{fin} (nm)	20
Gate WF (eV)	4.4
t_M (nm)	10→40
t_{MSB} (nm)	2→5
N_{MSB} (nm)	$1\times 10^{19}\rightarrow 5\times 10^{19}$
W_{sp} (nm)	-5 →5

Fig.2-2 Structural parameters of Tri-gate MSB-SOI used in device simulation.

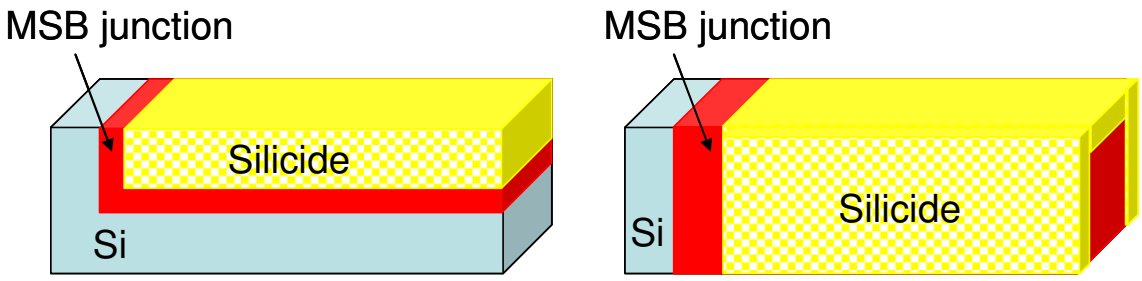


Fig.2-3 Two kinds of contact schemes: (a) planar contact (b) wrapped contact

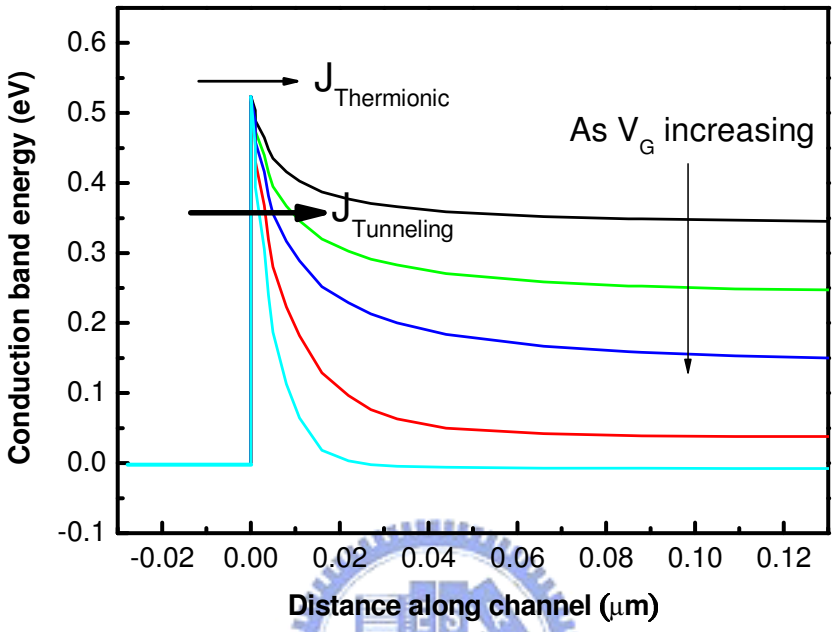


Fig.2-4 Conduction band energy at source-side with tunneling model as V_G increasing

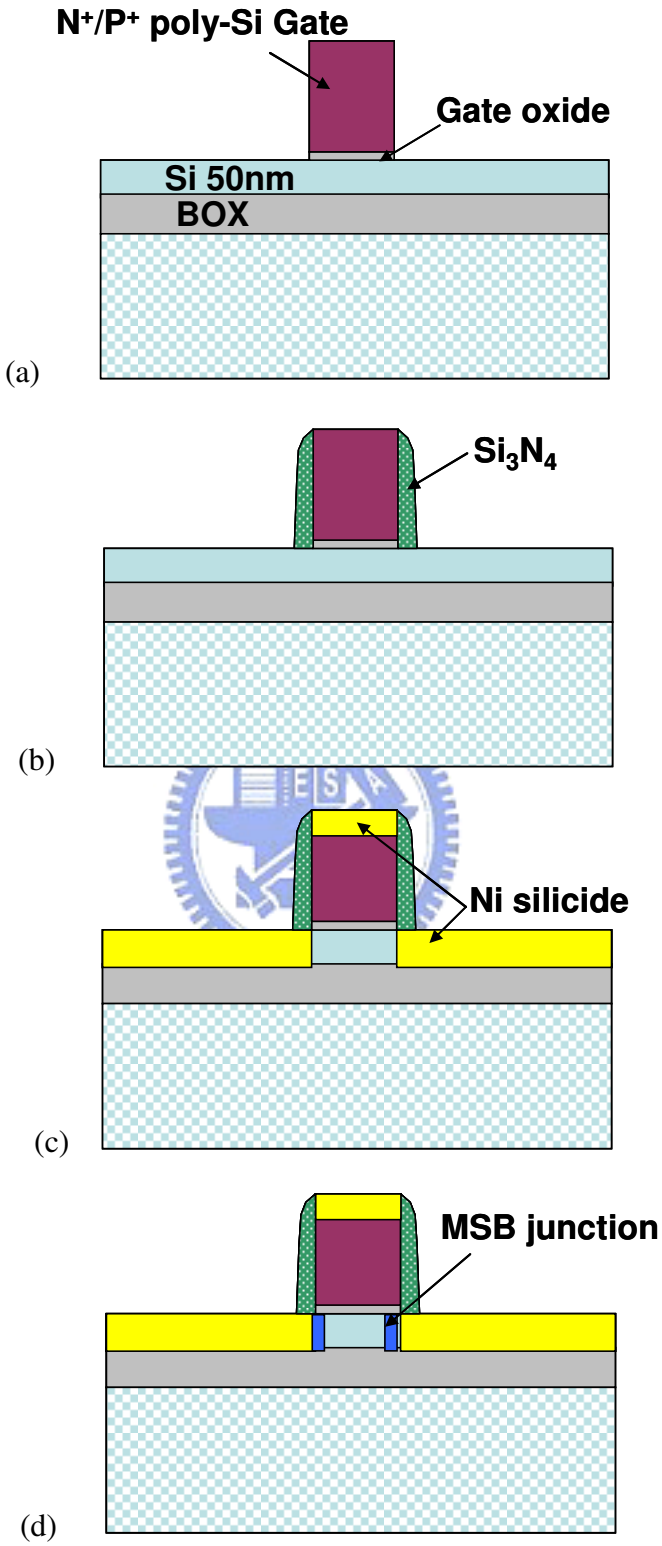


Fig.2-5 Main steps of fabrication process for MSB FETs.

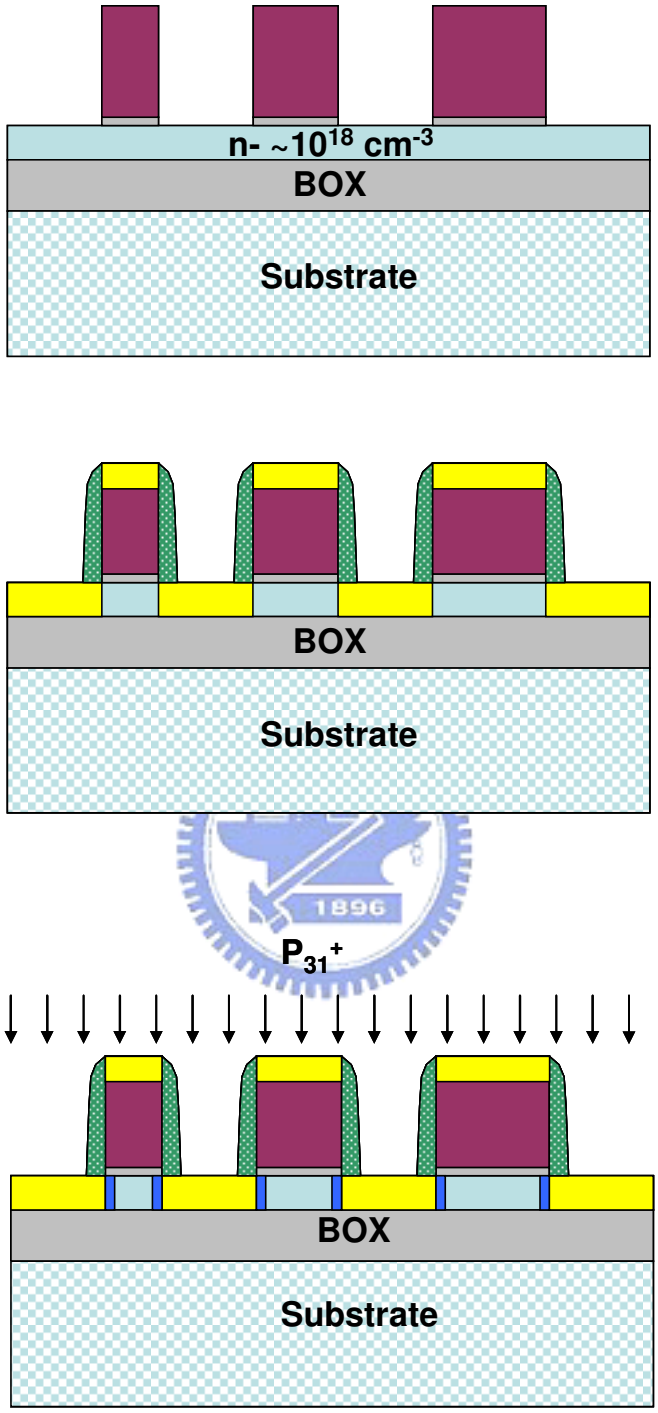
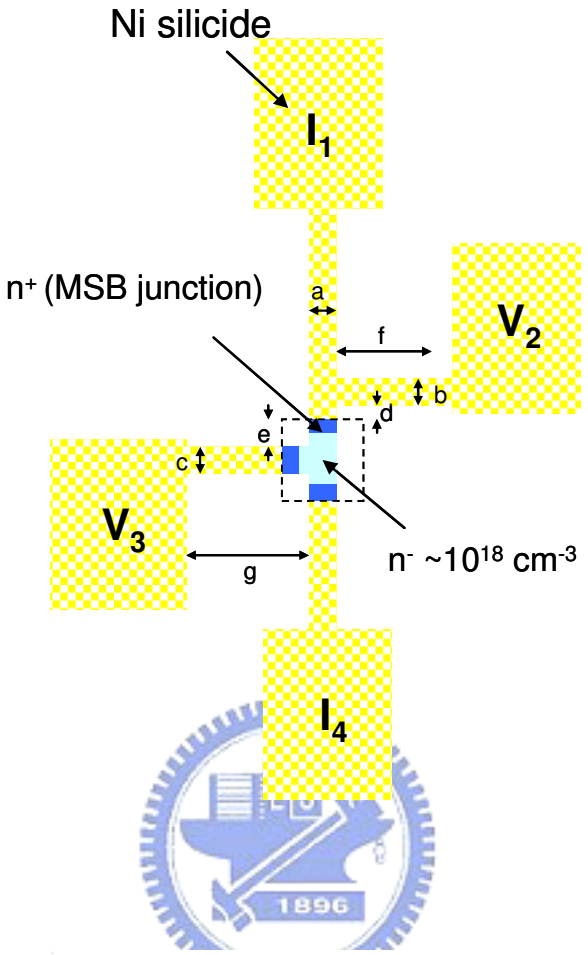


Fig.2-6 Main steps of fabrication process for Multi-junction series structure.

(a)



(b)

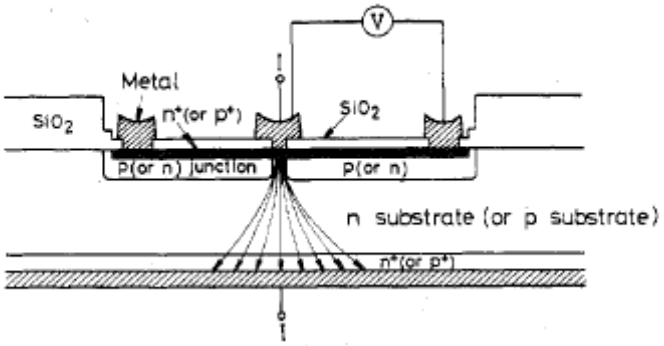


Fig.2-7 (a) The layout of Quasi-vertical Kelvin structure. (b) The cross-sectional view of vertical Kelvin test structure [43].

Chapter 3

Numerical Analysis on MSB (Modified-Schottky-Barrier) FETs

3-1 Introduction

As CMOS scaling, the conventional MOSFETs have many challenges to be overcome, such as short channel effect (SCE), drain-induced barrier lowering (DIBL), and abrupt ultra-shallow junction. Therefore, Schottky barrier (SB) FET becomes the promising device for better SCE and DIBL. The ideally abrupt source/drain junction is benefit for scaling down. The source side Schottky barrier dominates the device performance in SB-FETs. In order to enhance the on-current in SB FETs, The silicide materials with lower Schottky barrier height have been investigated. However, when the Schottky barrier is too low, the advantage of SCE and DIBL would vanish. In order to improve the SB-FETs performance, the Modified Schottky Barrier (MSB) FETs were proposed. As mentioned in chapter 1, the MSB FETs with n^+ region (for n-MOSFETs) results in the effective Schottky barrier lowering effect and improve the on-current. Also, the off-current can be reduced. Therefore, the MSB FETs have attracted more attention and become the promising structure for scaling. However, the parameters of the source/drain resistance clash with that of device performance generally. Therefore, in this thesis, we use the parameters including MSB doing concentration, MSB thickenss, silicide work-function, and silcide thickenss to obtain the effect on device characteristics and optimized the MSB region.

3-2 Fully-depleted MSB FETs

3-2-1 Effect of MSB doping concentration and MSB thickness

The SB and MSB FETs devices as shown in Fig.2-1 were used to simulate the effect of MSB doping concentration (N_{MSB}) and MSB thickness (t_{MSB}) on device performance. In these devices, the spacer length was defined to be 0 nm so that the device performance would be better than that with positive space length [44].

The transport mechanism of SB FETs includes the carriers transporting by thermionic emission and tunneling through the Schottky barrier. Therefore, the on-current is strongly dependent on the Schottky barrier at source-side. The on- and off-state band diagrams of SB FET are shown in Fig.3-1(a) and (b), respectively. In order to enhance the SB FETs performance, the silicide with low Schottky barrier such as $ErSi_2$ for n-type and PtSi for p-type have been proposed. In Fig.3-1(c), various silicide work-functions were simulated to understand the effect of barrier height. It is obtained that the on-current and subthreshold swing can be improved by decreasing the silicide work-function (decreasing the Schottky barrier for electron). Besides, the off-current can be suppressed by increasing the barrier for hole.

For MSB FETs, the on- and off-state band diagrams are shown in Fig. 3-2(a) and (b), respectively. This n^+ region would reduce the effective Schottky barrier height at source side at on-state and provide an effective barrier thickness at drain side to reduce the leakage current at off-state.

For the MSB FETs, this n^+ region influences the device characteristics critically. Thus, various values of N_{MSB} and t_{MSB} were defined to observe the MSB junction effects. Fig.3-3 presents the transfer characteristics of MSB FETs with t_{MSB} = 5 nm and varied N_{MSB}. The off-current could be reduced as the N_{MSB} increases. Fig.3-4 shows the simulated conduction band energy. At Vg = -1 V, the n^+ region would not be

depleted by gate voltage for higher N_{MSB}. Therefore, the n^+ region provides an effective barrier to hole and reduces the tunneling probability as is expected in Fig.3-2(b). In addition, the on-current is enhanced by increasing N_{MSB} due to the effective Schottky barrier lowering effect. Table3-1 shows the electrical characteristics of MSB FETs with various N_{MSB}.

For the MSB FETs, it has been observed that there are two slopes in subthreshold region when the N_{MSB} is low [45]. The simulation results confirm this as $N_{MSB} = 5\times 10^{18}$ or 1×10^{19} cm^{-3}. Fig.3-5(a) presents the transfer characteristics of the MSB FET with t_{MSB} = 5 nm and $N_{MSB} = 5\times 10^{18}$ cm^{-3}. The subthrehold swing (SS) shows two segments characteristic. At V_G = -0.2 V (SS is 67.8mV/dec), the conduction band diagram shown in Fig.3-5(b) indicates that after tunneling through the Schottky barrier, carriers encountered the channel potential barrier. In this case, the total conductance is dominated by the gate field induced channel potential barrier lowering. That is, the subthreshold characteristic follows the same thermal emission mechanism as the conventional MOSFET. On the other hand, at V_G = 0.2 V (SS is 238.5mV/dec), the conduction band diagram shown in Fig.3-5(c) indicates that the MSB region is depleted and the channel potential barrier is vanished by gate bias so that the Schottky barrier resistance dominates the total conductance. In this case, the SS is determined by the gate field induced effective Schottky barrier height lowering and a high value SS is observed.

When the MSB region has high doping concentration, for instance, Fig.3-6 shows the conduction band diagram of MSB FETs with $N_{MSB} = 5\times 10^{19}$ cm^{-3} and t_{MSB} = 5 nm, the MSB region would not be depleted even at gate bias equal to 1 V and the thermal emission across the channel potential barrier dominates the device performance. As a result, the MSB FETs with high MSB doping concentration exhibit the conventional-like characteristics.

Next, the effect of t_{MSB} on device performance was simulated. Fig. 3-7 presents the transfer characteristics of MSB FETs with N_{MSB} = 5× 10^{19} cm^{-3} and varied t_{MSB}. Even with high MSB doping concentration, the device performance becomes SB-like when the t_{MSB} is not thick enough. The MSB FETs with t_{MSB} = 1 nm does not have obvious improvement due to the MSB region is too thin and easily to be depleted. In contrast, MSB FET with thicker t_{MSB} = 5 nm and with N_{MSB} = 5× 10^{19} cm^{-3} presents conventional-like behavior. According to this discussion, the MSB FETs with thick t_{MSB} or high N_{MSB} would have conventional-like behavior. On the contrary, the behavior would become more SB-like with thin t_{MSB} and/or low N_{MSB}.

Fig. 3-8 presents the on/off current correlation of MSB FETs with various MSB parameters. It is observed that as the N_{MSB} or t_{MSB} increases, the SB-like characteristics would be suppressed. Choosing appropriate N_{MSB} and t_{MSB} can effectively suppress the off-current and enhance the on-current.

3-2-2 Effect of silicide thickness

In order to reduce the series resistance, various t_M at source/drain silicide region were simulated to identify the optimized source/drain structure. Fig.3-9 presents the on-current with various t_M. For devices with higher N_{MSB}, the optimized t_M is 20nm. The tunneling current and electrical potential are used to figure out the reason. Fig.3-10 presents the two-dimensional tunneling current distribution at source side with various t_M. As the t_M increasing, the tunneling current through sidewall interface increases. However, at the bottom interface, the tunneling current decreases as t_M increases. Fig.3-11(a) and (b) show electron-tunneling density through bottom and sidewall with various t_M, respectively. The total electron tunneling through the bottom and sidewall interface can be obtained by integrating the electron-tunneling density along the vertical-direction (y-direction) and lateral-direction (x-direction),

respectively. Table3-2 summarizes the integrated results with various t_M.

Fig.3-12(a) and (b) present the electron density at on-state with t_M= 10 and 40 nm, respectively. The electron density at channel region is concentrated at the Si surface, i.e. the inversion layer. The thickness of inversion is around 10nm [46]. If electrons tunnel through bottom side, they must flow along the sidewall MSB region at first to enter the channel region. The equivalent circuit is shown in Fig.3-11(c). According to this equivalent circuit, the series resistance along the thin sidewall MSB region increases as the t_M increases so that the bottom current decreases. It should be noted that as the t_M exceeds the inversion layer thickness, the electrons tunnel through the low part of the sidewall interface also have to flow along the thin MSB region. The current density decreases rapidly as the t_M increases. Due to the increase and decrease of sidewall current component and bottom current component, the optimum t_M value occurs at 20nm.

However, for devices with lower N_{MSB}, the trend of on-current with various t_M is totally different. The on-current decreases as t_M increasing. Fig.3-13(a) presents the tunneling current at sidewall. It is observed that the tunneling current is concentrated at the surface 10 nm. The effective contact area at sidewall does not increase as t_M increases. Besides, the tunneling current at sidewall is similar with the distribution of carriers at channel [46]. The electron-tunneling density at sidewall is exponential decay along the vertical-direction. Also, the distribution of carriers in inversion layer is also an exponential function of depth as shown in the insert in Fig.3-13(a). Since SB-like behavior dominates the low N_{MSB} device; electrons are hard to tunnel into the depletion region of the channel region. Therefore, increasing t_M does not increase sidewall current component. For t_M=10 nm, the electron-tunneling density shows a hump at about 10 nm depth due to the corner enhanced electrical field. Fig.3-13(b) presents the electron-tunneling density at bottom interface. The decrease of bottom

current as t_M increase is explained by the series resistance between the bottom interface and the inversion layer. In addition, for t_M = 10 nm, the electron-tunneling density at bottom interface is extremely higher than that with various t_M due to the corner induced electrical felid effect.

3-2-3 Effect of silicide work-function

In previous sections, the silicide material is assumed to be NiSi and has a work-function (WF_M) of 4.6eV. Nickel silicide can be applied to n-FETs and p-FETs and can reduce the complexity during fabrication. However, as the device scaling, the contact resistance must meet the ITRS roadmap and then dual silicide technique may be unavoidable. Hence, in this section, WF_M is varied to evaluate its effect on device performance.

Fig.3-14(a) and (b) present the transfer characteristics with various WF_M. For the devices of t_{MSB} = 1 nm, the effect of WF_M is notable. As the WF_M decreasing, the transfer characteristics become more conventional-like. However, for the devices with t_{MSB} = 3 nm, the transfer characteristic is very conventional-like behavior even if the WF_M equals to 4.6 eV. Decreasing the WF_M has little improvement on device performance.

Fig.3-15 compares the on-current versus t_M with various WF_M. The t_{MSB} is 3nm. With low WF_M, the MSB device performance becomes conventional-like. Therefore, the on-current trend is the same as that shown in section 3-2-2.

In summary, MSB region and WF_M affect the device performance. These MSB devices can be classified into two groups. One is conventional-like devices as the MSB region has thick t_{MSB} or high N_{MSB} or the WF_M is low enough for electron. For the conventional-like devices, the optimized silicide thickness is t_M = 20nm. The other group is SB-like devices, the drain current would degrade as t_M increases due to the

sidewall contact area can not provide an effective current path.

3-3 Tri-gate MSB FETs

In this section, tri-gate MSB FETs were simulated. The device parameters are similar to those used in section 3-2. For the tri-gate MSB FETs, the gate length is equal to 32 nm. Short channel effect and 3D effect are simulated especially.

3-3-1 Effect of MSB thickness and MSB concentration

First, the effects of N_{MSB} and t_{MSB} on device performance were simulated. Fig.3-16 presents the transfer characteristics of devices with t_{MSB} = 3 nm and various N_{MSB}. As the N_{MSB} increases, the on-current increases and the off-state leakage current decreases because the effective Schottky barrier thickness at source side is reduced by the MSB region. The subthreshold swing almost does not change with N_{MSB}. It is noted that the threshold voltage decreases 0.2V as the N_{MSB} increases from 1×10^{19} cm^{-3} to 5×10^{19} cm^{-3} because of the short channel effect. The doping concentration of Si layer is only 1×10^{15} cm^{-3}. Increasing the N_{MSB} will increase the depletion width of the source/drain junction. Therefore, the channel is easier to reach the fully-depletion condition and the threshold voltage is reduced.

Fig.3-17 presents the transfer characteristics of devices with $N_{MSB} = 5\times10^{19}$ cm^{-3} and various t_{MSB}. The subthreshold swing increases as the t_{MSB} increases because of the reduction of effective channel length. In these devices, the gate length is fixed at 32 nm so that the increase of t_{MSB} will decrease the effective channel length and then affect the device performance obviously. Therefore, in order to maintain the device performance, the MSB region with thick t_{MSB} is not suitable for short channel devices.

As we know, the conventional device has a serious problem with

drain-induced-barrier-lowering (DIBL) as device scaling. For SB FETs, the potential barrier at source side will be pinned by the Schottky barrier so that better DIBL performance is expected. Therefore, SB FETs would have better scalability than conventional device. For MSB FETs, the DIBL effect may be degraded. Fig.3-18 shows that the DIBL increases as N_{MSB} increases. The DIBL is 66.7 and 166.7 mV/V as N_{MSB} equals to 1×10^{19} and 5×10^{19} cm^{-3}, respectively. When the N_{MSB} is too high, the device becomes very conventional-like and the benefit of better DIBL performance disappears. Thus, the trade-off between on-current and DIBL limits the device performance. Fig.3-18(b) presents the DIBL versus on-current for MSB FETs and conventional device. The optimized condition is at $N_{MSB} = 3\times10^{19}$ cm^{-3} and the DIBL is 100 mV/V. The conventional device parameters are shown in Fig.3-18(c). It is obtained that the DIBL can be improved extremely by the MSB FETs than conventional device.

Fig.3-19 presents the effect of WF_M on device performance. The result is similar to that shown in Fig.3-14. The transfer characteristic is very conventional-like behavior as the WF_M equals to 4.6 eV with high N_{MSB} and thick t_{MSB}. Decreasing the WF_M just slightly increase the on-current. The subthreshold swing is not changed by WF_M because the subthreshold conduction is dominated by the thermal emission across the channel potential barrier.

According to the above discussions, higher N_{MSB} and lower WF_M improve the on/off state performance. However, the suppression of Schottky barrier property leads to the DIBL problem.

3-3-2 Effect of Contact Scheme

In this section, two source/drain contact schemes were evaluated. One is planar contact and the other one is wrapped contact. Fig.3-20 presents the on-current and

subthreshold swing as a function of t_M. For the planar contact, the optimized t_M is around 30-35nm, i.e. nearly fully silicided (FUSI) source/drain structure, as shown in Fig.3-20(a). This result is different from that in the top-gate MSB FETs. For the tri-gate device, there are top and two sidewall channels; therefore, the tunneling current from the lower part of the sidewall interface can flow into the sidewall channels instead of flowing through the thin MSB layer and then to the top channel. Therefore, the on-current increases as t_M increasing. The subthrshold swing slightly increases as t_M increases because of stronger drain coupling effect. For t_{MSB} = 5 nm and nearly FUSI source/drain structure, the subthrshold swing would be over than 100 mV/dec, which can not meet the ITRS roadmap).

The wrapped contact scheme provides larger contact area than planar contact scheme. Fig.3-20(b) presents the on-current and subthreshold swing as a function of t_M. The optimized t_M is about quarter of the fin width. The fin width is 20 nm in this simulation. For wrapped contact scheme, the tunneling current from the sidewall contacts can flow into sidewall channels directly. Since the inversion layer thickness is about 10 nm, the on-current increases with the increase of t_M until the t_M+t_{MSB} close to the inversion layer thickness. However, when the t_M+t_{MSB} exceeds to half of the fin width, the MSB region would shrink and the MSB resistance increases to degrade the on-current. The subthreshold swing shows the same t_M dependence with that of the on-current. Therefore, the trade-off between on-current and subthreshold swing must be considered.

3-3-3 Overlap/Underlap

In this section, the spacer width (W_{sp}) was changed to study the effect of underlap and overlap of gate to source/drain silicide. For SB FETs, the gate and source/drain overlap is needed to avoid unexpected potential barrier between silicide

and inverted channel. For MSB FETs, this problem is also existed. Therefore, for the device with the largest underlap of 5nm, the MSB region is just at the gate edge to avoid this issue. Fig.3-21 presents the transfer characteristics of the devices with various W_{sp}. For overlap devices (W_{sp} are negative), the subthreshold swing degrades greatly due to the reduction of effective channel length. It is clear that the silicide lateral growth is an importance parameter for short channel devices. If the silicide lateral growth is too much, the reduction of effective channel length degrades the device performance. In contrast, if the silicide lateral growth is too short, the high sheet resistance issue also degrades the device performance.

The results shown in Fig.3-21 were simulated at the fixed physical gate lenth so that the effective channel length defined as the distance between the two MSB edges changes with W_{sp}. In order to exclude the effect of change of effective channel length, Fig.3-22 shows the transfer characteristics simulated at fixed effective channel length. That is, the physical gate length was adjusted with the W_{sp}. The on-current and the subthreshold swing increase slightly as the overlap thickness increases. With overlap, an accumulation layer will be formed at MSB surface by gate field to reduce the series resistance of MSB region. The Schottky barrier thickness can also be modulated by the gate field to reduce the carrier injection resistance. Both effects improve the on-current. However, increasing the overlap, channel potential would be affected by drain potential so that the subthreshold swing degrades. At off-state, the underlap device presents better performance than overlap devices. The reason is that the gate field suppresses the drain-side Schottky barrier thickness to increase the leakage current for overlap devices. On the other hand, for the underlap devices, the Schottky barrier is out of gate electrode and is not affected by gate bias.

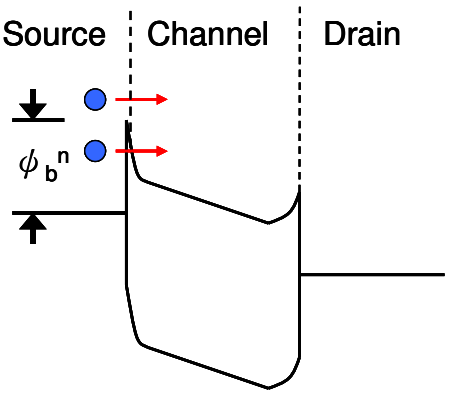
Table3-1 The electrical characteristics of MSB FETs with t_{MSB} = 5nm and varied N_{MSB}.

N_{MSB}	I_{on} (μA) @Vg =2V	I_{off} (A) @Vg = -1V	V_{th} (V)	S.S.(mV/dec)
$5\times10^{18}(cm^{-3})$	11.72	2.99×10^{-11}	0.343	67.8
$1\times10^{19}(cm^{-3})$	16.75	4.07×10^{-12}	0.112	63.0
$5\times10^{19}(cm^{-3})$	62.8	1.23×10^{-15}	-0.04	61.9

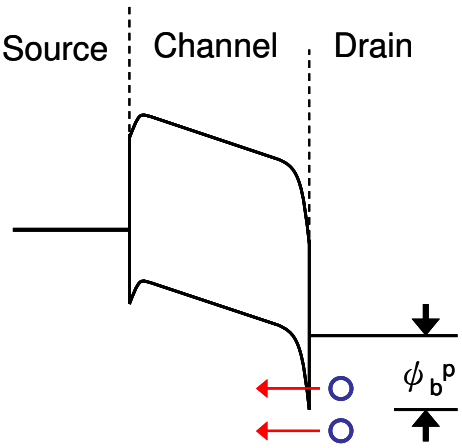
Table3-2 The tunneling current by integration at bottom and sidewall from Fig.3-12(a) and (b).

t_M (nm)	10	20	30	40
Bottom Integrate	6.99×10^{28}	4.89×10^{28}	3.23×10^{28}	2.34×10^{28}
Sidewall Integrate	9.57×10^{28}	1.47×10^{29}	1.18×10^{29}	1.26×10^{29}
Total	**1.626×10^{29}**	**1.959×10^{29}**	**1.503×10^{29}**	**1.494×10^{29}**

(a)



(b)



(c)

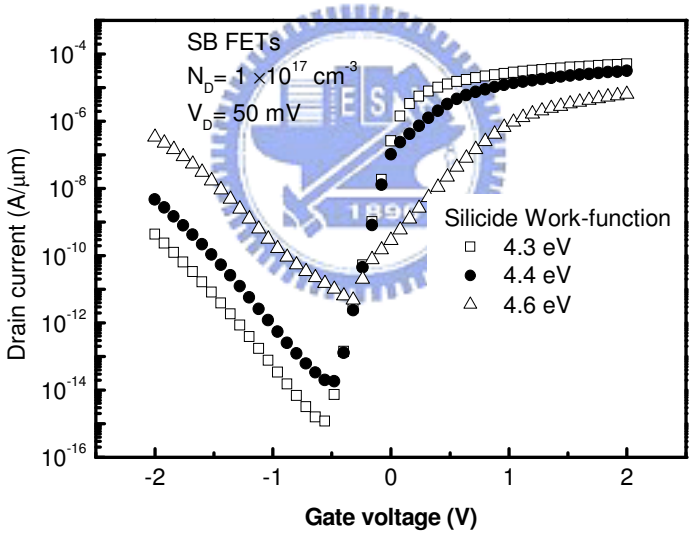
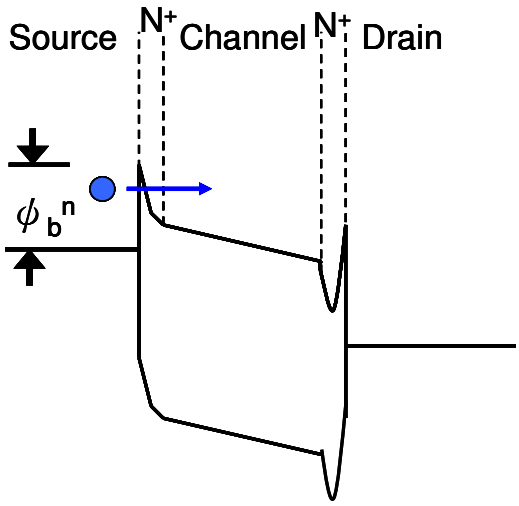


Fig.3-1 (a) and (b) are the on- and off-state band diagrams for SB FETs. (c) The transfer characteristics of SB FETs with various silicide work-function.

(a)



(b)

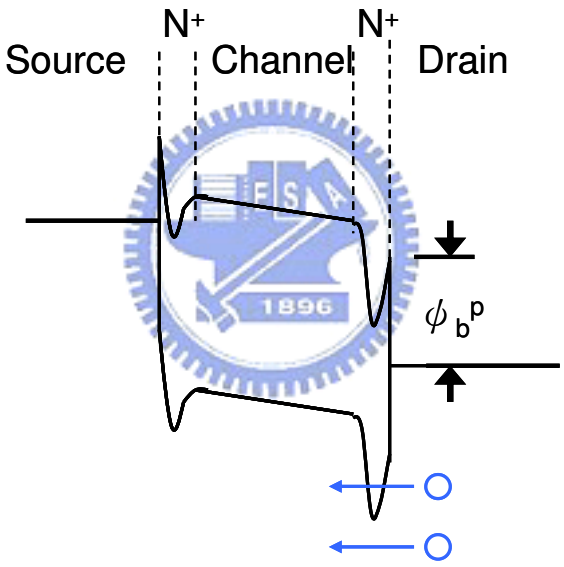


Fig.3-2 (a) and (b) the on- and off-state band diagrams for MSB FETs.

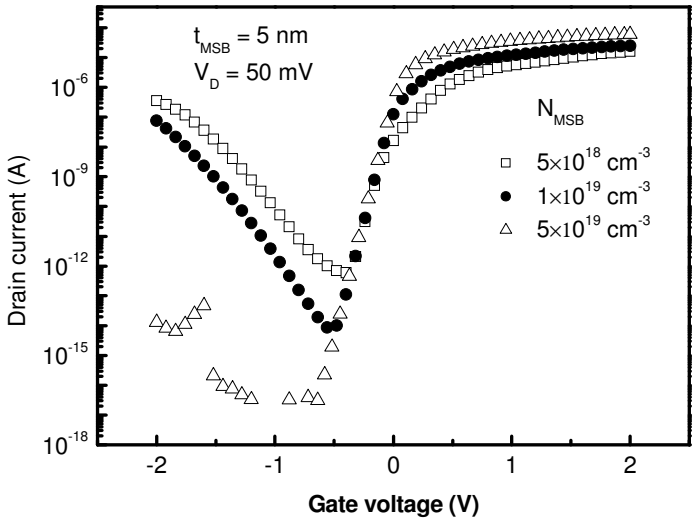


Fig.3-3 The transfer characteristics of MSB FETs with t_{MSB} = 5nm and varied N_{MSB}.

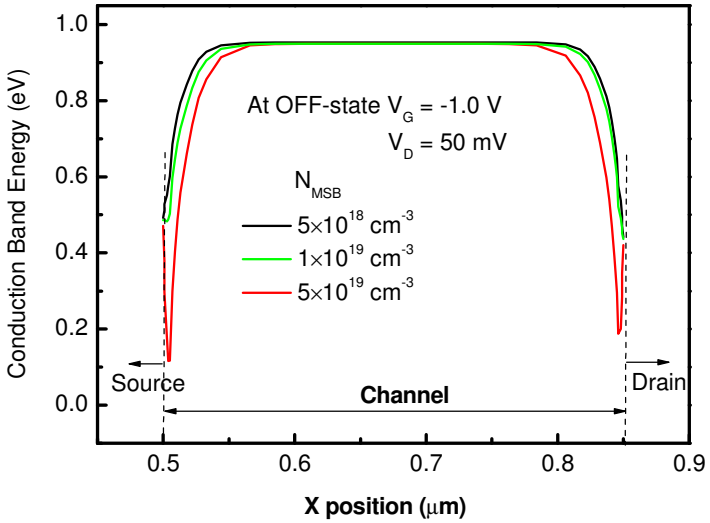
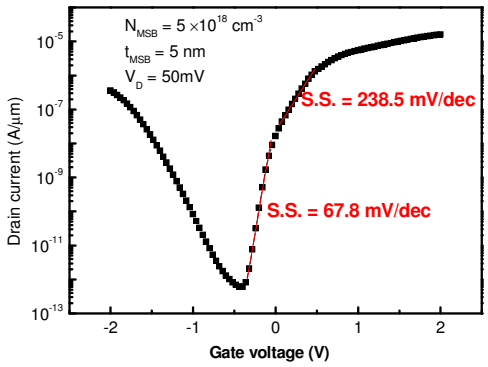
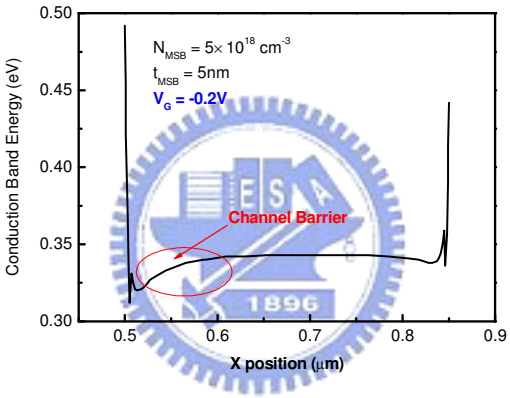


Fig.3-4 The conduction band energy at off state of MSB FETs with t_{MSB} = 5nm and varied N_{MSB}.

(a)



(b)



(c)

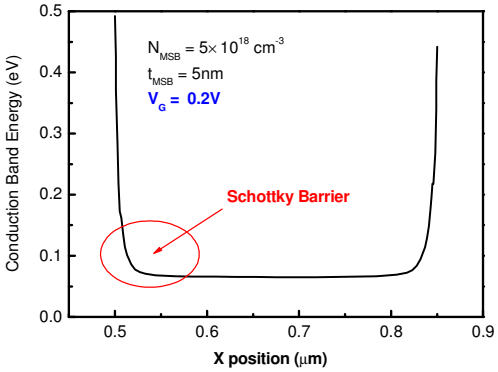


Fig.3-5 (a) The transfer characteristics of MSB FETs with t_{MSB} = 5nm and N_{MSB} = 5× 10^{18} cm^{-3} (b) The conduction band diagram at V_G = -0.2 V (c) The conduction band diagram at V_G = 0.2 V.

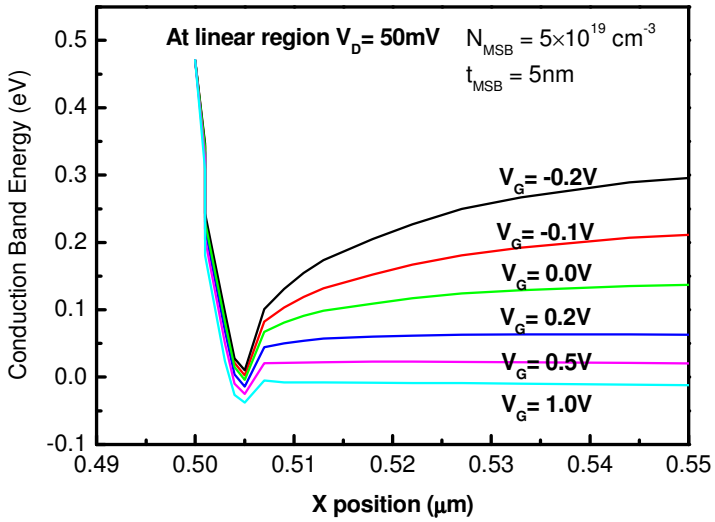


Fig.3-6 The conduction band energy of MSB FETs with t_{MSB} = 5nm and N_{MSB} = 5×10^{19} cm^{-3}.

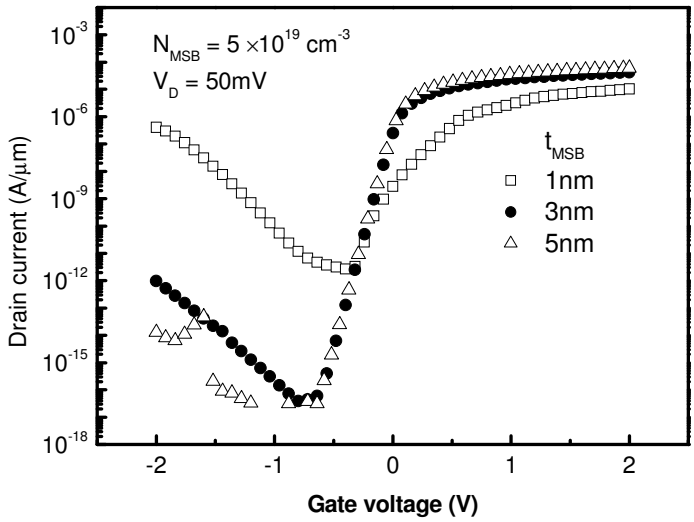


Fig.3-7 The transfer characteristics of MSB FETs with N_{MSB} = 5×10^{19} cm^{-3} and various t_{MSB}.

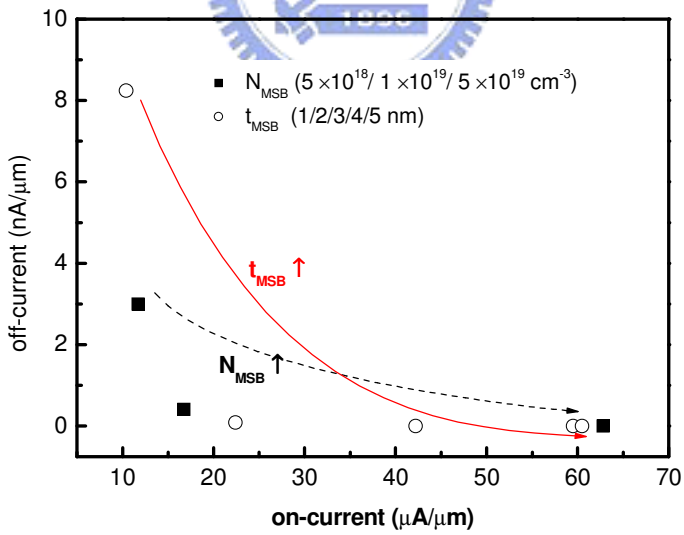


Fig.3-8 The on/off current relation of MSB FETs with various t_{MSB} and N_{MSB}.

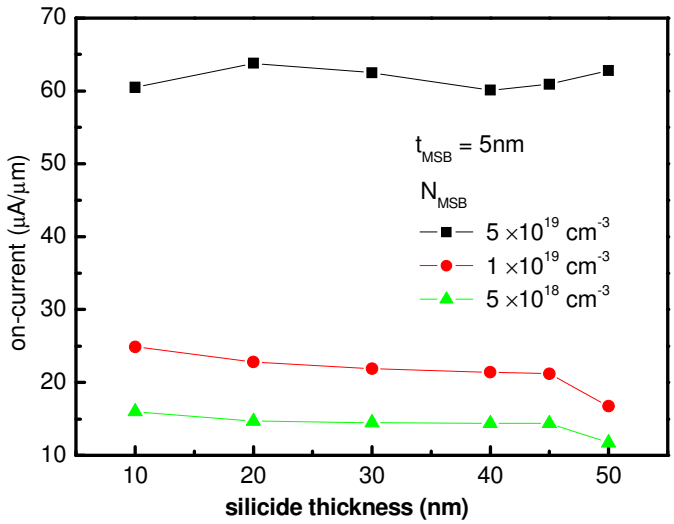


Fig.3-9 The on-current versus silicide thickness (t_M) with various N_{MSB} devices.

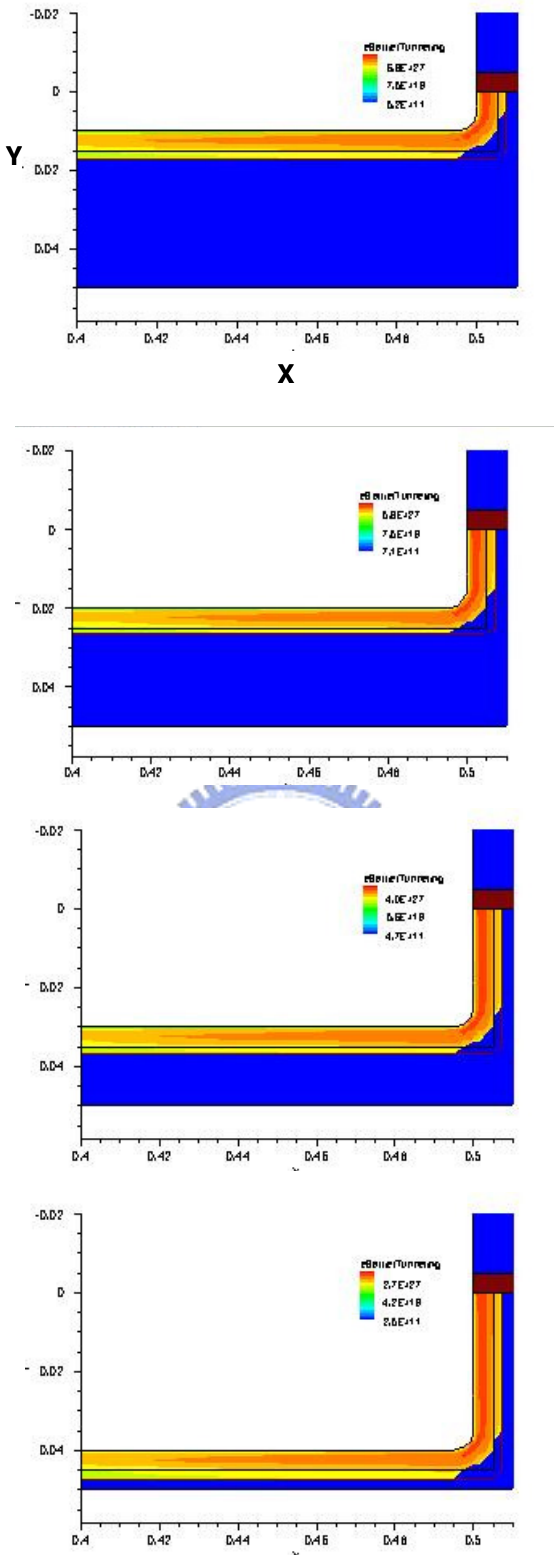
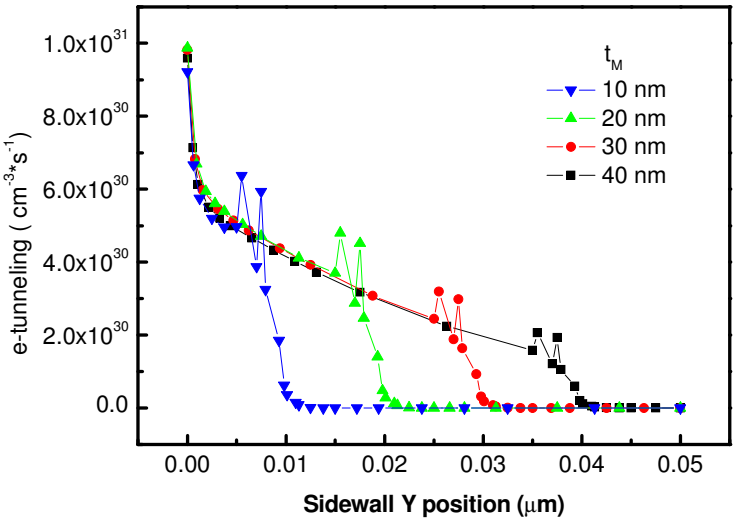


Fig.3-10 The two-dimensional tunneling current at source side with t_{MSB} = 5 nm, $N_{MSB} = 5\times 10^{19}\ cm^{-3}$ and t_M = 10/20/30/40 nm.

(a)



(b)

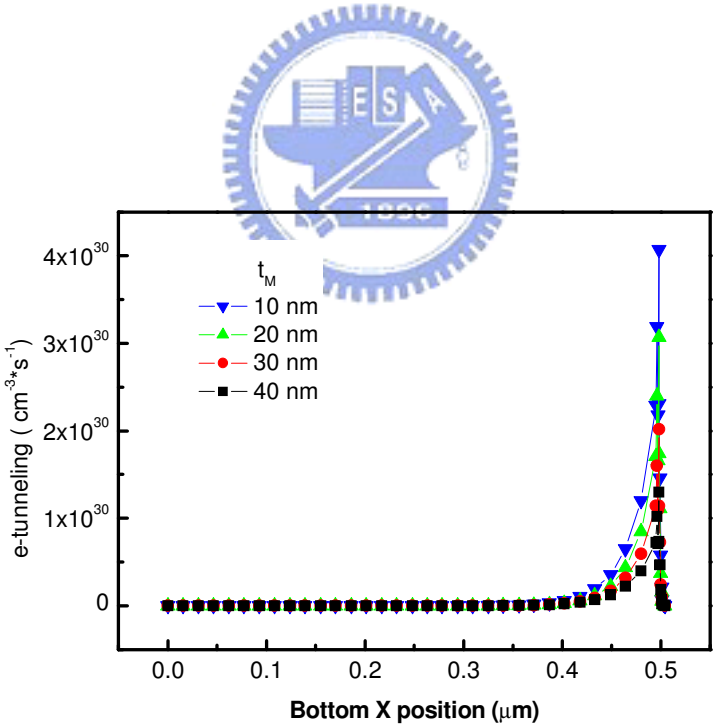
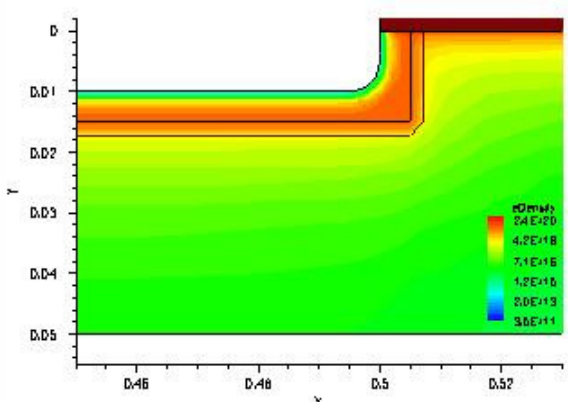
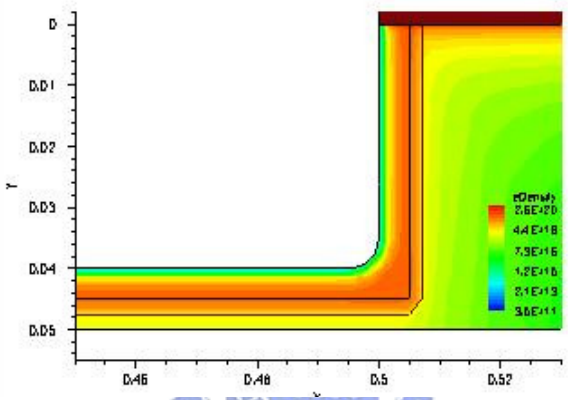


Fig.3-11 (a) The tunneling current at sidewall (b) the tunneling current at bottom of the MSB FETs with t_{MSB} = 5 nm, N_{MSB} = 5× 10^{19} cm^{-3}.

(a)



(b)



(c)

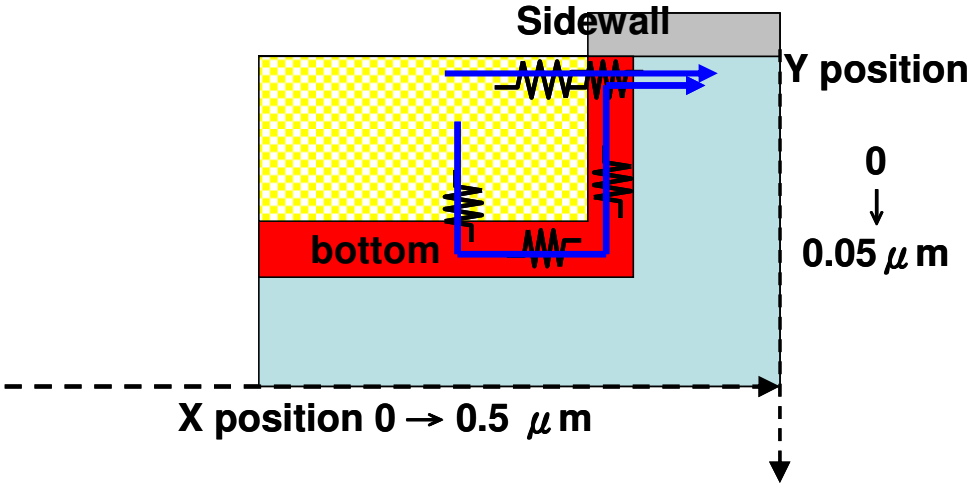
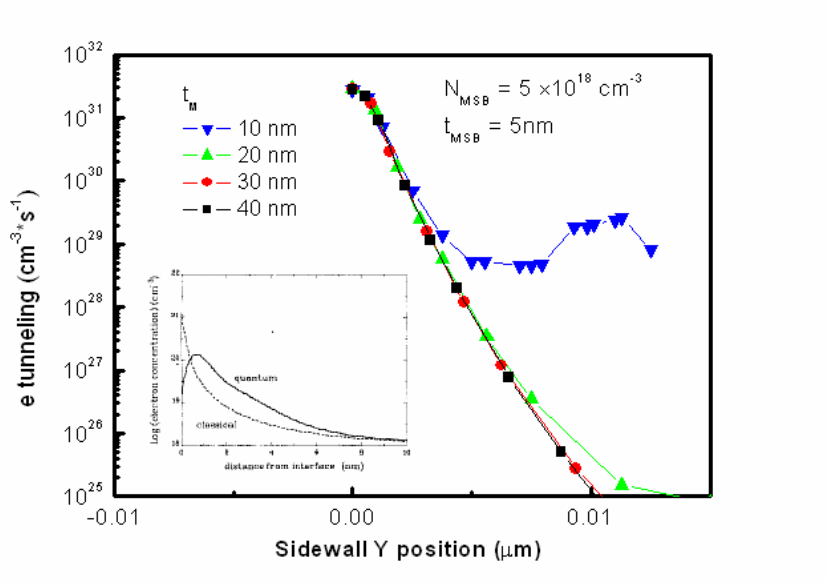


Fig.3-12 (a) and (b) The electron density at source side with t_M = 10/40 nm. (c) the equivalent circuit at source side in MSB FETs devices.

(a)



(b)

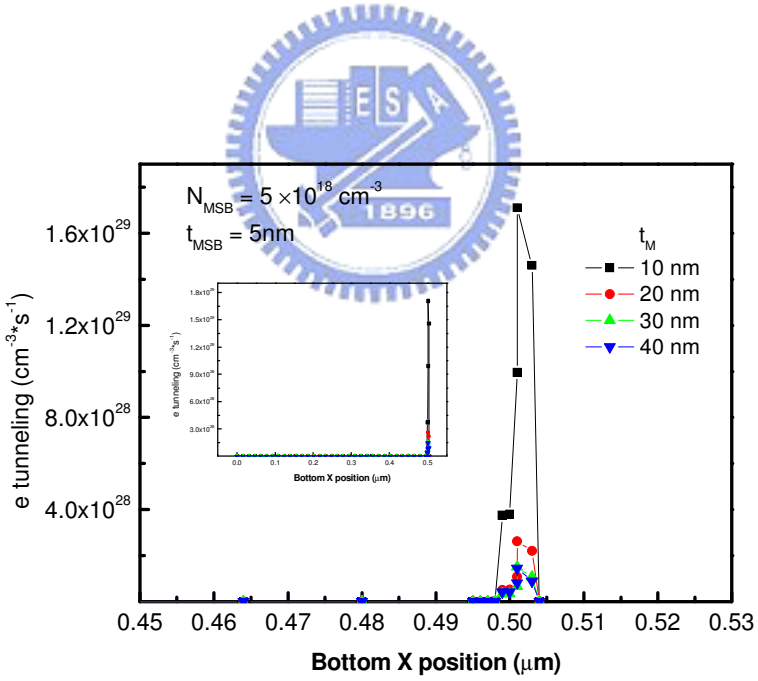
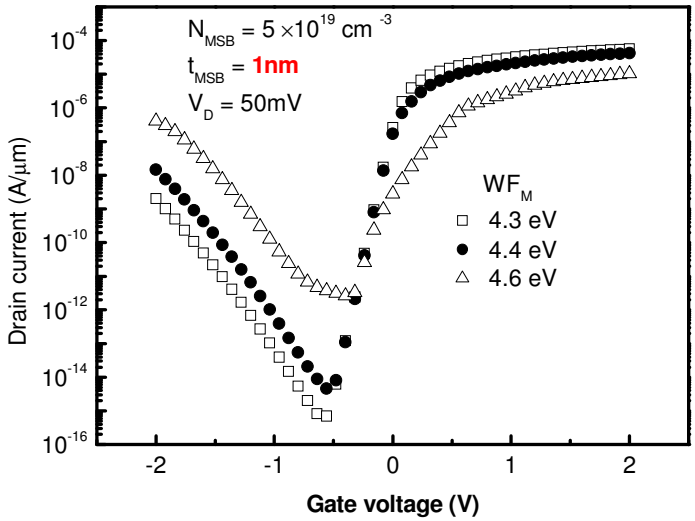


Fig.3-13 (a) The tunneling current at bottom (b) the tunneling current at sidewall of the MSB FETs with t_{MSB} = 5 nm, N_{MSB} = 5× 10^{18} cm^{-3}.

(a)



(b)

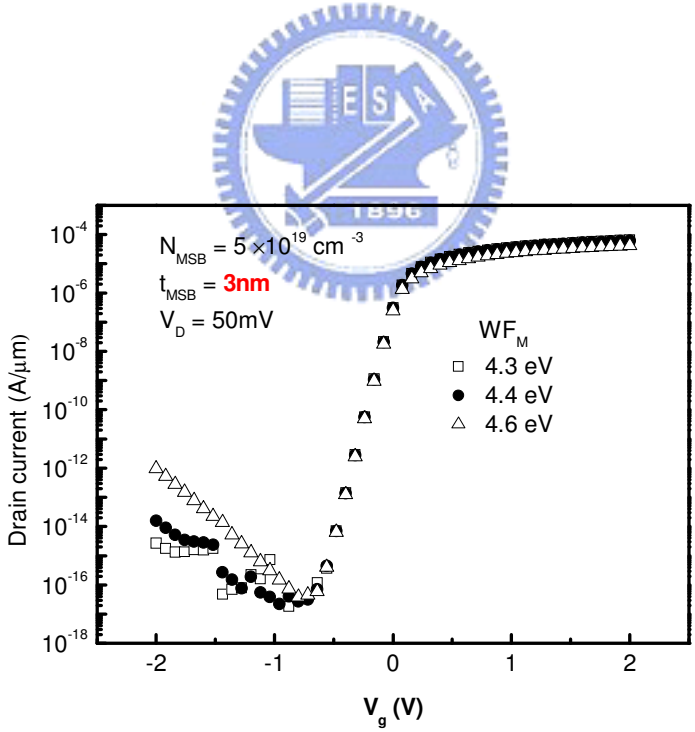


Fig.3-14 The transfer characteristics of MSB FETs with various silicide work-function (WF_M).

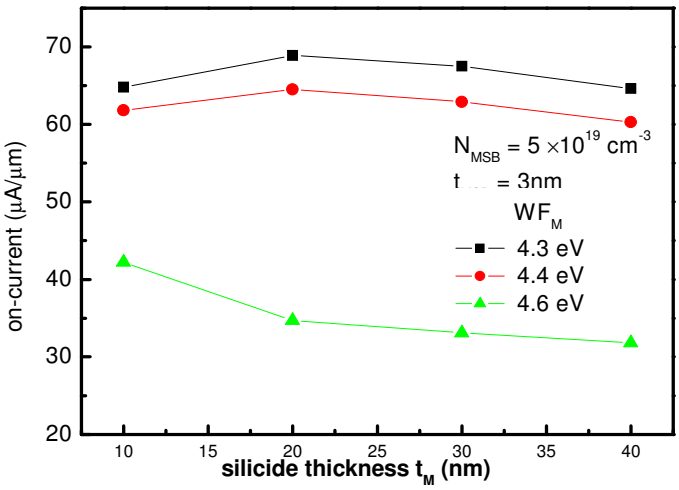


Fig.3-15 The on-current versus silicide thickness (t_M) of the MSB FETs with various silicide work-function (WF_M).

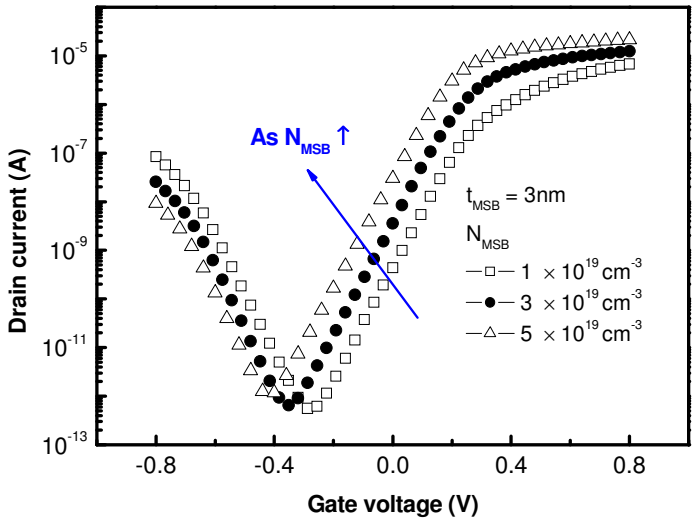


Fig.3-16 The transfer characteristics of tri-gate MSB FETs with t_{MSB} = 3 nm and varied N_{MSB}.

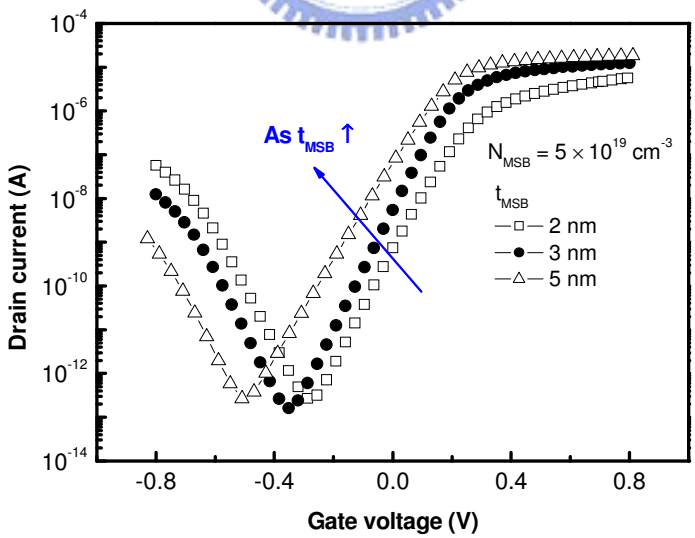
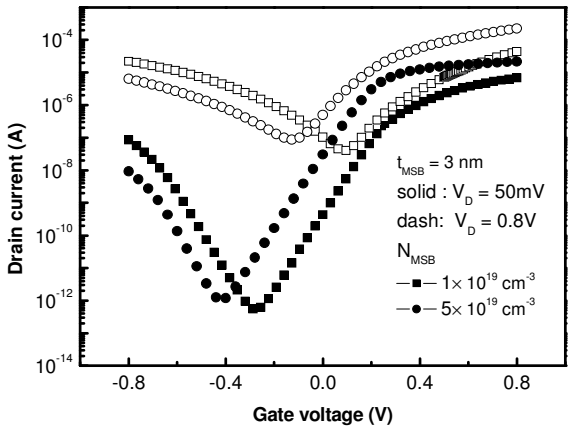
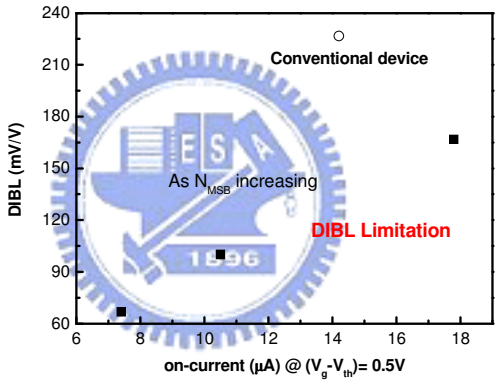


Fig.3-17 The transfer characteristics of tri-gate MSB FETs with N_{MSB} = 5× 10^{19} cm^{-3} and various t_{MSB}.

(a)



(b)



(c)

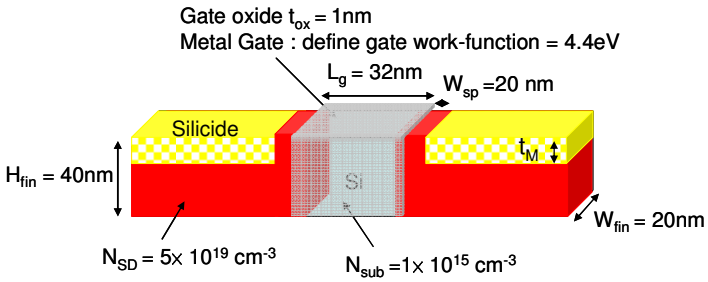


Fig. 3-18 (a) The transfer characteristics of tri-gate MSB FETs with t_{MSB} = 3nm and N_{MSB} = 1/5 × 10^{19} cm^{-3}. (b) the DIBL versus on-current at various N_{MSB} =1/3/5 × 10^{19} cm^{-3} and conventional device (c) the structural parameters of conventional deivce

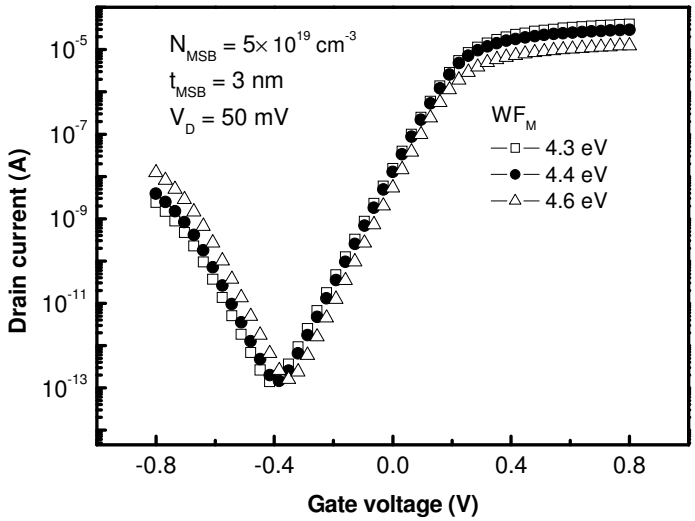
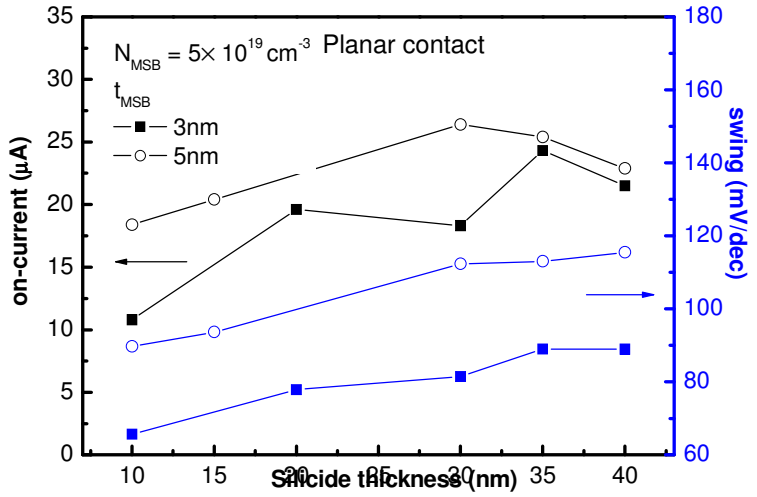


Fig.3-19 The transfer characteristics of tri-gate MSB FETs with t_{MSB} = 3 nm and $N_{MSB} = 5 \times 10^{19}$ cm^{-3} and various silicide work-function (WF_M).

(a)



(b)

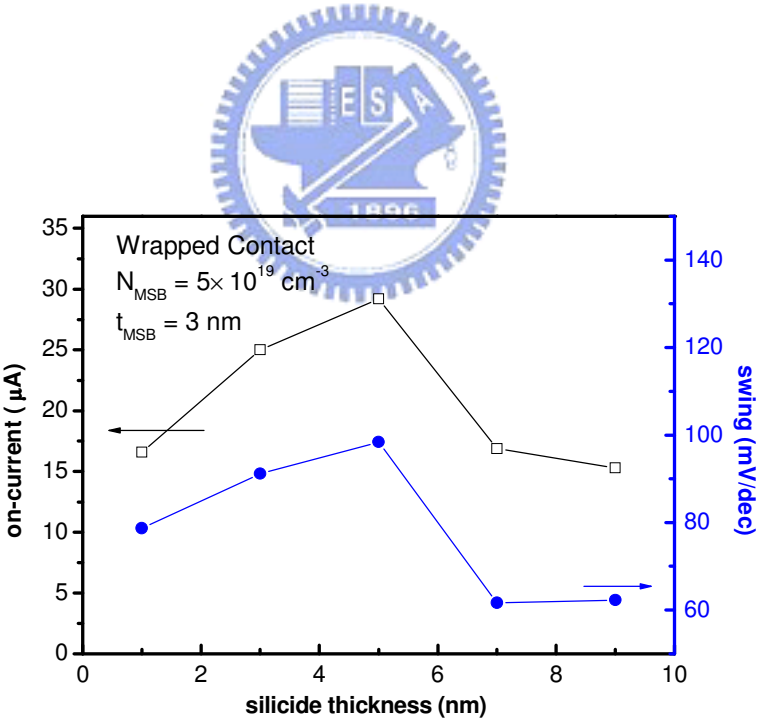
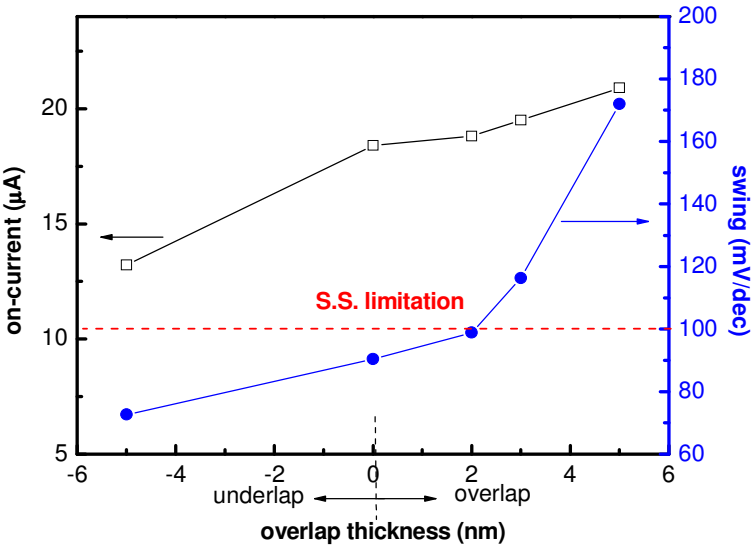


Fig.3-20 (a) The on-current and SS relation with various silicide thickness (t_M) in planar contact (b) in the wrapped contact.

(a)



(b)

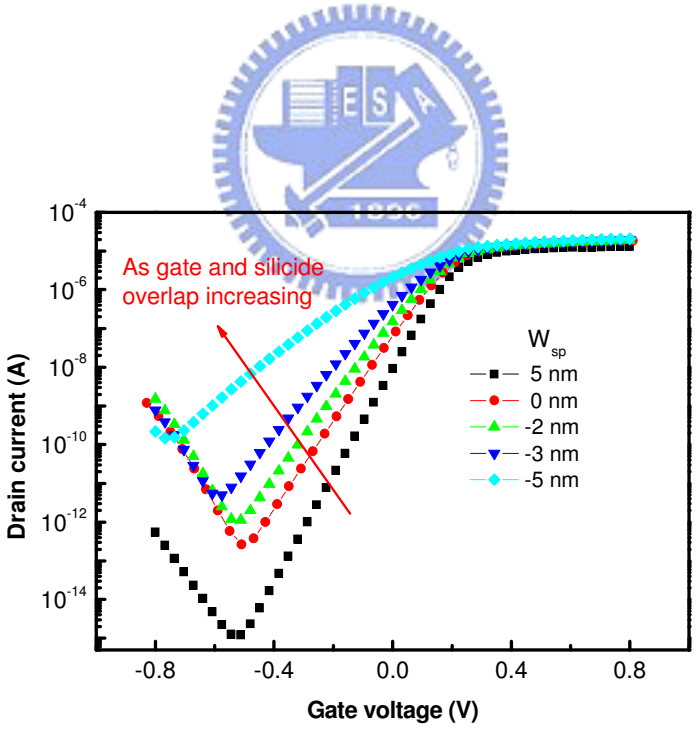
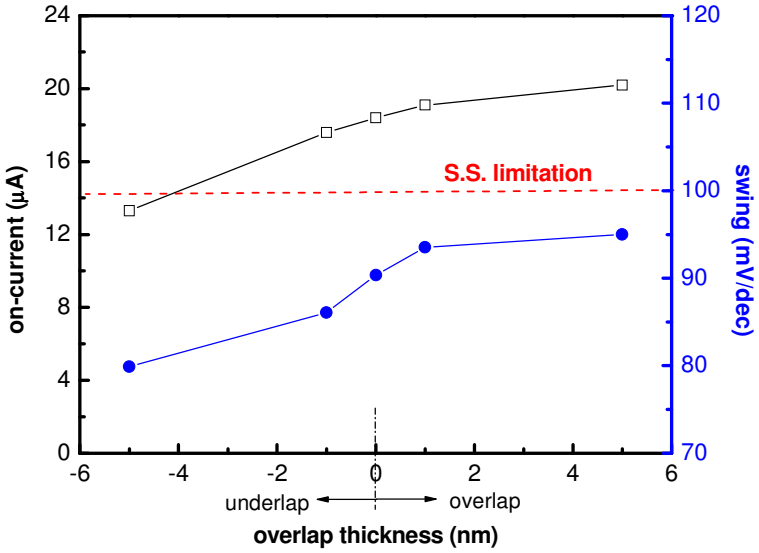


Fig.3-21 (a) The on-current and SS relation with underlap/overlap device (b) The transfer characteristics of tri-gate MSB FETs with various spacer thickness (W_{sp}) at same channel length (32 nm).

(a)



(b)

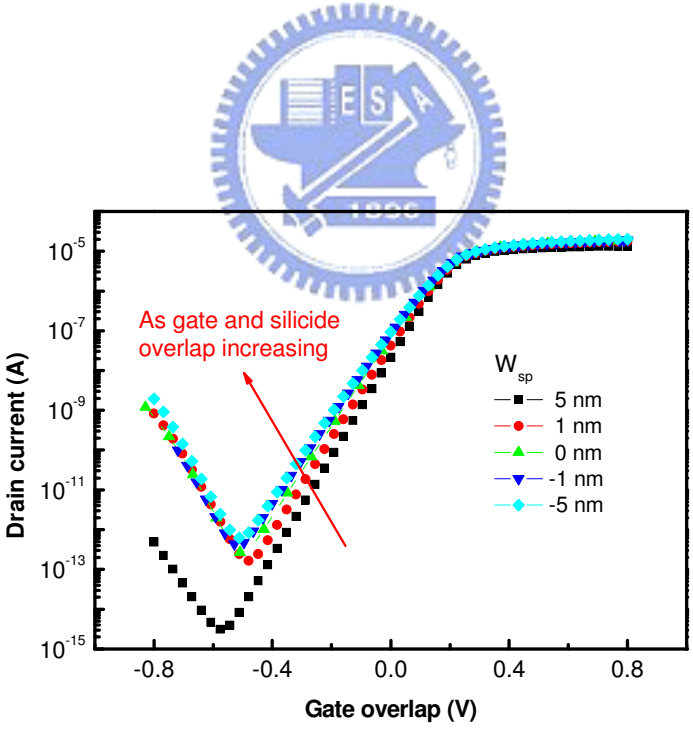


Fig.3-22 (a) The on-current and SS relation with underlap/overlap device (b) The transfer characteristics of tri-gate MSB FETs with various spacer thickness (W_{sp}) at same effective channel length.

Chapter 4

R_{sd} Extraction on MSB (Modified-Schottky-Barrier) FETs

4-1 External Loading Method

In 1983, S. T. Hsu presented the external loading method to determine series resistance and κ factor of MOSFETs [41]. The drain current (I_D) of MOSFETs in linear region is given by:

$$I_D = \kappa\left\{\left(V_G - V_T - \frac{1}{2}V_D\right)V_D\right\} \qquad \text{for } V_D << (V_G\text{-}V_T) \qquad (1)$$

where $\kappa = W\mu C_{ox}/L$, W is channel width, L is channel length, μ is carrier mobility, and C_{ox} is gate capacitance. In Eq. (1), the mobility is constant mobility model without gate bias effect, and the series resistance is not considering.

However, as we knew, the series resistance would degrade the device performance due to a voltage drop at source/drain region. In this case, the voltage drop in channel is reduced as shown in Fig.4-1. Therefore, considering about the series resistance effect (R_S and R_D at source/drain side), the drain current at linear region from Eq. (1) could be expressed as:

$$I_D = \kappa\left\{V_G - V_T - I_D(R_S + R_l) - \frac{1}{2}[V_D - I_D(R_S + R_D + R_l)]\right\}[V_D - I_D(R_S + R_D + R_l)]$$

, where R_l is loading resistance at source side (2)

Choose suitable loading resistance (R_l) to satisfy the following condition,

$$V_G - V_T - (V_D/2) >> (I_D/2)|R_D - R_S - R_l| \qquad (3)$$

Eq. (2) can be simplified as

$$I_D = \kappa\left[V_G - V_T - \frac{1}{2}V_D\right][V_D - I_D(R_S + R_D + R_l] \ . \qquad (4)$$

After some manipulations the following result is verified,

$$I_D = \frac{\kappa\left(V_G - V_T - \frac{1}{2}V_D\right)}{1+\kappa(R_T+R_l)\left(V_G - V_T - \frac{1}{2}V_D\right)} \rightarrow \frac{1}{I_D} = \frac{R_T+R_l}{V_D} + \frac{1}{\kappa\left(V_G - V_T - \frac{1}{2}V_D\right)V_D} \quad (5)$$

, where $R_T = R_S + R_D$ and R_T represents the total external resistance of this MOSFET. From Eq. (5), it is observed that I_D^{-1} is a linear function of R_l. Thus, from the plot of I_D^{-1} versus R_l with V_G as a parameter, a family of parallel straight lines is obtained. The slope of these straight lines is equal to V_D^{-1}, and these straight lines intersect the R_l axis at $R_{lo}(V_G)$, where

$$-R_{lo}(V_G) = R_T + \kappa^{-1}\left(V_G - V_T - \frac{1}{2}V_D\right)^{-1} \quad (6)$$

From Eg. (6), the $R_{lo}(V_G)$ is a linear function of $[V_G\text{-}V_T\text{-}(V_D/2)]^{-1}$. The slope of this straight line is κ^{-1}. The intersection of the straight line at R_{lo} axis gives R_T. Therefore, from the $R_{lo}(V_G)$ - $[V_G\text{-}V_T\text{-}(V_D/2)]^{-1}$ plot, the series resistance (R_T) and κ factor can be extracted. The external loading method provides a simple method to extract the series resistance from single device.

4-2 R_{sd} extraction on Simulation device

4-2-1 Conventional SOI device

The accuracy of applying the external loading method on SOI devices was examined by the Sentaurus-TCAD tool simulation. The conventional SOI device was used at first, and the structure of conventional device is shown in Fig.4-2. By using external loading method to extract series resistance, a loading resistance at source side is needed. In the simulation device, source electrode was serially connected by a loading resistance.

Fig.4-3(a) presents the I_D^{-1} - R_l plot. The slope of these straight lines is equal to

20 V^{-1}, which is equal to V_D^{-1} as expected. The $R_{lo}(V_G)$ are obtained from Fig.4-3(a) by extrapolating. Then, Fig.4-3(b) presents the $R_{lo}(V_G)$ versus $[V_G-V_T-(V_D/2)]^{-1}$ plot. The slope of this straight line is 1173.75 V^2A^{-1} and the mobility calculated from this value is 432 cm^2 V-sec. The series resistance extracted by the intersection at the R_{lo} axis is 200.9 Ω-μm.

The drain current of the device is calculated from Eq. (5) using the extrcated R_T and κ values to check the accuracy of this extraction method. Fig.4-4 shows the simulated and calculated transfer characteristics. The calculated values are well fitted with the simulated results. The calculated points are slightly higher than the simulated results because the calculation ignores mobility degradation at high gate bias.

Fig.4-5 presents the on-current and the extracted series resistance with various t_M. The optimize t_M for the highest on-current and the lowest series resistance are equal to 20 nm. The series resistance with t_M 20 nm is 173.6 Ω-μm. Moreover, the trend of on-current is native proportional to the trend of series resistance as expected. Table4-1 summarizes the detailed values of the series resistance, mobility, and on-current at gate bias of 2 V with various t_M.

4-2-2 Conventional-like MSB FET

From the results of chapter 3, MSB FETs can be classified into two groups. One is conventional-like device, whose MSB region would not be depleted even at high gate bias. The other one is SB-like device, which has conventional-like behavior at low subthreshold region while the Schottky barrier dominates device perfromaqnce at high gate bias because the MSB region is totally depleted. In this section, series resistance of conventional-like MSB FETs is extracted and discussed. SB-like MSB FETs will be discussed in the next section.

The simulated MSB FET has parameters of t_{MSB} = 5 nm, N_{MSB} = 5×10^{19} cm^{-3},

and WF_M = 4.6 eV. Fig.4-6(a) presents that the $R_{lo}(V_G)$ versus $[V_G-V_T-(V_D/2)]^{-1}$ plot shows an excellent linearity. The slope of this straight line is 1241.06 V^2A^{-1}. This extrapolated intersect at the $R_{lo}(V_G)$ axis is 172.06 Ω. Therefore, the mobility is 409 cm^2 V-sec and the series resistance is 172.06 Ω-μm. Substituting the extraction values of R_T and κ into Eq. (5), the calculated transfer characteristic exhibits excellent agreement with the simulated result as shown in Fig.4-6(b). Hence, the external loading method can be applied to conventional-like MSB FETs.

Fig.4-7 compares the on-current and series resistance with various t_M. The optimized t_M is 20 nm and series resistance is 160.01 Ω-μm. The series resistance of the MSB FET with FUSI source/drain structure, i.e. t_M = 45nm, is 220 Ω-μm, which translate to a specific contact resistivity of lower than 5.5×10^{-8} Ω-cm^2. This value is close to the requirement of ITRS roadmap [2]. That means t_{MSB} = 5 nm and N_{MSB} = 5×10^{19} cm^{-3} are acceptable parameters for sub 45nm technology nodes. Besides, the trend of on-current is consistent with the trend of series resistance. Table4-2 summarizes the detailed values of the series resistance, mobility, and on-current at gate bias of 2 V with various t_M.

Table4-3 lists the series resistance of the MSB FETs with various t_{MSB} and WF_M. As the WF_M equals to 4.4 eV, the series resistance is inversely proportional to t_{MSB}. In this case, the tunneling resistance is higher than the resistance of MSB region. Increasing the t_{MSB} results in the thin-down of the effective Schottky barrier thickness. However, when the WF_M reduces to 4.3 eV, the series resistance becomes proportional to t_{MSB}. The tunneling resistance is lower than the resistance of the MSB region. The resistance of the MSB region increases as t_{MSB} increases so that the series resistance increases with the increase of t_{MSB}.

4-2-3 SB-like MSB FET

The MSB FET with t_{MSB} = 3 nm, N_{MSB} = 5×10^{19} cm^{-3}, and WF_M = 4.6 eV becomes SB-like device. Fig.4-8(a) shows the I_D^{-1}- R_l plot. It is observed that the slopes of these straight lines are not equal to V_D^{-1}. Fig.4-8(b) shows that the $R_{lo}(V_G)$ is not linear proportional to the $[V_G-V_T-(V_D/2)]^{-1}$. Therefore, the external loading method can not be applied to the SB-like MSB FETs. Fig.4-9 presents the transfer characteristics and transconductance (g_m) of the simulated device. It is observed that the transfer characteristics consist of the effects of channel potential and Schottky barrier. The reason why the external loading method can not be applied is still under studying.

In order to estimate the series resistance of the SB-like devices, the series resistance is defined as the total resistance subtracted by the channel resistance. Fig.4-10 shows the variation of the series resistance as gate bias increases. Because the Schottky barrier resistance dominates the series resistance, the series resistance is affected by the gate bias induced effective Schottky barrier lowering.

4-3 R_{sd} extraction of real devices

4-3-1 MSB FET

The real MSB FETs were fabricated by the process flow describe in chapter 2. In order to fabricate MSB FETs with different conditions of the MSB region, two post-ITS annealing conditions were used. For the conventional-like device, the post-ITS annealing was performed at 600℃ for 30 minutes. Fig.4-11 shows the typical transfer characteristic and g_m. The transfer characteristic is very similar to that of the conventional devices. Therefore, it could be confirmed that the t_{MSB} and N_{MSB} are sufficient to reduce the effective Schottky barrier height.

The external loading method is then applied to extract the series resistance of the experimental device with channel length = 5 μm and channel width = 1 μm. Fig.4-12(a) shows that the $R_{lo}(V_G)$ versus $[V_G-V_T-(V_D/2)]^{-1}$ plot has an excellent linearity. The slope of this straight line is 27656 V^2A^{-1}. This straight line intersects the $R_{lo}(V_G)$ axis at 3161.4 Ω. Therefore, the series resistance of this device is equal to 3161.4 Ω-μm and the mobility is 261.9 cm^2 V-sec. The mobility is lower than the simulated results because of additional scatterings due to interface roughness and oxide charges. If the extracted series resistance is explained as the contact resistance, i.e. ignore the resistance of probing system, resistance of source/drain silicide, resistance due to current crowding, etc., the specific contact resistivity is calculated to be about 6×10^{-7} Ω-cm^2. The actual value should be lower than 6×10^{-7} Ω-cm^2 but is higher than the requirement of ITRS roadmap for future application. Fig.4-12(b) compares the transfer characteristic calculated from the extracted parameters with the directly measured characteristic. It is shown that the calculated results have a great agreement with the measured results. This agreement confirms that the external loading method can be applied to conventional-like MSB FETs. Table4-4 summarizes the extracted series resistance of devices with different L/W ratios. The series resistances distributes in the range of 1~3 kΩ-μm. The series resistances of real devices are one order larger than simulation results. The reason may be the doping concentration at silicide/silicon interface is not as high as 5×10^{19} cm^{-3}.

On the other hand, as the post-ITS annealing time is reduced to 30sec, the device exhibits SB-like behavior as shown in Fig.4-13(a). In this case, the $R_{lo}(V_G)$ versus $[V_G-V_T-(V_D/2)]^{-1}$ plot becomes nonlinear and the series resistance can not be extracted properly. This nonlinear phenomenon is consistent with the simulated result discussed in section 4-2-3.

4-3-2 R_c extraction by test structure

In this sub-section, the specific contact resistivity of the silicide/MSB region is extracted from the test structures proposed in chapter 2. For the multi-junction structure, four-terminal measurement is used. Current flows from electrode 1 to electrode 4. Electrode 2 and 3 were used to sense the voltage drop across the two junctions. The total resistance contains silicon sheet resistance and two times of the contact resistance ($R_{total} = R_{silicon} + 2\times R_c$). Structures with various silicon lengths (L_{Si}) were measured and the contact resistance can be extracted from the extrapolated intersection at R_{total} axis of the linear R_{total}-L_{Si} plot. Fig.4-14 presents the measured R_{total} - L_{Si} plot. The large variation at the same L_{Si} is due to the deviation of silicide lateral growth [30]. For larger fin width, the silicide region consists of multiple grains. The multigrain structure results in a nonuniform silicon/silicide interface. Therefore, for different structure with the same process condition, the silicide lateral growth is not identical which results in the deviation of L_{Si}. This issue can be improvement as the fin width can be reduced to about 50 nm because the silicide would become bamboo structure. Although deviation of R_{total} is large, a linear trend is still observed. The contact resistivity is estimated to be about $3\sim4\times10^{-7}$ Ω-cm^2 from Fig.4-14. This value is consistent with that estimated from the series resistance of MSB FETs (section 4-3-1).

The other test structure is the Quasi-vertical Kelvin structure. Fig.4-15 presents the current and the voltage difference of this structure. The extracted Rc is about 3.3 kΩ for fin width equals to 0.5 μm. To exclude the error of n^- sheet resistance (the detailed discussion in chapter 2), the actual contact resistance is about 2.4 kΩ and the contact resistivity is about 4.8×10^{-7} Ω-cm^2. The contact resistivity agrees with that in multi-junction structure. In these test structure, the extracted contact resistivity is lager than the required value in ITRS roadmap. The reason is the MSB doping

concentration is not high enough as expected. Therefore, the way to raising the doping concentration at silicide/silicon interface must be studied continually to meet the requirements.

Table4-1 The comparison of extracted values for conventional SOI FETs with varied t_M.

t_M (nm)	10	20	30	40
R_{sd} (Ω)	200.9	173.6	212.9	282.9
μ (cm^2 V-s)	432	430	431	431
I_{on} (Vg@2V)	6.21×10^{-5}	6.45×10^{-5}	6.14×10^{-5}	5.59×10^{-5}

Table4-2 The comparison of extracted values for MSB conventional-like FETs with varied t_M.

t_M (nm)	10	20	30	40	45
R_{sd} (Ω)	172.06	160.01	190.79	220.94	215.13
μ (cm^2 V-s)	408	418	427	431	431
I_{on} (Vg@2V)	6.05×10^{-5}	6.38×10^{-5}	6.25×10^{-5}	60.1×10^{-5}	6.09×10^{-5}

Table4-3 The comparison of extracted values for MSB FETs with varied MSB region condition and WF_M.

t_{MSB} (nm) WF_M (eV)	2	3	5
4.3	91.14	99.51	107.74
4.4	137.65	127.26	121.30

Table4-4 The comparison of extracted values for MSB FETs with various L/W ratios.

L/W (μm)	5/1	2/1	1/1	0.8/1	0.6/1
R_{sd} (Ω)	3161.4	1868.4	1735.8	1667.5	3055.5
	2166.2	2309.9	1468.1	1232.1	-
	3239.7	2723.2	953.54	-	-

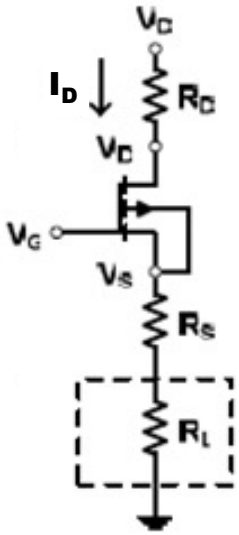


Fig.4-1 Equivalent circuit of a MOSFET.

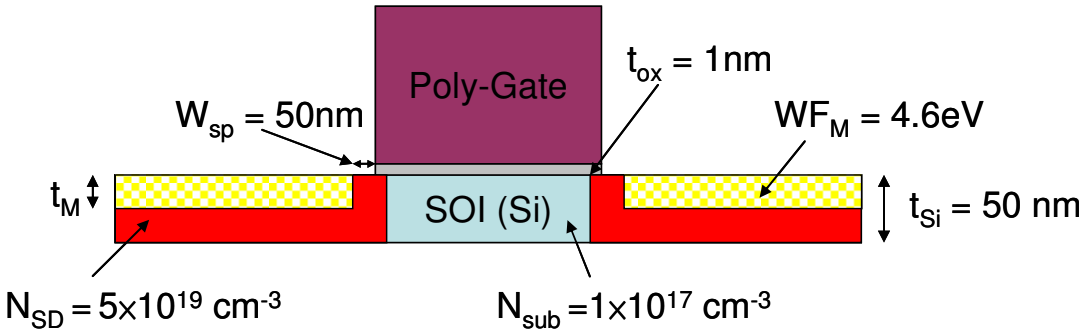
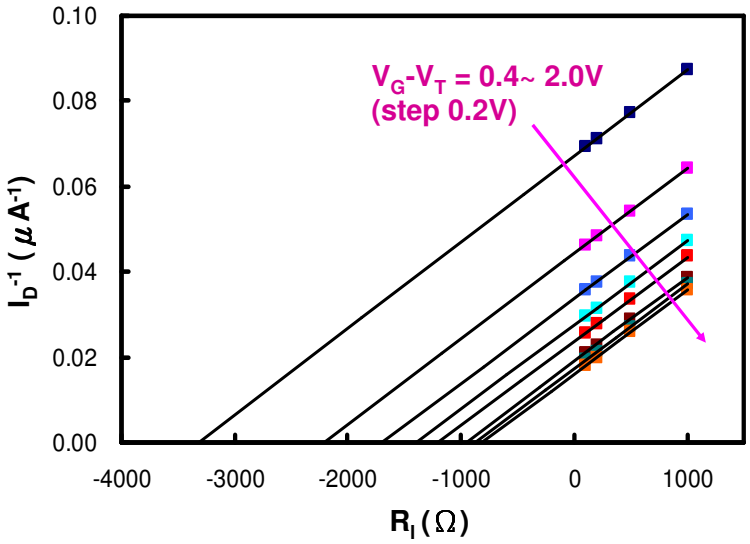


Fig.4-2 The simulation structure of conventional SOI device.

(a)



(b)

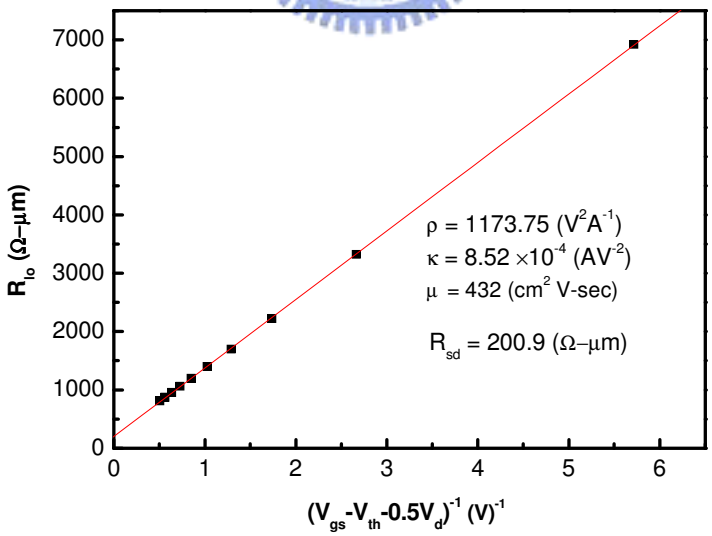


Fig.4-3 (a) $1/I_D$ versus R_{lo} of the conventional SOI FETs. (b) $R_{lo}(V_G)$ versus $[V_G\text{-}V_T\text{-}(V_D/2)]^{-1}$ characteristics of the conventional SOI FETs.

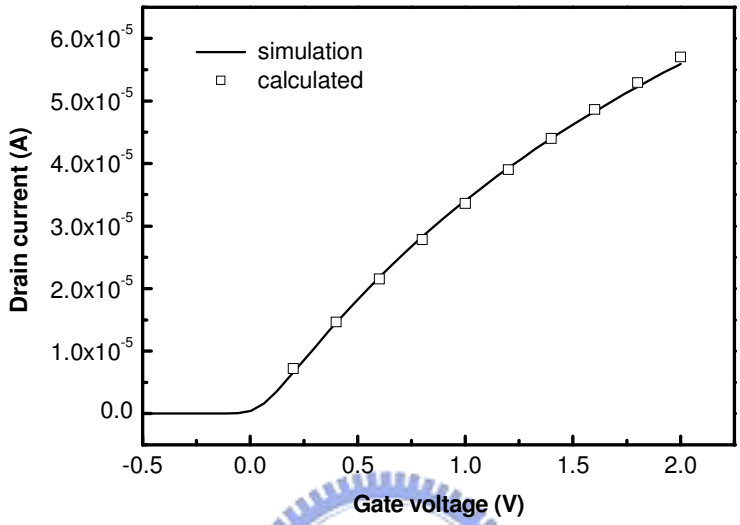


Fig.4-4 The transfer characteristics of the conventional SOI FETs in linear region (V_D at 50 mV). Curve is simulated and points are calculated.

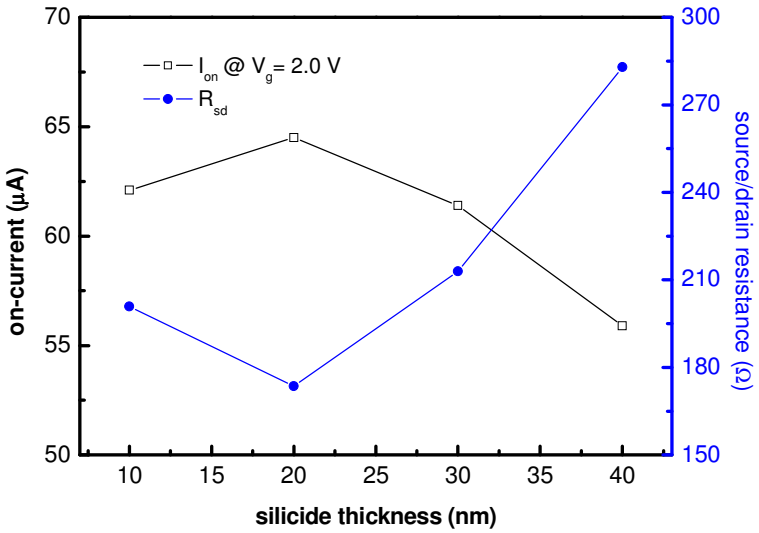
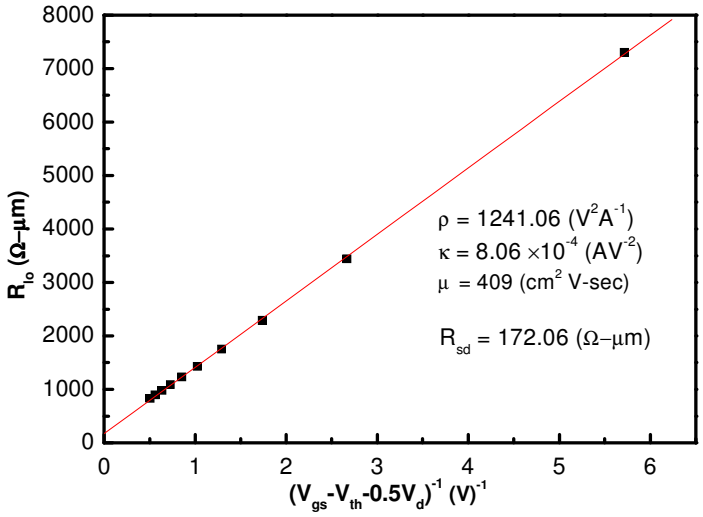


Fig.4-5 The on-current and series resistance trend with varied silicide thickness (t_M).

(a)



(b)

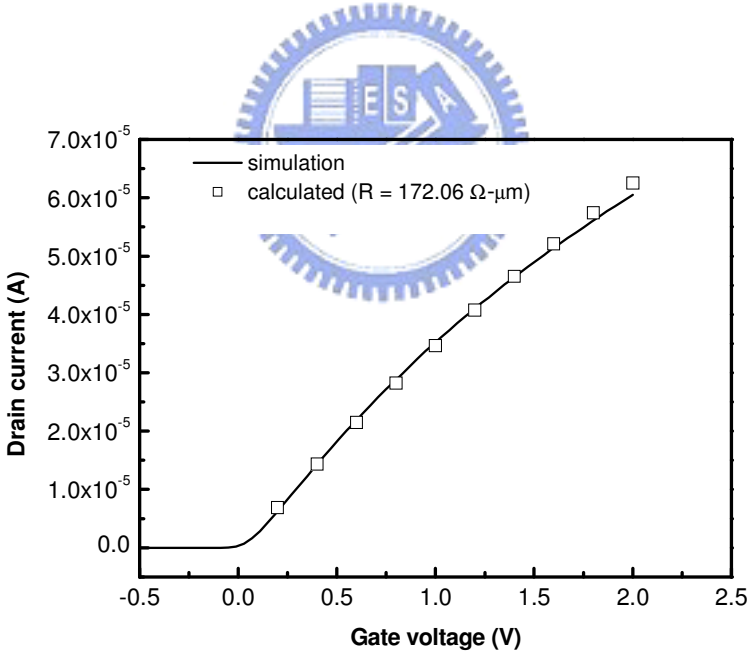


Fig.4-6 (a) $R_{lo}(V_G)$ versus $[V_G-V_T-(V_D/2)]^{-1}$ characteristics of the MSB conventional-like FETs.(parameter conditions of t_{MSB} = 5 nm, N_{MSB} = 5×10^{19} cm^{-3}, and t_M = 10 nm) (b) The transfer characteristics of the MSB conventional-like FETs in linear region(V_D at 50 mV).

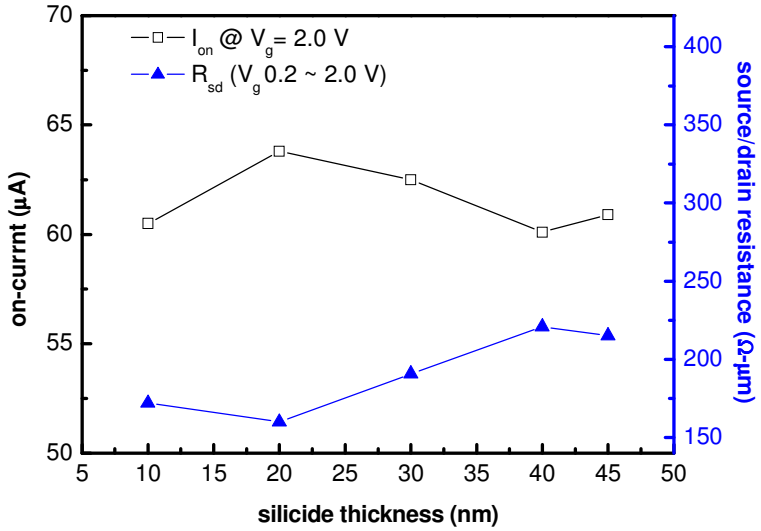
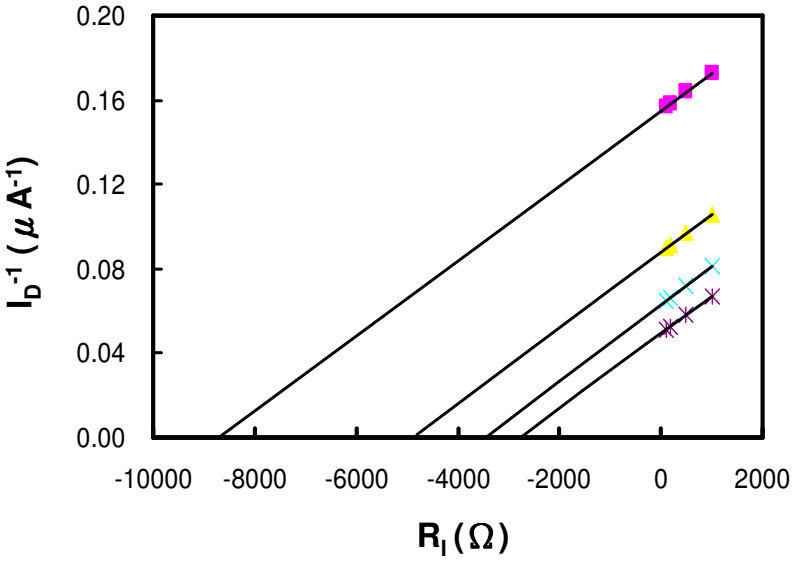


Fig.4-7 The on-current and series resistance trend with varied t_M in the MSB conventional-like FETs.

(a)



(b)

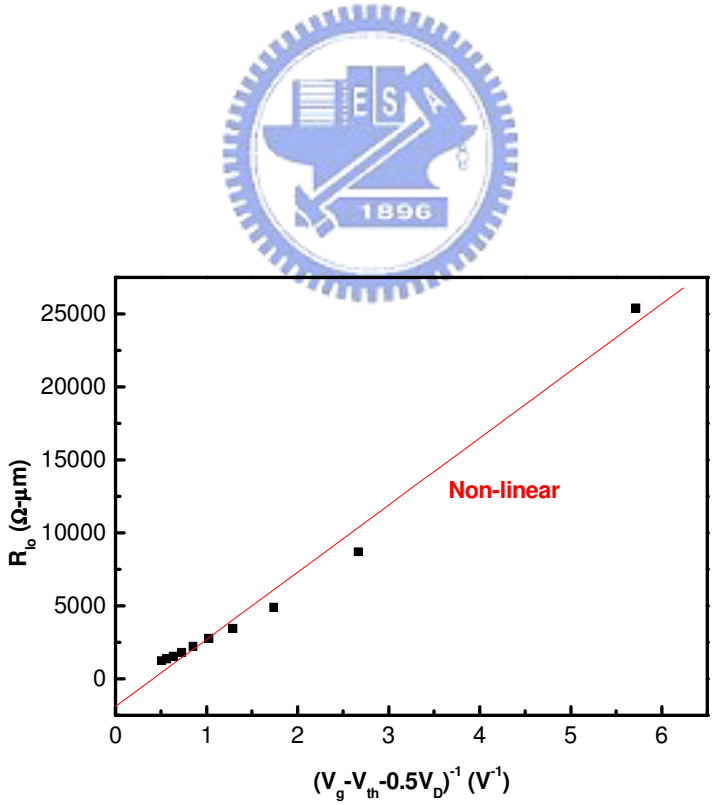


Fig.4-8 (a) $1/I_D$ versus R_{lo} of the MSB SB-like FETs. (b) $R_{lo}(V_G)$ versus $[V_G-V_T-(V_D/2)]^{-1}$ characteristics of the MSB SB-like FETs FETs.

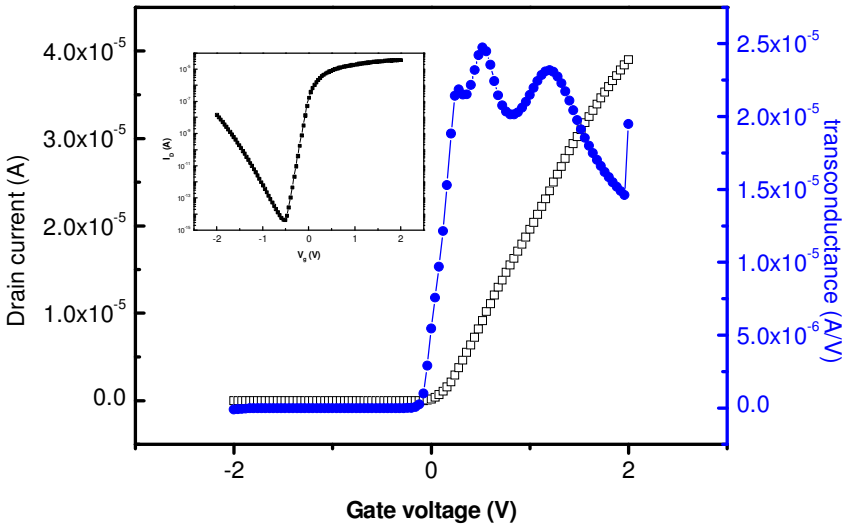


Fig.4-9 The transfer characteristics and transconductance (g_m) of the MSB SB-like FETs in linear region with parameter conditions of t_{MSB} = 3 nm, N_{MSB} =5×10^{19} cm^{-3}, t_M = 10 nm and WF_M = 4.6 eV.

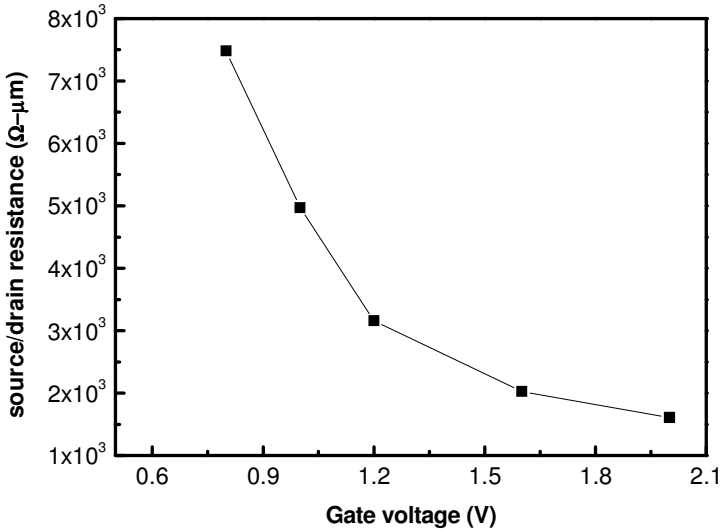


Fig.4-10 The series resistance versus gate voltage of the MSB SB-like FETs.

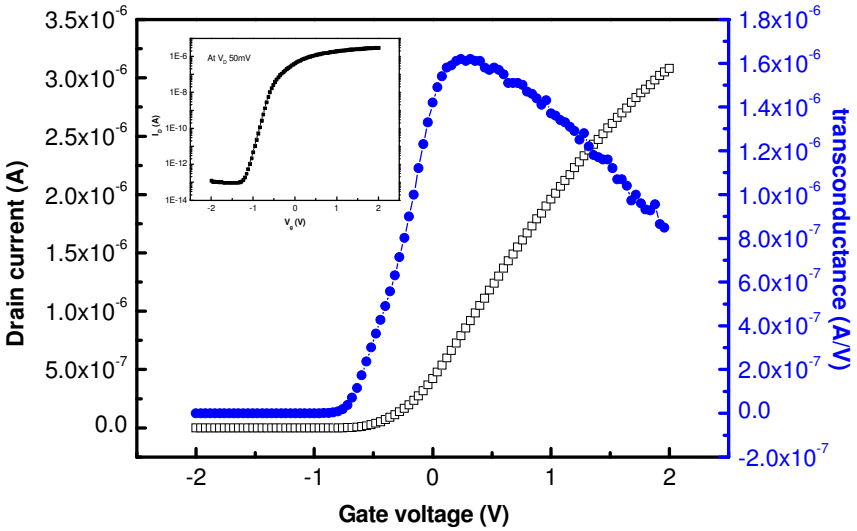
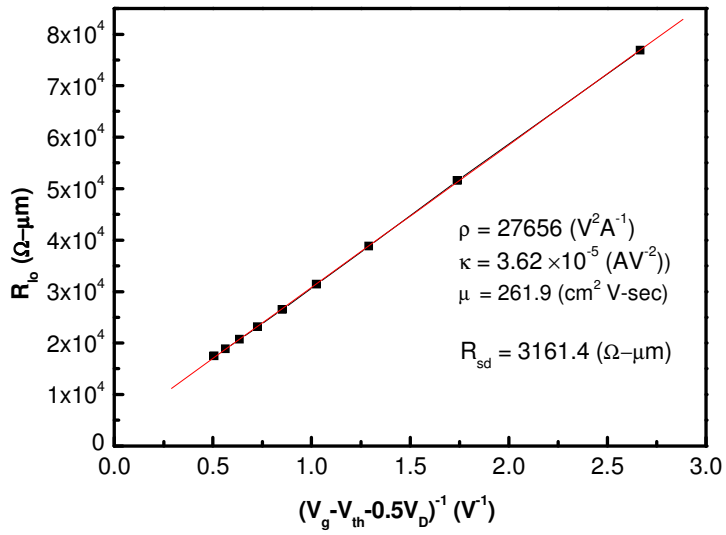


Fig.4-11 The drain current and transconductance (g_m) versus gate voltage of the MSB conventional-like FETs in real devices.

(a)



(b)

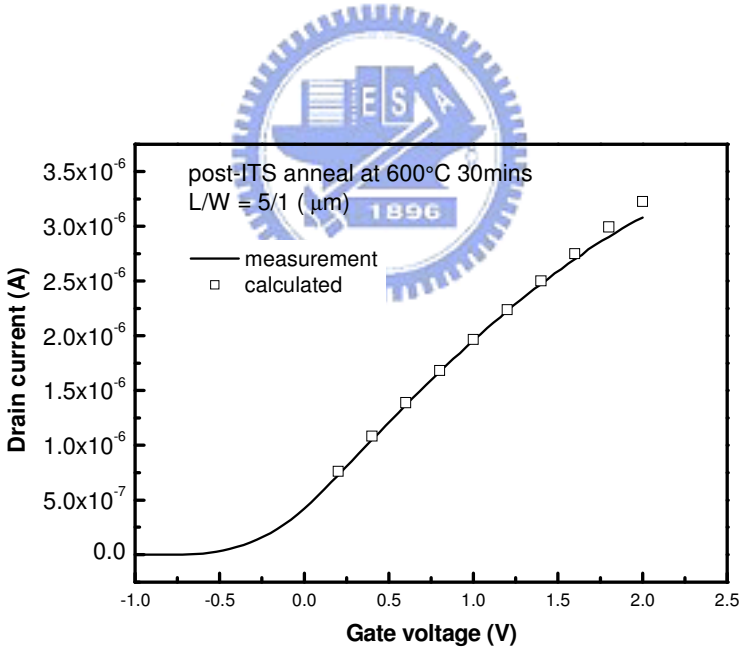
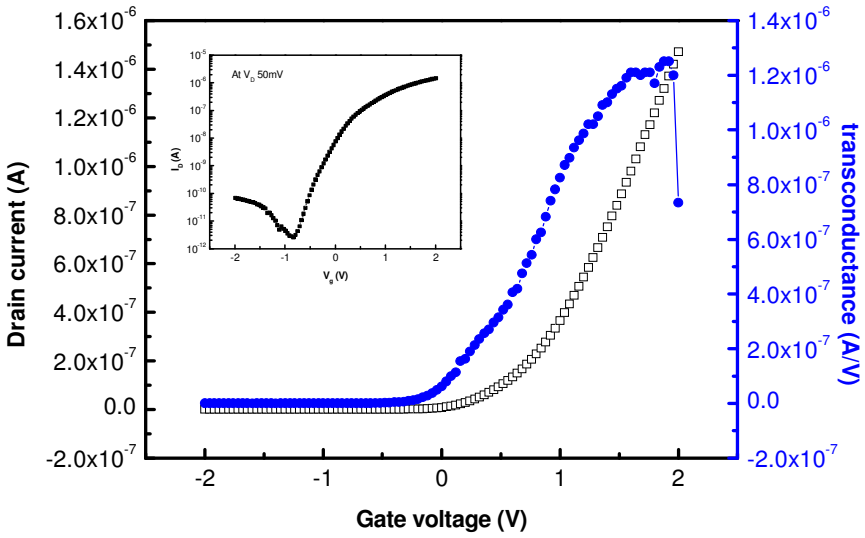


Fig.4-12 (a) $R_{lo}(V_G)$ versus $[V_G-V_T-(V_D/2)]^{-1}$ characteristics of the MSB conventional-like FETs.(post-ITS annealing at 600℃ 30 min) (b) The transfer characteristics of the MSB conventional-like FETs in linear region(V_D at 50 mV).

(a)



(b)

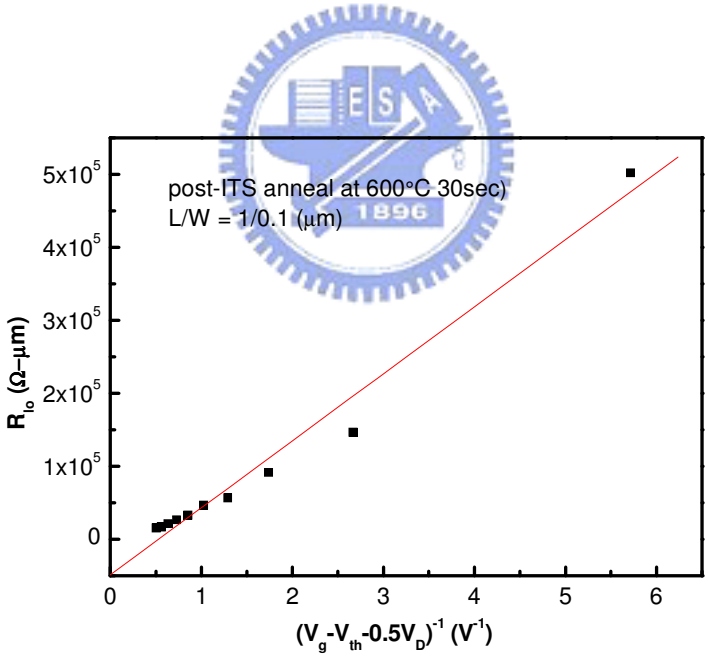


Fig.4-13 (a) The drain current and mutual conductance (g_m) versus gate voltage of the MSB SB-like FETs.(post-ITS annealing at 600℃ 30sec) (b) $R_{lo}(V_G)$ versus $[V_G-V_T-(V_D/2)]^{-1}$ characteristics of the MSB SB-like FETs.(post-ITS annealing at 600℃ 30sec).

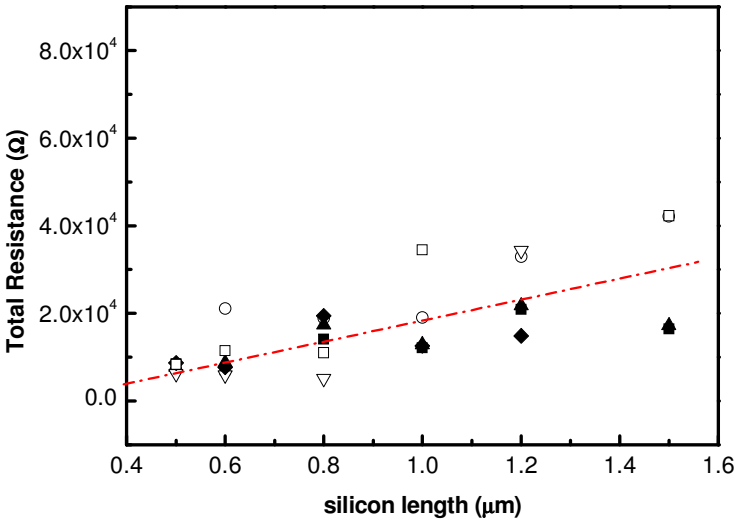


Fig.4-14 The plot of R_{total} versus L_{si} in the multi-junction series sturcture.

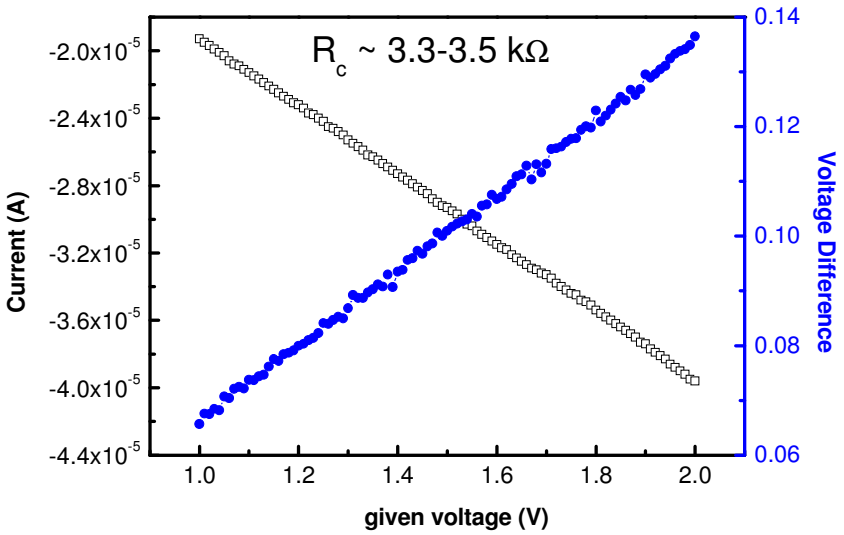


Fig.4-15 The plot of current and voltage difference versus given voltage in the Quasi-vertical Kelvin structure.

Chapter 5

Conclusions and Future Works

5-1 Conclusions

In this thesis, the effect of MSB region on devices performance was evaluated by 2-dimensional and 3-dimensional TCAD simulation. The MSB FETs can be classified into two groups. One is conventional-like device with high doping concentration or thick thickness of the MSB region. The MSB region thinner the Schottky barrier thickness effectively at source side; therefore, the on-current is increased and the channel resistance dominates the device performance. The other one is SB-like device, the MSB thickness is thin or the doping concentration is low. This MSB region would be depleted by gate bias easily which results in feckless of this MSB region. As device scaling down, the MSB region with thicker thickness would degrade the device performance due to the reduction of effective channel length. Therefore, the MSB region with high doping concentration and thin thickness is needed for short channel device. However, the drain induced barrier lowering (DIBL) is another issue for short channel device. According to the simulation results, the DIBL would increase as MSB doping concentration increases. Therefore, a tradeoff between on-current and DIBL should be considered. The suitable parameters for the device with channel length = 32 nm are MSB doping concentration = 3×10^{19} cm^{-3} and MSB thickness = 3 nm. In this case, the DIBL is equal to 100 mV/V. The conventional device with the same source/drain doping concentration and effective channel length shows DIBL equal to 226.7 mV/V. Therefore, the MSB FETs have better DIBL behavior than conventional device.

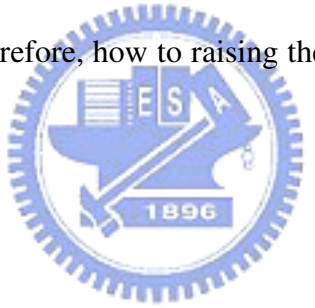
For the short channel device, the underlap/overlap structures were simulated to obtain this effect on device performance. For the overlap structure devices, the reduction of effect channel length would degrade the device performance and reduce the gate controllability. However, the underlap structure devices have a series resistance issue as the MSB region is not overlapped with gate. Therefore, the silicide lateral growth becomes an important issue for MSB FETs. The spacer length and the silicide formation condition are the parameters for silicide lateral growth.

For the study of source/drain resistance, the source/drain structures with various silicide thicknesses are used to increase the contact area. For the conventional-like devices the optimized value equal to 20 nm (about half of the silicon thickness). On the other hand, for the SB-like devices, the resistance increases as the silicide thickness increasing. The reason is the tunneling current concentrated at the channel surface; therefore, the effective contact area would not increase as silicide thickness increases. For tri-gate MSB FETs, two contact schemes were studied. One is planar contact, and the optimized value shifts to deeper silicide thickness which compares with that of the planar MSB FETs. It is caused by the sidewall channel effect. The other one is the wrapped contact, the optimized value is about quarter of the silicon fin width. In addition, the trends of on-current and subthreshold swing are the same; therefore, the tradeoff between on-current and subthreshild swing must be considered during device design.

The external loading method was used to extract the source/drain resistance. For the simulated devices, this method can be applied in the conventional-like devices. The extracted series resistances are consist with the on-current. For the MSB FETs with MSB doping concentration = 5×10^{19} cm^{-3} and thickness = 5 nm, the series resistance equals to 160.01 Ω-μm and the contact resistivity lower than 5.5×10^{-8} $\Omega\text{-}cm^2$ (regard series resistance as contact resistance). This value is close to the

requirement of ITRS roadmap. However, this device would suffer the DIBL problem. Therefore, in order to meet the ITRS roadmap, the lower silicide work-function material is needed to reduce the series resistance. For the real devices with conventional-like behavior, the external loading method is also suitable. The contact resistivity is about 6×10^{-7} Ω-cm^2, which is larger than expectation due to the MSB doping concentration is not high enough. On the other hand, this extraction method can not be applied to SB-like devices.

First time to extract the contact resistivity at the MSB region of sidewall surface by theses two test structure. The specific contact resistivity received from the contact resistivity test structures is about $3\sim5\times10^{-7}$ Ω-cm^2. This value is consistent with that estimated from the extracted series resistance of MSB FETs. The value is larger than that of ITRS requirement. Therefore, how to raising the MSB doping concentration is still needed to be improved.



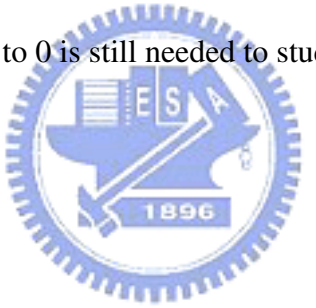
5-2 Future Works

In this thesis, the MSB region parameters are not considering about the doping gradient of the MSB region. In this thesis, the constant doping concentration in the MSB region was used to simulate and it is the ideal case. However, the doping gradient issue would become more and more serious for short channel device. Therefore, the doping gradient must be considered to obtain the effect on device performance and the scalability of the MSB region.

From the simulated results, the silicide lateral growth is an importance factor on device performance for short channel devices; therefore, the silicide formation condition must be optimized. For the lateral growth issue, the transmitted electron microscopy (TEM) can be used to obtain the optimized condition. And for the

source/drain structure of partially silicide also need to control the silicide formation condition. For Tri-gate MSB FETs with wrapped contact, the spacer at the sidewall of source/drain region is a big problem to fabricate an ideal wrapped contact. There are many process conditions still need to be investigate.

In the series resistance extraction section, the external loading method can not be applied for the SB-like device. The detailed reason is still studying and the method to extract series resistance on SB-like device is another topic to study. For the contact resistance test structure, the silicon width is too larger to cause the multigrain structure. In order to receive the actual contact resistivity, the silicon width should be scaled down to around 50 nm. For the Quasi-vertical Kelvin structure, the process error also limits the accuracy of the contact resistivity. How to create a structure with "e" parameter in Fig.2-7 equal to 0 is still needed to study.



References

[1] Yuan Taur, Douglas A. Buchanan, Wei Chen, David J. Frank, Khalid E. Ismail, Shih-hsien Lo, George A. Sai-halasz, Raman G. Viswanathan, Hsing-Jen C. Wann, Shalom J. Wind and Hon-Sum Wong, "CMOS Scaling into the Nanometer Regime," in *Proceeding of the IEEE*, pp.486-504, 1997.

[2] *International Technology Roadmap for Semiconductions(ITRS)*, 2007 edition.

[3] Y. K. Choi, K. Asano, N. Lindert, V. Subramanian, T. J. King, J. Bokor, and Chenming Hu, "Ultrathin-Body SOI MOSFET for Deep-Sub-Tenth Micron Era," in *IEEE Electron Device Letters*, vol. 21, pp. 254-255, 2000

[4] B. Doris, M. Ieong, T. Kanarsky, Y. Zhang, R. A. Roy, O. Dokumaci, Z. Ren, F. F. Jamin, L. Shi, W. Natzlem, H. J. Huang, J. Mezzapelle, A. Mocuta, S. Womack, M. Gribelyuk, E. C. Jones, R. J. Miller, H-S P. Wong, and W. Haensch, "Extreme Scaling with Ultra-Thin Si Channel MOSFETs," in *IEDM Tech. Dig.*, pp. 267-270, 2002

[5] X. Huang, W. C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y. K. Choi, K. Asano, V. Subramanian, T. J. King, J. Bokor, and Chemming Hu, "Sub 50-nm FinFET: PMOS," in *IEDM Tech. Dig.*, pp. 67-70, 1999

[6] B. S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios and R. Chau, "High Performance Fully-Depleted Tri-Gate CMOS Transistors," in *IEEE Electron Device Letters*, vol.24, pp. 263-265, 2003

[7] F. L. Yang, H. Y. Chen, F. C. Chen, C. C. Huang, C. Y. Chang, H. K. Chiu, C. C. Lee, C. C. Chen, H. T. Huang, C. J. Chenm H. J. Tao, Y. C. Yeo, M. S. Liangm and Chenming Hu, "25 nm CMOS Omega FETs," in *IEDM Tech. Dig.*, pp. 255-258, 2002

[8] K. H. Yeo, S. D. Suk, M. Li, Y. Y. Yeoh, K. H. Cho, K. H. Hong, S. Yun, M. S. Lee, N. Cho, K. Lee, D. Hwang, B. Park, D. W. Kim, D. Park, and B. I. Ryu, "Gate-All-Around(GAA) Twin Silicon Nanowire MOSFET (TSNWFET) with 15 nm Length Gate and 4 nm Radius Nanowires, " in *IEDM Tech. Dig.*, 2006

[9] W. Tsai, L. –A. Ragnarsson, L. Pantisano, P. J. Chen, B. Onsia, T. Schram, E. Cartier, A. Kerber, E. Young, M. Caymax, S. De Gendt, and M. Heyns, "Performance comparison of sub 1 nm supptered TiN/HfO_2 nMOS and pMOSFETs," in *IEDM Tech. Dig.*, pp. 311-314, 2003

[10] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M.Brazier, M. Buehler, A. Cappellani, R. Cham, C.-H. Choi, G. Ding, K. Fischer, I. Ghari, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Lin, J. Maiz, B. McIntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, I. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Ihomas, I. Inoeger, P. Vandervoom, S. Williams, and K. Zawadzki, "A 45nm Logic Technology with High-k + Metal Gate Transistors, Stained Silicon, 9 Cu Interconnect Layers, 193 nm Dry Patterning, and 100% Pb-free Packaging," in *IEDM Tech. Dig.*, pp. 247-250,2007

[11] S. Veeraraghavan and J. G. Fossum, "Short-Channel Effects in SOI MOSFET's," in *IEEE Transactions on Electron Devices*, vol. 36, pp. 522-528, 1989

[12] K. Uchida, J. Koga, R. Ohba, T. Numata, and S. Takagi, "Experimental Evidences of Quantum-Mechanical Effects on Low-filed Mobility, Gate-channel Capacitance, and Threshold Voltage of Ultrathin Boby SOI MOSFETs," in *IEDM Tech. Dig.*, pp. 633-636, 2001

[13] R. Chau, J. Kavalieros, B. Doyle, A.Murthy, N. Paulsen, D. Lionberger, D. Barlage, R. Arghavani, B. Roberds, and M. Docy, "A 50nm Depleted-Subtrate CMOS Transistor (DST)," in *IEDM Tech. Dig.*, pp. 621-624, 2001

[14] V. Trivedi, J. G. Fossum, and M. M. Chowdhury, "Nanoscale FinFETs with Gate-Source/Drain Underlap," in *IEEE Transactions on Electron Devices*, vol. 52, pp. 56-62, 2005

[15] J. W. Yang and J. G. Fossum, "On the Feasibility of NAnoscale Tri-Gate CMOS Transistors," in *IEEE Transactions on Electron Devices*, vol.52, pp. 1159-1164, 2005

[16] S. Thompson, P. Packan, T. Ghani, M. Alavi, I. Post, S. Tyagi, S. Ahmed, S. Yang, and M. Bohr, "Source/Drain Extension Scaling for 0.1μm and Below Channel Length MOSFETs," in *Symposium on VLSI Technology Dig. Tech. Papers*, pp. 132-133, 1998

[17] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices.* Cambridge, UK: Cambridge Univ., 1998

[18] J. M. Larson and J. P. Snyder, "Overview and Status of Metal S/D Schottky-Barrier MOSFET Technology," in *IEEE Transactions on Electron Devices*, vol. 53, pp. 1048-1058, 2006

[19] S. Xiong, T. J. King, and Jeffrey Bokor, "A Comparison Study of Symmetric Ultrathin-Body Double-Gate Devices With Metal Source/Drain and Doped Source/Drain," in *IEEE Transactions on Electron Devices,* vol. 52, pp. 1859-1867, 2005

[20] J. R. Tucker, "Schottky Barrier MOSFETs for Silicon Nanoelectronics," in *IEEE Proceedings of Workshop on Frontiers in Electronics*, pp. 97-100, 1997

[21] M. Jang, J. Oh, S. Maeng, W. Cho, K. Kang, and K. Park, "Characteristics of Erbium-silicided n-type Schottky barrier tunnel transistors," in *Applied*

Physics Letters, vol. 83, pp. 2611-1613, 2003

[22] T. P. Lee, E. J. Lim, K. M. Tan, T. Y. Liow, G. Q. Lo, G. S. Samudra, D. Z. Chi, and Y. C. Yeo, "N-channel FinFETs with 25-nm Gate Length and Schottky-Barrier Source and Drain Featuring Ytterbium Silicide", in *IEEE Electron Device Letters* vol. 28 pp. 164-167, 2007

[23] D. Connelly, C. Faulkner, D. E. Grupp, and J. S. Harris, "A New Route to Zero-Barrier Metal Source/Drain MOSFETs", in *IEEE Transactions on Nanotechnology* vol.3 pp. 98-104, 2004

[24] H. C. Lin, M. F. Wang, C. Y. Lu and T. Y. Huang, "Ambipolar Schottky barrier silicon-on-insulator metal-oxide-semiconductor transistors," in *Solid-State Electronics*, vol. 47, pp. 247-251, 2003

[25] A. Kinoshita, Y. Tsuchiya, A. Yagishita, K. Uchida, and J. Koga, "Solution for High-Performance Schottky-Source/Drain MOSFETs: Schottky Barrier Height Engineering with Dopant Segregation Technique," in *VLSI Tech. Digest of Tech.*, pp. 168-169, 2004

[26] A. Kinoshita, C. Tanaka, K. Uchida and J. Koga, "High-Performance 50-nm-Gate-Length Schottky-Source/Drain MOSFETs with Dopant-Segregation Junctions," in *VLSI Tech. Digest of Tech.*, pp. 158-159, 2005

[27] Z. Qiu, Z. Zhang, M. Ostling and S. L. Zhang, "A Comparative Study of Two Different Schemes to Dopant Segregation as NiSi/Si and PtSi/Si Interfaces for Schottky Barrier Height Lowering, " in *IEEE Transactions on Electron Devices*, vol. 55, pp. 396-403, 2008

[28] B. Y. Tsui and C. P. Lin, "A Novel 25-nm Modified Schottky-Barrier FinFET With High Performance," in *IEEE Electron Device Letters*, vol. 25, pp. 430-432, 2004

[29] Z. Zhang, Z. Qiu, R. Liu, M. Ostling, and S. L. Zhang, " Schottky-Barrier Height Tuning by Means of Ion Implantation Into Preformed Silicide Films Followed by Drive-In Anneal," in *IEEE Elelctron Device Letters*, vol. 28, pp. 565-568, 2007

[30] B. Y. Tsui and C. P. Lin, "Process and Characteristics of Modified Schottky Barrier (MSB) p-Channel FinFETs," in *IEEE Transactions on Electron Devices*, vol. 52, pp. 2455-2462, 2005

[31] K. K. Ng and W. T. Lynch, "Analysis of the Gate-Voltage Dependent Series Resistance of MOSFETs", in *IEEE Transactions on Electron Device* vol.ED-33 pp. 965-972, 1986

[32] S. D. Kim, C. M. Park, and J. C. S. Woo, "Advanced Model and Analysis of Series Resistance for CMOS Scaling Into Nanometer Regime-Part : Quantitative Analysis," in *IEEE Transactions on Electron Devices*, vol. 49, pp. 467-472, 2002

[33] R. S. Shenoy and K. C. Saraswat, "Optimization of Extrinsic Source/Drain Resistance in Ultrathin Body Double-gate FETs," in *IEEE Transactions on Nanotechnology*, vol.2, pp. 265-270, 2003

[34] A. Hokazono, K. Ohuchi, K. Miyano, I. Mizushima, Y. Tsunashima, and Y. Toyoshima, "Source/Drain Engineering for Sub-100 nm CMOS Using Selective Epitaxial Growth Technique", in *IEDM Tech. Dig.,* pp. 243-246, 2000

[35] H. Wakabayashi, T. Tatsumi, N. Ikarashi, M. Oshida, H. Kawamoto, N. Ikezawa, T. Lkezawa, T. Yamamoto, M. Hane, Y. Mochizuki, and T. Mogami, "Improved Sub-10-nm CMOS Device with Elevated Source/Drain Extensions by Tunneling Si-Selective-Epitaxial-Growth", in *IEDM Tech. Dig.,* pp. 145-148, 2005

[36] Z. Zhang, S. Zhang and M. Chan, "Self-Aligned Recessed Source Drain Ultrathin Body SOI MOSFET", in *IEEE Electron Device Letters* vol. 25 pp. 740-742, 2004

[37] C. G. Ahn, W. J. Cho, K. Im, J. H. Yang, I. B. Baek, S. Baek, and S. Lee, "30-nm Recessed S/D SOI MOSFET with an Ultrathin Body and a Low SDE Resistance", in *IEEE Electron Device Letters* vol. 26, pp. 486-488, 2005

[38] M. Ozturk, J. Liu and H. Mo, "Low Resistivity Nickel Germanosilicide Contacts to Ultra-Shallow $Si_{1-x}Ge_x$ Source/Drain Junctions for Nanoscale CMOS," in *IEDM Tech. Dig.*, pp. 375-378, 2003

[39] J. Liu and M. Ozturk, "Nickel Germanosilicide Contacts Formed on Heavily Boron Doped $Si_{1-x}Ge_x$ Source/Drain Junctions for Nanoscale CMOS," in *IEEE Transactions on Electron Devices*, vol. 52, pp. 1535-1540, 2005

[40] S. E. Thpmpson, M. Armstrong, C. Auth, M. Alavi, M. buehler, R. Chau, "A 90-nm Logic Technology Featuring Strained-Silicon" in *IEEE Transaction on Electron Devices*, vol 51, pp. 1-8, 2004

[41] *Sentaurus-TCAD Mannuls*

[42] S. T. Hsu, "A Simple Method to Determine Series Resistance and k Factor of an MOS Field Effect Transistor," in RCA Review, vol. 44, pp.424-429, 1983

[43] T. F. Lei, L. Y. Leu and C. L. Lee, "A Vertical Test Structure for Measuring the True Specific Contact Resistivity," in *IEEE Electron Device Letters,* pp. 259-261, 1986

[44] E. Dubois and G. Larrieu, "Low Schottky barrier source/drain for advanced MOS architecture: device design and material considerations," in *Solid-State Electronics*, pp. 997-1004, 2002

[45] B. Y. Tsui and C. P. Lu, "Current Transport Mechanisms of Schottky Barrier and Modified Schhottky Barrier MOSFETs," in *ESSDR conference*, 2007

[46] J. Suiik, P. Olivo, and B. Riccb, “Quantum-Mechanical Modeling of Accumulation Layers in MOS Structure,” in *IEEE Transactions on Electron Devices*, vol. 39, pp. 1732-1739, 1992

個人簡歷

姓名： 劉筱函

出生年月日： 民國 73 年 2 月 8 日

籍貫：台灣/苗栗縣

住址：苗栗縣公館鄉中義村 10 鄰 228-13 號

學歷：

新竹市立女子中學 (88.9-91.6)

國立交通大學電子工程學系 (91.9-95.6)

國立交通大電子所碩士 (95.9-97.7)

碩士論文題目：

修正蕭基位障電晶體之源極/汲極阻抗分析

Analysis of Source/Drain Resistance of Modified Schottky Barrier (MSB) FETs