國 立 交 通 大 學

電 子 工 程 學 系 電 子 研 究 所

碩 士 論 文

閘極直接穿隧及邊緣直接穿隧實驗施於有縱向及橫向應力N-型通道金氧半場效電晶體

Gate Direct Tunneling and Edge Direct Tunneling Experiment in n-MOSFETs under Longitudinal and Transverse Stress

研 究 生：梁惕華 Ti-Hua Liang

指導教授：陳明哲 Prof. Ming-Jer Chen

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Institute of Electronics

National Chiao Tung University

Abstract

This thesis investigates the conduction-band electron direct tunneling current through the 1.1 nm gate oxide of n-MOSFETs transistors that undergo transverse and longitudinal stress via a layout technique. By means of the triangular potential based quantum simulator (TRP), with known process parameters and published deformation potential constants as input, fitting of measured direct tunneling current versus gate voltage leads to the quantity of the channel stress. To examine the accuracy of the method, a link with the mobility measurement on the same device is conducted. The extracted stress is in good agreement with that of the direct tunneling, and therefore the experimental data are further utilized to extract the source/drain series resistance. Relating this external resistance to the dopant diffusivity under various stress conditions can lead to the activation energy per strain.

To reconfirm the validity of the above approach, the TRP simulator is again modified to deal with the edge direct tunneling counterpart. The resulting measurement data in the accumulation region furnishes the quantified gate-to-source/drain-extension overlap length. A retarded dopant diffusion phenomenon is straightforwardly observed. The corresponding strain-induced activation energy is then determined and is shown to be in good agreement with the extracted value obtained earlier. A physically oriented analytical model is therefore reached concerning the strain altered dopant diffusion.

研究生：梁惕華　　　　　　　　　　　　指導教授：陳明哲博士

國立交通大學

電子工程學系電子研究所

摘要

本文研究電子自一個閘極氧化層厚度 1.1 奈米之 N-型通道金氧半場效電晶體，因爲電路佈局而產生橫向及縱向應力之下之穿隧效應。藉由三角位能井模擬器 (TRP Simulator)，並由已刊出文獻取得重要的應力物理參數，可將實驗測得之穿隧效應電流和對應閘極電壓之間萃取出橫向及縱向應力。爲了檢驗上述方法之精確度，元件的載子遷移率被同時量測，並依此萃取得到和前述方法相一致之應力。接著，本文將不同應力下之源極、汲極電阻值的變化，與擴散係數做聯結，得到單位應變之活化能。

爲了再證實本文之萃取方法之可靠度，藉由些微修正三角位能井模擬器，可以模擬由閘極穿隧至源極及汲極之邊緣電流 (EDT)，並可以藉此萃取出閘極與源極或汲極間之疊合處長度，觀察到摻雜載子擴散遲延的效應。最後，單位應變之活化能再次被萃取，並和先前的萃取數值吻合，再次驗證了本文方法之可靠度。一個以物理爲導向之可解析模擬器也在此被提出。

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Chapter 1 Introduction

Due to the aggressive downscaling of CMOS technology, shallow trench isolation (STI) induced mechanical stress can significantly alter many electrical properties such as hot carrier immunity [1], mobility [2-10], and gate direct tunneling current [5,10,11,15,17]. As a result, the capability of quantitatively determining the magnitude of the underlying mechanical stress as well as its status (compressive or tensile) is crucial. Three fundamentally different methods have been introduced in this direction: 1) wafer bending jig [18]; 2) sophisticated stress simulation [24]; and 3) the Raman spectroscopy [25]. Obviously, the electrical approach to mechanical stress determination was lacking to date. However, it is noteworthy that the gate direct tunneling current has been well studied under externally applied mechanical stress [15]. Therefore, with the well known deformation potential constants, it is plausible to measure mechanical stress by means of the gate direct tunneling current. Both experiment work and numerical stimulations have been conducted to extract the magnitude of the STI stress and to confirm our results by further extracting the dopant diffusion activation energy per strain.

In this thesis, we consider stresses acting in parallel and perpendicular to the channel direction, different from most studies primarily focusing on uniaxial and biaxial stress MOSFET devices [4]. Moreover, the ability to trace the electrical measurements on the formed device back to the stress-related dopant diffusion in the manufacturing process is also essential. Traditionally, this was done with the aid of the TCAD method [20],[26]. In this thesis, we also present the electrical approach to find the local mechanical stress around the source/drain extension of longitudinal and

transverse stress n-MOSFETs. Straightforwardly, the underlying lateral diffusion can be determined, following by the confirmative evidence through the extra extraction of the activation energy.

Chapter 2 Stress Extraction

Section 2.1 Device Under Study

The n^+ poly-silicon gate n-MOSFETs were fabricated in a state-of-the-art manufacturing process. Three key process parameters obtained by the capacitance-voltage (C-V) fitting are as follows: n^+ poly-silicon doping concentration = $5\times10^{19}\,cm^{-3}$, gate oxide thickness = $1.1\ nm$, and substrate doping concentration = $3\times10^{17}\,cm^{-3}$. A layout technique was utilized to produce a variety of stress in terms of the gate edge to STI sidewall spacing, designated as a, with three values of 10, 2.4, and 0.21 μm.

In this thesis, different devices were characterized, for gate length L of 1 μm and 0.08 μm, and gate width W of 10 μm and 1 μm. One of the device, with a gate edge to STI spacing of 10 μm, is chosen as the reference due to the large values of both the gate edge to STI spacing and the gate width, indicating that the transverse and longitudinal stresses on the silicon lattice are negligible. For other devices , with the comparable gate width and gate length and gate to STI spacing of 10, 2.4, and 0.21 μm, the transverse ($\langle 1\bar{1}0\rangle$) and longitudinal stress ($\langle 110\rangle$) induced by the shallow trench isolation (STI) are nonnegligible. Table.I. lists the dimensions of the these devices along with the components of the stresses that must be considered. The cross symbol means that the stress component is negligible, whereas for the circle symbol the stress component needs to be taken into account.

The relative orientation direction between the silicon lattice and the stress applied

by the STI is depicted in Fig. 1, with transverse stress applied normal to the channel length direction and the longitudinal stress parallel to the channel length direction. Considering the transverse and longitudinal stress individually, we are able to further decompose the underlying stress into different components acting on each of the surface of the silicon lattice, as shown in Fig. 2.

In this thesis, the transverse and longitudinal stress are applied along the diagonal of the lattice structure, causing a change of 45 degree angle between the applied stress direction and the silicon lattice plane. At the mechanical equilibrium, we can subsequently construct a set of stress tensor component, by means of dividing the silicon lattice into four parts and hence analyze the stress components acting on each of the silicon lattice plane independently.

A mathematical approach to constructing the stress tensors are introduced in Fig. 3 and Fig. 4. The result can be written as follows:

$$\begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \tau_{yz} \\ \tau_{zx} \\ \tau_{xy} \end{bmatrix} = \begin{bmatrix} \sigma_{long}/2 \\ \sigma_{long}/2 \\ 0 \\ 0 \\ 0 \\ \sigma_{long}/2 \end{bmatrix} + \begin{bmatrix} \sigma_{tran}/2 \\ \sigma_{tran}/2 \\ 0 \\ 0 \\ 0 \\ -\sigma_{tran}/2 \end{bmatrix} = \begin{bmatrix} (\sigma_{long}+\sigma_{tran})/2 \\ (\sigma_{long}+\sigma_{tran})/2 \\ 0 \\ 0 \\ 0 \\ (\sigma_{long}-\sigma_{tran})/2 \end{bmatrix} \quad (1)$$

where $\sigma_{xx}, \sigma_{yy}, and\ \sigma_{zz}$ are the normal stress components acting on the faces perpendicular to the x, y and z direction respectively, and $\tau_{xy}, \tau_{yz}, and\ \tau_{zx}$ are the shear stress components oriented on the y, z, and x direction with normal to the x, y and z direction, respectively. $\sigma_{long}\ and\ \sigma_{trsn}$ are the applied longitudinal and

transverse stress, respectively.

Section 2.2 The TRP Simulator

The TRP simulator was constructed to quantify the direct tunneling current density on the basis of the triangular potential approximation in the channel, taking into account the poly-silicon depletion [12]. A good starting point to understand the band splitting induced by strain or stress is from the aspect of broken symmetry. Due to the commutation between operations and crystal Hamiltonian , symmetry plays a vital role in determining the band structure. The longitudinal and transverse compressive stress breaks the symmetry on the x-y plane where the channel lies such that the x-y plane is only symmetrical with respect to the two $\langle 110 \rangle$ diagonals.

The conduction band shifts are well defined in the literature[10-13] , and by means of a slight modification, the conduction energy shift for silicon under longitudinal stress σ_{long} and transverse stress σ_{tran} in the reciprocal space along $[100]$, $[\bar{1}00]$, $[010]$, and $[0\bar{1}0]$ directions can be written as:

$$\Delta E_C = \Xi_d (S_{11} + 2S_{12})(\sigma_{long} + \sigma_{tran}) + \Xi_u \left(\frac{S_{11} + S_{12}}{2} \right)(\sigma_{long} + \sigma_{tran}) = 2.922 \times 10^{-11} (\sigma_{long} + \sigma_{tran})(eV) \quad (2)$$

and

$$\Delta E_C = \Xi_d (S_{11} + 2S_{12})(\sigma_{long} + \sigma_{tran}) + \Xi_u (S_{12})(\sigma_{long} + \sigma_{tran}) = -1.576 \times 10^{-11} (\sigma_{long} + \sigma_{tran})(eV) \quad (3)$$

for $[001]$ and $[00\bar{1}]$ directions.

Therefore, we can show that strain alters the subband levels in the 2D confinement region by the following expressions [10-13]:

$$E_{\Delta 2}=\left(\frac{9hqE_{eff,\Delta 2}}{16\sqrt{2m_{\Delta 2}^{*}}}\right)^{\frac{2}{3}}+\left(\Xi_{d}+\frac{\Xi_{u}}{3}\right)(S_{11}+2S_{12})(\sigma_{long}+\sigma_{tran})+\left(\frac{\Xi_{u}}{3}\right)(S_{12}-S_{11})(\sigma_{long}+\sigma_{tran}) \quad (4)$$

$$E_{\Delta 4}=\left(\frac{9hqE_{eff,\Delta 4}}{16\sqrt{2m_{\Delta 4}^{*}}}\right)^{\frac{2}{3}}+\left(\Xi_{d}+\frac{\Xi_{u}}{3}\right)(S_{11}+2S_{12})(\sigma_{long}+\sigma_{tran})-\left(\frac{\Xi_{u}}{6}\right)(S_{12}-S_{11})(\sigma_{long}+\sigma_{tran}) \quad (5)$$

where $E_{\Delta 2}$ and $E_{\Delta 4}$ denote the energy levels for the Δ_2 and Δ_4 valley ewspectively, the quantization effective masses are $m_{\Delta 2}^{*}=0.92m_o$ and $m_{\Delta 4}^{*}=0.19m_o$, and the elastic compliance constants are $S_{11}=7.68\times10^{-12}\left(m^2/N\right)$ and $S_{12}=-2.14\times10^{-12}\left(m^2/N\right)$. The hydrostatic and shear deformation potential constants $\Xi_d=1.13eV$ and $\Xi_u=9.16eV$, which are close to those in [15], were cited here. A qualitative schematic of the electron direct tunneling process and subband splitting for n-MOSFET is shown in Fig. 5.

Compressive stress from both the longitudinal and transverse direction causes the repopulation of the electrons, decreasing the electron density and Si/SiO_2 barrier height in the Δ_2 valley, while increasing the electron density and Si/SiO_2 barrier height in the Δ_4 valley [7]. Note from the expression listed above that the change in the conduction band energy may cause the strain altered gate leakage.

Sketched in Fig.6 (a) and (b) is the band structure for silicon, which are ellipsoids of constant electron energy in reciprocal space, each corresponding to one of the degenerate conduction band valleys. In this thesis, quantum confinement and stress both enhance the degeneracy between the four in-plane valleys(Δ_4) and the two out-of- plane valleys (Δ_2) owing to energy splitting. Compressive stress decreases the electron population in the Δ_2 valley due to a higher out-of-plane mass and a significantly longer lifetime compared to the Δ_4 valley, resulting in an increased

electron tunneling current [5].

The electron direct tunneling current density can be modeled by the TRP simulator. First of all, the potential drop due to poly depletion is determined through the following expression [10]: $V_{poly} = \varepsilon_{ox}^2 F_{ox}^2 / 2q\varepsilon_{si} N_{poly}$, and the substrate band bending can be written as $V_s = |V_G - V_{FB}| - V_{poly} - V_{ox}$, where V_G is the applied gate voltage, V_{FB} the flat band voltage , V_{ox} the oxide potential drop, and V_{poly} the potential drop in the n^+ poly-silicon region. The reference point of this model is the conduction band edge of the Δ_4 subband. Therefore , the tunneling barrier at the cathode-side interface and the relative positions of the Δ_2 and Δ_4 subbands can be defined as [14]:

$$\phi_{BC}(\text{stressed}) = \phi_{BC}(unstressed) - E_{d4} \tag{6}$$

$$E_{\Delta 2}(stressed) = E_{\Delta 2}(unstressed) + E_{d2} - E_{d4} \tag{7}$$

$$E_{\Delta 4}(stressed) = E_{\Delta 4}(unstressed) \tag{8}$$

where

$$\phi_{BC}(unstressed) = 3.15\text{eV} \tag{9}$$

$$E_{d2} = \left(\Xi_d + \frac{\Xi_u}{3}\right)(S_{11} + 2S_{12})(\sigma_{long} + \sigma_{tran}) + \left(\frac{\Xi_u}{3}\right)(S_{12} - S_{11})(\sigma_{long} + \sigma_{tran}) \tag{10}$$

$$E_{d4} = \left(\Xi_d + \frac{\Xi_u}{3}\right)(S_{11} + 2S_{12})(\sigma_{long} + \sigma_{tran}) - \left(\frac{\Xi_u}{6}\right)(S_{12} - S_{11})(\sigma_{long} + \sigma_{tran}) \tag{11}$$

The change in the energy bandgap is then considered:

$$E_g(stress) = E_g(unstress) + \Delta E_{V1} + \Delta E_{d4} \quad (12)$$

Fig. 7 presents the band diagram when the cathode side is stressed, whereas no stress is applied on the cathode-side. Taking into consideration that the n^+ poly-silicon region is also stressed, as depicted in Fig. 8, the electron group velocity normal to the interface in the anode-side should also be modified. By modeling the energy band as parabolic one, we can compare the relative energy shifts on both sides of the silicon oxide to derive electron group velocity normal to the interface on both the anode and cathode sides. The modifications in the following expressions alter the correction factors in our TRP simulator and thus change the transmission probability [14].

The normal component of electron group velocity on both the anode and cathode sides are listed below:

$$\mathrm{V_{Si}}(cath) = \frac{\sqrt{2E_{su}(cath)}}{m_Z}, \mathrm{V_{Si}}(An) = \frac{\sqrt{2E_{su}(An)}}{m_Z} \quad (13)$$

where $\mathrm{E}_{si}(Cath) = \left(E_{\Delta 2}(unstressed) - (\Delta E_{d2} - \Delta E_{d4})\right)$ (14)

$$\mathrm{E}_{si}(An) = \left(E_{\Delta 2}(unstressed) - (\Delta E_{d2} - \Delta E_{d4})\right) + \left(\Delta E_{d2} - \Delta E_{d2}'\right) + qV_{ox} \quad (15)$$

$$m_Z = 0.91 m_0 \quad \text{for} \quad \Delta_2 \text{ valley} \quad (16)$$

$$\mathrm{E}_{si}(Cath) = \left(E_{\Delta 4}(unstressed)\right) \quad (17)$$

$$\mathrm{E}_{si}(An) = \left(E_{\Delta 4}(unstressed)\right) + \left(\Delta E_{d4} - \Delta E_{d4}'\right) + qV_{ox} \quad (18)$$

$$m_Z = 0.19 m_0 \quad \text{for} \quad \Delta_4 \text{ valley} \quad (19)$$

the primed and unprimed symbols represent the energy shift in the n^+ poly-silicon region and the underlying substrate region, respectively.

It is now a straightforward task to calculate the electron direct tunneling current density. If all the subband energy levels are determined, then the inversion-layer carrier density per unit area can be expressed as [10-11],[13-15]

$N_i = \left(\frac{K_B T}{\pi\hbar^2}\right) g_i m_{di} \ln\left(1 + \exp\left(\left(E_f - E_i\right)/K_B T\right)\right)$, where the subscript i denotes Δ_2 and Δ_4, $K_B T$ is the thermal energy, g_i is the degeneracy of the valley, and m_{di} is the density of state effect mass. Then, by relating the boundary conditions between the oxide and silicon surface, the charge conservation relationship $q\left(N_S + N_{depl}\right) \approx \varepsilon_{ox} F_{ox}$ [10],[12] can be established. From now on, it is the TRP simulator that employs an iteration procedure to select the appropriate oxide field value to meet the above expression. The flowchart of the TRP simulator is drawn in Fig. 9.

Section 2.3 Stress Extraction via TRP simulator

After determining the relative positions on each of the two subbands and the Fermi level, the inversion-layer carrier density per unit area can be calculated. The Wentzel-Kramers-Brillouin tunneling probability, taking into account the corrections for reflections from the potential discontinuity is conducted [14]. Note that the electron dispersion relationship is used with $m_{ox} = 0.61 m_o$ for the tunneling electrons in the oxide in the context of the Franz-type dispersion. Consequently, the electron direct tunneling current density can be calculated as a function of stress [10],[15].

$$J_g\left(\sigma_{long}, \sigma_{tran}\right) = \frac{qN_{\Delta 2}\left(\sigma_{long}, \sigma_{tran}\right)}{\tau_{\Delta 2}\left(\sigma_{long}, \sigma_{tran}\right)} + \frac{qN_{\Delta 4}\left(\sigma_{long}, \sigma_{tran}\right)}{\tau_{\Delta 4}\left(\sigma_{long}, \sigma_{tran}\right)} \qquad (20)$$

where σ_{tran} is a fixed value in our experiment, the $\tau_{\Delta 2}$ and $\tau_{\Delta 4}$ are the tunneling lifetime for Δ_2 and Δ_4 valley , respectively.

The gate direct tunneling current was measured in inversion conditions, with the source, drain, and substrate all tied to the ground. The simultaneously measured valance-band electron tunneling counterpart or equivalently the substrate hole current was found to be unchanged, regardless of stress [10]. This indicates that the gate oxide thickness under study remains constant. And the change of the conduction-band electron direct tunneling at $V_G = 1V$, all with respect to W=10 μm, L=1 μm, and a=10 μm is then measured.

With the above method, the transverse stress can be extracted by comparing W=10 μm, L=1 μm, and a=10 μm with W=1 μm, L=0.08 μm, and a=10 μm. The longitudinal stress for the device W=1 μm, L=0.08 μm can also be extracted . Fig. 10 shows the corresponding electron direct tunneling current change versus longitudinal stress under various transverse stress conditions.

The resulting gate current change versus the extracted channel stress is plotted in Fig. 11 for gate voltage of 1V. It is noteworthy that the magnitude of the gate current increases with the applied longitudinal stress. This phenomenon reveals the fact that as the source/drain diffusion length decreases, the STI approaches closer to the MOSFET core region and thus increases the magnitude of compressive stress.

Section 2.4 Confirmative Evidence for the Extracted Stress

The mobility reduction under compressive stress mainly comes from the citation [5],[7]: Firstly, conductivity mass (the effective mass along $\langle 110 \rangle$) increases due to electrons repopulation from Δ_2 to Δ_4 valleys. The electron mobility partly decreases via a enhanced out of plane mass due to the unfavorable mass of the Δ_2 valley, which results in fewer electrons with the in-plane transverse effective mass and out-of- plane longitudinal mass. Secondly, intrinsic scattering is enhanced due to the splitting-induced DOS increase. Finally, conductivity mass (unstressed: $m_t = 0.19 m_o, m_l = 0.98 m_o$) increases due to changes of the energy versus k-space curvature, named the band warping.

To furnish the confirmative evidence for our extracted longitudinal stress, numerous tasks must to be done. The most effective approach is to evaluate strain-altered mobility through the empirically determined piezoresistance coefficient, which has the benefit of capturing mobility reduction or enhancement on the basis of the changes in conductivity mass. To date , bulk piezoresistance coefficients have significantly been favored although essentially piezoresistance of MOSFETs from inversion-layer quantization should be used [5].

The mechanical stress effect on mobility is expressed as follows[5],[8],[18]: $\Delta\mu/\mu \approx \pi_{//}\sigma_{//} + \pi_{\perp}\sigma_{\perp}$, where $\Delta\mu/\mu$ is the fraction change in mobility, $\sigma_{//}$ *and* $\sigma_{\perp}$ are the longitudinal and transverse stress, respectively. $\pi_{//}$ *and* $\pi_{\perp}$ are the longitudinal and transverse piezoresistance coefficients expressed in Pa^{-1}, respectively.

S.Suthram , et al. [18] has shown that the piezoresistance coefficient for short devices only remains constant when a correction of the parasitic source/drain series

resistance (R_{sd}) has been taken into consideration. Therefore, a constant-mobility method to enable MOSFET series-resistance extraction was applied. D. W. Lin , et al. [19] demonstrated that when different back- bias conditions are used on the same MOSFET device, the inversion carrier mobility converges to single curve when the effective silicon vertical electrical field is sufficiently high. In consequence, comparing the same device operating in linear region with two different back biases, $V_B = 0V \ and \ V_B = -0.4V$,we are able to extract the parasitic source/drain series resistance. The mobility was then modified by using the following expression:

$$\mu' = \mu(V_{ds})/(V_{ds} - (Rsd/W)I_d) \tag{21}$$

where μ' denotes the modified mobility.

The modified mobility change versus extracted stress is shown in Fig. 12, with the piezoresistance coefficients of

$\pi_{//} = -31.6\times10^{12} dyn^{-1}cm^2$、$\pi_{\perp} = -17.6\times10^{12} dyn^{-1}cm^2$.

With the transverse stress fixed to value of -300MPa (Section 2.3), we can further extract another set of longitudinal stress for gate to STI spacing values. Illustrated in Fig. 13 is the comparison of our two stress extraction approaches, one from the stress induced electron direct tunneling current change and the other from the piezoresistance coefficient extraction.

With the above method , the transverse stress extracted by comparing W=10 μm,L=1 μm, and a=10 μm with W=1 μm,L=0.08 μm, and a=10 μm is around -300MPa. The longitudinal stress for the device W=1 μm and L=0.08 μm is around 0, -50MPa, and -310Mpa for a gate-to-STI spacing of 10 μm,2.4 μm, and 0.21 μm, respectively.The results are quantitatively consistent with each other. Therefore, the

validity of our methodology has been corroborated.

Chapter 3 Extraction of Activation Energy

Section 3.1 Strain Induced Dopant Diffusion

In the present paper [20] , dopant impurities introduced to form n-MOSFETs are boron, indium, arsenic and phosphorus. Extraction of parasitic source/drain series resistance implies that stress may alter the doping profiles. Specifically, most of the impurities are retarded by compressive stress.

We then seek relations between the dopant diffusivity and the activation energy per unit strain. An approach dealing with dopant diffusion dependencies on strain is briefly depicted in the following procedure. The general concept of our approach is to express dopant diffusion under mechanical stress. In the case of compressively strained silicon, the dopant diffusion dependence follows the Arrhenius form [20]:

$$D_S = D_I \exp\left(-\frac{QV}{KT}\right) \tag{22}$$

where D_S is the dopant diffusivity under strain, D_I is the dopant diffusivity without strain, V is strain volume change ratio due to stress, Q is the activation energy per volume change depending on dopant species, and T is the temperature. In our case, when the stress is small, by converting our developed stress tensor into strain tensor, the resulting matrix is shown below:

$$\begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \tau_{yz} \\ \tau_{zz} \\ \tau_{xy} \end{bmatrix} = \begin{bmatrix} \frac{\sigma}{2} \\ \frac{\sigma}{2} \\ 0 \\ 0 \\ 0 \\ \frac{\sigma}{2} \end{bmatrix} \Rightarrow \begin{bmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ \varepsilon_{yz} \\ \varepsilon_{zx} \\ \varepsilon_{xy} \end{bmatrix} = \begin{bmatrix} (S_{11}+S_{12})\frac{\sigma}{2} \\ (S_{11}+S_{12})\frac{\sigma}{2} \\ S_{12}\sigma \\ 0 \\ 0 \\ S_{44}\frac{\sigma}{4} \end{bmatrix} = \begin{bmatrix} (S_{11}+S_{12})\left(\frac{\sigma_{long}+\sigma_{tran}}{2}\right) \\ (S_{11}+S_{12})\left(\frac{\sigma_{long}+\sigma_{tran}}{2}\right) \\ S_{12}\left(\frac{\sigma_{long}+\sigma_{tran}}{2}\right) \\ 0 \\ 0 \\ S_{44}\left(\frac{\sigma_{long}+\sigma_{tran}}{4}\right) \end{bmatrix} \tag{23}$$

Then, we divide our studies into two categories:

$Case\,1: V \approx \varepsilon_{xx} + \varepsilon_{yy}$

$Case\,2: V \approx \varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{ZZ}$

Both cases neglect the volume change caused by shear stress components, assuming that all volume change is due to normal stress components. Moreover, the first case further neglects the volume change in the z direction.

Section 3.2 Extraction of Activation Energy

The general form of the diffusivity for a dopant A is:

$$D_A = D_{AX^0} + D_{AX^+}(P/n_i) + D_{AX^-}(n/n_i) + D_{AX^=}(n/n_i)^2 \quad (24)$$

Where each diffusion component has a pre-exponential factor and activation energy of diffusion such as $D_{AX^0} = D^0 \exp(-E^0/KT)$. The diffusivity of phosphorous and arsenic is shown in the following:

$$D_{As} = 8 \times \exp(4.05/KT) + 12.8 \times \exp(4.05/KT)(n/n_i) \quad (25)$$

$$D_p = 3.84 \times \exp(3.66/KT) + 4.44 \times \exp(4/KT)(n/n_i) + 44.2 \times \exp(4.37/KT)(n/n_i)^2 \quad (26)$$

Values for the diffusivity of phosphorous comes from Fair [21] , values for arsenic comes from Chin and Barbuscia [21]. The expressions for arsenic agree reasonably well with experiment, while the value for phosphorous is not as reliable due to anomalies [21].

The diffusivity of phosphorus is explained as a vacancy dominated diffusion, and in high concentration region the extrinsic diffusivity of phosphorus is given by:

$$D_P = D_P^0 + D_P^{=}\left(\frac{n}{n_i}\right)^2 \quad (27)$$

where D_P^0 is the neutral vacancy, $D_P^{=}$ is the doubly negatively charged vacancy, and n_i is the intrinsic carrier concentration. Note that in extrinsic diffusion region, such as the MOSFETs' source/drain region, the assumption is made that the diffusivity of phosphorus is essentially proportional to the square of the dopant concentration.

Arsenic, another type of impurity as mostly used in MOSFET, is believed to diffuse primarily through a vacancy mechanism with an interstitialcy component. Above approximately $1000\ ^0C$, diffusion is dominated by vacancy pairs As^+V^- with $As^+V^=$ being relatively rare to the small binding energy. The diffusivity of arsenic can be written as:

$$D_{AS} = D_{AS}^0 + D_{AS}^-\left(\frac{n}{n_i}\right) \quad (28)$$

where D_{AS}^- is the negatively charged vacancy. And in extrinsic diffusion region. The assumption is also made that the diffusivity of phosphorus is essentially proportional to the dopant concentration.

Then, given that the parasitic source/drain series resistance is inversely proportional to electron mobility and the dopant impurity concentration, we are able to relate the dopant diffusivity to the source/drain series resistance. By examining the experimental data, we found that the change in mobility is less than the change of source/drain series resistance, which implies that the stress acting on the silicon lattice not only alters the electron population in the subbands, but alters the doping profile, showing dopant diffusion retardation phenomenon. The result can be shown in Fig. 14.

Finally, the activation energy per strain is obtained. For case one, which neglects the strain in the z direction, by comparing the differences in diffusivity under different stress conditions, an analytical model can be obtained the following formula.

$$\frac{D(\varepsilon,\varepsilon')}{D(0,\varepsilon')}=\frac{\exp\left(\frac{-Q(\varepsilon+\varepsilon')}{KT}\right)}{\exp\left(\frac{-Q\varepsilon'}{KT}\right)}=\exp\left(\frac{-Q\sigma}{KT(180\times10^{9})}\right)=\frac{D(\sigma,\sigma')}{D(0,\sigma')}$$
$$\Rightarrow Q(\sigma)=-\ln\left(\frac{D(\sigma,\sigma')}{D(0,\sigma')}\right)\left(\frac{KT(180\times10^{9})}{\sigma}\right) \tag{29}$$

where ε and ε' denotes the strain induced by the longitudinal stress and transverse stress. Subsequently, case two can also be derived:

$$\frac{D(\varepsilon,\varepsilon')}{D(0,\varepsilon')}=\frac{\exp\left(\frac{-Q(\varepsilon+\varepsilon')}{KT}\right)}{\exp\left(\frac{-Q\varepsilon'}{KT}\right)}=\exp\left(\frac{-Q\sigma}{KT}\left(\frac{1}{180\times10^{9}}-\frac{1}{467\times10^{9}}\right)\right)=\frac{D(\sigma,\sigma')}{D(0,\sigma')}$$
$$\Rightarrow Q(\sigma)=-\ln\left(\frac{D(\sigma,\sigma')}{D(0,\sigma')}\right)\left(\frac{KT}{\frac{\sigma}{180\times10^{9}}-\frac{\sigma}{467\times10^{9}}}\right) \tag{30}$$

Here, a typical temperature of 1300K for the manufacturing process is used. The activation energy can hence be determined.

Chapter 4

Confirmative Evidence for Edge Direct Tunneling

Section 4.1 Edge Direct Tunneling

Direct tunneling current from the gate overlap region into the underlying source/drain extension region (also identified in current literature as edge direct tunneling or EDT) has been identified as the principal source of offstate power dissipation in state-of-the-art VLSI chips. Yang, et al. [22]. has also shown that this component of gate leakage exceeds even band-to-band tunneling (BTBT) and gate induced drain leakage (GIDL) for ultrathin gate oxide n-MOSFETs. When the gate electrode is biased negatively, the gate overlap region over the source/drain extension region immediately goes into accumulation given the fact that the flat band voltage between the heavily doped n^+ poly-Si region and the source/drain extension region is almost zero. However, the poly gate region over the p-type substrate remains in depletion until $V_g = V_{fb}$ (for the poly gate and p-type substrate).Here the flat band voltage is approximately −1.0 V. These accumulated electrons in the gate overlap region tunnel into the source/drain extension region, giving rise to the edge direct tunneling.

Section 4.2 Extraction of Activation Energy

The electron direct tunneling from the accumulated poly-silicon surface down to the underlying silicon was measured. To determine the underlying gate-to-source/drain extension overlap length where the EDT prevails, the TRP

simulator has been modified to meet our requirements. Fig. 15 shows the flow chart of the TRP simulator in case of EDT current. And the band diagram drawn along n^+ poly-gate/SiO_2/diffusion extension is shown in Fig. 16.

First of all, the potential drop due to poly depletion is determined through the following expression [22-23]: $V_{DE} = \varepsilon_{ox}^2 F_{ox}^2 / 2q\varepsilon_{si} N_{DE}$, where N_{DE} and V_{DE} are the dopant concentration and potential drop in the source/drain extension respectively. The poly gate band bending can be described as $V_{DG} - V_{FB} = V_{poly} + V_{ox} + V_{DE}$, where V_{DG} is the applied gate voltage, V_{FB} the flat band voltage, and V_{ox} the oxide potential drop. The reference point remains the same: the conduction band edge of the Δ_4 subband. The stress in the source/drain region is also considered. In the modeling processes, including the determination of the subband energy shift caused by the applied stress, the calculated inversion-layer carrier density per unit area follows that of modeling electron direct tunneling current, except that the charge conservation relationship should be rewritten as $q(N_S) \approx \varepsilon_{ox} F_{ox}$. The poly-silicon gate is now operating at accumulation region, with no depletion charge existing. Another difference is that the flat band voltage is nearly zero $V_{FB} \approx 0$ (compared with $V_{FB} = -[E_g/q + (KT/q)(N_{sub}/N_V)]$ for modeling electron direct tunneling current) and the Fermi level becomes $E_F = q(V_{poly} + V_{FB})$ (compared with $E_F = q(V_s + V_{FB})$ for modeling electron direct tunneling current).

As a result, the gate-to-source/drain overlap L_{TN} can be directly extracted [22]:

$$I_{EDT}(\sigma_{long}, \sigma_{tran}) = WL_{TN} \frac{qN_{\Delta 2}(\sigma_{long}, \sigma_{tran})}{\tau_{\Delta 2}(\sigma_{long}, \sigma_{tran})} + WL_{TN} \frac{qN_{\Delta 4}(\sigma_{long}, \sigma_{tran})}{\tau_{\Delta 4}(\sigma_{long}, \sigma_{tran})} \quad (31)$$

where W is the channel width, and $N_{\Delta 2}$ and $N_{\Delta 4}$ are the available charge in Δ_2 and Δ_4 valley for tunneling process, respecticely. The tunneling lifetime in the following equations can be connected with the transmission probability:

$$\tau_{\Delta 2} = \pi\hbar / \left(\mathrm{T}_{\Delta 2}\left(\sigma_{long}, \sigma_{tran}\right) \mathrm{E}_{\Delta 2}\left(\sigma_{long}, \sigma_{tran}\right)\right) \tag{32}$$

$$\tau_{\Delta 4} = \pi\hbar / \left(\mathrm{T}_{\Delta 4}\left(\sigma_{long}, \sigma_{tran}\right) \mathrm{E}_{\Delta 4}\left(\sigma_{long}, \sigma_{tran}\right)\right) \tag{33}$$

It is worthy to notice that with our modified TRP simulator , the retarded dopant diffusion phenomenon caused by STI stress can be systematically treated . The tunneling current density change under different stress conditions only reflects the change in the available charge for tunneling and the tunneling lifetime. However, by examining the differences between the modeling result and the experiment data, it is a straightforward task to extract the gate-to-source/drain overlap L_{TN} .

$$\frac{J_1 - J_2}{J_2} = \frac{\Delta J}{J} \tag{34}$$

The above equation represents the tunneling current density change for different stress conditions 1 and 2, as shown in Fig.17. If the retarded dopant diffusion was applied, the change in tunneling current is rewritten as:

$$\frac{J_1 W L_{TN}' - J_2 W L_{TN}}{J_2 W L_{TN}} = \frac{J_1 W L_{TN}' - J_1 W L_{TN} + J_1 W L_{TN} - J_2 W L_{TN}'}{J_2 W L_{TN}} = \frac{J_1}{J_2}\left(\frac{L_{TN} - L_{TN}'}{L_{TN}}\right) + \frac{J_1 - J_2}{J_2} \tag{35}$$

$$= \left(\frac{\Delta J}{J} + 1\right)\frac{\Delta L_{TN}}{L_{TN}} + \frac{\Delta J}{J}$$

where $\frac{\Delta J}{J}$ can be derived by the TRP stimulator, whereas $\frac{J_1 W L_{TN}' - J_2 W L_{TN}}{J_2 W L_{TN}}$ can be subsequently obtained by comparing experimental data.

Fig. 18, shows the resulting edge direct tunneling current contributed by different

subbands with gate voltage varying from -0 to -1.4 V. Fig. 19 reveals the energy level of the lowest two subbands and Fermi energy level under various gate biases. The energy level of the lowest two subbands and Fermi energy level under various stress conditions is shown in Fig. 20, which indicates a narrow in energy- level spacing between the lowest two subbands as applied stress increases. Fig.21 shows simulation results of the edge direct tunneling current contributed by each of the subband operating under different compressive stresses. Finally, the extracted gate-to-source/drain overlap L_{TN} spans a range of, 6.5nm, 6.35nm, and6.25nm for a=10 μm, 2.4 μm, and 0.21 μm, respectively. Other extractions results are shown in Fig. 22, 23 , and24.

To reconfirm our results, given that the gate-to-source/drain overlap L_{TN} is proportional to $\sqrt{Dt}$,then the diffusivity change under different stress condition $\Delta L/L = \Delta\sqrt{Dt}/\sqrt{Dt}$ is calculated. Then applying the expressions listed in section 3.1, the activation energy $Q(\sigma)$ can be reproduced. Table 2. lists of the value of the activation energy extracted by the two approaches. Approach one mainly focuses on the series-resistance change under applied stress in order to obtain the diffusivity difference, whereas approaches two aims at the gate-to-source/drain overlap difference caused by stress for the extract ion of the diffusivity change. Note that our results from the parasitic source/drain series resistance are quantitatively consistent with the gate direct tunneling mode , especially in case 2. This indicates that both the longitudinal and transverse in-plane stress to cause considerable deformation in the Z direction.

Chapter 5 Conclusion

With the known process parameters and published deformation potential constants as input, fitting of the gate tunneling current versus gate voltage data has led to the value of the underlying channel stress. By utilizing the constant mobility method, the parasitic source/drain series resistances are extracted. The increase in series resistances under high in-plane stress has revealed a dopant retarded diffusion. Moreover, the method to calculate activation energy has been illustrated. To further confirm our results, the edge direct tunneling technique has been applied, thus extracted the actual gate-to-source/drain overlap L_{TN} as well as magnitude under different stress conditions. Consequently, the activation energy has again been obtained and has matched well with that of source/drain series resistance as well as the process simulation.

Reference

[1] A. Hamada, T. Furusawa, N. Saito, and E. Takeda, "A new aspect of mechanical stress effects in scaled MOS devices," *IEEE Trans Electron Devices*, Vol. 38, No. 4, pp.895-900, April. 1991.

[2] Victor Moroz, Norbert Strecker, Xiaopeng Xu, Lee Smith, Ingo Bork, "Modeling the impact of stress on silicon process and devices", *Material Science in Semiconductor Processing*, Vol. 6, pp. 27-36, 2003.

[3] S.E Thompson, M. Armstrong, C. Auth, M. Alavi, M. Buehler, R. Chau, S. Cea, T. Ghani, G. Glass, T. Hoffman, C. H. Jan, C. Kenyon, L. Klaus, K. Kuhn, Z. Ma, B. Meintyre, K. Mistry, A. Murthy, B. Obradovic, R. Nagisetty, P. Nguyen, S. Sivakumar, R. Shaheed, L. shifren, B. Tufts, S. Tyagi, M. Bohr, and Y. E;-Mansy, "A 90-nm technology featuring strained silicon", *IEEE Trans Electron Devices* , VOL. 51 , NO. 11 , pp.1790-1791, November. 2004.

[4] S.E. Thompson, G. Sun, K. Wu., J. Lim, and T. Nishida, "Key Differences For Process induced Uniaxial vs. Substrate-induced Biaxial stressed Si and Ge Channel MOSFETs", *IEDM* , Vol. 221, 2004.

[5] Scott E. Thompson, Guangyu Sun, Youn Sung Choi, and Toshikazu Nishida, "Uniaxial-Process-Induced Strain-Si: Extending the CMOS Roadmap" , *IEEE Trans. Electron Devices* , Vol. 53 , No. 5 , May. 2006.

[6] Y.-J. Yang., W.S. Ho, and C.-F. Huang, "Electron mobility enhancement in

strained-germanium n-channel metal-oxide-semiconductor field-effect transistors" , *Appl. Phys. Lett.* , Vol. 91, 2007

[7] Y. Sun, G. Sun, S. Parthasarathy, S. E. Thompson, "Physics of process induced uniaxially strained Si" , *Materials Science and Engineering B,* Vol. 135, pp. 179-183, 2006

[8] Scott E. Thompson, Mark Armstrong, Chis Auth, Steve Cea, Robert Chau, Glenn Glass,Thomas Hoffman, Jason Klaus, Zhiyong Ma, Brian Mcintyre, Anand Murthy, Borna Obradovic, Lucian Shifren, Sam Sivakumar, Sunit Tyagi, Tahir Ghani, Kaizad Mistry, Mark Bohr, and Youssef EL-Mansy, "A Logic Nanotechnology Featuring Strained-Silicon" , *IEEE Trans Electron Devices.*, Vol. 25 , No. 4 , April. 2004.

[9] Ken Uchida, Tejas Krishnamohan, Krishna C. Saraswat, and Yoshio Nishi, "Physical Mechanisms of Electrons Mobility Enhancement in Uniaxial Stressed MOSFETs and Impact of Uniaxial Stress Engineering in Ballistic Regime, *IEEE*, 2005.

[10] Chen-Yu Hsieh, and Ming-Jer Chen , "Measurement of Channel Stress Using Gate Direct Tunneling Current in Uniaxially Stressed NMOSFETs" , *IEEE Trans. Electron Devices.*, Vol. 28 , No. 9 , September. 2007.

[11] I. Balslev, "Influence of uniaxial stress on the indirect absorption edge in silicon and germanium", *Phys. Rev.*, Vol. 143, No. 2, March. 1966.

[12] H. Hartmut Mueller and Max J. Schulz, “Simplified Method to Calculate the Band Bending and the Subband Energies in MOS Capacitors.”, *IEEE Tran. Electron Devices.*, Vol. 44 , No. 9, September. 1997.

[13] K. N. Yang, H. T. Huang, M. C. Chang, C. M. Chu, Y. S. Chen, M. J. Chen, “Model for hole direct tunneling current in P^+ poly-gate pMOSFETs with ultrathin gate oxides” , *IEEE Trans Electron Devices*, Vol. 47, No. 11, November. 2000.

[14] Leonard F. Register, “Analytic model for direct tunneling current in polycrystalline silicon-gate metal-oxide-semiconductor devices, *Appl. Phys . Lett.*,Vol. 74 , No. 3 , January. 1999.

[15] Ji-Song Lim, Xiaodong Yang, Toshijazu Nishida, and Scott E. Thompson, “Measurement of conduction band deformation potential constants using gate direct tunneling current n-type metal oxide semiconductor field effect transistors under mechanical stress” , *Appl. Phys. Lett.*, Vol. 89, pp.073509, 2006

[16] N. Yang, H. K. Henson, J. R. Hauser, and J. J. Wortman, “Modeling study of ultrathin gate oxides using direct tunneling current and capacitance-voltage measurements in MOS devices” , *IEEE Trans. Electron Devices.*, Vol. 46, No. 7, July. 1999.

[17] Xiaodong Yang, Younsung Choi, Toshikazu Nishida, and Scott. E. Thompson, “Gate Direct Tunneling in Uniaxial Stressed MOSFETS”, *IEEE*, pp.149-152, 2007.

[18] S. Suthram, J. C. Ziegert, T. Nishida, and S.E. Thompson, ”Piezoresistance Coefficient of (100) Silicon nMOSFETs Measured at Low and High(~1.5GPa) Channel Stress, *IEEE Trans. Electron Devices.*, Vol. 28, No. 1, January. 2007.

[19] Da-Wen Lin, Ming-Lung Cheng, Shyh-Wei Wang, Chung-Cheng Wu, and Ming-Jer Chen,”A Constant Mobility Method to Enable MOSFET Series-Resistance Extraction” , *IEEE Trans. Electron Devices.*, Vol. 28 ,No. 12 , December. 2007.

[20] Yi-Ming Sheu, Sheng-Jier Yang, Chih-Chiang Wang, Chih-Sheng Chang, Li-Ping Huang, Tsung-Yi Huang, Ming-Jer Chen, and Carlos H. Diaz, ,”Modeling Mechanical Stress Effect on Dopant Diffusion in Scaled MOSFETS”, *IEEE Trans. Electron Devices.*, Vol. 52, No. 1, January. 2005.

[21] P.M Fahey, P. B. Griffin, and J. D. Plummer, “Points defects and dopant diffusion in silicon”, *Reviews of Modern Physics.*, Vol. 61 , No. 2, April. 1989.

[22] K.N. Yang, H, T. Huang, M.J. Chen , Senior Menber, IEEE, Y. M. Lin, M. C. Yu, S. M. Jang, Douglas C. H. Yu, and M. S. Liang, “Characterization and Modeling of Edge Direct Tunneling (EDT) Leakage in Ultrathin Gate Oxide MOSFETS” , *IEEE Trans. Electron Devices.*, Vol. 48, No. 6, June. 2001.

[23] Chen-Yu Hsieh, and Ming-Jer Chen,”Electrical Measurement of Local Stress and lateral Diffusion Near Source/Drain Extension Corner of Uniaxially Stress n-MOSFETs”, *IEEE Trans. Electron Devices.*, Vol. 55, NO. 3, March. 2008.

[24] R.A. Bianchi, G. Bouche, and O. Roux-dit-Buisson, "Accurate modeling of trench isolation induced mechanical stress on MOSFET electrical performance "in *IEDM Tech. Dog.*, pp.1254-1261, 2002.

[25] I.D. Wolf," Micro-Ramam spectroscopy to study local mechanical stress in silicon integrated circuits." *Semicond. Sci. Technol.*, Vol. 11, No.2, pp.139-154, February. 1956

[26] M.J. Chen and Y. M. Sheu, "Effect of uniaxial strain on anisotropic diffusion in silicon," *Appl. Phys. Lett.*, Vol. 89, pp. 161908-161908~3, October , 2006

Device Width	Device Length	Gate to STI Spacing	Long Stress	Tran Stress
10μm	1μm	10μm	×	×
1μm	0.08μm	10μm	×	○
1μm	0.08μm	2.4,0.21μm	○	○

Table. I

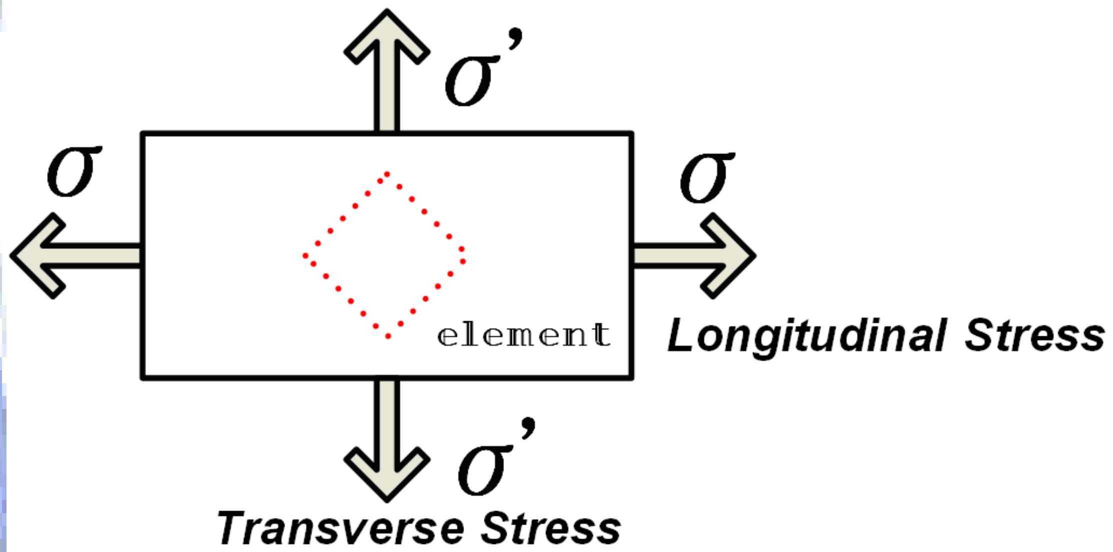

Fig.1

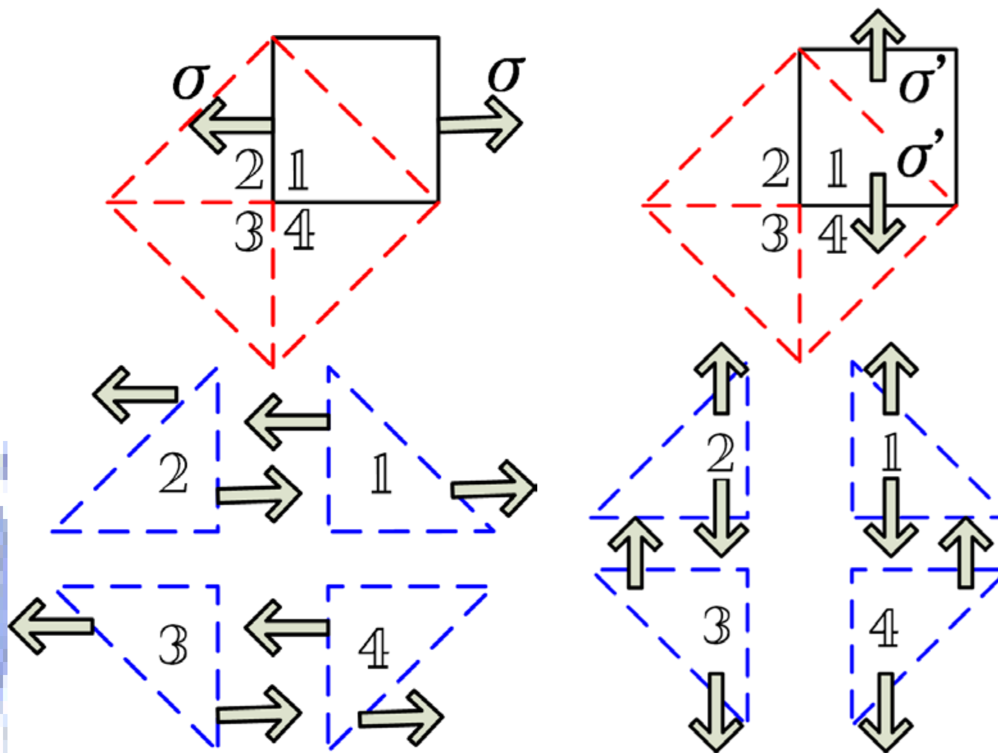

Fig.2

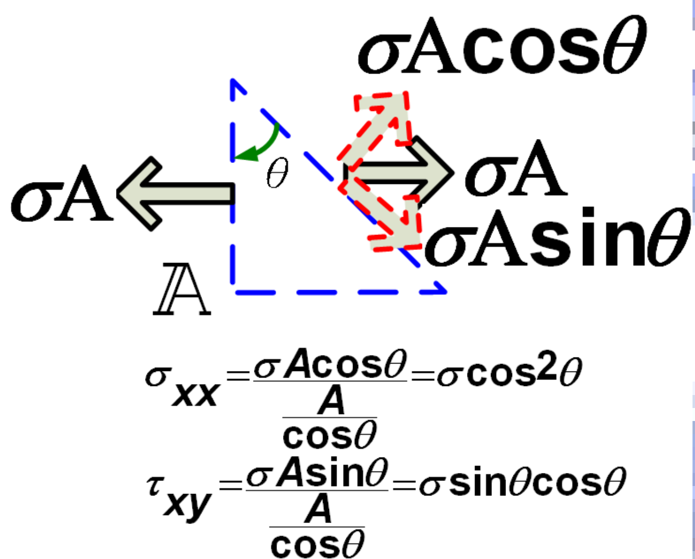

Fig.3

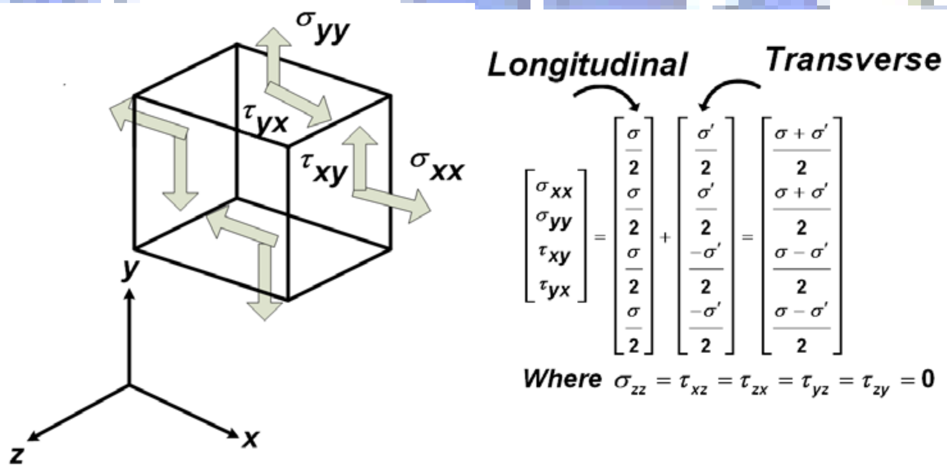

Fig.4

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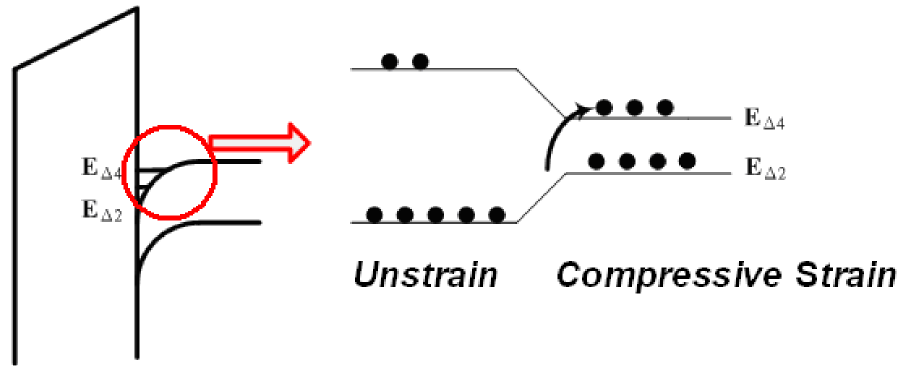

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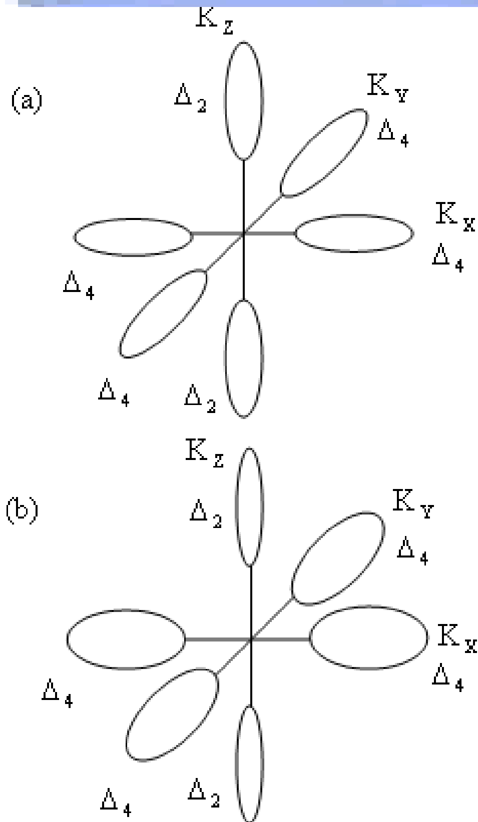


Fig.6

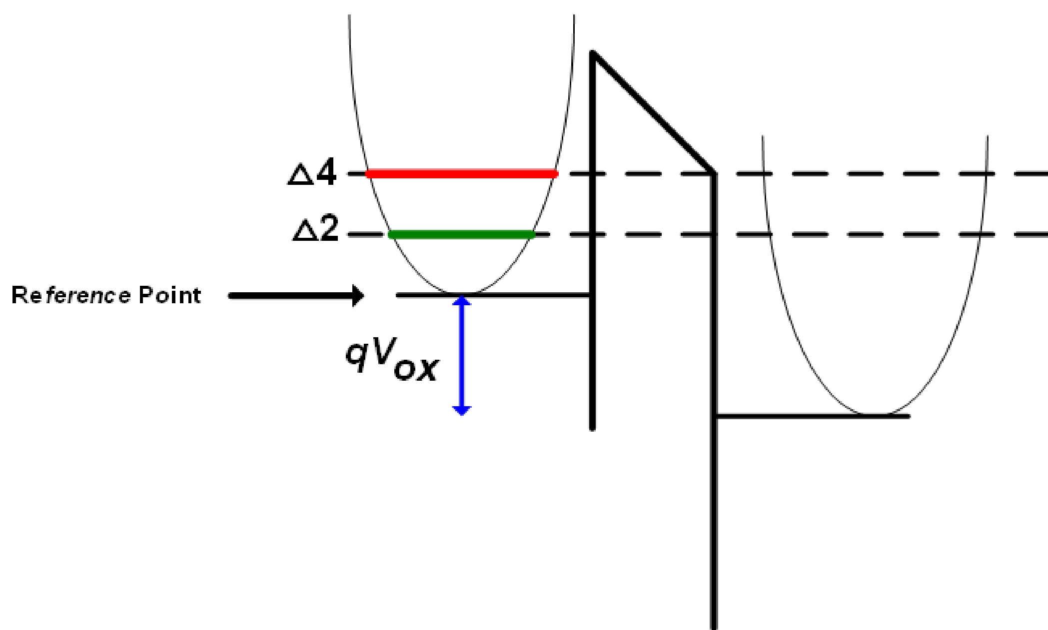


Fig.7

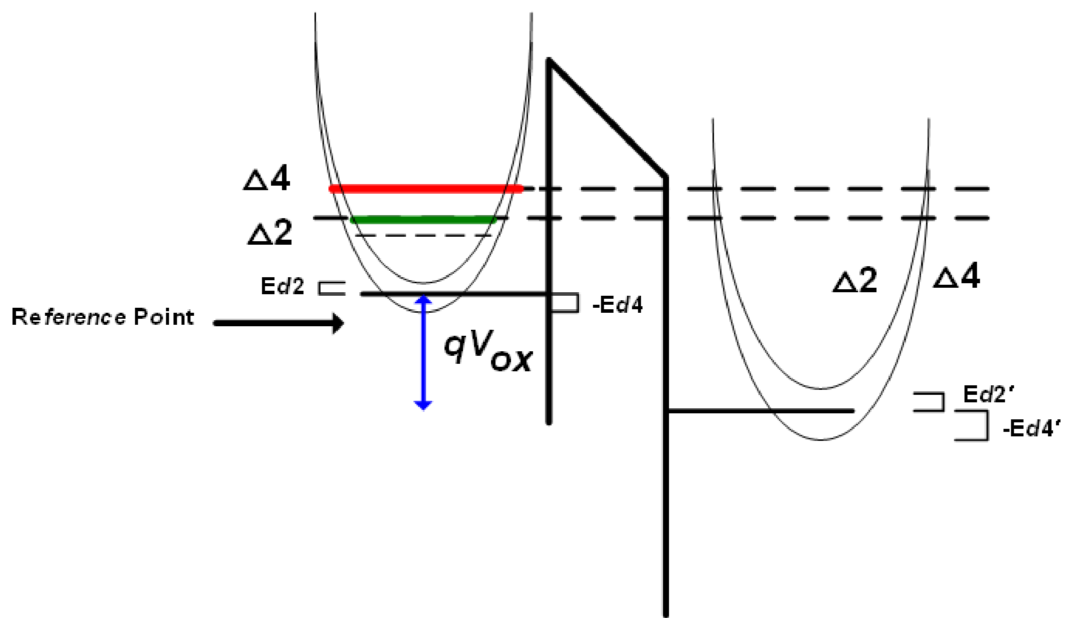


Fig.8

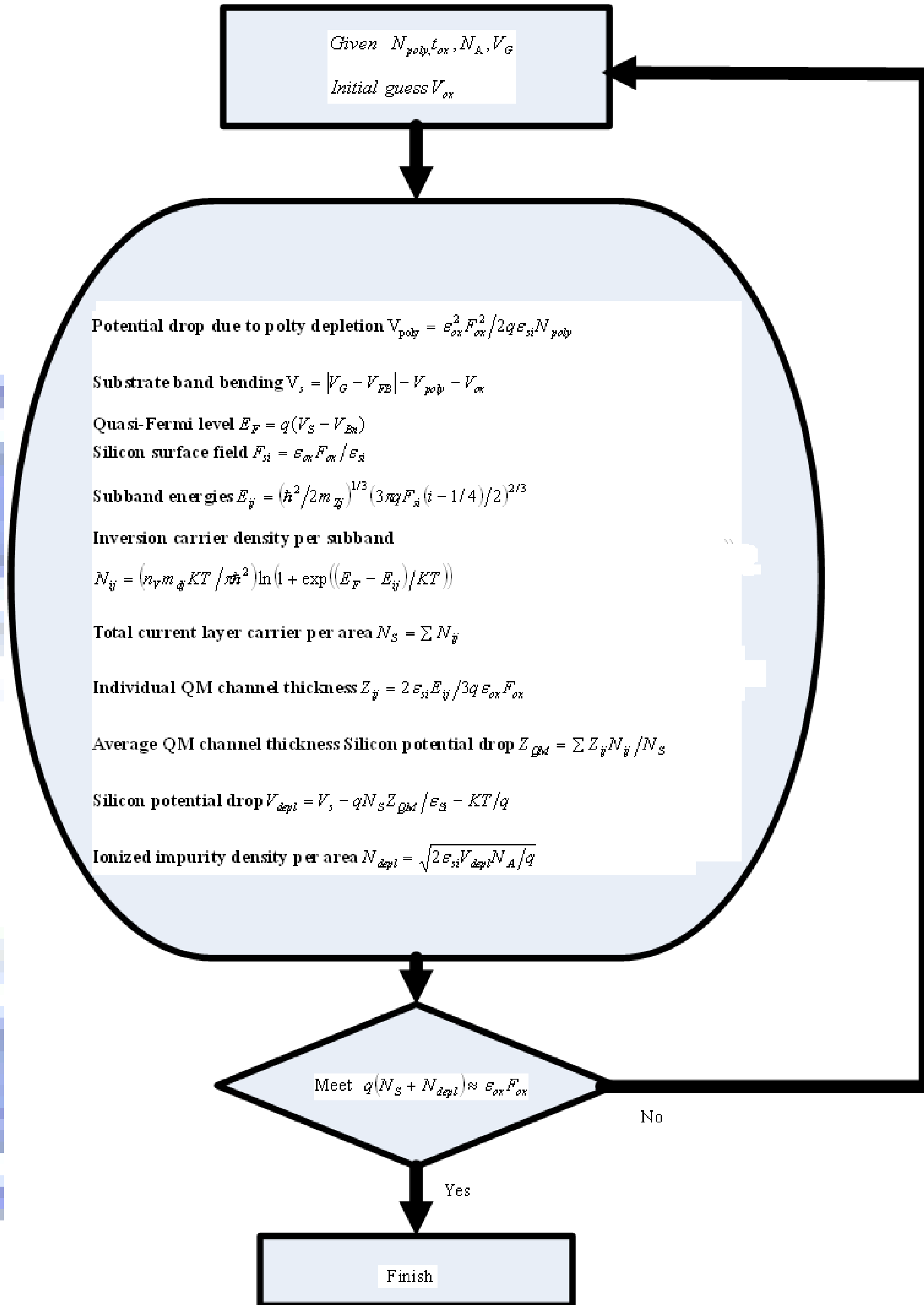


Fig.9

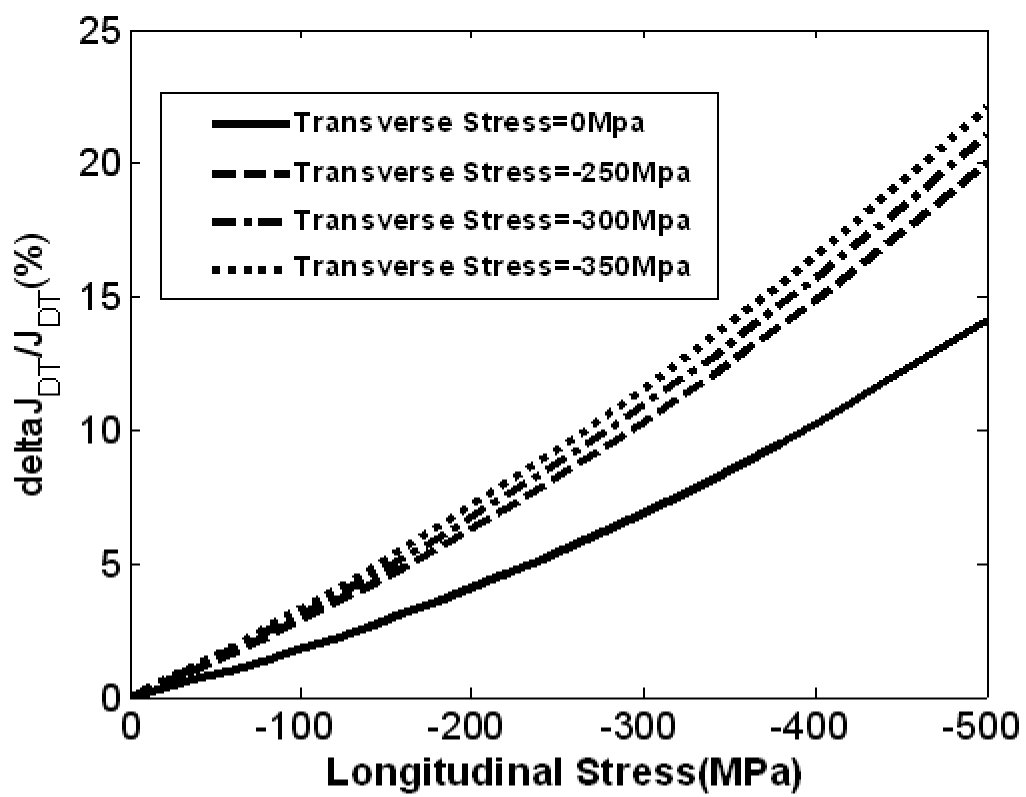


Fig.10

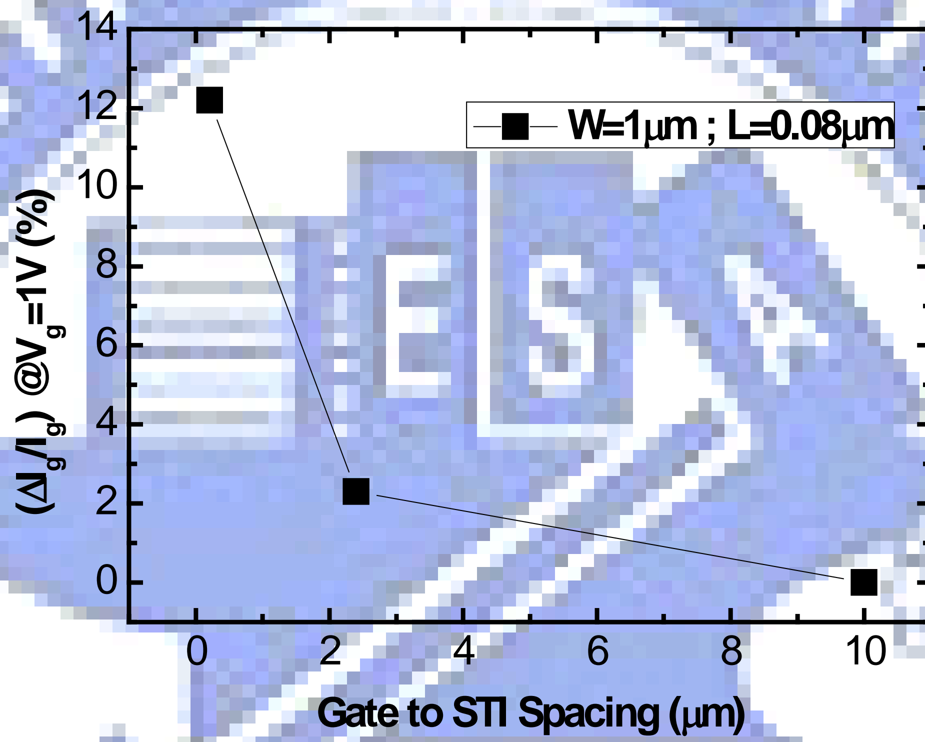


Fig.11

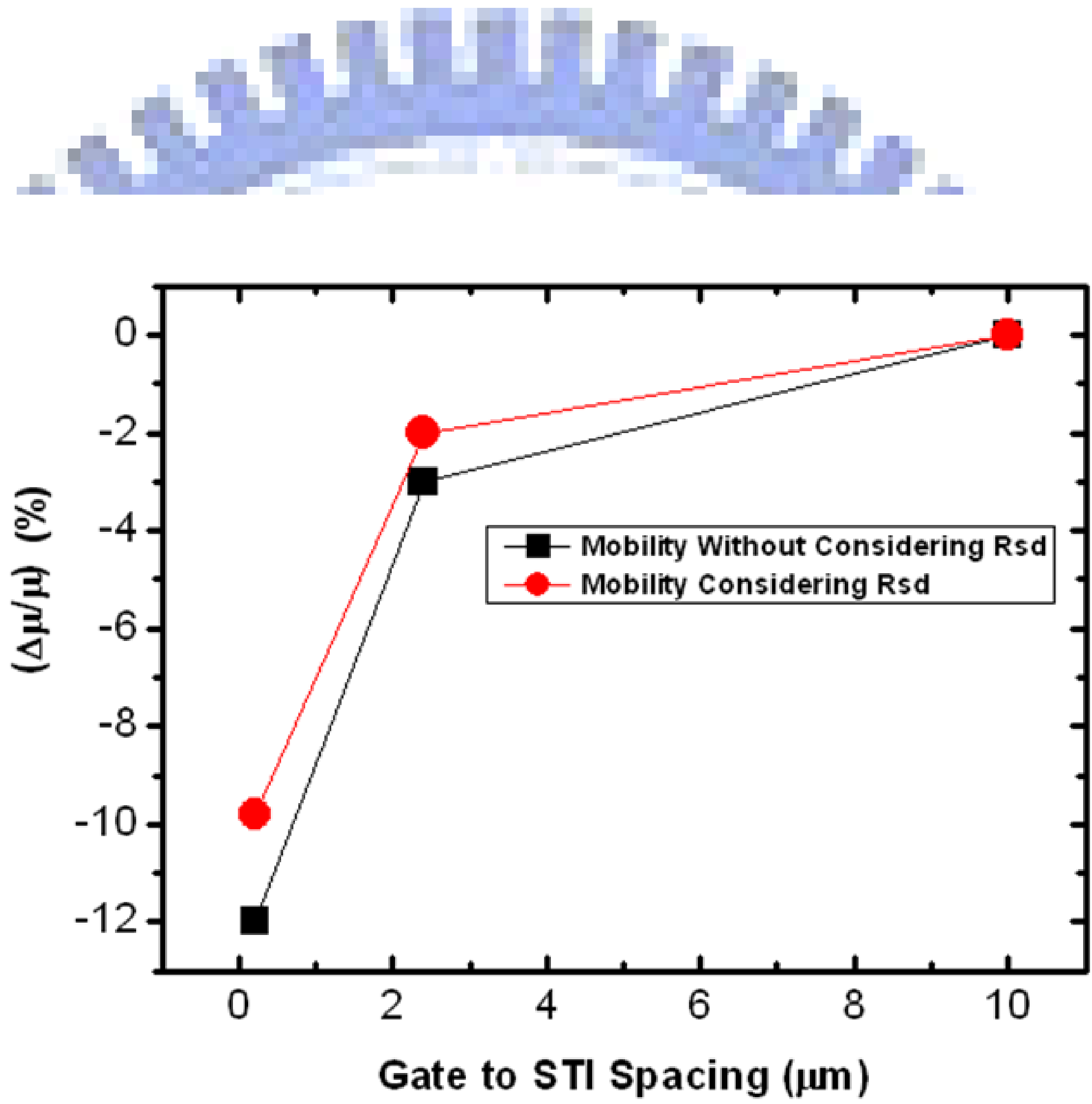


Fig.12

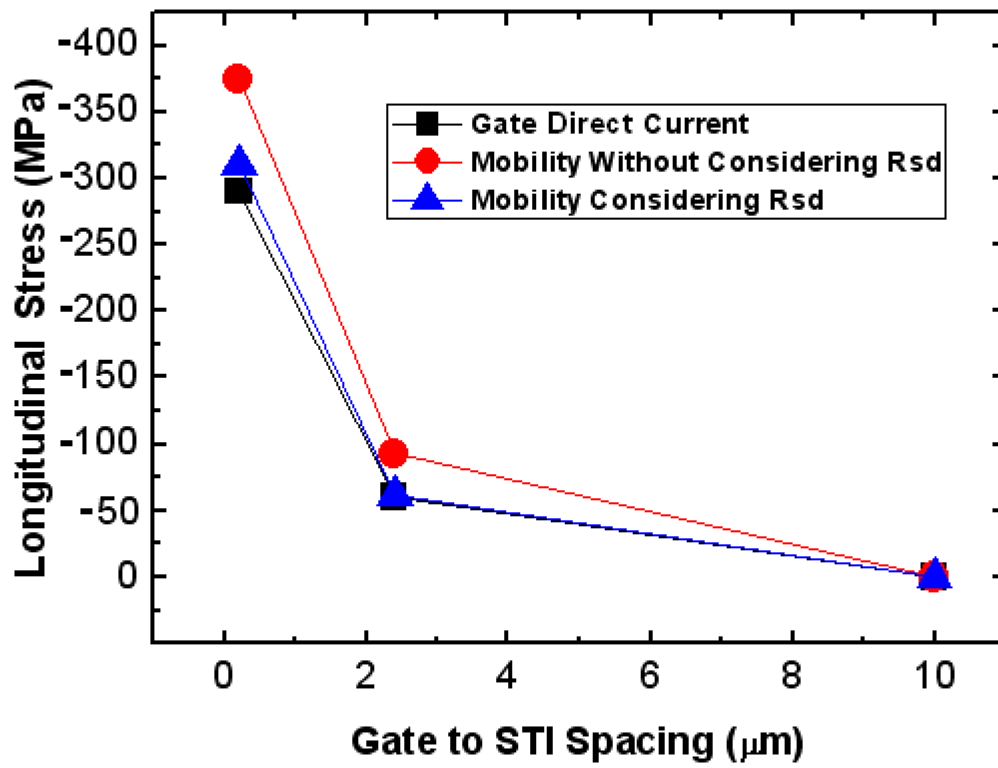


Fig.13

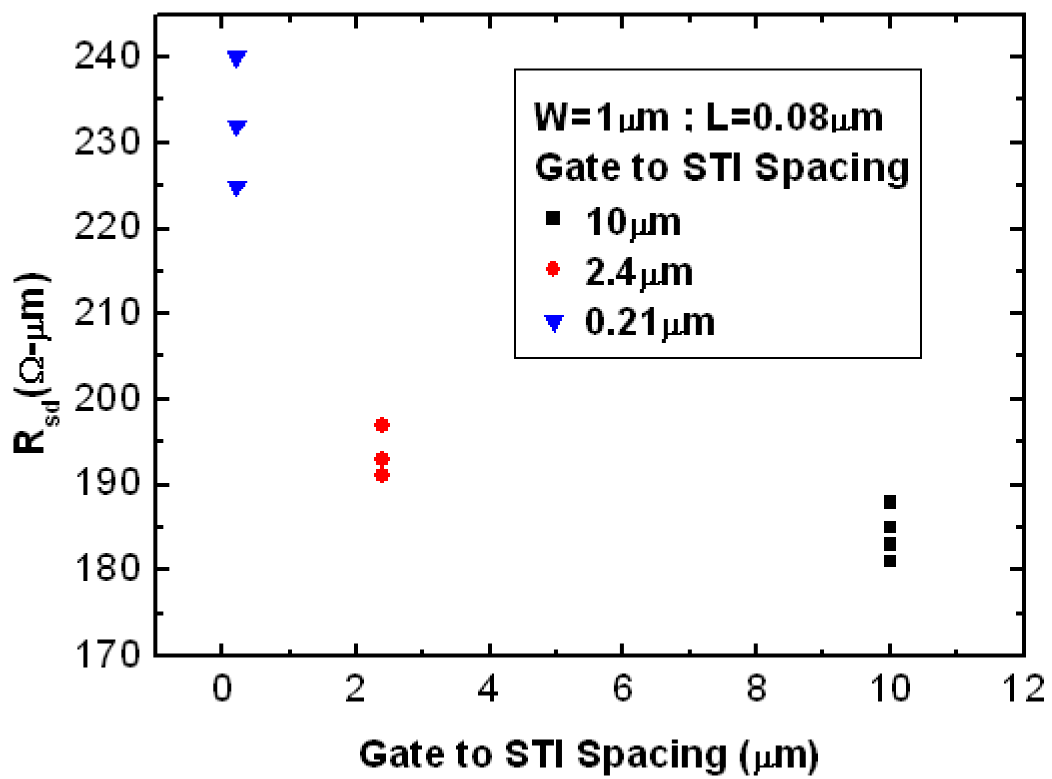


Fig.14

Given $N_{poly}, t_{ox}, N_{DE}, V_{DG}$

Initial guess V_{ox}

Potential drop due to polty depletion $V_{DE} = \varepsilon_{ox}^2 F_{ox}^2 / 2q\,\varepsilon_{si} N_{DE}$

Substrate band bending $V_{DE} - V_{FB} = V_{poly} + V_{ox} + V_{DE}$

Quasi-Fermi level $E_F = q(V_S + V_{fb})$

Silicon surface field $F_{si} = \varepsilon_{ox} F_{ox} / \varepsilon_{si}$

Subband energies $E_{ij} = \left(\hbar^2 / 2m_{Zj}\right)^{1/3} \left(3\pi q F_{si}(i - 1/4)/2\right)^{2/3}$

Inversion carrier density per subband

$N_{ij} = \left(n_V m_{dj} KT / \pi\hbar^2\right) \ln\left(1 + \exp\left(\left(E_F - E_{ij}\right)/KT\right)\right)$

Total current layer carrier per area $N_S = \sum N_{ij}$

Meet $q(N_S) \approx \varepsilon_{ox} F_{ox}$

No

Yes

Finish

Fig.15

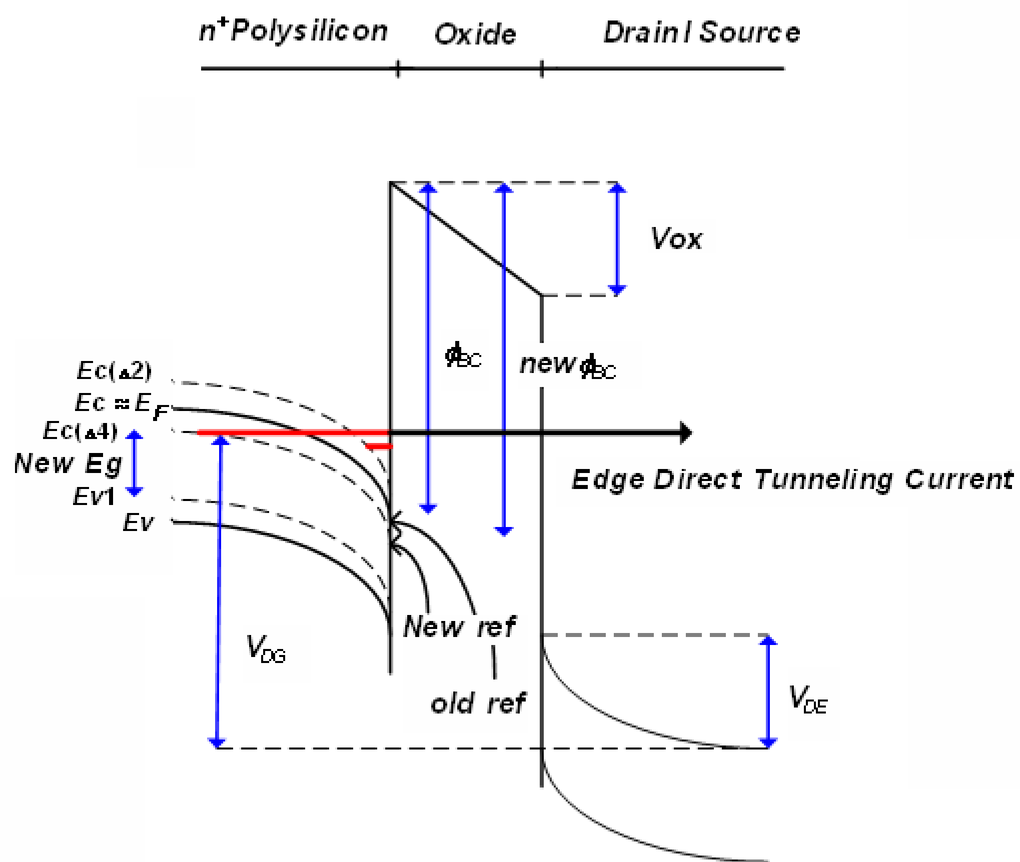


Fig.16

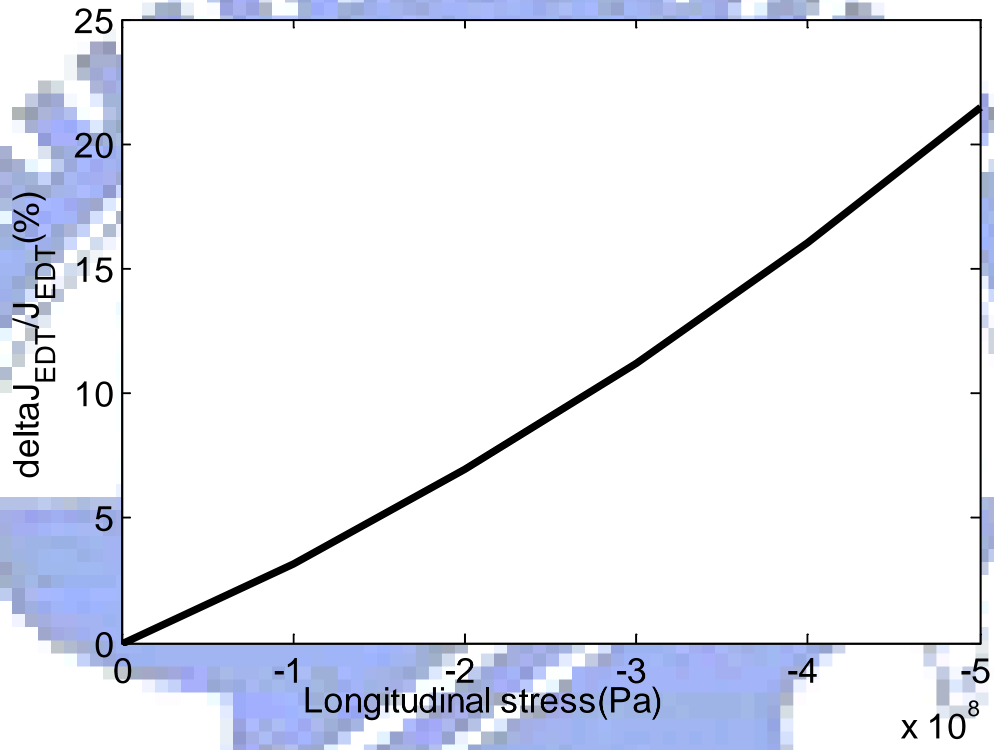


Fig.17

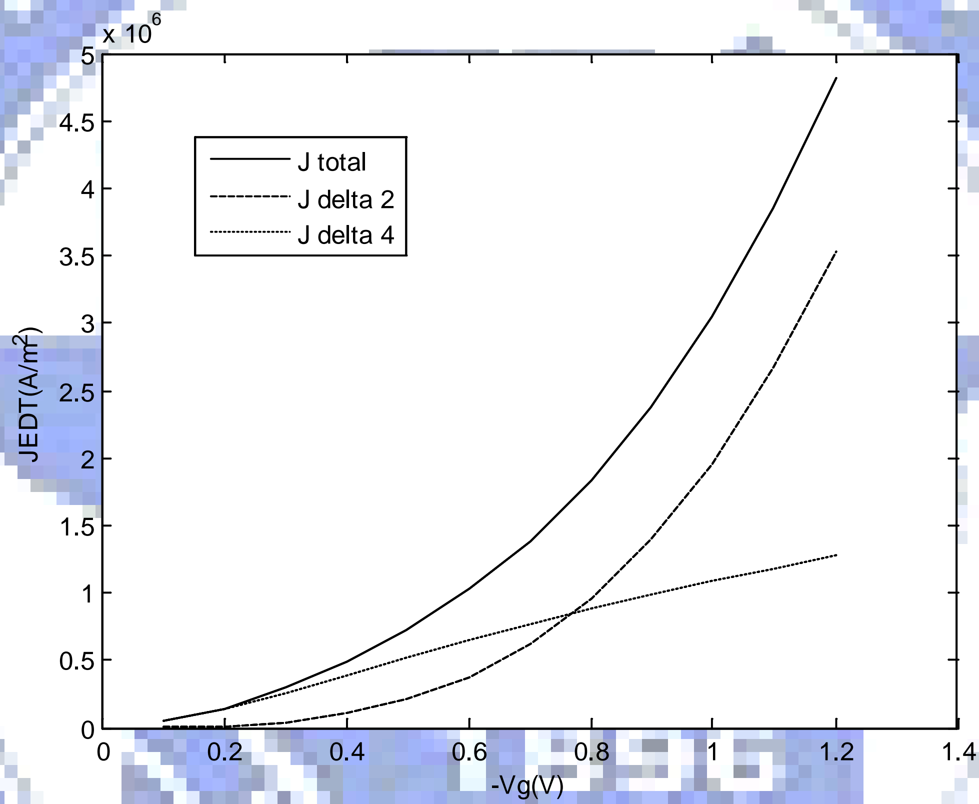


Fig.18

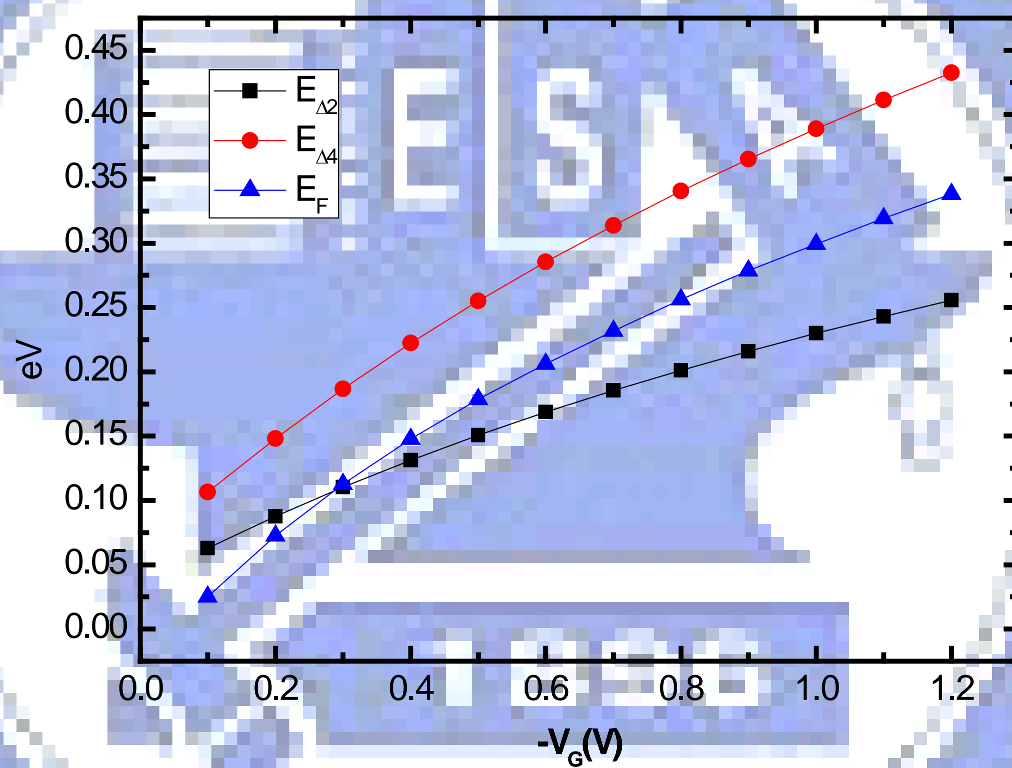


Fig.19

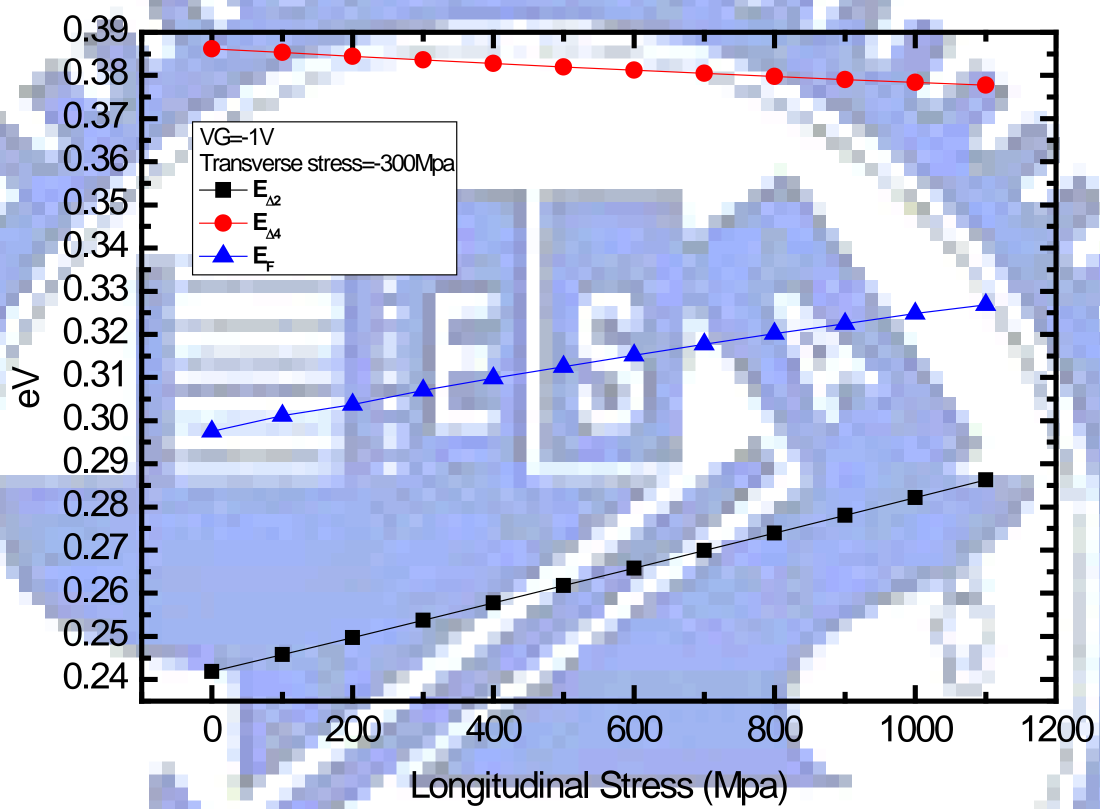


Fig.20

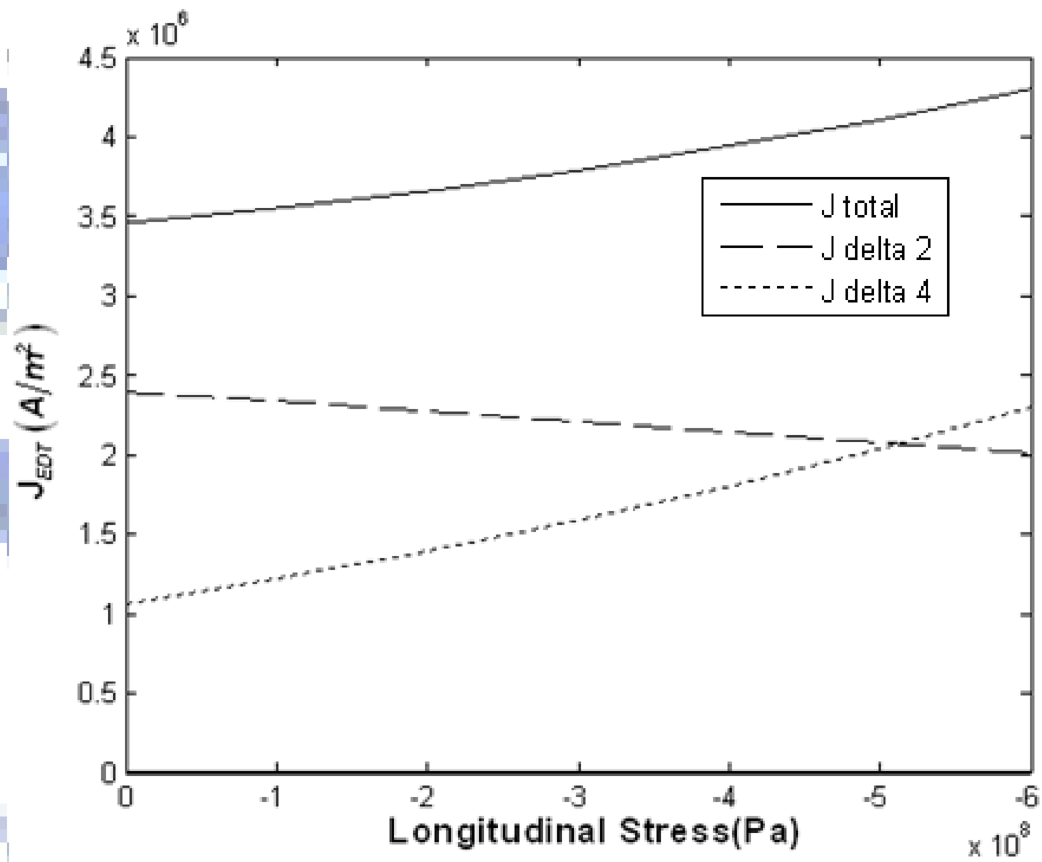
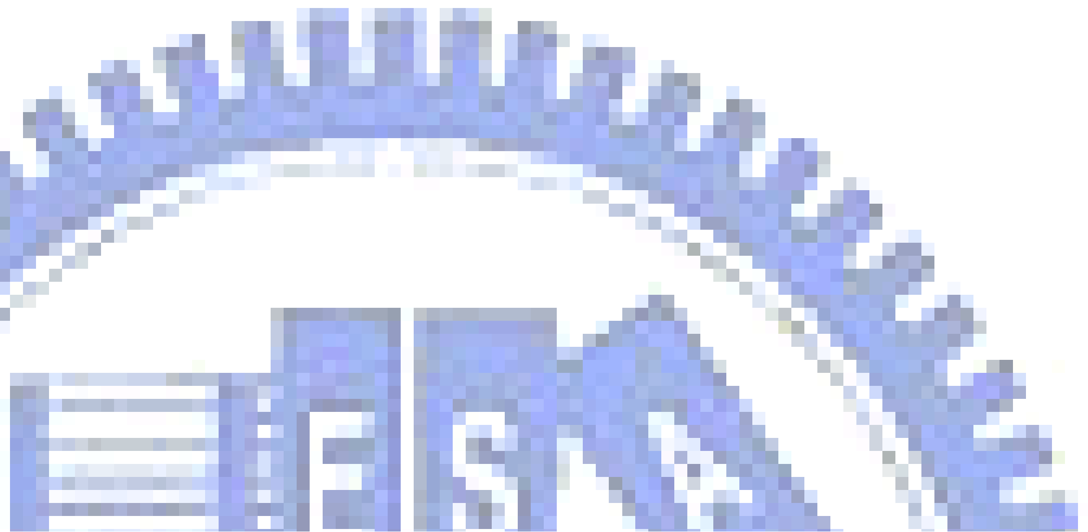


Fig.21



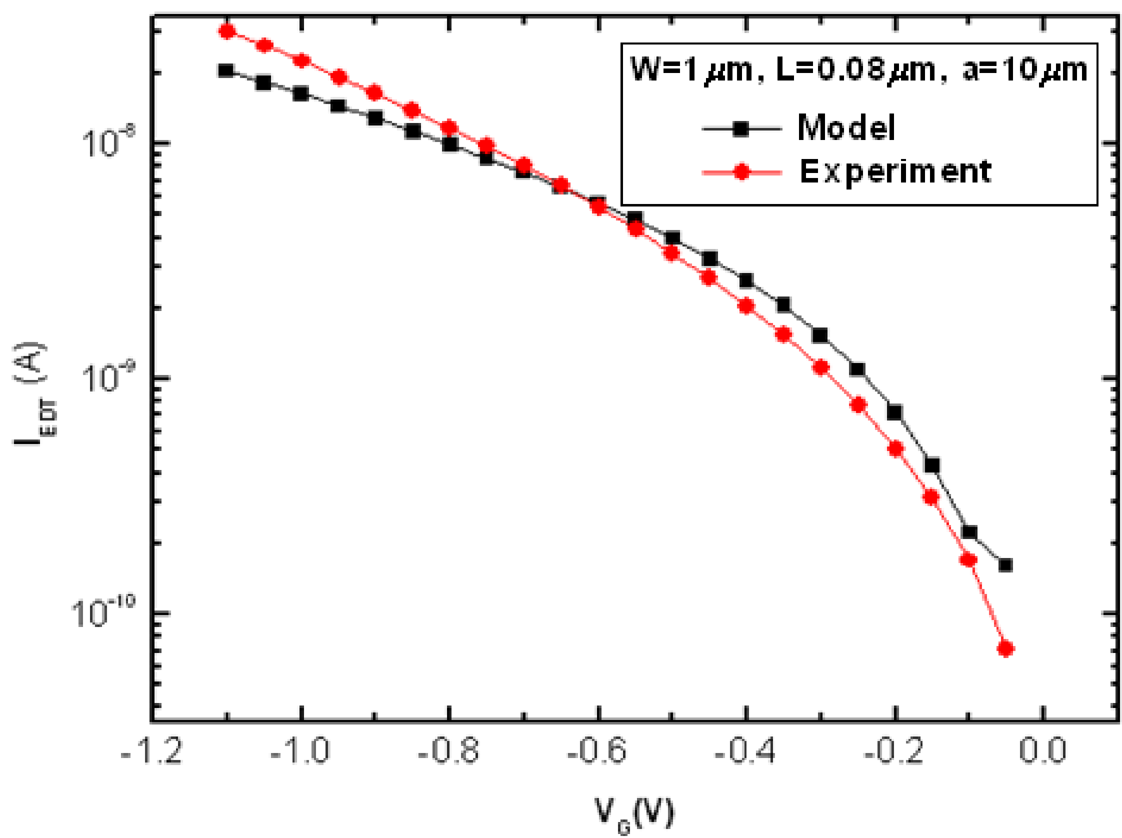


Fig.22

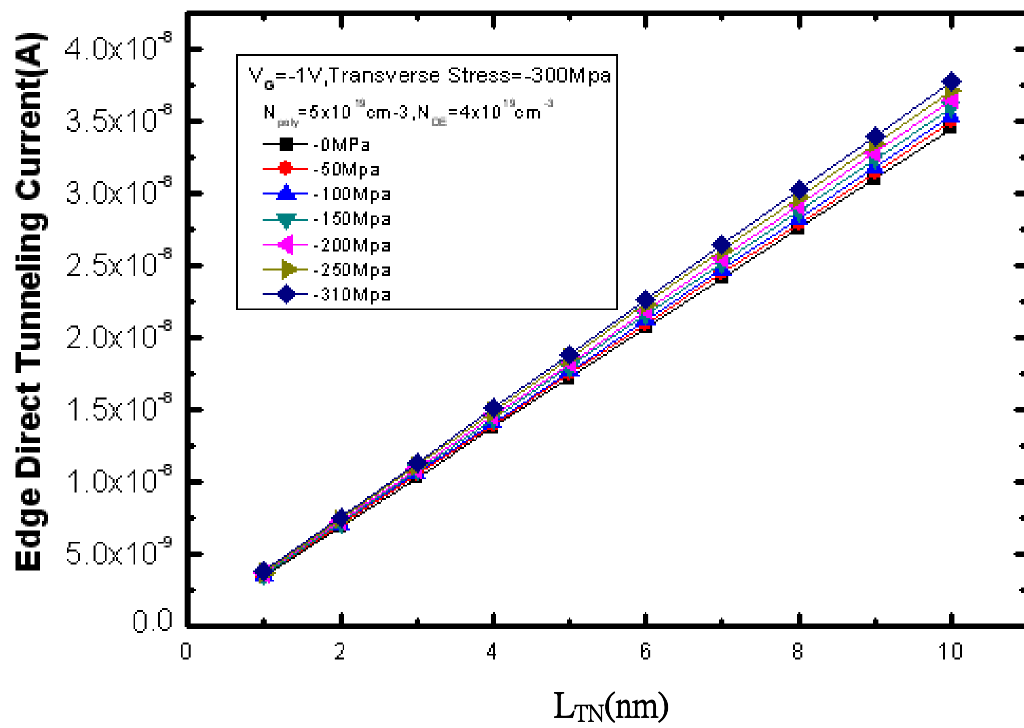


Fig.23

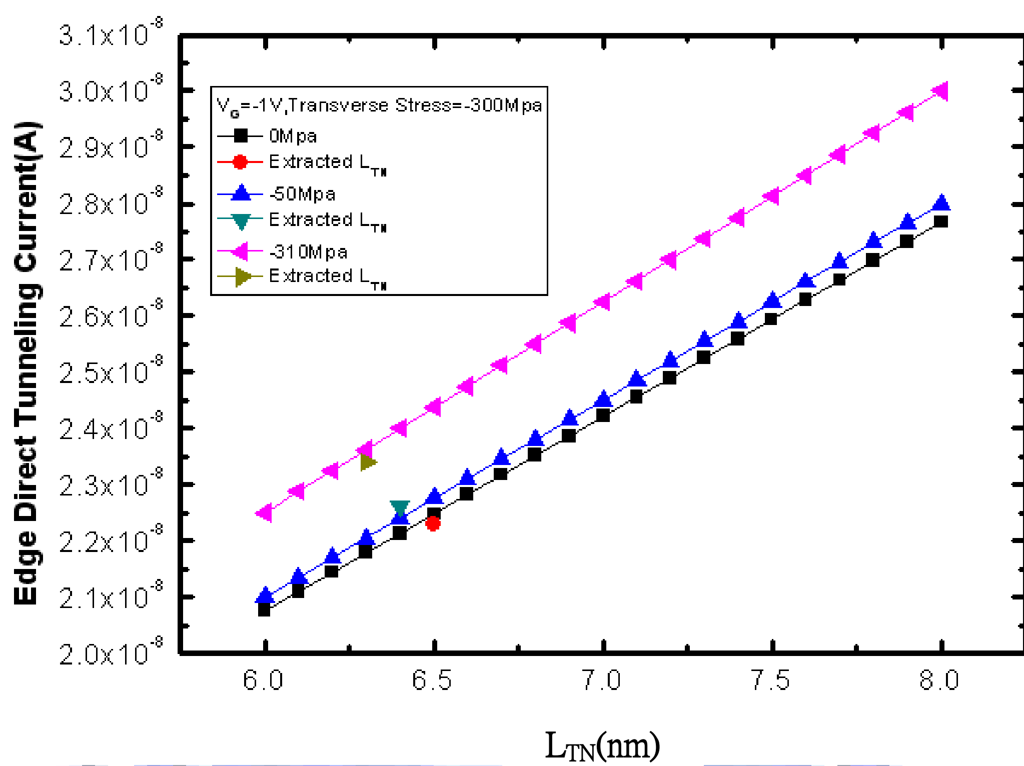


Fig.24

$Q(\sigma)$ (Approach 1)			$Q(\sigma)$ (Approach 2)	
	$D \propto n$	$D \propto n^2$		
$\varepsilon_{ZZ} = 0$	$-13.01eV$	$-20.52eV$	$\varepsilon_{ZZ} = 0$	$-25.24eV$
$\varepsilon_{ZZ} \neq 0$	$-26.02eV$	$-41.05eV$	$\varepsilon_{ZZ} \neq 0$	$-41.08eV$

Table. II