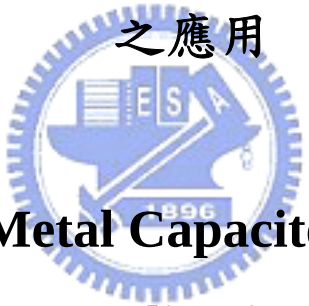
# 國立交通大學

## 電子工程學系 電子研究所碩士班

碩 士 論 文

# 金屬-氧化鈦鉿-金屬電容於動態記憶體與射頻電路之應用



# Metal-HfTiO-Metal Capacitors for DRAM/RF Applications

研 究 生：徐曉萱

指導教授：崔秉鉞 博士

中 華 民 國 九 十 七 年 七 月

# 金屬-氧化鈦鉿-金屬電容於動態記憶體與射頻電路之應用

# Metal-HfTiO-Metal Capacitors for DRAM/RF Applications


研 究 生：徐曉萱　　Student：Hsiao-Hsuan Hsu

指導教授：崔秉鉞 博士　　Advisor：Dr. Bing-Yue Tsui

**國 立 交 通 大 學**

**電子工程學系　電子研究所碩士班**


**碩 士 論 文**

A Thesis

Submitted to Department of Electronics Engineering and Institute of Electronics

College of Electrical and Computer Engineering

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of Master

in

Electronic Engineering

July 2008

Hsinchu, Taiwan, Republic of China

**中華民國九十七年七月**

# 金屬-氧化鈦鉿-金屬電容於動態記憶體與射頻電路之應用

研究生：徐曉萱　　指導教授：崔秉鉞 博士

國立交通大學

電子工程學系　電子研究所碩士班

## 摘要

本篇論文中，我們採用高介電常數的二氧化鈦($TiO_2$)，摻雜具有較大導帶不連續(conduction band offset)和能帶寬度的二氧化鉿($HfO_2$)，混合而成的鈦化鉿(HfTiO)材料作為金屬-氧化物-金屬(MIM)電容的介電質，來改善金氧金電容特性，以達到動態記憶體以及射頻電路的需求。本論文重點在比較上電極的效應、和介電層組成相關的漏電機制以及應力效應。在Pt/HfTiO/TaN 金氧金電容中，我們得到一個高電容密度約 17.5 $fF/\mu m^2$而所對應到的κ值為 37，且在電壓-1 伏特下得到很低的漏電約 $3.4x10^{-8}$ $A/cm^2$。和Al電極相比，高功函數的Pt電極不只改善漏電，同時可以改良類比特性，像是電壓電容係數(VCC)以及溫度電容係數(TCC)。除此之外，不同的Hf含量對HfTiO介電層的特性改善亦有研究。實驗數據顯示，增加Hf含量從 35%至 48%可以抑制漏電在電壓-3 伏特下約 1.5 個等級。在改良漏電方面，我們成功發展出氮氣電漿處理HfTiO介電層上的方法，在電壓-3 伏特下可以有效降低約兩個等級大小的漏電，同時維持電容密度以及VCC特性。

為了找出降低VCC的方法，深入了解VCC的基本機制是必須的。由於影響VCC特性的原因很多，在此，我們僅針對介電質的厚度效應、介電質成份組成以及堆疊式金氧金結構(laminate MIM structure)三個方向來探討。實驗結果顯示增加Hf的比例、增加介電層的厚度均可降低VCC。然而，使用HfTiO/$Y_2O_3$(三氧化二釔)堆疊式電容亦可達到降低VCC的效果，這是由於$Y_2O_3$具有負的VCC-α可以抵消具有正VCC-α的HfTiO，進而降低了VCC。

為了要達到高頻電容的需求，我們成功製造出厚度 51 奈米的HfTiO金氧金電容，電容密度為 5.1 fF/$\mu m^2$，且在電壓-1 伏特下的漏電為 1.3x$10^{-9}$ A/$cm^2$。此外，在頻率 100 kHz下的VCC-α值約 40 ppm/$V^2$，此一電容特性已符合 2012 ITRS的規格。

最後，我們探討金氧金電容在定電壓應力測試(constant voltage stress)下，基本電性以及電壓電容係數特性的變化。同時，可以觀察到電荷捕捉以及電荷釋放的現象以及小於 1%的電容密度變化。使用 Pt 電極不僅可以降低漏電，同時可以抑制應力產生漏電(stress-induced leakage current)和電容密度變化，並得到較好的VCC 特性以確保長時間下的可靠度。

# Metal- HfTiO -Metal Capacitors for DRAM/RF Applications

**Student: Hsiao-Hsuan Hsu** **Advisor: Dr. Bing-Yue Tsui**

**Department of Electronics Engineering and Institute of Electronics**
**National Chiao Tung University**

## Abstract

In this thesis, we adopted a hafnium titanate (HfTiO) film as MIM dielectric, which dopes $HfO_2$ with large conduction band offset and wide bandgap into high-κ $TiO_2$ (κ~50-80) to improve the performance of MIM capacitors for DRAM/RF applications. The attention of the thesis is focused on the effect of electrodes, conduction mechanism, film composition, and stress behavior. Low leakage current of $3.4x10^{-8}$ A/cm$^2$ at -1 V and high capacitance density of 17.5 fF/μm$^2$, which reflects a dielectric constant of 37, were obtained in a Pt/HfTiO/TaN MIM capacitor. Compared with Al top electrode, using high-work-function and thermodynamically stable Pt metal not only reduces the leakage current largely but also modify the analog characteristics (ex: VCC and TCC). Besides, the effect of Hf content on the performance of HfTiO dielectric was investigated. The experimental results indicate that the leakage current can be suppressed by nearly 1.5 orders of magnitude at gate bias of -3 V as Hf content increase from 35% to 48%. We developed successfully a $N_2$

plasma treatment on HfTiO dielectrics to further lower leakage current by two orders of magnitude at -3 V and no apparent degradation is observed on the capacitance and VCC properties.

To find out the solutions for reducing voltage nonlinearity, thickness effect, film composition, and laminate MIM structure are investigated. From the experimental results, we found that the VCC properties can be reduced effectively as the increase of Hf content and thickness of HfTiO dielectrics. Similar effects also can be achieved by using a HfTiO/$Y_2O_3$ laminate, which adding $Y_2O_3$ results in a drop in VCC-$\alpha$ because of canceling out the effect of positive VCC-$\alpha$ due to with the negative VCC-$\alpha$ of $Y_2O_3$. To meet the requirement of a RF capacitor, a 51 nm-thick Pt/HfTiO/TaN capacitor was fabricated successfully, which a capacitance density of 5.1 fF/$\mu m^2$ , low leakage current of $1.3x10^{-9}$ A/$cm^2$ at -1 V and very small VCC-$\alpha$ value of 40 ppm/$V^2$ at 100 KHz were obtained to achieve the goals of 2012 ITRS.

Finally, we investigate the stress behavior of [Pt or Al]/HfTiO/TaN MIM capacitors on electrical properties and VCC characteristics under constant voltage stress (CVS). Charge trapping and trap generation phenomena are observed on the HfTiO MIM capacitors under CVS stress. Capacitance variation less than 1% can be achieved. The use of Pt electrode not only reduces the leakage current but also can suppress the stress-induced leakage current and capacitance variation to get a better VCC for long-term reliability.

# 謝誌

研究所兩年的生涯中，首先要感謝我的指導老師 崔秉鉞教授，老師的諄諄教誨以及嚴謹認真的專業態度，總讓我受益匪淺;而老師的熱心公益以及耿直的做人態度更是我學習的典範。

感謝實驗室的學長姐 李振銘、李振欽、洪玉仁、謝志民、盧季霈以及黃勻珮在實驗上的討論幫忙與機台的訓練;感謝實驗室的夥伴 蔡雨蓁、張孝瑜、劉筱函、張嘉文、羅正愷，有你們一起分享作實驗的酸甜苦辣，彼此加油打氣，真的很棒;謝謝學弟們 周智超、蔡依成、羅子歆幫忙約 run 以及處理實驗室的事務，讓我們可以更專心在實驗上，謝謝你們大家。謝謝曾俊元實驗室的學長以 林志洋、吳明錡、林孟漢、同學 詹世緯的幫忙與建議，讓我在實驗上能很快的上手。由衷感謝荊鳳德實驗室的學長 鄭淳護、黃靖謙以及鄧志剛，有了你們，讓我實驗能夠一路披荊斬棘，越挫越勇。

謝謝我的好朋友們 陳玲、高珮玲、郭全雯、謝承佑以及游泳隊的夥伴們，有你們六年來的的聊天與陪伴，美好的回憶我點滴在心，祝福你們。

最重要的感謝我親愛的父母 徐明芳先生、劉素淑女氏，謝謝你們從小的栽培與照顧，以及姊姊 徐悅晴給予專業的諮詢，使我無後顧之憂得以完成論文。我把這本論文獻給你們。

# Contents

# Table Captions

## Chapter 1 Introduction



## Chapter 4 Improvement on Capacitance Behavior Dependence of Voltage and Temperature

# Figure Captions

## Chapter 1 Introduction



## Chapter 2 Experimental Procedure



## Chapter 3 HfTiO MIM Capacitors for DRAM and RF Applications

## Chapter 4 Improvement on Capacitance Behavior Dependence of Voltage and Temperature

## Chapter 5 The Observation on Stress Performance of MIM Capacitors under Constant Voltage Stress

# Chapter 1

# Introduction

## 1.1 Why Using $HfO_2$ Doped $TiO_2$ Dielectrics for MIM Capacitors

In recent years, a global research has been implemented to identify suitable high-dielectric-constant (high-κ) materials. In CMOS technology, the continuous downscaling of the gate dielectric thickness to achieve further gains in performance and productivity is an enormous task due to direct tunneling currents and boron penetration in $SiO_2$ below 1.5 nm. Similar problems are expected in the case of the dynamic random access memory (DRAM) storage capacitor dielectrics. According to International Technology Roadmap for Semiconductors (ITRS) [1.1], migration of gigabit DRAM capacitor structures from silicon-insulator-metal (MIS) to metal-insulator-metal (MIM) with design rules of 0.10 μm and below is essential [1.2]. In addition, MIM capacitors in silicon analog circuit applications have attracted great attention due to their high conductive electrodes and low parasitic capacitance between the capacitor and the substrate [1.3, 1.4].

The accelerative downscaling of metal-insulator-metal (MIM) capacitors requires a corresponding reduction in the thickness of dielectrics to achieve high capacitance density and thus results in increasing leakage current and poor voltage linearity [1.5]. In addition to the leakage issue, as an increase in the integration level and the scale-down of chip size, capacitors consume a large fraction of the area and thus disputing reduction of the circuit density and the system cost. From the viewpoint of power consumption, capacitance density, and circuit density, one solution for these problems is to replace conventional silicon dioxide [1.6] and silicon nitride [1.3, 1.5, 1.7] with high-κ dielectrics to maintain the capacitance density in each generation as

well as suppress the leakage current. Table 1-I illustrates the summarized material and electric properties of several high-κ gate dielectrics [1.8]. High-κ dielectrics have been proposed for several years, such as $HfO_2$ [1.9–1.12], $Al_2O_3$ [1.12, 1.15], $(HfO_2)_{1-x}(Al_2O_3)_x$ [1.13], AlTaO [1.14], $AlTiO_x$ [1.15], and $Ta_2O_5$ [1.12, 1.16], for MIM capacitors.

Among these investigated high-κ dielectrics, titanium oxide, $TiO_2$ dielectrics have been characterized by its high dielectric constant (κ~50-80) [1.17], which makes it's potentially useful in various roles in integrated circuits (IC), including capacitors, gate oxides, and other circuit elements [1.18, 1.19]. It is believed that dielectric constant variability is related to the presence of low-permittivity interfacial layers and to the difference crystalline phase. The dielectric constant of $TiO_2$ changes from ~31 to 60-100 for crystalline anatase and rutile, respectively [1.20, 1.21]. Although $TiO_2$ has a merit of high dielectric constant, the small band offset is a serious concern on the leakage current due to the limitation for real devices. Therefore, a critical goal is to increase the breakdown field and reduce the leakage current density.

Fig.1-1 shows the energy band alignment of various high-κ dielectrics with respect to silicon. The dashed lines represent 1 eV above and below the conduction and valence band, respectively, which point out the minimum barrier height to suppress the leakage current [1.22]. One approach to decrease leakage current due to eliminate defects in $TiO_x$ might be the incorporation of foreign cations into the thin film. It has also been reported that adding 10-30 at.% of Nd, Tb, or Dy to amorphous Ti–O thin films can decrease the leakage current, increase the breakdown voltage, and yet retain the relatively high dielectric constant (k~50-100) [1.23]. In addition, Zirconium titantate-based thin films have been determined to be the promising candidate for ultra-large-scale integration [1.24]. The element of Sn can further improve the electrical properties of amorphous Ti–Zr oxide [1.25]. As shown in Fig.

1-2, the trend of bandgap decline with increasing relative dielectric constant [1.8]. There is a trade-off between the leakage current and the dielectric constant. Therefore, the merit of introducing $HfO_2$ is its medium dielectric constant (k~20) and large band offset ($\Delta E_c$~1.5 eV) which might compensate the leakage issue of $TiO_2$ dielectrics and maintain high dielectric constant at the same time. In addition, from the viewpoint of high-κ dielectrics materials, low-valence ions in $TiO_2$ will produce oxygen vacancies, which lead to a higher ionic conductivity. For example, 8% $Y_2O_3$ ($Y^{3+}$) doped $HfO_2$ results in a high ionic conductivity of 0.03 $\Omega^{-1}cm^{-1}$ is reported due to low-valence ions doping [1.26]. Ti and Hf are both four-valence elements. So $HfO_2$ doped $TiO_2$ would not exhibit any increase in oxygen voids which attribute the leakage current in the film.

Many articles [1.27-1.31] studied the electrical as well as structural properties of mixtures of $HfO_2$ and $TiO_2$ as possible high-κ gate dielectrics. However, relatively few attempt to investigate the mixture of $HfO_2$ and $TiO_2$ as the dielectrics in the MIM capacitors.

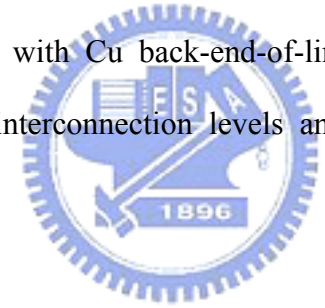
## 1.2 MIM Capacitors in RF Applications

The dramatic increase in wired and wireless communications in recent years has demanded the need for high quality passives for mixed and analog signal applications. MIM capacitors, which are typically used in RF circuits for impendence matching and direct current (DC) filtering, as well as analog capacitors in mixed-signal product [1.5], draw much attention due to its high quality factor low parasitic capacitance better matching, and small voltage coefficient of capacitance (VCC) [1.6, 1.32],

Both in analog and RF applications, one of the desired properties of MIM capacitors is a high degree of voltage linearity also called voltage coefficient of capacitor (VCC), which traduces the dependence of capacitance on the applied bias.

In MIM capacitors, one of the greatest challenges is to achieve small VCC, which is required for capacitors to minimize harmonic generation and improve balancing [1.33, 1.34]. According to International Technology Roadmap for Semiconductor (ITRS), VCC is required less than 100 ppm/$V^2$ from now on to 2020 as showed in Table 1-II and Fig. 1-3 [1.1].

Except the specification for VCC, the dielectrics of MIM capacitors has to fulfill the following main requirement: (1) high capacitance density (>5 fF/$\mu m^2$), in terms of ITRS, the need for RF capacitor is 4 to 12 fF/$\mu m^2$ in 2008 to 2020, (2) low leakage currents ($10^{-8}$ A/$cm^2$), (3) high breakdown electric field (holding at least a voltage bias of 5 V), and (4) low dielectric loss [$\tan\delta$ <0.05, i.e., Q factor (=1/ $\tan\delta$ )>20] [1.35]. Moreover, a low thermal budget (450℃) is required for MIM capacitors to be compatible with Cu back-end-of-line (BEOL) process, since the devices are located in the interconnection levels and above the active integrated circuit layers.



## 1.3 MIM Capacitors in DRAM Applications

Today, most of computer memory chips use the dynamic random access memory (DRAM) in which each bit of information is stored in a memory cell consisting of one transistor and one capacitor (1T1C). This kind of memory was first invented by an IBM researcher named Robert Heath Dennard in 1967. It has become a breakthrough that made DRAM become the standard memory chip for personal computers replacing magnetic core memory. Until 1972, Intel had already released the world's first generally available 4 Kb DRAM chip and transformed the microelectronics industry throughout. Nowadays, DRAMs have been advanced by focusing on how to make memory cells smaller to realize higher density DRAMs.

The conventional “shrink technology” up to Gbit density encounters many

challenges, especially in the cell capacitance point of view. Memory cell capacitance is the key parameter which determines the sensing signal voltage, sensing speed, data retention times and endurance against the soft error event [1.36]. In the Gbit era, it's generally accepted that the minimum cell capacitance should be kept more than 25 fF regardless of density. The strategies for achieving higher cell capacitance are either reducing the thickness of the dielectrics or adopting high-κ materials. However, aggressive scaling down the thickness would result in leakage current, power consumption, and reliability issues due to electrons tunneling [1.37]. In order to offer the thicker physical thickness and maintain the same capacitance density, high-κ capacitor becomes the only one solution [1.38].

For DRAM trench capacitor, using of NO dielectric (nitride/oxide stack) has been extended through the 70 nm generation, with high-κ materials being introduced at the 65 nm generation [1.1]. According to the ITRS, dielectric constant of 50 is demanded for the stacked DRAM from now on to the year of 2010 as shown in Table 1-III [1.1]. Table 1-IV [1.1] shows the possible materials for DRAM stacked capacitor although mass-production solutions are not optimized yet after 2010 [1.1, 1.39]. Table 1-V also presents the requirements for the DRAM trench capacitor [1.1].

In the recent years, thin film perovskite materials with ultra high-κ such as PZT [1.39], $SrTiO_3$ [1.40] and $(Ba,Sr)TiO_3$ [1.41] have been investigated as dielectric materials for DRAM. According to 2007 ITRS roadmap [1.1], one of the difficult challenges is scaling of the physical dielectric thickness, $T_{phy}$ while maintaining dielectric constant and leakage current of dielectrics. To obtain ultra high-κ value ($\kappa > 130$) for DRAM requirement of 2014 ITRS, large leakage current caused by small conduction band offset (~ -0.1 eV) will be unacceptable for $SrTiO_3$ materials. Therefore, thicker thickness is required to reduce the electric field across the dielectric. However, these ultra high-κ dielectrics have the thickness limit due to the capacitor

geometry, since the aspect ratio of the deep trench and metal-1 contact of stacked capacitors [1.42], which are related to the ability of gap-filling, should be taken into consideration. In particular, the G-bit DRAM will only have space for a dielectric layer no thicker than 20 nm [1.43]. Besides, it's a challenge to deposit ternary materials into high aspect ratio structures with a uniform film composition by CVD process, let along PVD process. Also, these ultra high-κ dielectrics aren't suitable for RF applications due to low thermal budget issues and much lower capacitance density being needed. Therefore, around 10 nm thin film and high-κ dielectric of $HfTiO_x$ is adopted in this thesis to achieve parts of the specifications for both RF and DRAM applications.

In addition to the high dielectric constant, low leakage current is another key design feature for DRAM cells, since the refresh interval is governed by the stored charge loss at the capacitor [1.44, 1.45]. Increasing tunneling current due to scaling down the dielectrics has been shown in D. J. Frank *et al.*[1.46]. In terms of the ITRS shown in Table1-III, leakage current around $1x10^{-7}$ A/cm$^2$ is acceptable until 2020.

## 1.4 The Organization of this Thesis

The organization of this thesis is briefly described below. Chapter 1 depicts the motivation to adopt the high-κ HfTiO dielectrics and the MIM capacitors in RF and DRAM applications. Chapter 2 describes the process procedure of the HfTiO MIM capacitors as well as the methods of electrical and material analysis. Chapter 3 discusses the electrical characteristics of HfTiO MIM capacitor using in RF and DRAM field. The effects of top electrode and plasma treatment have also been investigated. Chapter 4 illustrates the physical model of charge trapping and detrapping to explain the mechanism of voltage nonlinearity. Four methods to improve the voltage linearity is also proposed, including using high work function top

electrode, increasing the amount of $HfO_2$, adopting stack structure and increasing the dielectric thickness. Chapter 5 studies the long-term reliability of HfTiO MIM capacitors with top electrodes of Pt and Al in terms of constant voltage stress (CVS). Chapter 6 summarizes the conclusions and contributions of this thesis, and provides the suggested directions for further research.

Table 1-I Summarized material and electric properties of several high-$\kappa$ gate dielectrics [1.8].

| Dielectric | Dielectric constant | Bandgap (eV) | Conduction band offset | Thermal stability on Si substrate |
|---|---|---|---|---|
| $SiO_2$ | 3.9 | 9 | 3.5 | >1050℃ |
| $Si_3N_4$ | 7 | 5.3 | 2.4 | >1050℃ |
| $Al_2O_3$ | ~10 | 8.8 | 2.8 | ~1000℃ |
| $Ta_2O_5$ | 25 | 4.4 | 0.36 | Not stable |
| $La_2O_3$ | ~21 | 6* | 2.3 | |
| $Gd_2O_3$ | ~12 | | | |
| $Y_2O_3$ | ~15 | 6 | 2.3 | Silicate formation |
| $HfO_2$ | ~20 | 6 | 1.5 | ~950℃ |
| $ZrO_2$ | ~23 | 5.8 | 1.4 | ~900℃ |
| $SrTiO_3$ | | 3.3 | ~0.1 | |
| $ZrSiO_4$ | | 6* | 1.5 | |
| $HfSiO_4$ | | 6* | 1.5 | |

*Estimated value

Table 1-II The requirement for RF devices according to ITRS [1.1].

| Metal-Insulator-Metal Capacitor | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Year of Production** | 2008 | 2010 | 2012 | 2014 | 2016 | 2018 | 2020 |
| **Density (fF/μm²)** | 4 | 5 | 5 | 7 | 10 | 10 | 12 |
| **Voltage linearity (ppm/V²)** | <100 | < 100 | < 100 | < 100 | < 100 | < 100 | < 100 |
| **Leakage (A/cm²)** | <1e-8 | <1e-8 | <1e-8 | <1e-8 | <1e-8 | <1e-8 | <1e-8 |
| **$\sigma$ Matching (%·μm)** | 0.5 | 0.4 | 0.4 | 0.3 | 0.2 | 0.2 | 0.2 |
| **Q (5 GHz for 1pF)** | >50 | >50 | >50 | >50 | >50 | >50 | >50 |

Table 1-III DRAM stacked capacitor films technology requirements [1.1].

| **Year of Production** | 2008 | 2010 | 2012 | 2014 | 2016 | 2018 | 2020 |
|---|---|---|---|---|---|---|---|
| **DRAM ½ Pitch (nm)** | 57 | 45 | 36 | 28 | 22 | 18 | 14 |
| **Capacitor structure** | Cylinder / Pedestal MIM | Cylinder / Pedestal MIM | Cylinder / Pedestal MIM | Pedestal MIM | Pedestal MIM | Pedestal MIM | Pedestal MIM |
| **$t_{eq}$ at 25fF (nm)** | 0.90 | 0.60 | 0.40 | 0.30 | 0.30 | 0.30 | 0.20 |
| **Dielectric constant** | 43 | 65 | 98 | 130 | 91 | 78 | 80 |
| **Leak current (fA/cell)** | 0.70 | 0.64 | 0.64 | 0.59 | 0.41 | 0.35 | 0.35 |
| **Leak current density ($nA/cm^2$)** | 107.9 | 148.4 | 222.6 | 269.8 | 188.8 | 161.9 | 242.8 |
| **$V_{capacitor}$ (Volts)** | 1.2 | 1.1 | 1.1 | 1 | 0.7 | 0.6 | 0.6 |
| **Retention time (ms)** | 64 | 64 | 64 | 64 | 64 | 64 | 64 |
| **Deposition temperature (degree C)** | ~500 | ~500 | ~500 | ~500 | ~500 | ~500 | ~500 |
| **Film anneal temperature (degree C)** | ~750 | <750 | ~650 | <650 | <650 | <650 | <650 |

Table 1-IV DRAM stacked capacitor potential solutions [1.1, 1.43].

| **Year of Production** | 2008 | 2010 | 2012 | 2014 | 2016 | 2018 | 2020 |
|---|---|---|---|---|---|---|---|
| **DRAM M1 1/2-pitch (nm)** | 65 | 45 | 45 | 32 | 22 | 16 | 16 |
| **DRAM Product** | 4G | 4G | 8G | 16G | 32G | 32G | 32G |
| **Top Electrode** | TiN | | Ru, $RuO_2$, Pt, $IrO_2$, SrRuO….. | | | | |
| **Dielectric Material** | $HfO_2$, $Ta_2O_5$, $ZrO_2$ | | $TiO_2$, STO, BST | | | | |
| **Bottom Electrode** | TiN | | Ru, $RuO_2$, Pt, $IrO_2$, SrRuO….. | | | | |

=

Table 1-V DRAM trench capacitor technology requirements [1.1].

| **Year of Production** | 2008 | 2010 | 2012 | 2014 | 2016 |
|---|---|---|---|---|---|
| **DRAM ½ Pitch (nm)** | 57 | 45 | 36 | 28 | 22 |
| **Trench structure** | **bottled** | **bottled** | **bottled** | **bottled** | **bottled** |
| **Trench circumference (nm)** | 483 | 374 | 300 | 233 | 208 |
| **Effective oxide thickness (CET)(nm)** | 2.8 | 1.8 | 1.1 | 0.7 | 0.6 |
| **Cell size ($\mu m^2$)** | 0.028 | 0.016 | 0.0104 | 0.0063 | 0.0039 |
| **Trench depth [µm], (at 35fF)** | 6 | 5.6 | 4.5 | 3.7 | 3 |
| **Aspect ratio** | 74 | 89 | 89 | 94 | 97 |
| **Capacitor structure/dielectric** | **MIS/High-κ** | **MIS/High-κ**<br>**MIM/High-κ** | **MIM/High-κ** | **MIM/High-κ** | **MIM/High-κ** |

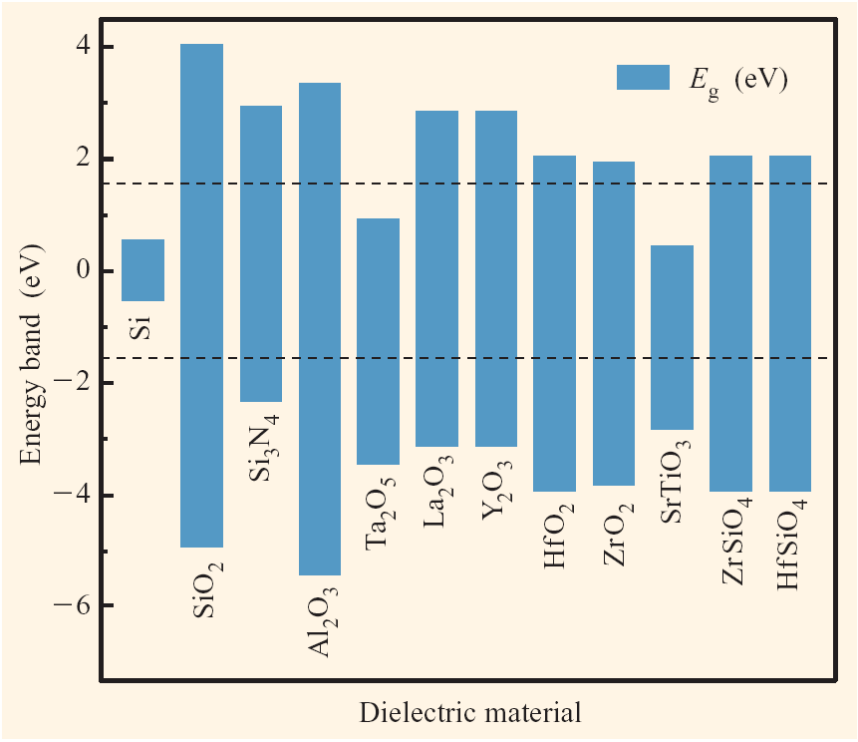



Fig. 1-1 Energy band alignment of various high-κ dielectrics with respect to silicon. Dashed lines represent 1 eV above and below the conduction and valence band, respectively, which point out the minimum barrier height to suppress the gate leakage current [1.22].

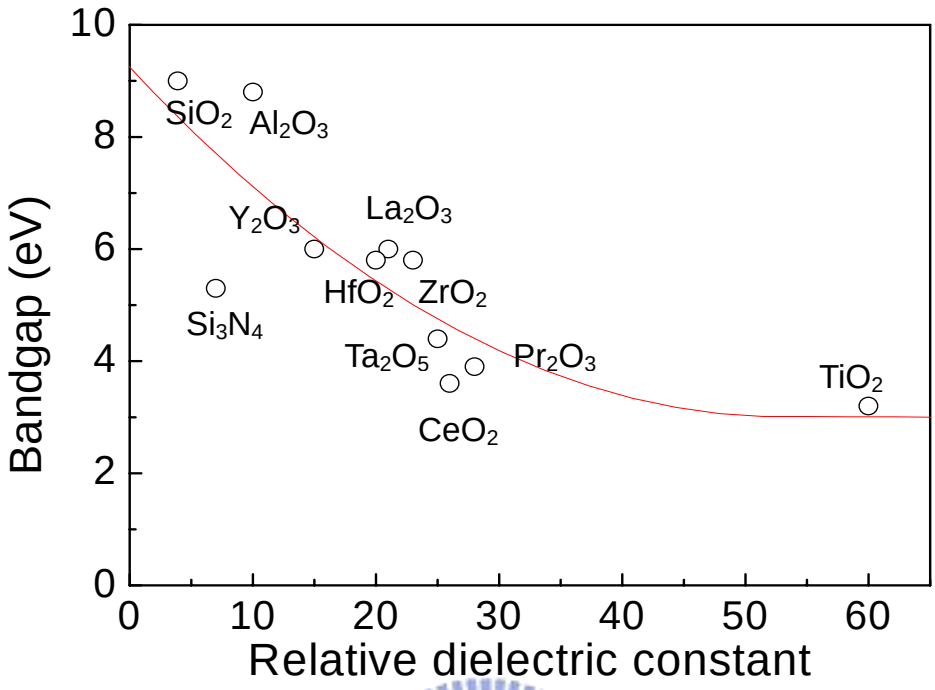



Fig. 1-2 Bandgap as the function of relative dielectric constant for various oxides [1.26].

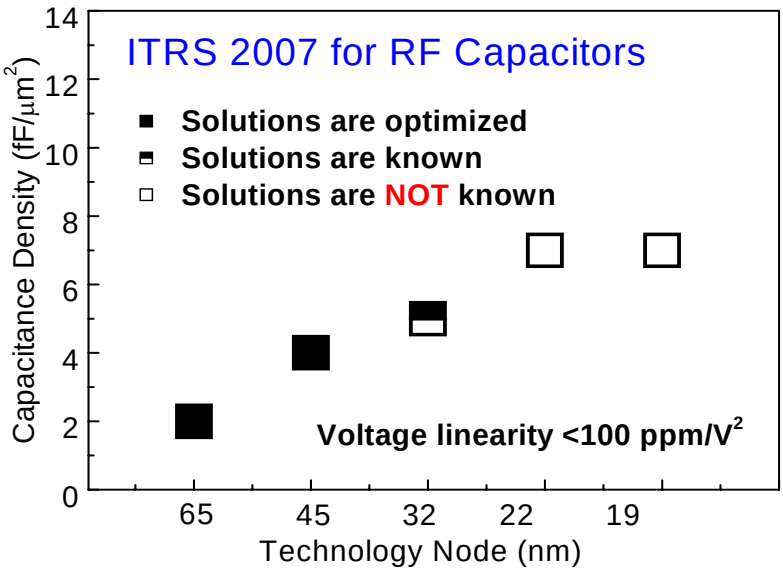



Fig. 1-3 The requirement of capacitance density for RF application verse technology node in condition of the voltage linearity < 100 ppm/$V^2$ [1.1].

# Chapter 2

# Experimental Procedure

## 2.1 Device Fabrication

Four inches diameter n-type (100) silicon wafers with a nominal resistivity of 10 to 100 Ω-cm were used as substrates. Wafers were cleaned by the standard RCA clean process to remove particles and metal ions and followed by a 300 nm thick $SiO_2$ growth by wet oxidation at 950℃ for 1 hour to ensure the substrate isolation. Then Ta(50 nm)/TaN(250 nm) bottom electrode was deposited without breaking vacuum by DC sputtering of Ta target and was patterned by the shadow mask as shown in Fig 2-1 (a)-(d). The chamber pressure during the deposition was maintained at 6 mtorr with an Ar flow rate of 30 sccm and $Ar/O_2$ flow rate of 30/1.8 sccm for Ta and TaN, respectively. Neither substrate bias nor substrate heating was intentionally applied. Ta was used to reduce series resistance and TaN acts as the diffusion barrier [2.1, 2.2] between the high-κ HfTiO and the Ta/TaN electrode.

After bottom electrode deposition, $NH_3$ plasma treatment was introduced by multi-chamber plasma enhanced chemical vapor deposition (multi-PECVD) with power of 200 W and $NH_3$ flow rate of 700 sccm for 15 min to suppress the growth of interfacial layer [2.1]-[2.5] as shown in Fig 2-1 (e). During plasma treatment, the chamber pressure was 600 torr and the substrate was kept at 300 ℃.

Before depositing of HfTiO dielectrics, $Y_2O_3$ film was deposited on some samples as shown in Fig 2-1 (f). The $Y_2O_3$ film was formed by dual E-gun evaporation using $Y_2O_3$ slits. The chamber pressure is kept at $5x10^{-2}$ torr and without substrate heating intentionally. The thicknesses of $Y_2O_3$ films were in the range of 5 to 10 nm and were controlled by quartz crystal oscillation.

Then HfTiO films were formed as depicted in Fig. 2-1 (g) via dual E-gun evaporation using the source of $TiO_2$ and $HfO_2$ slits at a substrate temperature of 25 ℃. The chamber pressure was maintained at $5\times10^{-2}$ torr. The thicknesses of HfTiO films were in the range of 10 to 40 nm and were controlled by quartz crystal oscillation. The actual thicknesses were precisely measured by transmission electron microscopy (TEM) or scanning electron microscopy (SEM).

After the preparation of HfTiO dielectrics, all of the wafers were annealed at 400℃ in $O_2$ ambient furnace for 10 to 90 min to eliminate defects and assist in fully oxidation. The selection of annealing time depends on the film thickness. It's noted that annealing temperature was kept at 400℃ for MIM capacitor fabrication to meet the thermal budget requirement of Cu back-end-of-line (BEOL) process. After formation of HfTiO dielectrics and annealing process, some samples were introduced $N_2$ plasma treatment to further improve electrical performance as shown in Fig. 2-1 (h). The $N_2$ plasma treatment was carried on by a multi-chamber plasma enhanced chemical vapor deposition (multi-PECVD) system with power in the range of 10 to 100 W and $N_2$ flow rate of 500 sccm for 20 sec to 300 sec. During the $N_2$ plasma treatment, the chamber pressure was 600 torr and substrate was kept at 300℃.

Finally, the counterparts of MIM capacitors with Pt and Al metals as top electrodes were fabricated for comparison purpose. Pt electrode was deposited by dual E-gun evaporation using Pt slits as shown in Fig. 2-1 (i) and Al electrode was deposited by thermal evaporation. The top electrode of MIM capacitors were patterned by shadow mask with area of $3.14\times10^{4}$ $\mu m^2$ in circle.

## 2.2 Material Analysis

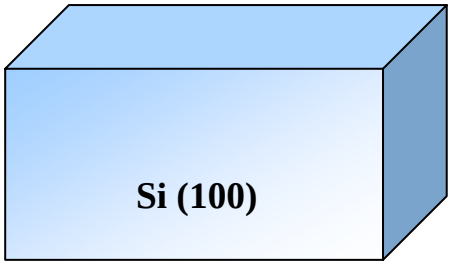
The surface roughness was measured by atomic force microscopy (AFM) working in contact mode. The scan rate was 1 Hz. The root mean square (rms)

roughness values were calculated on a 5×5 $\mu m^2$ area. The Hf:Ti ratio was detected by Rutherford backscattering spectroscopy (RBS) with 2 MeV $He^{2+}$ ions and was double checked by inductively coupled plasma-mass spectrometer (ICP-MS). The resulting spectra were analyzed by integration methods. X-ray diffraction (XRD) was employed to identify the crystal structure of the films using Cu Kα radiation with $\lambda$ =0.5418 nm. Film morphology and interfacial details were investigated by transmission electron microscope (TEM). Auger electron spectroscopy (AES) was used to determine atomic depth profile and inter-diffusion between films. AES depth profiles of the samples were carried on using $Ar^+$ sputtering. After removing top electrodes, chemical bonds in the HfTiO dielectrics and the interfacial layer between HfTiO dielectric and bottom electrode were examined by X-ray photoelectron spectroscopy (XPS).

## 2.3 Electrical Measurement

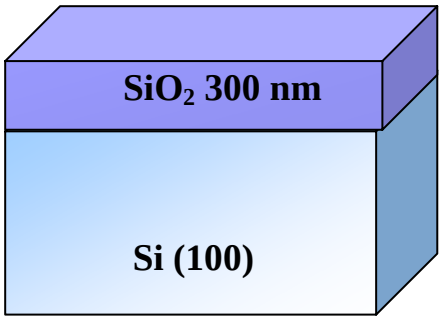
For electrical measurement, the leakage current-voltage (*J*-*V*) curves were measured by the semiconductor parameter analyzer of model Agilent 4156C. The capacitance-voltage (*C*-*V*) curves were measured by the precision impedance meter of model Agilent 4284A at frequencies varied from 100 kHz to 1 MHz by applying a small ac (25 mV) signal. To analyze the reliability of the dielectrics, constant voltage stress (CVS) was also conducted. In order to investigate the thermal stability of the high-κ dielectric film, thermal stress was carried on with measurement temperatures varied from 25 to 125℃. For all of the electrical measurement, the voltage is biased to the top electrode, while the bottom electrode is grounded.

RCA cleaned Si wafer



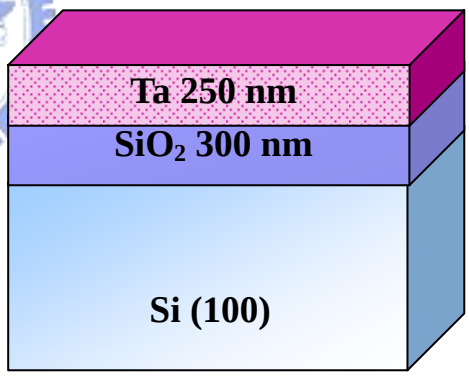

(a)

Wet oxidation 300 nm $SiO_2$



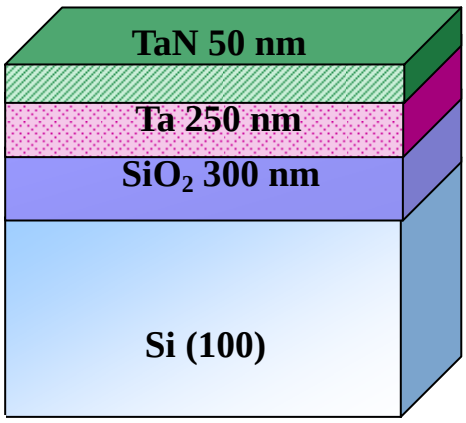

(b)

Sputtering 250 nm Ta

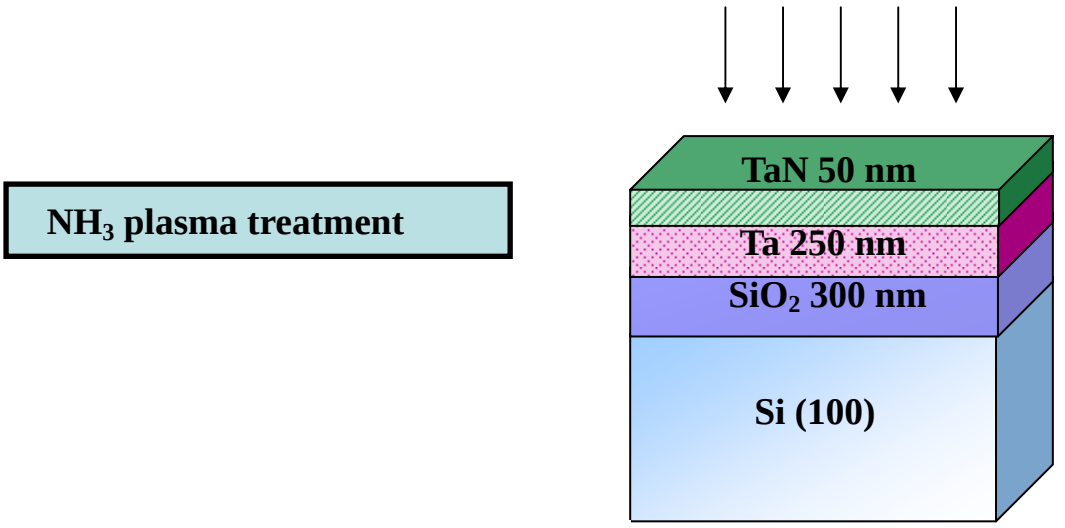



(c)

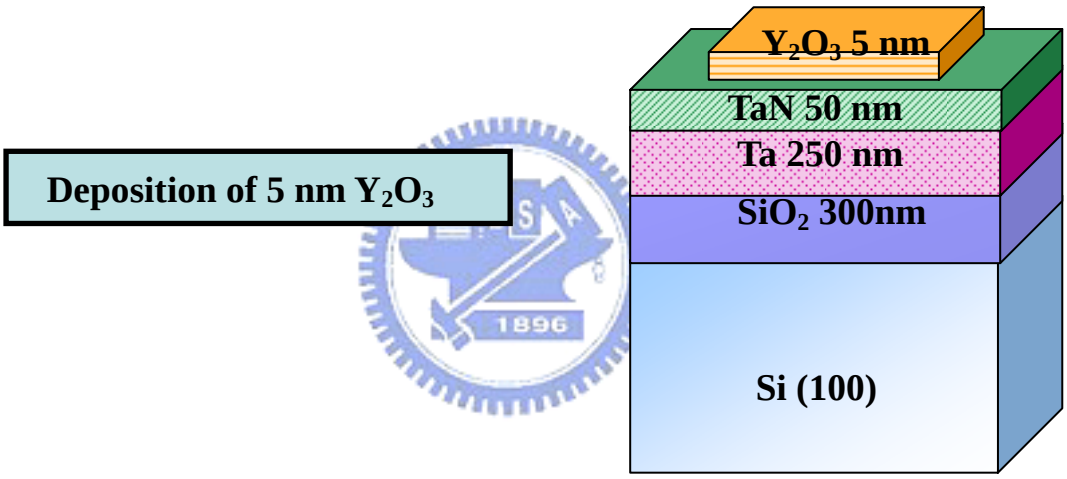
Sputtering 50 nm TaN



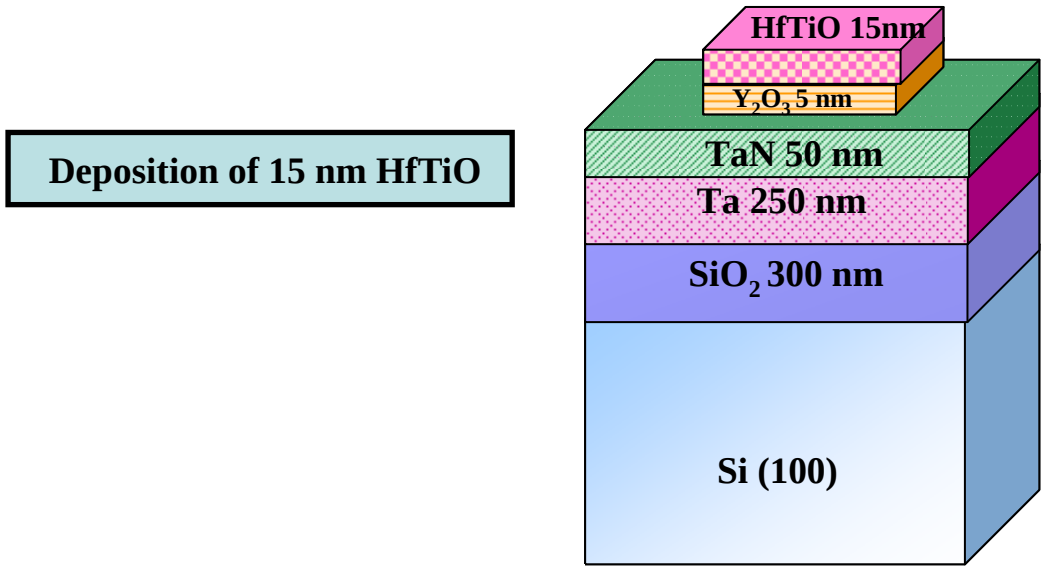

(d)


NH3 plasma treatment
TaN 50 nm
Ta 250 nm
SiO2 300 nm
Si (100)

(e)


Deposition of 5 nm Y2O3
Y2O3 5 nm
TaN 50 nm
Ta 250 nm
SiO2 300nm
Si (100)

(f)


Deposition of 15 nm HfTiO
HfTiO 15nm
Y2O3 5 nm
TaN 50 nm
Ta 250 nm
SiO2 300 nm
Si (100)

(g)

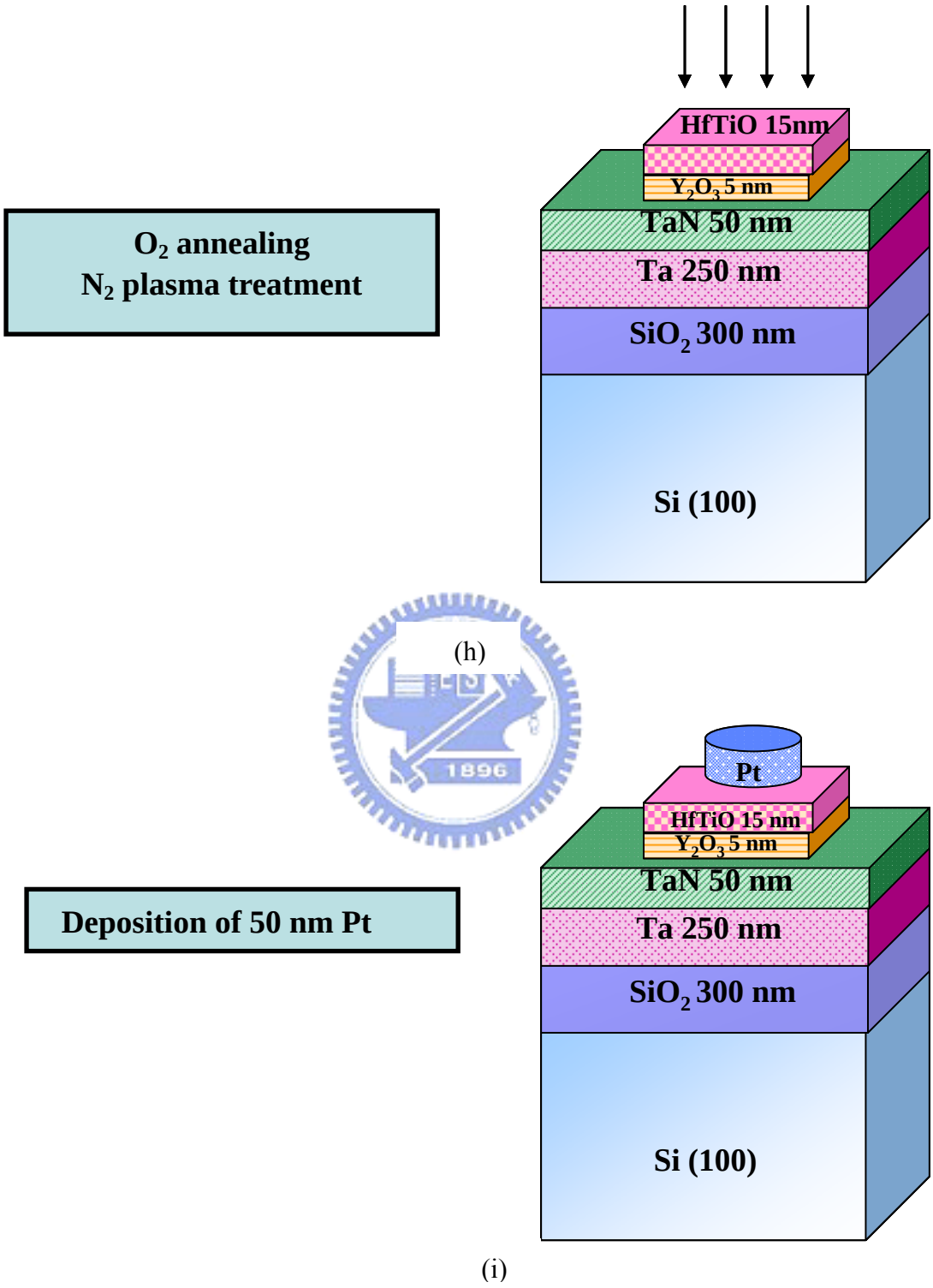



Fig. 2-1 Fabrication flow of Pt/HfTiO/$Y_2O_3$/TaN/Ta MIM capacitor.

# Chapter 3

# HfTiO MIM Capacitors for DRAM and RF Applications

## 3.1 Introduction

Dielectric materials for MIM capacitors with high dielectric constant (κ~ 20-40) have to be surveyed and researched for stacked and trench capacitors before 2010. Besides, the physical thickness of high-κ dielectric also should be scaled down to fit the minimum feature size. On trench DRAM technology, a thicker dielectric would increase the difficulty in film filling process caused by more and more large aspect ratio. On the other hand, the medium dielectric constant materials (5<κ<40) or laminated stack structure would be good solutions for RF application.

In this chapter we propose a mixed high-κ dielectric (κ~ 35–38) for DRAM/RF applications and discuss the improvement on the capacitors properties by different top electrodes and plasma treatment.

## 3.2 Basic Properties of the $HfO_2$ Doped $TiO_2$ Dielectrics

Fig. 3-1 (a) shows the Auger depth profile of HfTiO/TaN with and without $NH_3$ plasma treatment on the bottom electrode of TaN. The titanium metal penetration into bottom electrode can be observed in the samples without $NH_3$ plasma treatment. It implies that the thicker interfacial layer of TiTaO is formed at the bottom interface during PDA process. It may result in the degradation of the overall performance. In contrast, the samples with $NH_3$ plasma on bottom electrode exhibit less metal interdiffusion. This can be suggested the $NH_3$ plasma treatment passivates the bottom TaN surface, which

suppress the formation of bottom interface layer. From the bottom surface morphology analyzed by AFM spectroscopy shown in Fig. 3-1 (b), root mean square (rms) roughness of 0.35 nm and 0.57 nm were observed on the samples with or without plasma treatment, respectively. It is believed that increased surface roughness can be interpreted as an image force that lowers the barrier height for electron injection [3.1, 3.2]. Therefore, in this thesis, the bottom electrode of all MIM samples will be treated by $NH_3$ plasma.

Fig. 3-2 (a) shows the cross-sectional TEM image of the Pt/HfTiO/TaN MIM capacitor with a capacitance density of 17.6 fF/$\mu m^2$. A 19 nm-thick HfTiO dielectric with a 4.8 nm-thick bottom interfacial layer which gives a $\kappa$ value of 37 was observed. In Fig. 3-2 (b), the EDX analysis shows the compositions of interfacial layer marked in TEM picture is TiTaO. In this thesis, we only investigated the electrical properties of MIM capacitors such as leakage current mechanisms and analog properties like VCC and TCC under negative bias but those under positive bias are not discussed to avoid the disturbance due to this bottom interfacial layer. From Fig. 3-2 (c), cross-sectional TEM pattern of the Al/HfTiO/TaN MIM capacitor shows a 18 nm-thick HfTiO dielectric with 1.5 and 5.4 nm-thick interfacial layers at the top and bottom electrodes, respectively, which gives a $\kappa$ value of 39.

ICP-MS analysis identified that the ratio of $TiO_2/HfO_2$ is equal to 1.85 which is confirmed by the RBS spectra in Fig. 3-3. Fig. 3-4 (a) and (b) show that the leakage current of HfTiO dielectric is lower than $TiO_2$ dielectrics by almost five orders of magnitude at -3 V at the similar capacitance density of ~17.5 fF/$\mu m^2$. In addition, the oxidation of bottom TaN electrode and a poor interface formation after 400$^o$C-PDA will result in a larger electron tunneling current from bottom electrode than that from top electrode. From the asymmetry *C-V* curve, the more apparent voltage dispersion at

positive bias may be caused by the poor interface between bottom electrode and dielectric.

The structural properties of $TiO_2$ and HfTiO dielectrics experienced different PDA temperatures were investigated by x-ray diffraction (XRD) and the spectra are shown in Fig. 3-5. Significant (004) diffraction peak of crystallized-$TiO_2$ with an anatase phase is observed in the $TiO_2$ dielectric after 400$^oC$ annealing in $O_2$ atmosphere for 10 min. The large leakage current due to low electron barrier height and crystallization of the $TiO_2$ at low temperature is a major limitation for device applications. In contrast, the HfTiO dielectric remains amorphous even after 600$^oC$-PDA in $O_2$ atmosphere for 10 min. Importantly the spectrum of HfTiO dielectric shows no evidence of $TiO_2$ with rutile or anatase phase, even though the film was a titanium-rich metal oxide ($HfO_2$:$TiO_2$=1:1.85). It has been known that $HfO_2$ is crystallized after 600$^oC$-PDA [3.3]. Our results suggest that the crystallization phenomenon can be suppressed by the combination of the $HfO_2$ and $TiO_2$ up to 600$^oC$-PDA at least.

## 3.3 Leakage Current Improved by High-Work-Function Electrode

Fig. 3-6 shows the energy band diagram of the [Pt and Al]/HfTiO/TaN MIM capacitor. The electron affinity of HfTiO dielectric is assumed to be between 2.5~3.9 eV, which corresponds to that of $HfO_2$ and $TiO_2$ are 2.5 and 3.9 eV [3.4], respectively, and is nearly 2.55~4.15 eV reported by K. C. Chiang *et al.* [3.5]. Since electron affinity of $Ta_2O_5$ is 3.2 eV [3.4], the electron affinity of interfacial layer of TaTiO was considered to be approximately 3.4~3.9 eV [3.6] and then the variation of the electron affinity is dependent on film compositions. High work function top electrode such as Pt is expected to achieve low leakage current.

The capacitance densities for Pt and Al top electrodes are 17.5 fF/$\mu m^2$ and 19.5 fF/$\mu m^2$, respectively, calculated from the 1 MHz *C-V* characteristics shown in Fig. 3-7 (a). The capacitance densities are almost constant with varied bias from -2 to 2 V for Pt top electrode, but larger voltage dispersion for Al top electrode beyond +1.5 V bias is due to larger leakage current. The top electrode area is $3.14\times10^4$ $\mu m^2$ in circle for all of the capacitors. The difference of capacitance density for HfTiO MIM capacitors with Pt or Al top electrodes may be caused by different metal deposition process or film uniformity. From the *J-V* characteristics in Fig. 3-7 (b), the leakage current density for Pt electrode measured at -1 V at room temperature is much lower than that for Al electrode by three orders of magnitude although the capacitance density of Pt electrode is slightly lower than that of Al electrode.

The gate injected leakage currents for both Pt and Al case are contributed from not only high density of traps in dielectric caused by incomplete dielectric activation but also the different Schottky barrier heights between top electrode and dielectric. This may be due to larger work function difference between top Pt and bottom TaN electrodes increasing metal-insulator barrier height to suppress the leakage current from top or bottom carrier injection. Beside this, several phenomena such as Fermi level pinning or the formation of interfacial layer between top metal and insulator as shown in Fig. 3-2 (c) may also affect the leakage current. Therefore, current transport mechanisms should be investigated carefully.

The *J-V* characteristics of the MIM capacitor with Pt and Al as top electrodes measured at temperatures ranging from 25 to 125$^o$C are shown in Fig. 3-8 (a) and (b), respectively. A small leakage current and weak temperature dependence of $2.4\text{x}10^{-6}$ and $9.8\ \text{x}10^{-6}$ A/$cm^2$ at 25 and 125$^o$C for Pt electrode are obtained, respectively, at -3 V.

However, much high leakage currents and significant temperature dependence for Al case at 25 and 125°C are 1.01 and 11.3 A/cm$^2$, respectively, at -3 V. The thermal leakage current of high-κ MIM capacitors is very important due to the requirement of a small leakage current at high temperature for both DRAM and nonvolatile memory applications [3.7]. Moreover, it can be observed that the improvement on the leakage current at 125°C by Pt electrode is apparent and the high work function electrode of Ir also had been proved to improve high-temperature leakage current [3.8].

To recognize the leakage current mechanism of the HfTiO MIM capacitors, we take Schottky emission (SE) mechanism into consideration at low field. It is well known that SE mechanism, which the leakage current is electrode-limited and contributed by the carriers that overcome the barrier height between the electrode and the dielectric, has a linear $\ln(J/T^2)$ - $E^{1/2}$ relation as depicted by Eq. (3-2) and (3-3) [3.9, 3.10],

$$J = A^* T^2 \exp\left(\frac{\gamma E^{1/2} - \varphi_b}{kT}\right) \tag{3-2}$$

$$\gamma = \left(\frac{e^3}{4\pi\varepsilon_o K_\infty}\right)^{1/2} \tag{3-3}$$

where $A^*$ denotes the Richardson constant, $k$ is the Boltzmann's constant, $T$ is the absolute temperature (K), $E$ is the applied external electric field, $e$ is the electron charge, $\varepsilon_o$ is the permittivity in vacuum, $K_\infty$ is the high-frequency dielectric constant [3.11] (= $n^2$, where $n$ is the refractive index) and $\varphi_b$ is corresponding to the barrier height between metal/dielectric. Compared with the ideal Schottky barrier height ($\varphi_0$), the actual $\varphi_b$ usually exhibits a smaller value due to image force, surface states, and external electric field. We have plotted $\ln(J/T^2)$ versus $E^{1/2}$ curve for Pt

electrode at 25 and 125°C as shown in Fig 3-9 (a) and extracted the slopes of 0.0069 and 0.0053 eV(m/V)$^{1/2}$ at low field, respectively. The slopes yield the refractive index of 2.09 and 2.74 from the leakage current of 25 and 125°C, respectively. Since the refractive index of $TiO_2$ [3.12] and $HfO_2$ [3.13] are about 1.7-1.9 and 2.55-2.83, respectively, the refractive index extracted at low field supports that the leakage current mechanism is probably a Schottky emission. Then we use linear extrapolation to extract the Schottky barrier height (SBH) of 0.92 and 0.82 eV at 25 and 125°C, respectively. It is well known that lower SBH at higher temperature would result in increased leakage current.

For the leakage current at very low field, the leakage current increases linearly with the increase of voltage bias as shown in Fig. 3-9 (b). It presents an Ohmic conduction mechanism, which describes the thermal excitation of trapped electrons from one trap to another at low field [3.14]. It is observed that the segment of Ohmic conduction occurred at low electric field become shorter with the temperature increasing.

Fig. 3-10 shows the Schottky emission fitting for Al/HfTiO/TaN MIM capacitors at 25 and 125°C. The linear relationship of ln($J/T^2$) versus $E^{1/2}$ curve was obtained for Al electrode, which gives the slope of 0.00672 eV(m/V)$^{1/2}$ with a refractive index of 2.18 and slope of 0.0102 eV(m/V)$^{1/2}$ with a refractive index of 1.44 for 25 and 125°C, respectively. The extracted SBH for Al electrode is 0.80 eV (0.67 eV), which is slightly smaller than that of Pt electrode with 0.92 eV (0.82 eV) at 25 °C (125 °C). For Schottky barrier height, we found that the high-work-function Pt can reduce the barrier height lowering at high temperature.

The work function of Pt is around 5.6 eV and the electron affinity of HfTiO

is 2.5~3.9 eV, which gives the SBH between Pt/HfTiO is 1.7~3.1 eV in theory. However, the SBH of 0.92 eV at 25 $^{o}$C for Pt electrode is far smaller than theoretical value and this similar result was also observed from Al case. It is suspected that little difference of SBH compared to work function difference between Pt and Al electrodes may be originated by Fermi level pinning, which describes that the work function of metals on high-κ dielectrics have been observed to differ from their values in vacuum, with the discrepancy depends on the dielectrics used [3.15-3.18]. In addition, it is suspected that the interfacial layer formed between Al electrode and HfTiO as shown in Fig. 3-2 (c) was probably another reason to modulate the SBH and enhance the overall leakage current.

To investigate the leakage current mechanism of the MIM capacitors at high electric field, the ln(*J*/*E*) versus $E^{1/2}$ plots for Pt and Al electrodes are shown in Fig. 3-11 (a) and (b), respectively. The Frenkel-Poole (F-P) conduction mechanism, which is a bulk-limited current and controlled by the detrapping of the electrons from the trap centers to the conduction band of the dielectric. The F-P effect can be described as by Eq. (3-4) and (3-5) [3.7, 3.8],

$$J = BE\exp\left(\frac{\gamma E^{1/2} - \varphi_b}{kT}\right) \tag{3-4}$$

$$\gamma = \left(\frac{e^3}{\pi \varepsilon_0 K_\infty}\right)^{1/2} \tag{3-5}$$

Where *B* is the constant and $\varphi_b$ is corresponding to the trap energy level. We can extract n values of 3.06 and 2.52 from the slopes for Pt electrode at 25 and 125$^{o}$C, respectively. For Al electrode, extracted n values of 2.37 and 3.22 are obtained at 25 and

125$^{o}$C, respectively. The proper n values can explain that the leakage current at high field is the F-P conduction mechanism. To extract the trapping level of HfTiO dielectric, the ln(*J/E*)-1*/KT* relationship is plotted in Fig. 3-12 (a) and (b) for Pt and Al electrodes, respectively. Trap energy for Pt and Al electrodes is 0.44 and 0.75 eV, respectively. The trap energies are less than SBH of 0.92 eV and 0.80 eV for Pt and Al cases, respectively, which supports that the conduction mechanism at high electric field were dominated by the F-P rather than SE. Apparent difference exists in the extracted trap potential height with respect to different top electrodes. This indicates that the trap at and around the interface instead of the traps at deep level in the dielectric bulk play the major role to the conduction mechanism [3.19]. It has been observed that by incorporating Al into $HfO_2$ film, shallow trap levels will be eliminated [3.20]. In this thesis, the trapping level for Al case is deeper than that for the Pt case. It is postulated that this phenomenon may be attribute to the incorporation of Al into the HfTiO layer at the Al/HfTiO interface.

## 3.4 VCC Characteristics Improved by High-Work-Function Electrode

The capacitance variation with the varied bias is an important index for precision analog circuit application. The voltage dispersion of capacitance, which is also called voltage linearity, can be depicted as voltage of capacitance coefficient (VCC), which is related to the traps in bulk and interface layer [3.21]. The VCC is very important for analog or RF capacitors since high level of charge variation would result in the data loss and distortion [3.4]. Fig. 3-12 (a) shows the variation of $\triangle C(V)/C_0$ as a function of voltage for Pt/[HfTiO or $TiO_2$]/TaN capacitors. To depict the voltage nonlinearity, it has become customary to express the relative capacitance variation as the following equation:

$$\frac{\Delta C}{C_0} = \alpha V^2 + \beta V \tag{3.1}$$

, where $C_0$ is the capacitance at zero bias, $\Delta C = C(V) - C_0$, and α and β are quadratic and linear coefficient of the capacitance, respectively, as determined by using a second order polynomial curve fit to measured data. The parameter of β (ppm/V), which is commonly attributed to charge repartition in the dielectrics, can be cancelled by circuit design [3.22]. It will not be studied in this thesis. Quadratic coefficient of the capacitance, α (ppm/V$^2$), is extracted from the *C-V* curve measured at 100 K to 1 MHz for a voltage range from +2 to -2 V.

From the extracted VCC-α in Fig. 3-13 (a), the mixed HfTiO dielectric not only reduces the leakage current but also improves the voltage dispersion in comparison with $TiO_2$ dielectric. The VCC-α value can be effectively reduced from 8331 to 3730 ppm/V$^2$ by using HfTiO dielectric to replace $TiO_2$ dielectric. The mechanism of voltage nonlinearity would be discussed in detail in Chapter 4.

Fig. 3-13 (b) depicts the VCC-α for Pt or Al gate at 100 KHz and 1 MHz. Using the Pt top electrode to replace Al can dramatically reduce VCC-α from 6537 to 3730 ppm/V$^2$. It is noted that the high work function metal not only improved the leakage current but also VCC-α due to larger barrier height reducing the charges which are detraped from bulk or interfacial layer. Another possible reason for the poor VCC-α is the Al-incorporated interfacial layer as shown in Fig. 3-2 (c).

In order to understand the trap effect to VCC-α further, we try to discuss the experimental results at an elevated temperature. In Fig. 3-14 VCC characteristics of the Pt/HfTiO/TaN MIM capacitors were measured in the temperature range from 25 to 125$^o$C at (a) 100 KHz and (b) 1 MHz. The results show that the VCC-α increases with the

temperature from 25 to 125$^{o}$C. It could be expected that the higher charge trapping/detrapping rate of dielectric at high temperature would increase the number of mobile charges to affect the VCC-α. The Fig. 3-14 (c) plotted the VCC-α as a function of temperature at the frequency range from 100 KHz to 1 MHz for HfTiO MIM capacitors. The results present that the VCC-α deceases with the frequency and increases with an elevated temperature. In general, voltage and frequency dispersion are believed to be related to the existence of traps at electrode/dielectric interface. Some slow traps can not follow the measurement AC signal and thus do not contribute to the capacitance. In this case, the VCC-α is reduced.

In addition, the temperature coefficient of capacitance (TCC) is also an important parameter since ICs usually need to be operated at elevated temperature. Fig. 3-15 (a) and (b) show the TCC characteristics of the HfTiO MIM capacitors for Pt and Al top electrodes, respectively, with frequency dispersion. A small TCC value of 95 ppm/$^{o}$C for the Pt-electrode sample was extracted, while large TCC value of 379 ppm/$^{o}$C for the Al-electrode sample was extracted at 100 kHz. The improvement for Pt top electrode on TCC is thought to be related with charge trapping and detrapping. The Pt-electrode sample exhibits low leakage current, i.e. less charge injection. The Al-incorporated interfacial layer of the Al-electrode sample may also contribute to the poorer TCC characteristic. An increasing trend of TCC with frequency for both Pt and Al electrode is observed. At high frequency, only the fast traps can follow the AC signal for capacitance measurement. Since the trapping/detrapping time constant decreases with the increase of temperature so that more fast traps can follow the AC signal. Hence, the TCC becomes higher at higher frequency.

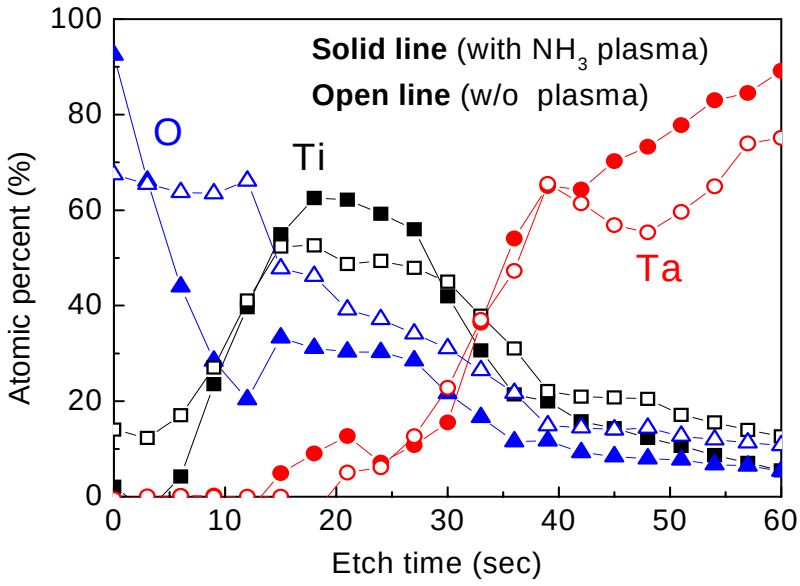
## 3.5 Effects of $N_2$ Plasma Treatment on Dielectrics

The $N_2$ plasma treatment was introduced to the HfTiO dielectrics to improve the electrical properties. With optimized $N_2$ plasma treatment condition, a power of 20 W under substrate temperature of 300$^{o}$C, the MIM capacitors exhibit lower leakage current. In Fig 3-16 (a) the improvement of almost two orders of magnitude on the leakage current at -3 V was obtained by $N_2$ plasma treatment for 20 and 40 sec. The leakage current is apparently improved at negative bias than at positive bias due to nitrogen incorporation into the top surface of the HfTiO dielectric. Besides, although leakage current decreases dramatically, capacitance density and VCC-α show no apparent variation as shown in Fig. 3-16 (b) and (c), respectively.

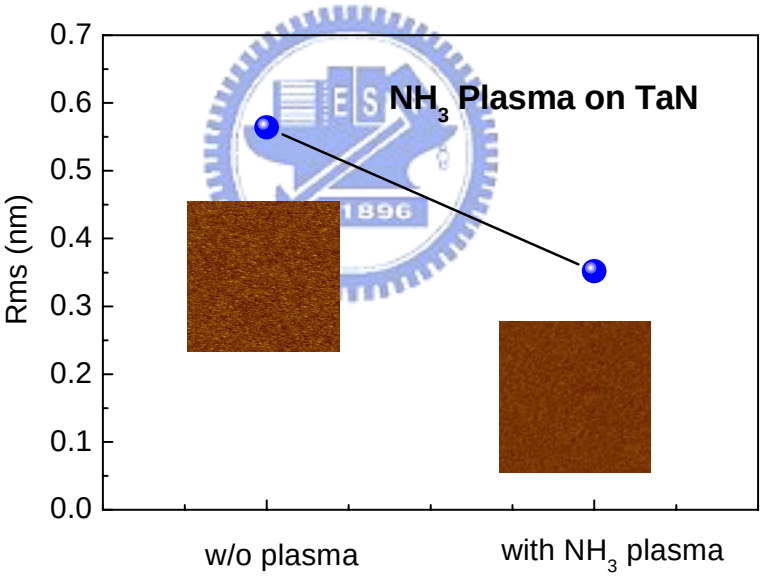
The Fig. 3-17 shows XPS depth profile for a 51 nm-thick HfTiO dielectric with and without $N_2$ plasma treatment for (a) whole elements within sputter time from 0 to 20 min and (b) the Ti, Hf snd N elements within sputter time from 0 to 6 min. Nitrogen accumulating at the surface of the HfTiO is found for the dielectric with $N_2$ plasma treatment for 40 sec. We can observe that 5% nitrogen replace oxygen and its incorporation depth is around 6 nm estimated from the sputtering rate, as shown in Fig. 3-17 (a). Umezawa *et al.* [3.23] suggested an atomistic model to explain the influence of oxygen vacancies (Vo) on electron leakage current. This theory demonstrated that two N atoms occupy the nearest neighbor O sites to Vo and are likely to couple with Vo. In the result, nitrogen possesses intrinsic effect to reduce leakage current by deactivating the Vo related gap states. In addition, N atoms incorporation can reduce the diffusion of Vo due to the consideration of total energy.

The reduction of the leakage current in $N_2$ plasma treatment samples is probably due to a decrease of surface roughness. It is known that increased surface roughness of

the dielectric would increase the local electric field at the electrode/dielectric interface which enhance electron transportation and therefore degrade the leakage property. The samples treated at 20 W for 20 and 40 sec perform root mean square (rms) roughness of 0.36 and 0.57 nm, respectively, while no plasma treated samples have rms roughness of about 0.66 nm as shown in Fig. 3-18. The plasma treated samples exhibit 0.21 nm difference on roughness and only less than two times leakage current difference. The roughness of the plasma non-treated sample is only 0.9 nm higher than the 40 sec plasma treated sample but the leakage current increase by two orders of magnitude. Since the leakage current variation is not proportional to the roughness variation well, another mechanism must be considered. Yong-kuk Jeong, *et al.* [3.24] assumed that $N_2$ plasma treatment can eliminate parasitic capacitors originated from defect or depletion between top electrodes and dielectrics; moreover, Nak-Jin Seong *et al.* [3.25] also showed that $N_2$ plasma can reduce leakage current due to microstructure densification. This explanation is more reasonable because the leakage current mechanism is changed by the $N_2$ plasma treatment as shown in Fig.3-16 (a).

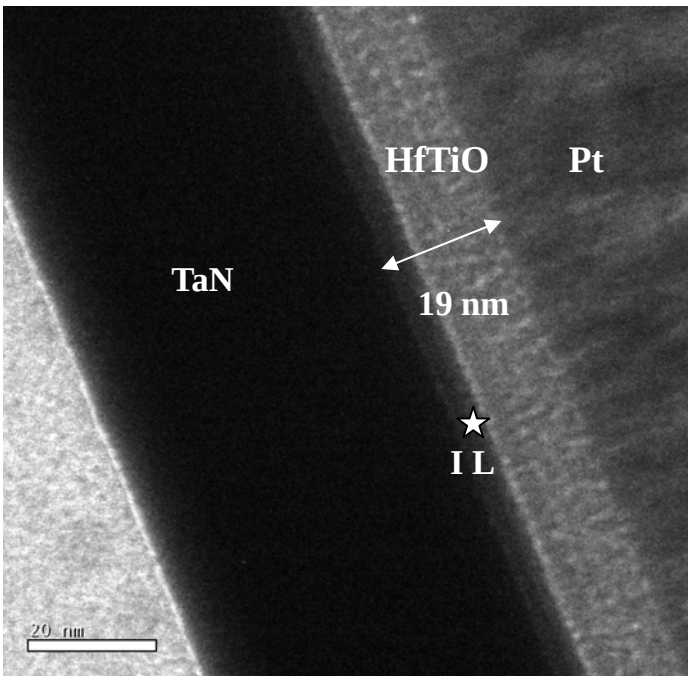



(a)

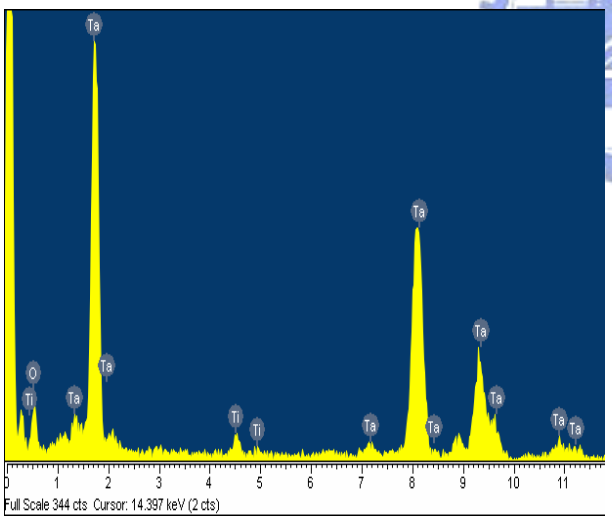



(b)

Fig. 3-1 (a) Auger depth profile of HfTiO/TaN with and without $NH_3$ plasma on the bottom electrode of TaN and (b) surface roughness of bottom electrode of TaN with and without $NH_3$ plasma treatment by AFM microscopy.

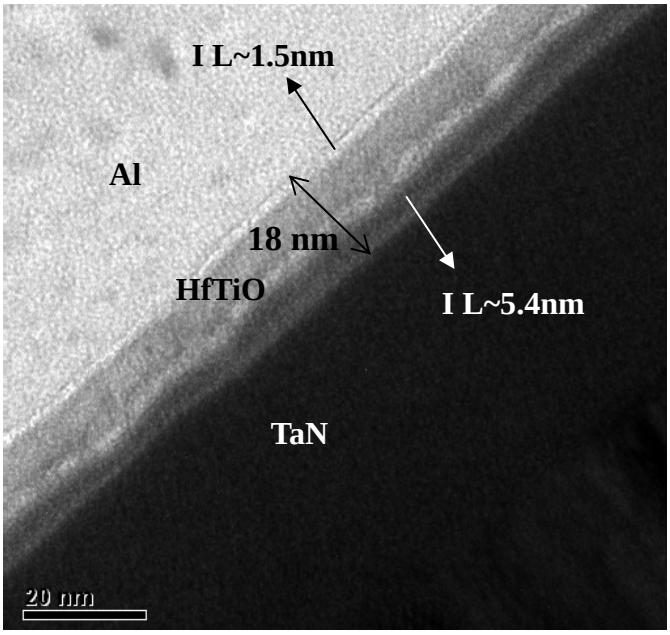



(a)




| Element | Weight (%) | Atomic(%) |
|---|---|---|
| O K | 4.67 | 34.16 |
| Ti K | 2.32 | 5.67 |
| Ta L | 93.01 | 60.16 |
| Totals | 100.00 | |

(b)




(c)

Fig. 3-2 (a) Cross-section TEM pattern of a 19 nm-thick Pt/HfTiO/TaN MIM capacitor, which gives the high-κ value of 37 and (b) the compositions of TaTiO interfacial layer by EDX analysis. (c) Cross-section TEM pattern of a 18 nm-thick Al/HfTiO/TaN MIM capacitor giving the high-κ value of 39.

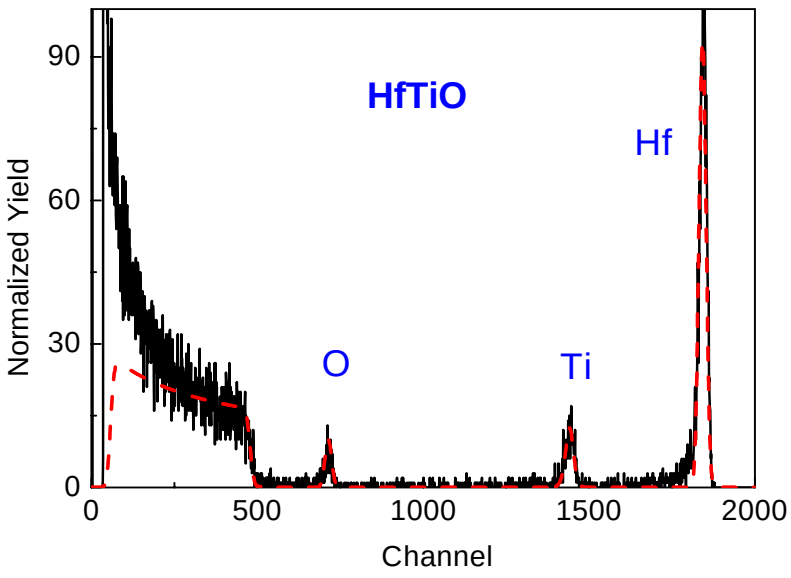
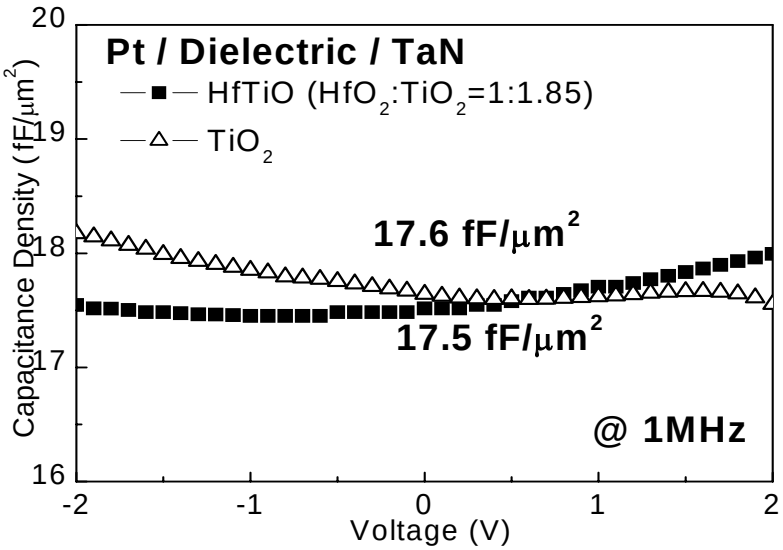
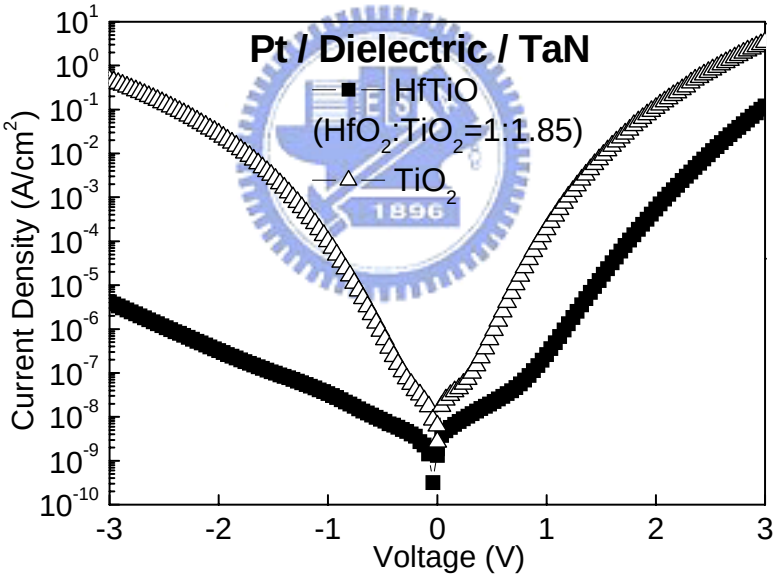



Fig. 3-3 RBS spectra of the HfTiO dielectric. The ratio of $HfO_2$:$TiO_2$ is equal to 1:1.85, which is confirmed by ICP-MS.




(a)




(b)

Fig. 3-4 (a) *C-V* and (b) *J-V* characteristics of MIM capacitors using HfTiO or $TiO_2$ as a dielectric.

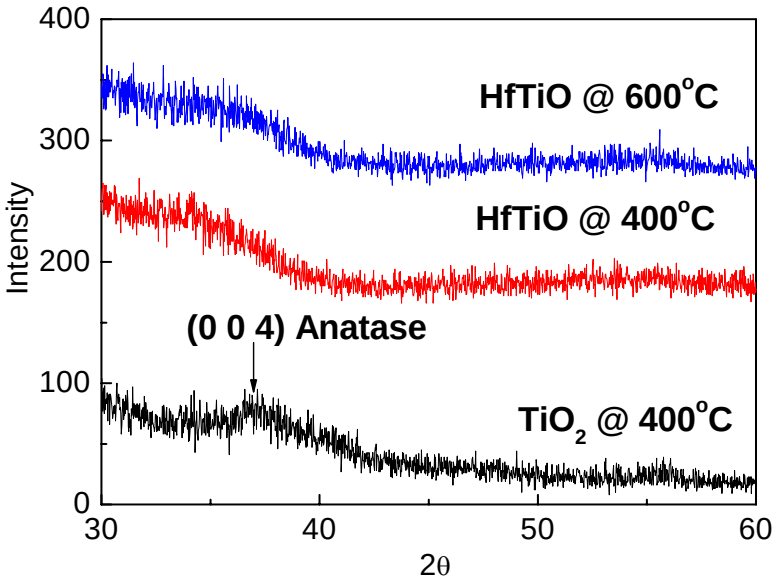



Fig. 3-5 XRD patterns of $TiO_2$ dielectric annealed at 400°C and HfTiO dielectric annealed at 400 and 600°C.

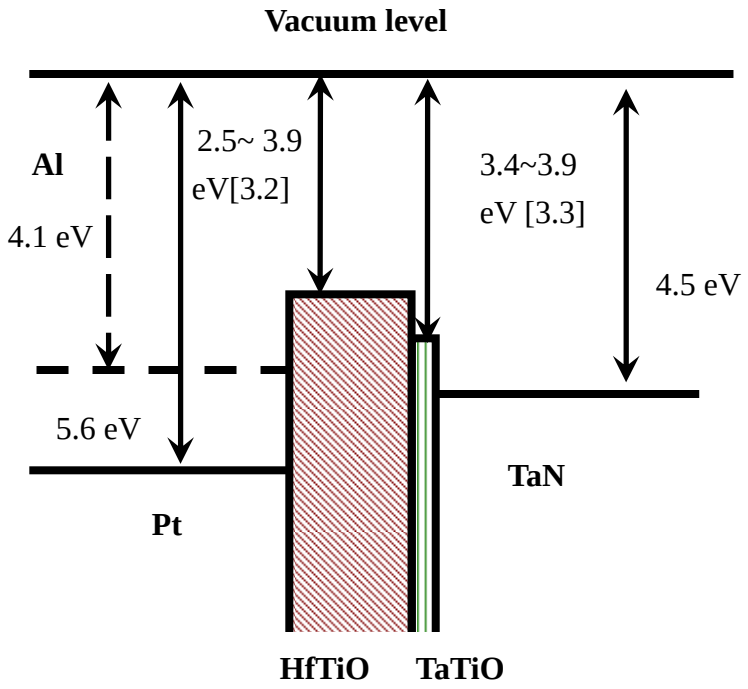
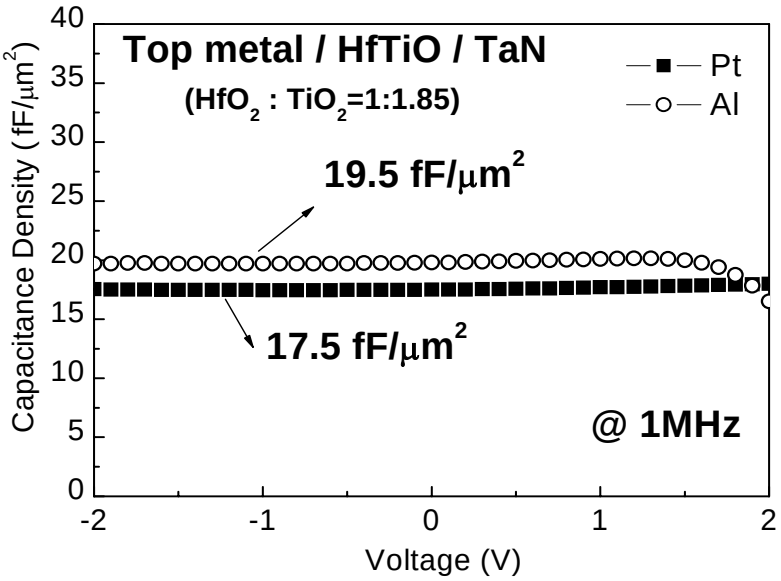
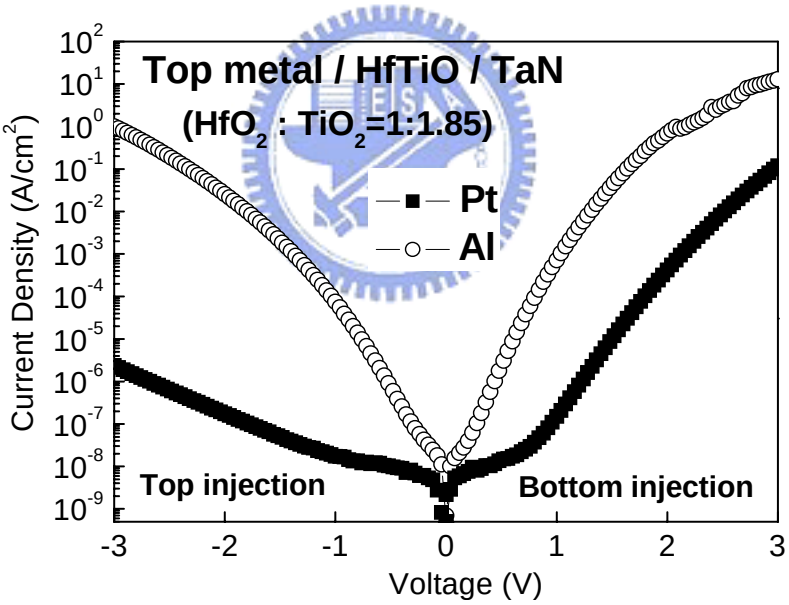



Fig. 3-6 Band diagram of a [Pt and Al]/HfTiO/TaN MIM capacitor.

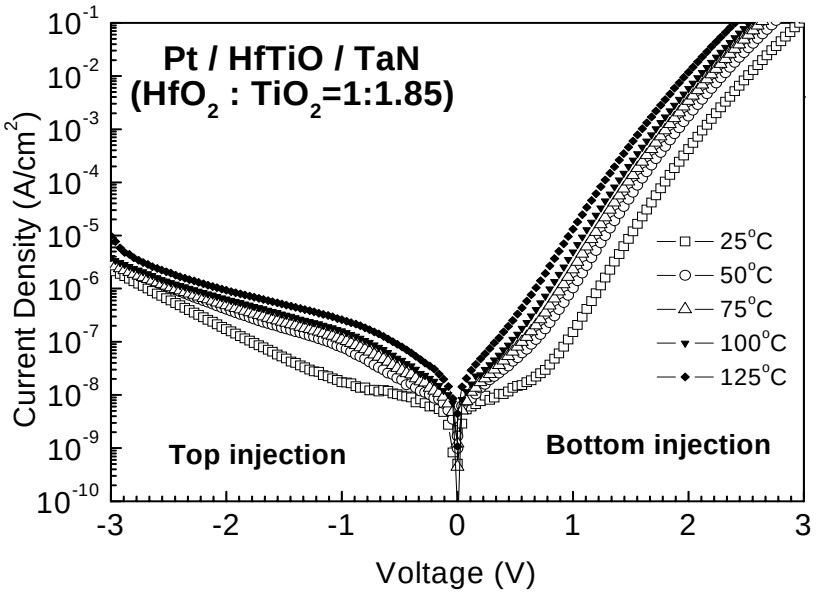



(a)

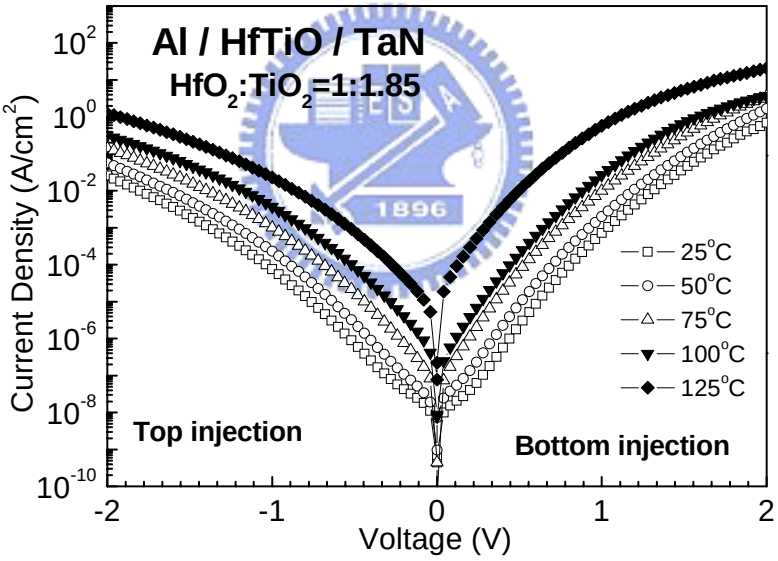



(b)

Fig. 3-7 (a) *C-V* and (b) *J-V* characteristics of HfTiO MIM capacitors with Pt or Al top electrodes.

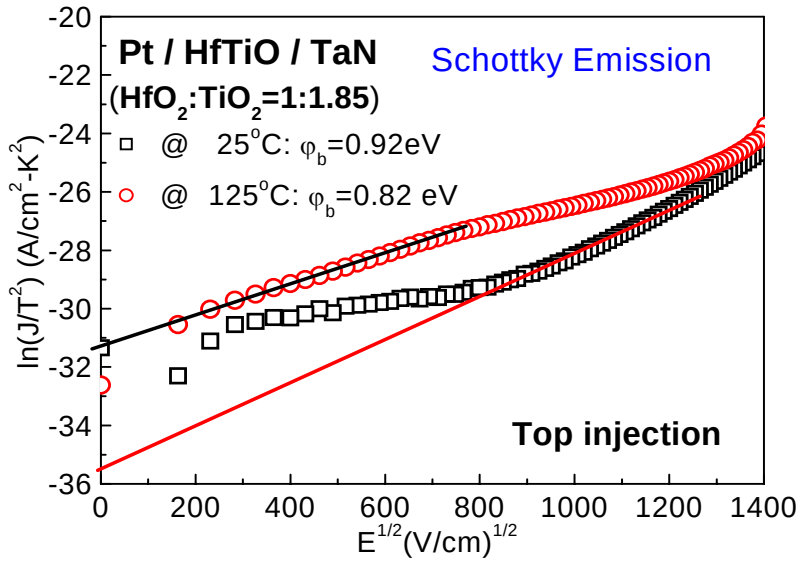



(a)

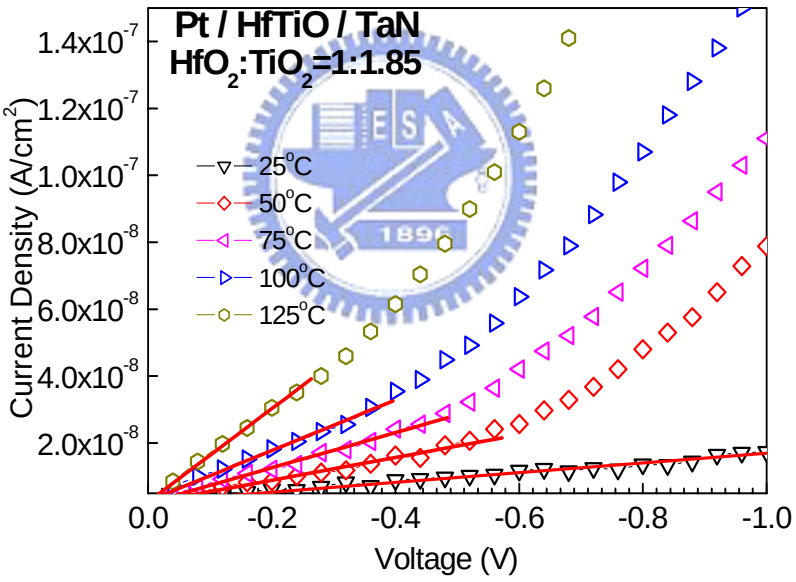



(b)

Fig. 3-8 *J-V* characteristics of HfTiO MIM capacitors with top electrodes of (a) Pt and (b) Al under varied temperature from 25 to 125°C.




(a)




(b)

Fig. 3-9 (a) Schottky emission fitting of v/HfTiO/TaN MIM capacitors at 25 and 125°C and (b) ohmic conduction fitting for Pt electrode at low electric field at 25 °C.

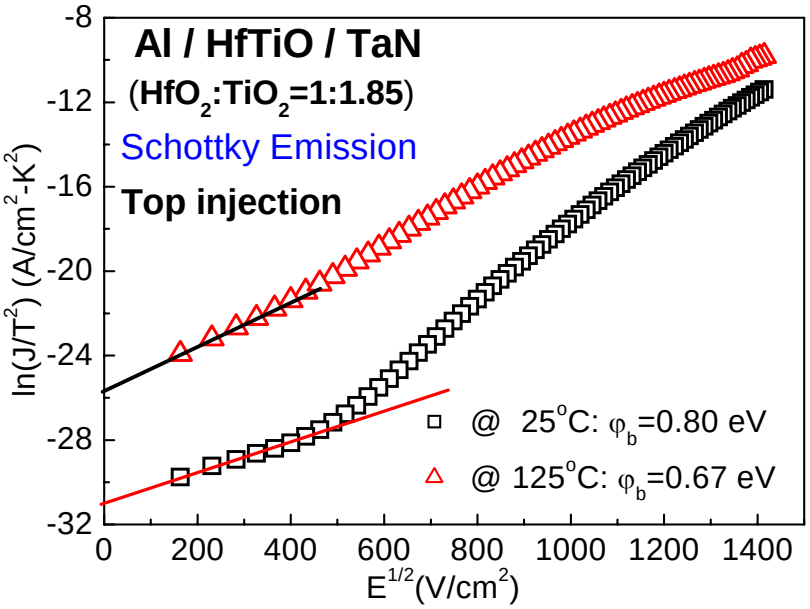
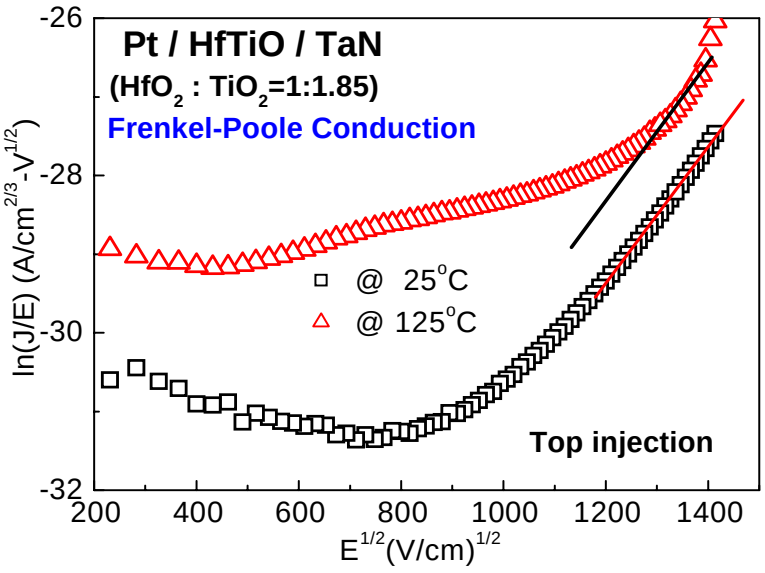
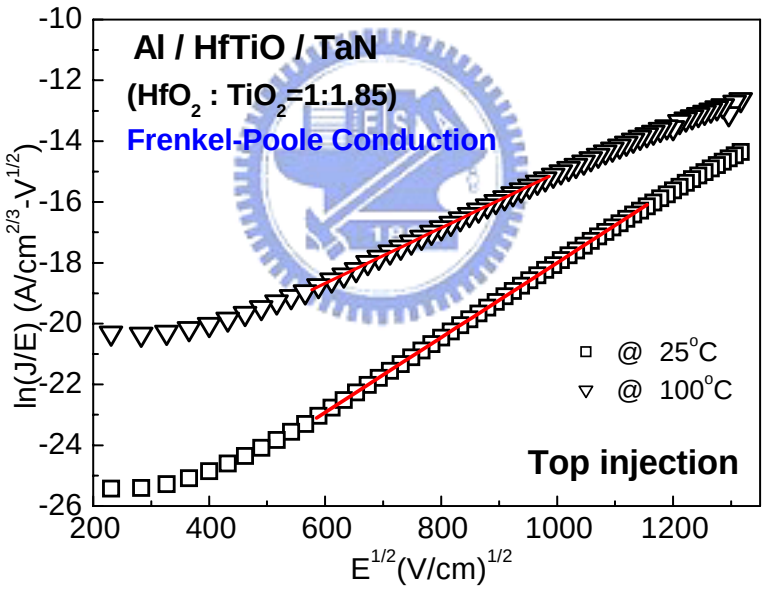



Fig. 3-10 Schottky emission fitting of Al/HfTiO/TaN MIM capacitors at 25 and 125°C.

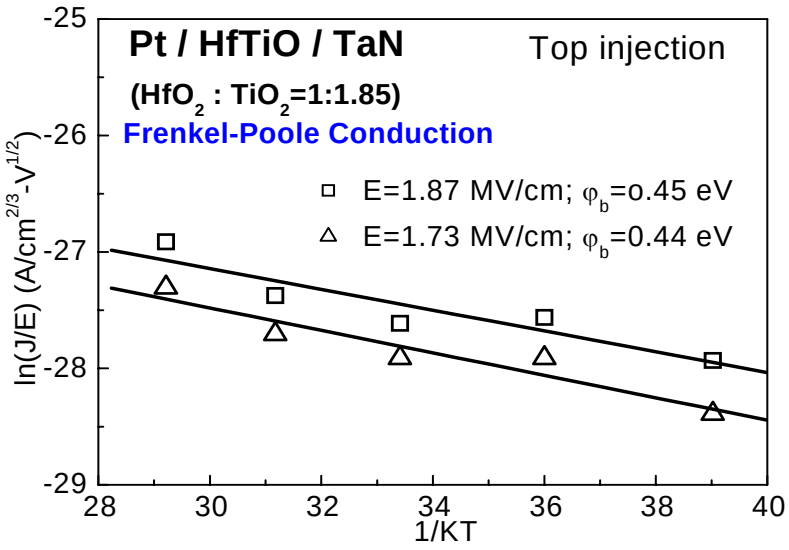



(a)

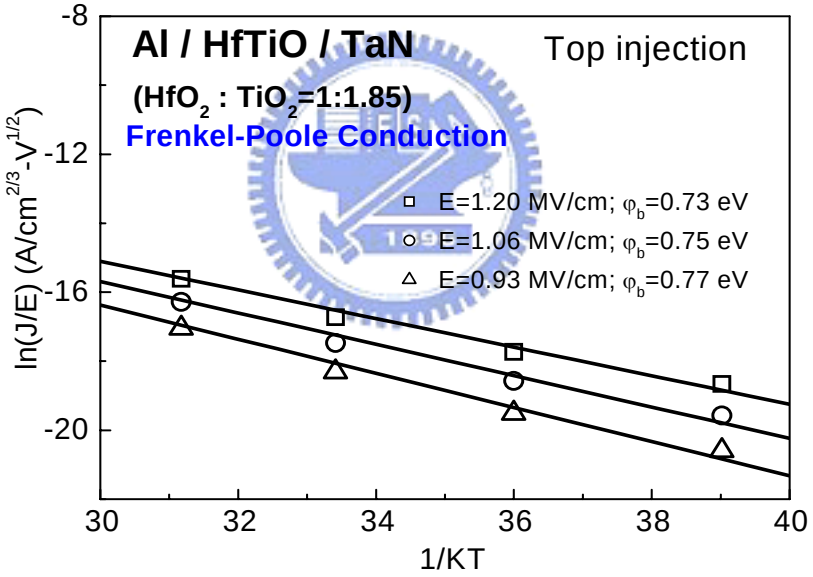



(b)

Fig. 3-11 ln($J/E$)-$E^{1/2}$ curve of Top electrode/HfTiO/TaN MIM capacitors at 25 and 125°C for (a) Pt and (b) Al electrodes.

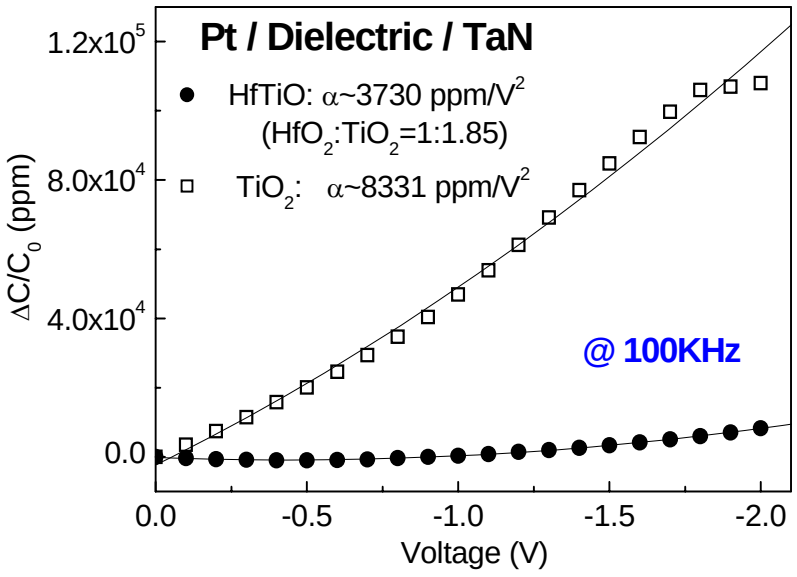



(a)

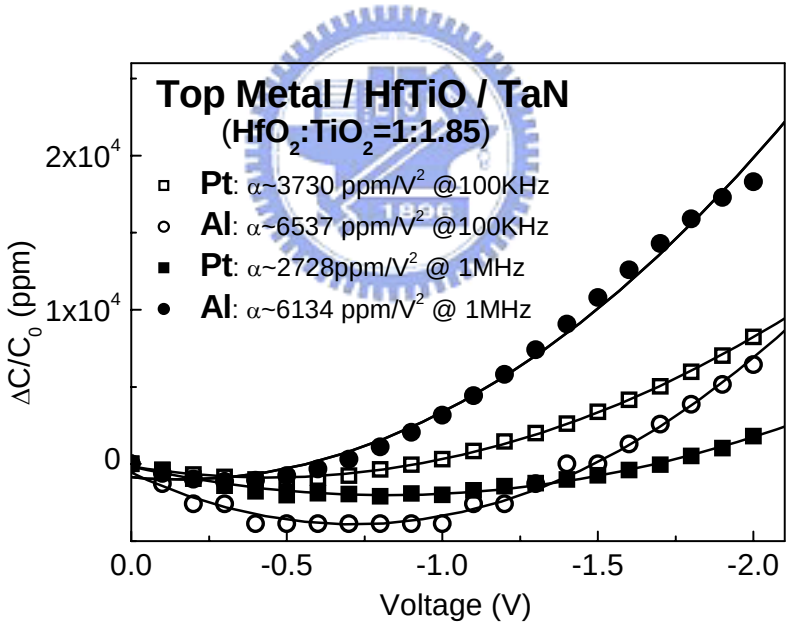



(b)

Fig. 3-12 The Frenkel-Poole conduction fitting of HfTiO MIM capacitors for top (a) Pt electrode and (b) Al electrode.

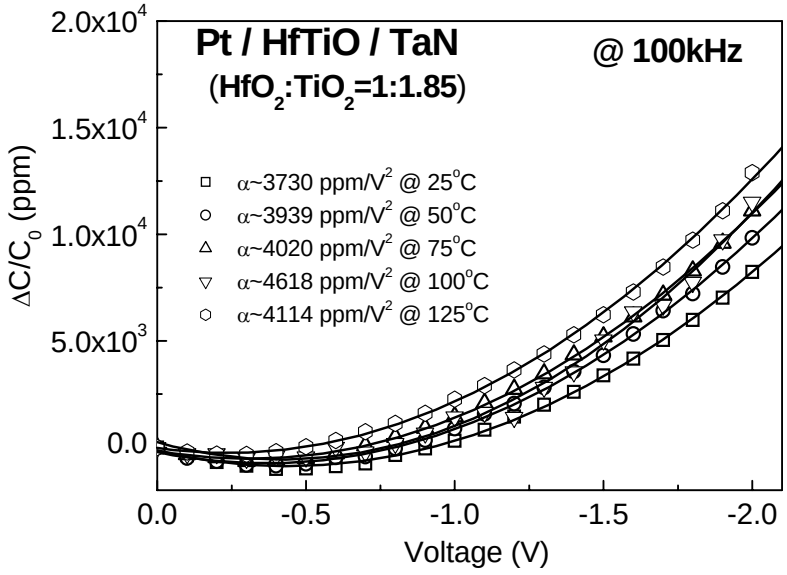



(a)

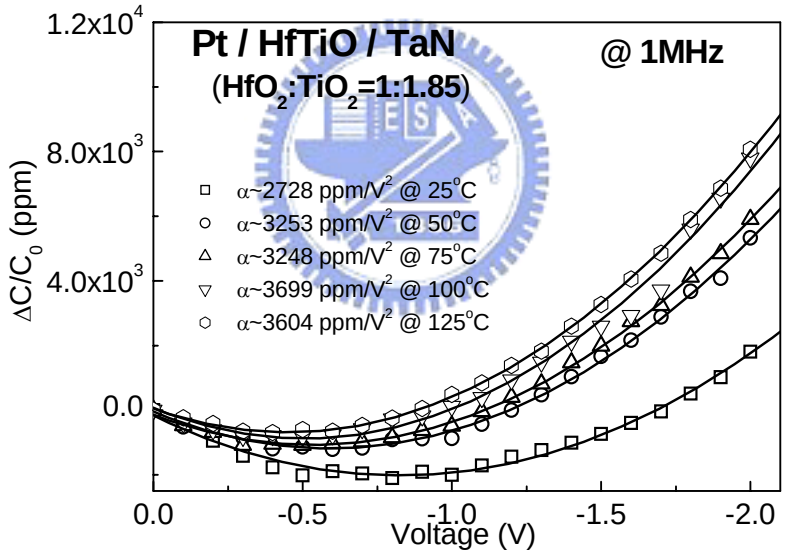



(b)

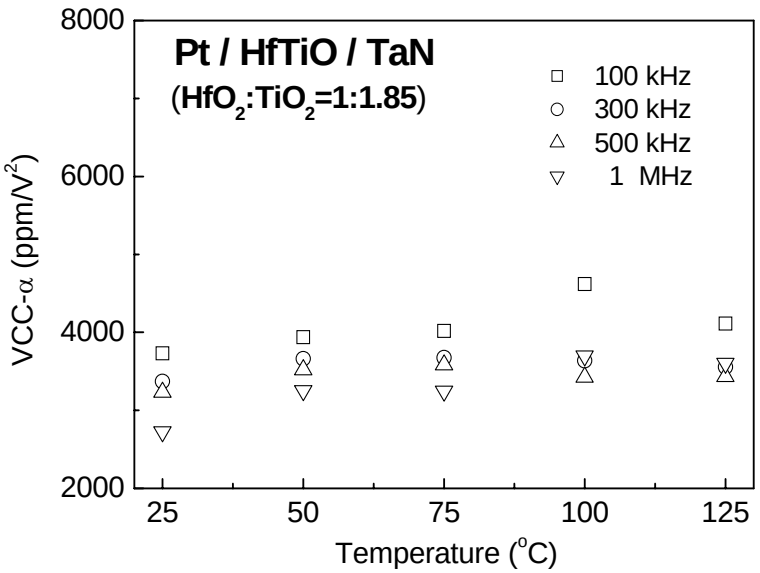
Fig. 3-13 The VCC-α characteristics of (a) HfTiO and $TiO_2$ MIM capacitors (b) [Pt or Al]/HfTiO/TaN MIM capacitors at 100 kHz and 1 MHz.


Pt / HfTiO / TaN
(HfO2:TiO2=1:1.85)
@ 100kHz
α~3730 ppm/V2 @ 25°C
α~3939 ppm/V2 @ 50°C
α~4020 ppm/V2 @ 75°C
α~4618 ppm/V2 @ 100°C
α~4114 ppm/V2 @ 125°C
ΔC/C0 (ppm)
Voltage (V)
2.0x10^4
1.5x10^4
1.0x10^4
5.0x10^3
0.0
0.0
-0.5
-1.0
-1.5
-2.0

(a)

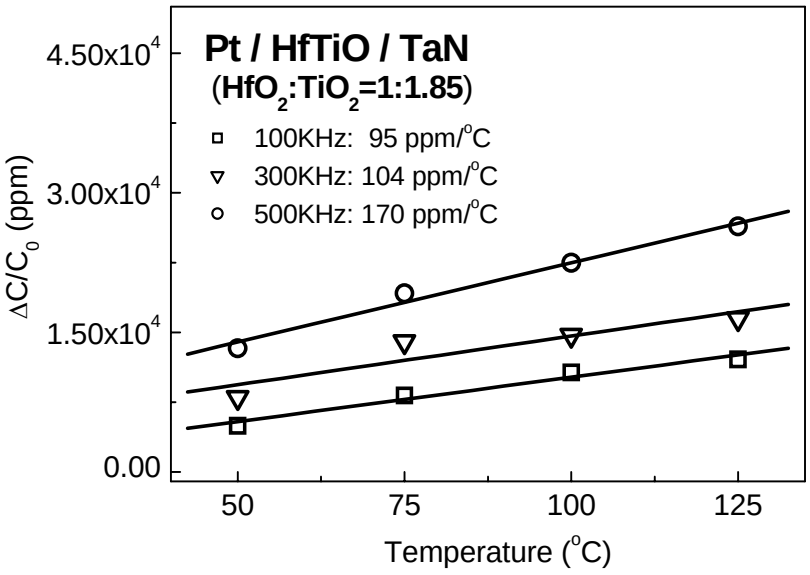

Pt / HfTiO / TaN
(HfO2:TiO2=1:1.85)
@ 1MHz
α~2728 ppm/V2 @ 25°C
α~3253 ppm/V2 @ 50°C
α~3248 ppm/V2 @ 75°C
α~3699 ppm/V2 @ 100°C
α~3604 ppm/V2 @ 125°C
ΔC/C0 (ppm)
Voltage (V)
1.2x10^4
8.0x10^3
4.0x10^3
0.0
0.0
-0.5
-1.0
-1.5
-2.0

(b)

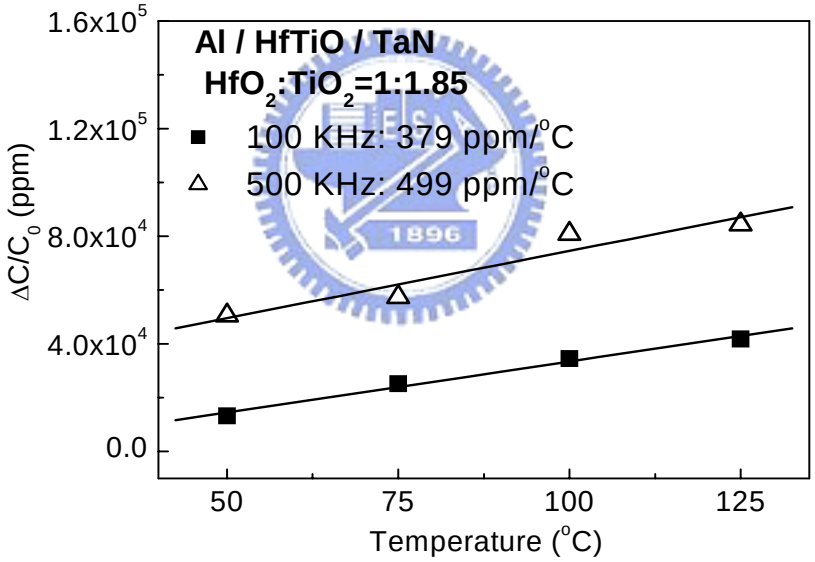



(c)

Fig. 3-14 VCC characteristics of Pt/HfTiO/TaN MIM capacitors under an elevated temperature range from 25°C to 125°C at (a) 100 kHz, (b) 1 MHz and the VCC-α as a function of temperature shown in (c)

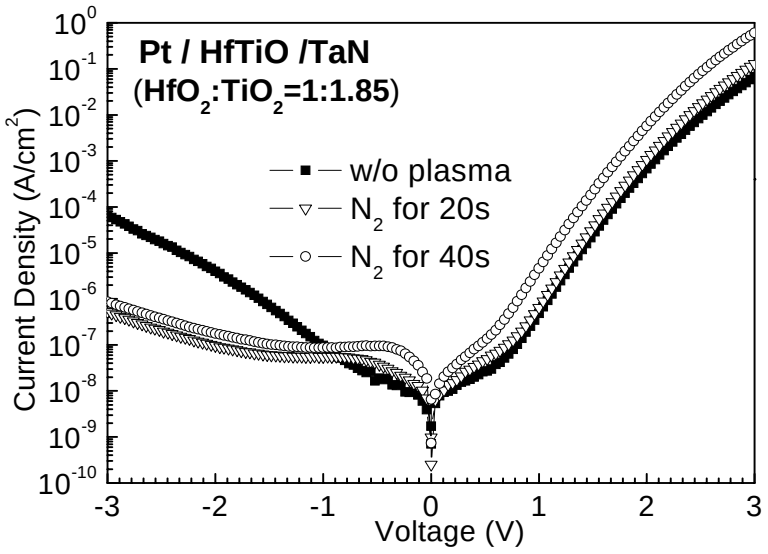



(a)

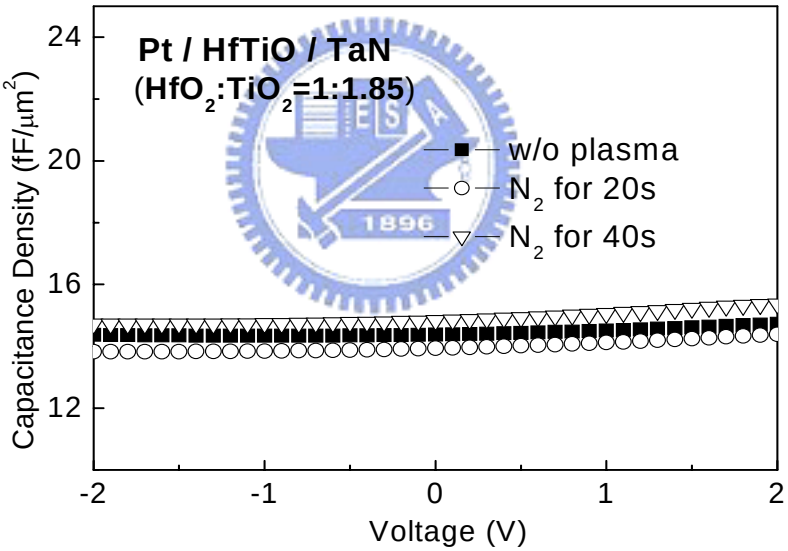



(b)

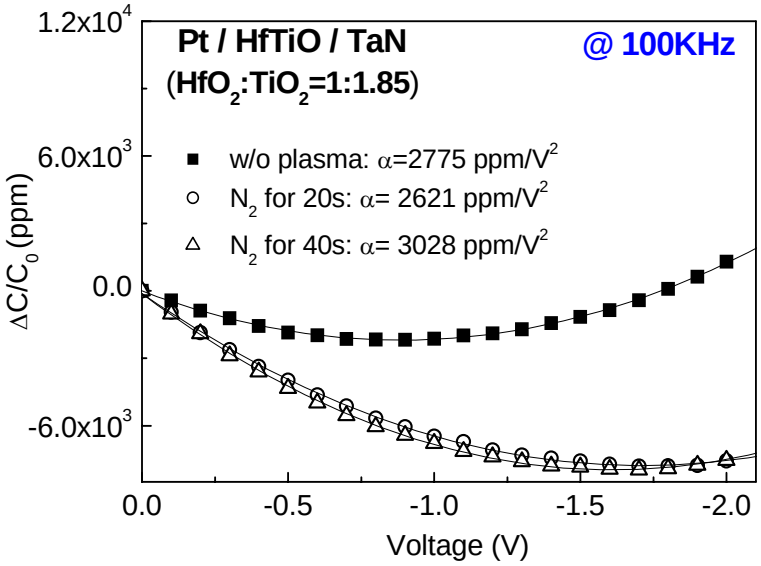
Fig. 3-15 TCC characteristics of HfTiO MIM capacitors for (a) Pt and (b) Al top electrodes at different frequencies.


Pt / HfTiO /TaN
(HfO2:TiO2=1:1.85)
w/o plasma
N2 for 20s
N2 for 40s
Current Density (A/cm2)
Voltage (V)

(a)

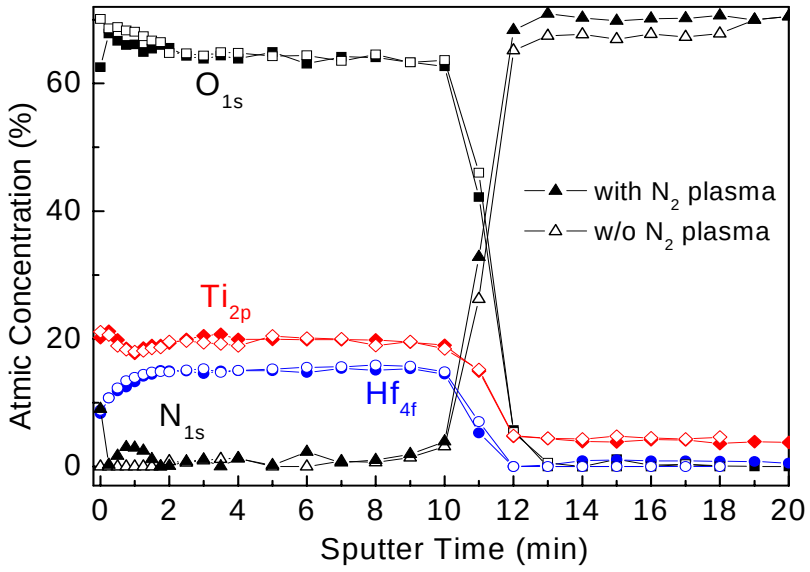

Pt / HfTiO / TaN
(HfO2:TiO2=1:1.85)
w/o plasma
N2 for 20s
N2 for 40s
Capacitance Density (fF/μm2)
Voltage (V)

(b)

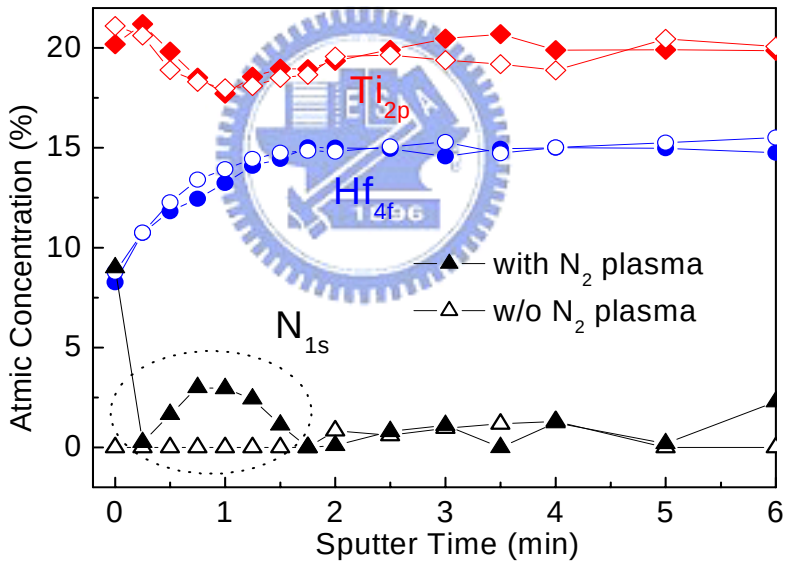



(c)

Fig. 3-16 The (a) *J-V*, (b) *C-V* and (c) VCC-α characteristics of Pt/HfTiO/TaN MIM capacitors with or without $N_2$ plasma treatment after post deposition annealing.




(a)




(b)

Fig. 3-17 XPS depth profile for HfTiO dielectrics with and without $N_2$ plasma treatment on dielectric for (a) all elements within sputter time from 0 to 20 min and (b) only Ti, Hf snd N elements within sputter time from 0 to 6 min.

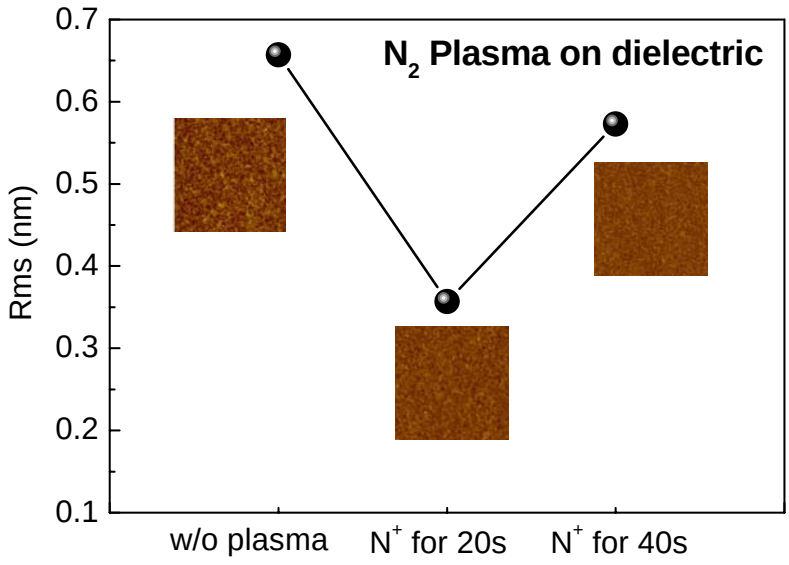



Fig. 3-18 Surface roughness of HfTiO dielectrics with and without $N_2$ plasma treatment by AFM microscopy.

# Chapter 4

# Improvement on Capacitance Behavior Dependence of Voltage and Temperature

## 4.1 Introduction

According to the ITRS 2007 [4.1], the capacitance density of RF MIM capacitors has to increase to help reduce chip size and cost of ICs. Besides the high capacitance density, low leakage current and limited thermal budget for Cu-BEOL is required. In addition, voltage linearity is an important feature that depends on many factors. According to some reports [4.2]-[4.4], this behavior is related to the existence of interface traps which induce charges with different time constants and modulate the capacitance at certain frequencies. When frequency is increasing, the induced charges will be more difficult to follow the ac signal and therefore result in lower VCC. Stephane Becu *et al.* [4.5] suggested nonlinear metal-oxide bond polarizability as a source of nonlinearity. In addition, VCC-α is known to be conversely proportional to the dielectric thickness as a function of electric field which has been demonstrated recently [4.6]-[4.8]. However, to obtain the high capacitance density, the dielectric thickness should be scaled down, which result in degradation not only the leakage current but also the voltage nonlinearity. One solution is to adopt the high-κ dielectrics, which unfortunately exhibits a very strong positive $\Delta C/C_0$ curve probably due to high degree of electric field polarization and carrier injection [4.8]. S. J. Kim *et al.* [4.9] have demonstrated that voltage linearity can be manipulated by combining a single $SiO_2$ layer with negative $\Delta C/C_0$ curve stack with the high-κ $HfO_2$ with positive $\Delta C/C_0$ curve as a laminated dielectric for the use of MIM capacitors. There is no report focusing on the engineering of dielectrics to achieve smaller VCCs for HfTiO

thin films.

In this chapter, we discuss the mechanism of VCC-α by using free carrier model and investigate the factors influencing the voltage linearity, including dielectric compositions, laminated structure, and dielectric thickness. Importantly, this is the first time to engineer the HfTiO dielectric by stacking negative $\Delta C/C_0$ dielectrics to obtain low VCC value.

## 4.2 The Physical Model of Voltage Nonlinearity

Although the physical reasons for the voltage nonlinearity are still not understood, several researches have been published recently [4.2-4.4]. In this thesis, we introduced a space charge model to discuss the related mechanism. The physical model of the voltage nonlinearity based on space charge relaxation [4.10] is also called electrode polarization [4.11]. This mechanism describes that the mobile carriers accumulated at electrode, over a Debye length. When the ac bias is applied, the accumulation region is modulated by the ac field that leads to voltage dependent double-layer capacitance. These mobile carriers are suggested to be free electrons that are injected from electrodes [4.10] or to be oxygen vacancies originated during oxide growth [4.11]. According to this model, oxygen vacancies are contributed to the double-layer capacitance which varies with frequency as

$$C = C_m\left(1+\frac{A}{1+\omega^{2n}\tau^{2n}}\right) \tag{4.2}$$

, where $C_m$ is the bulk capacitance, $A$ is an amplitude factor, and $2n$ ($0 < n < 1$) is an exponential introduced to depart from a Debye law according to Jonscher universal law [4.12]. Parameter $\tau$ is equal to

$$\tau = \tau_0 \frac{1}{2+\rho}\frac{L}{L_D} \tag{4.3}$$

, where $L_D = (\varepsilon_0\varepsilon\kappa_B T/Nq^2)^{1/2}$ is the Debye length (N is the density of mobile charges)

and ρ is the "blocking parameter," which describes the electrode transparency. $\tau_0$ is the intrinsic relaxation time,

$$\tau_0 = \varepsilon\varepsilon_0 / \sigma \tag{4.4}$$

, where σ is the conductivity, which can be written as

$$\sigma = \sigma_0 \exp(qEs / 2k_B T). \tag{4.5}$$

This is equivalent to say that the mobility is field activated with $\mu=\mu_0\exp(qEs/2k_BT)$, where s is the hopping distance of mobile carriers. Frequencies of space charge are low [4.13]-[4.15], so at the test frequencies (100 kHz-1 MHz) we are observing the high-frequency tail of the space charge relaxation. Thus, in Eq. (4.2), we can assume $(\omega\tau)^{2n} << 1$ and Eq. (4.2) is modified to

$$C=C_m(1+A\ \omega^{-2n}\tau^{-2n}). \tag{4.6}$$

Finally, an assumption is made that $C_0 \sim C_m$ and insert Eq. (4.3)-(4.5) in Eq. (4.6), one gets

$$\frac{\Delta C}{C_0} = \frac{2}{(\varepsilon\varepsilon_0)^{2n}}\left(\frac{L}{L_D}\right)^{1-2n} \frac{1}{(\rho+2)^{2(1-n)}} \frac{1}{\omega^{2n}} \sigma_0^{\ 2n} \times \left[\exp(nqEs / k_B T) - 1\right]. \tag{4.7}$$

From Eq. (4.7), we can predict that $\Delta C/C_0$ should decrease with frequency increasing ($\omega^{-2n}$, $0 < 2n < 1$) and should increase with the leakage current ( $\sigma_0^{\ 2n}$). In addition, a field activated mobility is introduced that leads to an exponential increase of the capacitance with bias. These are all verified by experimental data mentioned below.

The parameter ρ depends on the charge transfer rate at the electrode-dielectric interface. Therefore the parameter ρ can also predict that *C*-*V* characteristics should depend on electrode nature. In previous chapter, it has been confirmed that voltage nonlinearity is strongly dependent on electrode nature. A decrease of voltage nonlinearity is achieved by using Pt electrode to replace Al electrode. This experimental result confirms that the electrode effect dominate the voltage

nonlinearity rather than bulk effect such as a field dependent polarization [4.16]. F. El Kamel *et al.* [4.17] suggested that voltage nonlinearity decreases as the work function of metal increases and concluded that the reduction of top electrode work function is to increase electron injection and so to increase the concentration of electrons hopping between oxygen vacancies. This explains the accumulation of electrons at electrodes and the increase of double-layer capacitance which results in higher voltage nonlinearity.

## 4.3 The Methods to Improve the Voltage Nonlinearity

### 4.3.1 Effect of $TiO_2/HfO_2$ Ratio

In this sub-section, the effects of $TiO_2/HfO_2$ ratio on the HfTiO characteristics are examined. The $TiO_2/HfO_2$ ratios were determined by RBS and ICP-MS analysis and the HfTiO thicknesses were determined by cross-sectional TEM inspection. The TEM and RBS results of the samples with higher $TiO_2/HfO_2$ ratio have been shown in previous chapter and those with lower $TiO_2/HfO_2$ are shown in Fig.4-1.

In Fig. 4-2(a), the *C-V* characteristics of HfTiO dielectric with the $TiO_2/HfO_2$ ratio of 1.1 and 1.85 shows capacitance density of 13 and 16 fF/μm$^2$, respectively. The physical thickness of the 13 fF/μm$^2$-density HfTiO is about 17 nm by TEM inspection and is shown in Fig. 4-1 (a), which translates a κ-value of ~25. The asymmetry *J-V* characteristics of HfTiO dielectric in Fig. 4-2 (b) is attributed to the metal work function difference between the top (Pt~5.6 eV) and bottom (TaN~4.5 eV) electrodes. In addition, the lower leakage current for the sample with ratio of 1:1.1 than that of 1:1.85 could be due to higher tunneling barrer height because of more $HfO_2$ with a $\Delta E_c$ of ~1.4 eV in HfTiO dielectric.

It has been proved that lower band offset between electrode and dielectric results in serious thermal leakage [4.18]. The conduction band offset of $HfO_2$ is about

1.4 eV and is larger than that (~0.1 eV) of $TiO_2$ [4.19]. The more $HfO_2$ doped into small band gap $TiO_2$ will reduce the thermal leakage and the expected result is shown in Fig. 4-3 (a). As shown in Fig. 4-3(b), HfTiO dielectrics with the $TiO_2/HfO_2$ ratio of 1:1.1 and 1:1.85 both show a slight variation of leakage current dependence on temperature in range from 25°C to 125°C. However, it is easy to observe that the leakage current density of the $TiO_2$-rich dielectrics (the ratio of 1:1.85) increases by nearly one order of magnitude than that of the $HfO_2$-rich dielectrics (the ratio of 1:1.1) since $HfO_2$ has the merit of higher energy band gap and $\Delta Ec$, compared to $TiO_2$, against thermally activated carriers.

To investigate the leakage current mechanism of Pt/HfTiO/TaN capacitors with different $TiO_2/HfO_2$ ratios, the SE mechanism was obtained from the $\ln(J/T^2)$ - $E^{1/2}$ relationship, as shown in Fig. 4-4 (a). The extracted slopes of 0.00729 $eV(m/V)^{1/2}$ yielding the refractive index of 2.02 for $HfO_2$:$TiO_2$=1:1.1 sample. Then higher SBH of 0.95 eV is extracted for the ratio of 1:1.1 compared to that of 1:1.85 (0.92 eV) by linear extrapolation. The fitting results confirm that the $HfO_2$-rich dielectric (the ratio of 1:1.1) with a higher barrier height to result in a lower leakage current. At high electric field, the F-P leakage mechanism observed apparently from the sample with $TiO_2/HfO_2$ ratio of 1:1.85 is due to bulk-traps. Increasing $HfO_2$ substantially delays the on-set of the F-P conduction mechanism from the sample with $TiO_2/HfO_2$ ratio of 1:1.1. Fig. 4-4 (b) shows the leakage current of $HfO_2$-rich dielectric (the ratio of 1:1.1) increases linearly with the increase of voltage bias, which is attributed to the Ohmic conduction mechanism.

From the VCC data extracted from the capacitance density-voltage characteristic in chapter 3, we can understand that doping $HfO_2$ into $TiO_2$ not only improves the thermal leakage but also lower the voltage nonlinearity. In addition, the capacitance variation with increasing voltage or temperature is believed to be

improved by high work function of electrode [4.20], since the high work function electrodes will suppress electron injection and amount of electrons hopping between vacancy sites to improve the voltage linearity [4.17]. In summary, by using high work-function-metal and large ΔEc dielectric to increase the barrier height can lower the capacitance variation effectively to obtain better VCC characteristics.

In Fig. 4-5 (a) and (b) the VCC-α of HfTiO dielectric with different ratios has been extracted. The HfTiO dielectric with the ratio of 1:1.1 shows lower quadratic-coefficient α value of 1229 and 1602 ppm/$V^2$ at 1 MHz and 100 kHz, respectively, compared to the case of the ratio of 1:1.85 with α value of 3042 and 3653 ppm/$V^2$. The lower α value is attributed to more $HfO_2$ into dielectrics to increase the relaxation time of traps.

In order to investigate the capacitance variation further at high temperature, we measured the MIM devices at 25°C or 125°C and the extracted VCC-α value are shown in Fig. 4-6 (a) and (b). In Fig. 4-6 (c), the VCC characteristic of HfTiO MIM capacitors with $TiO_2/HfO_2$ ratio of 1.1 was measured in the temperature range from 25 to 125°C at different frequencies. The trend that the VCC-α decreases with the temperature increase from 25 to 125°C suggests that relaxation time of charges is increased at elevated temperature [4.21]. However, this trend is opposite to the $TiO_2/HfO_2$ ratio of 1:1.85 as shown in Fig. 3-14 and previous reported voltage nonlinearity model [4.16, 4.17]. Therefore, further study on the physical mechanism of VCC is required.

Fig. 4-7 summarizes the VCC-α as a function of capacitance density for HfTiO dielectric with the ratio of $TiO_2/HfO_2$ is equal to 1.85 and 1.1. The trend shows that VCC-α decreases apparently with the ratio of HfTiO changing from 1.85 to 1.1.

### 4.3.2 Effect of Laminated Dielectric Structure

Fig. 4-8 shows (a) *C-V* and (b) *J-V* characteristics of the $TiO_2$, $HfO_2$ and $Y_2O_3$ dielectrics. The $TiO_2$ capacitor has the highest capacitance density of 17.6 $fF/\mu m^2$, while the capacitance densities of $HfO_2$ and $Y_2O_3$ are about 11.6 and 10.3 $fF/\mu m^2$, respectively. In addition, $Y_2O_3$ exhibits the lowest leakage current density of $4.17x10^{-8}$ $A/cm^2$, as shown in Fig. 4-8 (b). The leakage current of $Y_2O_3$ is smaller than that of $HfO_2$ by about one order of magnitude at a similar capacitance density.

In Fig. 4-9, the VCC-α at different frequencies of 100, 300, 500 kHz and 1 MHz was extracted for (a) $TiO_2$, (b) $HfO_2$ and (c) $Y_2O_3$ MIM capacitors. From the extracted quadratic-coefficient α value, $Y_2O_3$ and $HfO_2$ exhibit much better analog characteristics than $TiO_2$. Both $Y_2O$ and $HfO_2$ show the VCC-α value around 1900 $ppm/V^{2,}$ while the VCC-α value of $TiO_2$ is 8331 $ppm/V^2$ at 100 KHz. The excellent VCC-α of $HfO_2$ and $Y_2O_3$ in comparison with $TiO_2$ is probably due to better interface property such as low parasitic capacitance caused by depletion and defects [4.18].

From Fig. 4-10 (a), the $HfO_2$ and $TiO_2$ capacitors show positive VCC-α values of 1991 and 8331 $ppm/V^2$, respectively, but the $Y_2O_3$ capacitor shows a negative VCC-α value of 1805 $ppm/V^2$ at 100 kHz. It has been confirmed by combining a positive-α material with a negative-α material can obtain a low VCC-α value. According to S. J. Kim *et al.*'s research, they used a $HfO_2$ film with positive α value to stack with a $SiO_2$ with negative α and found that adding $SiO_2$ results in a faster drop in α because of the canceling out effect due to the negative α of $SiO_2$ [4.9]. Fig. 4-10 (b) presents the extracted VCC-α as a function of frequency, which α value decreases with frequency increasing for three materials. The trend is not the special case but universal phenomenon for the most materials where the charges fail to follow the ac signal at high frequencies. Among these materials, $HfO_2$ and $Y_2O_3$ dielectric show a smaller frequency-dispersion probably due to large band gap and $\Delta E_c$, compared to

that of $TiO_2$.

Fig. 4-11 depicts $\Delta C/C_0$ of the Pt/$Y_2O_3$/TaN MIM capacitor as a function of temperature at various temperatures. The extracted TCC decreases slightly from 571 to 537 ppm/$^oC$ with frequency increasing from 100 to 500 kHz. It indicates that little frequency dependents on TCC. It is interesting that the trend of TCC properties is opposite to the HfTiO dielectric.

In addition, $Y_2O_3$ dielectrics attract much attention due to having the negative VCC-α around 1800 ppm/$V^2$ at 100 KHz without crystallization under 400$^o$C PDA, as shown in Fig. 4-12 (a). No XRD peak for $Y_2O_3$ is observed as annealing at 600$^o$C, which means $Y_2O_3$ can maintain amorphous or nanocrystal phase at 600$^o$C. The $Y_2O_3$ without crystallization up to 700$^o$C PDA has been reported by Durand *et al.* [4.22]. The good thermal stability makes $Y_2O_3$ dielectric with large conduction band offset (~2.4 eV) become a potential candidate in both DRAM and RF region.

Using stack structure to improve electrical properties has been reported by Yong-kuk Jeong, *et al.* [4.18] and S. Jeannot *et al.* [4.23] It is a good solution for the development of MIM capacitor. According to Yong-kuk Jeong *et al.*'s research, an ultra low VCC-α and excellent leakage current were obtained by using the THT ($Ta_2O_5/HfO_2/Ta_2O_5$) multi-layered dielectric stack. S. Jeannot *et al.* also adopting the most promising high-κ materials such as $HfO_2$, $Al_2O_3$, $ZrO_2$ to stack with $Ta_2O_5$ for analog capacitor applications to achieve very low leakage currents. The stack structures are today in production to achieve more aggressive specifications, such as at least 10 fF/μm$^2$ capacitance density and lower leakage current to reduce power consumption [4.23].

In this study, we have successfully developed a HfTiO/$Y_2O_3$ laminated structure to improve electrical characteristics. The HfTiO/$Y_2O_3$ laminated structure to improve the leakage current and VCC-α is expected due to the combination of large

conduction band offset and band gap (~6 eV) of $Y_2O_3$ with negative VCC-α.

Fig. 4-13 (a) and (b) show the TEM images of the HfTiO (~7.2 nm)/$Y_2O_3$ (~4.5 nm) laminated MIM capacitors with IL~2 nm and a single 8.1 nm thick HfTiO with IL~5 nm MIM capacitors, respectively. Fig. 4-14 (a) shows the *C-V* characteristics of HfTiO/$Y_2O_3$ laminated MIM capacitors. By inserting $Y_2O_3$ layer into the HfTiO MIM capacitor, total capacitance density decreases from 15.5 to 11 fF/μm$^2$. This is attributed to a nearly 0.6 nm-increase on the total thickness and lower κ value (~15) [4.24] of the inserted $Y_2O_3$ layer. In addition, the thinner interfacial layer of $Y_2O_3$/TaN (~2 nm) compared to that of HfTiO/TaN (~5 nm) indicates that little diffusion and chemical reaction between $Y_2O_3$/TaN interface. Therefore, we inserted $Y_2O_3$ between HfTiO and TaN to reduce interfacial layer formation and avoid capacitance density degradation.

Fig. 4-14 (b) shows the HfTiO(7.2nm)/$Y_2O_3$(4.5nm) laminated structure can effectively reduce the leakage current by almost three orders of magnitude at -3 V, compared to mixed HfTiO dielectrics since the increase of nearly 0.6 nm-thickness and larger $\Delta E_c$ (~2.4 eV) and band gap of $Y_2O_3$ [4.19] than that of HfTiO.

Most importantly, in Fig 4-15 (a), the HfTiO(7.2 nm)/$Y_2O_3$(4.5 nm) laminated structure performs a good VCC-α improvement from the value of 3136 ppm/V$^2$ to 1222 ppm/V$^2$ at 100 KHz. As the thickness of $Y_2O_3$ increases to 10 nm, VCC-α can be further reduced to 892 ppm/V$^2$. Additional increase of $Y_2O_3$ thickness will degrade the capacitance density dramatically. In this thesis, 4.5 nm thick $Y_2O_3$ is the optimized condition to improve VCC-α characteristics and reduce the leakage current while maintain high capacitance density at the same time. Fig 4-15 (b) shows the VCC-α as a function of frequency for HfTiO/$Y_2O_3$ laminated with or without $Y_2O_3$ dielectrics. The HfTiO dielectric has stronger frequency dependence of VCC-α, which is undesirable for MIM capacitors application. However, the HfTiO/$Y_2O_3$ laminated

structure shows small frequency dispersion on VCC properties probably due to the better nondispersive characteristics of $Y_2O_3$ than that of $TiO_2$ as shown in Fig. 4-9.

### 4.3.3 Effect of Dielectric Thickness

To meet the 2012 ITRS requirements for an analog/RF capacitor, we try to fabricate a HfTiO MIM capacitor with a thicker thickness. A small VCC-α may be obtained with the thickness increasing, but a trade-off on capacitance density is encountered. The improvement of VCC-α with increasing dielectric thickness is attributed to the reduction of electric field [4.25]. It can be further proved by S. J. Ding *et al*. [4.26] and C. Durand *et al.* [4.27] who reported a very similar dependence of $\triangle C/C_0$ on electric field regardless of thickness. R. B. Van Dover *et al.* [4.28] also suggested that thickness dependence of VCC-α has a relation of $\alpha \propto t^{-n}$, where $t$ is the dielectric thickness.

Under the thermal budget of 400°C PDA in $O_2$ atmosphere for 60 min, a 51 nm-thick HfTiO capacitor was fabricated successfully to achieve the ITRS goals of 5 fF/μm$^2$ density, leakage current of 1x10$^{-8}$ A/cm$^2$ and VCC-α < 100 ppm/V$^2$ [4.29].

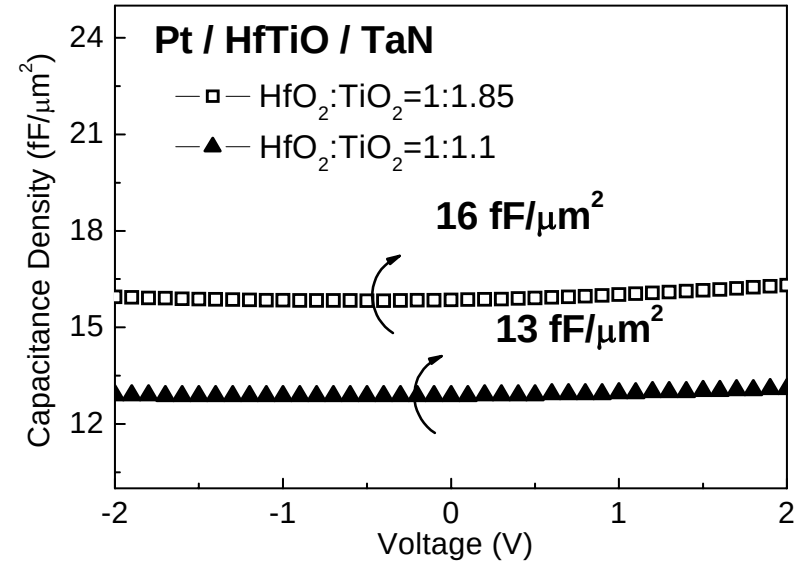
Fig. 4-16 (a) and (b) show the capacitance density of 5.1 fF/μm$^2$ and leakage current of 1.33x10$^{-9}$ A/cm$^2$ at -1 V for a 51 nm-thick HfTiO MIM capacitor. The leakage current at negative bias is markedly lower than that at positive bias due to higher work function of Pt than TaN and better interface quality between Pt/HfTiO dielectric. A very small VCC-α value of 40 ppm/V$^2$ was obtained from a HfTiO MIM capacitor with a 5.1 fF/μm$^2$ density at 100 KHz as shown in Fig. 4-17. These electrical characteristics meet the ITRS of radio frequency and analog/mixed-signal technologies for wireless communications at 2012. Fig. 4-18 shows the SEM image of a MIM capacitor with a 51 nm-thickness HfTiO, which gives a dielectric constant of ~30.

Fig. 4-19 depicts the dependence of VCC-α as a function of the inverse capacitance density (1/*C*). A decrease of VCC-α with increasing 1/*C* was observed for the $Ta_2O_5$ [4.30], $HfO_2$ [4.31], Tb-doped $HfO_2$ [4.32], and HfTiO(this work) dielectrics. The HfTiO shows a good choice to meet the ITRS requirement at 2012 than $HfO_2$, $Ta_2O_5$ and Tb-doped $HfO_2$. Besides, for the same required VCC-α < 100 ppm/$V^2$, the HfTiO dielectric can have higher capacitance density than using $HfO_2$, $Ta_2O_5$ and Tb-doped $HfO_2$.

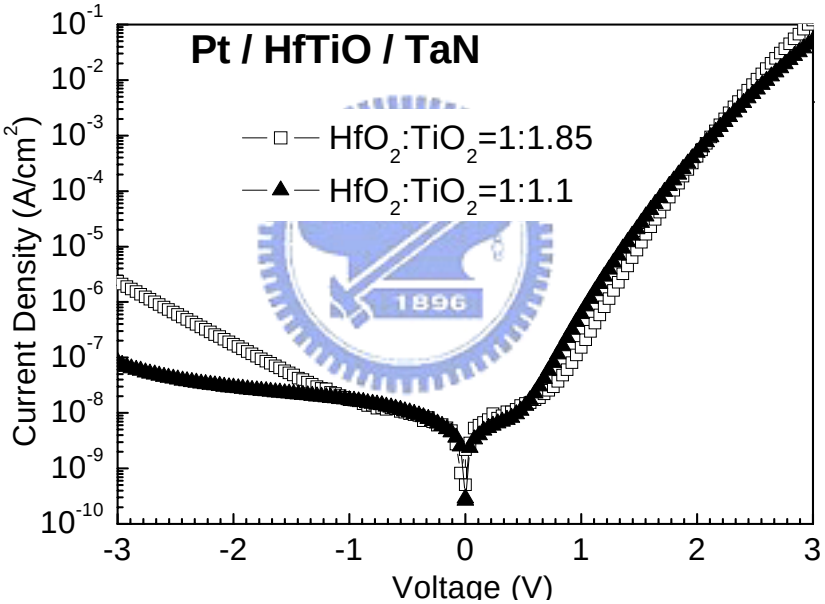
Finally, we make a comparison with previously reported high-κ MIM capacitors summarized in Table 4-I. The results show that HfTiO MIM capacitors has the highest capacitance density of 17.5 fF/μm$^2$ among these capacitors and a low leakage current of 3x10$^{-7}$ A/cm$^2$ at -2 V which is close to that of TaTiO capacitors with a lower capacitance density of 14.3 fF/μm$^2$ reported in 2005 IEDM [4.33]. In addition, the 51 nm-thick HfTiO MIM capacitor with the capacitance density of 5.1 fF/μm$^2$ meets the requirement of ITRS at 2012.

Table Ⅰ. The comparison of various high-κ MIM capacitors for the analog/RF application. In this work, the Pt/HfTiO/TaN capacitor meets the requirements of ITRS at 2012.

| | Tb-$HfO_2$ [4.31] | $HfO_2$ [4.30] | TiTaO [4.32] | **ITRS @ 2012** | **This work** | | |
|---|---|---|---|---|---|---|---|
| C Density ($fF/\mu m^2$) | 13.3 | 12.8 | 14.3 | **5** | 5.1 | 13 | 17.5 |
| J ($A/cm^2$) | $1x10^{-7}$ @ -2V | $8x10^{-9}$ @ -2V | $2x10^{-7}$ @ -2V | **< $1x10^{-8}$** | $2.8x10^{-8}$ @ -2V | $5.4x10^{-8}$ @ -2V | $3x10^{-7}$ @ -2V |
| $\alpha$ ($ppm/V^2$) | 2667 | 1990 | 634 | **<100** | 40 | 1525 | 3730 |

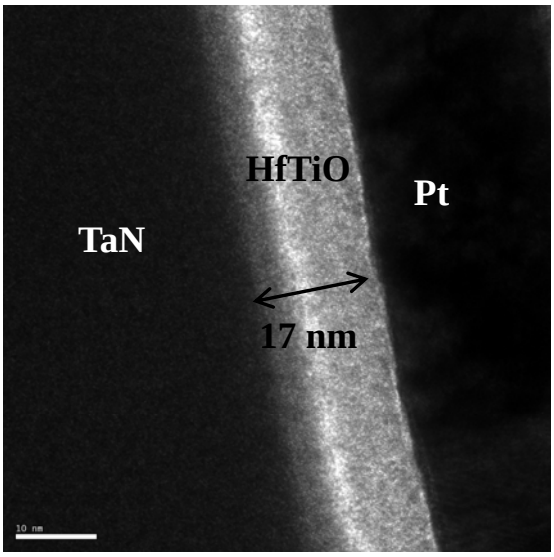



(a)

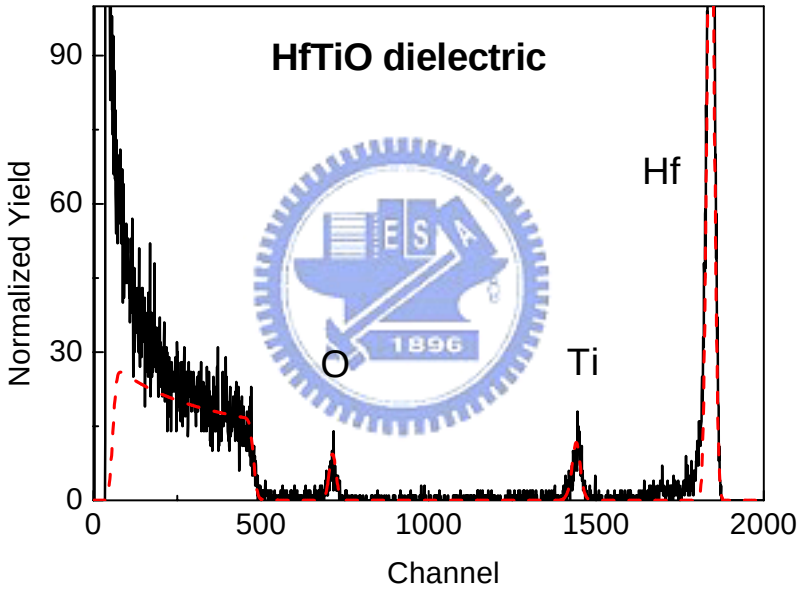



(b)

Fig. 4-1 (a) *C-V* and (b) *J-V* characteristics of HfTiO dielectric for $TiO_2/HfO_2$ ratio of 1.85 and 1.1.

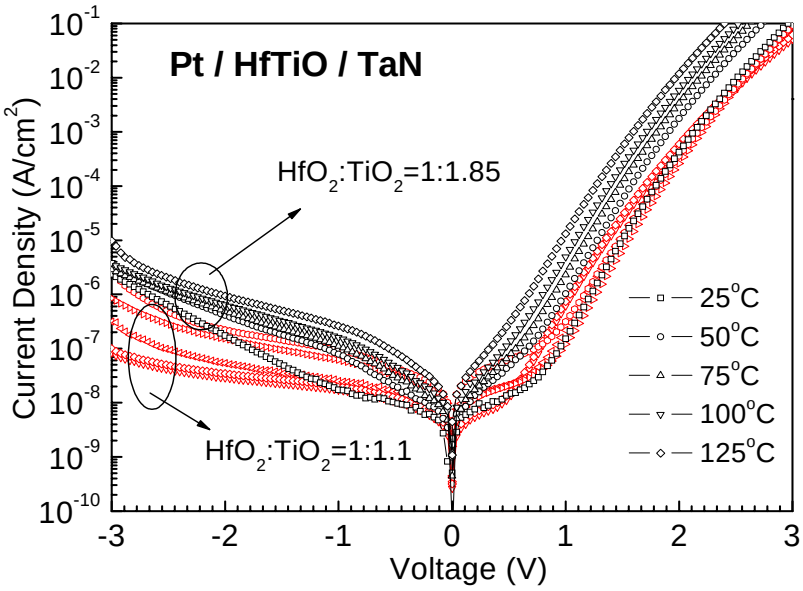



(a)

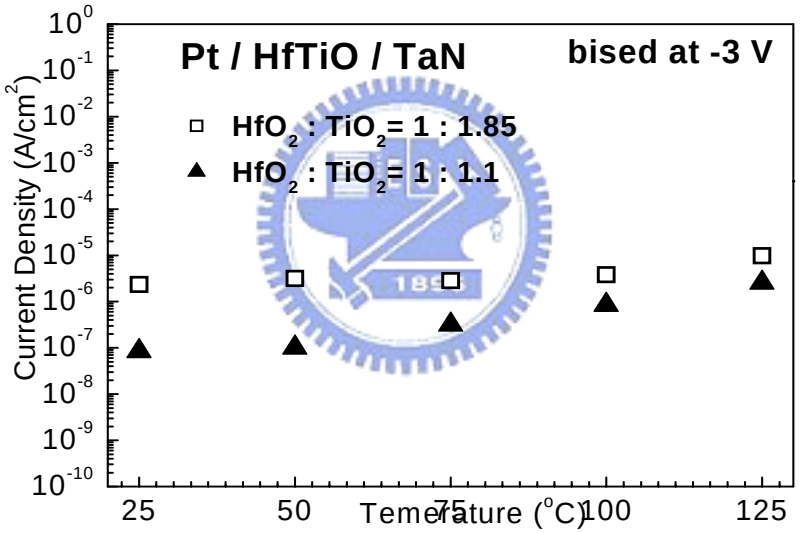



(b)

Fig. 4-2 (a) The TEM image of a capacitance density of 13 fF/μm2 HfTiO dielectric with 17 nm thickness which gives a high-κ value of 25, and (b) RBS spectra of the HfTiO dielectric. The ratio of $HfO_2$:$TiO_2$ is equal to 1:1.1, which is confirmed by ICP-MS.



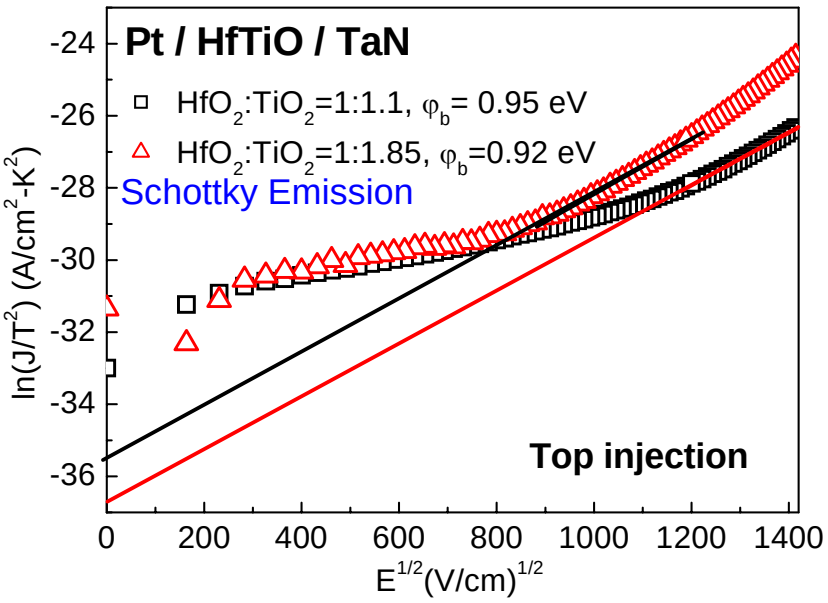

(a)



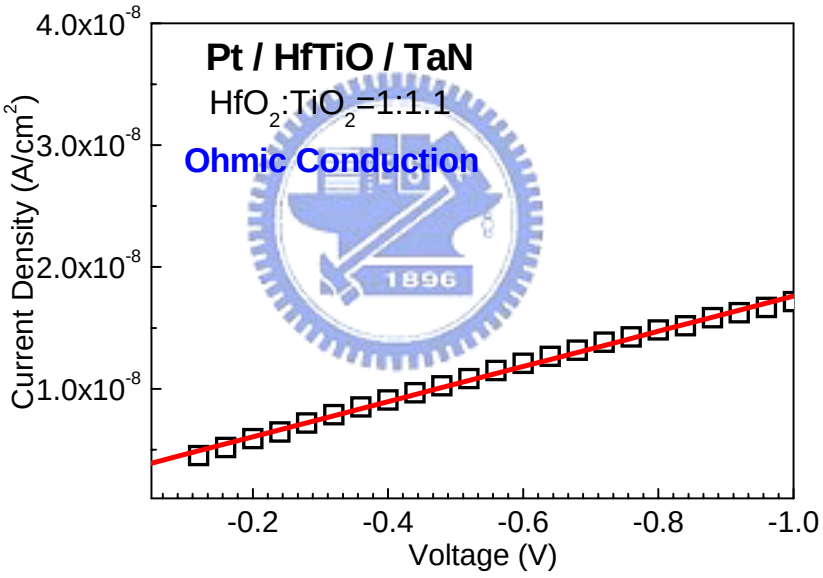

(b)

Fig. 4-3 (a) *J-V* characteristics of HfTiO dielectric for $TiO_2/HfO_2$ ratio of 1.85 and 1.1 at temperature range from 25 to 125°C and (b) the current density at -3 V for $TiO_2/HfO_2$ ratio of 1.85 and 1.1 at temperature range from 25 to 125°C.

(a)

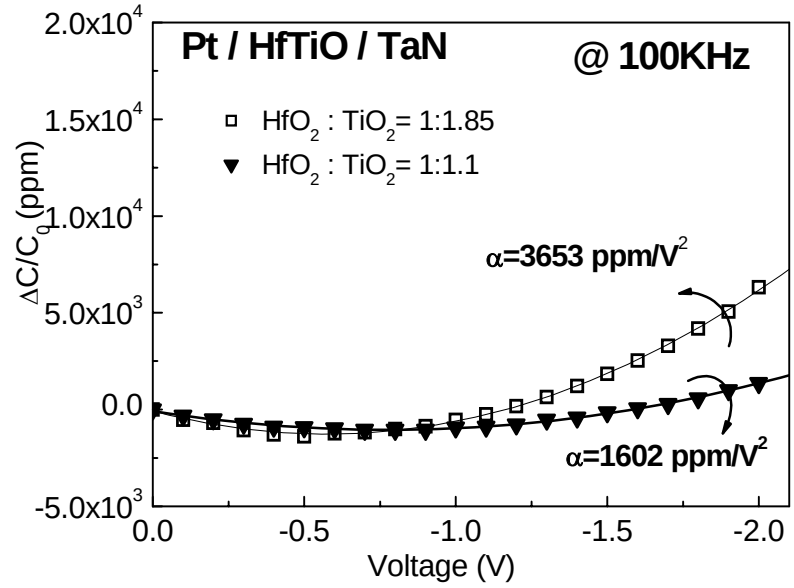



(a)

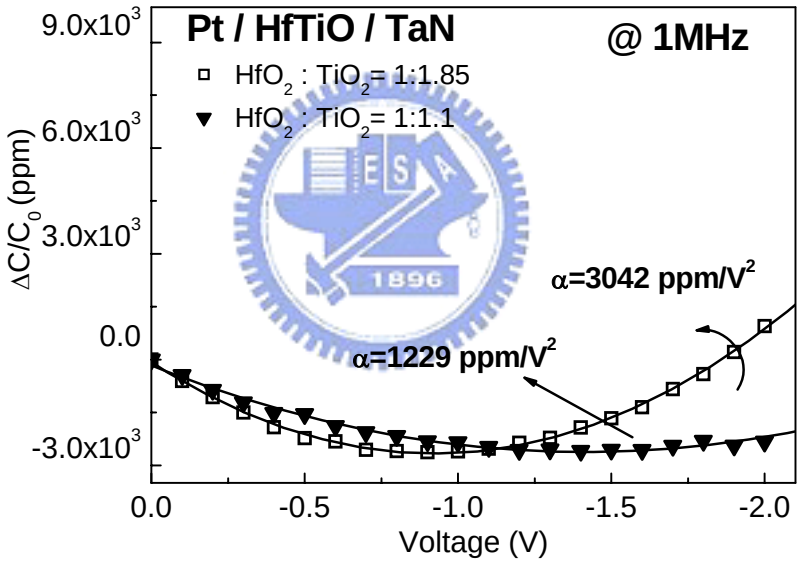



(b)

Fig. 4-4 (a) $\ln(J/T^2)$-$E^{1/2}$ of Pt/HfTiO/TaN MIM capacitors with $HfO_2$:$TiO_2$=1:1.85 and 1:1.1 and (b) Ohmic conduction fitting for the ratio of 1:1.1 at low electric field.

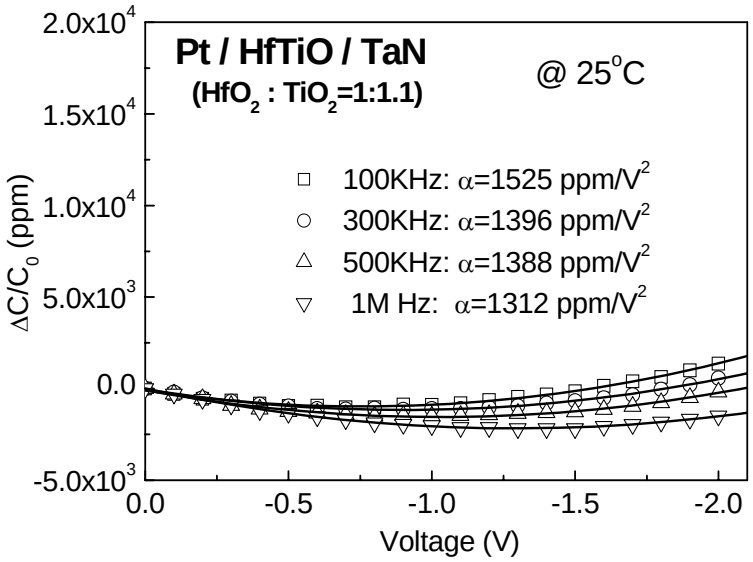



(a)

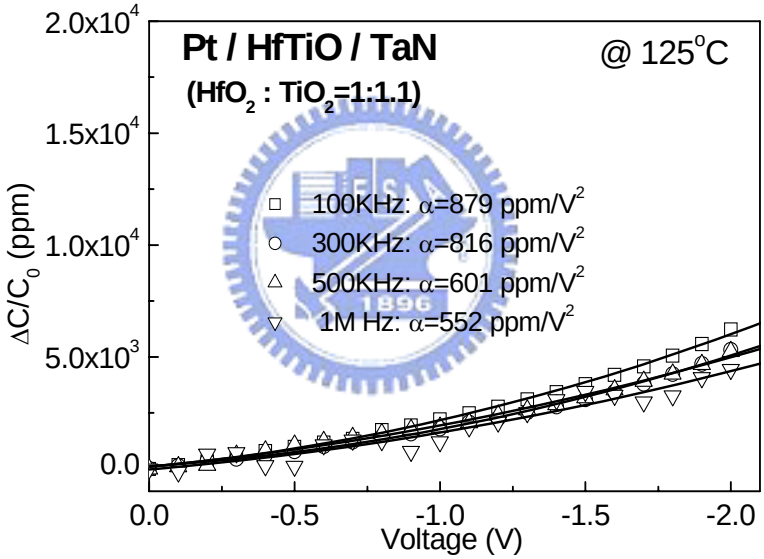



(b)

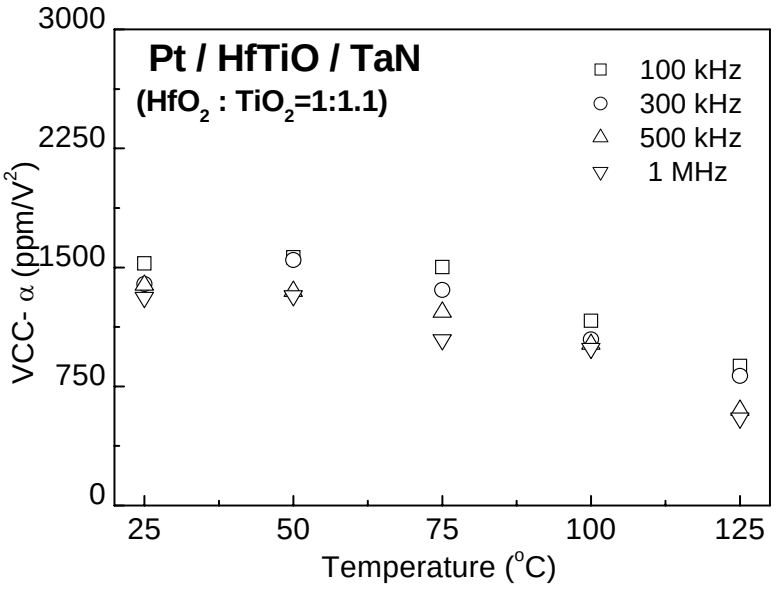
Fig. 4-5 VCC-α characteristics extracted at (a) 100 kHz and (b) 1 MHz for HfTiO MIM capacitor with the $TiO_2/HfO_2$ ratio of 1.85 and 1.1


Pt / HfTiO / TaN
(HfO2 : TiO2=1:1.1)
@ 25°C
100KHz: α=1525 ppm/V2
300KHz: α=1396 ppm/V2
500KHz: α=1388 ppm/V2
1M Hz: α=1312 ppm/V2
ΔC/C0 (ppm)
Voltage (V)
2.0x10^4
1.5x10^4
1.0x10^4
5.0x10^3
0.0
-5.0x10^3
0.0
-0.5
-1.0
-1.5
-2.0

(a)


Pt / HfTiO / TaN
(HfO2 : TiO2=1:1.1)
@ 125°C
100KHz: α=879 ppm/V2
300KHz: α=816 ppm/V2
500KHz: α=601 ppm/V2
1M Hz: α=552 ppm/V2
ΔC/C0 (ppm)
Voltage (V)
2.0x10^4
1.5x10^4
1.0x10^4
5.0x10^3
0.0
0.0
-0.5
-1.0
-1.5
-2.0

(b)




(c)

Fig. 4-6 $\Delta C/C_0$ as the function of voltage for $TiO_2/HfO_2$ ratio of 1.1 and VCC-α extracted at the frequencies of 100, 300, 500 kHz and 1 MHz at (a) 25°C and (b) 125°C and (c) VCC-α as a function of temperature measured at different frequencies for $TiO_2/HfO_2$ ratio of 1.1.

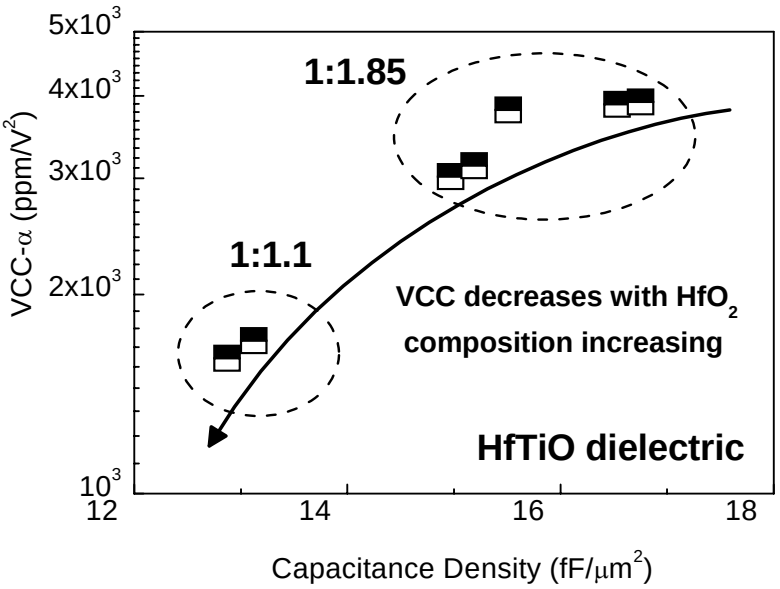
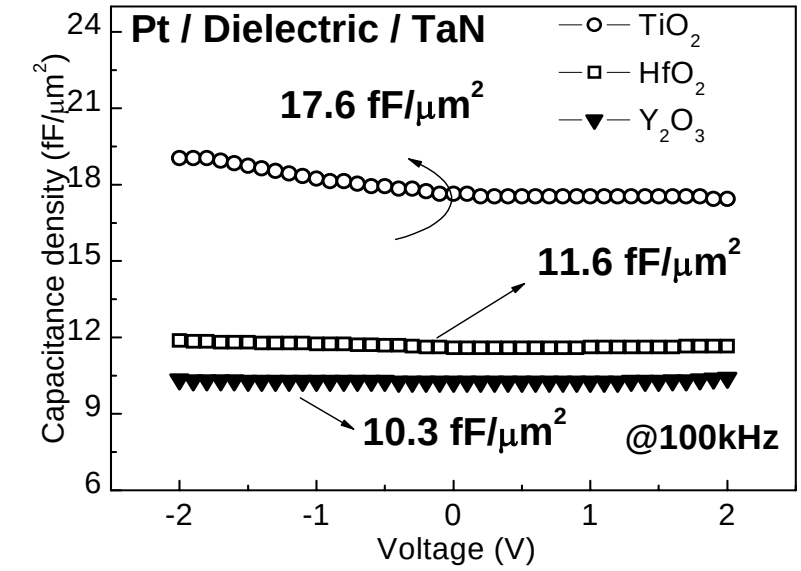
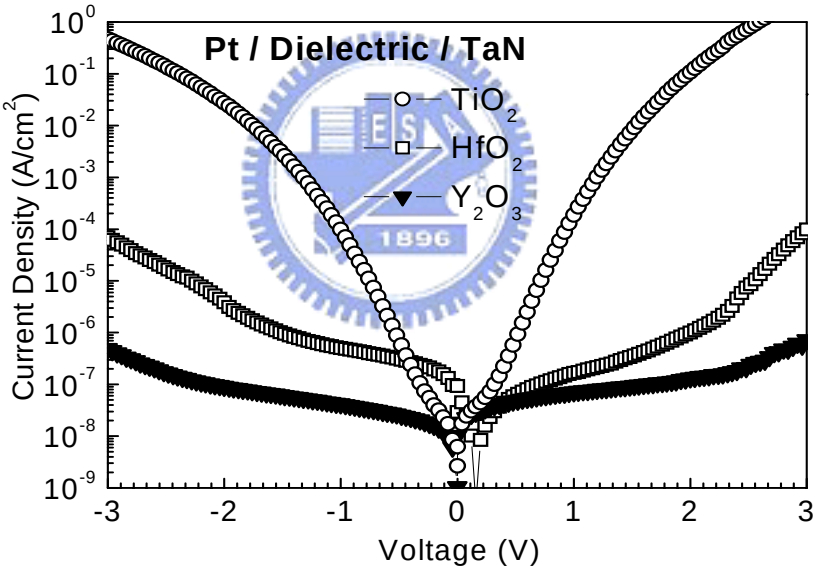



Fig. 4-7 Trends of VCC-α values with respect to capacitance density when the ratio of $HfO_2$ changes from 1.85 to 1.1

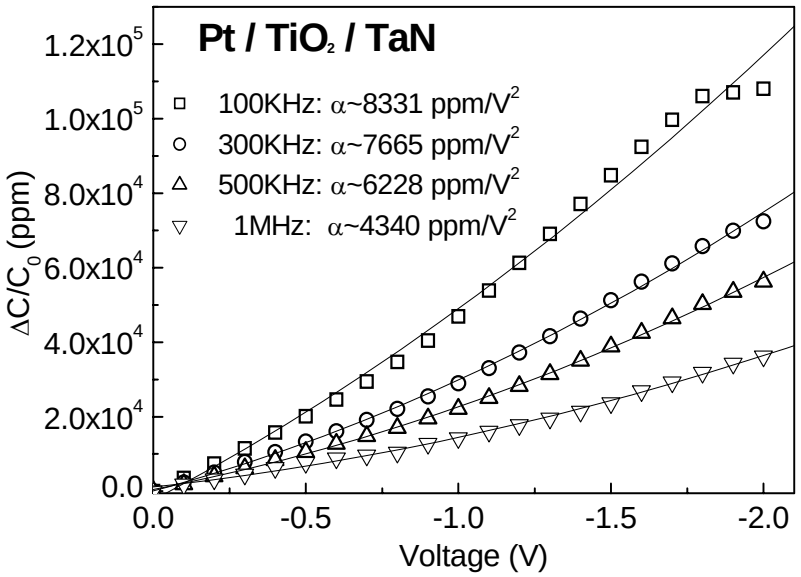



(a)

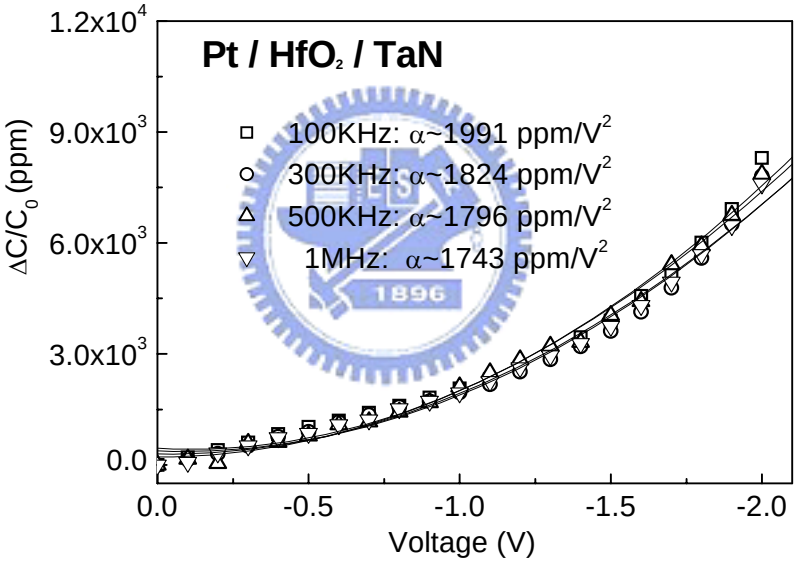



(b)

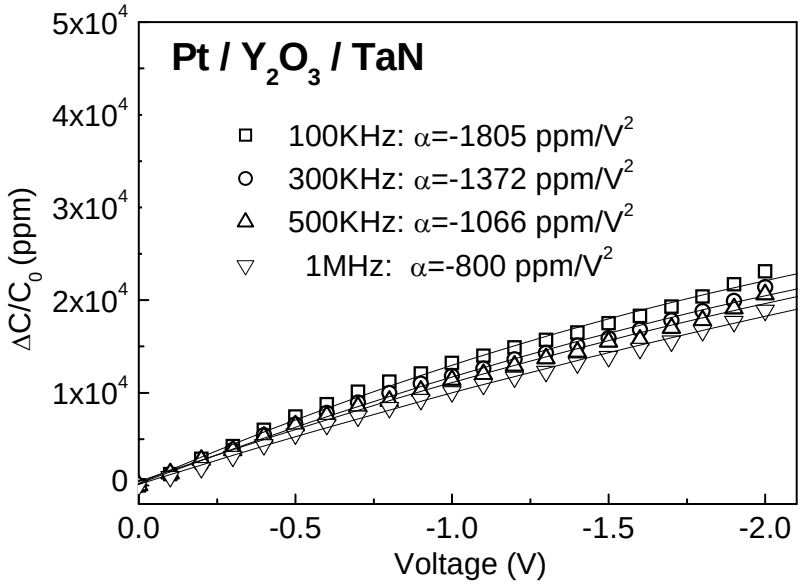
Fig. 4-8 The (a) *C-V* and (b) *J-V* characteristics of $TiO_2$, $HfO_2$ and $Y_2O_3$ MIM capacitors.


Pt / TiO₂ / TaN
100KHz: α~8331 ppm/V²
300KHz: α~7665 ppm/V²
500KHz: α~6228 ppm/V²
1MHz: α~4340 ppm/V²
ΔC/C₀ (ppm)
Voltage (V)
1.2x10⁵
1.0x10⁵
8.0x10⁴
6.0x10⁴
4.0x10⁴
2.0x10⁴
0.0
0.0
-0.5
-1.0
-1.5
-2.0

(a)

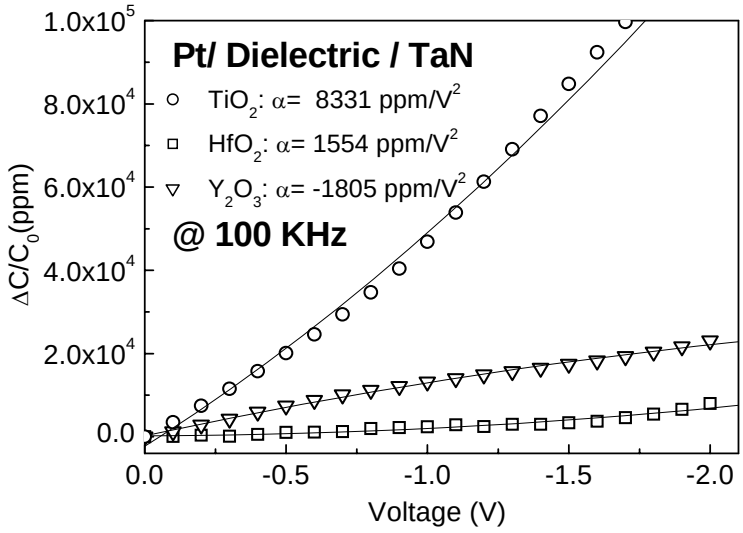

Pt / HfO₂ / TaN
100KHz: α~1991 ppm/V²
300KHz: α~1824 ppm/V²
500KHz: α~1796 ppm/V²
1MHz: α~1743 ppm/V²
ΔC/C₀ (ppm)
Voltage (V)
1.2x10⁴
9.0x10³
6.0x10³
3.0x10³
0.0
0.0
-0.5
-1.0
-1.5
-2.0

(b)

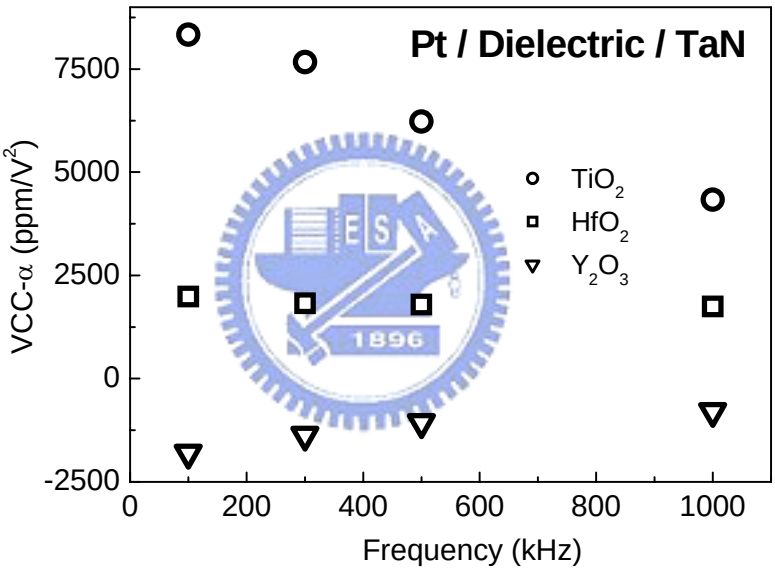



(c)

Fig. 4-9 The VCC-α characteristics of (a) $TiO_2$ (b) $HfO_2$ (c) $Y_2O_3$ MIM capacitors at different frequencies.




(a)




(b)

Fig. 4-10 The (a) VCC-α characteristics at 100 kHz and (b) frequency dependence of VCC-α for $TiO_2$, $HfO_2$ and $Y_2O_3$ MIM capacitors.

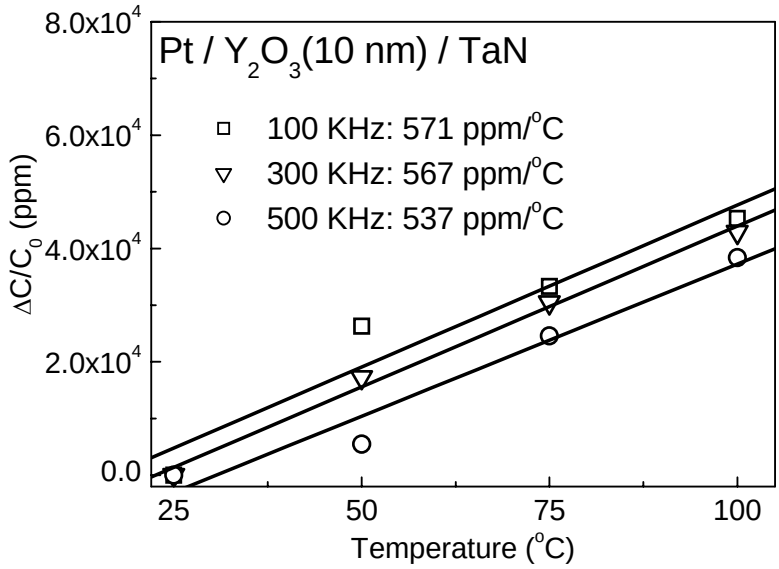



Fig. 4-11 The TCC characteristics of a $Pt/Y_2O_3/TaN$ MIM capacitor at the frequencies of 100 kHz, 300 kHz and 500 kHz.

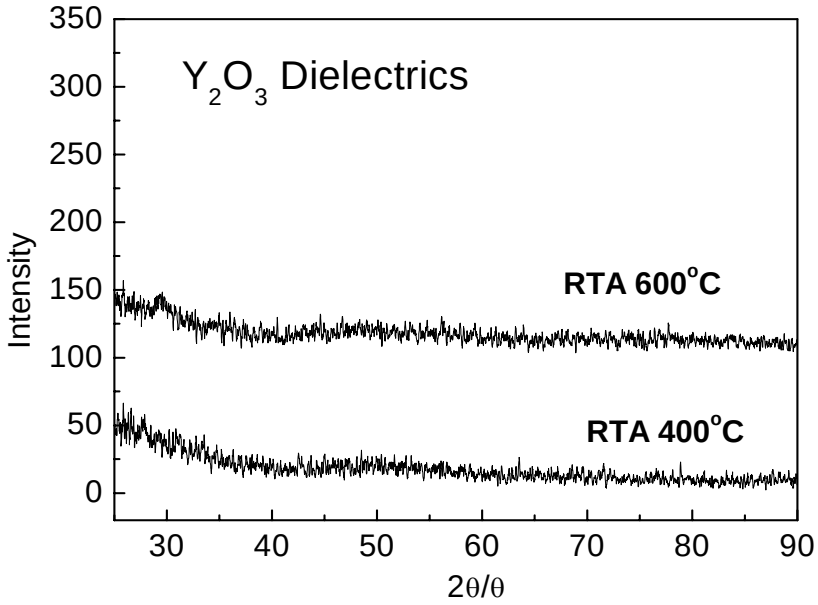
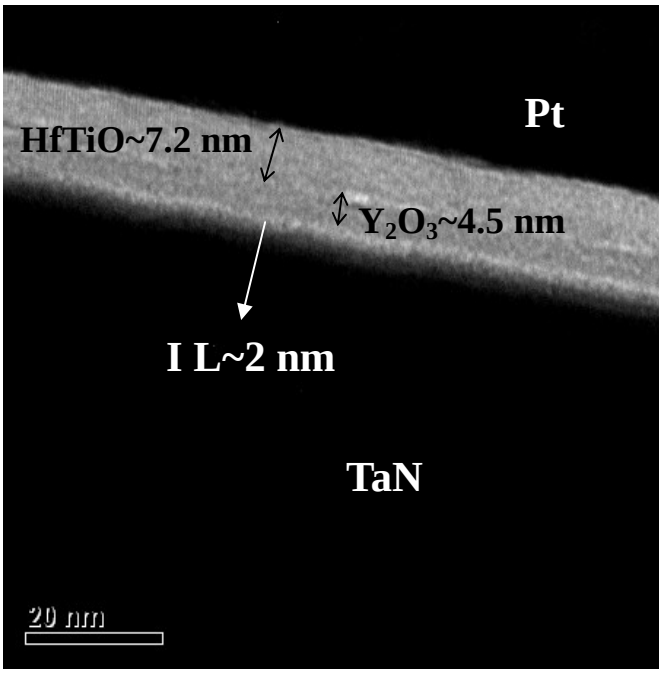
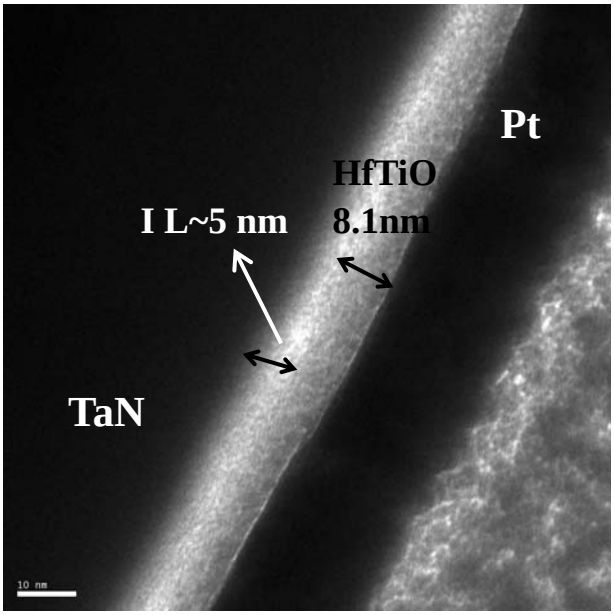



Fig. 4-12 XRD analysis of $Y_2O_3$ dielectric under 400°C and 600°C PDA.

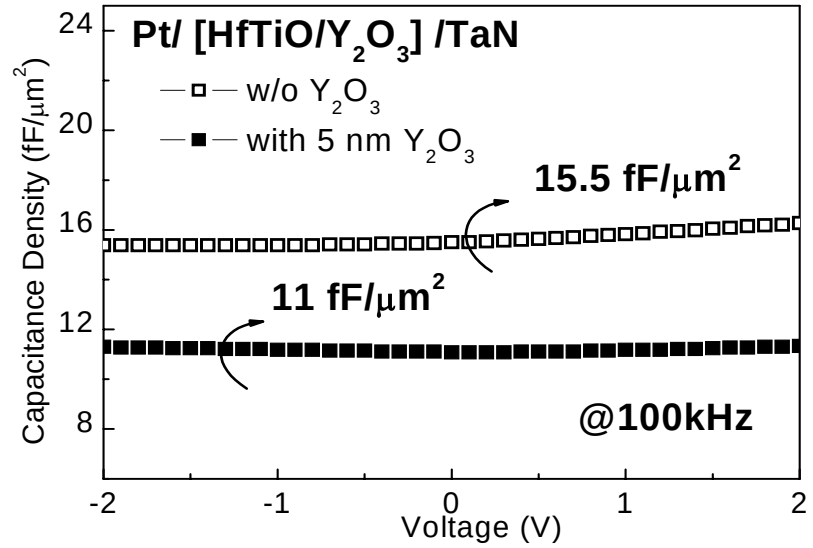



(a)

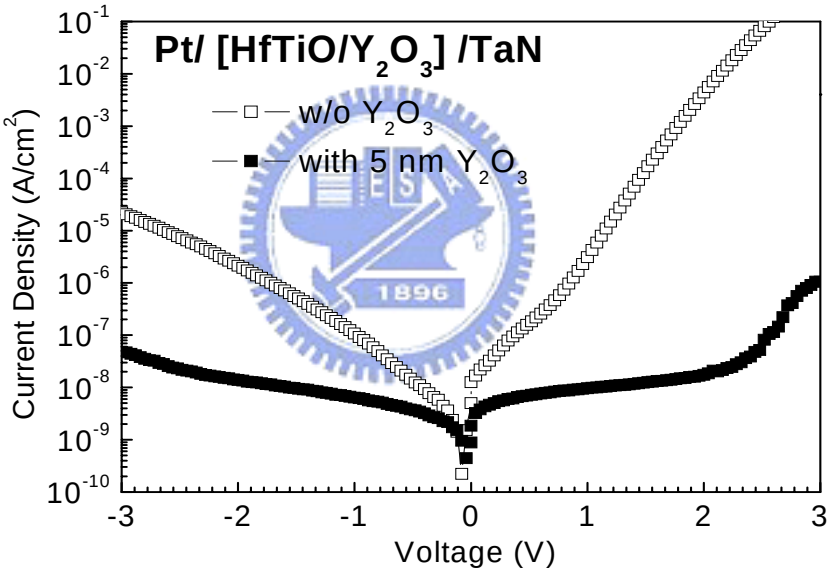



(b)

Fig. 4-13 The TEM images of (a) a HfTiO (~7.2 nm)/$Y_2O_3$ (~4.5 nm) laminated MIM capacitor and (b) a 8.1 nm-thick HfTiO MIM capacitors, respectively

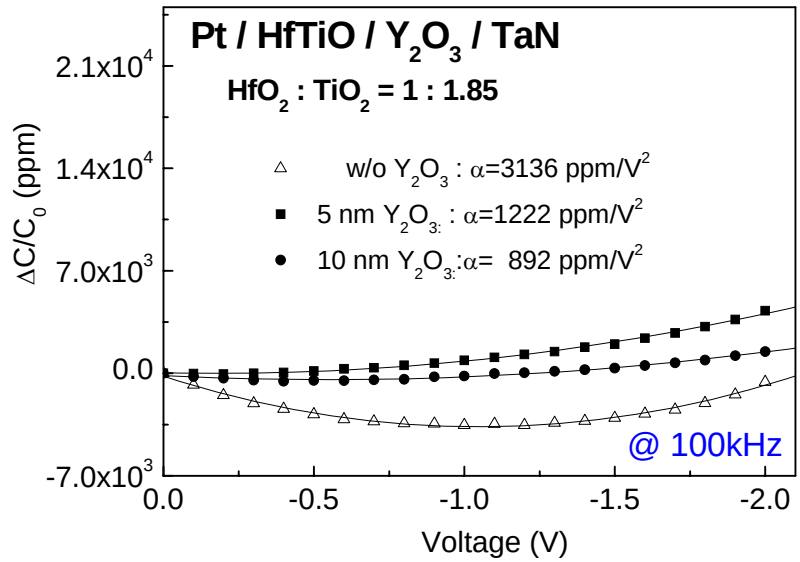



(a)

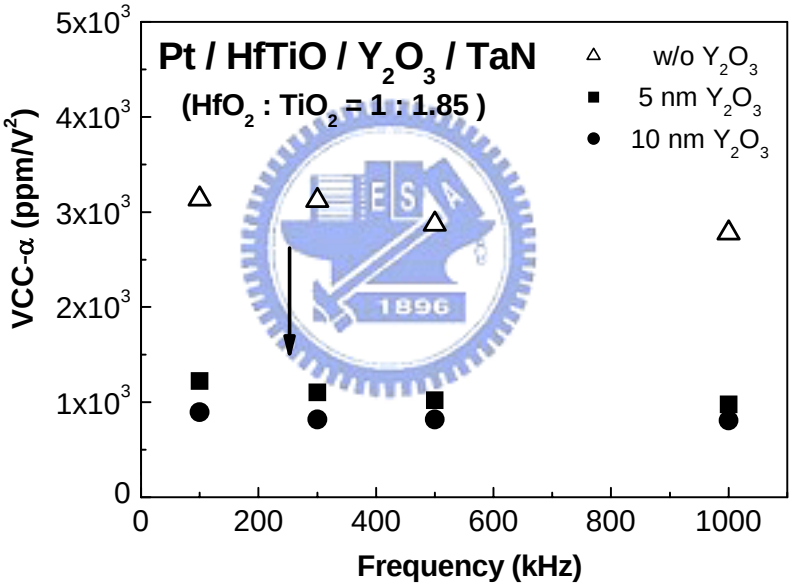



(b)

Fig. 4-14 The *C-V* and *J-V* characteristics of HfTiO MIM capacitors with or without $Y_2O_3$ layer

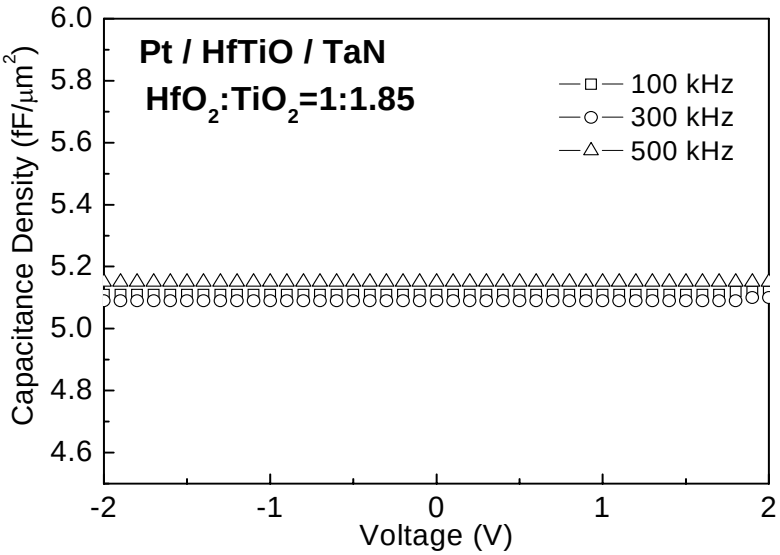



(a)

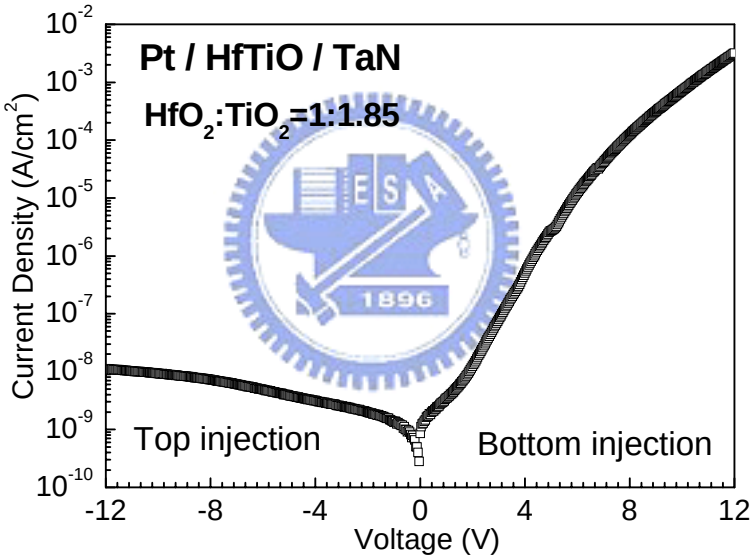



(b)

Fig. 4-15 The (a) VCC characteristics at 100 kHz and (b) frequency depdence of VCC-α for $HfTiO/Y_2O_3$ laminated MIM capacitors




(a)




(b)

Fig. 4-16 (a) *C-V* and (b) *J-V* characteristics of a 51 nm-thick HfTiO MIM capacitor.

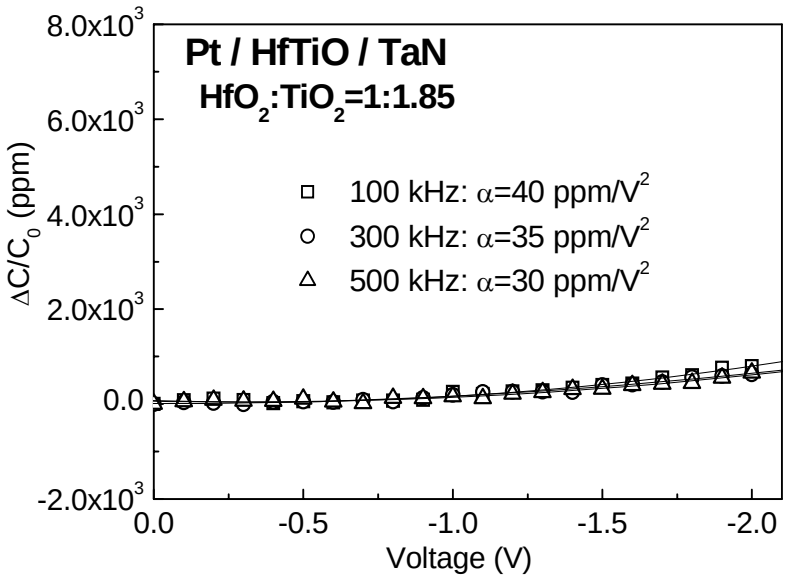



Fig. 4-17 The VCC-α characteristics of Pt/HfTiO/TaN MIM capacitors at the frequencies of 100, 300 and 500 kHz.

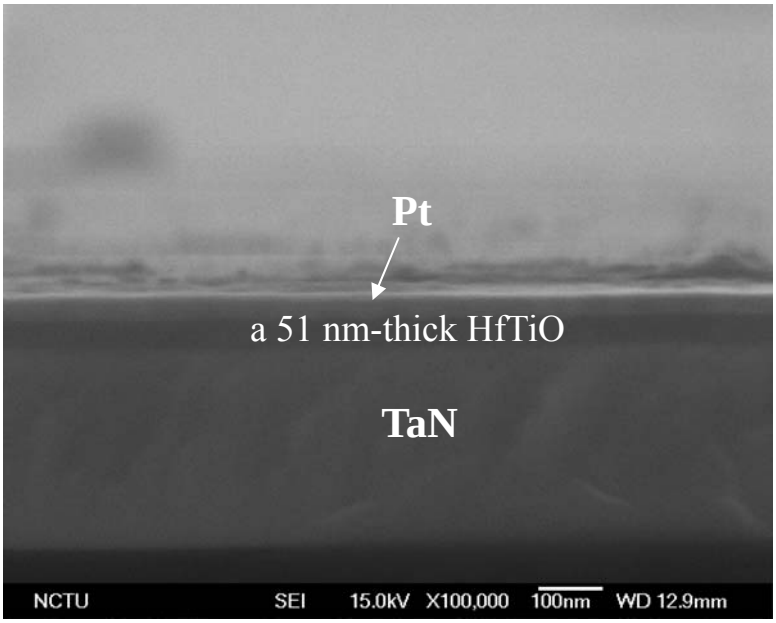



Fig. 4-18 SEM image of a Pt/HfTiO/TaN MIM capacitor with a 51nm-thickness

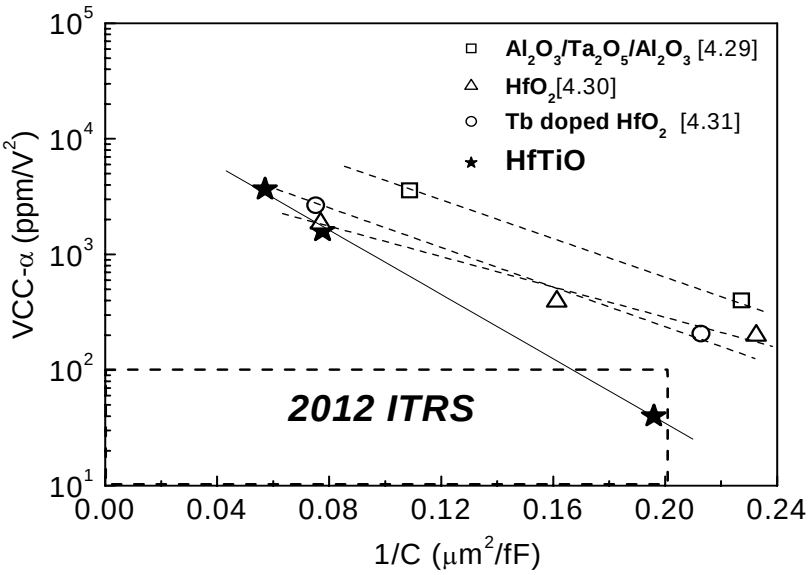



Fig. 4-19 VCC-α verse 1/*C* plot for various high-κ MIM capacitors. The exponential decrease with increasing 1/*C* is important to design capacitors for different applications.

# Chapter 5

# The Observation on Stress Performance of MIM Capacitors under Constant Voltage Stress

## 5.1 Introduction

The metal-insulator-metal (MIM) capacitors as passive components are widely used for precision analog and RF applications. The stability, precision, and endurance properties are important for analog or RF capacitors. For applications requiring extreme precision, such as A/D and D/A converters, only a 0.1% mismatch is allowed [5.1]. However, the capacitance-degradation behavior of a capacitor has not been well characterized [5.2, 5.3]. In this chapter, we investigate the stress behavior on electrical properties and VCC characteristics related to capacitance variation under constant voltage stress test.

## 5.2 The Stress Behavior of Pt/HfTiO/TaN MIM capacitors

Fig. 5-1 shows the leakage current as a function of stress time for the Pt/HfTiO/TaN MIM capacitor under constant voltage stress (CVS) at different negative biases. The peaks of current density are due to the CVS was interrupted every 1000 seconds so that *I-V* characteristic can be monitored every 1000 seconds. Electron trapping phenomenon at smaller stressed-voltage of -3.5 V and hole trapping phenomenon at higher stress-voltage of -4.5 V or -5 V are observed.

Fig. 5-2 (a) and (b) show the *C-V* and *J-V* behavior after CVS at -3.5 V for various stress time. In Fig. 5-2 (a), the capacitance density increases with the increase of stress time since the injected charges pile up in HfTiO films near Pt electrode. The

charges pile-up will cause lower electric field to reduce the leakage current at lower voltage as shown in Fig. 5-2 (b). The electron trapping phenomenon occurred at low field is dominated by Schottky emission, which is electrode limited, and the leakage current will decrease with the space charges increasing near the top electrode. In general, smaller stress bias or shorter stress time is expected to result in an electron trapping phenomenon.

However, an excessive voltage (higher than -4.5 V) could increase the charges-injected energy largely to damage the dielectric and generate hole traps. During CVS, the capacitance density decreases and leakage current increases as shown in Fig. 5-3 (a) and 5-3 (b), respectively. It has been demonstrated that interfacial layer of TaTiO is formed between bottom TaN electrode and HfTiO dielectric during PDA, leading to oxygen deficient dielectric layer. This assumption agrees with the identified presence of oxygen vacancies near MIM electrodes [5.4, 5.5]. J. P. Manceau *et al.* [5.6] proposed that those oxygen vacancies located at the interface between bottom electrode and HfTiO dielectrics move up to top electrode and create a leakage current path during the negative voltage stress. The bulk properties of the HfTiO layer was changed so that the stress induced leakage current (SILC) shown in Fig. 5-3 (b) is observed at the whole voltage range.

The stress-induced behavior on capacitance density and leakage current are summarized in Fig. 5-4 (a) and (b), respectively. It can be observed that the capacitance density increases and leakage current decreases after CVS at low voltage and vice versa at high voltage. At low CVS voltage, electrons were injected into dielectric and some of them were trapped in dielectric. The existing traps were filled by the injected electrons and no new traps were generated because the electron energy was not high enough. Therefore, capacitance density increased because of the new dipole formed due to the piled-up electrons. The coulomb scattering due to the

trapped electron reduced the low field leakage current. Since no new traps were generated, the high field leakage current was not affected. At high CVS voltage, electrons tunneled through the dielectric layer easily so that few electrons were trapped but many new traps were generated in the bulk of dielectric by the high energy electrons. Electrons can tunnel through the dielectric layer via the newly generated traps so that the leakage current increased at both low field and high field. The decrease of capacitance density may be explained by the few trapped electrons.

Fig. 5-5 (a) shows the capacitance variation ($\Delta C/C_0$) measured at an interval of 1000 sec after constant voltage stress at -3V for 1000 sec. Here, $\Delta C$ is defined as the difference of the capacitance at -2 V and 0 V, and $C_0$ is the capacitance at zero bias. The reduction of $\Delta C/C_0$ implies the improvement of VCC performance. It appears that the relative-capacitance variation is a combination of two different effects. In the early stage, it decreases dramatically while starting to stress for a while (the first 1000 sec after the onset of stress test). It is suspected that the existing traps were filled during the stress stage so that these traps did not contribute to capacitance after stress. The reversal phenomenon on capacitance variation observed on post-stress stage because the trapped electrons escaped from the traps slowly and the VCC performance recovered gradually.

Fig. 5-5 (b) shows the capacitance variation during continuous CVS stage. The capacitance variation decreased within 1000 sec independent of the stress voltage due to the trap filling. For a CVS at -5 V, the capacitance variation increased monotonically after CVS for 1000 sec. It is suspected that many new traps were generated during stress so that the VCC performance was degraded. This observation is consistent with that reported in [5.7]. For a CVS at -4.5 V, slight recovery of the capacitance variation can be observed because the trap generation rate at -4.5 V is slower than that at -5 V. The capacitance variation decreased continuously as stressing

at -3.5 V because no new traps were generated while existing traps were filled with the increase of stress time. It is worthy to note that the change of capacitance variation is consistent with the changes of capacitance density and leakage current.

## 5.3 The Stress Behavior of Al/HfTiO/TaN MIM capacitors

The Al metal with a low work function was already fabricated to a MIM capacitor and the performance was presented in Chapter 3. Here, the HfTiO MIM capacitors with Al top electrode was also experienced CVS and then a comparison with Pt/HfTiO/TaN MIM capacitors was made.

In Fig. 5-6, leakage current as a function of stress time for Al/HfTiO/TaN MIM capacitors under CVS at -2.5 V or -3 V is shown. Because the stress voltage is not high enough, electron trapping phenomenon is observed. The noisy current density after stressing for 1000 sec may be due to the complicated electron/hole trapping and detrapping.

The effects of stress on capacitance density and leakage current are shown in Fig. 5-7 (a) and (b), respectively. After CVS, the capacitance density increased at stressed-voltage of -2.5 V and decreased at -3 V with the increase of stress time. This result is similar to that shown in Fig.5-4(a) and can be explained by the same mechanisms, i.e., low level stress increases the capacitance density due to electron pile-up at the electrode/dielectric interface while high level stress decreases capacitance density due to few trapped electrons. In Fig. 5-7 (b), stress induced leakage current can be observed at low field after high level stress (-3 V). The high field leakage current is not affected by the CVS. This is reasonable because the stress voltage is not very high so that only a few traps can be generated. The reason why -3 V can not generate traps for the Pt-top electrode sample but can generate some traps for the Al-top electrode sample may be attributed to the much higher leakage current,

i.e., much higher charge injection level, for the Al sample.

Finally, Fig.5-8 shows that the CVS at both -2.5 V and -3 V decreased the capacitance variation because the trap generation is limited.

In summary, charge trapping and trap generation phenomena were observed on the HfTiO MIM capacitors under CVS stress. Capacitance variation less than 1% can be achieved. The use of Pt electrodes not only reduces the leakage current but also can suppress the stress-induced leakage current and capacitance variation to get a better VCC-$\alpha$ for long-term reliability.

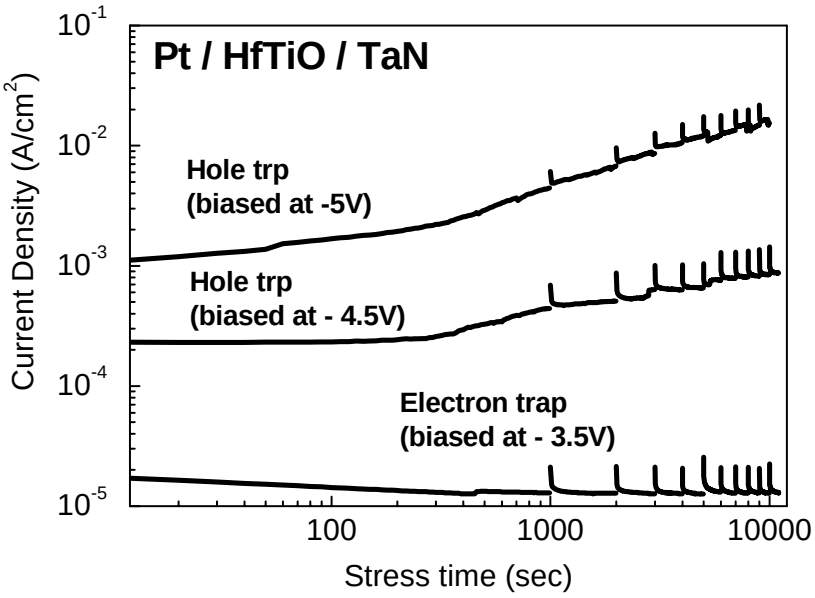
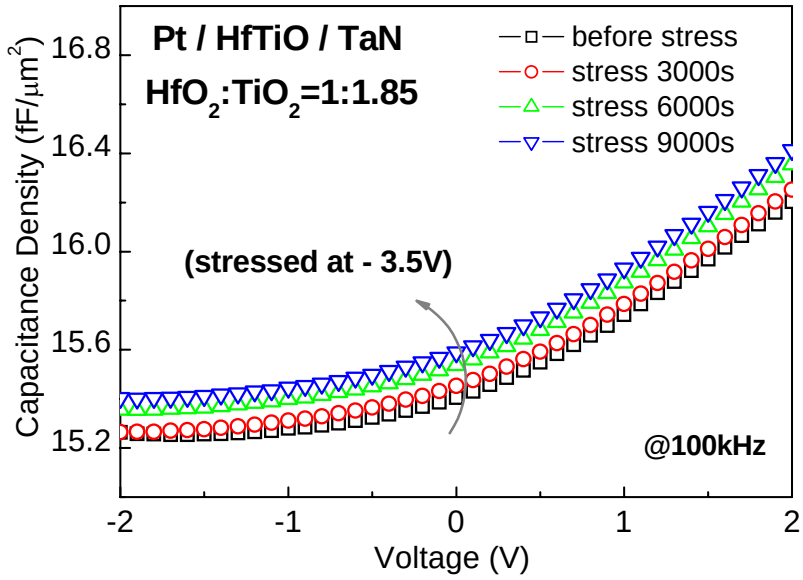
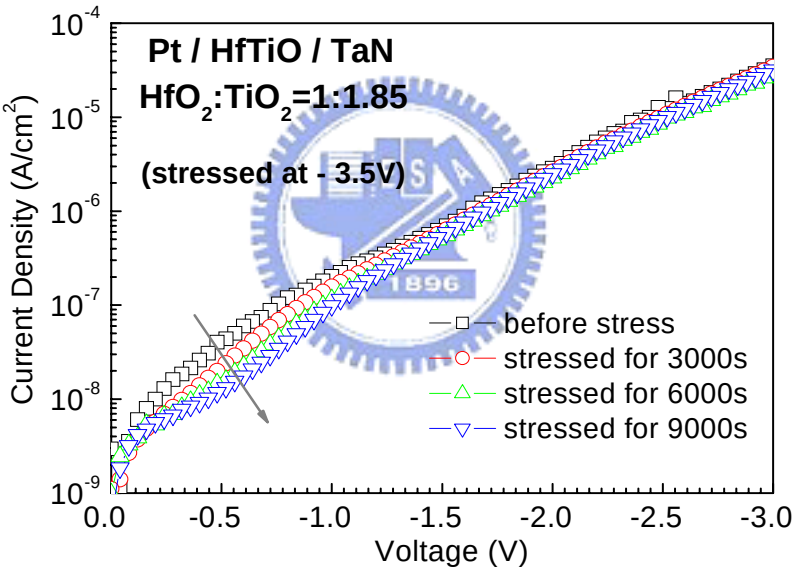



Fig. 5-1 Leakage current-stress time properties of Pt/HfTiO/TaN MIM capacitors under different negative bias by constant voltage stress.

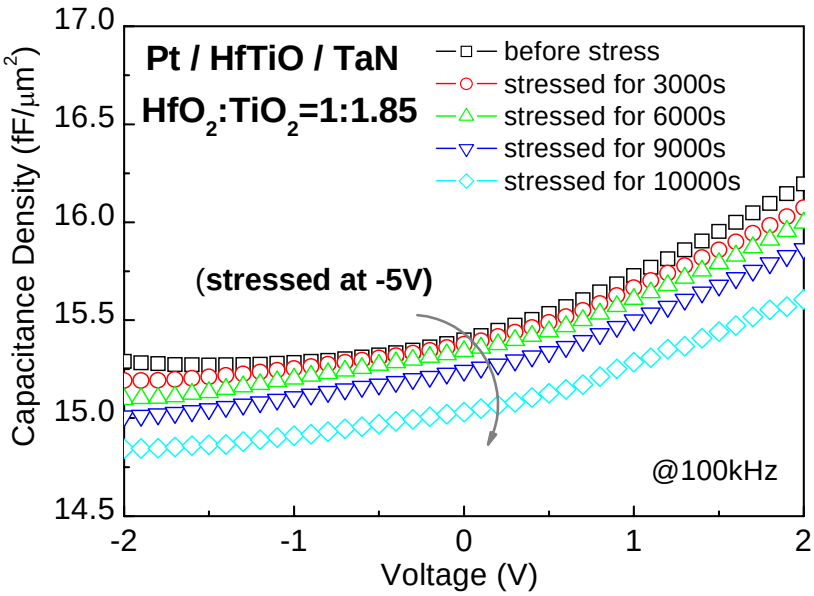



(a)

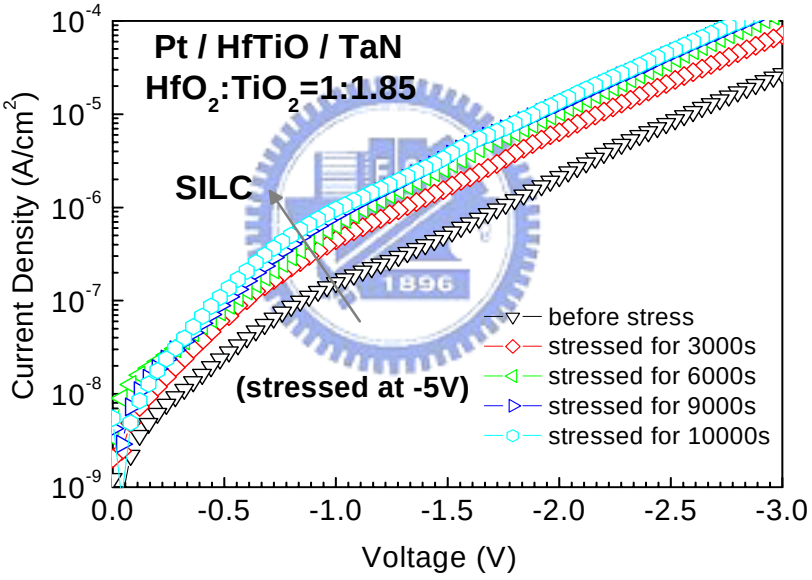



(b)

Fig. 5-2 The effect of constant-voltage stress biased at -3.5 V on (a) *C-V* and (b) *J-V* of Pt/HfTiO/TaN capacitors.

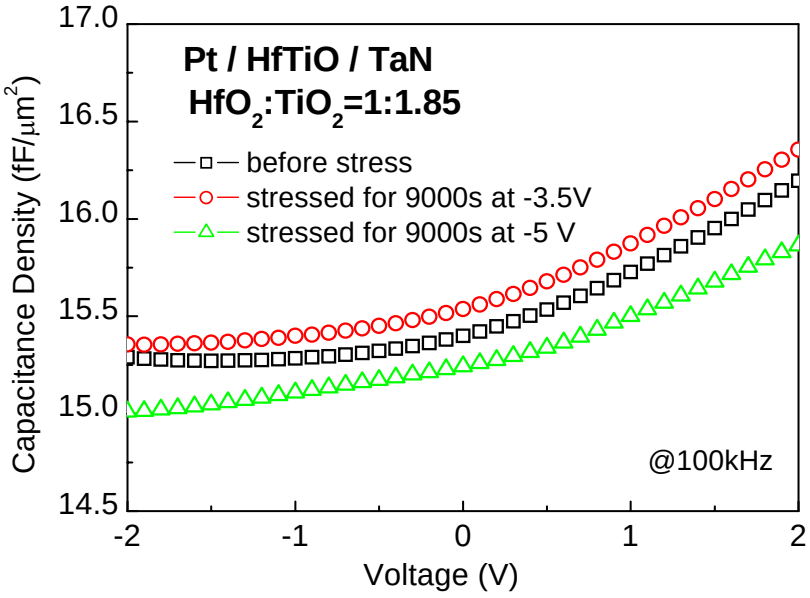



(a)

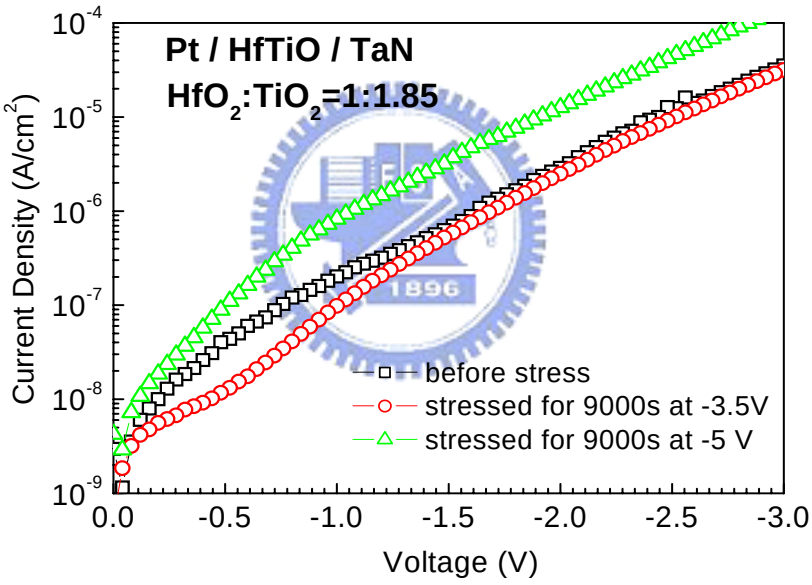



(b)

Fig. 5-3 The effect of constant-voltage stress biased at -5 V on (a) *C-V* and (b) *J-V* of Pt/HfTiO/TaN capacitors.

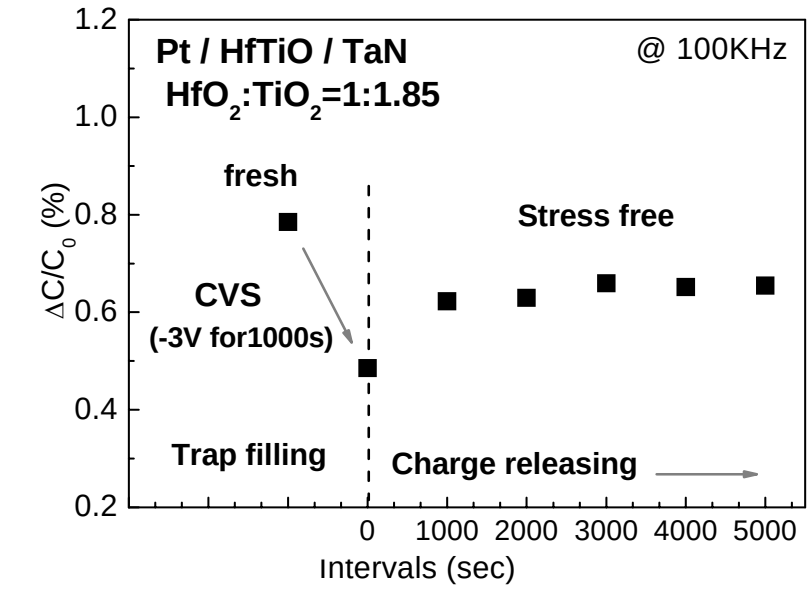



(a)

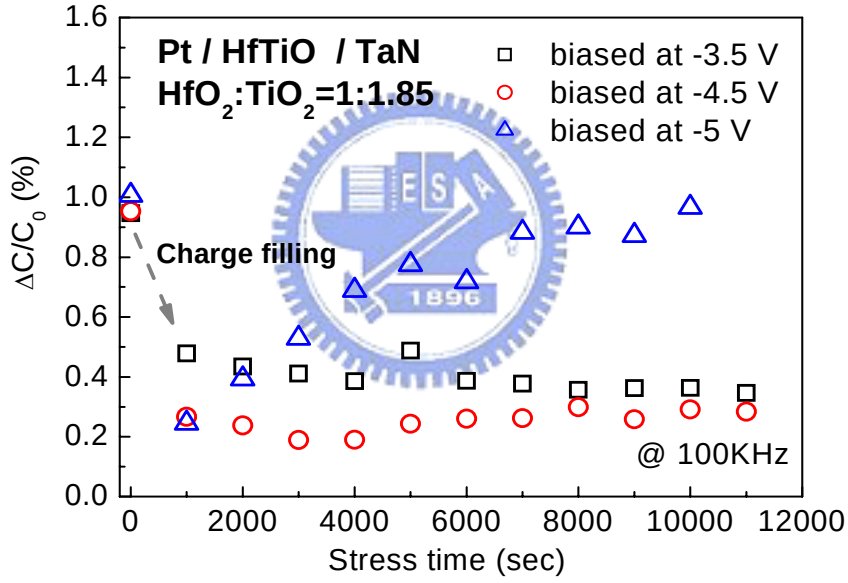



(b)

Fig. 5-4 (a) *C-V* and (b) *J-V* of Pt/HfTiO/TaN capacitors before stress or after different stress condition.




(a)




(b)

Fig. 5-5 Charge-induced capacitance variation (a) measured at regular intervals of 1000 sec after CVS and (b) as a function of stress time at different biased voltage by CVS.

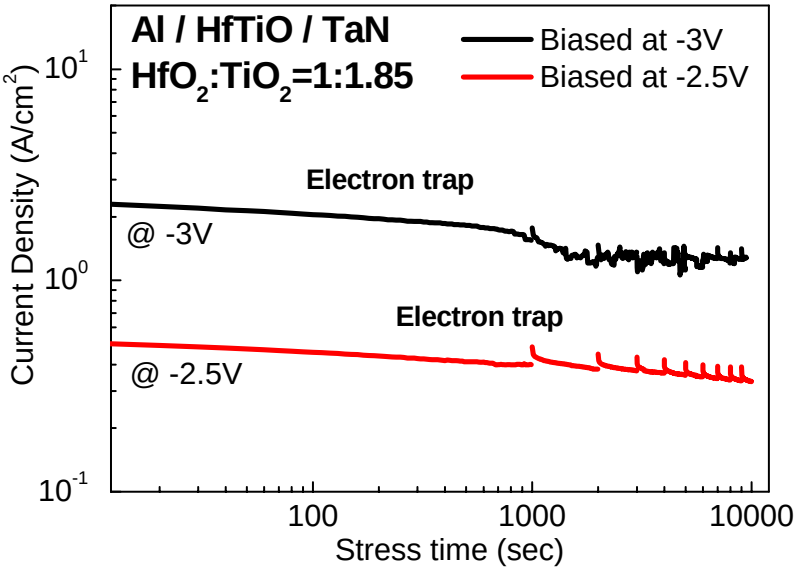
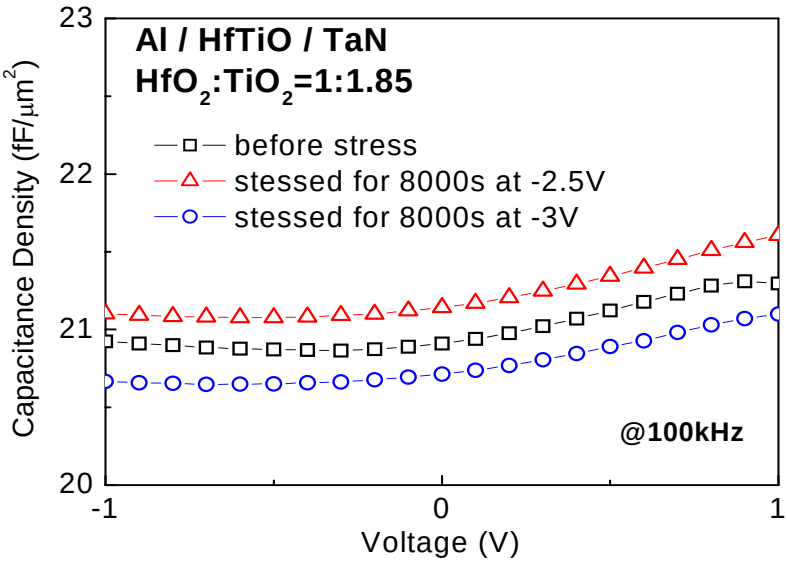
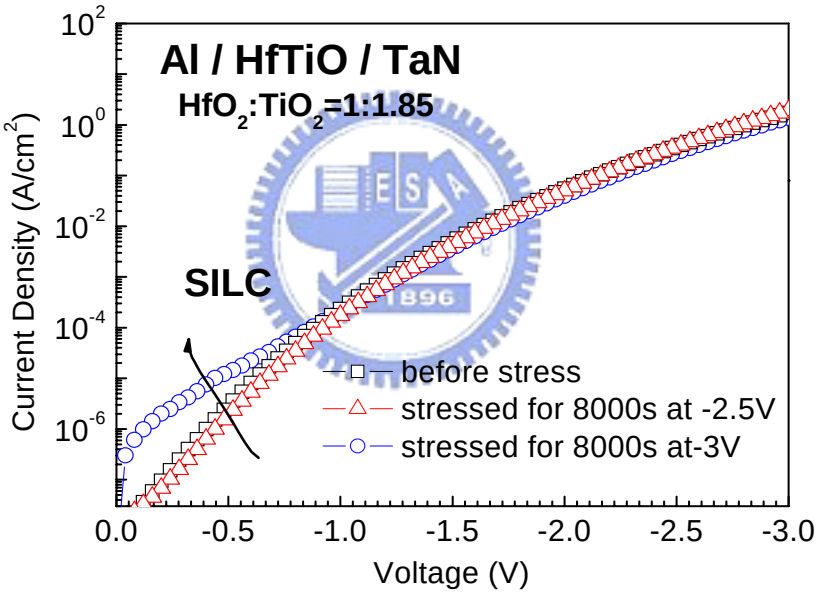



Fig. 5-6 Leakage current-stress time properties of Al/HfTiO/TaN capacitors under CVS biased at -2.5 V and -3 V.




(a)




(b)

Fig. 5-7 The effect of constant-voltage stress biased at -2.5 V and -3 V on (a) *C-V* and (b) *J-V* of Al/HfTiO/TaN capacitors.

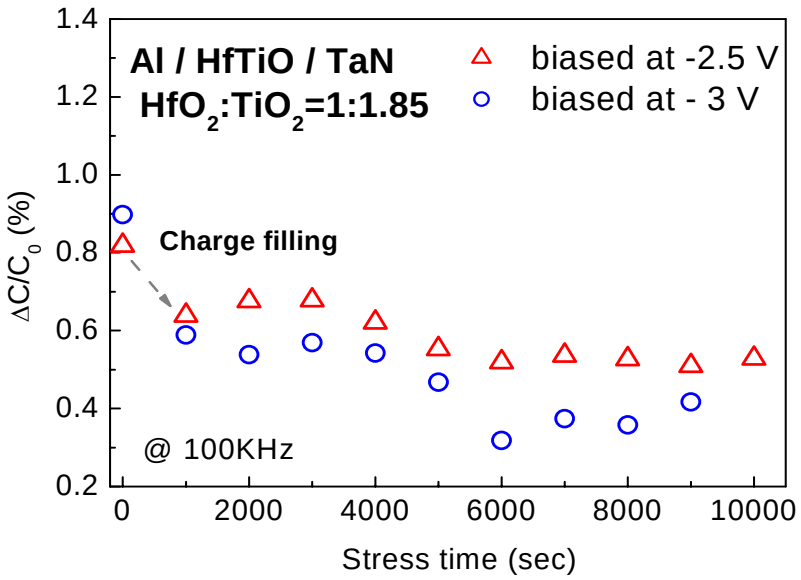



Fig. 5-8 Charge-induced capacitance variation under different biased voltage by CVS for Al/HfTiO/TaN MIM capacitors.

# Chapter 6

# Conclusions

## 6.1 Summary

The pure $TiO_2$ dielectric with a small band gap is easy to crystallize at low temperature post deposition annealing (< 400$^{o}$C) and then suffers from a high leakage current. To overcome the poor electrical properties, a mixed HfTiO dielectric was developed successfully as a high performance MIM capacitor with high work function and thermodynamic stable Pt metal. A high capacitance density of 17.5 fF/$\mu m^2$ and low leakage current of $3.4x10^{-8}$ A/$cm^2$ at -1 V were obtained. The good performance implies the feasibility of HfTiO films as a dielectric for DRAM application. For the leakage issue of MIM capacitors, the bottom interface layer is responsible for high leakage current and voltage nonlinearity, while can be improved by simple $NH_3$ plasma treatment. Besides, it has been demonstrated that using bottom interface treatment to combine with a dielectric-plasma treatment will improve largely the overall leakage current in this study.

The VCC mechanism affected by the thickness effect, work-function of electrodes, film compositions, and laminate dielectric was investigated in this thesis. The results will be beneficial for the improvement on VCC properties for RF/DRAM

applications. Here, it is worth to note that the $Y_2O_3$ material with a negative VCC-$\alpha$ was proposed to be an inserting layer for laminate MIM structure and reduced the value of VCC-$\alpha$ effectively for the first time. The 51 nm-thick HfTiO film had a capacitance density of 5.1 fF/$\mu m^2$ with a low leakage current of $1.3x10^{-9}$ A/$cm^2$ at -1 V and its VCC-$\alpha$ value at 100 kHz is 40 ppm/$V^2$ smaller than the required value ($\alpha$<100 ppm/$V^2$), which meets the ITRS requirement of a RF capacitor in 2012. These results confirm that the HfTiO film can be used as a high performance MIM capacitor and the 400$^o$C temperature of PDA enable them to be integrated into back-end-of-line process.

Finally, respecting the importance of VCC properties for RF capacitors in long-term use, an evaluation on analog characteristics is necessary. We used a constant voltage stress (CVS) on MIM capacitors to study the stress behavior of the lekage current and VCC characteristics. We found that capacitance variation less than 1% can be achieved with the help of Pt electrode. Therefore, the use of Pt electrodes not only reduces the leakage current but also can suppress the stress-induced leakage current and capacitance variation to get a better VCC-$\alpha$ for long-term reliability.

## 6.2 Future Works

For DRAM MIM capacitors, the higher dielectric constant (κ>50) is required while the activation temperature of dielectric is a major concern among the high-κ materials due to the limitation of 400$^{o}$C BEOL process. Crystallized materials may be a choice for obtaining a higher capacitance density, but a large leakage current seems to be unavoidable. By combining with high-work-function metal to suppress an unwanted leakage current is already a trend for the DRAM development beyond 60 nm. Therefore, developing a very high-κ material (ex: crystallized $SrTiO_3$ or $BaSrTiO_3$ dielectrics) match with a high-work-function metal or laminated structure to reduce the leakage current may be a research topic in the future.

For RF capacitors, the analog properties are most important, especially for VCC and TCC. The physical mechanisms of VCC are still unclear and a detail investigation is necessary. In addition, we have to understand that a small VCC-α and capacitance density may be a relationship of trade-off. Therefore, to search high-κ materials with small VCC properties or combine negative VCC material with thicker positive VCC material are both good research directions.

In addition, the effect of Fermi level pinning or interfacial layer on the SBH extraction needs to be further identified.

# References

## Chapter 1


[1.1] "International Technology Roadmap for Semiconductors," ITRS, 2007 edition.

[1.2] Yoshida, M., Kumauchi, T., Kawakita, K., Ohashi, N., Enomoto, H., Umezawa, T., Yamamoto, N., Asano, I. and Tadaki, Y., "Low temperature metal-based cell integration technology for gigabit and embedded DRAMs," *IEEE IEDM Tech. Dig.*, 2007, pp. 41-44.

[1.3] Stein, K., Kocis, J., Hueckel, G., Eld, E., Bartush, T., Groves, R., Greco, N., Harame, D. and Tewksbury, T., "High reliability metal insulator metal capacitors for silicon germanium analog applications," IEEE *Bipolar/BiCMOS Circuits and Technology Meeting*, 1997. pp. 191-194.

[1.4] Yoshitomi, T., Ebuchi, Y., Kimijama, H., Ohguro, T., Morifuji, E., Momose, H.S., Kasai, K., Ishimaru, K., Matsuoka, F., Katsumata, Y., Kinugawa, M., and Iwai, H., "High performance MIM capacitor for RF BiCMOS/CMOS LSIs," *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, pp.133-136, 1999.

[1.5] Arjun Kar-Roy, Chun Hu, Marco Racanelli, Cory A. Compton, Paul Kempf, Gurvinder Jolly, Phil N.Sherman, Jie Zheng, Zhe Zhang and Aiguo Yin, "High density metal insulator metal capacitors using PECVD nitride for mixed signal and RF circuits," *IEEE Interconnect Technology International Conference*, pp. 245-247, 1999.

[1.6] Zurcher, P., Alluri, P., Chu, P., Duvallet, A., Happ, C., Henderson, R., Mendonca, J., Kim, M., Petras, M., Raymond, M., Remmel, T., Roberts, D., Steimle, B., Stipanuk, J., Straub, S., Sparks, T., Tarabbia, M., Thibieroz,

H. and Miller, M., “Integration of thin film MIM capacitors and resistors into copper metallization based RF-CMOS and Bi-CMOS technologies,” *IEEE IEDM Tech. Dig.*, 2000, pp. 153-156.

[1.7] Jeffrey A. Babcock, Scott G. Balster, Angelo Pinto, Christoph Dirnecker, Philipp Steinmann, Reiner Jumpertz, and Badih El-Kareh, “Analog characteristics of metal–insulator–metal capacitors using PECVD nitride dielectrics,” *IEEE Electron Device Lett.*, vol. 22, no. 5, pp. 230-232, May 2001.

[1.8] H.-S. P. Wong, “Beyond the conventional transistor,” *IBM J. Res. Develop.*, vol. 46, no. 2/3, pp. 133-168, 2002.

[1.9] S. J. Kim, B. J. Cho, M. F. Li, C. Zhu, A. Chin, and D. L. Kwong, “$HfO_2$ and lanthanide-doped $HfO_2$ MIM capacitors for RF/mixed IC applications,” *IEEE Symp. VLSI Tech. Dig.*, 2003, pp. 77-78.

[1.10] X. Yu, C. Zhu, H. Hu, A. Chin, M. F. Li, B. J. Cho, D. L. Kwong, P. D. Foo, and M. B. Yu, “A high-density MIM capacitor (13 fF/$\mu m^2$) using ALD $HfO_2$ dielectrics,” *IEEE Electron Device Lett.*, vol. 24, no. 2, pp. 63-65, Feb. 2003.

[1.11] H. Hu, C. Zhu,Y. F. Lu, M. F. Li, B. J. Cho, and W. K. Choi, “A high-performance MIM capacitor using $HfO_2$ dielectrics,” *IEEE Electron Device Lett.*, vol. 23, no. 9, pp. 514-516, Sep. 2002.

[1.12] Y. L. Tu, H. L. Lin, L. L. Chao, D. Wu, C. S. Tsai, C. Wang, C. F. Huang, C. H. Lin, and J. Sun, “Characterization and comparison of high-k metal-insulator-metal (MIM) capacitors in 0.13 μm Cu BEOL for mixed-mode and RF applications,” *IEEE Symp. VLSI Tech. Dig*, 2003, pp. 79–80.

[1.13] H. Hu, C. Zhu, X. Yu, A. Chin, M. F. Li, B. J. Cho, D.-L. Kwong, P. D. Foo,

M. B. Yu, X. Liu, and J. Winkler, “MIM capacitors using atomic-layer-deposited high-κ $(HfO_2)_{1-x}(Al_2O_3)_x$ dielectrics,” *IEEE Electron Device Lett.*, vol. 24, no. 2, pp. 60-62, Feb. 2003.

[1.14] M. Y. Yang, C. H. Huang, A. Chin, C. Zhu, M. F. Li, and D.-L. Kwong, “High-density MIM capacitors using AlTaO dielectrics,” *IEEE Electron Device Lett.*, vol. 24, no. 5, pp. 306-308, May 2003.

[1.15] S. B. Chen, C. H. Lai, A. Chin, J. C. Hsieh, and J. Liu, “High-density MIM capacitors using $Al_2O_3$ and $AlTiO_x$ dielectrics,” *IEEE Electron Device Lett.*, vol. 23, no. 4, pp. 185-187, Apr. 2002.

[1.16] T. Ishikawa, D. Kodama, Y. Matsui, M. Hiratani, T. Furusawa, and D. Hisamoto, “High-capacitance $Cu/Ta_2O_5/Cu$ MIM structure for SoC applications featuring a single-mask add-on process,” *IEEE IEDM Tech. Dig.*, 2002, pp. 940-942.

[1.17] Masahiko Hiratani, Masaru Kadoshima, Tatsumi Hirano, Yasuhiro Shimamoto, Yuichi Matsui, Toshihide Nabatame, Kazuyoshi Torii, Shinichiro Kimura, “Ultra-thin titanium oxide film with a rutile-type structure,” *Applied Surface Science*, vol. 207, no. 1-4, pp. 13-19, 2003.

[1.18] Young H. Lee, Kevin K. Chan, and Michael J. Brady, “Plasma enhanced chemical vapor deposition of $TiO_2$ in microwave-radio frequency hybrid plasma reactor,” *J. Vac. Sci. Technol. A*, vol. 13, no. 3, pp. 596-601, 1995.

[1.19] J. Yan, D. C. Gilmer, S. A. Campbell, W. L. Gladfelter, and P. G. Schmid, “Structural and electrical characterization of $TiO_2$ grown from titanium tetrakis-isopropoxide (TTIP) and $TTIP/H_2O$ ambient,” *J. Vac. Sci. Technol. B*, vol. 14, no. 3, pp. 1706-1711, 1996.

[1.20] H. Tang, K. Prasad, R. Sanjinbs, P. E. Schmid, and F. Levy, “Electrical and optical properties of $Ti0_2$ anatase thin films,” *J. Appl. Phys*. vol. 75, no. 4, pp. 2042-2047, Feb. 1994.

[1.21] P Alexandrov, J Koprinarova and D Todorov, “Dielectric properties of $TiO_2$-films reactively sputtered from Ti in an RF magnetron,” *Solid-State Electron,* vol. 47, no. 11, pp. 1333-1336, 1996.

[1.22] J. Robertson, “Band offsets of wide-band-gap oxides and implications for future electronic devices,” *J. Vac. Sci. Tech. B,* vol. 18, no. 3, pp 1785-1791, May/Jun 2000.

[1.23] R. B. van Dover, “Amorphous lanthanide-doped $TiO_x$ dielectric films,” *Applied Physics Lett.*, vol. 74, no. 20, pp. 3041-3043, 1999.

[1.24] E. S. Ramakrishnan, Kenneth D. Cornell, Gary H. Shapiro and Wei-Yean Howng, “Dielectric properties of radio frequency magnetron sputter deposited zirconium titanate-based thin films,” *J. Electrochem. Soc.*, vol. 145, Issue 1, pp. 358-362, Jan. 1998.

[1.25] R. B. van Dover, L. F. Schneemeyer, and R. M. Fleming, “Deposition of uniform Zr–Sn–Ti–O films by on-axis reactive sputtering ,” *IEEE Electron Device Lett.*, vol. 19, no. 9, pp. 329-331, Sep. 1998.

[1.26] A.Kvist, in: J. Hladik (Ed.), *Physics of Electrolytes*, vol. 1, Academic Press, Inc, 1972, p. 330.

[1.27] Q. Fang, J. -Y. Zhang, Z. M. Wang, J. X. Wu, B. J. O'Sullivan, P. K. Hurley, T. L. Leedham, H. Davies, M. A. Audier, C. Jimenez, J. -P. Senateur and Ian W. Boyd, “Investigation of $TiO_2$-doped $HfO_2$ thin films deposited by photo-CVD,” *Thin Solid Films*, vol. 428, issue 1-2, pp. 263-268, 2003.

[1.28] A. Paskaleva, A. J. Bauer, M. Lemberger and S. Zu¨rcher, “Different current conduction mechanisms through thin high-κ $Hf_xTi_ySi_zO$ films due

to the varying Hf to Ti ratio," *J. Appl. Phys.*, vol. 95, no. 10, pp. 5583-5590, May 2004.

[1.29] Kazutaka Honda, Akira Sakai, Mitsuo Sakashita, Hiroya Ikeda, Shigeaki Zaima1 and Yukio Yasuda, "Pulsed laser deposition and analysis for structural and electrical properties," *J. J. Appl. Phys.*, vol. 43, no. 4A, 2004, pp. 1571-1576.

[1.30] F. Chen , X. Bin , C. Hella , X. Shi , W. L. Gladfelter and S. A. Campbell, "A study of mixtures of $HfO_2$ and $TiO_2$ as high-κ gate dielectrics," *Microelectronic Engineering*, vol. 72, Issues 1-4, Apr. 2004, pp. 263-266.

[1.31] M. Li, Z. Zhang, S. A. Campbell, W. L. Gladfelter, M. P. Agustin, D. O. Klenov, and S. Stemmer, "Electrical and material characterizations of high-permittivity $Hf_xTi_{1-x}O_2$ gate insulators," *J. Appl. Phys.*, vol. 98, issue 5, pp. 054506, 2005.

[1.32] M. Armacost, A. Augustin, P. Felsner, Y. Feng, G. Friese, J. Heidenreich, G.Hueckel, O. Prigge, and K. Stein, "A high reliability metal insulator metal capacitor for 0.18 μm copper technology," *IEEE IEDM Tech. Dig.*, pp. 157-160, 2000.

[1.33] R. B. van Dover, R. M. Fleming, L. F. Schneemejrer, G. B. Alers, and D. J. Werder, "Advanced dielectrics for gate oxide, DRAM and rf capacitors," *IEEE IEDM Tech. Dig.*, pp. 98-823, 1998.

[1.34] Roberto Aparicio and Ali Hajimiri, "Capacity Limits and Matching Properties of Integrated Capacitors," *IEEE Journal of Solid-State Circuit*, vol. 37, no. 3, pp. 384-393, Mar. 2002.

[1.35] C. Durand et al., "Electrical property improvements of yttrium oxide-based metal-insulator-metal capacitors," *J. Vac. Sci. Technol. A*, vol. 24, no. 3, pp.

459-466, May/Jun. 2006.

[1.36] S. Ezhilvalavan, Tseung-Yuen Tseng, “Progress in the developments of (Ba,Sr)$TiO_3$ (BST) thin films for Gigabit era DRAMs,” *Materials Chemistry and Physics*, vol. 65, 2000, pp. 227-248.

[1.37] T. Remmel, R. Ramprasad, and J. Walls, “Leakage behavior and reliability assessment of tantalum oxide dielectric MIM capacitors,” *IEEE Intl. Rel. Phys. Symp.*, 2003, pp. 277-281.

[1.38] R. Moazzami, C. Hu, W.H. Shepherd, “Electrical characteristics of ferroelectric PZT thin films for DRAM applications,” *IEEE Trans. Electron Devices*, vol. 39, issue 9, pp. 2044-2049, 1992.

[1.39] Hieda, K., Eguchi, K., Fukushima, N., Aoyama, T., Natori, K., Kiyotoshi, M., Yamazaki, S., Izuha, M., Niwa, S., Fukuzumi, Y., Ishibashi, Y., Kohyama, Y., Arikado, T. and Okumura, K., “All brovskite Capacitor (APEC) Technology for (Ba, Sr)$Ti0_3$ Capacitor Scaling toward CL10pm Stacked DRAMS,” *IEEE IEDM Tech. Dig.*, pp. 807-810, 1998.

[1.40] Shuichi Komatsu, Kazuhide Abe, “Crystallographic orientation dependence of dielectric constant in epitaxially grown $SrTiO_3$ films,” *Jpn. J. Appl. Phys.*, Vol. 34, pp. 3597-3601, 1995.

[1.41] Cheol Seong Hwang, Soon Oh Park, Hag-Ju Cho, Chang Suk Kang, Ho-Kyu Kang, Sang In Lee, and Moon Yong Lee, “Deposition of extremely thin (Ba,Sr)$TiO_3$ thin films for ultra-large-scale integrated dynamic random access memory application,” *Appl. Phys. Lett.*, vol. 67 , no. 19, pp. 2819-2821, 1995.

[1.42] Itabashi, K., Tsuboi, S., Nakamura, H., Hashimoto, K., Futoh, W., Fukuda, K., Hanyu, I., Asai, S., Chijimatsu, T., Kawamura, E., Yao, T., Takagi, H., Ohta, Y., Karasawa, T., Iio, H., Onods, M., Inoue, F., Nomura, H., Satoh,

Y., Higashimoto, M., Matsumiya, M., Miyabo, T., Ikeda, T., Yamazaki, T., Miyajima, M., Watanabe, K., Kawamura, S. and Taguchi, M., "Fully Planarized Stacked Capacitor Cell with Deep and High Aspect Ratio Contact Hole for Giga-bit DRAM," *IEEE Symp. VLSI Tech. Dig*., 1997, pp. 21-22.

[1.43] Hiratani, M., Hamada, T., Iijima, S., Ohji, Y., Asano, I., Nakanishi, N. and Kimura, S. , "A heteroepitaxial MIM-$Ta_20_5$ capacitor with enhanced dielectric constant for DRAMs of G-bit generation and beyond," *IEEE Symp. VLSI Tech. Dig*., 2001, pp. 21-22.

[1.44] Kinam Kim and Gitae Jeong , "Memory technologies in nano-era: challenges and opportunities," *IEEE Integrated Circuit Design and Technology*, 2005, pp. 63-67.

[1.45] Kinam Kim, Chang-Gyu Hwang and Jong Gil Lee , "DRAM technology perspective for Gigabit era," *IEEE Trans. Electron Devices*, vol. 45, pp.598-608, 1998.

[1.46] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H.-S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies," *IEEE Proc.*, vol. 89, no. 3, pp. 259-288, 2001.

## Chapter 2


[2.1] C. C. Huang, C. H. Cheng, Albert Chin, and C. P. Chou, "Leakage current improvement of Ni/TiNiO/TaN metal-insulator-metal capacitors using optimized $N^+$ plasma treatment and oxygen annealing," *Electrochemical and Solid-State Lett.*, vol. 10, issue 10, pp. H287-H290, 2007.

[2.2] K. C. Chiang, Ching-Chien Huang, G. L. Chen, Wen Jauh Chen, H. L. Kao, Yung-Hsien Wu, and Albert Chin, "High-performance $SrTiO_3$ MIM capacitors for analog applications," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2312-2319, Sep. 2006.

[2.3] K. C. Chiang, C. C. Huang, A. Chin, W. J. Chen, H. L. Kao, M. Hong, and J. Kwo, "High performance micro-crystallized TaN/$SrTiO_3$/TaN capacitors for analog and RF applications," in *IEEE VLSI Symp. Tech. Dig.*, 2006, pp. 126-127.

[2.4] K. C. Chiang, C. H. Cheng, H. C. Pan, C. N. Hsiao, C. P. Chou, A. Chin, and H. L. Hwang, "High temperature leakage improvement in metal–insulator–metal capacitors by work-function tuning," *IEEE Electron Device Lett.*, vol. 28, no. 3, pp. 235-237, Mar. 2007.

[2.5] K. C. Chiang, C. H. Cheng, K. Y. Jhou, H. C. Pan, C. N. Hsiao, C. P. Chou, S. P. McAlister, Albert Chin, and H. L. Hwang, 'Use of a high-work-function Ni electrode to improve the stress reliability of analog $SrTiO_3$ metal–insulator–metal capacitors," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 694-696, Aug. 2007.

## Chapter 3


[3.1] Hang Hu, Chunxiang Zhu, Y. F. Lu, Y. H. Wu, T. Liew, M. F. Li, B. J. Cho, W. K. Choi and N. Yakovlev, "Physical and electrical characterization of $HfO_2$ metal-insulator-metal capacitors for Si analog circuit applications," *J. Appl. Phys.,* vol. 94, no. 1, pp. 551-557, 2003.

[3.2] S. Blonkowski, M. Regache, and A. Halimaoui, "Investigation and modeling of the electrical properties of metal-oxide-metal structure formed from chemical vapor deposited $Ta_2O_5$ films," *J. Appl. Phys.,* vol. 90, no. 3, pp. 1501-1508, 2001.

[3.3] Se Jong Rhee, Chang Seok Kang, Chang Hwan Choi,'Chang Yong Kang, Siddarth Krishnan, Manhong Zhang, Mohammad S. Akbar and Jack C. Lee, "Improved electrical and material characteristics of hafnium titanate multi-metal oxide n-MOSFETs with ultra-thin EOT (~8Å) gate dielectric application," *IEEE, IEDM Tech. Dig. Int*, pp. 837-840, 2004.

[3.4] John Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices," *J. Vac. Sci. Technol. B,* vol. 18, no. 3, May/Jun 2000, pp. 1785-1791.

[3.5] K. C. Chiang, C. C. Huang, H. C. Pan, C. N. Hsiao, J. W. Lin, I. J. Hsieh, C. H. Cheng, C. P. Chou, A. Chin, H. L. Hwang and S. P. McAlister, "Thermal leakage improvement by using a high-work-function Ni electrode in high-κ TiHfO metal–insulator–metal capacitors," *J. Electronchem. Soc.*, vol. 154, no. 3, pp. G54-G57, 2007.

[3.6] Chiang, K.C. , Chin, A., Lai, C.H., Chen, W.J., Cheng, C.R., Hung, B.R. and Liao, C.C., "Very high-κ and density TiTaO MIM capacitors for Analog and RF applications" *IEEE Symp. VLSI Tech. Dig.*, Jun. 2005, pp. 62-63.

[3.7] C. H. Lai, A Chin, H. L. Kao, K. M. Chen, M Hong, J Kwo and C. C. Chi, "Very low voltage $SiO_2$/HfON/HfAlO/TaN memory with fast speed and good retention," *IEEE VLSI Symp. Tech. Dig.*, 2006, pp. 54-55.

[3.8] C. H. Cheng, H. C. Pan, H. J. Yang, C. N. Hsiao, C. P. Chou, S. P. McAlister and Albert Chin, "Improved High-Temperature Leakage in High-Density MIM Capacitors by Using a TiLaO Dielectric and an Ir Electrode," *IEEE Electron Device Lett.*, vol. 28, no. 12, pp. 1095-1097, 2007.

[3.9] Trevor Pi-chun Juan, Si-min Chen, and Joseph Ya-min Lee, "Temperature dependence of the current conduction mechanisms in ferroelectric $Pb(Zr_{0.53},Ti_{0.47})O_3$ thin films," *J. Appl. Phys.*, vol. 95, issue 6, pp. 3120-3125, 2004.

[3.10] C. Chaneliere, J. L. Autran and R. A. B. Devine, "Conduction mechanisms in $Ta_2O_5/SiO_2$ and $Ta_2O_5/Si_3N_4$ stacked structures on Si," *J. Appl. Phys.*, vol. 86, issue 1, pp. 480-486, 1999.

[3.11] Leon I. Maissel and Reinhard Glang, Handbook of thin film technology, McGraw-Hill, Ch. 14, pp. 25.

[3.12] Kunio Okimura, "Low temperature growth of rutile $TiO_2$ films in modified rf magnetron sputtering," *Surface and Coatings Technology*, vol. 135, 2001, pp. 286-290.

[3.13] D. S. Jeong, H. B. Park and C. S. Hwang, "Reasons of obtaining an optical dielectric constant from the Poole-Frenkel conduction behavior of atomic-layer-deposited $HfO_2$ films," *Appl. Phys. Lett.*, vol. 86, pp. 072903, 2005.

[3.14] S. Ezhilvalavan and Tseung-Yuen Tseng, "Conduction mechanisms in amorphous and crystalline $Ta_2O_5$ thin films," *J. Appl. Phys.*, vol. 83, no. 9,

May 1998, pp.4797-4801.

[3.15] C. C. Hobbs, L. R. C. Fonseca, A. Knizhnik, V. Dhandapani, S. B. Samavedam, W. J. Taylor, J. M. Grant, L. G. Dip, D. H. Triyoso, R. I. Hegde, D. C. Gilmer, R. Garcia, D. Roan, M. L.Lovejoy, R. S. Rai, E. A. Hebert, Hsing-Huang Tseng, S. G. H. Anderson, B. E. White, P. J. Tobin, "Fermi-level pinning at the polysilicon/metal-oxide interface-Part II," *IEEE Trans. Electron Devices,* vol. 51, pp. 978-984, June 2004.

[3.16] C. C. Hobbs, L. R. C. Fonseca, A. Knizhnik, V. Dhandapani, S. B. Samavedam, W. J. Taylor, J. M. Grant, L. G. Dip, D. H. Triyoso, R. I. Hegde, D. C. Gilmer, R. Garcia, D. Roan, M. L.Lovejoy, R. S. Rai, E. A. Hebert, Hsing-Huang Tseng, S. G. H. Anderson, B. E. White, P. J. Tobin, "Fermi-level pinning at the polysilicon/metal-oxide interface-Part I," *IEEE Trans. Electron Devices,* vol. 51, pp. 971- 977, June 2004.

[3.17] Y. C. Yeo, Pushkar Ranade, Ronald Lin, Tsu-Jae King, and Chenming Hu, "Effects of high-k gate dielectrics material on Metal and Silicon Gate Workfunctions" *IEEE Electron Device Lett.*, vol. 23, no. 6, pp. 342-344, 2002.

[3.18] H. Y. Yu, C. Ren, Y. C. Yeo, J. F. Kang, X. P. Wang, H. H. H. Ma, M. F. Li, D. S. H. Chan, D. L. Kwong, "Fermi pinning-induced thermal instability of metal-gate work functions," *IEEE Electron Device Lett.*, vol. 25, no. 5, pp. 337-339, May 2004.

[3.19] T. H. Perng, C. H. Chien, C. W. Chen, P Lehnen, C. Y. Chang, "High-density MIM capacitors with $HfO_2$ dielectrics ," *Thin Solid Films*, vol. 469-470, pp. 345-349, 2004.

[3.20] Chun-Chen Yeh, T. P. Ma and Kyu Min, "Frenkel-Poole trap energy extraction of atomic layer deposited $Al_2O_3$ and $Hf_xAl_yO$ thin films," *Appl.*

*Phys. Lett.*, vol. 91, pp. 113521, 2007.

[3.21] Babcock, J.A., Balster, S.G., Pinto, A., Dirnecker, C., Steinmann, P., Jumpertz, R. and El-Kareh, B., "Analog characteristics of metal–insulator -metal capacitors using PECVD nitride dielectrics," *IEEE Electron Device Lett.*, vol. 22, no. 5, pp. 230-232, 2001.

[3.22] International Technology Roadmap for Semiconductors, 2007 Edition, Process Integration, Devices, & Structure.

[3.23] N. Umezawa, K. Shiraishi, T. Ohno, H. Watanabe, T. Chikyow, K. Torii, K. Yamabe, K. Yamada, H. Kitajima and T. Arikado, "First-principles studies of the intrinsic effect of nitrogen atoms on reduction in gate leakage current through Hf-based high-k dielectrics," *J. Appl. Phys.*, vol. 86, pp. 143507, 2005.

[3.24] Jeong Y. K., Won S. J., Kwon D. J., Song M. W., Kim W. H., Park M. H., Jeong J. H., Oh H. S., Kang H. K. and Suh K. P., "High quality High-κ MIM capacitor by $Ta_2O_5/HfO_2/Ta_2O_5$ Mulity-layered Dielectric and $NH_3$ plasma interface treatment for mixed-signal/RF application," *IEEE Sympo. Tech. Dig.*, pp. 222-223, 2004.

[3.25] N. J. Seong, S. G. Yoon, S. J. Yeom, H. K. Woo, D. S. Kil, J. S. Roh and H. C. Sohn, "Effect of nitrogen incorporation on improvement of leakage properties in high-κ $HfO_2$ capacitors treated by $N_2$-plasma," *Appl. Phys. Lett.*, vol. 87, pp. 132903, 2005.

## Chapter 4


[4.1] International Technology Roadmap for Semiconductors, 2007 Edition, Process Integration, Devices, & Structure.

[4.2] J. A. Babcock, S. G. Balster, A. Pinto, C. Dirnecker, P. Steinmann, R. Jumpertz, and B. El-Kareh, "Analog characteristics of metal-insulator-metal capacitors using PECVD nitride dielectrics," *IEEE Electron Device Lett.*, vol. 22, no. 5, pp. 230-232, 2001.

[4.3] H. Hu, C. Zhu, Y. F. Lu, M. F. Li, B. J. Cho and W. K. Choi, " A high performance MIM capacitor using $HfO_2$ dielectrics," *IEEE Electron Device Lett.*, vol. 23, no. 9, pp. 514-516, 2002.

[4.4] H. Hu, C. Zhu, Y. F. Lu, Y. H. Wu, T. Liew, M. F. Li, B. J. Cho, W. K. Choi, and N. Yakovlev, "Physical and electrical characterization of $HfO_2$ metal–insulator–metal capacitors for Si analog circuit applications," *J. Appl. Phys.*, vol. 94, no. 1, pp. 551-557 , 2003.

[4.5] Stéphane Bécu, and Sébastien Crémer, "Microscopic model for dielectric constant in metal-insulator-metal capacitors with high-permittivity metallic oxides," *Appl. Phys. Lett.*, vol. 88, pp. 052902, 2006.

[4.6] X. Yu, C. Zhu, H. Hu, Chin, A., Li M.F., B. J. Cho, D. L. Kwong, P. D. Foo and M. B. Yu, "A high-density MIM capacitor (13 fF/$\mu m^2$) using ALD $HfO_2$ dielectrics," *IEEE Electron Device Lett.*, vol. 24, no. 2, Feb. 2003, pp.63-65.

[4.7] Arjun Kar-Roy, Chun Hu, Marco Racanelli, Cory A. Compton, Paul Kempf, Gurvinder Jolly, Phil N.Sherman, Jie Zheng, Zhe Zhang and Aiguo Yin, "High density metal insulator metal capacitors using PECVD nitride for mixed signal and RF circuits," *IEEE Int. Interconnect Technology, Conf.*, 1999, pp. 245-247.

[4.8] Chunxiang Zhu, Hang Hu, Xiongfei Yu, Kim, S. J., Chin, A., Li, M. F., Byung Jin Cho, Kwong, D. L., "Voltage and temperature dependence of capacitance of high-κ $HfO_2$ MIM capacitors: a unified understanding and prediction," *IEEE, IEDM Tech. Dig. Int.*, 2003, pp. 879-882.

[4.9] Sun Jung Kim, Byung Jin Cho, Ming-Fu Li, Shi-Jin Ding, Chunxiang Zhu, Ming Bin Yu, Babu Narayanan, Albert Chin, and Dim-Lee Kwong, "Improvement of voltage linearity in High-κ MIM capacitors using $HfO_2$–$SiO_2$ stacked Dielectric," *IEEE Electron Device Lett.*, vol. 25, no. 8, Aug. 2004, pp. 538-540.

[4.10] S. Blonkowski, M. Regache, and A. Halimaoui, "Investigation and modeling of the electrical properties of metal–oxide–metal structures formed from chemical vapor deposited $Ta_2O_5$ films," *J. Appl. Phys.*, vol. 90, pp. 1501-1508, 2001.

[4.11] P. Gonon and C. Vallée, "Modeling of nonlinearities in the capacitance-voltage characteristics of high-κ metal-insulator-metal capacitors," *Appl. Phys. Lett.*, vol.90, pp. 142906, 2007.

[4.12] A. K. Jonscher, Dielectric Relaxation in Solids (Chelsea Dielectrics, London, 1983), Chap. 5, pp. 247-251; A. K. Jonscher, J. Phys. D 32, R57 ,1999.

[4.13] J. R. Macdonald, "Theory of ac space-charge polarization effects in photoconductors, semiconductors, and electrolytes," *Phys. Rev.*, vol. 92, pp. 4-17, 1953.

[4.14] J. H. Beaumont and P. W. M. Jacobs, "Polarization in potassium chloride crystals," *J. Phys. Chem. Solids*, vol. 28, issue 4, pp. 657-667, 1967.

[4.15] S. P. Mitoff and R. J. Charles, "Electrode polarization of ionic conductors," *J. Appl. Phys.*, vol. 43, pp. 927-934, 1972.

[4.16] S. Bécu, S. Crémer, and J.-L. Autran, "Microscopic model for dielectric constant in metal-insulator-metal capacitors with high-permittivity metallic oxides," Appl. Phys. Lett., vol. 88, pp. 052902, 2006.

[4.17] F. El Kamel, P. Gonon and C. Vallée, "Experimental evidence for the role of electrodes and oxygen vacancies in voltage nonlinearities observed in high-κ metal-insulator-metal capacitors," *Appl. Phys. Lett.*, vol. 91, pp. 172909, 2007.

[4.18] Jeong Y. K., Won S. J., Kwon D. J., Song M. W., Kim W. H., Park M. H., Jeong J. H., Oh H. S., Kang H. K. and Suh K. P., "High quality High-κ MIM capacitor by $Ta_2O_5/HfO_2/Ta_2O_5$ Mulity-layered Dielectric and $NH_3$ plasma interface treatment for mixed-signal/RF application," in *Symp. on VLSI Tech. Dig.*, pp. 222-223, 2004.

[4.19] J. Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices," *J. Vac. Sci. Tech. B*, vol. 18, no. 3, pp 1785-1791, May 2000.

[4.20] K. C. Chiang, C. C. Huang, Albert Chin, W. J. Chen, H. L. Kao, M. Hong, and J. Kwo, "High performance micro-crystallized TaN/SrTiO3/TaN capacitors for analog and RF applications," *in Symp. on VLSI Tech. Dig.*, 2006, pp. 126-127.

[4.21] B. Gross, "Dose rate dependence of carrier mobility," *Solid State Communication,* vol. 15, pp. 1655-1657, 1974.

[4.22] C. Durand, C. Vallee, V. Loup, and O. Salicio, C. Dubourdieu, S. Blonkowski, M. Bonvalot , P. Holliger, and O. Joubert , "Metal-insulator-metal capacitors using $Y_2O_3$ dielectric grown by pulsed-injection plasma enhanced metalorganic chemical vapor deposition," *J. Vac. Sci. Technol. A,*

vol. 22, issue 3, pp. 655-660, 2004.

[4.23] S. Jeannot, A. Bajolet, J. P. Manceau, S. Cremer, E. Deloffre, J. P. Oddou, C. Perrot, D. Benoit, C. Richard, P. Bouillon, and S. Bruyere, "Toward next high performance MIM generation: up to 30 fF/$\mu m^2$ with 3D architecture and high-κ materials," in *IEDM Tech. Dig.*, pp. 997-1000, 2007.

[4.24] H. S. P. Wong, "Beyond the conventional transistor," *IBM J. Res. Develop.*, vol. 46, no. 2/3, pp. 133-168, 2002.

[4.25] C. Zhu, H. Hu, X. Yu, A. Chin, M. F. Li, B. J. Cho and D. L. Kwong, "Voltage and temperature dependences of capacitance of high-κ $HfO_2$ MIM capacitors: a unified understanding and prediction," in *IEDM Tech. Dig.*, 2003, pp. 879-882.

[4.26] S. J. Ding, H. Hu, C. Zhu, S. J. King, X. Yu, M. F. Li, B. J. Cho, Daniel S. H. Chan, M. B. Yu, S. C. Rustagi, A. Chin and D. L. Kwong, " RF, DC and reliability characteristics of ALD HfO2-Al2O3 Laminate MIM capacitors for Si RF IC applications," *IEEE Trans. Electron Devices,* vol. 51, no. 6, pp. 886-894, June 2004.

[4.27] C. Durand, C.Vallee, C. Dubourdieu, M. Kahn, M. Derivaz, S. Blonkowski, D. Jalabert, P. Hollinger, Q. Fang and I. W. Boyd, "Electrical property improvements of yttrium oxide-based metal-insulator-metal capacitors," *J. Vac. Sci. Technol. A.*, vol. 24, no. 3, pp. 459-466, 2004.

[4.28] R. B. Van Dover, R. M. Fleming, L. F. Schneemeyer, G. B. Alers and D. J. Werder, "Advanced dielectrics for gate oxide, DRAM and rf capacitors," in *Proc. of IEDM*, pp. 823-826, 1998.

[4.29] International Technology Roadmap for Semiconductors, 2007 Edition, Radio Frequency and Analog/Mixed-signal Technologies for Wireless Communications.

[4.30] T. Ishikawa, D. Kodama, Y. Matsui, M. Hiratani, T. Furusawa, and D. Hisamoto, "High-capacitance Cu/$Ta_2O_5$/Cu MIM structure for SoC applications featuring a single-mask add-on process," in *IEDM Tech. Dig.*, 2002, pp. 940–942.

[4.31] H. Hu, S. J. Ding, H. F. Lim, C. Zhu, M. F. Li, S. J. Kim, X. F. Yu, J. H. Chen, Y. F. Yong, B. J. Cho, D. S. H. Chan, S. C. Rustagi, M. B. Yu, C. H. Tung, A. Du, D. My, P. D. Fu, A. Chin, and D. L. Kwong, "High performance $HfO_2$−$Al_2O_3$ laminate MIM capacitors by ALD for RF and mixed signal IC applications," in *IEDM Tech. Dig.*, 2003, pp. 879-882.

[4.32] S. J. Kim, B. J. Cho, M.-F. Li, C. Zhu, A. Chin, and D. L. Kwong, "$HfO_2$ and lanthanide-doped $HfO_2$ MIM capacitors for RF/mixed IC applications," in *Symp. on VLSI Tech. Dig.*, 2003, pp. 77-78.

[4.33] K. C. Chiang, Albert Chin, C. H. Lai, W. J. Chen, C. F. Cheng, B. F. Hung and C. C. Liao, "Very high-κ and high density TiTaO MIM capacitors for analog and RF applications," in *Symp. on VLSI Tech. Dig.*, 2005, pp. 62-63.

## Chapter 5


[5.1] A Hastings, *The Art of Analog Layout*. Englewood Cliffs, NJ:Prentice-Hall, 2001, Ch.7, pp.249-257.

[5.2] C. Besset, S. Bruyere, S. Blonkowski, S. Cremer, and E. Vincent, "MIM capacitance variation under electrical stress," *Microelectron. Reliab.*, vol. 43, no. 8, pp. 1237-1240, Aug. 2003.

[5.3] Yamada, T. Moriwaki, M. Harada, Y. Fujii, S. Eriguchi, K., "The metal gate MOS reliability with improved sputtering process forgate electrode," *IEEE, IEDM Tech. Dig. Int.*, 1999, pp. 319-322.

[5.4] W. S. Lau, T. S. Tan, and Premila Babu, "Mechanism of leakage current reduction of tantalum oxide capacitors by titanium doping," *Appl. Phys. Lett.*, vol. 90, pp. 112903, 2007.

[5.5] J. P. Chang, M. L. Steigerwald, R. M. Fleming, R. L. Opila, and G. B. Alers, "Thermal stability of $Ta_2O_5$ in metal-oxide-metal capacitor structures," *Appl. Phys. Lett.*, vol. 74, no. 24, pp. 3705-3707, 1999.

[5.6] J.-P. Manceau, S. Bruyere, S. Jeannot, A. Sylvestre, and P. Gonon, "Metal-insulator-metal capacitor's current instability improvement using dielectric stacks to prevent oxygen vacancies formation," *Appl. Phys. Lett.*, vol. 91, pp. 132907, 2007.

[5.7] Chi-Chao Hung, Anthony S. Oates, Horng-Chih Lin, Yu-En Percy Chang, Jia-Lian Wang, Cheng-Chung Huang and You-Wen Yau, "An innovative Understanding of Metal-Insulator-Metal (MIM)-Capacitor Degradation Under Constant-Current Stress," *IEEE Trans. Electron Devices*, vol. 7, no. 3, pp. 462-467, Sep. 2007.

# 個人簡歷 (Vita)

姓名：徐曉萱

性別：女

生日：73 年 7 月 23 日

籍貫：台灣省新竹縣

住址：台北市松山路 204 巷 9 號 15 樓

學歷：國立交通大學材料科學與工程學系

（91 年 9 月~ 95 年 6 月）

國立交通大學電子研究所碩士班

（95 年 9 月~ 97 年 7 月）

碩士論文題目：

**金屬-氧化鈦鉿-金屬電容於動態記憶體與射頻電路之應用**

**Metal-HfTiO-Metal Capacitors for DRAM/RF Applications**