# 國立交通大學

## 電子工程學系 電子研究所碩士班

## 碩士論文

# 複晶矽雙閘極薄膜電晶體特性及電性擾動分析

# A Study of Characteristics and Variability of Double-Gated Poly-Si Thin-Film Transistors

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中 華 民 國 九 十 七 年 七 月

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## 摘　要

在本篇論文中，我們製作了複晶矽雙閘極的平面結構電晶體並探討其特性。實驗發現縮小通道層的厚度，得到較好的閘極耦合效應，從而改善了次臨界擺幅(subthreshold swing)和得到較高的開關電流比 (on/off current ratio)。另外，由於閘極的耦合效應，只要在控制閘極施加適當的固定偏壓，便可彈性地調整臨界電壓(threshold voltage)的大小。本論文也針對體反轉(volume inversion)的現象進行探索與分析。

除此之外，在本論文裡，我們也探討了一種複晶矽雙閘極奈米線電晶體的基本電性擾動分析。從我們實驗數據顯示，元件量測所得之臨界電壓的標準差與閘極寬度、長度乘積開根號($\sqrt{WL}$)成一個倒數的關係，與前人的模擬結果有同樣的趨向，我們也推測與複晶矽奈米線通道中的缺陷密度有一密切的關聯性。電漿處理可以有效的修補通道裡的缺陷，使元件之間的臨界電壓差異性降低。此外，在不同的操作模式下，以雙閘極操作模式，可得到最小的臨界電壓標準差。另外，我們的實驗數據也首次證實：當控制閘極的固定偏壓存在著一個最佳值，能有效地壓抑臨界電壓的差異性。

# A Study of Characteristics and Variability of Double-Gated Poly-Si Thin-Film Transistors

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## ABSTRACT

In this thesis, planar DG-TFTs were fabricated and characterized. With thin poly-Si body (30nm), gate-to-gate coupling effect in DG mode is more prominent, resulting in better gate controllability, higher ON-current and steeper sub-threshold swing (SS), compared with the single-gated mode. And, there is a significant enhancement in drain current under DG mode due to the volume inversion. In addition, threshold voltage can be modulated over a wide range by $V_{TH}$-control gate (back gate). Compared with symmetric gate oxide, subthreshold swing can be slightly improved by using thicker $V_{th}$-control gate oxide to gain higher $I_{on}/I_{off}$ ratio.

In this study, we also explore the threshold voltage variation in nanowire DG-TFTs. It is confirmed that threshold voltage fluctuation is inversely proportional

to channel length and width. $NH_3$-plasma treatment can effectively suppress threshold voltage fluctuation owing to the passivation of the trap states. It is also found that there is an optimum back gate bias for suppressing the short channel effect which may lead to a larger threshold voltage variation.

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陳玲　誌於風城

2008 年 7 月

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# *CHAPTER 1*

# Introduction

## 1-1 Double-gated Poly-Si Thin Film Transistors

Under the Moore's Law, the number of transistors on a chip will double every 18 months, which means the feature size of the devices will be scaled by 0.7X in each generation. With downscaling of MOSFETs, short channel effects (SCEs), namely, threshold voltage roll-off and subthreshold slope degradation, become a serious issue. Thus, how to increase gate controllability has been a major topic in the development of advanced device technology.

Transistors with innovative structure need to be explored and developed in order to suppress the above-mentioned problems and sustain high-performance and low-power application. In the past twenty years, there are lots of researches on novel structures, such as DELTA structure in 1989 [1], gate-all-around (GAA) structure [2] in 1990 and FinFET structure [3] in 1998. The main purpose of these structures is to increase the gate controllability.

In the past ten years, many researches focus on double-gated (DG) SOI devices due to their good gate controllability. Compared with single-gated device, DG-SOI can effectively suppress the penetration of electric field from the drain side into the

channel, thus SCEs can be suppressed [4-12]. On the other hand, DG structure has a higher drain current because of its wider conduction channel area. Also, a better subthrehold slope can be achieved due to strong gate controllability on channel potential. All are helpful to extend the scaling limit.

For ultra-thin body (UTB) DG-SOI, volume inversion can be obtained when the channel body is sufficiently thin [10-11]. If the channel body is thicker than the maximum depletion width, the wave function of electrons in one channel is unlikely to overlap with that in the other channel, thus coupling effect between two channels is negligible. However, if the channel body is thinner than the maximum depletion width of a planar device, the potential of the two channels will be coupled together, especially at a low-gate voltage condition. It redistributes the inversion electrons and peaks the distribution at the center of the channel film, rather than close to the interface between gate oxide and the channel. Such phenomenon is known as "volume-inversion" [13-14]. When this happens, a substantial enhancement in both carrier concentration and mobility and, consequently, an increased drive current can be achieved.

The conventional means for threshold voltage ($V_{TH}$) adjustment is done through varying the channel doping or the gate work-function. However, using channel doping might lead to a larger $V_{TH}$-fluctuation and mobility degradation. In recent years,

DG-SOI has been reported to modulate $V_{TH}$ by multiple independent gates. In the scheme, at least one of the gates fixed with a specific voltage is employed to modulate and control the threshold voltage of the device [15-20]. In this method, it has been demonstrated that a wide range of $V_{TH}$ adjustment could be achieved which can be beneficial for optimization of circuit's power and speed performance.

## 1-2 Threshold Voltage Fluctuation

Accompanied with aggressively scaling of MOSFETs is the reduction of the operation voltage to ensure good device reliability. This would lead to some side effects, however. For example, the noise margin of circuits such as SRAM becomes smaller. As a result, devices are more sensitive to the fluctuation of device characteristics, especially for the threshold voltage [21-22]. This fluctuation is an intrinsic barrier to further downscaling. The causes come from two main factors. One is process variations such as line-edge roughness (LER) related to lithographic and etching steps [23], and film thickness variation from deposition [24-25]. Other is the intrinsic variation like channel dopant fluctuation [26-27]. Both factors need to be taken into consideration in the development of a new technology node.

Random dopant fluctuation is reasonable for devices with very small dimensions. Although typically the channel concentration looks pretty high (e.g., $10^{18}$ $cm^{-3}$), the

total amount of dopants in the small volume of a nano-scale device is small and the distribution of dopants becomes "discrete." For example, for a semiconductor with dopant concentration of $10^{18}$ $cm^{-3}$, there are only 8 dopants in a cube with edge length of 20 nm. As a result, the introduction or losing of one dopant may result in a significant change in device performance. To cope with the situation, possible solutions are the use of intrinsic-channel SOI and/or to control the vertical doping profiles [28-29]. Besides, advancement of the process techniques to improve the control over film thickness, channel length, and channel width is also essential. Another way is to develop novel structure like DG-SOI [33] to increase gate controllability, or through appropriate circuit design to reduce the impact of device variability. For example, the use of independent multiple-gated configuration to independently manipulate the potential of different channel region.

## 1-3 Motivation

Although poly-Si thin-film transistors (TFTs) are typically fabricated with planar structure, it was expected that the DG scheme is useful to improve the device performance, especially when the channel is thin. Actually, very few works were devoted to fabricate and explore poly-Si TFTs configured with multiple-gate, not to mention the associated effects like the volume inversion as well as the ability of $V_{TH}$

modulation with independent gate control. This motivates us to fabricate planar DG poly-Si TFTs and study these interesting topics. In addition to the planar devices, we have also investigated the characteristics of an inverse-T double-gated nanowire (NW) TFT that was developed previously in our group [34]. Issues like $V_{TH}$-fluctuation due to channel length and width, as well as the intrinsic variation from the defects contained in the channel, are investigated. Suppression of the $V_{TH}$-fluctuation with independent gate control modes is also explored in our study.

## 1-4 Thesis Organization

After the overviews of DG devices and $V_{TH}$-fluctuation issues introduced in this chapter, in Chapter 2, we will briefly introduce our device process flow and the measurement methods. Chapter 3 will be dedicated to the electrical characteristics of doubled-gated TFT. Three operation modes, namely, TG mode (i.e., bias applied to the top-gate with grounded bottom-gate), BG mode (i.e., bias applied to the bottom-gate with grounded top-gate), and DG mode (i.e., bias applied to the top-gate and bottom-gate simultaneously) will be discussed in Section 3.1. The modulation of $V_{TH}$ by using multiple independent gates will be investigated in Section 3.2. In Chapter 4, we will discuss the variation of $V_{TH}$ and the impacts of some parameters, namely, channel length, channel width and channel dopant concentration. Besides, we

will also explore the methods to suppress the $V_{TH}$-fluctuation. Then, conclusions and future work will be summarized in Chapter 5.

# *CHAPTER 2*

# Device Fabrication and Measurements

## 2-1 Device Structure and Process Flow

### 2-1-1 Process Flow of DG-TFTs

The structure of planar DG-TFTs is shown in Fig. 2-1. Schematic flow-charts of the fabrication process for the proposed devices are shown in Figs. 2-2 (a) to (d). Briefly, 6-inch n-type Si wafers were used as the starting substrate. First, 100nm in-situ doped n+ poly-Si was deposited on Si substrate to serve as the bottom-gate, followed by depositing an oxide layer with low-pressure chemical vapor deposition (LPCVD) to serve as the dielectric of the bottom-gate. The bottom oxide thickness was split at 20nm and 50nm (Fig. 2-2 (a)).

An amorphous-Si layer with thickness of 30nm or 50nm was then deposited by LPCVD system, followed by an annealing step at 600°C in $N_2$ ambient for 16-hour to transform the amorphous-Si into poly-Si. Afterwards, polysilicon active layer was definite by I-line lithography and subsequent dry etching steps (Fig. 2-2 (b)). Then, a 20nm-thick top-gate oxide was formed by LPCVD, followed by the deposition of 100nm poly-Si top-gate (Fig. 2-2 (c)). Subsequently, poly-Si top-gate was defined by I-line lithography and patterned by dry etching step. Top-gate and Source/Drain (S/D)

implant were performed by $P^+$ implantation at 35keV for split with channel body of 50nm and 25KeV for the split with channel body of 30nm, both with dose of $5\times10^{15}\,cm^{-2}$ (Fig. 2-2 (d)). Next, a 400nm $SiO_2$ passivation layer was deposited, followed by a standard metallization procedure to form metal pads. Finally, $NH_3$ plasma treatment was performed at 300°C for 1-hour before characterization.

## 2-1-2 Process flow of Inverse-T Double-gated NWTFTs

The top view and cross-sectional view of an inverse-T double-gated NWTFT are shown in Fig. 2-3. Schematic flow-charts of the fabrication process for the proposed devices are shown in Figs. 2-4 (a) to (f). Briefly, 6-inch n-type Si wafers were used as the starting substrate. A 100nm-thick $SiO_2$ layer was deposited to simulate a glass-like substrate. Then a 150nm-thick *in situ* doped $n^+$ poly-Si was deposited, followed by twice applying the standard G-line lithography and dry etching steps to form the inverse-T gate (Figs. 2-4 (a), (b)). A 20 nm-thick oxide layer was then deposited by LPCVD system to serve as the dielectric of inverse-T gate. Afterwards, a 100nm-thick amorphous-Si layer was deposited by LPCVD system, followed by an annealing step at 600°C in $N_2$ ambient for 24-hour to transform the amorphous-Si into poly-Si (Fig. 2-4 (c)). Source/drain (S/D) implant was performed by $P^+$ implantation at 15keV and $1\times10^{15}\,cm^{-2}$ (Fig. 2-4 (d)). It should be noted that the implant energy was kept low so

that the implanted dopants were distributed near the top surface of the poly-Si layer. S/D photoresis (PR) patterns were formed by G-line lithography and defined simultaneously with the NW channels in subsequent reactive plasma etching step (Fig. 2-4 (e)). Channel size can be controlled by carefully adjusting the over-etching time. A 20nm-thick oxide was deposited by LPCVD to serve as the top-gate oxide, and a 100nm-thick *in situ* doped $n^+$ poly-Si was then deposited and patterned to serve as the top-gate (Fig. 2-4 (f)). Finally, a 200nm-thick $SiO_2$ passivation layer was deposited, followed by a standard metallization process to form metal pads. Finally, $NH_3$ plasma treatment was performed at 300°C for 3-hour before characterization.

## 2-2 Electrical Characterization and Measurement Setup

Electrical characteristics of all devices were characterized by HP 4156 semiconductor parameter analyzer and Interactive Characterization Software (ICS) program. During the measurements, the temperature was kept at a stable value by temperature regulated hot-chuck.

From the $I_D$-$V_G$ curve measured at $V_D$ = 0.5V, the characteristics of DG-TFTs and NW devices including subthreshold swing (SS), threshold voltage (Vth) and field-effect mobility ($\mu_{FE}$) can be extracted according to their definition stated below:

Subthreshold swing (SS) can be calculated from the subthreshold current in the weak inversion region by

$$SS = \frac{\partial V_G}{\partial (\log I_D)} \quad (2\text{-}1).$$

The threshold voltage is defined by using the constant current method, i.e., the gate voltage ($V_G$) needed to achieve a drain current ($I_D$) of (W/L)×10nA:

$$V_{TH} = V_G @ I_D = \frac{W}{L} \times 10nA \quad (2\text{-}2),$$

where W and L are channel width and length, respectively.

Finally, the field-effect mobility ($\mu_{FE}$) is determined by

$$\mu_{FE} = \frac{LG_m}{WC_{OX}V_D} \quad (2\text{-}3),$$

where $G_m$ is the maximum transconductance and $C_{ox}$ is the gate capacitance per unit area.

The transconductance, Gm, is extracted by the differentiation of $I_D$ to $V_G$

$$G_M = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const} = \left(\frac{W}{L}\right)\mu C_{OX} V_D \quad (2\text{-}4).$$

# *CHAPTER 3*

# Double-Gated Thin-Film Transistors

## 3-1 Electrical Characteristics of Various Operation Modes

DG-TFTs can be operated in several different modes, namely, single-gated (SG) modes and double-gated (DG) mode. In SG modes, a sweeping bias is applied to one gate (denoted as the driving gate) while the other gate, denoted as the control gate, is applied with a fixed voltage (usually 0V); whereas in DG mode, the top-gate and bottom-gate are connected together to serve as the driving gate. In this work two SG modes are investigated: the first mode using the top-gate as the driving gate with the bottom-gate grounded is called the top-gate (TG) mode; the other SG mode, called the bottom-gate (BG) mode, has the biasing configuration opposite to the TG mode.

Figure 3-1 shows the transfer curves of a device with channel thickness of 30nm and symmetrical gate oxide of 20nm, under DG, TG, and BG mode of operations. Figs. 3-1(a) & (b) show the characteristics before and after $NH_3$-1hour plasma treatment, respectively. It is clear that devices operating DG mode exhibit better performance, such as steeper SS and higher on-current. The BG mode depicts the worst subthreshold slope (SS) among the three modes of operation in Fig.3-1(a), implying

the poorer crystallinity in the bottom channel. Nevertheless, it is obvious that the subthreshold slope (SS) in BG mode has been significantly improved by plasma treatment since the defects at grain boundaries have been effectively passivated, and the SS of the BG mode become closer to that of the TG mode, as shown in Fig.3-1(b).

As mentioned above, thanks to its strong gate controllability, DG mode depicts steeper subthreshold slope (SS) compared with the SG mode. This is also confirmed in Fig. 3-1(b), in which SS is 554 mV/dec and 690mV/dec for TG mode and BG mode, respectively. It is worthy to note that SS is 422mV/dec for DG mode due to the coupling effect of the two channels. Owing to twice the conductive width compared with either TG or BG mode, DG mode has a higher drive current than either TG or BG mode, resulting in a larger $I_{on}/I_{off}$ ratio.

Figure 3-2 shows the TG and DG transfer characteristics of a short-channel device (L=0.7μm) with drain voltage of 0.5V and 3.5V, respectively. It could be seen that drain induced barrier lowering (DIBL) can be slightly suppressed with the DG mode.

Figure 3-3 shows the transfer characteristics of a device with channel thickness of 50nm and symmetrical gate oxide of 20nm, under DG, TG, and BG modes of operation. The device received a plasma treatment before the characterization. Since the channel body is thicker than the devices characterized in Figs. 3-1 and 3-2, the

gate-to-gate coupling effect should be weaker. This explains why the DG mode exhibits less improvement in SS over the SG modes.

For the structures studied above, the bottom gate oxide and the top gate oxide are both 20nm-thick. We have also investigates cases with asymmetric gate oxide (i.e., the thickness of the bottom gate oxide and the top gate oxide are different.). Figure 3-4 (a) shows the transfer characteristics of a device with 30nm-thick channel body, 20nm-thick top gate oxide, and 50nm-thick bottom gate oxide. Since the bottom oxide is much thicker than the top one, the BG mode shows much worse performance than the TG mode, so the operation of the DG mode is actually dominated by the conduction of the top channel. As a result, the DG curves are very close to the TG curves. With 50nm-thick channel body, 20nm-thick top gate oxide and 50nm-thick bottom gate oxide, as shown in Fig. 3-4(b), the trend becomes even clear. The SS under various operation modes are summarized in Table 3-1.

Figure 3-5 shows output characteristics of a device with 30nm-thick channel body with symmetric gate oxide. It is found that TG mode has a higher drive current than BG mode. It is ascribed to the small grain size in the bottom channel region. This also results in the degradation of mobility as shown in Fig. 3-6. It is worth noting that the drain current is enhanced in DG mode, as shown in Fig. 3-5. As can be seen in the figure, the on-current of the DG mode is actually higher than the sum of the two SG

modes. However, the mobility characteristics tell a different story. As can be seen in Fig. 3-6, the peak value of mobility of the DG mode extracted at $V_d$=0.5 V is actually smaller than the SG modes.

There are many reports investigating the so-called “volume inversion” phenomenon that may happen when the channel body is sufficiently thin [35]. If the channel body is thicker than the maximum depletion width, there will be negligible interaction between the top and the bottom channels. In such case, the DG operation is simply the combination of two independent MOSFETs in parallel. However, if the channel body is thinner than the maximum depletion width, the two triangular shape quantum potential wells of the opposite channels will couple each other, as shown in Fig. 3-7. Such coupling effect may lead to the redistribution of the inversion electrons throughout the entire channel body, rather than concentrating near the top and bottom $Si/SiO_2$ interfaces, a phenomenon known as “volume inversion”. Note that such volume inversion happens in an ultra-thin body and is significant at a low transverse electric-field (see Fig. 3-8). When vertical electric field increases, the volume inversion is weakened, since inversion charges will tend to accumulate toward the interfaces due to the high vertical electric field.

Volume inversion has several significant advantages, such as [35-36]

(a) an enhancement of carriers density,

(b) a reduction of surface scattering, thus an increase in mobility, and

(c) an increase in drain current and transconductance.

These advantages for DG devices were previously reported for devices with crystalline Si channel. To this date, no related works are reported on the cases using poly-Si channel. To confirm if the volume inversion happens, Figure 3-9 shows the drain current ratio of DG mode to the sum of TG and BG modes. It is found that the drain current in DG mode is larger than the sum of TG and BG modes, especially in low gate voltage. In low gate voltage ($V_g$-$V_{TH}$=1 or 2V), the drain current ratio ($I_{DG}/(I_{TG}+I_{BG})$) can be around 1.5 x. It may be due to the volume inversion or the decrease of series resistance. Figure 3-10 shows the series resistance. The series resistance is 43KΩ for TG mode and 40KΩ for BG mode. It drops to 33KΩ for DG mode, which is larger than the equivalent resistance of the two parallel TG and BG resistances (~22KΩ). This means that the series resistance in DG mode is not low enough to contribute so large an enhancement in $I_{DG}$ shown in Fig. 3-9. However, there is no enhancement in DG mode mobility (shown in Fig. 3-6). Figure 3-11 shows the device transconductance in DG, TG, and BG modes, where $G_{m(DG)}/(G_{m(TG)}+G_{m(BG)})$ is smaller than 1. Some remarks on the results are drawn here. First, the mobility extracted from the Gm is the so-called field-effect mobility, which is different than the equivalent mobility value [37]. Sometimes it cannot represent the whole picture of the

mobility characteristics. Second, although volume inversion may reduce the surface scattering rate, in the present case the inversion electrons accumulate in the channel may suffer from the scattering events with the defects contained in the grain boundaries of the poly-Si channel. This may explain the degraded mobility under the DG mode. Based on the analysis, we conclude that the enhancement in drain current under DG mode mainly comes from the increase of inversion electron concentration.

To understand the importance of the channel thickness, we have also characterized devices with 50nm-thick channel body with symmetric gate oxide. Typical output characteristics are shown in Fig. 3-12(a), and Fig. 3-12(b) plots the drain current ratio ($I_{DG}/(I_{TG}+I_{BG})$). The ratio is around 1x, indicating the top and bottom channels are operating independently.

## 3-2 Device Characteristics with Independent Double-gated Operation

Conventionally, we employ channel implant and gate work function to adjust the $V_{TH}$. However, channel implant leads to a larger characteristics fluctuation due to random dopant distribution, while the gate work-function can not adjust the $V_{TH}$ widely. In recent years, several works have reported that a 4-terminal configuration (i.e., source, drain, first and second gates) can modulate the $V_{TH}$ flexibly [15-20]. Due

to the thin body, the channel potential is sensitive to both gates, and thus strong gate-to-gate coupling phenomenon can be observed and would allow the tunable threshold voltage by adjusting the voltage applied to the control gate.

In the following characterization, the top-gate (TG) is used as the driving gate and the bottom gate (BG) is used as the $V_{TH}$-control gate. Figure 3-13 shows the modulation on $V_{TH}$. It is obvious that $I_d$-$V_g$ curve shifts with various BG voltage, and $V_{TH}$ can be effectively modulated. Figure 3-14 shows the extracted $V_{TH}$ and SS from Fig.3-13 as a function of bottom-gate voltage. The plots are divided into two regions by $V_{TH(DG)}$, the $V_{TH}$ measured in DG mode. In this case with 30nm-thick body, $V_{TH(DG)}$ is 1.1V. It is found that $V_{TH}$ shift rate at high $V_{BG}$ is larger than that at low $V_{BG}$. The $V_{TH}$ shift rate at $V_{BG}<V_{TH(DG)}$ is 0.32V/V and 2.84V/V at $V_{BG}>V_{TH(DG)}$. On the other hand, the SS increases with increasing $V_{BG}$ and soars as $V_{BG}>V_{TH(DG)}$.

The above findings can be explained as follows: as $V_{BG}$ is smaller than $V_{TH(DG)}$, the bottom channel is depleted and the inversion layer is formed on the top-gate channel only. In this situation, since the distance between bottom gate and inversion layer (the total distance is about the thickness of bottom gate oxide plus the fully depleted body) is quiet long, the modulation ability of bottom gate voltage on $V_{TH}$ is relatively weak. When $V_{BG}$ is larger than $V_{TH(DG)}$, the channel is formed on the surface of the bottom gate side, $V_{TH}$ modulation ability is strong due to the short distance

between the inversion layer and bottom gate. However, the parasitic leakage path along the bottom-channel may also deteriorate the SS of the transfer characteristics driven by the TG.

To more deeply understand this phenomenon, a simple model with schematic potential distributions described in Fig. 3-15 proposed in a previous work [15] is adopted. The G2 is defined as the $V_{TH}$-control gate and G1 as the driving gate. Si channel body is assumed to be fully depleted. $T_{ox1}$ and $T_{ox2}$ are multiplied by a factor of 3 according to the ratio of the dielectric constant (i.e., $\varepsilon_{Si}/\varepsilon_{SiO2}$=11.9/3.9). Since the Si body and the oxide are treated as an identical dielectric, we can plot the potential distribution as straight lines. For state A ($V_{G2}<V_{TH(DG)}$) in the figure, recall that the channel is formed on the G1 side. We can obtain the back-gate-effect factor $\gamma = dV_{TH(G1)}/dV_{G2}$ through the similarity of $\triangle ABC$ and $\triangle DEC$, which can represent the $V_{TH}$ shift rate and subthreshold slope as

$$\left|\frac{\partial V_{TH(G1)}}{\partial V_{G2}}\right| = \frac{3T_{ox1}}{3T_{ox2}+T_{Si}} = \gamma_A \tag{3-2}$$

$$\text{and} \quad S_A = 0.06\cdot(1+\gamma_A) \tag{3-3}$$

, respectively, where $T_{ox1}$ and $T_{ox2}$ are the top- and bottom-gate oxide, respectively, and $T_{si}$ is the channel body thickness.

For state C ($V_{G2}>V_{TH(DG)}$), the channel is formed on the G2 side. Similarly, the $V_{TH(G1)}$ shift rate by varying $V_{g2}$ and the subthreshold slope are expressed as

$$\left|\frac{\partial V_{TH(G1)}}{\partial V_{G2}}\right| = \frac{3T_{ox1} + T_{Si}}{3T_{ox2}} = \gamma_C \quad (3\text{-}4)$$

$$\text{and} \quad S_C = 0.06 \cdot (1 + \gamma_C) \quad (3\text{-}5).$$

It is noted that the SS is proportional to (1 + γ) analytically, thus the SS is smaller when $V_{G2} < V_{TH(DG)}$, but lager when $V_{G2} > V_{TH(DG)}$. From this model, we can expect that $V_{TH(TG)}$ shift rate as $V_{BG} < V_{TH(DG)}$ is less than that as $V_{BG} > V_{TH(DG)}$. And SS is worse in the situation as $V_{BG} > V_{TH(DG)}$, which is consistent with the result shown in Fig. 3-13.

Figure 3-16 shows the $V_{TH}$-modulation with 50nm body thickness. $I_d$-$V_g$ hardly shifts with different BG voltage since the 50nm-thick body is too thick for the coupling to occur. When BG voltage increases, the off-current becomes larger due to the existence of leakage path along the bottom channel. Obviously the ability of $V_{TH}$-modulation in 50nm-thick body is much weaker than that of 30nm-thick body.

As mentioned above, SS is inversely proportional to $T_{ox2}$ ($SS\alpha\frac{1}{T_{ox2}}$). It implies that SS can be further lowered when the bottom gate oxide ($T_{ox2}$) is thicker [40]. Figure 3-17 shows the $I_d$-$V_g$ curves modulated by the bottom-gate voltage. Note in this figure the characterized device has identical structural parameters as that in Fig. 3-13 except for the thicker $T_{ox2}$. Compared with the results shown in Fig. 3-13, owing to the thick $T_{ox2}$, the off-state leakage is effectively suppressed even at a high bottom gate voltage. Figure 3-18 compares the $V_{TH}$ and SS as a function of bottom gate

voltage between the devices with symmetric and asymmetric $T_{ox}$. It is seen that SS is dramatically improved especially for the condition of $V_{BG} > V_{TH(DG)}$ (i.e., channel formed in the BG side). The thicker bottom gate oxide will weaken back-gate-effect on surface potential, thus SS can be improved. To recall the pervious model, it can be expected that the back-gate-effect $\gamma$ is relatively small compared with the symmetric $T_{ox}$, which results in a smaller $V_{TH}$ shift rate.

Since we can widely tune the $V_{TH}$ through the back gate bias, it is useful for application in high-performance and low standby power VLSIs. For active state, a positive $V_{BG}$ is applied in order to get a higher drive current. For standby state, a negative $V_{BG}$ is applied in order to obtain a small off-state leakage, which is shown in Fig. 3-19.

# *CHAPTER 4*

# Threshold Voltage Fluctuation

## 4-1 Random Dopant Induced Threshold Voltage Fluctuation

As we mentioned in Chapter 1, with aggressive scaling of operation voltage, devices become increasingly more sensitive to the fluctuations in the device characteristics. In this Chapter, we investigate the issue associated with the multiple-gated TFTs devices with nanowire (NW) channels. These devices were provided from seniors of our group. The cross-sectional transmission electron microscopic (TEM) images of two types of such devices with triangular-shaped NW channel are shown in Fig. 4-1. Figure 4-1(a) shows the one with larger NW dimensions of around 40nm, 50nm and 80nm. This type is denoted as NW-A. The other type, denoted as NW-B, is with smaller NW dimensions of around 20nm, 30nm and 45nm. In the following fluctuation analysis, we measure around 25 to 30 devices for each split of device structures.

Figure 4-2 shows the transfer characteristics of 25 NW-A type devices with various channel length. Figure 4-3 shows the $V_{TH}$ distribution of these splits shown in Fig. 4-2. From the figures it is obviously seen that the range of $V_{TH}$ distribution

becomes wider as the channel length is shortened. The trend is consistent with the data reported in previous papers [26-32]. Figure 4-4 shows characteristics of the NW-B devices. Trends are similar to those observed in the NW-A devices (Fig. 4-2 and Fig. 4-3), albeit with tighter distribution, thanks to the smaller dimensions in the NW-B type.

To more deeply understand the experimental results, a simple $V_{TH}$ fluctuation model considering the random-dopant-fluctuation (RDF) is adopted in this study [42]. Figure 4-5 shows the vertical electric field, E, as a function of depth, x, in the channel region. If there is an extra charge sheet $\Delta Q$ placed within the channel depletion layer, E(x) will be modified from the solid line to the dashed line so that the voltage drop between surface and the depletion region edge ($x=W_{DEP}$) is constant. A change in the surface electric field will result in a $V_{TH}$ shift, expressed as

$$\Delta V_{TH} = (\frac{\Delta Q}{C_{OX}})(\frac{1-x}{W_{DEP}}) \quad (4\text{-}1),$$

which is valid for both uniform doping and non-uniform doping.

Assuming that the extra charge sheet ($\Delta Q$) volume is $LW\Delta x$, the standard deviation of $\Delta Q$ is expressed as

$$\Delta Q = \frac{q}{LW}\sqrt{N(x)LW\Delta x} \quad (4\text{-}2)$$

where N(x) is the doping concentration, L and W are channel length and width, respectively. Standard deviation of $V_{TH}$ can be obtained by integrating the charge

sheet from x=0 to x= $W_{DEP}$, expressed as

$$\sigma V_{TH}^2 = \sum_{x=0}^{x=W_{DEP}} \Delta V_{TH}^2 \quad (4\text{-}3).$$

This expression results in

$$\sigma V_{TH} = \frac{q}{C_{OX}} \sqrt{\frac{N_{EFF} W_{DEP}}{3LW}} \quad (4\text{-}4),$$

where $N_{EFF}$ is a weighted average of N(x), defined as

$$N_{EFF} = 3 \int_0^{W_{DEP}} N_{SUB}(x)(1 - \frac{x}{W_{DEP}})^2 \frac{dx}{W_{DEP}} \quad (4\text{-}5).$$

From Eq. (4-4), we can obtain the relationship between standard deviation of $V_{TH}$, channel length, and width,

$$\sigma V_{TH} \propto \frac{1}{\sqrt{LW}} \quad (4\text{-}6).$$

It should be noted that, the above model considers the dopant fluctuation effect in bulk CMOS devices. It is well known that threshold voltage is dependent on the channel dopant concentration since the channel dopants need to be depleted first in order to effectively shift the surface potential with the applied gate voltage. In the present case, no intentional doping was implemented in the poly-Si NW channels of the fabricated devices. However, similar situation happens to poly-Si NW channels. Note that there are many defects presenting in the grain boundaries. These defects act as trap centers and a large portion of them are occupied by electrons before the channel potential is inverted. As a result the threshold voltage can be expressed as

[43]

$$V_{TH} \cong V_{FB} + 2\phi_F + \frac{qN_{Trap}W_d}{C_{OX}} \quad (4\text{-}7),$$

where $N_{Trap}$ and $W_d$ are trap states density and effective depletion width, respectively. The equation above is valid for partially depleted body ($T_{si}>W_d$). Figure 4-6 shows the schematics of $V_{TH}$ dependence of trap density at poly-Si grain boundaries. When the body is fully depleted, $W_d$ is simply $T_{si}$. For a multiple-gated configuration $W_d$ is smaller than $T_{si}$. For example, the double-gated configuration shown in Fig.4-6(c), $W_d$ is a half of $T_{si}$.

As stated above, similar to the dopants in the channel of bulk devices, the defects presenting in the grain boundaries of the poly-Si films affect the threshold voltage and subthreshold swing of devices, so it is assumed that the defects also play a similar role as the dopants in affecting the device performance fluctuation. So in the following analysis the $N_{EFF}$ in Eqs. (4-4) and (4-5) is considered to be the effective defect concentration, $N_{Trap,}$ contained in the poly-Si NW layer.

Figure 4-7 shows the $V_{TH}$ deviation as a function of $\sqrt{LW}$ . The trend is very well described by the model mentioned above. In Fig. 4-7, it is obvious that $V_{TH}$ deviation in thicker NW body (NW-A) is larger than that in thinner NW body (NW-B). This is reasonable according to Eq. 4-4, since a larger depletion width leads to more dopant fluctuation. Figure 4-8 shows the $V_{TH}$ deviation after normalizing the effective

depletion width where the depletion width ($W_d$) is estimated to be half of maximum poly-Si NW thickness in Fig. 4-1, which is around 4nm-thick for NW-B and 12nm-thick for NW-A. After the treatment the two curves becomes very close to each other, confirming the suitability of the model for fluctuation analysis.

Since the grain size and grain number vary from cell to cell, such effective trap states at grain boundaries will lead to $V_{TH}$-fluctuation. In order to study the impact drawn by the trap density, we have investigated and compared the characteristics of $V_{TH}$-fluctuation before and after $NH_3$-plasma treatment. The $V_{TH}$ distributions before and after $NH_3$-plasma treatment are shown in Fig. 4-9. It can be seen that the mean value and standard deviation of $V_{TH}$ before $NH_3$-plasma treatment is larger than those after treatment. This indicates that the $NH_3$-plasma treatment can effectively passivate the trap states and result in a significantly reduced trap density. The effective trap states density per unit area, $T_{Trap}$, in the poly-Si NW channel can be extracted from the subthreshold swing with the following equation.

$$SS = \ln 10 \times (\frac{kT}{q}) \times (1 + \frac{C_{dm}}{C_{ox}}) \text{, where } C_{dm} = q \times T_{Trap} \qquad (4\text{-}7)$$

For the thicker poly-Si channel fabricated in this chapter, the SS for fresh device is around 350mV/dec (see Fig. 4-10), which is equivalent to $T_{Trap}=5.2\times10^{12}$ $cm^{-2}$. The SS after $NH_3$-plasma treatment is about 150mV/dec, converting to $T_{Trap}=1.6\times10^{12}$ $cm^{-2}$. And the effective trap-state concentration ($N_{Trap} = T_{Trap}/W_d$) can be calculated.

The $T_{Trap}$ extracted from the SS and effective trap states concentration are summarized and listed in Table 4-1.

For effective trap states, it should follow a Gaussian distribution in the NW channel. The standard deviation of $N_T$, $\sigma N_T$ is equal to the square root of $N_T$ [27]. Thus, the standard deviation of $V_{TH}$ due to $\sigma N_T$ is proportional to $\sqrt{N_T}$. Figure 4-11 shows $V_{TH}$ standard deviation as a function of $\sqrt{N_T}$ for the NW-A devices, which confirms the inference. Another expression is shown in Fig. 4-12. In Fig. 4-11(a), the $V_{TH}$ standard deviation is expressed as a function of $\frac{1}{\sqrt{LW}}$. The curve for the devices before plasma treatment exhibits a much steeper slope, owing to a higher trap density. When the trap density is taken into account, as shown in Fig. 4-12(b) in which the $V_{TH}$ standard deviation is expressed as a function of $\sqrt{\frac{T_{trap}}{LW}}$, the two lines tend to converge each other. The same phenomenon is also observed in NW-B devices, as shown in Fig. 4-13. Figure 4-14 shows the standard deviation of $V_{TH}$ as a function of $\sqrt{\frac{W_d T_{trap}}{LW}}$ for the two types of NW devices. The two curves coincide each other, as predicted by Eq. (4-5).

## 4-2 Threshold Voltage Fluctuation in Independent Double-gated Operation

In addition to optimize the fabrication and the structural parameters of the

devices, the use of circuit technique to suppress the $V_{TH}$ fluctuation represents another useful approach [40]. In this work various operation modes are investigated to address the feasibility. As we mentioned in previous chapter, DG-TFTs can be operated in three modes. This also applies to the NW-DGTFTs since the devices are configured with two independent gates. From the cross-sectional TEM images shown in Fig. 4-1, it could be seen that NW is surrounded by the top gate and inverse-T gate. In this case, when the top gate and inverse-T gate are both connected together to serve as the driving gate, it is denoted as the DG mode. When sweeping bias is applied to the top gate while the inverse-T gate is grounded, the mode is called the top-gate (TG) mode. When the bias conditions used in the TG mode is interchanged, the mode is called the inverse-T gate (ITG) mode.

Figure 4-15 shows the $V_{TH}$ standard deviation in various operation modes. It is found that standard deviation of $V_{TH}$ is the largest in TG mode with the ITG mode falls in the middle among the three operation modes. Since the NW channel is positioned on the upper-step corners of the inverse-T gate (shown in Fig. 4-1), the effective conduction widths for ITG mode is larger than that of TG mode, resulting in a better gate controllability and a less $V_{TH}$ standard deviation. In DG mode, $V_{TH}$ standard deviation is expected to be the least due to the best gate controllability among the three operation modes

In our device structure, $V_{TH}$ of the single-gate mode can be modulated by the voltage applied to the control gate (e.g., the inverse-T gate in TG mode, and the top gate in ITG mode). In this work we also address the $V_{TH}$-fluctuation issues in these operation conditions. Figure 4-16 shows the distribution of transfer curves of twenty five devices characterized under TG and ITG modes, and Fig. 4-17 shows the $V_{TH}$-fluctuation results as a function of $V_{TH}$-control gate voltage in TG and ITG modes. It is found that the $V_{TH}$ standard deviation is reduced when $V_{TH}$-control gate voltage is applied with -1V for the two single-gate modes. Moreover, such improvement in $V_{TH}$-fluctuation is especially profound as the channel length is scaled down.

It is worth noting that the threshold voltage of the NW-TFTs device under DG mode of operation, $V_{TH(DG),}$ is about 0.42V. Here we consider the operation of the ITG mode when 1V is applied to the top-gate. The device now becomes a normally-on device since an inversion layer will be formed at the channel interface adjacent to the top gate surface. To turn off the device, the voltage applied to the inverse-T gate must be sufficiently negative to deplete the aforementioned conduction channel. Such situation will increase the effective gate dielectric thickness which is about the sum of the thickness of inverse-T gate oxide plus the fully depleted body, thus deteriorating the short-channel effect. As a result, a larger $V_{TH}$-fluctuation is observed in

short-channel devices. This explains the results shown in Fig. 4-17 that $V_{TH}$ standard deviation in devices with channel length of 0.8μm is degraded when 1V is applied to the control gate. For long-channel devices, $V_{TH}$ standard deviation is almost independent of the voltage applied to the control gate since the short channel effect is not obvious. When top-gate voltage is less than $V_{TH(DG)}$, the conduction channel is formed solely at the channel interface adjacent to the inverse-T gate, and short channel effect can be suppressed. Thus, the $V_{TH}$-fluctuation will be less sensitive to the channel length.

Besides, since the distance between inverse-T gate and inversion layer includes the fully depleted body at $V_{TG} > V_{TH(DG)}$, the variation of NW body thickness is another factor that affects the $V_{TH}$ standard deviation. To further explain this phenomenon, we recall the model mentioned in pervious chapter:

Case 1: $$\Delta\left|\frac{\partial V_{TH(G1)}}{\partial V_{G2}}\right| \propto \frac{3T_{ox1}}{3T_{ox2}+T_{Si}+\Delta T_{Si}} \quad \text{for } V_{G2} < V_{TH(DG)} \qquad (4\text{-}8);$$

Case 2: $$\Delta\left|\frac{\partial V_{TH(G1)}}{\partial V_{G2}}\right| \propto \frac{3T_{ox1}+T_{Si}+\Delta T_{Si}}{3T_{ox2}} \quad \text{for } V_{G2} > V_{TH(DG)} \qquad (4\text{-}9).$$

In the two cases, the main difference is the channel body thickness, $T_{si}$. For Case 1 (corresponding to the case when -1V is applied to the top gate), the standard deviation of $T_{si}$ is part of the denominator, which will lead to a reduced standard deviation on $V_{TH}$ shift rate. For the Case 2 (corresponding to the case when 1V is applied to top gate), the standard deviation of $T_{si}$ is part the numerator, which will

amplify the $V_{TH}$-fluctuation.

However, there exists an optimum top-gate (control gate) bias for minimizing the fluctuation. A high negative top-gate bias will result in a large vertical electric field in the Si channel. This will amplify the impact of small $T_{si}$ (i.e., channel thickness of the Si channel) variation on the modulation of the channel potential, thus leading to a larger $V_{TH}$ variation [45]. An example is shown in Fig. 4-18. We can see that the optimized voltage applied to the top-gate (i.e., the control gate) is in the range from 0 to -1V

Figure 4-19 shows the standard deviation of $V_{TH}$ under the TG mode, compared with the DG mode. It is seen that the DG mode has a better suppression in $V_{TH}$ fluctuation, owing to the reduction in effective depletion width. Whereas TG mode with $V_{ITG}$=1V has the worst $V_{TH}$ variation. As mentioned above, this could be ascribed to the increase in effective gate dielectric thickness.

# *CHAPTER 5*

# Conclusions and Future Works

## 5-1 Conclusions

In this thesis, planar DG-TFTs were fabricated and characterized. With thin poly-Si body (30nm), gate-to-gate coupling effect in DG mode is more prominent, resulting in better gate controllability, higher ON-current and steeper sub-threshold swing (SS), compared with the single-gated mode.

Moreover, due to the strong coupling between the top gate and bottom gate, threshold voltage can be modulated over a wide range by $V_{TH}$-control gate. Compared with symmetric gate oxide, subthreshold swing can be slightly improved by using thicker $V_{TH}$-control gate oxide to gain higher $I_{on}/I_{off}$ ratio.

In this study, we also explore the threshold voltage variation in nanowire DG-TFTs. It is confirmed that threshold voltage fluctuation is inversely proportional to channel length and width. Moreover, $NH_3$-plasma treatment can effectively suppress threshold voltage fluctuation owing to the passivation of the trap states.

Besides, it is found that there is an optimum back gate bias for suppressing the short channel effect which may lead to a larger threshold voltage variation.

## 5-2 Future Works

In this thesis, electrical characteristics of planar DG-TFTs have been developed and characterized. For the purpose of further improvement, some topics and directions for the future work are suggested as follows:

1. From the output characteristics, it could be seen that the carrier transport at the top and bottom channel is poor due to the grain boundaries. In this thesis, poly-Si TFTs were prepared by solid-phase crystallization (SPC). However, many methods are known to increase the grain size of the poly-Si thin film, such as excimer laser annealing (ELA) and metal-induced lateral crystallization (MILC). DG-TFTs with large-grain-poly-Si channel are expected to exhibit much improved performance and interesting characteristics under the DG mode of operation.

2. In order to further improve performance, ultra-thin body ($T_{si}$<10nm) is needed to eliminate any leakage paths and to enhance the gate coupling effect. However, the high parasitic resistance due to the ultra-thin body needs to be addressed in the device fabrication.

3. In this thesis, due to the time limitation, we only focus on the study of NW-TFTs fluctuation. Of course the issue also exists in the planar-TFTs, and deserves to be

thoroughly addressed.

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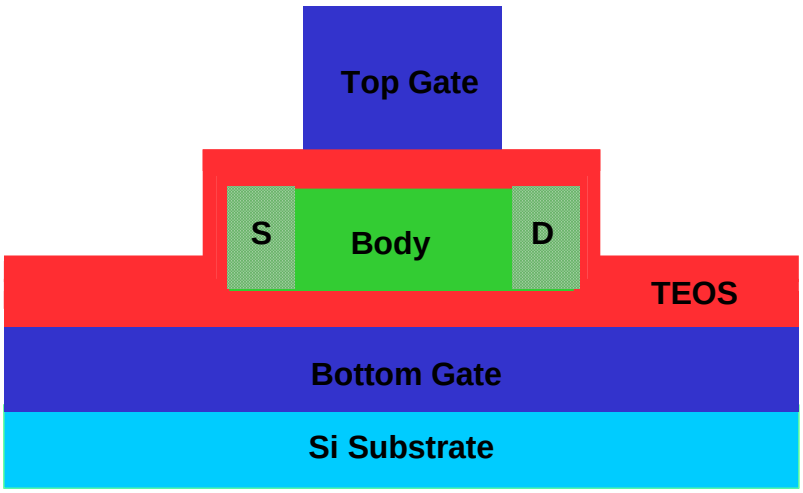



**Fig. 2-1** The structure of DG-TFTs

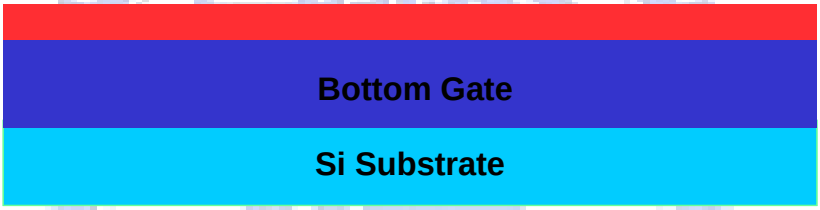



**Fig. 2-2** (a) Deposition of in-situ doped n+ poly-Si bottom gate and bottom gate oxide.

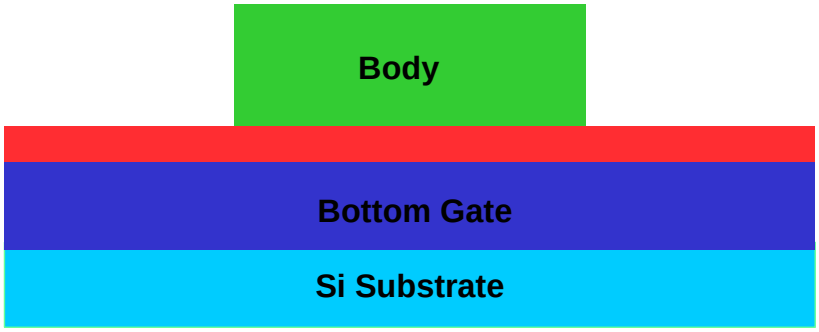



**Fig. 2-2** (b) Deposition and pattern of poly-Si body.

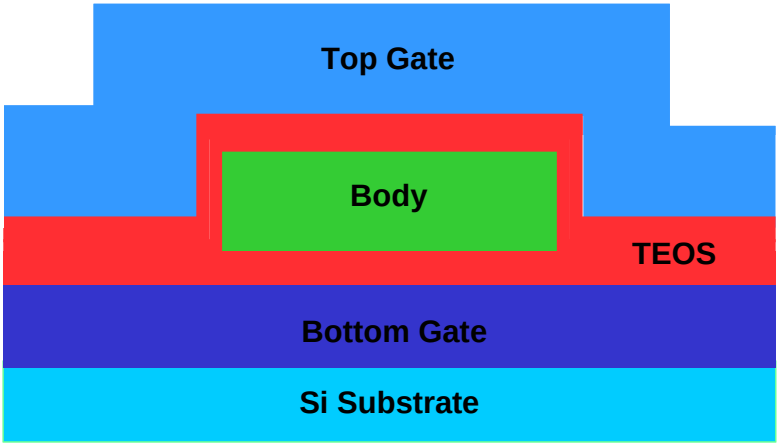



**Fig. 2-2** (c) Deposition of 20nm-thick top gate oxide and 100nm poly-Si top gate.

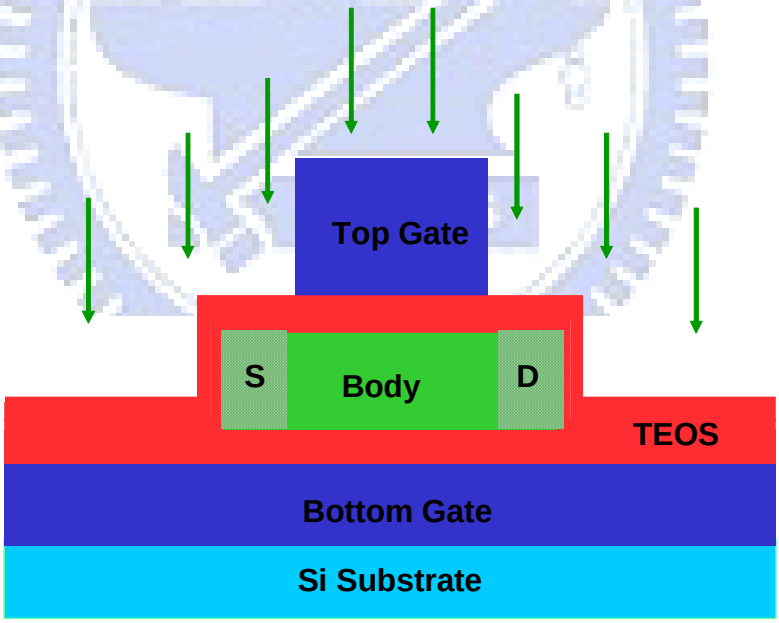



**Fig. 2-2** (d) Definition of poly-Si top gate and self-aligned implantation.

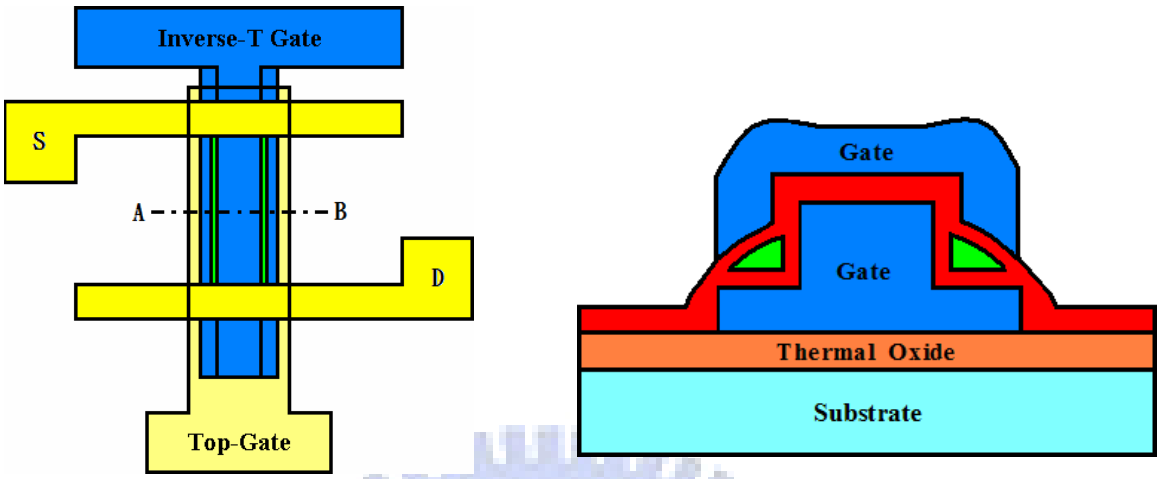



**Fig. 2-3** Top view and cross-sectional view of inverse-T double-gate NWTFTs.

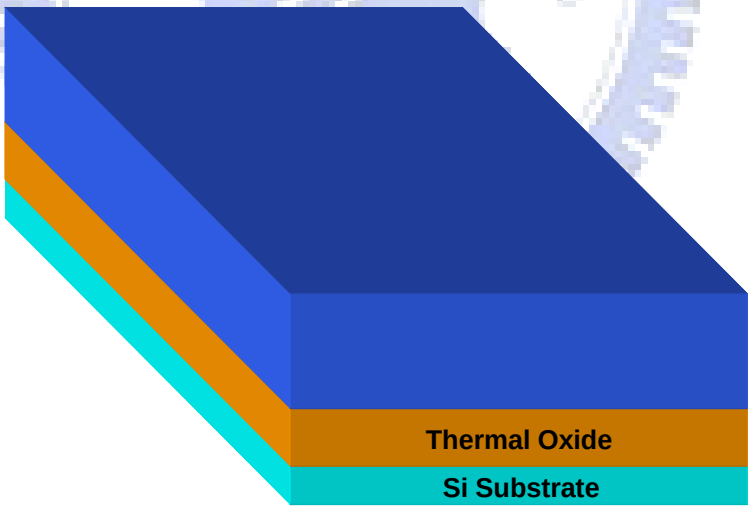



**Fig. 2-4** (a) Deposition of in-situ doped n+ poly-Si on glass like substrate.

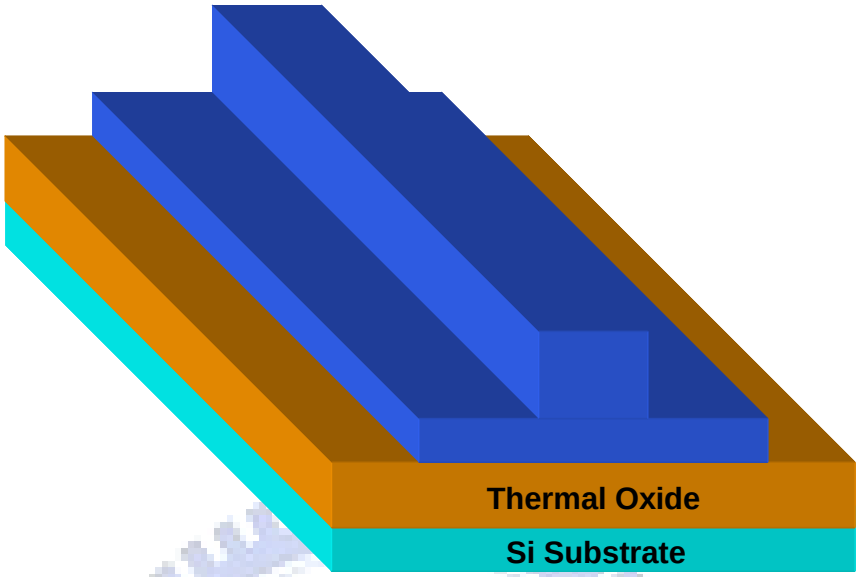



**Fig. 2-4** (b) Definition of inverse-T gate.

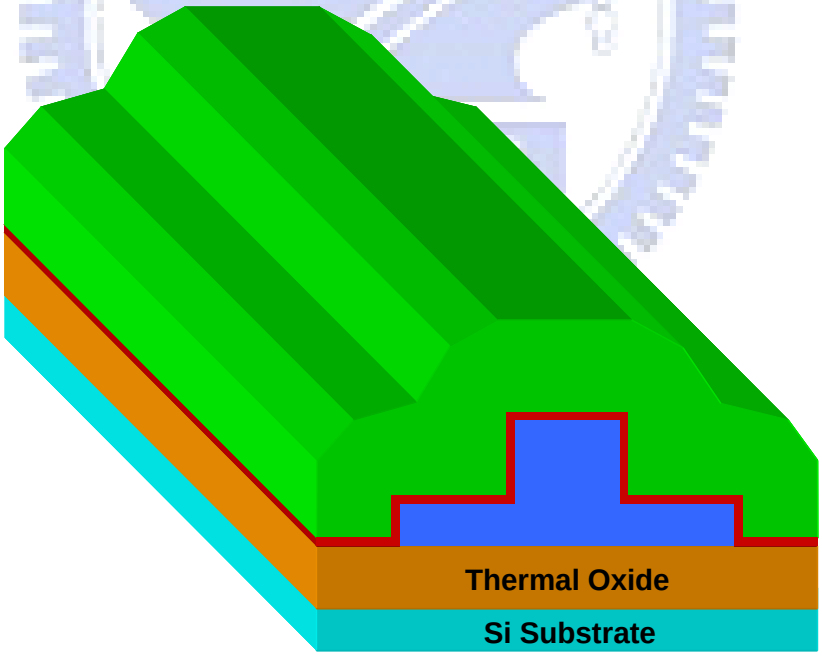



**Fig. 2-4** (c) Deposition of inverse-T gate oxide and poly-Si active layer.

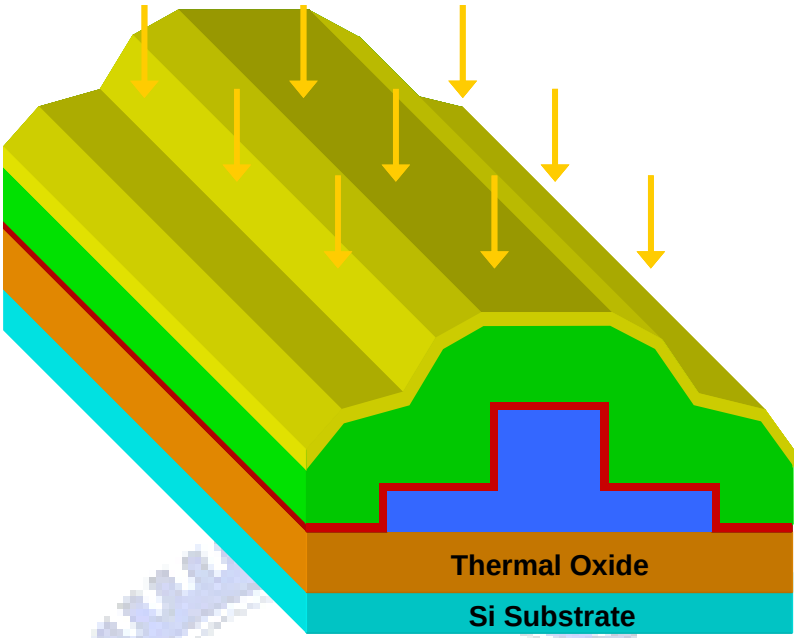



**Fig. 2-4** (d) Source/drain ion implantation.

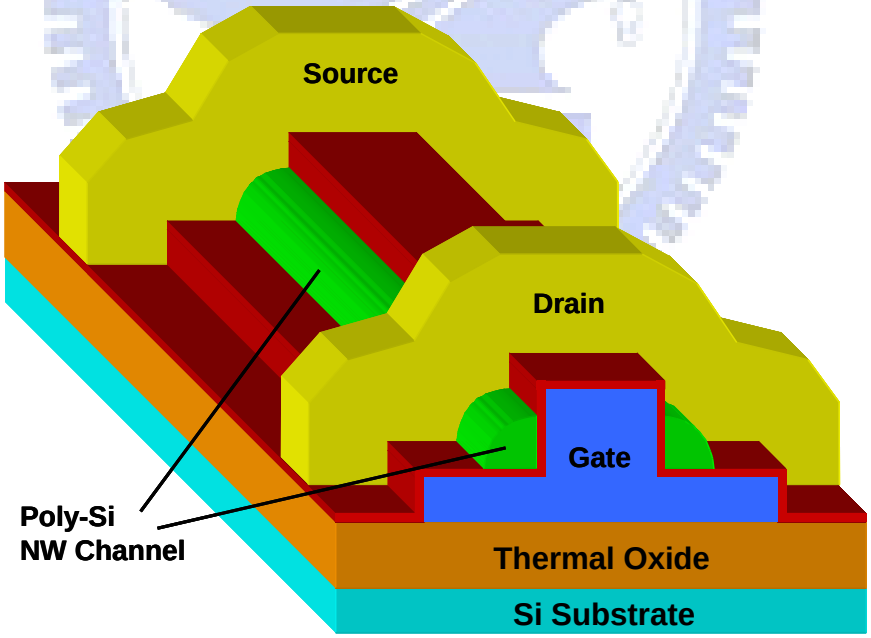



**Fig. 2-4** (e) Definition of source/drain and nanowire channel.

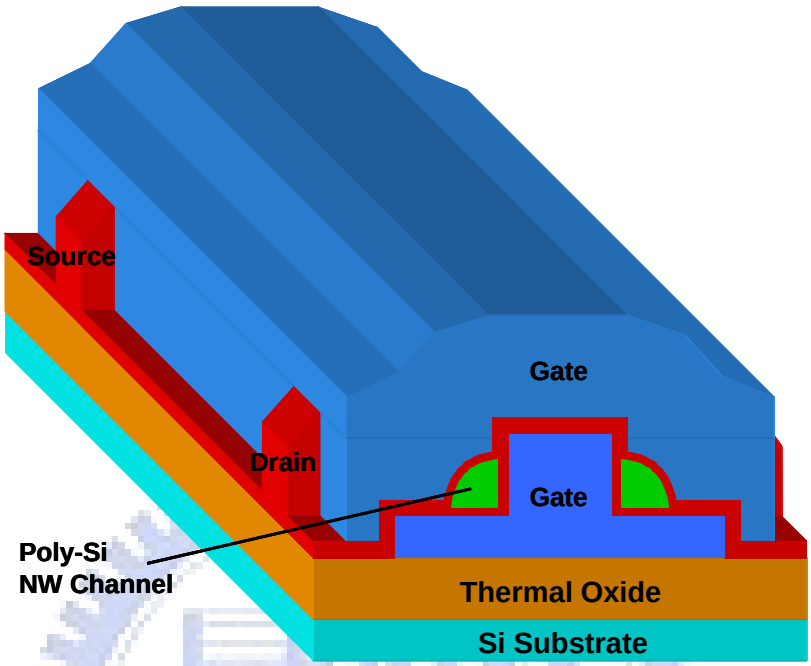
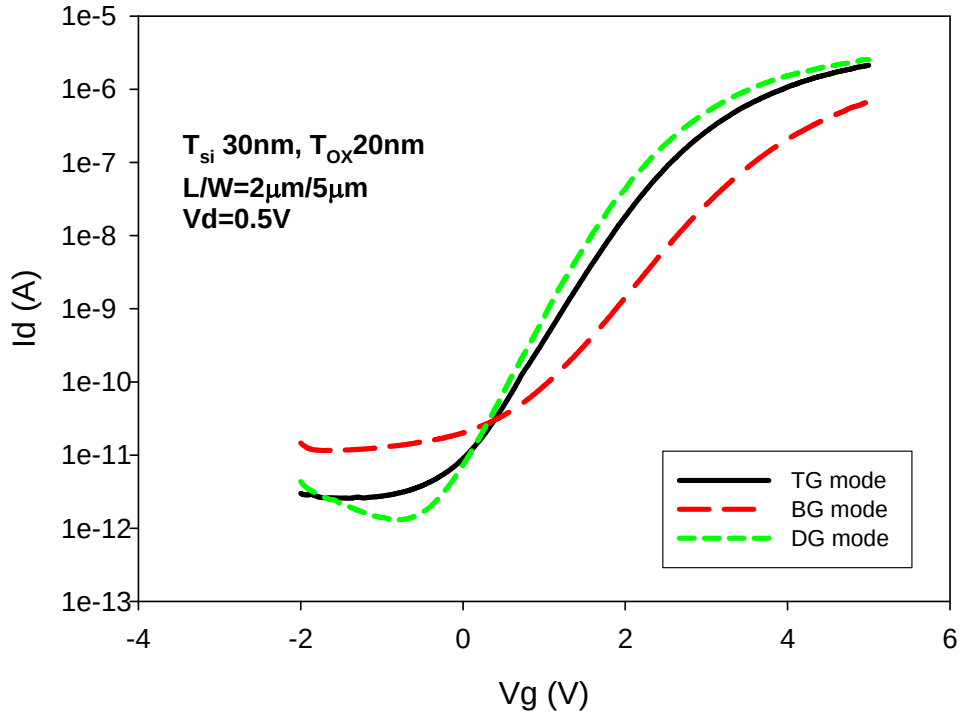
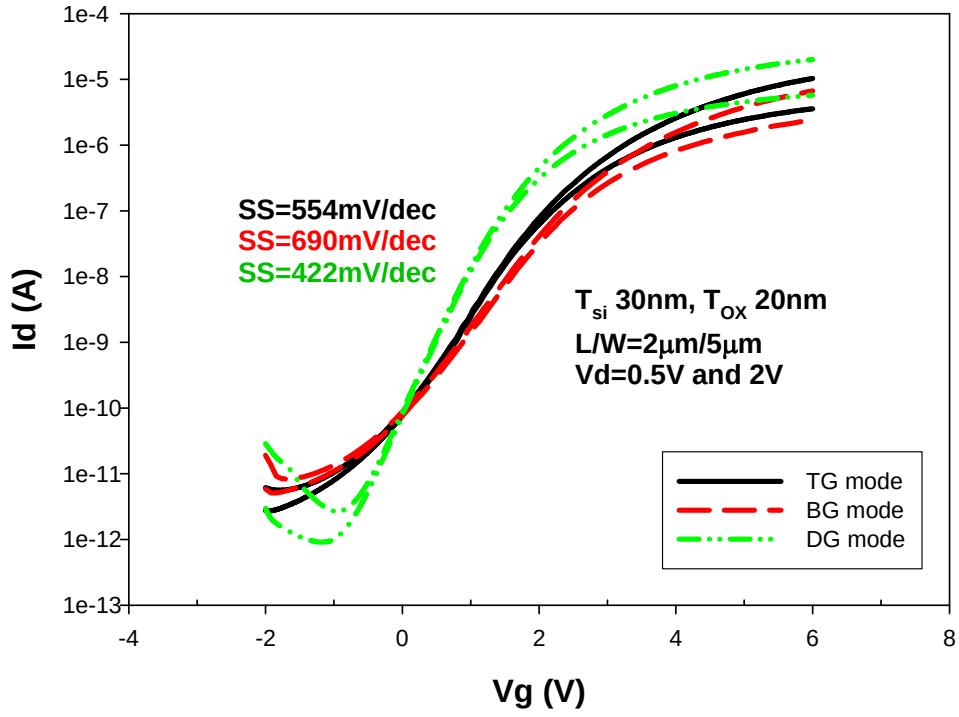



**Fig. 2-4** (f) Formation of top gate.




(a)




(b)

**Fig. 3-1** Transfer characteristics of DG-TFTs under different operation modes: (a) before $NH_3$-plasma treatment, and (b) after $NH_3$-plasma treatment.

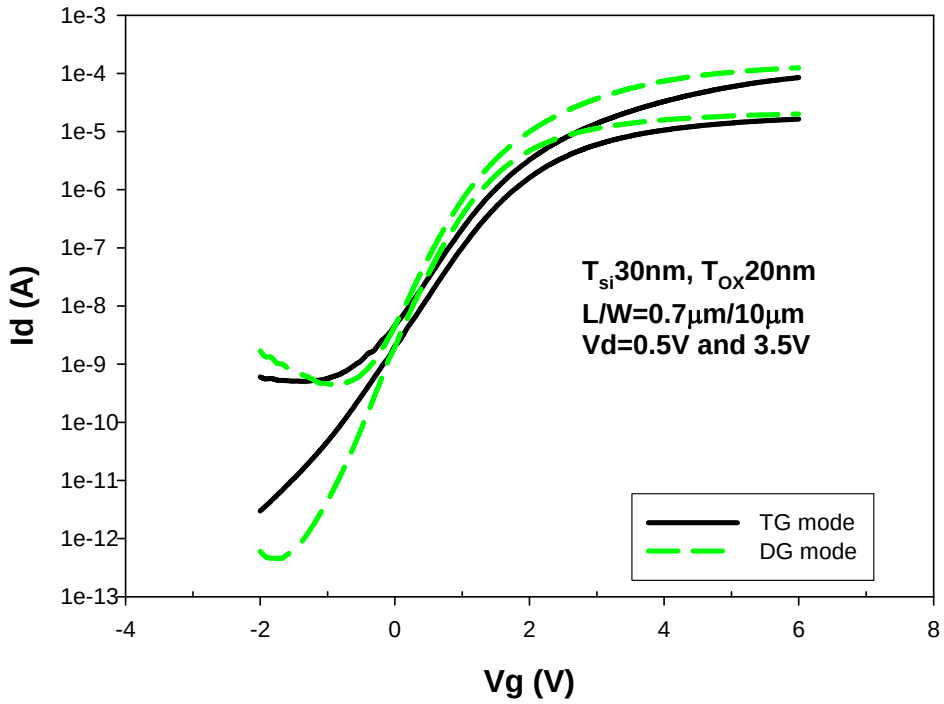



**Fig. 3-2** Transfer characteristics of a short-channel (L=0.7μm) device under TG and DG modes of operation.

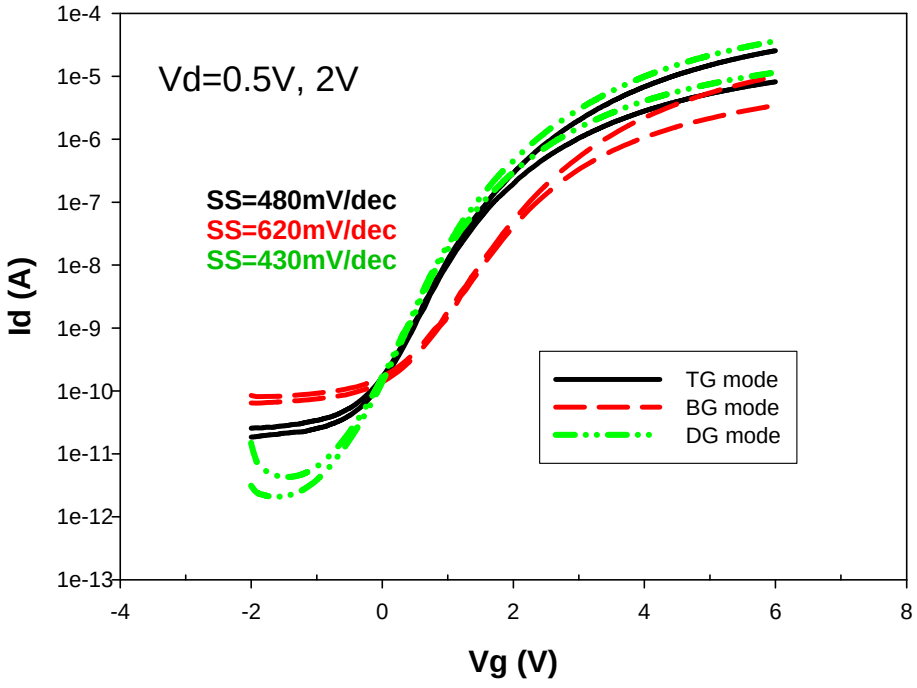
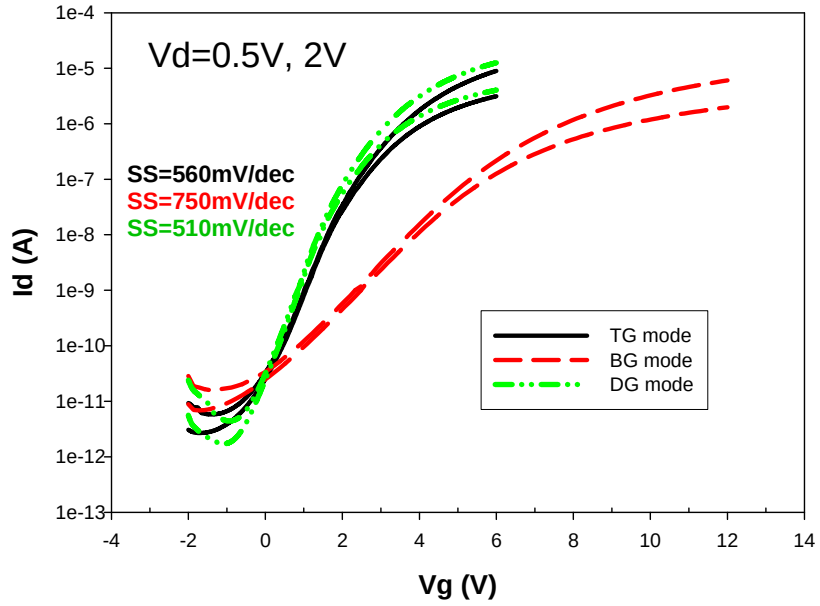
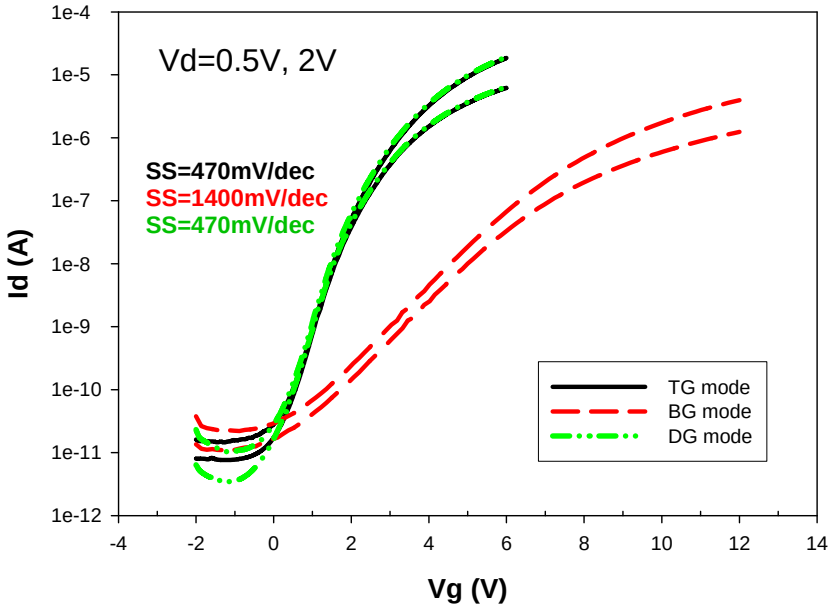



**Fig. 3-3** Transfer characteristics of a DG-TFT under different operation modes. The channel thickness is 50nm. Bottom and top gate oxide are both 20nm.




(a)




(b)

**Fig. 3-4** Transfer characteristics of devices with asymmetric gate oxide and channel thickness of (a) 30nm and (b) 50nm. Bottom and top gate oxide are 50nm and 20nm, respectively.

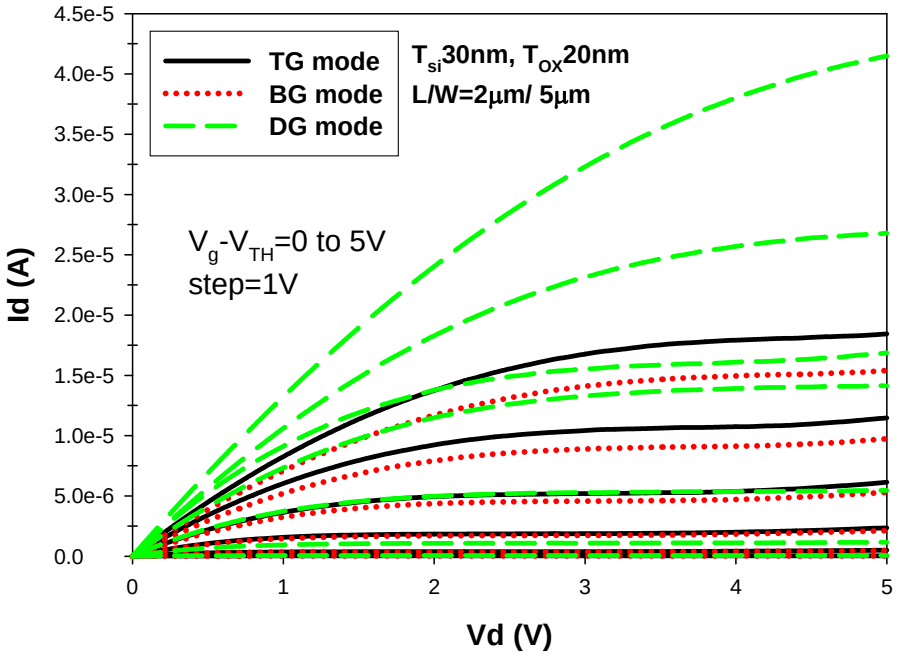



**Fig. 3-5** Output characteristics of a device with symmetric gate oxide of 20nm and channel thickness of 30nm.

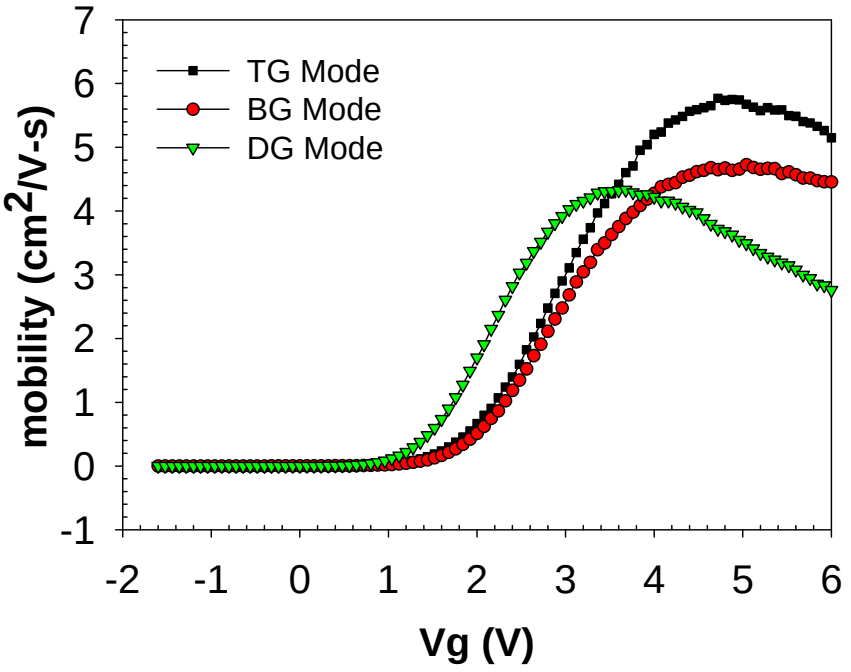
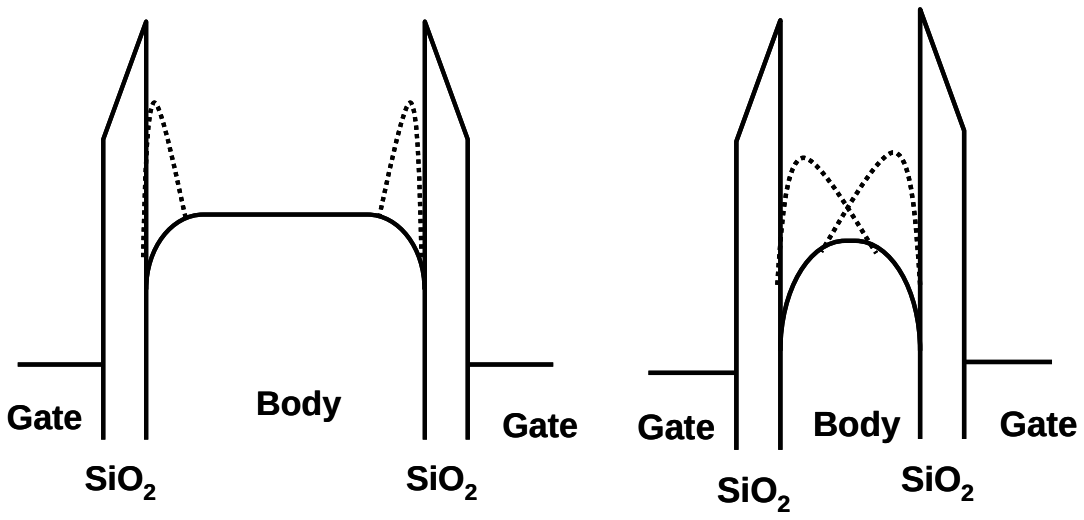



**Fig. 3-6** Mobility of a device under different modes of operation. The device is with symmetric gate oxide of 20nm and channel thickness of 30nm.




(a) (b)

**Fig. 3-7** Energy band diagrams for (a) thick channel body, (b) thin channel body. Dashed lines represent the distribution of the inversion charges.

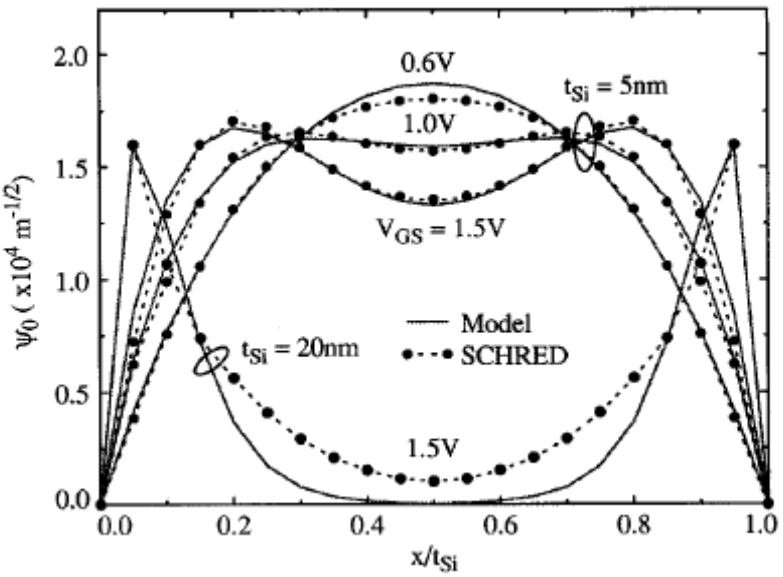



**Fig. 3-8** Simulated electron wave functions in the channel of a DG configuration under different Si channel thickness and bias conditions.[13]

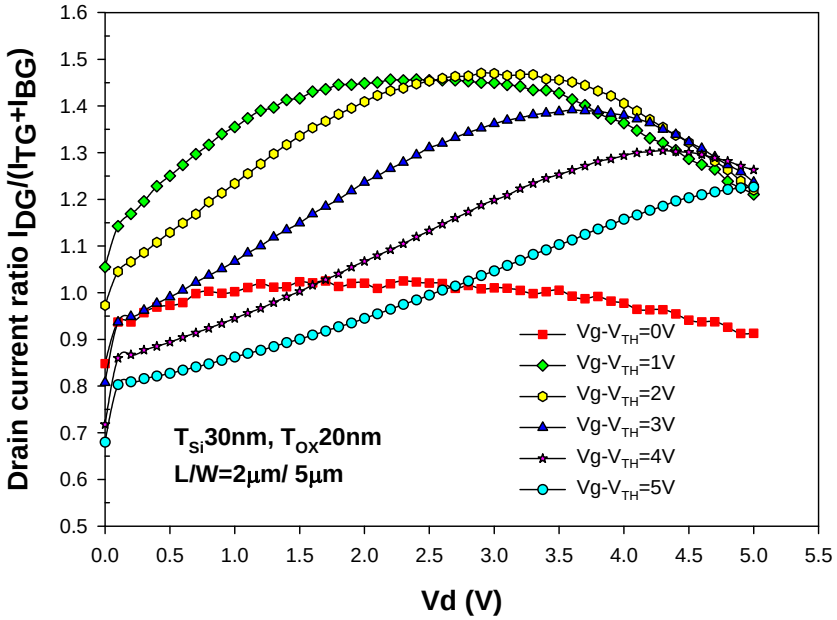
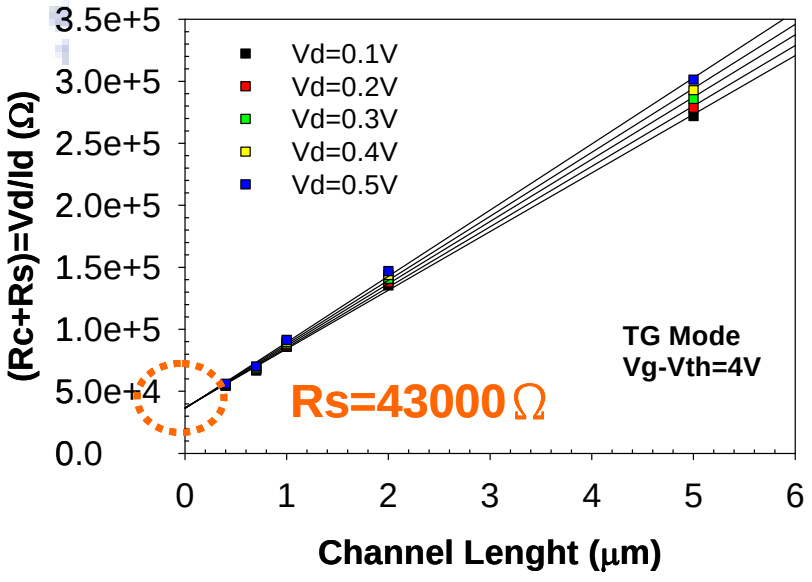
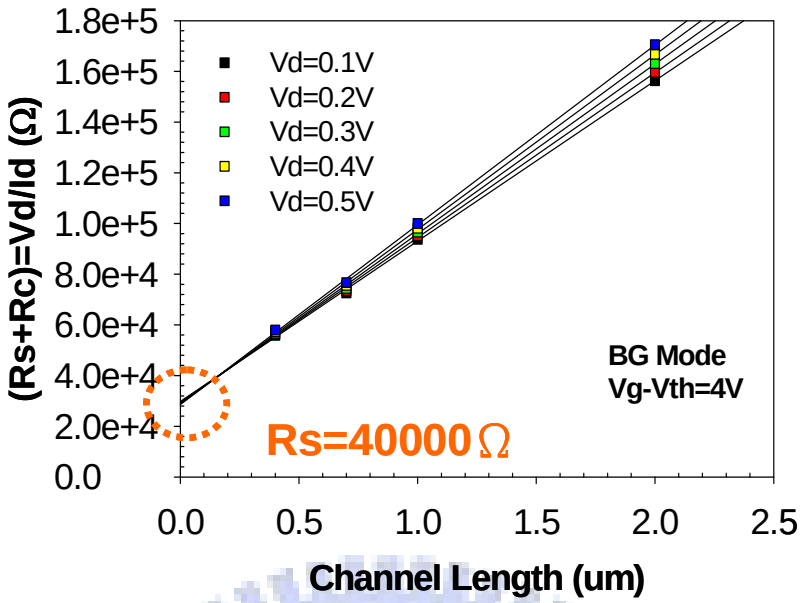


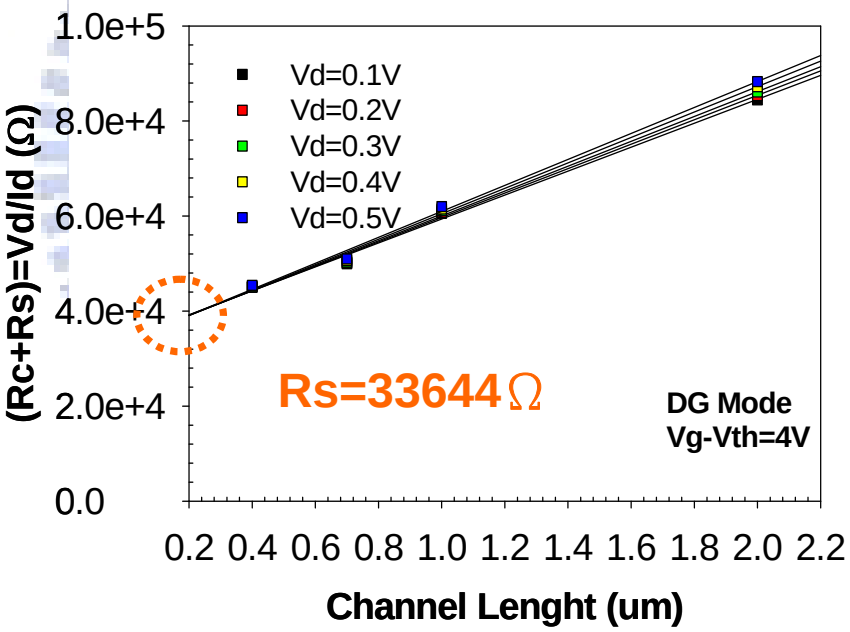

**Fig. 3-9** Drain current ratio for the results shown in Fig. 3-5.




(a)




(b)




(c)

**Fig. 3-10** The series resistance of devices under (a) TG, (b) BG, and (c) DG operation modes. The devices are with symmetric gate oxide of 20nm and channel thickness of 30nm.

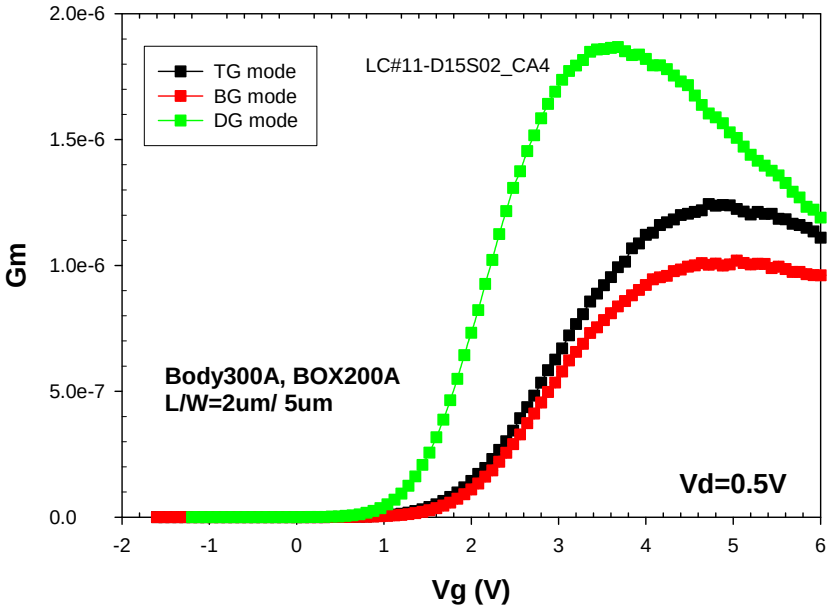
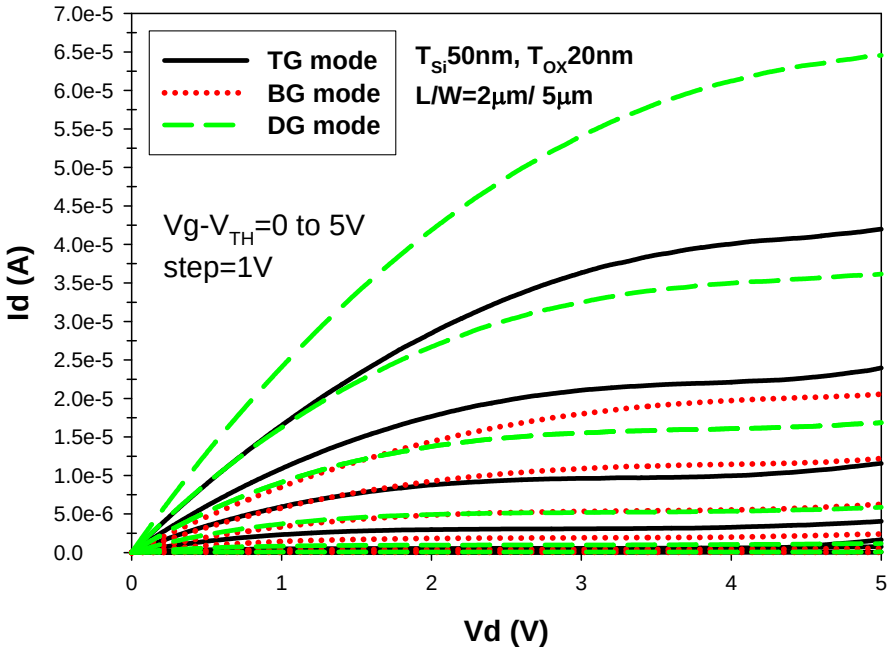
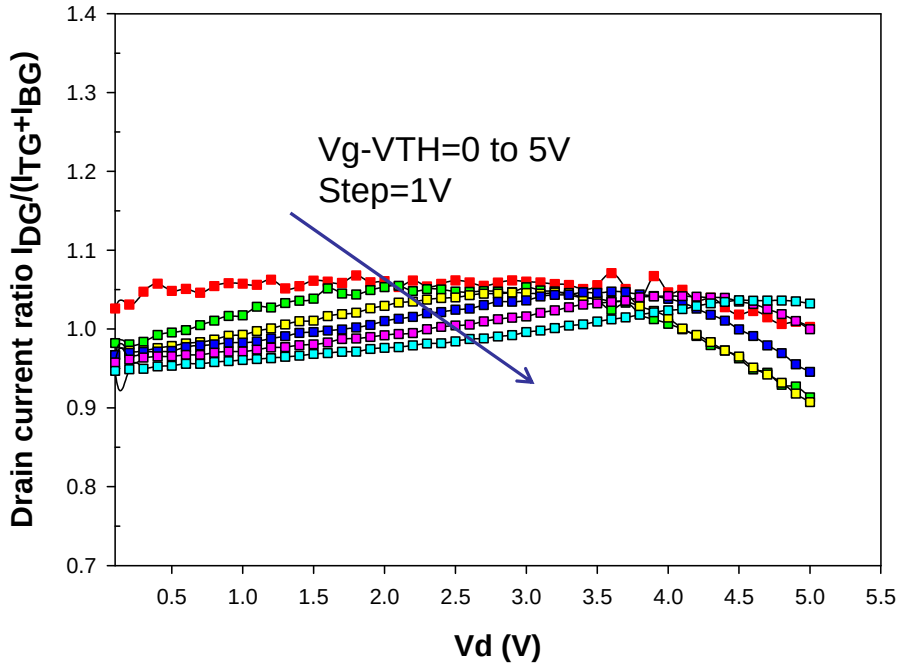



**Fig. 3-11** Transconductance of a device under different operation modes. The device is with symmetric gate oxide of 20nm and channel thickness of 30nm.




(a)




(b)

**Fig. 3-12** (a) Output characteristics of a device with symmetric gate oxide of 20nm and channel thickness of 50nm. (b) The extracted drain current ratio.

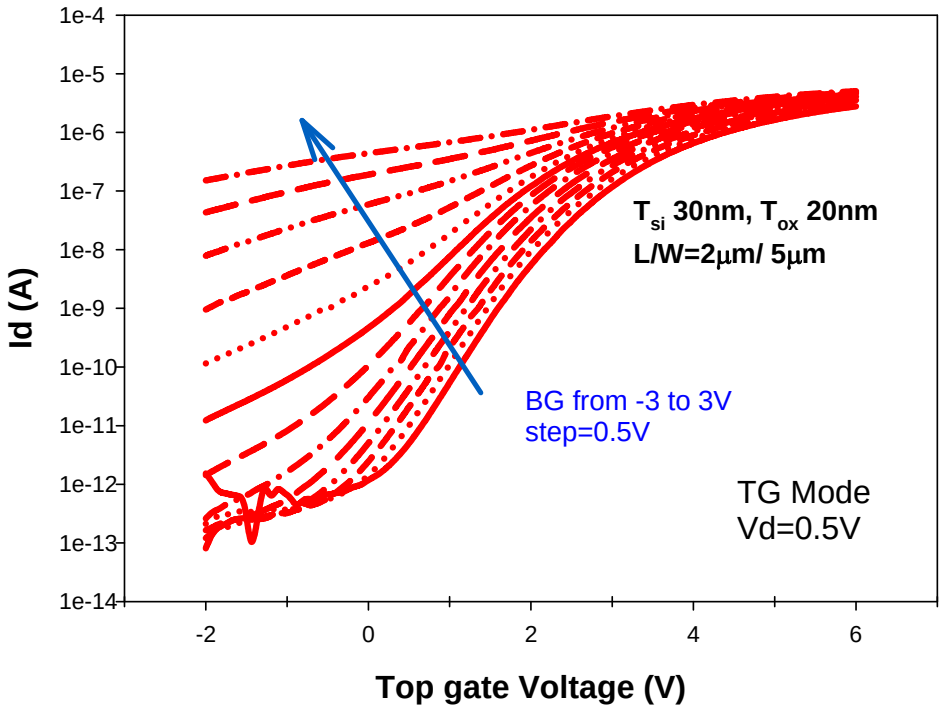



**Fig. 3-13** Modulation of transfer characteristics with BG voltage.

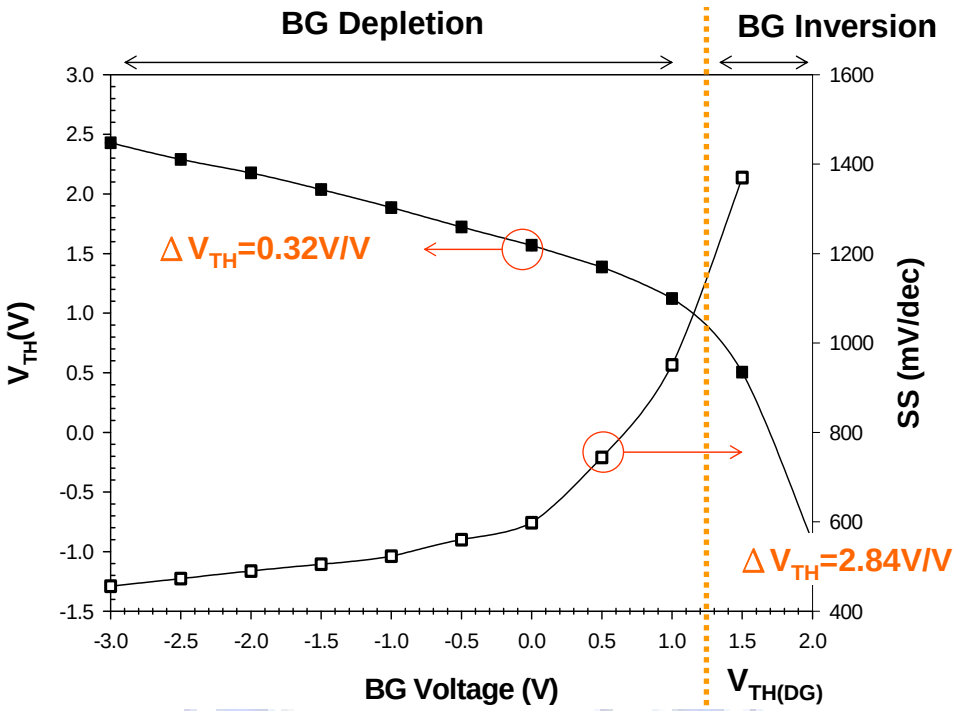



**Fig. 3-14** Modulation of Vth (TG) and SS as a function of BG voltage.

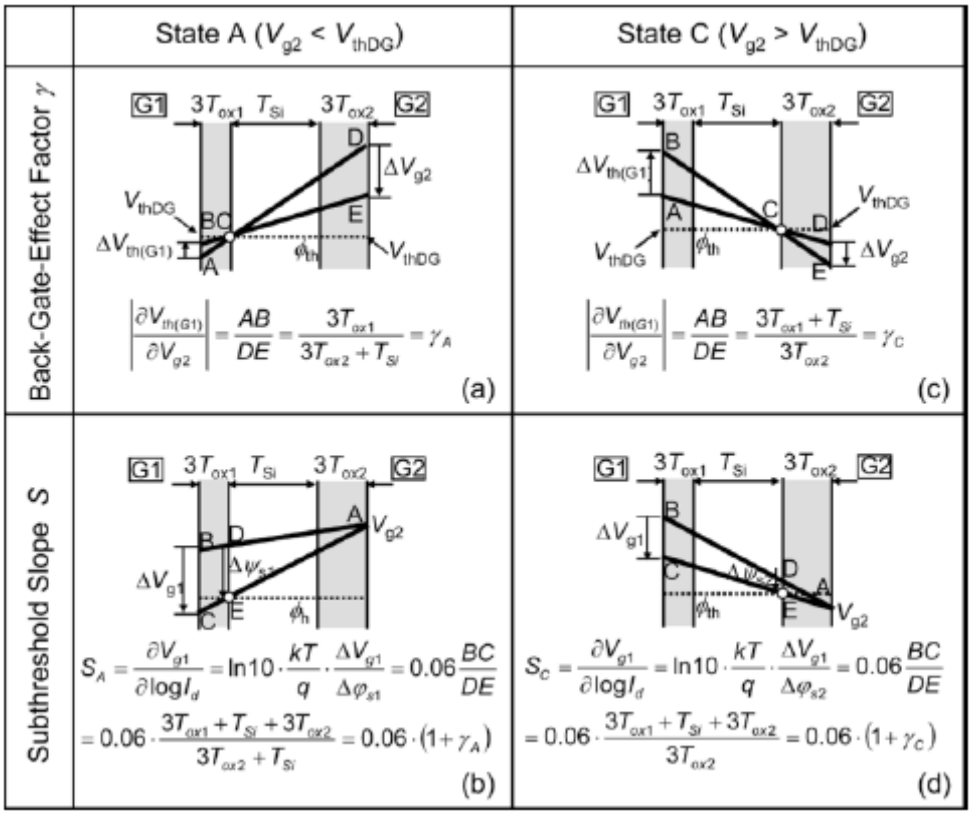



**Fig. 3-15** Schematic illustration of the potential variation with various bias configurations. [15]

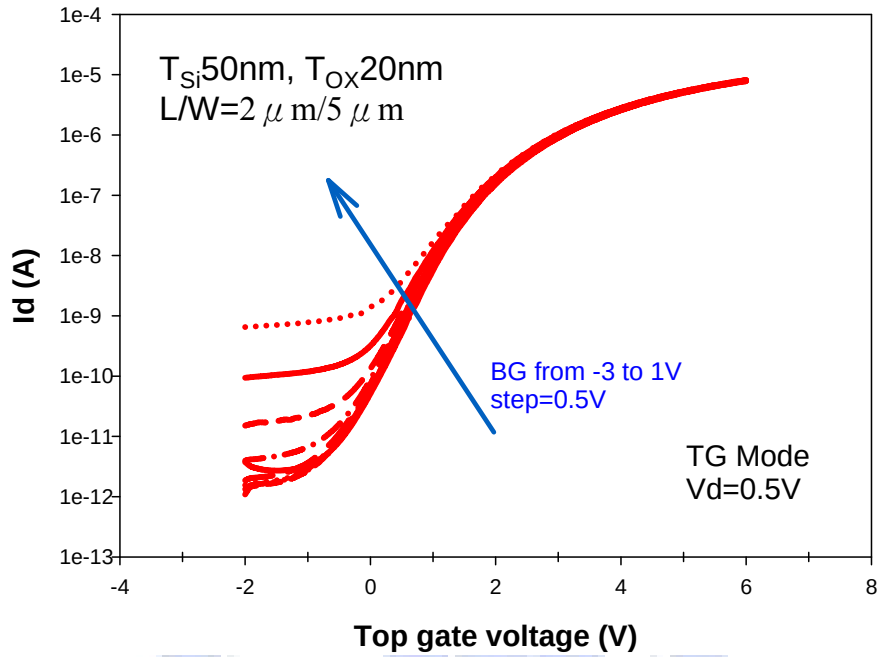



**Fig. 3-16** Modulation of transfer characteristics with BG voltage for a device with symmetrical gate oxide (20nm). The channel thickness is 50nm.

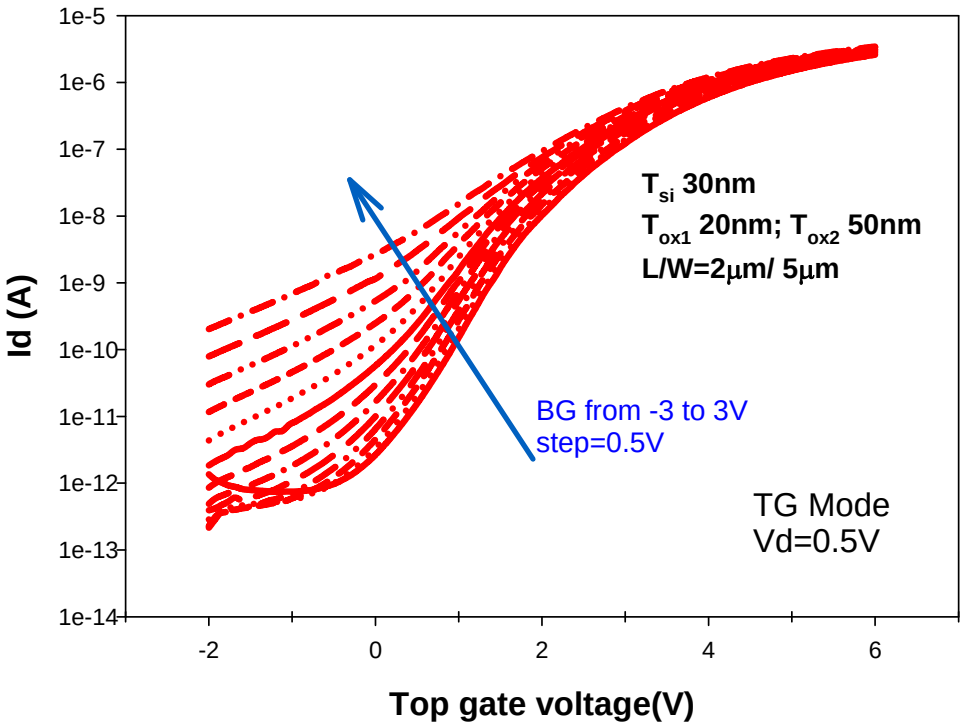



**Fig. 3-17** Modulation of transfer characteristics with BG voltage for a device with asymmetrical gate oxide. The channel thickness is 30nm.

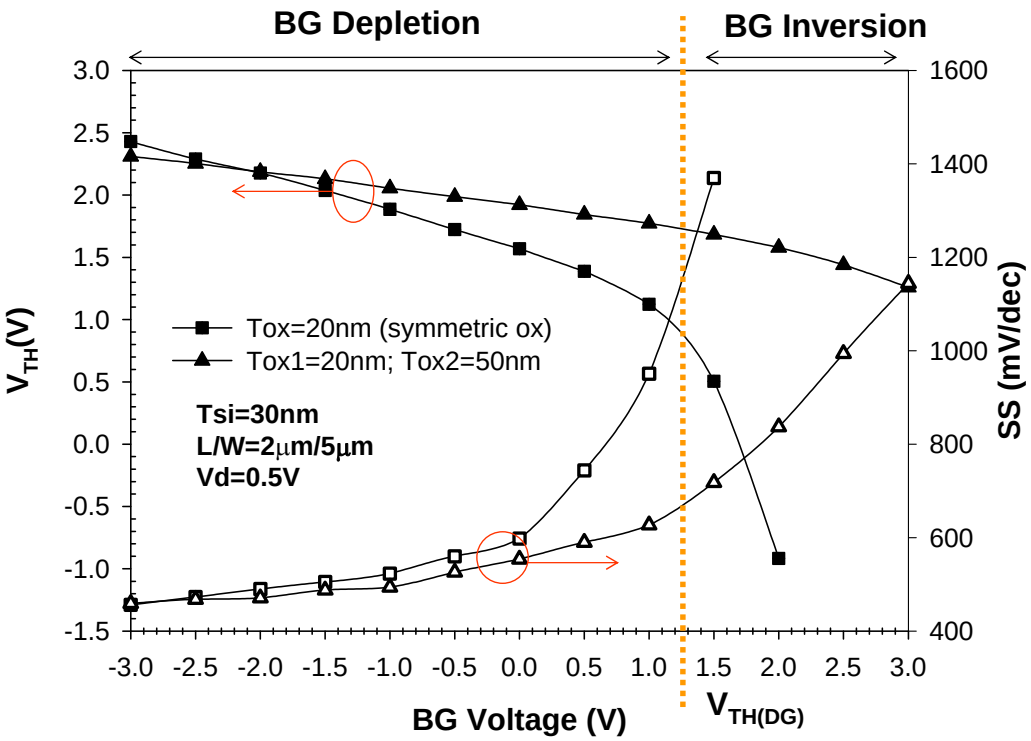



**Fig. 3-18** Modulation of Vth (TG) and SS as a function of BG voltage for devices with symmetrical and asymmetrical gate oxide configurations.

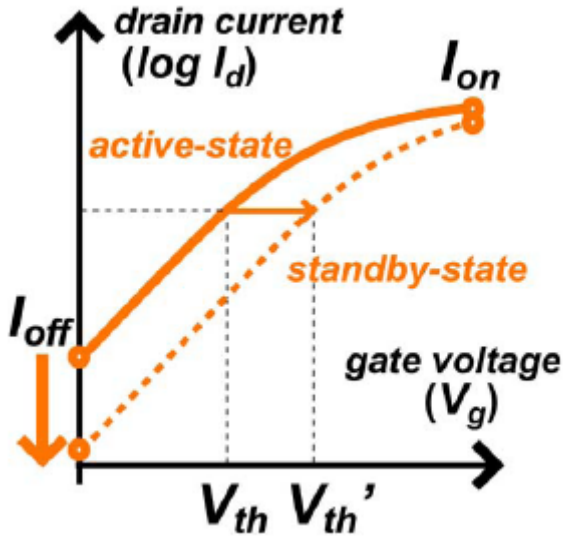



**Fig. 3-19** Schematic Id–Vg curves of a DG modulated by a control gate for active- and standby-state operation [41].

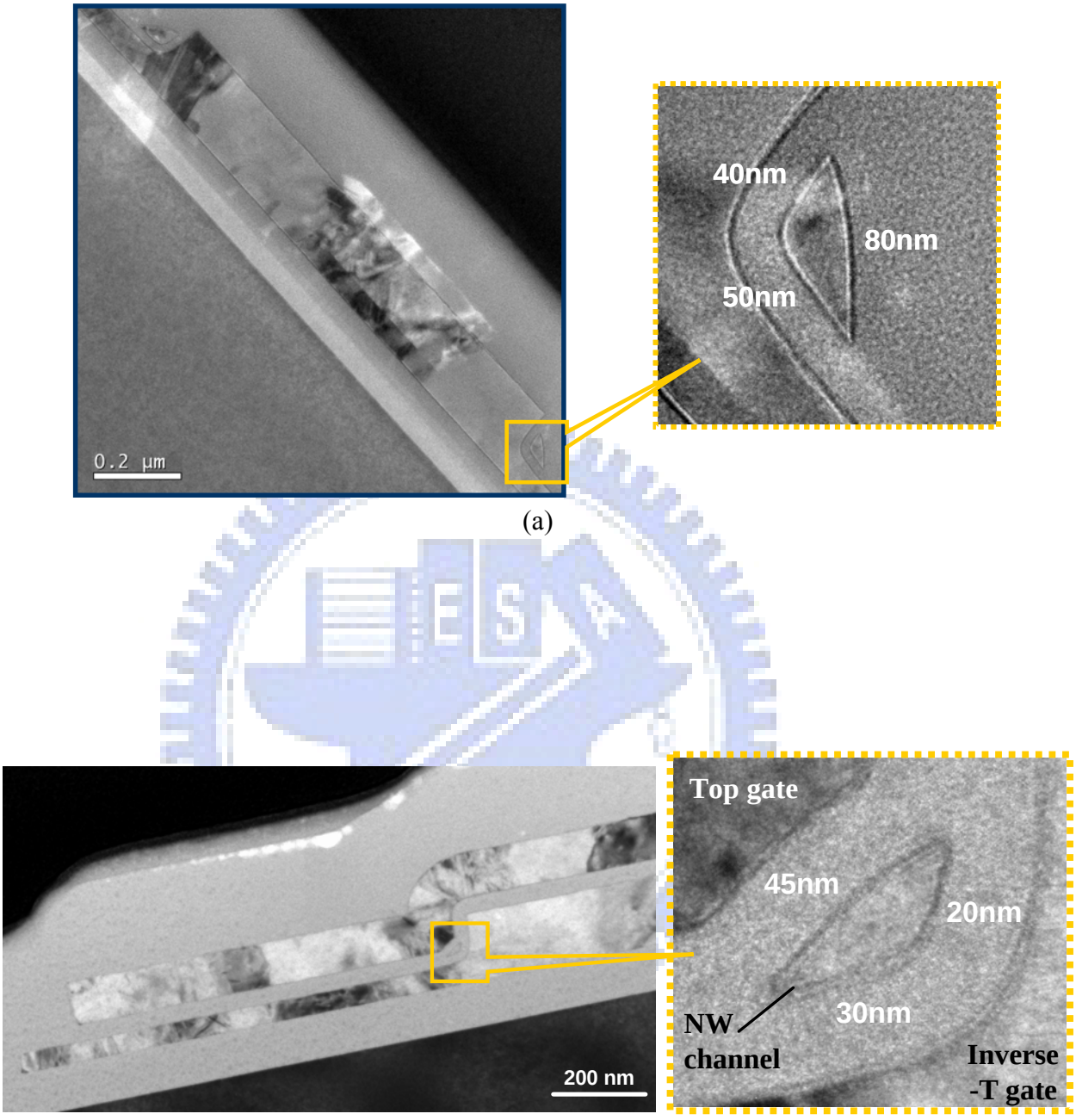
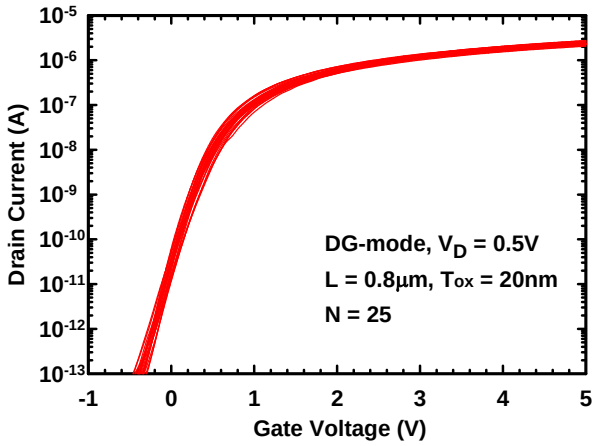
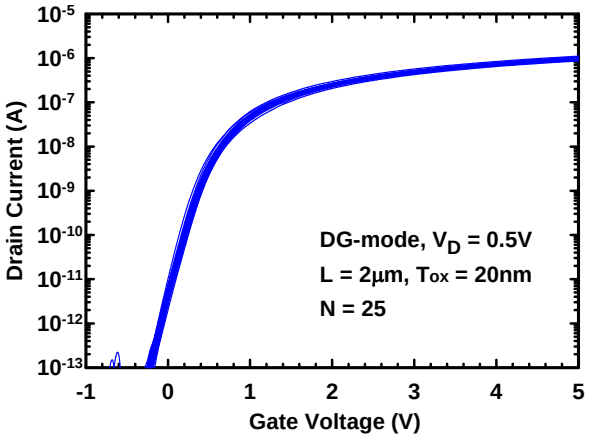


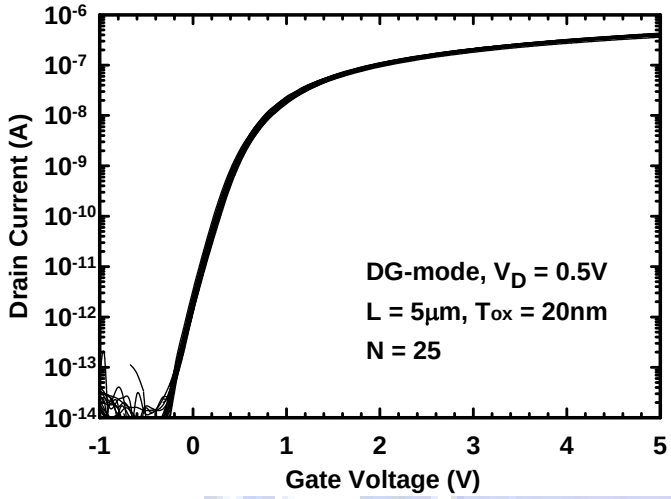

**Fig. 4-1** Cross-sectional TEM views of NW-TFTs: (a) NW-A type and (b) NW-B type.




(a)

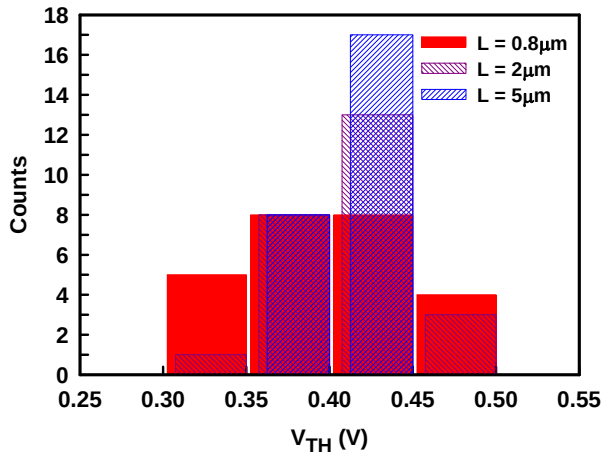



(b)

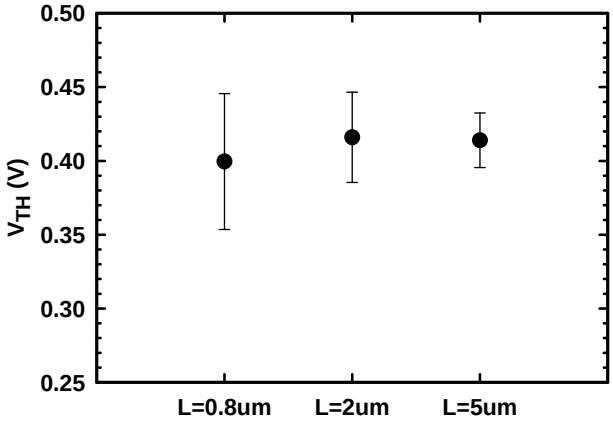



(c)

**Fig. 4-2** Transfer characteristics of NW-A devices with (a) L=0.8μm, (b) L=2μm, and (c) L=5μm. In each split 25 devices were measured.




(a)




(b)

**Fig. 4-3** (a) Distribution, (b) mean-value and standard deviation of $V_{TH}$ of NW-A devices with various channel length.

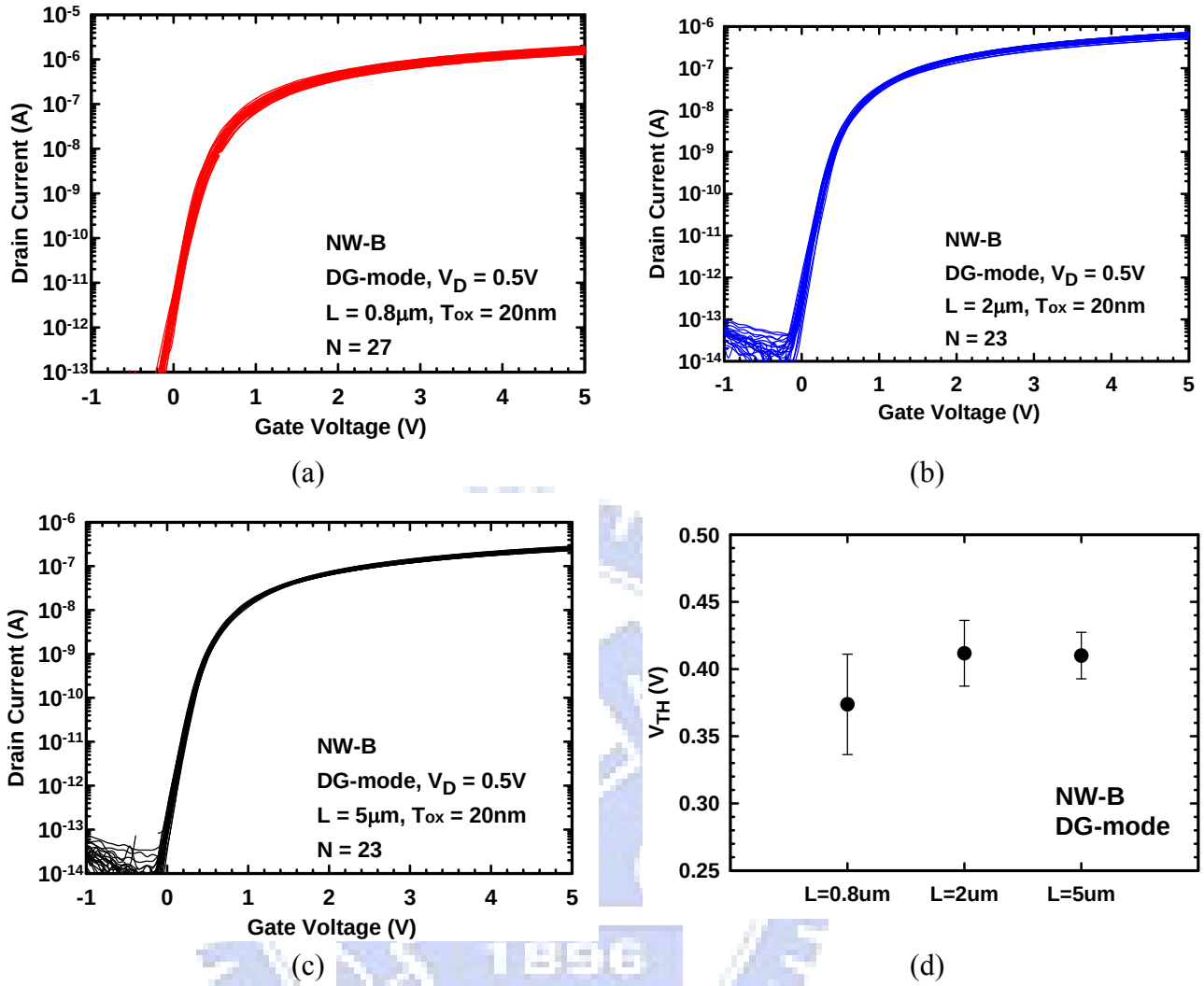



**Fig.4-4** Transfer characteristics of NW-B devices with (a) L=0.8μm, (b) L=2μm, and (c) L=5μm. In each split 25 devices were measured. (d) Mean-value and standard deviation of $V_{TH}$ of the NW-B devices with various channel length.

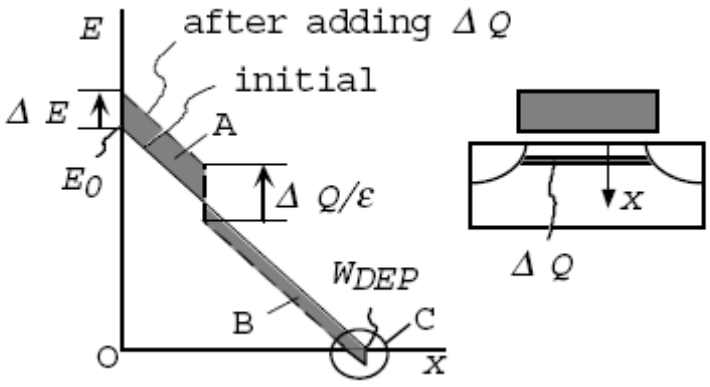
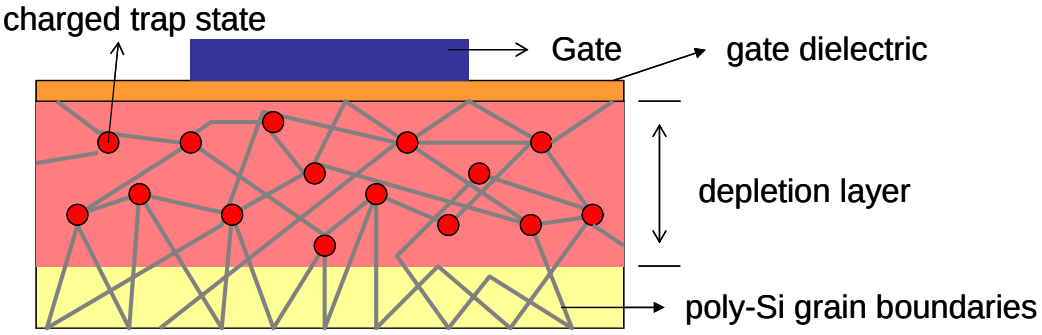


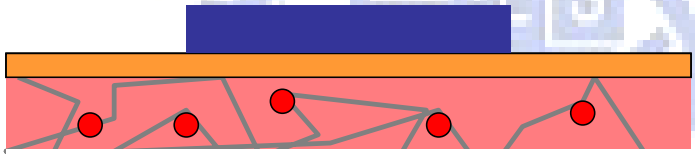

**Fig. 4-5** Schematic illustration of electric field, E, as a function of depth x in the channel region of an MOSFET [31].




$$V_{th} \cong V_{FB} + 2\phi_F + \frac{qN_{Trap}W_d}{C_{OX}}$$

$$\partial V_{th} \propto \partial\sqrt{N_{Trap}}$$

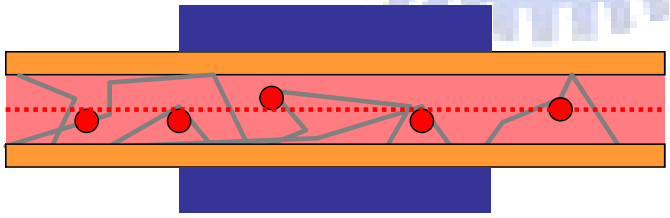
(a) $T_{si} > W_d$



$$V_{th} \cong V_{FB} + 2\phi_F + \frac{qN_{Trap}T_{Si}}{C_{OX}}$$

$$\partial V_{th} \propto T_{Si}\partial\sqrt{N_{Trap}}$$

(b) $T_{si} < W_d$ in SG mode



$$V_{th} \cong V_{FB} + 2\phi_F + \frac{qN_{Trap} \cdot T_{Si}/2}{C_{OX}}$$

$$\partial V_{th} \propto T_{Si}\partial\sqrt{N_{Trap}}$$

(c) $T_{si} < W_d$ in DG mode

**Fig. 4-6** $V_{TH}$ dependence on the poly-Si channel thickness: (a) single-gated devices with partially depleted channel, (b) single-gated devices with fully depleted channel, and (c) double-gated devices with fully depleted channel.

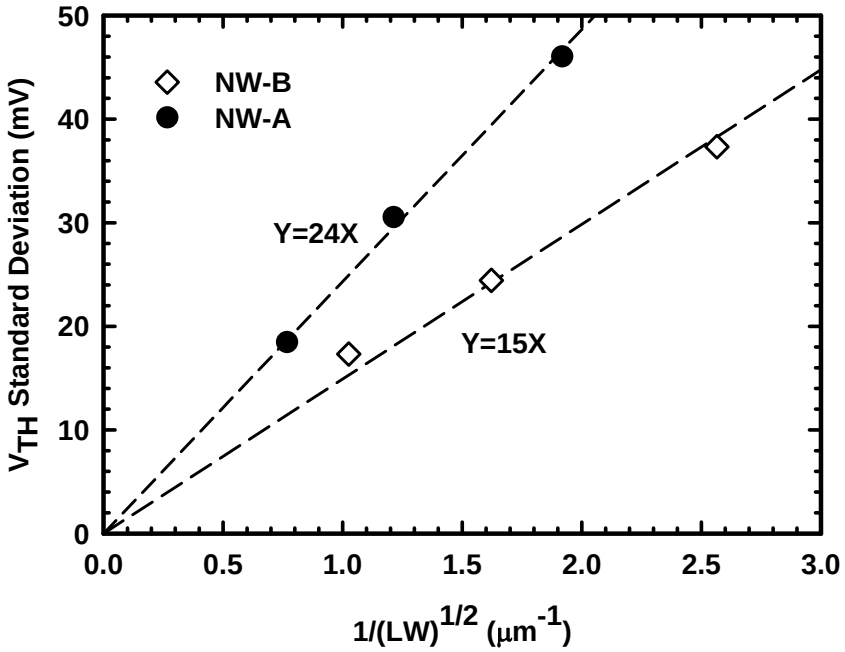



**Fig.4-7** $V_{TH}$ standard deviation of the NW-A and NW-B devices as a function of $\frac{1}{\sqrt{LW}}$.

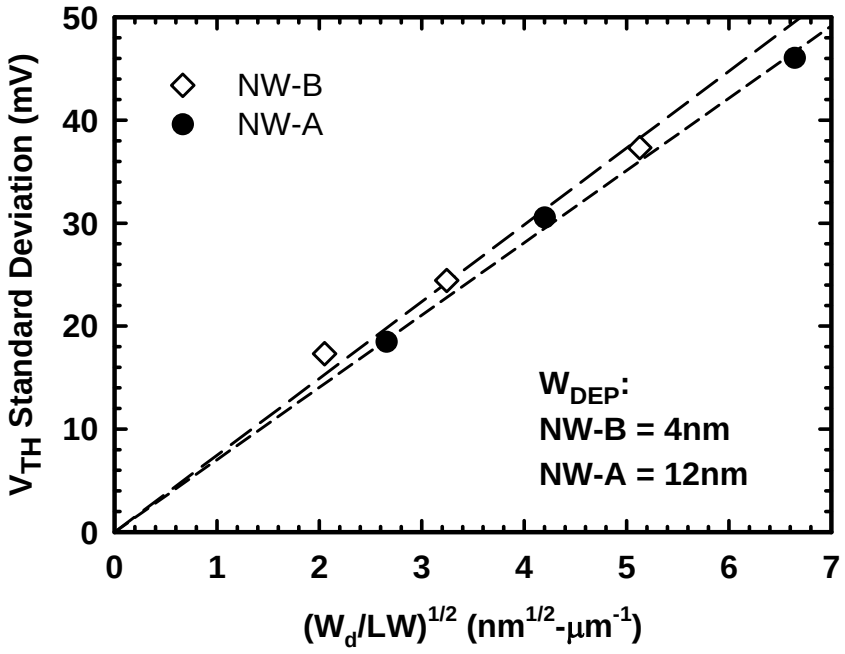
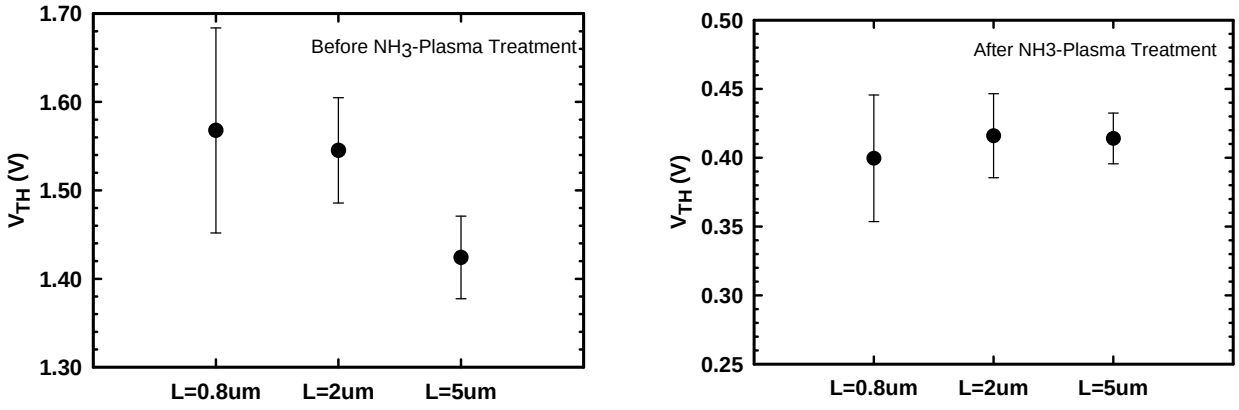
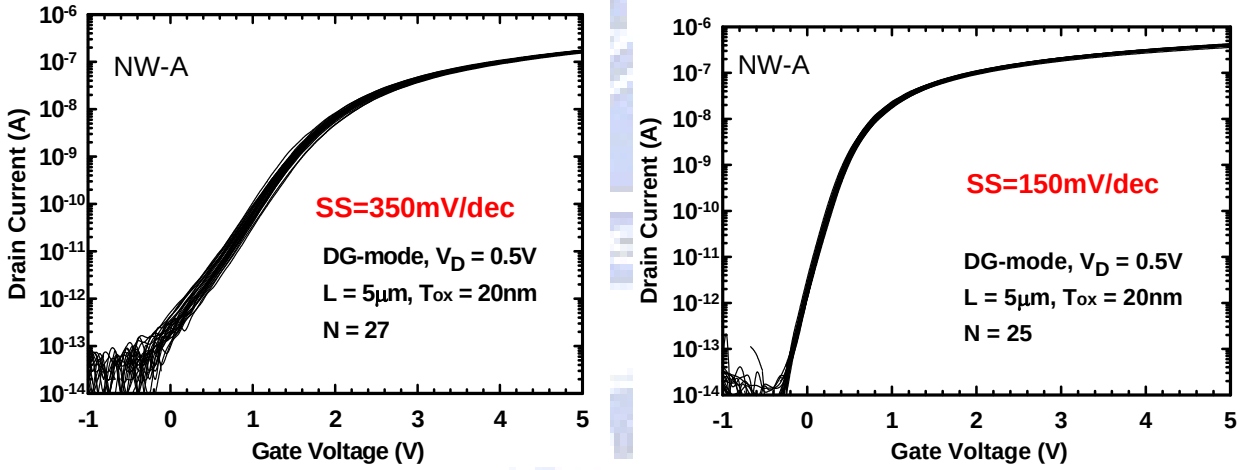



**Fig. 4-8** $V_{TH}$ standard deviation of NW-A and NW-B devices as a function of $\sqrt{\frac{Wd}{LW}}$.




(a) (b)

**Fig. 4-9** Mean value and standard deviation of $V_{TH}$ of NW-A devices (a) before and (b) after $NH_3$-plasma treatment.




(a) (b)

**Fig. 4-10** Transfer curves of NW-A devices (a) before and (b) after $NH_3$-plasma treatment.

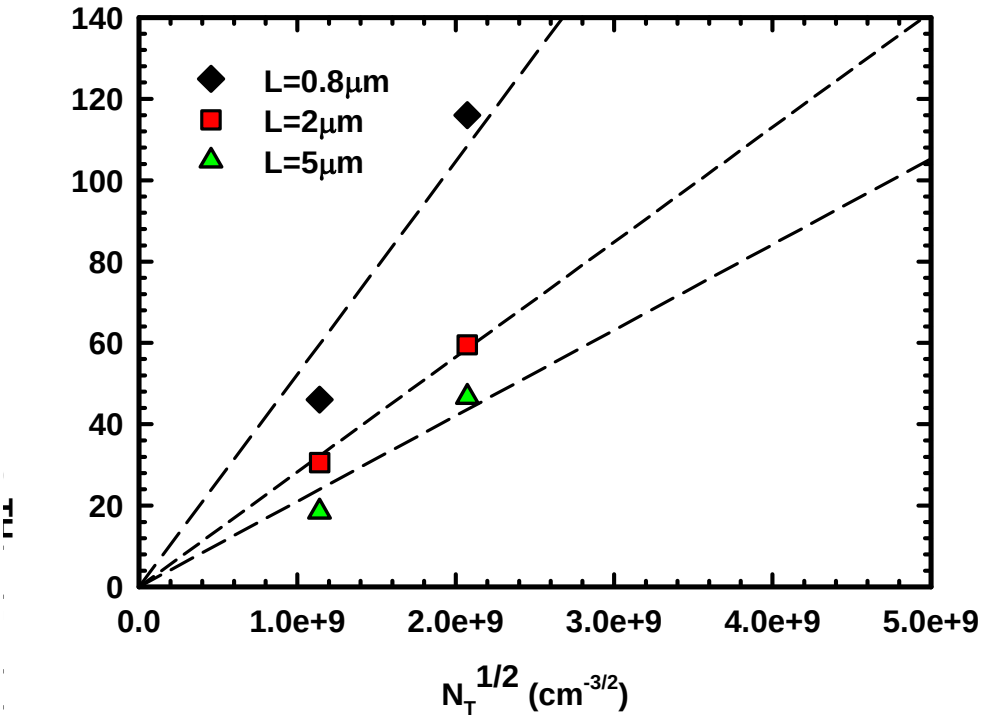



**Fig. 4-11** $V_{TH}$ standard deviation as a function of $\sqrt{N_T}$ .

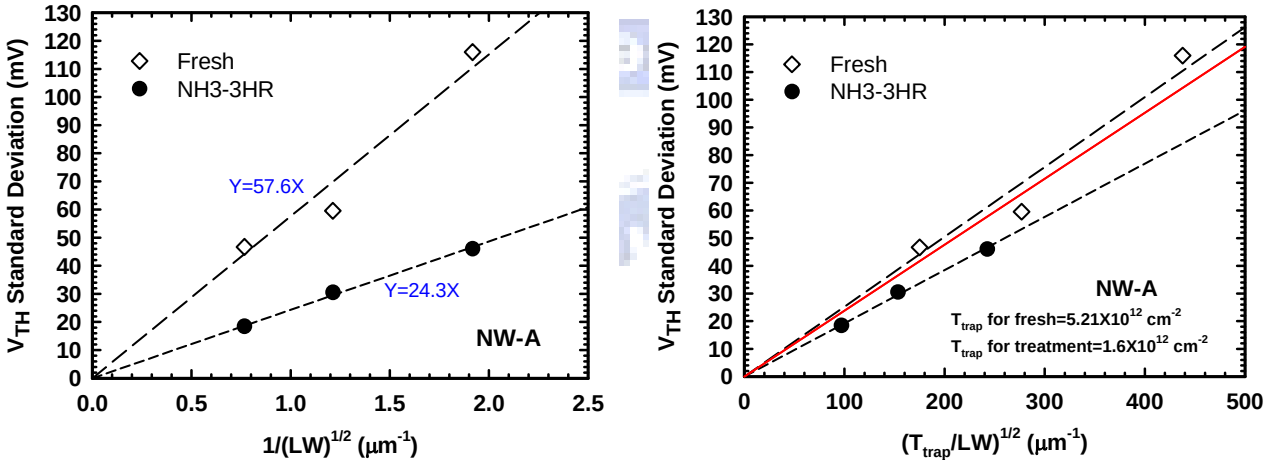



**Fig. 4-12** $V_{TH}$ standard deviation of NW-A devices before and after $NH_3$-plasma treatment.

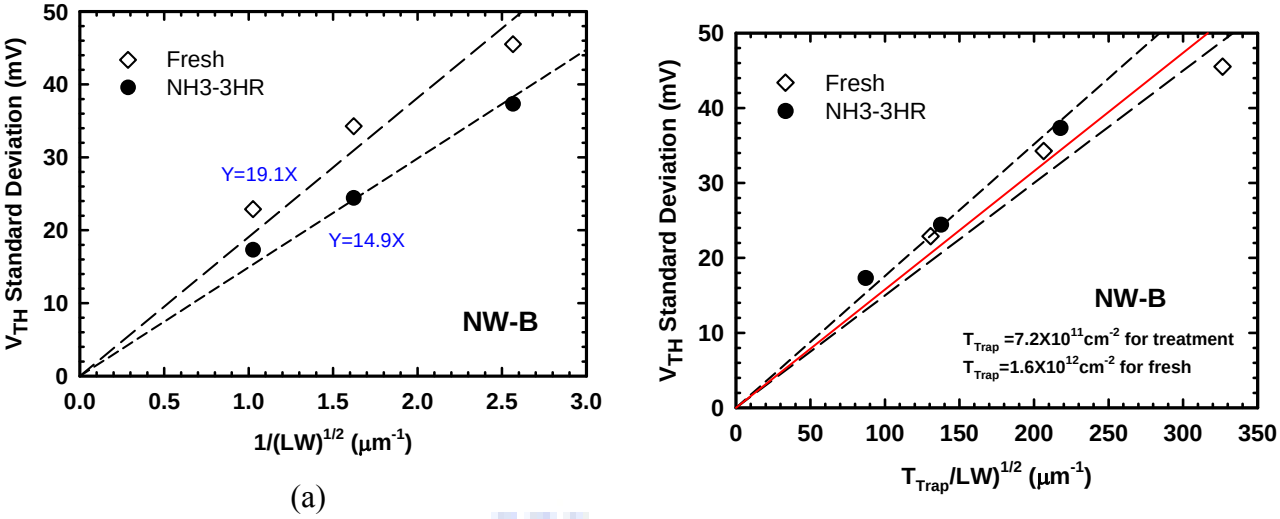



**Fig. 4-13** $V_{TH}$ standard deviation of NW-B devices before and after $NH_3$-plasma treatment.

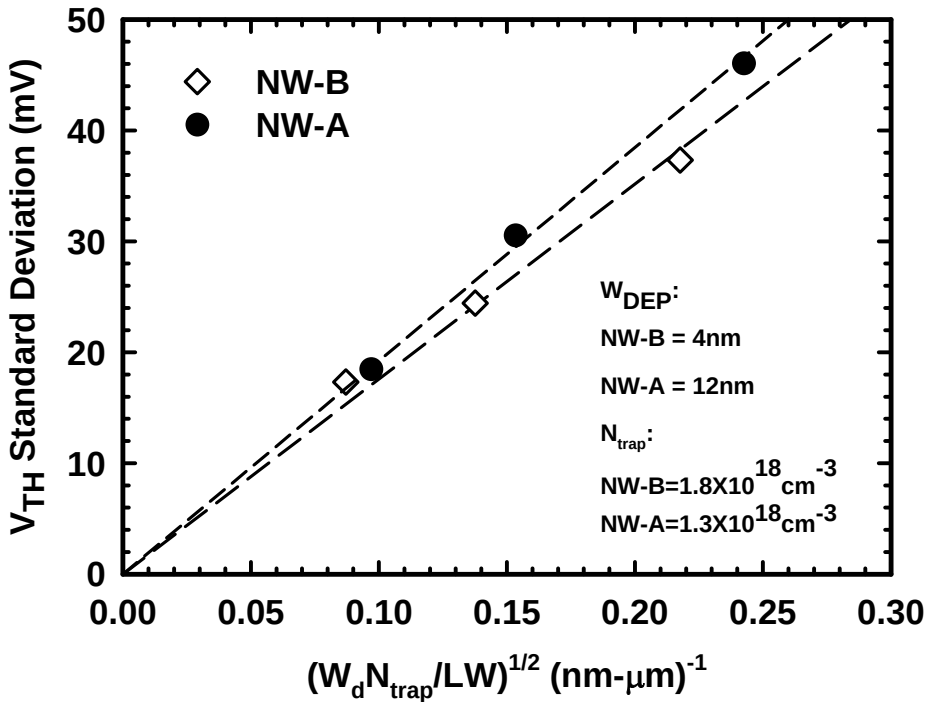



**Fig. 4-14** $V_{TH}$ standard deviation of NW-A and NW-B devices as a function of. $\sqrt{\frac{W_d N_T}{LW}}$ .

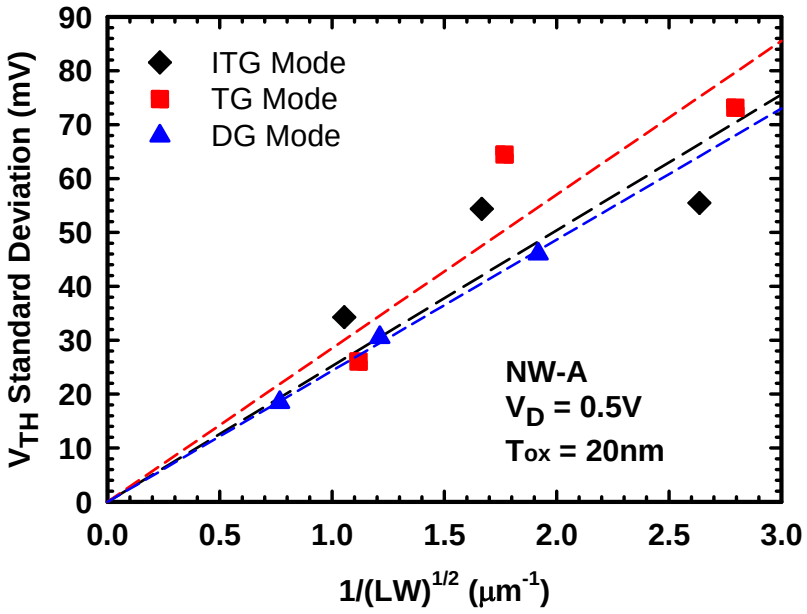
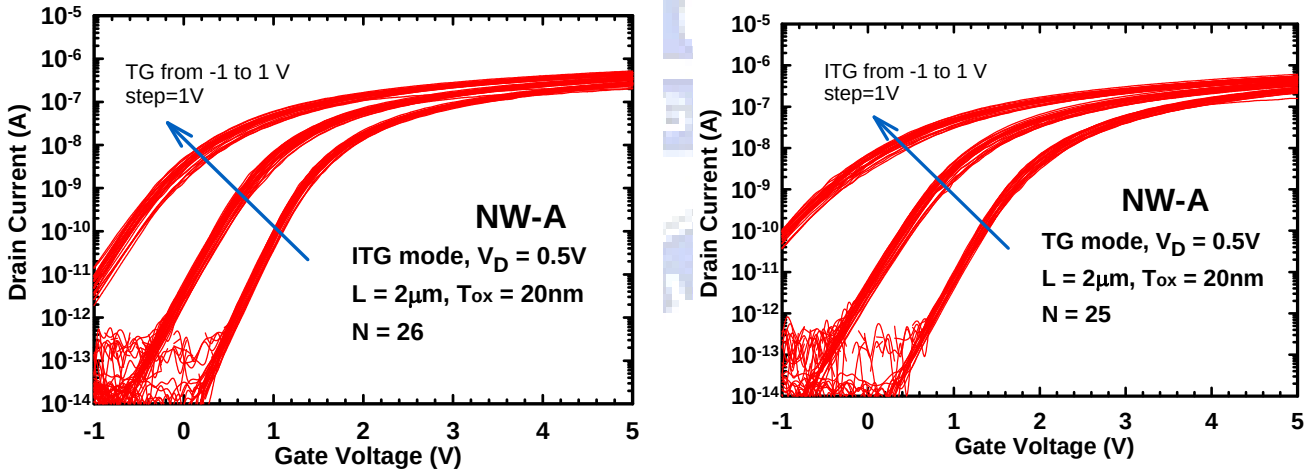



**Fig. 4-15** $V_{TH}$ standard deviation of NW-A devices under various operation modes as a function of $\sqrt{\frac{1}{LW}}$




(a) (b)

**Fig. 4-16** Transfer curves of NW-A devices in (a) ITG mode; (b) TG mode. In each figure 25 devices were measured. Three different voltages (-1, 0, and 1V) were applied to the control gate to modulate the transfer characteristics.

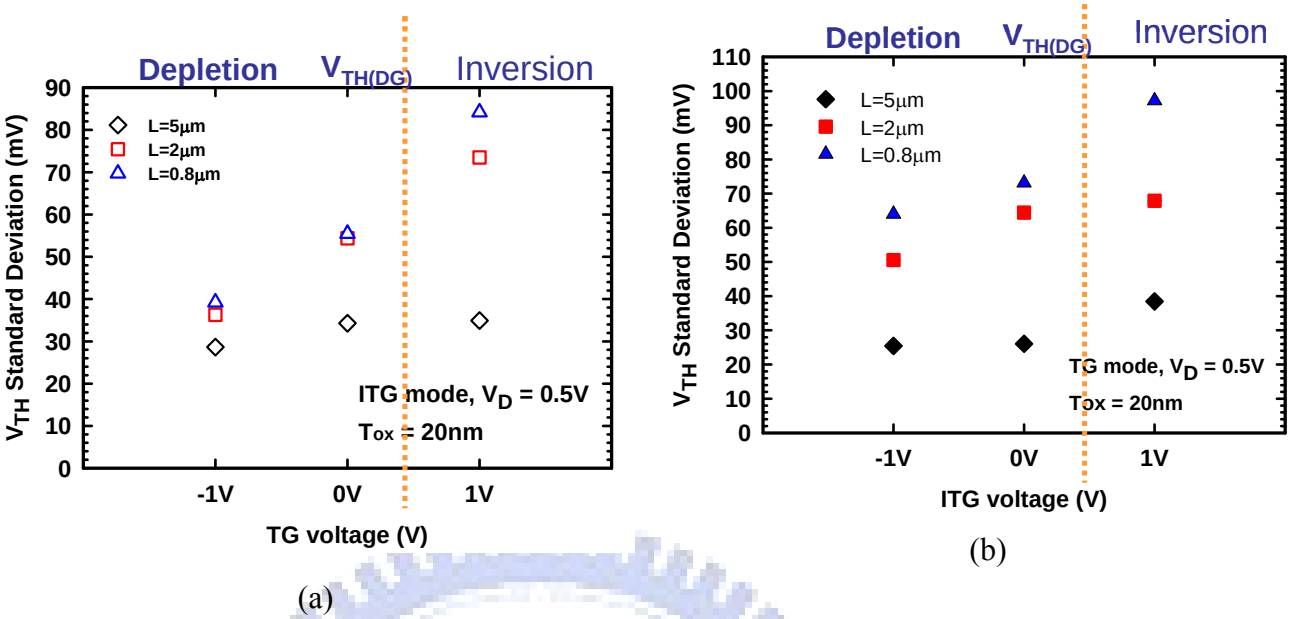



**Fig. 4-17** $V_{TH}$ standard deviation in (a) ITG mode; (b) TG mode.

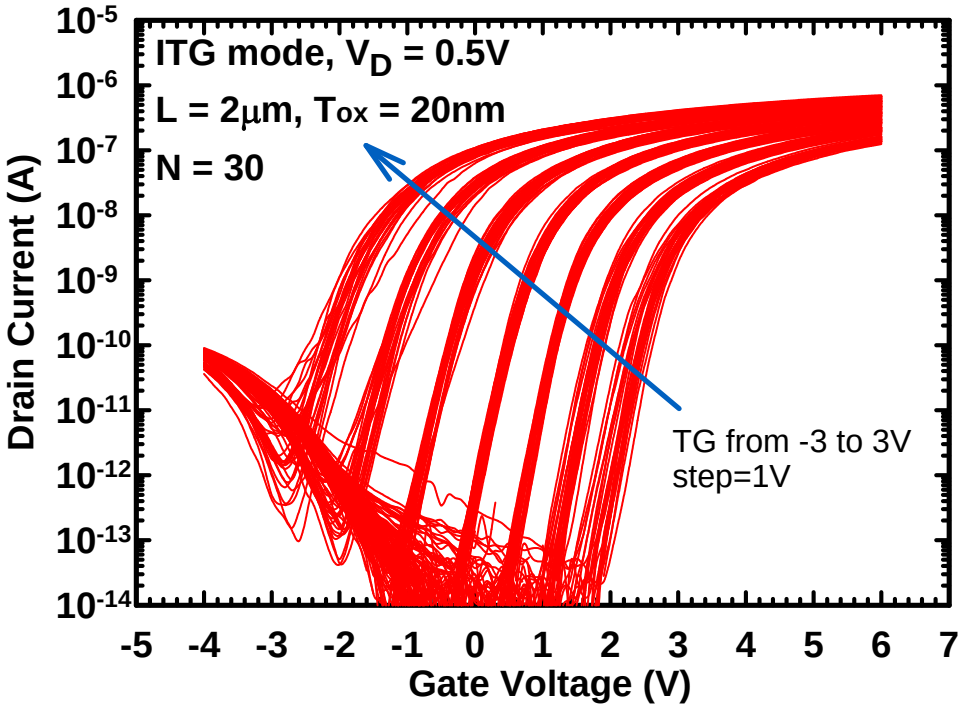



**Fig. 4-18** Distribution of transfer curves in ITG mode.

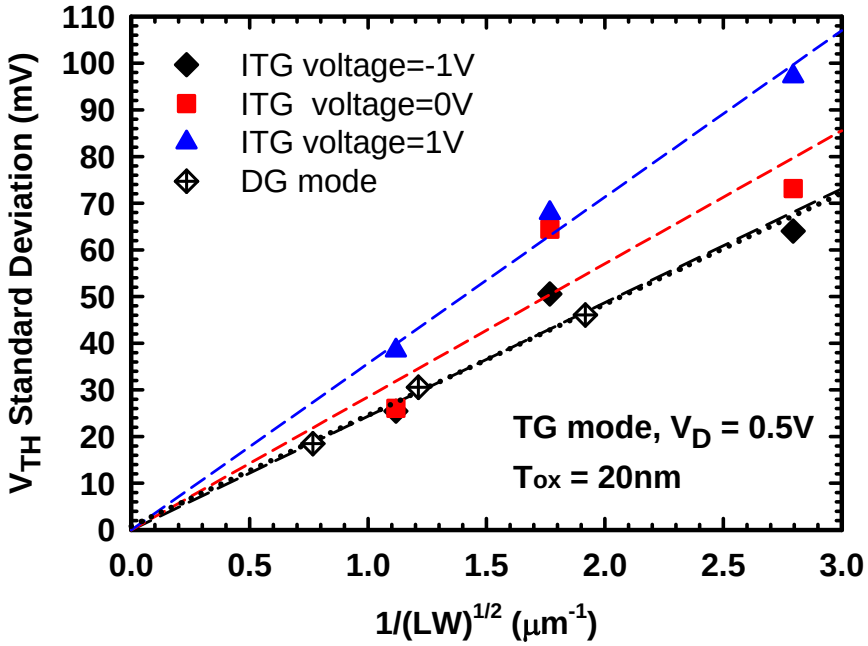



**Figure 4-19** Standard deviation of $V_{TH}$ for TG and DG modes.

**Table 3-1**. Subthreshold slope for DG-TFTs (at $V_D$=0.5V) under various operation modes.

| | TG mode | BG mode | DG mode |
|---|---|---|---|
| DG1<br>$T_{si}$=30nm<br>$T_{ox,top}$=20nm<br>$T_{ox,\ bottom}$=20nm | 554 (mV/dec) | 690 (mV/dec) | 422 (mV/dec) |
| DG2<br>$T_{si}$=50nm<br>$T_{ox,top}$=20nm<br>$T_{ox,\ bottom}$=20nm | 480 (mV/dec) | 620 (mV/dec) | 430 (mV/dec) |
| DG3<br>$T_{si}$=30nm<br>$T_{ox,top}$=20nm<br>$T_{ox,\ bottom}$=50nm | 560 (mV/dec) | 750 (mV/dec) | 510 (mV/dec) |
| DG4<br>$T_{si}$=50nm<br>$T_{ox,top}$=20nm<br>$T_{ox,\ bottom}$=50nm | 470 (mV/dec) | 1400 (mV/dec) | 470 (mV/dec) |

**Table 4-1** The $N_{Trap}$ extracted from the SS and effective trap states concentration.

| | | SS (mV/dec) | $T_{Trap}$ ($cm^{-2}$) | $W_{dm}$ (nm) | $N_{Trap}$ ($cm^{-3}$) |
|---|---|---|---|---|---|
| NW-A | Before treatment | 350 | $5.2\times10^{12}$ | 12 | $4.3\times10^{18}$ |
| | After treatment | 150 | $1.6\times10^{12}$ | 12 | $1.3\times10^{18}$ |
| NW-B | Before treatment | 150 | $1.6\times10^{12}$ | 4 | $4.1\times10^{18}$ |
| | After treatment | 100 | $7.2\times10^{11}$ | 4 | $1.8\times10^{18}$ |

**Table 4-2** The comparison of the trap states density ratio extracted from SS and Figs. 4-12 and 4-13

| | $\sqrt{\frac{N_{T(before)}}{N_{T(after)}}}$ | $\frac{slope_{(before)}}{slope_{(after)}}$ |
|---|---|---|
| NW-A | 1.8 | $\frac{57.6}{24.3}=2.37$ |
| NW-B | 1.5 | $\frac{19.1}{14.9}=1.28$ |

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