

國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

SONOS 記憶體因寫入電子之隨機特性造

成臨界電壓擾動之模擬分析



**TCAD Simulation of Random Program Charge
Induced Threshold Voltage Fluctuations in
SONOS Device**

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摘要

SONOS 記憶體是以氮化矽(Si_3N_4)作為電荷陷捕層(Charge Trapping Layer)來取代傳統以多晶矽來儲存電荷的浮閘極元件。由於氮化矽是以單顆離散的陷捕(Trap)來儲存電荷，因此會造成非均勻的通道位能，進而導致臨界電壓受到儲存電荷排列方式的影響。換而言之，當通道中電子導通的路徑不同時，便會造成臨界電壓擾動的現象。在此篇論文中，採用三維飄移擴散模型(Drift-Diffusion)，並以 ISE 為工具對 SONOS 元件中因儲存於氮化矽內的寫入電子隨機排列所造成臨界電壓擾動的現象進行研究。

首先模擬在不同的元件參數下(通道長度、通道寬度、寫入電壓窗(Program Window)以及頂層與底層的氧化層厚度)對於臨界電壓擾動的影響。在每項參數中，均以一百個具有不同排列之寫入電子的元件來進行統計 V_T 的變化量，以對每項參數進行分析。

模擬的結果顯示，當元件微縮以及寫入電子的數量變多時會讓 V_T 的分佈曲線變寬，此外，底層氧化層的厚度變薄會讓 V_T 的擾動變的更嚴重，其原因在論文中詳細的論述。根據模擬結果，利用 high-k 材料來取代頂層氧化層能有效的改善此現象。最後為了更接近記憶體元件實際的情形，將隨機摻雜的因素也加

入模擬中，可以預見的，這項因素的加入會讓 V_T 的擾動變的更加嚴重。雖然在通道加入低摻雜的磊晶層(epi-taxial layer)可抑制隨機摻雜造成的問題，但仍無法有效降低寫入狀態的 V_T 擾動，由此可知隨機寫入電子是造成 V_T 擾動最主要的因素。



TCAD Simulation of Random Program Charge Induced Threshold Voltage Fluctuations in SONOS Device

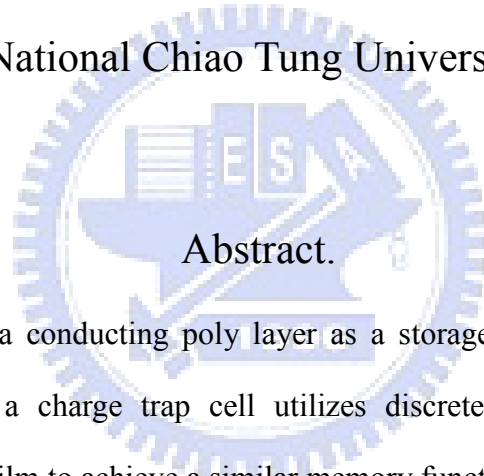
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Abstract.

Instead of using a conducting poly layer as a storage node in a conventional floating gate device, a charge trap cell utilizes discrete trapping centers of an appropriate dielectric film to achieve a similar memory function. In such structure, the channel potential becomes inhomogeneous due to the discreteness of the storage charges and thus the threshold voltage (V_T) will strongly depend on how an inversion percolation path from source to drain is formed in the channel. In this work, SONOS devices with randomly distributed storage charges in a nitride layer are used and the induced V_T fluctuations are then emulated by using a three-dimensional drift-diffusion simulator (ISE).

In the beginning, the effects of various parameters including channel length, channel width, program window, and both top and bottom oxide thicknesses on the V_T fluctuation are studied. For each case, samples of 100 microscopically different

programmed cells are used. The statistics variation of V_T are then collected and analyzed with respect to each variable. Basically, more programmed charges or the shrinkage of device dimensions will worsen the V_T distribution. Besides, the bottom oxide shows more pronounced effect than the top oxide and reasons will be given in this thesis. Finally, to further approach the real situations of memory cells, the effect of random charges with random dopants are also investigated. As expected, the fluctuation of cells gets even worse. Adopting an epi-taxial layer with a lightly doped concentration on the Si surface is useful for suppressing the random dopant effect. But the program state threshold voltage fluctuations can not be improved significantly. Thus, the random charge effect is the main source induced the dispersion of V_T .



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“海上升明月，天涯共此時”，兩年碩士生涯的粹練與同學們的同甘共苦點點滴滴盡涵於薄紙。

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元元是 411 的開心果，他實在傾國傾城(以上不代表本作者立場)，也為我們帶來了歡樂動力；超愛健身的熊勛廷，也是愛搞笑的成員之一，他的興趣就是在別人打電動時在旁助威吶喊(其實都在鬼叫)；他們兩人組成了搞笑二人組，彼此間互相嘻笑怒罵，度過了兩年甘苦的學生生涯。子華則是我大學時代就認識的用功魔人，他學習認真的態度實在令人激賞。和我們同實驗室的莊紹勳菁英研究軍團；重義氣的小郭、很呆又很聰明的謝易叡、愛煮咖啡的 zeky、機車的曾有良，還有一堆可愛的學弟妹們都是我們的好夥伴。這兩年來如果沒有你們，411 必定失色不少。

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Chapter 1

Introduction

The basic operating principle of nonvolatile memory devices is the storage of charges in a material above a MOSFET as depicted in Fig. 1.1. Insulators to prevent the escape of charges usually surround this storage node. If these charges can be put or removed by electrical methods, such as positive Fowler-Nordheim (+FN) (Fig. 1.2 (a)) and negative Fowler-Nordheim (-FN) injections (Fig. 1.2 (b)), the threshold voltage (V_T) of the transistor can be modified to switch between two distinct values, and these devices are named as Electrically Erasable Programmable Read-Only Memory (EEPROM). However, as the number of measured cells is increased, the drain current-gate voltage (I_D - V_G) curve will disperse and the V_G under a same read current will spread accordingly. The two distinct values of a device then become two V_T distribution sets of a product as shown in Fig. 1.3. Currently, three main storage materials are frequently discussed in literatures. A conventional floating gate device (FG) uses poly-silicon to store its charges while a nitride and Si nano-dots are used in a SONOS and a nano-crystal device, respectively. A critical concern of these cells is the tight control of threshold voltage (V_T) within given specifications, especially in multi-level cells (MLC) [1]. The V_T distribution further shifts and broadens due to repeated program/ erase cycles and trap assisted tunneling or charge loss during retention [2, 3].

In fresh virgin cells, the V_T distribution is generally wide, due to the effects of process variations being amplified upon the shrunken cell geometry [4]. Moreover, according to reference [5], which we copy the figure as Fig. 1.4, the number of electrons representing one

bit dramatically reduces as the dimensions of flash memories are scaled down with increasing memory density. In other words, the V_T distribution of product will show less immunity to the number fluctuation of both dosage counts and stored electrons during scaling. This implies that small perturbations in processing and operation of the cell will give rise to larger V_T distributions. Many efforts have been devoted to tightening the V_T distribution not only by process optimization but also by correction algorithms [6].

In addition, V_T dispersion is also sensitively affected by local effects such as the discrete dopant fluctuation [7], random poly-silicon grain size etc. [8]. Concerning this, silicon nanocrystals (Si-ncs) or SONOS, should suffer worse V_T variation than convention FG devices. It has recently been shown that the exclusion zone around Si-ncs obtained by chemical vapor deposition [9] plays a fundamental role in the fluctuations from bit to bit of the dot surface coverage. Similarly, the detailed microscopic program charge arrangement in the nitride layer, which allows the formation of one or few conduction paths connecting the source to drain, is supposed to have non-negligible influences on device electrical performance. Therefore, in this work, we employed a three-dimensional drift-diffusion simulator (ISE) to examine the dependence of the V_T on discrete microscopic random distribution/arrangement of the program charges in the nitride layer. The scaling effect will also be studied in such way.

This thesis is organized into five chapters. Following the introduction, flow charts and basic assumptions are detailed described in chapter 2. And then, four main factors including length, width, the dielectric thickness, program window and the random dopant variation will be investigated. Finally, some improved methods and suggestions are given.

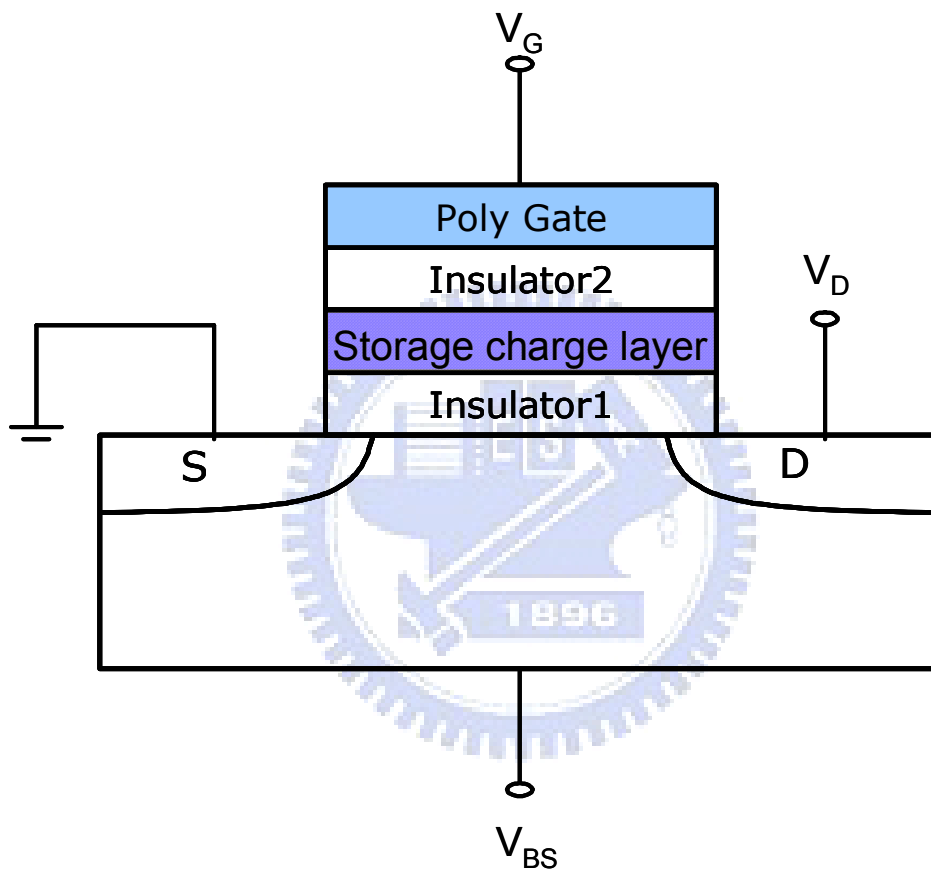


Fig. 1.1 The schematic cross section of nonvolatile memory device.

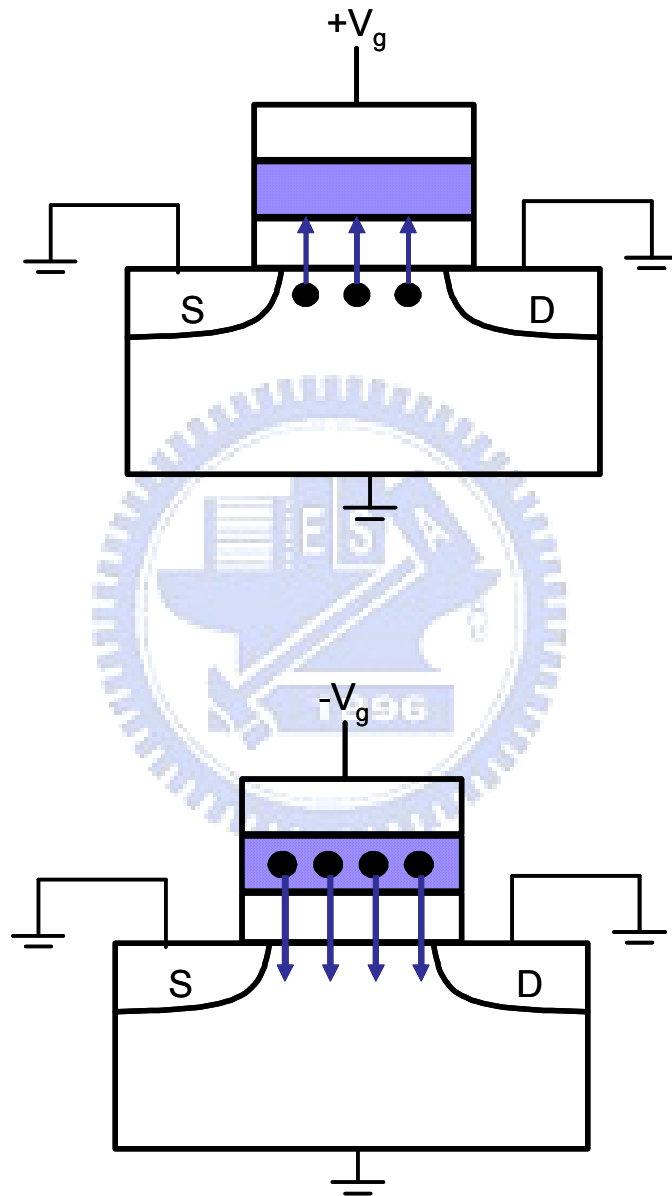


Fig. 1.2 Charge injections in nonvolatile memory during (a) +FN write and (b) -FN erase operation

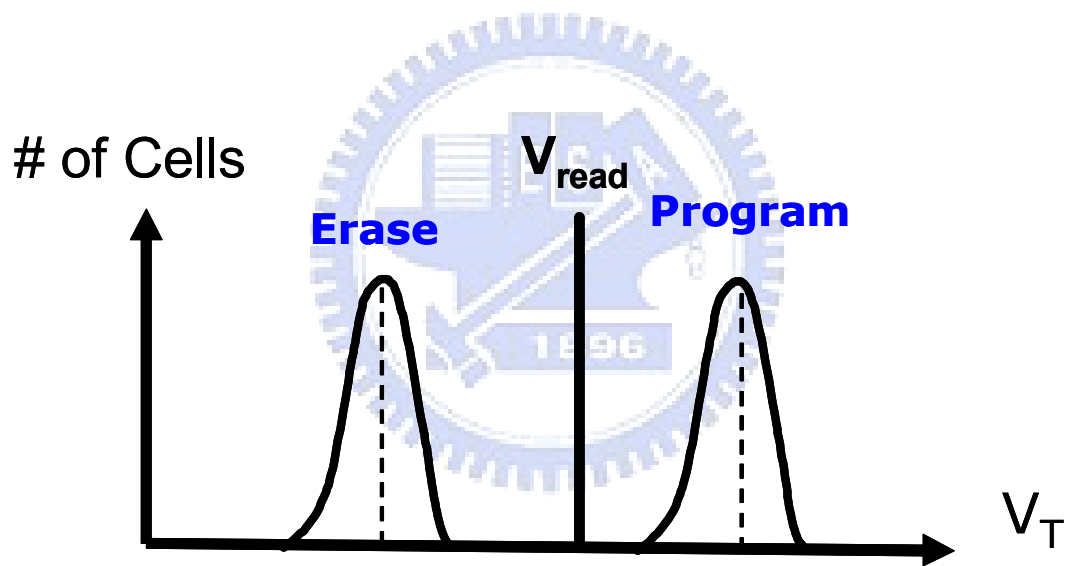


Fig. 1.3 Cell V_T distribution after FN tunneling Program/Erase operation.

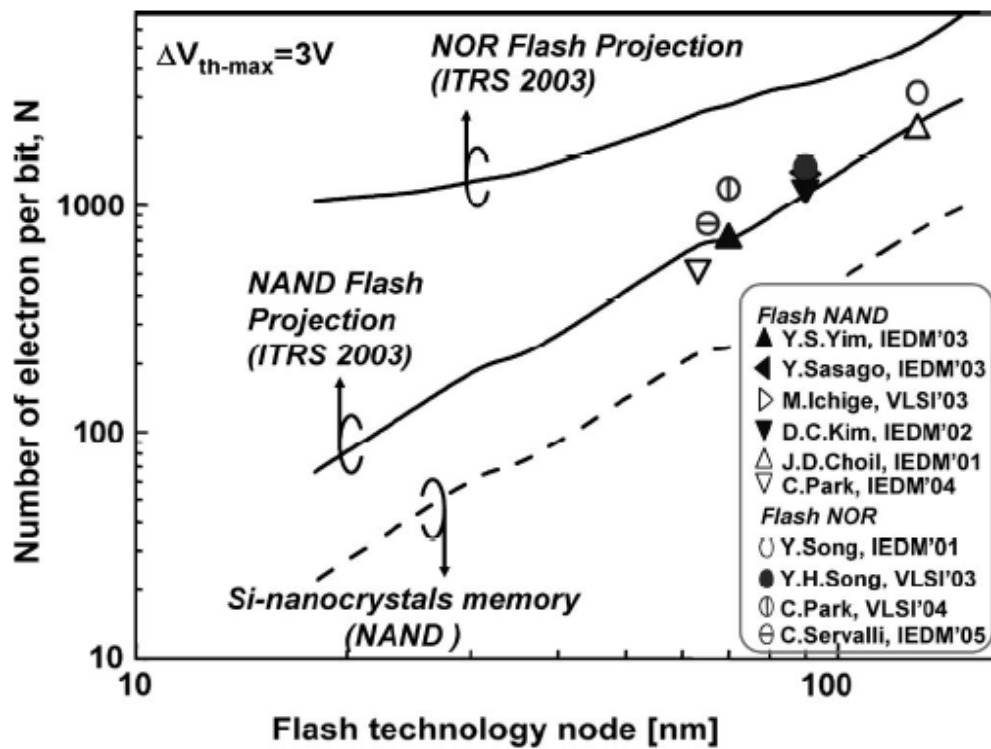


Fig. 1.4 Number of electrons representing a bit as a function of the Flash technology node (only single bit cell are considered), according to the ITRS 2003 edition.

Chapter 2

Simulation Technique

2.1 Devices structure and Simulation Tools

We present TCAD simulations of NAND-type SONOS memories performed with commercial tools, which allow for a good understanding of the impact of the localized charge on electrostatics of the cell. Devices tested in this work are NMOS memory cells with a layer of nitride as trapping layer.

Our simulations are centered on SONOS's with a channel length $L_g = 22$ nm to research the end of roadmap in the future. The channel length is defined as gate length. The channel width in most of the simulations is $W_{\text{eff}} = 45$ nm. And the doping level of $N_A = 10^{18} \text{ cm}^{-3}$ is required to efficiently suppress the short channel effect around the 22 nm channel length barrier. The bottom, top oxide and nitride layer are with a thickness of 3 nm, 8 nm and 7 nm, respectively. Top and bottom oxide layers are considered as pure potential barrier (no traps), and we neglect the electron to escape from them.

The quantum confinement energy becomes significant when the nanocrystal size shrinks to the nanometer range [10]. Similarly, we use a trap as a cubic with spacing 1nm in nitride layer, and assume a fixed charge $Q = -e$ in a storage trap (Fig. 2.1). The average number of charges in this region is calculated by integrating the continuous charged trap density distribution within it. Program charges with a probability distribution corresponding to the continuous charge distribution are placed randomly in the nitride layer.

2.2 Electrostatic Simulations

DESSIS was used to simulate numerically full 3D physical devices. We adopted

three-dimensional, drift- diffusion, which solve self-consistently the Poisson (1) and the carrier continuity equations(2) (3).

$$\nabla \varepsilon \cdot \nabla \psi = -q(p - n + N_{D+} - N_{A-}) \quad (1)$$

$$\nabla \cdot \vec{J}_n = qR + q \frac{\partial n}{\partial t} \quad (2)$$

$$-\nabla \cdot \vec{J}_p = qR + q \frac{\partial p}{\partial t} \quad (3)$$

In our simulation, the threshold voltage is determined by using a current criteria of $10^{-6} W_{\text{eff}}/L_g$ A . The boundary conditions are $V = 0$ at the source contact, $V = V_d$ at the drain contact, and zero normal derivative of V at all other boundaries of the solution domain. And our simulations do not include the quantization in the inversion layer and the poly-depletion effect.

2.3 Percolation theory

When a negative charge is trapped in the storage node, channel inversion close to the traps is inhibited, whereas positive charging can locally enhance the inversion charge. As a result, the inversion charge in the channel is not uniform, and the concept of threshold voltage must be revisited.

Non-uniform charge distribution changes the local V_T in various parts of the device. In the channel width direction, the device may be viewed as many parallel transistors, and the device is controlled by the local minimum- V_T region (Fig. 2.2) [11]. This conduction criterion corresponds to a percolation condition, where channel electrons are able to percolate from source to drain through inverted regions. This local minimum- V_T region can be considered as the critical percolation bridge connecting the source side to the drain side.

The number of electrons representing one bit dramatically reduces as the dimensions of

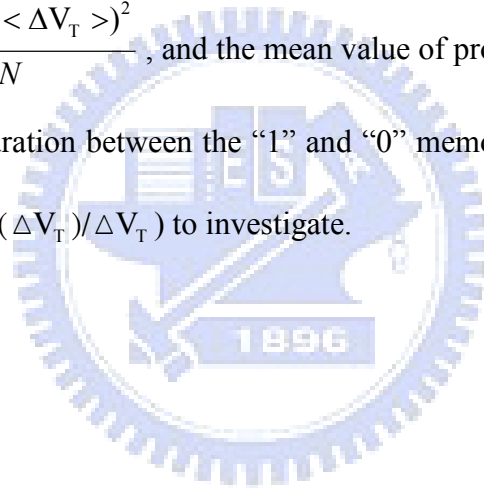
flash memories are scaled down. As a result, the variation in number and position of program charges in the nitride layer makes the microscopic difference between each programmed SONOS more obvious. Most importantly, the random program charge induced inhomogeneous channel potential, inherent to the atomistic simulations, and associated with percolation of the channel current through “valleys” in the potential fluctuations.

2.4 Statistic Method

We adopted the hypothesis that the threshold voltage fluctuations associated with random program charge follow a normal distribution. The standard deviation of the program window for the whole population of microscopically different transistors is

$\sigma < \Delta V_T > = \sqrt{\frac{\sum_{i=1}^N (\Delta V_{Ti} - < \Delta V_T >)^2}{N}}$, and the mean value of program window is ΔV_T . In order

to maintain a clear separation between the “1” and “0” memory programmed states, we used normalize deviation ($\sigma (\Delta V_T) / \Delta V_T$) to investigate.



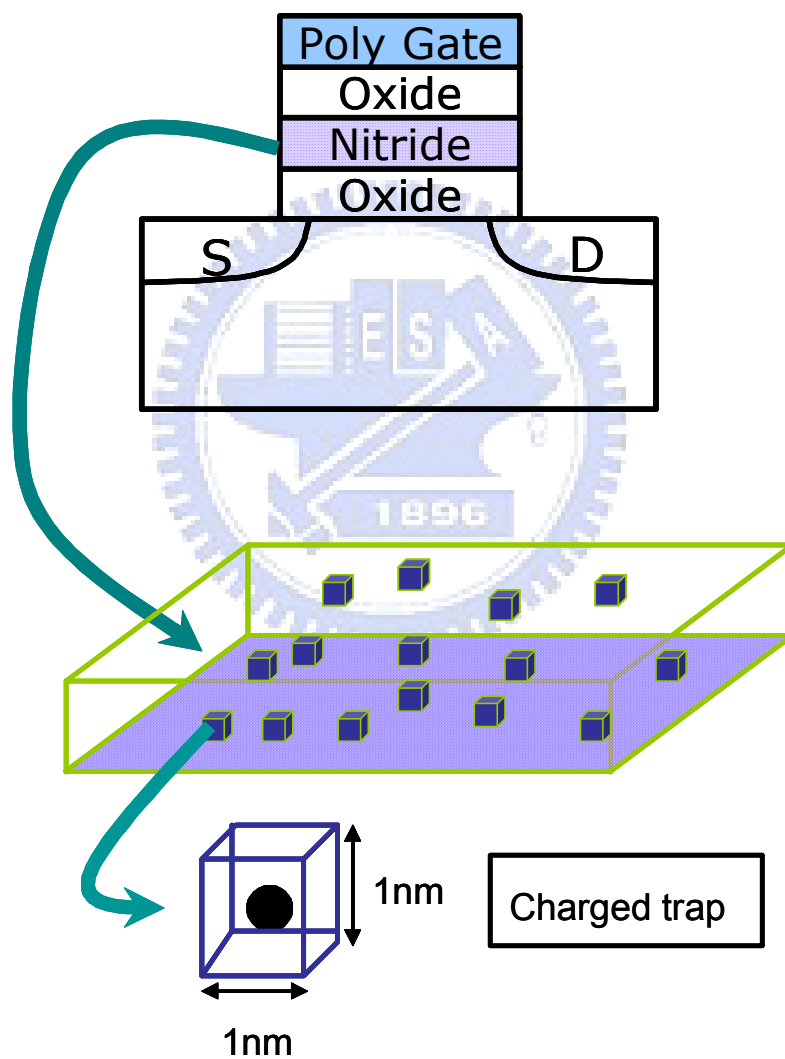


Fig. 2.1 The trap is a cubic with spacing 1nm in nitride layer, and assume a fixed charge $Q = -e$ in a storage trap.

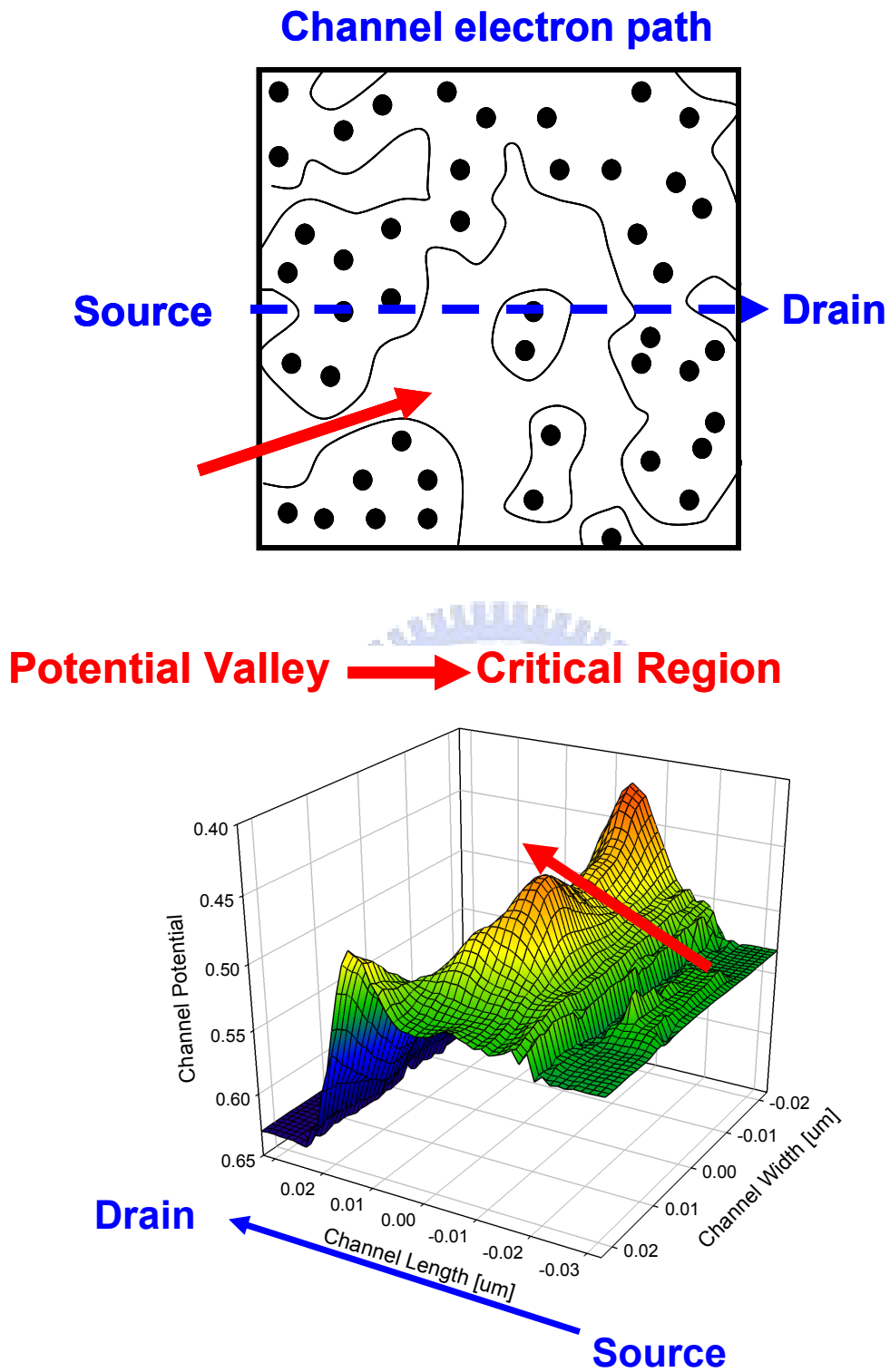


Fig. 2.2 Device is controlled by the local minimum- V_T region.

Chapter 3

Statistical Distribution of ΔV_T with Fixed Program Charge Number

3.1 Introduction

The programming mechanism of NAND-type SONOS flash memory is Fowler-Nordheim (FN) tunneling. The number of electrons representing one bit dramatically reduces as the dimensions of flash memories are scaled down. Thus the characteristic of the discrete charged traps can not be neglected. A complete understanding of the influence of the program charge distribution on threshold voltage fluctuation needs to be built in order to define the specifications and the limits of the device. In order to investigate this effect on the threshold voltage fluctuation, we have evaluated V_T asymmetry by interchanging the source and the drain terminals [12]. And both L_g , W_{eff} , program window and dielectric thickness are varied in the different simulation experiments.

3.2 Both forward and reverse source/ drain operation

Microscopic program charge distribution gave rise to asymmetry in drain current upon interchange the source and the drain. V_{TF} and V_{TR} show the threshold voltages before and after interchanging the source and the drain terminals, respectively. Fig. 3.1 (a) and (b) show the relationship between V_{TF} and V_{TR} of SONOS at the drain bias V_d of 1 and 0.1 V, respectively, where L_g is about 22 nm. Moreover, the correlation between V_{TF} and V_{TR} becomes degraded at a high drain bias. It should be noted that V_{TF} significantly differs from V_{TR} in the case of $V_d = 1$ V, but V_{TF} is almost the same as V_{TR} at $V_d = 0.1$ V. This fact means that the threshold voltage has asymmetry on interchanging the source and the drain terminals at a high drain bias, and this asymmetrical V_T disappears when the drain bias is reduced.

When drain (source) side depletion broadens toward to the direction of channel region, part of program charge region was covered. At that time, V_T is affected by the program charge region which is near the source (drain) side.

In Fig. 3.2, the difference of surface potential landscape between $V_d = 0.1V$ and $V_s=0.1V$ is not obvious. For $V_d= 1.0 V$ and $V_s=1.0 V$, we found the critical region is very different. Therefore, V_T asymmetry is considered to be the fact that the program charge arrangement near the drain side and the source side microscopically fluctuate and statistically differ from each others. We can say that this V_T asymmetry is caused by the statistical-random distributed program charge in the nitride layer. In other words, V_T asymmetry increases with decreasing the effective channel length.

3.3 Channel length dependence of ΔV_T

Different probabilities of percolation, depending on the distance between the two electrodes that has to be connected by the percolation path (i.e. L) and on the width of the electrodes (i.e. W). In fact, as the inter-electrode distance L is increased, the probabilities of percolation decreased, since it requires the connection among an increasing number of independent inverted regions (In Fig. 3.3). As expected, the average V_T increases as the L is increased, corresponding to increasingly less probable percolation through inverted regions, as indicated in Fig.3.4.

Fig. 3.5(a) and (b) shows the fluctuations in threshold voltage, $\sigma < \Delta V_T >$, for SONOSs scaled from 65nm to 32nm. When channel length continues to increase, the number of independent inversion regions which is needed to connect to percolate from source to drain increase. The more trapped charges make the more critical regions to control percolation. Thus, the effect of charge distribution has abated, and the threshold voltage variation

decreases.

3.4 Channel width dependence of ΔV_T

In the channel width direction, the device may be viewed as many parallel transistors and the device is controlled by the local minimum- V_T region. Increasing the channel width W_{eff} improves the probability for the percolation by simply increasing the number of possible paths connecting source and drain.

Note that the reduction of W_{eff} also results in an increase of the threshold voltage fluctuation (In Fig. 3.6 (a) and (b)). The influence of one electron is much larger in the narrow channel device, and the electrons in several local minimum- V_T regions dominant the conductance of the whole channel. Thus, small number of trapped charges makes each SONOS which one has the same number of program charge very differently (In Fig. 3.7). The increased spread of the V_T distribution can be explained by the typically small number of traps controlling the percolation bottleneck.

3.5 Program charge density dependence of ΔV_T

From section 3.3 and 3.4, we can find that the charge number is the main factor to decide the importance of the program charge placement. In this section, we investigate the V_T spread in the different program charge density in the cell with the same channel width $W_{\text{eff}}=45\text{nm}$ and channel length $L_g=45\text{nm}$. The spreading of V_{TS} ($\sigma\Delta V_T$) becomes more serious as we increase the programmed charge density (In Fig. 3.8) induced by the increment of the randomness of conduction paths from source to drain should be responsible for this phenomenon.

Even though the spread of V_T is increasing with increase of program window, it still has chance to get the larger operation window (In Fig. 3.9). The higher operation window can

maintain a clear separation between the “1” and “0” memory programmed states. In Fig. 3.10, we considered SONOS memory cells with channel length 32nm, 45nm with channel width 45nm and channel width 22nm, 45nm with channel length 45nm. In order to maintain a clear separation between the “1” and “0” memory programmed states, we have to assure σ (ΔV_T)/ $\Delta V_T < 6\%$ on our devices, for whatever combination of cell area and program charge density. The results indicate smaller device needs more program charges to ease the fluctuation of ΔV_T induced by random program charge. This means that going toward smaller and smaller cell areas, higher and higher program charge density will be needed, which assures both small dispersion and clearly detached memory states.

3.6 Oxide-nitride-oxide (ONO) stacked layers dependence of ΔV_T

3.6.1 Bottom oxide thickness

Important for embedded SONOS memories are the lower program and erase voltages compared to floating gate flash, due to the thin bottom oxide. These low voltages are combined with excellent endurance, but the data retention is an issue [13].

Since surface potential is remotely controlled by trapped charges and a thinner bottom oxide means that a shorter distance from programmed charges to Si-surface, these charges certainly will show a stronger impact on the surface potential than those stored above a thicker oxide. Fig. 3.11 indicates thinner bottom oxide makes the local channel potential more sensitive induced by trapped charge. In other words, the thinner bottom oxide results inhomogeneous channel potential more serious. We used device with $L_g=22\text{nm}$ $W_{\text{eff}}=22\text{nm}$ to investigate how about random charge effect at the same program window with discrete program charge in different bottom oxide thickness ($T_{\text{BOX}}=1, 3, 5 \text{ nm}$). The decreasing of bottom oxide thickness results in the increasing of spread of threshold voltage (Fig. 3.12). The

thinner bottom oxide makes the more sensitive on threshold voltage fluctuations induced by random program charge distribution effect. In other words, even the total effective oxide thickness (EOT) does not change much during bottom oxide scaling, the V_T fluctuation is greatly affected.

3.6.2 Top ON stakes thickness

Usually SiO_2 is applied as a top oxide in a conventional SONOS. Since SiO_2 has low dielectric constant $\epsilon = 3.9$ in comparison with Si_3N_4 ($\epsilon = 7.5$) the electric field in top oxide is about two time larger, than in nitride. Therefore, for scaled SONOS device with comparable thickness of nitride and SiO_2 top oxide, a remarkable part of applied voltage drops on the top oxide during W/E programming . Replacing SiO_2 by high-k dielectric can decrease this undesirable voltage drop and, consequently, the total applied voltage [14].

We used the different top oxide thickness with the EOT of different dielectric constant material (Si_3N_4 ($\epsilon = 3.9$), Al_2O_3 ($\epsilon = 9$) and ZrO_2 ($\epsilon = 25$)), which have the same physical thickness, to investigate the influence of ON stacks capacitance in threshold voltage fluctuations. According to equation (4)

$$\Delta V_T = -\frac{Q_{SiN}}{\epsilon_0} \left(\frac{x_{BO}}{\epsilon_{BO}} + \frac{x_N}{\epsilon_N} \right) \quad (4)$$

Q_{SiN} is the total amount of the charge trapped in the nitride, $\epsilon_{BO}, \epsilon_N$ are the dielectric constants in the blocking oxide and nitride. Here, it can be shown that the higher dielectric constant makes the lower EOT of ON stacks. Thus the contribution of one trapped charge in V_T deviation is reduced. Even the lower EOT the more number of program charge to represent one bit is needed, the deviation of V_T is offset by lower EOT. In Fig. 3.13(a) and (b), the higher dielectric constant material can have the tight distribution of program threshold

voltage. As the results, the top oxide or trapped layer replaced by high-k material can ease the random charge effect.

3.7 Summary

In this chapter, we investigate the cell V_T in presence of negatively charged traps is statistically distributed due to the statistical fluctuation of charged trap positions at the trapped layer. For fixed charged trap number, the fluctuation in the trapped charge positions induces a statistical modulation of the local inversion charge in the silicon substrate. For a fixed applied gate voltage, the inversion charge is in fact smaller near the negatively charged traps, reducing the current flow in these regions. Nonuniform channel conduction thus results, with cell ΔV_T strictly dependent on the possibility for the trapped charges efficiently stop the current flow from source to drain.

As device is scaled, the ΔV_T fluctuation is more serious. The standard deviation increases with decreasing of channel length and width, which illustrates the discrete program charge effect is non-negligible. And the spread of ΔV_T is also increasing for cells with higher program charge density, because the increment of randomness of percolation path. This means that going toward smaller and smaller cell areas, higher and higher program charge density will be needed, which assures both small dispersion and clearly detached memory states. In our knowledge, the program threshold voltage is related with ON stacks capacitance. In this work, we found the random charge effect is not only related with ON capacitance but also bottom oxide thickness.

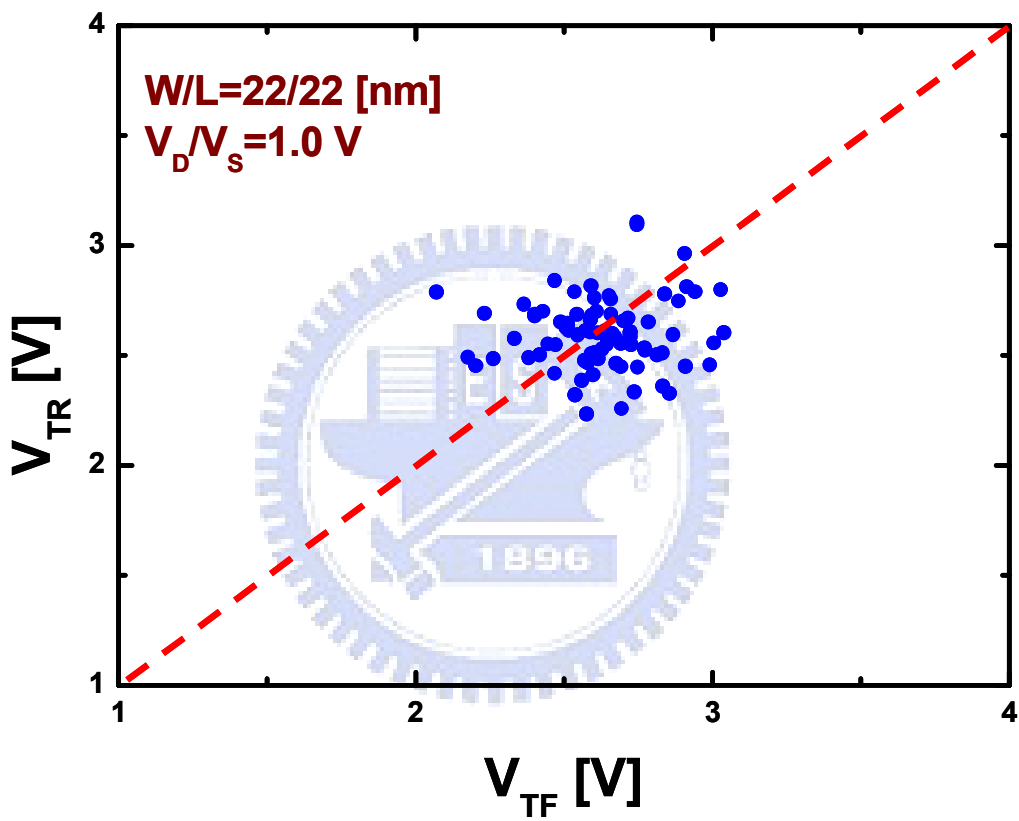


Fig. 3.1(a) It indicates a lack of correlation between V_{TF} and V_{TR} of SONOS at the drain bias $V_d=1V$.

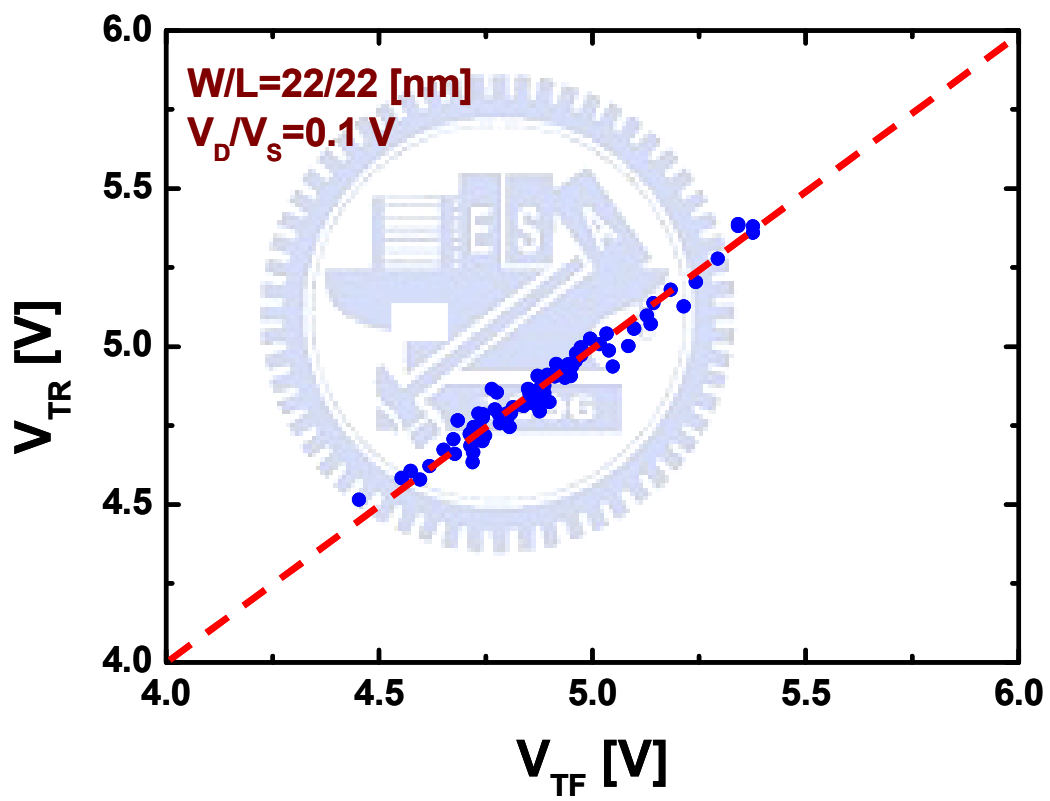
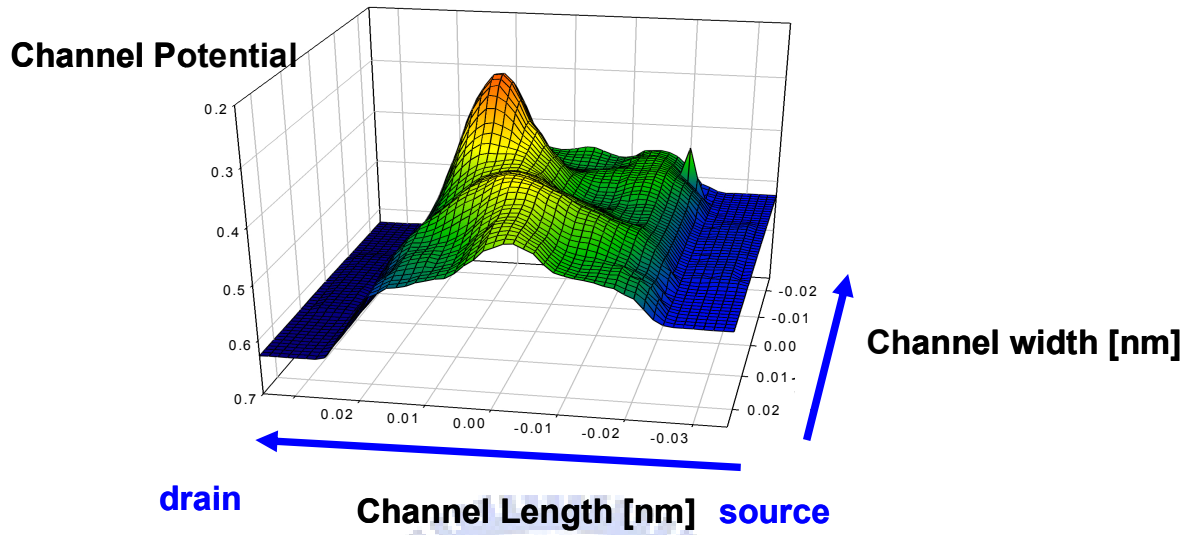


Fig. 3.1(b) It indicates they are highly correlated between V_{TF} and V_{TR} of SONOS at the drain bias $V_d=0.1V$.

$$V_G=4.7 \text{ V}_D=0.1$$



$$V_G=4.7 \text{ V}_S=0.1$$

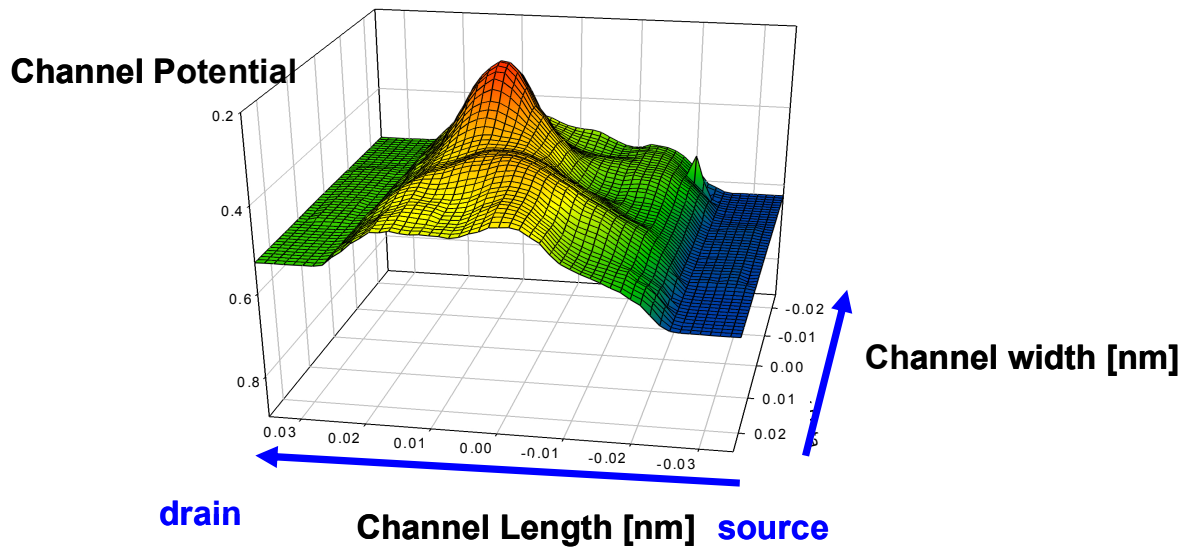
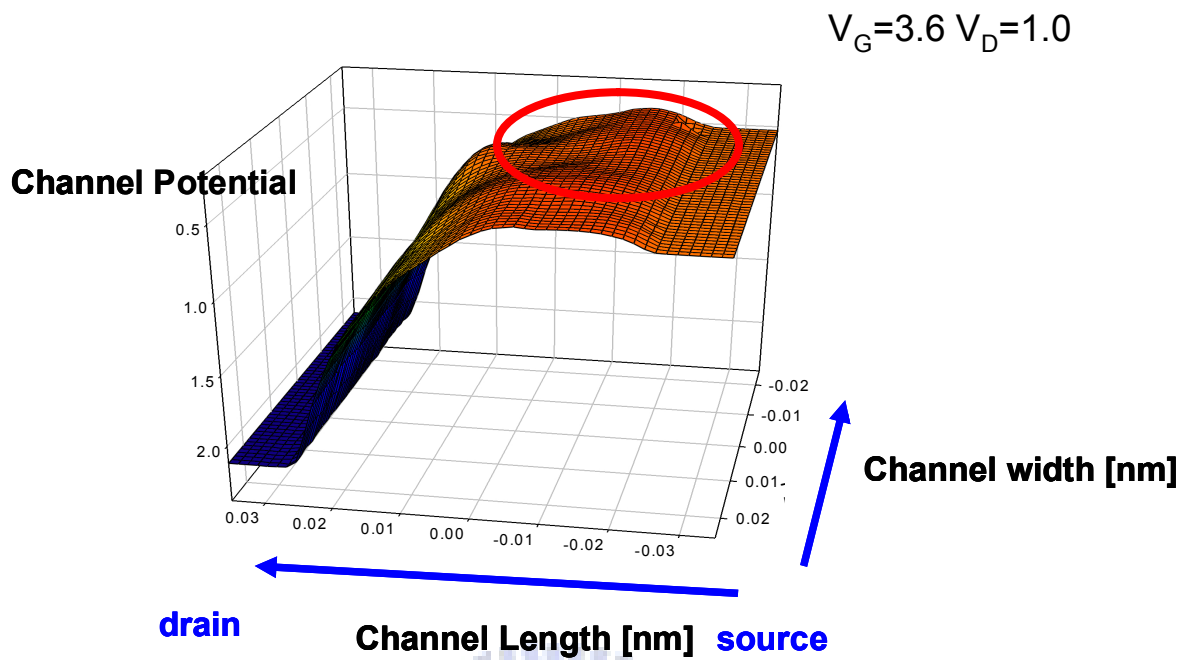


Fig. 3.2(a) Difference of surface potential landscape between $V_d = 0.1\text{V}$ and $V_s=0.1\text{V}$ is not obvious.



Critical region

$V_G=3.6$ $V_S=1.0$

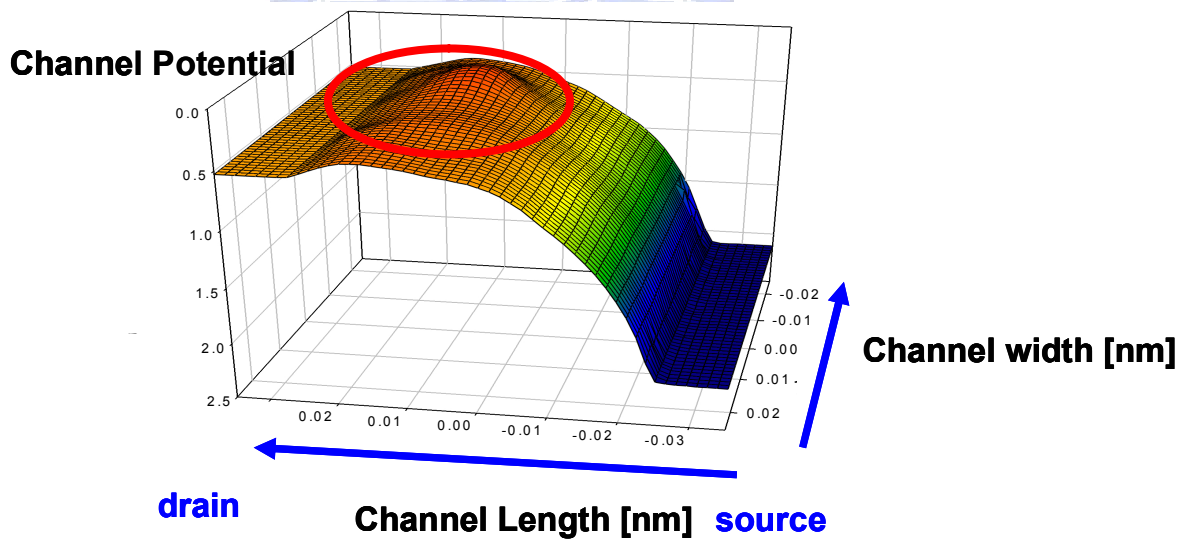


Fig. 3.2(b) Potential of the critical region between $V_d=1.0$ V and $V_s=1.0$ V is very different in microscopic.

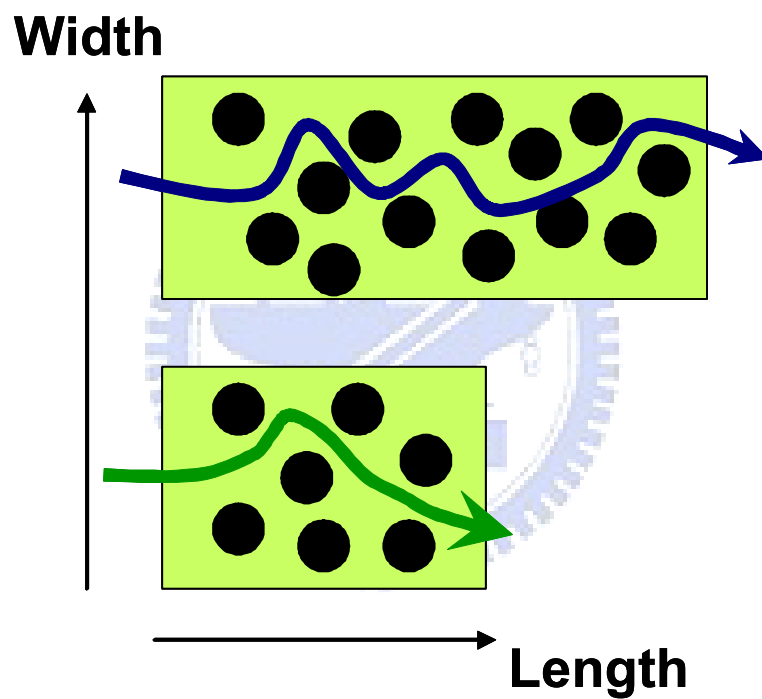


Fig. 3.3 As L is increased, the probabilities of percolation decreased, since it requires the connection among an increasing number of independent inverted regions.

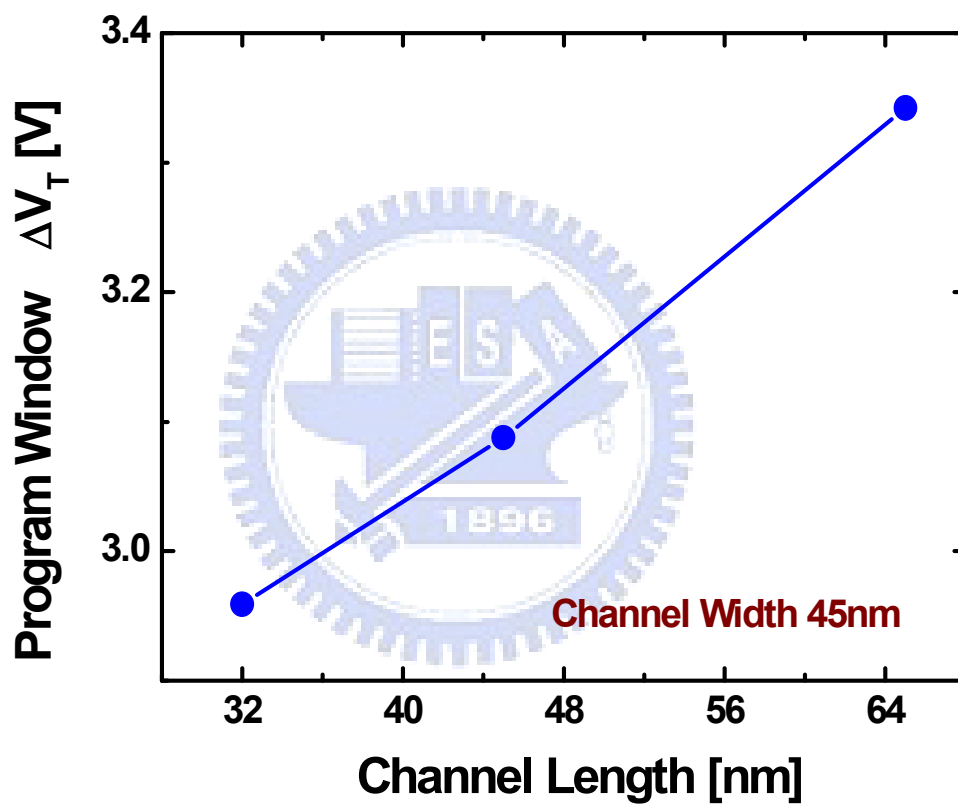


Fig. 3.4 Average V_T increases as the L is increased due to decrease of percolation path.

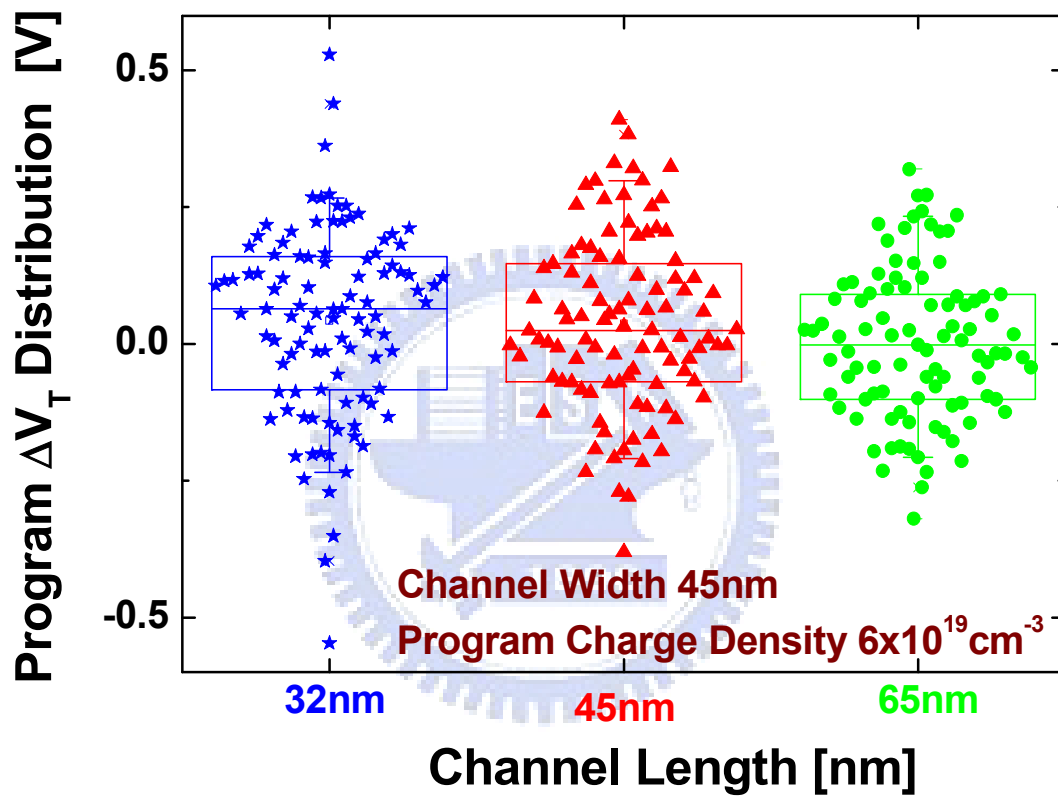


Fig. 3.5 (a) When channel length decrease the magnitude of the fluctuations increase.

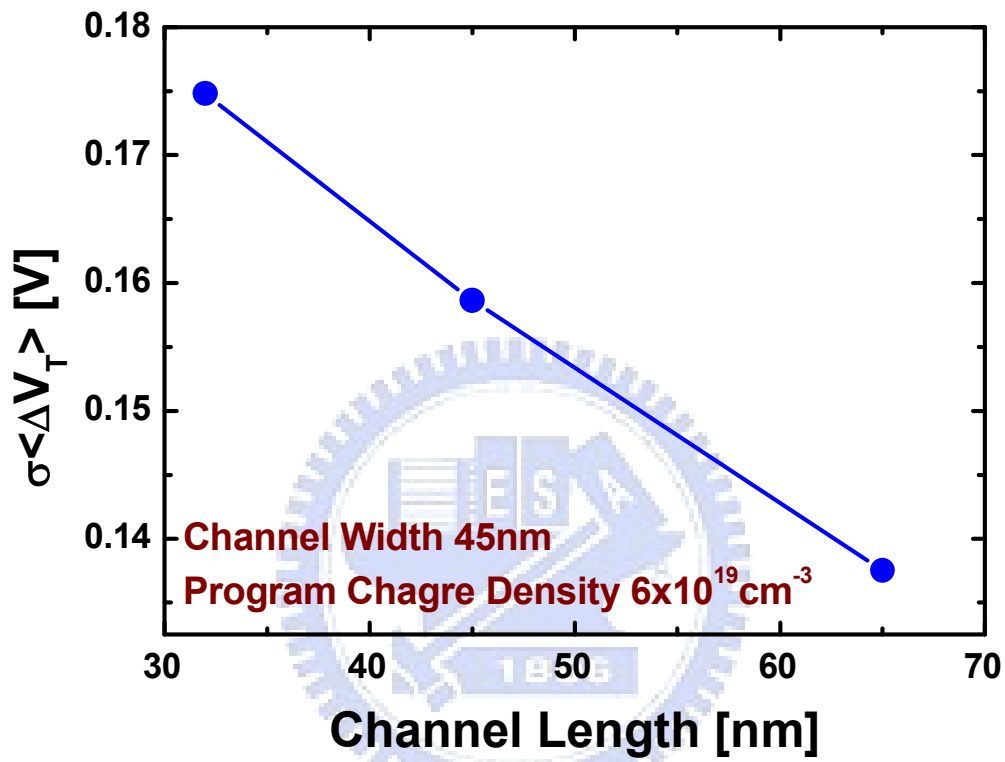


Fig. 3.5 (b) As dimensions are decreased the magnitude of the fluctuations increase.

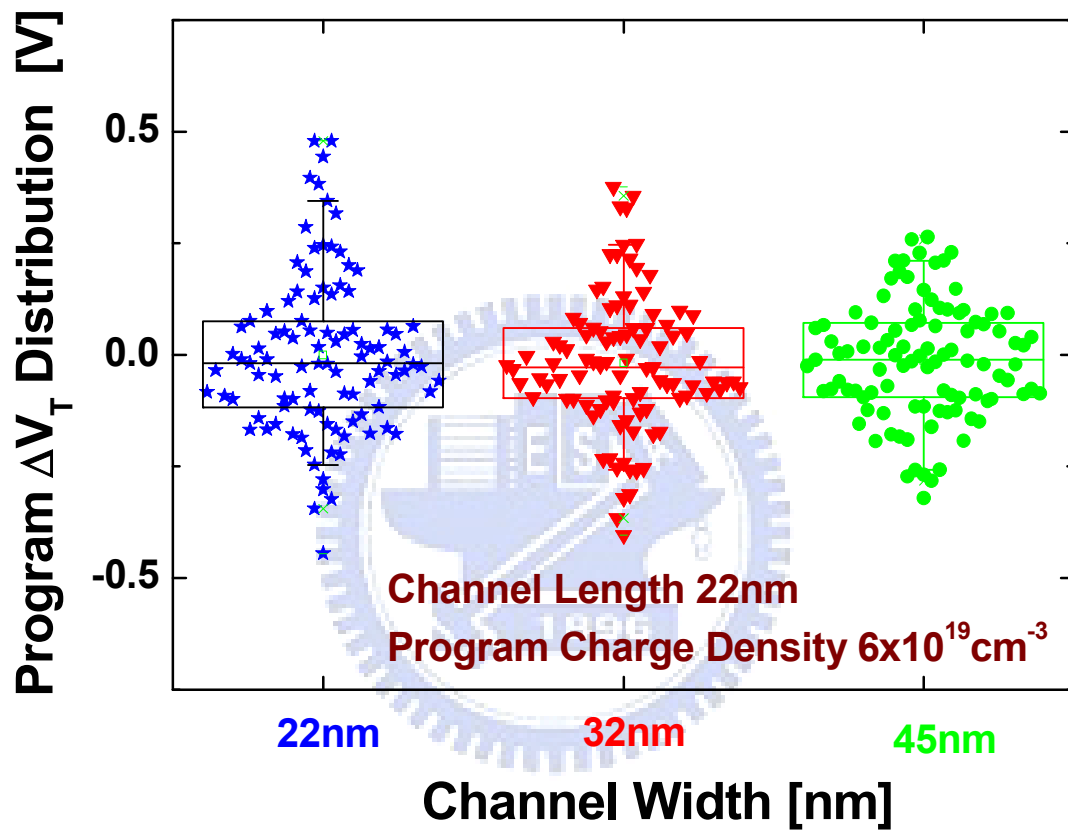


Fig. 3.6(a) The reduction of W_{eff} also results in an increase of the threshold voltage fluctuation.

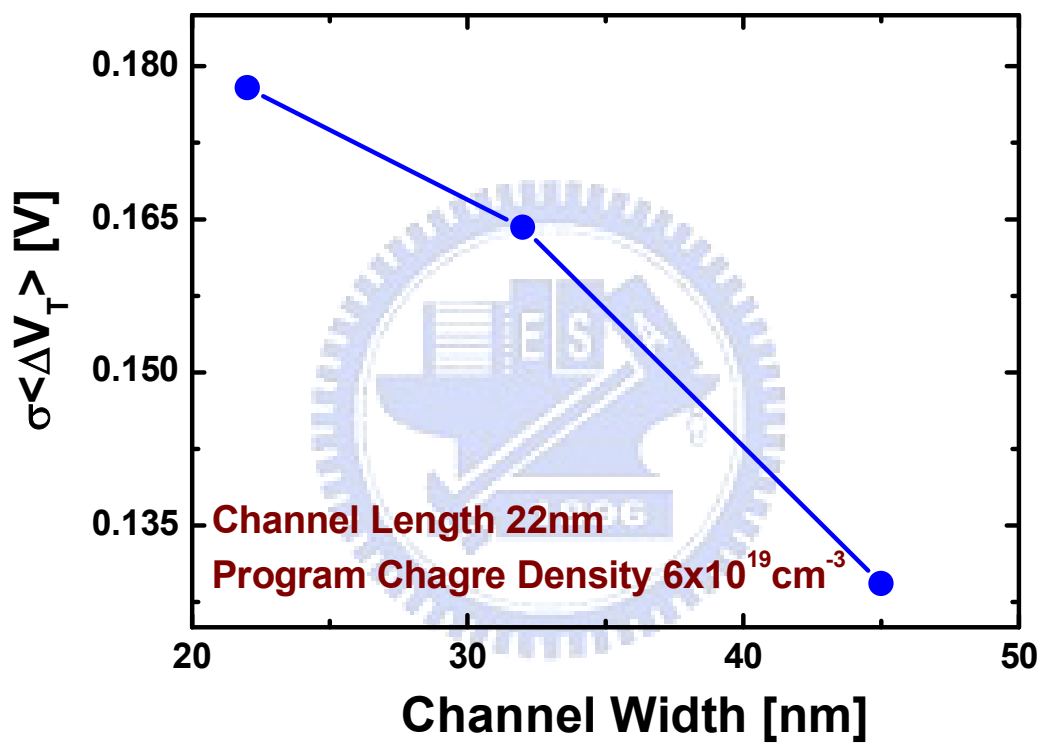


Fig. 3.6(b) The reduction of W_{eff} also results in an increase of the threshold voltage fluctuation.

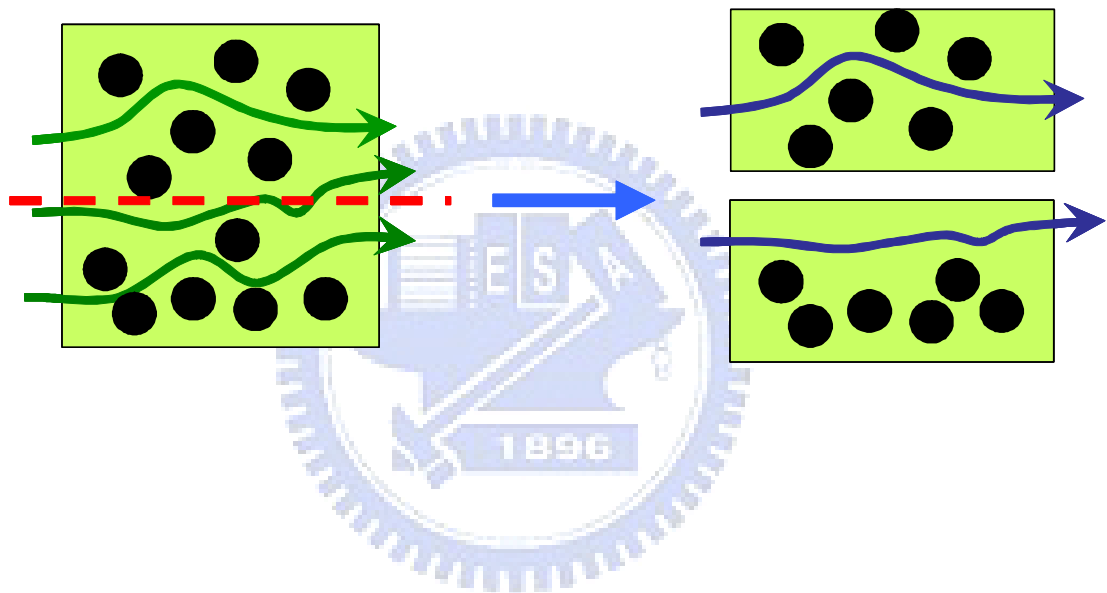


Fig. 3.7 Small number of trapped charges results in extremely condition on charge arrangement easily.

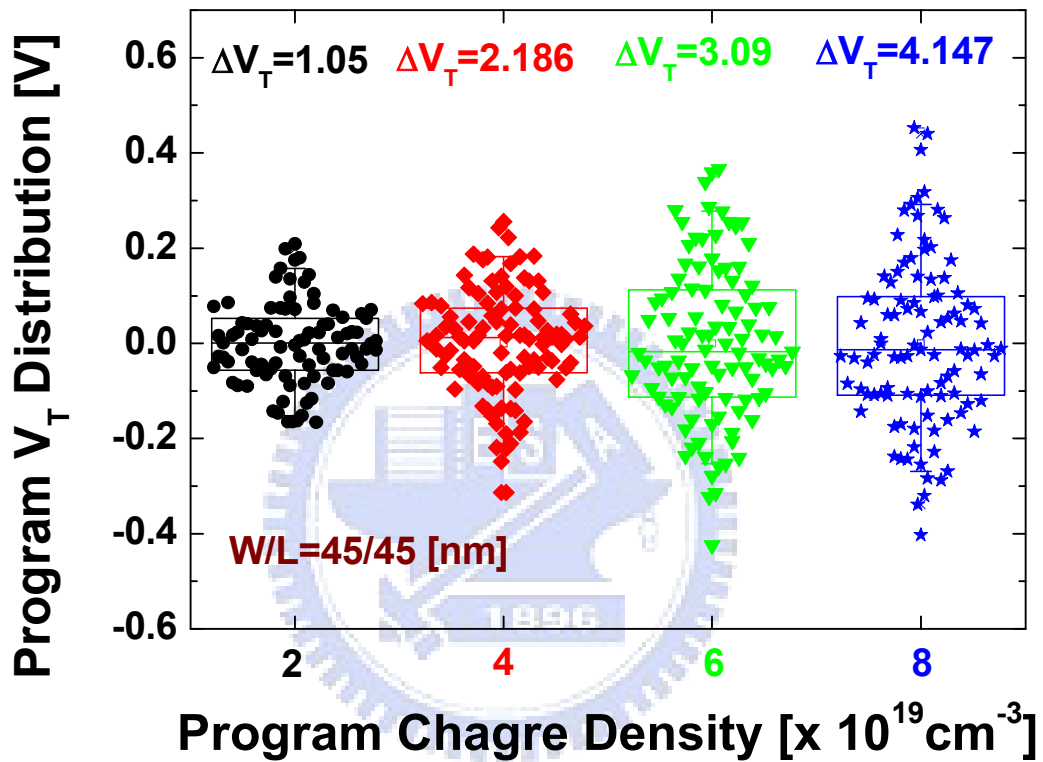


Fig. 3.8 The spreading of V_{TS} ($\sigma\Delta V_T$) becomes more serious as we increase the programmed charge density

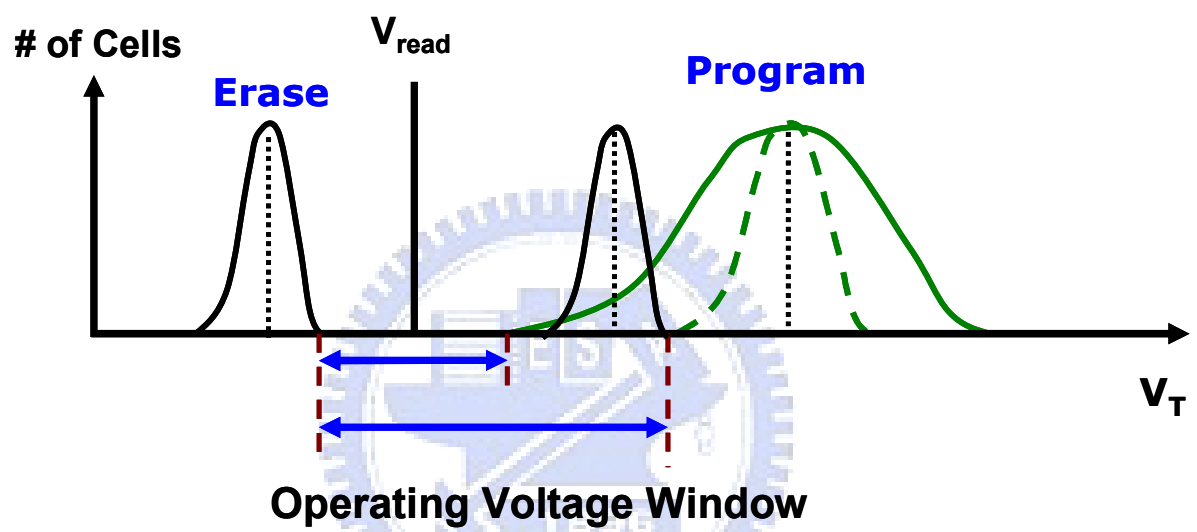


Fig. 3.9 Even though the spread of V_T is increasing with increase of program window, it still has chance to owe the larger operation window.

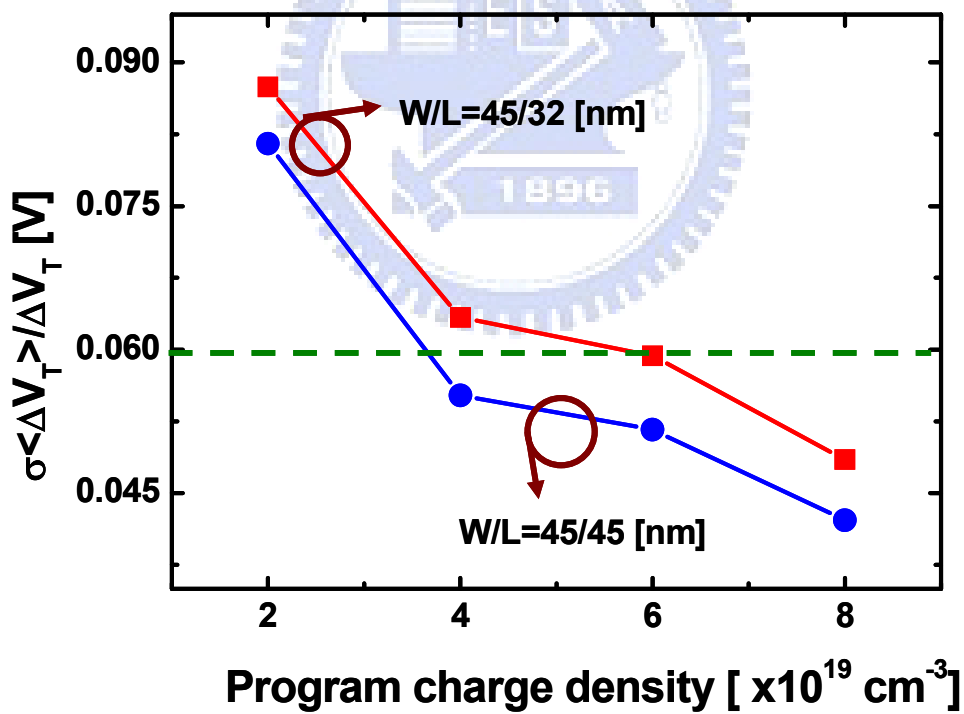
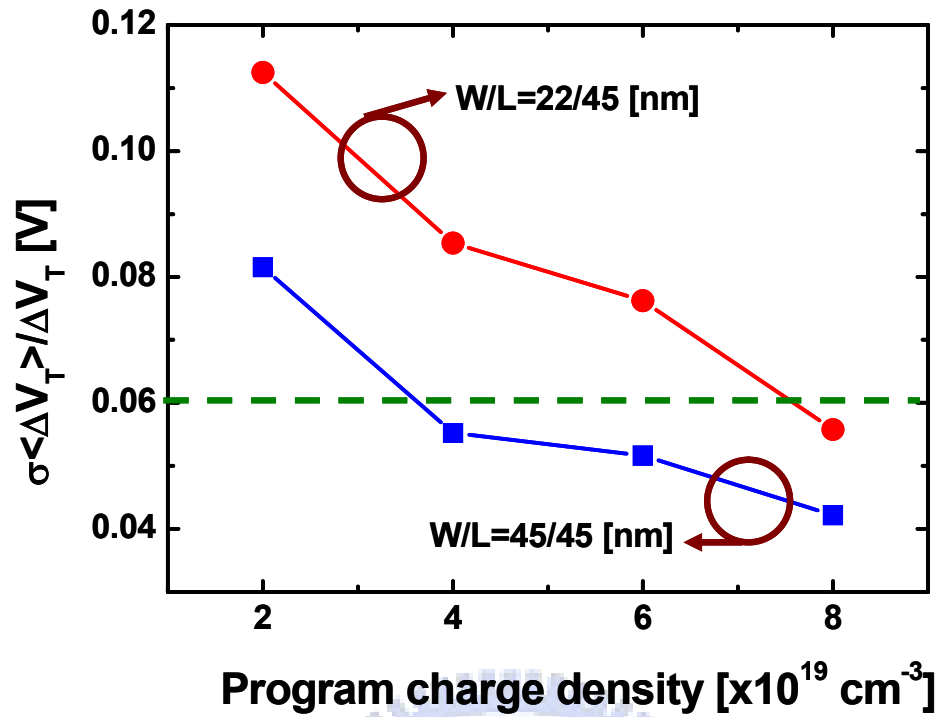


Fig. 3.10 This means that going toward smaller and smaller cell areas, higher and higher program charge density will be needed.

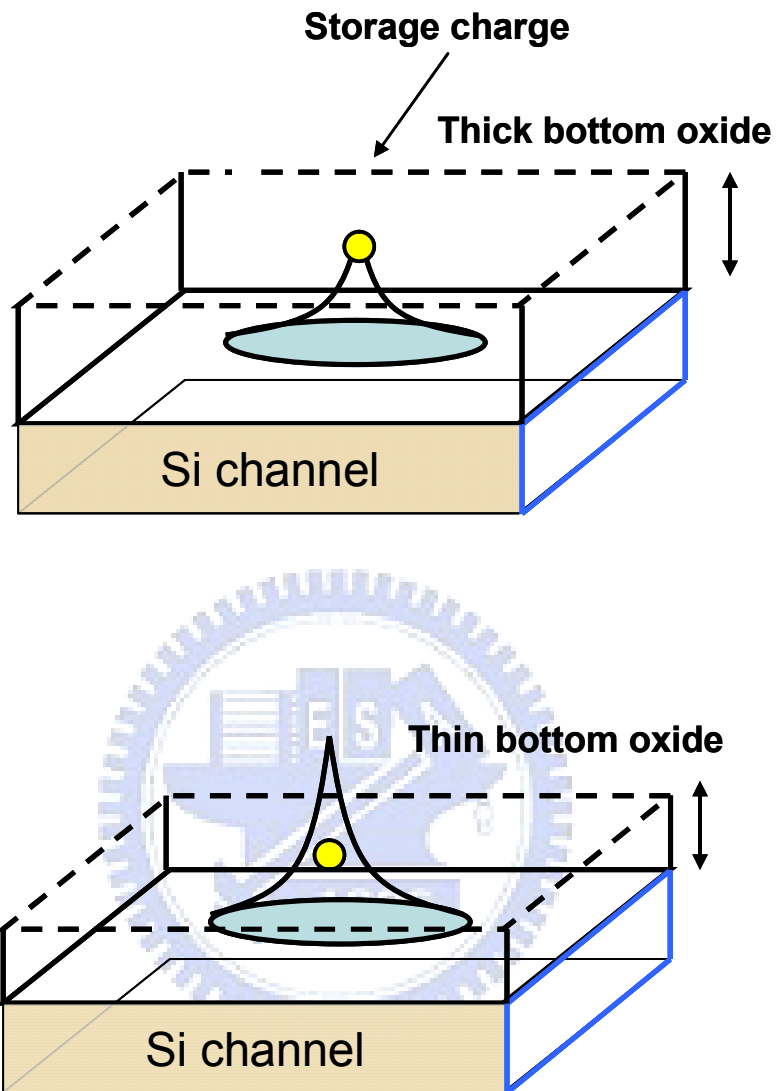


Fig. 3.11 Thinner bottom oxide makes the local channel potential more sensitive induced by trapped charge.

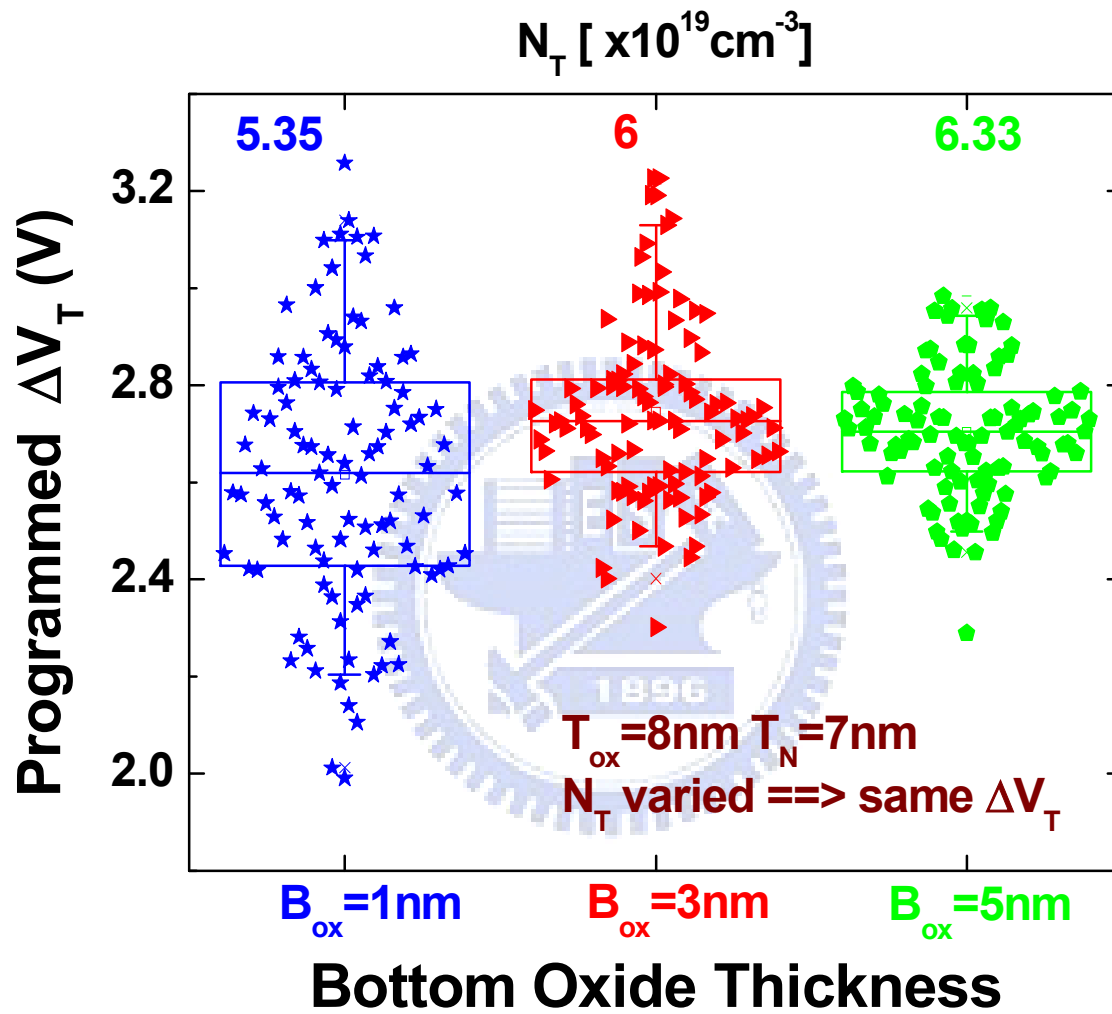


Fig. 3.12(a) The thinner bottom oxide makes the difference of surface potential between each local channel region is higher than the device with thick bottom oxide

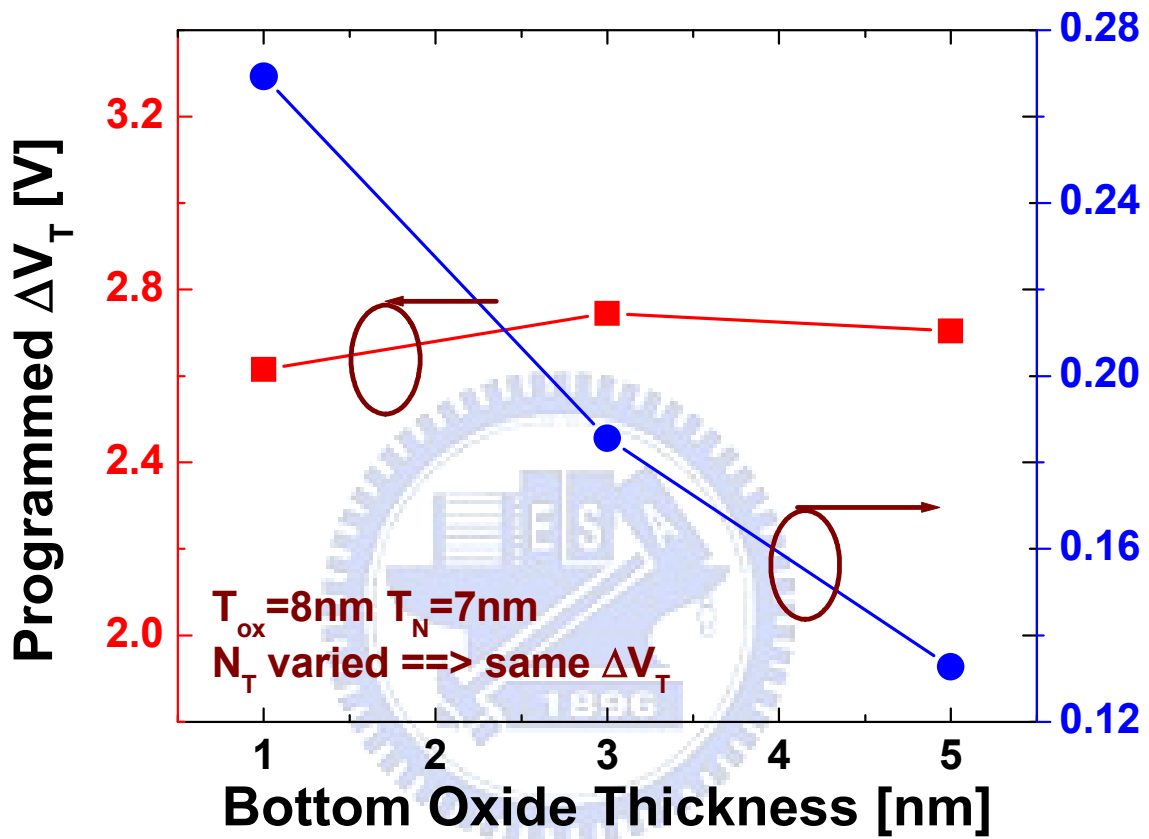


Fig. 3.12(b) The thinner bottom oxide makes the more sensitive on threshold voltage fluctuations induced by random program charge distribution effect.

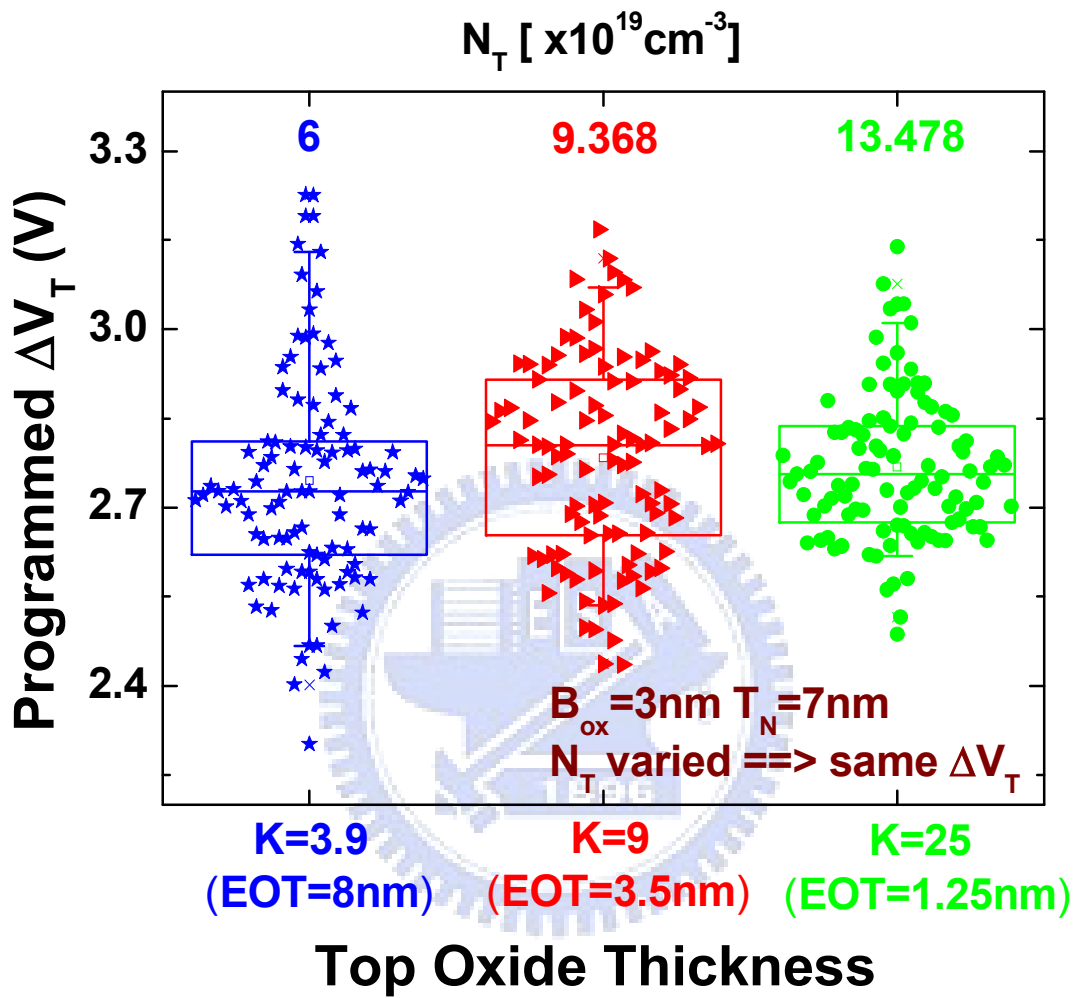


Fig. 3.13(a) The thinner top oxide thickness can have the tight distribution of program threshold voltage.

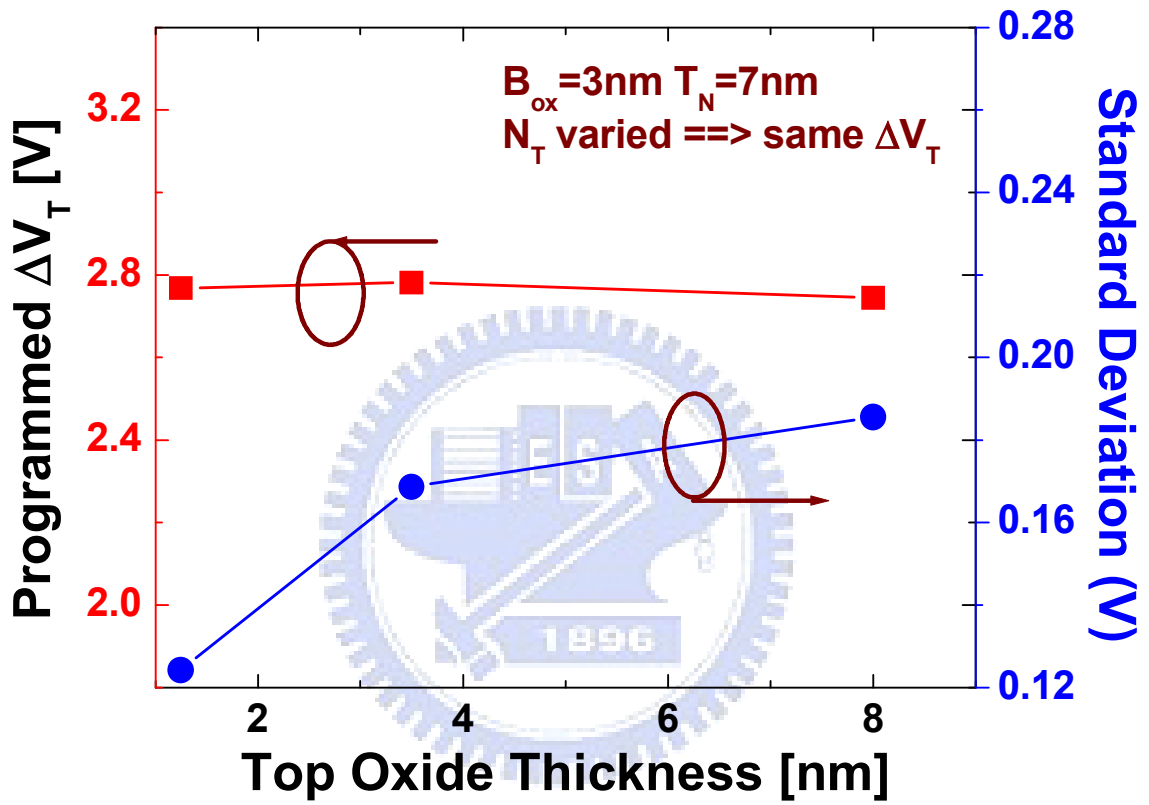


Fig. 3.13(b) The thinner top oxide thickness can have the tight distribution of program threshold voltage.

Chapter 4

The Effect of Random trapped charge with Random dopant in Threshold Voltage Fluctuations

4.1 Introduction

The different sources of intrinsic parameter fluctuations, which can be separated in simulations, will occur simultaneously within a single SONOS. To understand how these fluctuations will interact and to what extent they are statistically independent we have carried out simulations with more than one source of fluctuation present [15]. In this chapter, pairs of fluctuation sources are simulated in order to test their statistical interdependence or possible correlation. The pairs considered included discrete random program charges with discrete random dopants. And we considered (I) number fluctuations and (II) atomistically microscopic distribution in random program charges and random dopants.

4.2 Random Dopant Induced Threshold Voltage Fluctuations

As silicon MOSFET is scaled, the number of dopants is of the order of hundreds in the depletion region (In Fig. 4.1), and below 100 in the inversion layer, for minimum geometry devices. As a result, the detailed microscopic dopant distribution in the MOSFET channel will have non-negligible influences on device electrical performances [16].

The depletion width is 36nm in our device structure. To substantially reduce the computation time, we need to investigate which part is efficient to affect threshold voltage. Our simulation focuses on the 22 nm channel length and channel width, and the doping level is $N_A=10^{18}\text{cm}^{-3}$ in the following simulations. First, as shown in Fig.4.2 (a), a 4-nm-thick lightly doped layer ($N_A=10^{15}\text{cm}^{-3}$, background doping concentration) was placed on the

substrate surface. Then we continued to increase the thickness of the lightly doped layer thickness (case A). To confirm which part in the substrate contributes effectively to affect threshold voltage, we carried out other simulations. As show in Fig. 4.2 (b), we used a 4-nm-thick lightly doped layer to replace the heavily doped layer and increase its thickness from the bottom of depletion region to the substrate surface (case B).

Fig. 4.3 shows the V_T dependence on the lightly doped layer thickness. The V_T was most decreased when lightly doped layer was placed at the surface. However, the decreasing rate of V_T became slow down when the lightly doped layer was 18nm in both cases. The results in Fig. 4.3 indicate that dopant contributions to V_T are not the same through the depletion layer. Thus we chose 15nm depth in the substrate to simulate random dopant effect. The fluctuations are studied using typical samples of 100 atomistically different SONOS. Simulation results agree with [16], the random dopant induced threshold voltage lowering, inherent to the atomistic simulations, (threshold voltage of uniform doping, $V_{T0}=2.15$ V; average threshold voltage of random dopant simulation, $\langle V_T \rangle = 1.927$ V, and the standard deviation, $\sigma \langle V_{T(RD)} \rangle = 0.13198$).

4.3 Dual Sources of fluctuations

4.3.1 Random dopant (RD) and random trapped charge (RC)

It is important to note that, in realistic devices, the number of program charge in the cell is not constant, as assumed in the simulation results, but is affected by a statistical spread due to the Poisson distribution of charged traps in the nitride layer. In this work, we used random program charge density ($N_T=3.33 \times 10^{19} \text{ cm}^{-3}$) to simulate the real condition for SONOS operation. The V_T standard deviations are $\sigma \langle V_{T(RD)} \rangle = 0.13198$ V and $\sigma \langle V_{T(RC)} \rangle = 0.4876$ V in the random dopant and random charge effect, respectively..

The standard deviation produced by these two sources of intrinsic parameter fluctuations is $\sigma < V_{T(RC\&RD)} > = 0.48903$. The combined effect of two statistically independent variables on the standard deviation is described by the relation $\sigma_{1,2} = \sqrt{(\sigma_1^2 + \sigma_2^2)}$ [15]. If we use this expression to combine the standard deviations associated with random program charge and random discrete dopants the combined standard deviation is 0.505 V which is higher than the value obtained from the simultaneous simulation of two fluctuation source ($\sigma < V_{T(RC\&RD)} > = 0.48903$ V). This provides strong additional evidence that these two sources of intrinsic parameter fluctuation in the SONOS device are statistically dependent. In Fig. 4.4, the spread of V_T induced by random charge is higher than random dopant. It indicates the random charge effect is the main source in threshold voltage fluctuations.

4.3.2 Random trapped charge with the method of Suppression random dopant effect

According to reference [17], we have already known the random dopant effect can be suppressed by epitaxial layer with lightly doped concentration (In Fig. 4.5). When the epitaxial layer is relatively thick, the width of the depletion layer in the heavily doped region beneath the epitaxial layer becomes rather small. The holes in the heavily doped region start to screen the charge of the discrete random acceptors in the thin depletion layer, reducing their effect on the threshold voltage fluctuation. In our simulation, the thickness of the epitaxial layer has to be chosen 15nm, which part in the substrate contributes effectively to affect threshold voltage. And the background doping in the epitaxial layer is assumed to be 10^{15} cm^{-3} , and the doping behind it is 10^{18} cm^{-3} .

The simulation results are compared with conventional random dopant effect in Fig. 4.6. It indicates that epitaxial layer can efficiency reduce the threshold voltage fluctuation induced by random dopant. But this method can not significantly reduce the program state threshold

voltage fluctuation because of random trapped charge is the main factor to result in V_T variation.



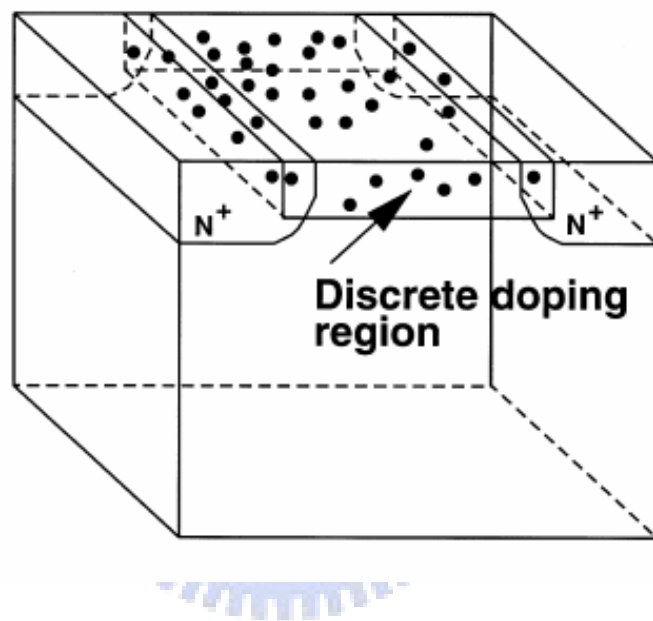


Fig. 4.1 Investigate the influence of discrete dopant in the depletion region.

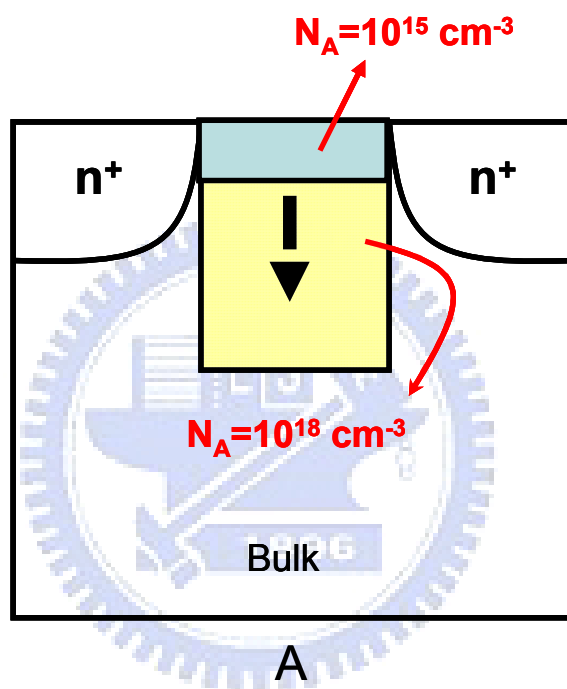


Fig. 4.2(a) A 4-nm-thick lightly doped layer ($N_A=10^{15}\text{cm}^{-3}$, background doping concentration) was placed on the substrate surface.

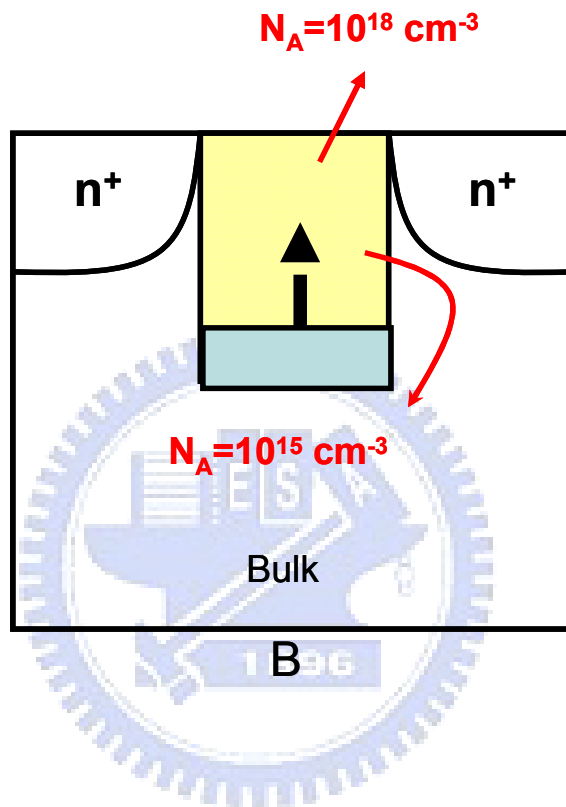


Fig. 4.2(b) We used a 4-nm-thick lightly doped layer to replace the heavily doped layer and increase its thickness from the bottom of depletion region to the substrate surface

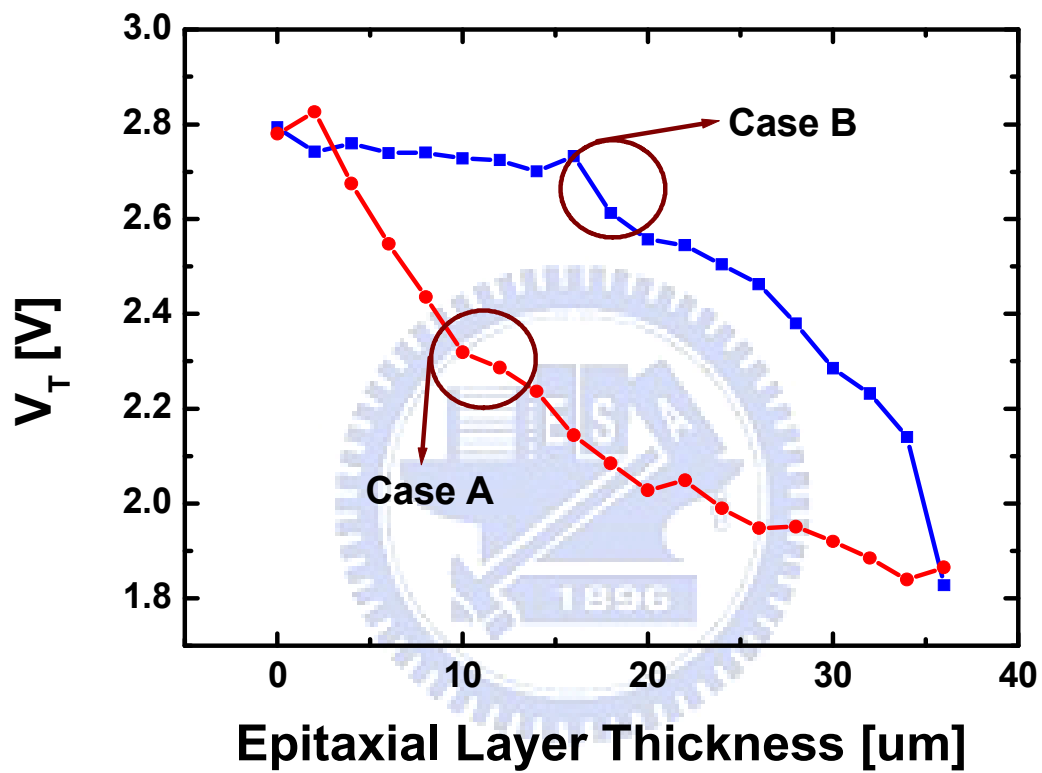


Fig. 4.3 The V_T dependence is on the lightly doped layer thickness.

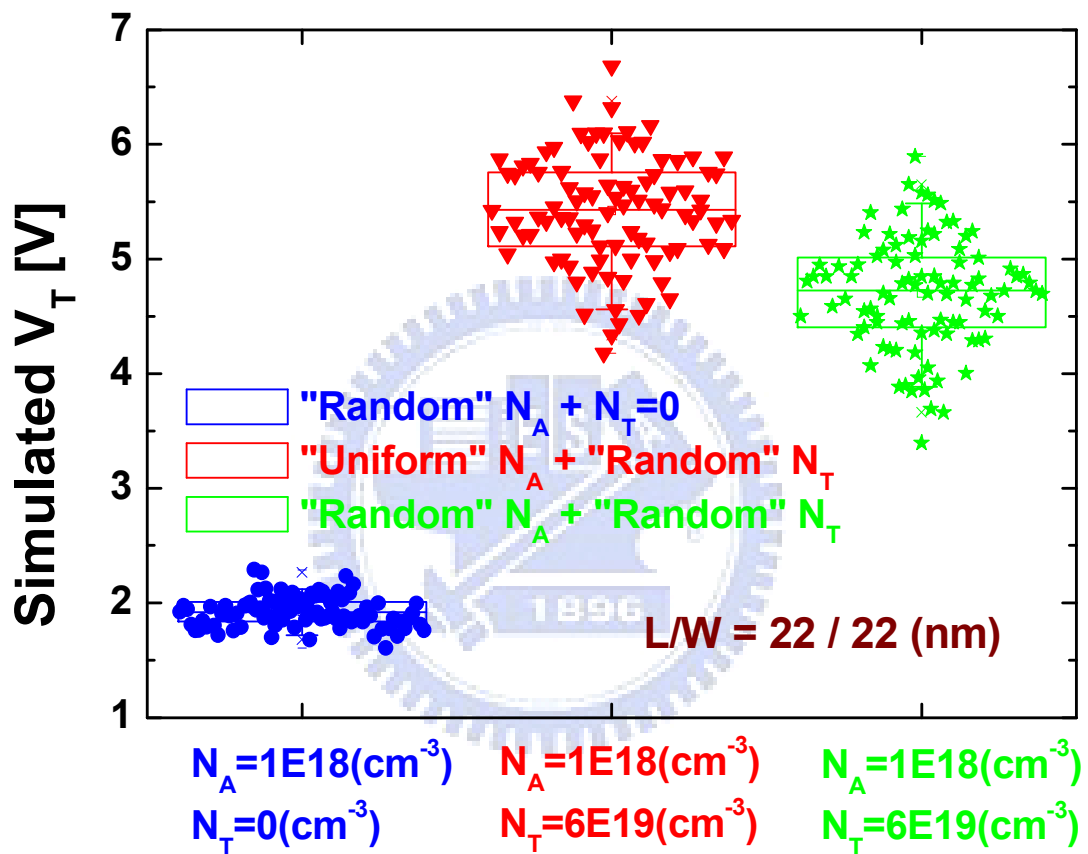


Fig. 4.4 the spread of V_T induced by random charge is higher than random dopant. It indicates the random charge effect is the main source in threshold voltage fluctuations.

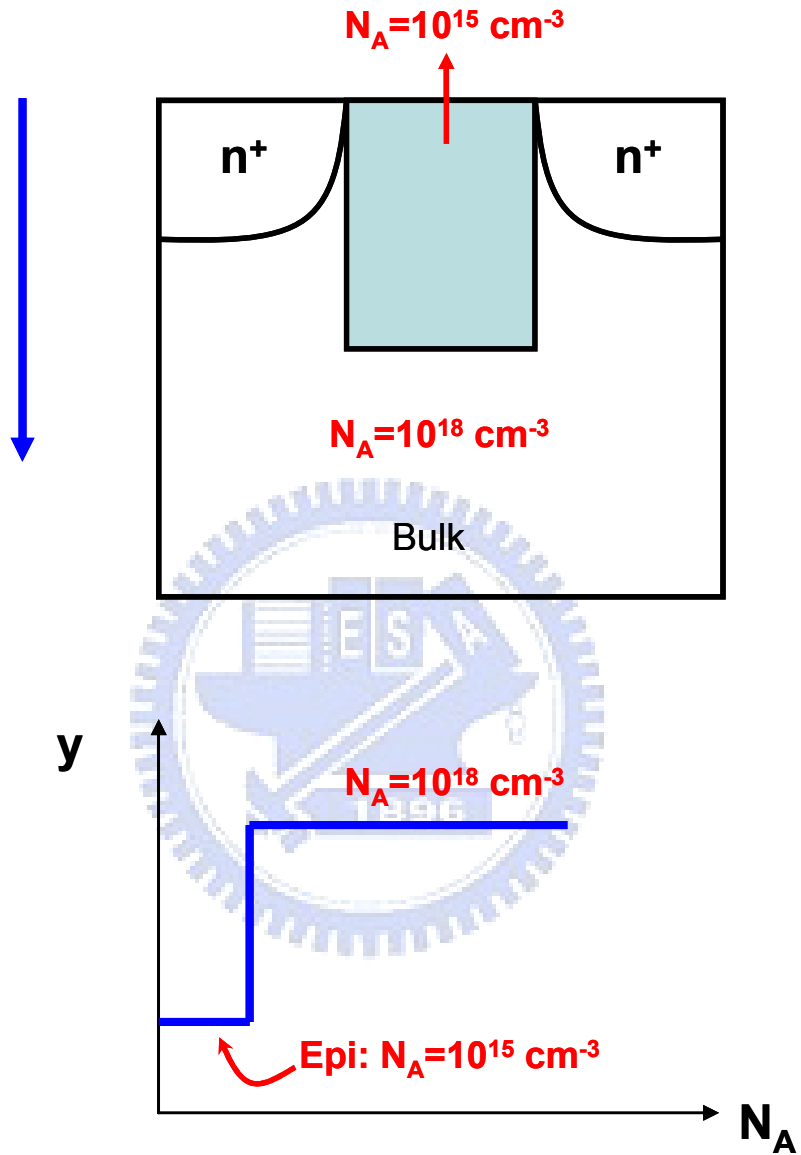


Fig. 4.5 Random dopant effect can be suppressed by epitaxial layer with lightly doped concentration.

	Random Dopant	Random charge with Random dopant
Conventional SONOS device	$\sigma V_T = 0.1319$	$\sigma V_T = 0.48903$
SONOS device with epitaxial layer	$\sigma V_T = 0.0916$	$\sigma V_T = 0.48204$

Fig. 4.6 The simulation results are compared with conventional random dopant effect.

Chapter 5

Conclusion

The correlation between programmed charges and threshold voltage (V_T) fluctuations are investigated on a SONOS device. Since the charges of such device are locally trapped in a nitride layer, the current path through the channel region differs from device to device from the statistics point of view and this will lead to deviation in V_T and dispersion in program window. The impact of various device parameters has been addressed in this thesis.

According to our simulation, we found that V_T fluctuations increase with decreasing in channel length and channel width under fixed amount of trapped charges (N_T). These results confirm that statistics problem becomes pronounced as device scales. The spreading of V_T s ($\sigma\Delta V_T$) becomes more serious as we increase the programmed charge density although the ratio between V_T and $\sigma\Delta V_T$ ($\sigma\Delta V_T/V_T$) is reduced. The increment of the choice of conduction paths from source to drain should be responsible for this phenomenon. Moreover, varying bottom oxide thickness shows more significant effect than changing top oxide thickness. Since surface potential is remotely controlled by trapped charges and a thinner bottom oxide means that a shorter distance from programmed charges to Si-surface, these charges certainly will show a stronger impact on the surface potential than those stored above a thicker oxide. In other words, even the total effective oxide thickness (EOT) does not change much during bottom oxide scaling, the V_T fluctuation is greatly affected. On the other hand, although reducing the top oxide thickness also reduces $\sigma\Delta V_T$, it is merely due to the reduction of EOT.

In addition, when random dopants are taken into account, the V_T variations become even worse. Our simulation results indicate that there is a positive correlation between random charge and random dopant on V_T fluctuations. This implies that the two factors are not

independent. By using the method described in [17], random dopant fluctuation can be suppressed by using an epi-taxial layer with a lightly doped Si surface concentration. However, random charge effect itself is still a main fluctuation source induced V_T spread.



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