

國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

利用 RTS 方法研究 SONOS 快閃記憶體  
寫入/抹除電荷之橫向分佈特性



**Characterization of Program/Erase Charge Lateral  
Distribution in SONOS Flash Memory Cell by Using  
RTS Technique**

研究生：趙元鵬

指導教授：汪大暉 博士

中華民國九十七年六月

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### 摘要

本篇論文主要提供了一個新的方法來探測小面積 SONOS 快閃記憶體沿著通道的表面電位變化，這個新方法是藉由結合缺陷位置萃取技術和底層二氧化矽缺陷所產生的隨機電報雜訊(Random Telegraph Noise)來達成。

我們使用這個新方法來驗證 SONOS 快閃記憶體中通道熱電子(Channel Hot Electron)的寫入電荷分佈和通道引發二次電子射入的電荷分佈之不同。此外，這個方法也被應用在觀察通道熱電子寫入和能帶到能帶穿隧產生之熱電動(Band-to-Band Tunneling Hot Hole)抹除電荷分佈的不對稱現象。最後，高溫下氮化矽中的正電荷遷移也有利用此方法研究。

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The main concept of this dissertation provides a new method to probe the change of the surface potential along the channel in a small area SONOS type memory. It is accomplished by combining the extraction of the trap position with the random telegraph signal (RTS) resulted from the interface trap located in the bottom oxide. This method is used to verify the difference of the program charge distribution between channel hot electron (CHE) and channel initiated secondary electron (CHISEL) injection. Moreover, this method could be applied to observe the charge misalignment of CHE program and band-to-band tunneling

(BTBT) hot hole erase. The migration of the positive charge in the nitride layer is also inspected as well.



## 謝誌

本篇論文完成，首先要感謝指導教授汪大暉教授。汪大暉教授提供了良好的實驗儀器及研究環境，使我們可以進行許多先進元件的研究。他紮實且深入的研究訓練，加上嚴謹的研究態度，讓我獲益良多。

再來最需要感謝的就是指導我實驗的馬煥淇學長。在實驗做不出來的時候，給我明確的方向，也教了我做實驗的方法與態度。另外還要感謝實驗室的小鄭、DaDa、阿雄和阿多肯學長給予我生活上和學業上的意見，在我剛進實驗室時，幫助我融入這個實驗室。同屆的彥君、佑亮、小熊、還有子華，感謝他們在我失意的時候，都能在我身邊給予我精神上的支持。最後還有學妹阿杜和莊 group 的同學們，讓我的研究生生活，除了嚴肅的學術研究外，還多了許多歡樂。

最後要感謝我的父母、家人，在求學期間給我的鼓勵和支持，有了他們經濟上支持，無怨無悔的付出與關心，才能讓我完成我的碩士學位。

2008. 4

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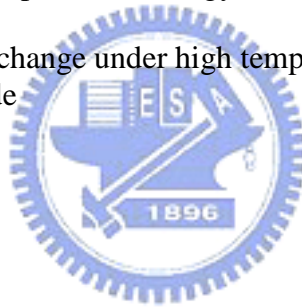
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# Chapter I

## Introduction

Nowadays, flash memories are widely used in personal computers and electronic products. Due to the non-volatile property, the data can be stored, erased and read from the devices for many times and the data will not be lost after the power is off. Nevertheless, with recent advances in VLSI processing, we have reached the point at which the effect of a single electron on a typical device can be quite significant. While such effects will eventually cause fundamental scaling and reliability problems, parallel advances in physics have helped create opportunities for extracting new kinds of information about VLSI devices by observing single-electron trapping effects.

In this thesis, channel hot electron (CHE) is used to program the memory cell, and with the random telegraph signal (RTS) resulted from the interface trap in the bottom oxide[1.1][1.2], the surface potential variation in the vicinity of the trap could be investigated during programming. Next, accompanied with the trap position extraction technique[1.3], the surface potential change can be known at a specific position along the channel. Besides, this method may also be utilized to observe the channel surface potential change of the devices in other applications.

There are five chapters in this thesis. Chapter 1 is Introduction and we would give a brief outline of the dissertation. In Chapter 2, the RTS mechanism is reviewed and the trap position extraction idea will be explained. In Chapter 3, the experimental process and result of probing the channel surface potential throughout CHE programming will be described, and next, other applications will be shown in Chapter4. Finally, the summary and conclusion will be given in Chapter5.

# Chapter 2

## Random Telegraph Signal Mechanism and Trap Position Extraction

### 2.1 Introduction

Trapping of a single carrier charge in defect states near the Si/gate dielectric interface and related local modulation in carrier density and mobility will have a profound effect on the drain current in such devices. Current fluctuations on such a scale will become a serious issue, not only as a source of excessive low-frequency noise in analog and mixed-mode circuits, but also in dynamic random access memory and static random access memory and other digital application.

Depending on the device geometry, a single or few discrete charges trapped in hot carrier, radiation or bias temperature stress created defect states will be sufficient to cause significant performance degradation in nanometer scale SONOS flash memories. For devices with very small channel area, it is possible to have only one oxide trap in the vicinity of surface Fermi level over the entire channel. Thus, individual traps can be observed in their neutral or charged state and the current fluctuation between two discrete levels. The study of random telegraph signal (RTS) noise in submicron MOS transistors offers the unique opportunity of studying the trapping/de-trapping behavior of a single interface trap.

### 2.2 RTS Theory

Fig. 2.1 displays a typical time domain trace of the drain current illustrating the three main RTS parameters. In small enough devices, normally, only trap energy level

within a few  $kT$  from the Fermi level would make current fluctuation where  $k$  and  $T$  are the Boltzmann's constant and equilibrium temperature, respectively. Traps with energy levels several  $kT$  below the Fermi level would be permanently filled while traps with energy levels several  $kT$  above the Fermi level would be permanently empty, resulting in negligible noise power.

Up to now, the discrete change in current has generally been modeled as the superposition of two effects that occurs when the trap changes its state: the effect of number fluctuation of free channel carriers  $\Delta N$ , and the mobility fluctuation  $\Delta\mu$  described as [2.1][2.2]:

$$\frac{\Delta I_d}{I_d} = \frac{\Delta N}{N} \pm \frac{\Delta\mu}{\mu} = -\frac{1}{W \cdot L} \left[ \frac{1}{N} \pm \alpha\mu \right] \quad \text{Eq (2.1)}$$

in strong inversion. Here,  $N$  is the channel carriers per unit area. It is assumed that the mobility is limited by oxide charge scattering with a coefficient  $\alpha$ . The sign in front of the mobility fluctuation is determined by the type of the trap, i.e., a repulsive or an attractive scattering center. For an acceptor trap, the high level corresponds to the trap in a neutral state while the low level corresponds to the negatively charged state. Therefore, the RTS are completely determined by the up and down times and its amplitude.

## 2-3 How to Use RTS Noise

RTS noise is characterized by three parameters: the average of the high ( $\langle \tau_e \rangle$ ) and low ( $\langle \tau_c \rangle$ ) time constants and the magnitude of the current fluctuation ( $\Delta I_d$ ), which are also shown in Fig 2.1. The range of the time constants is from milli-seconds to seconds. Since there is an important relation between  $\langle \tau_c \rangle / \langle \tau_e \rangle$  and  $E_t - E_F$ :

$$\frac{\langle \tau_c \rangle}{\langle \tau_e \rangle} = g \exp\left(\frac{E_t - E_F}{kT}\right) \quad \text{Eq (2.2)}$$

where  $g$  is the degeneracy factor,  $E_t - E_F$  is the trap energy relative to the Fermi-level, and the trap is at the interface of the bottom oxide, we could use  $\langle \tau_c \rangle / \langle \tau_e \rangle$  to inspect the surface potential change as shown in Fig. 2.2.

## 2-4 Measurement of RTS Noise

Agilent-4155C was used for our measurements of small-area SONOS at room temperature. The sampling mode was selected, and the bias voltages ( $V_D$ ,  $V_G$ ) were well controlled so that the traps were kept in the vicinity of the Fermi level. With fast enough sampling rate, the current fluctuation would be extracted and shown on the screen of 4155C.

A program written by Fortran 6.0 was used to extract the capture time ( $\tau_c$ ) and the emission time ( $\tau_e$ ), which used the numbers of the points in the data from 4155C and the interval of any two points to compute the time constants. The whole measurement setup is shown in Fig. 2.3.

The capture time is sensitive to the concentration of the carriers in the channel under the trap, which is described as [2.3]

$$\tau_c = \frac{1}{n\sigma v_{th}} \quad \text{Eq (2.3)}$$

where  $n$  is the electron density in the channel under the trap,  $\sigma$  is the capture cross-section, and  $v_{th}$  is the thermal velocity. Therefore, as shown in Fig. 2.4 and Fig. 2.5, with the gate voltage increased, the capture time would be decreased due to the increased carrier concentration below the trap.

## 2-4 Extraction of the Trap Position

Before RTN is utilized to detect the potential variation in the channel, an important element is to find the location of the trap in the device. The method was proposed by IBM[1.3] which is based on the characteristic of linear voltage drop along the channel while operated in linear region. Thus, the applied drain voltage ( $V_{ds}$ ) affects the trap in a manner which depends on its position in the device. The experimental detail is described as below.

The devices used here are SONOS flash memories with a top oxide of 7nm, a nitride layer of 8.5nm and a bottom oxide of 6nm. The channel length (L) is  $0.1 \mu\text{m}$ , and the channel width (W) is  $0.1 \mu\text{m}$ .

First, a very small voltage is given (0.05V), which could almost be neglected, to the drain side, and the correlation between the capture time ( $\tau_c$ ) and gate voltage ( $V_g$ ) is measured, which is plotted in Fig. 2.6. Next, the drain voltage is increased to 0.3V also with the relation of capture time and  $V_g$  measured, and the result is shown in Fig. 2.6 as well. Note that the operations are all in the linear region. Since the capture time ( $\tau_c$ ) is dominated by the voltage drop between the gate and the channel right below the trap, the amount of the lateral shift of these two curves is equal to the voltage raised by the drain side at the point of the trap. Therefore, the following equation allows us to extract the trap position along the channel:

$$\frac{V_{ts}}{V_{ds}} = \frac{L_{ts}}{L_{ds}} \quad \text{Eq (2.4)}$$

where  $V_{ts}$  denotes the voltage raised at the trap position by the drain voltage and other meanings of the objects are specified individually in Fig. 2.7. For this case, the trap is at the position of  $0.2L$  to the source side, where L is the channel length. Another

example for the extraction of the trap position is given in Fig. 2.8.



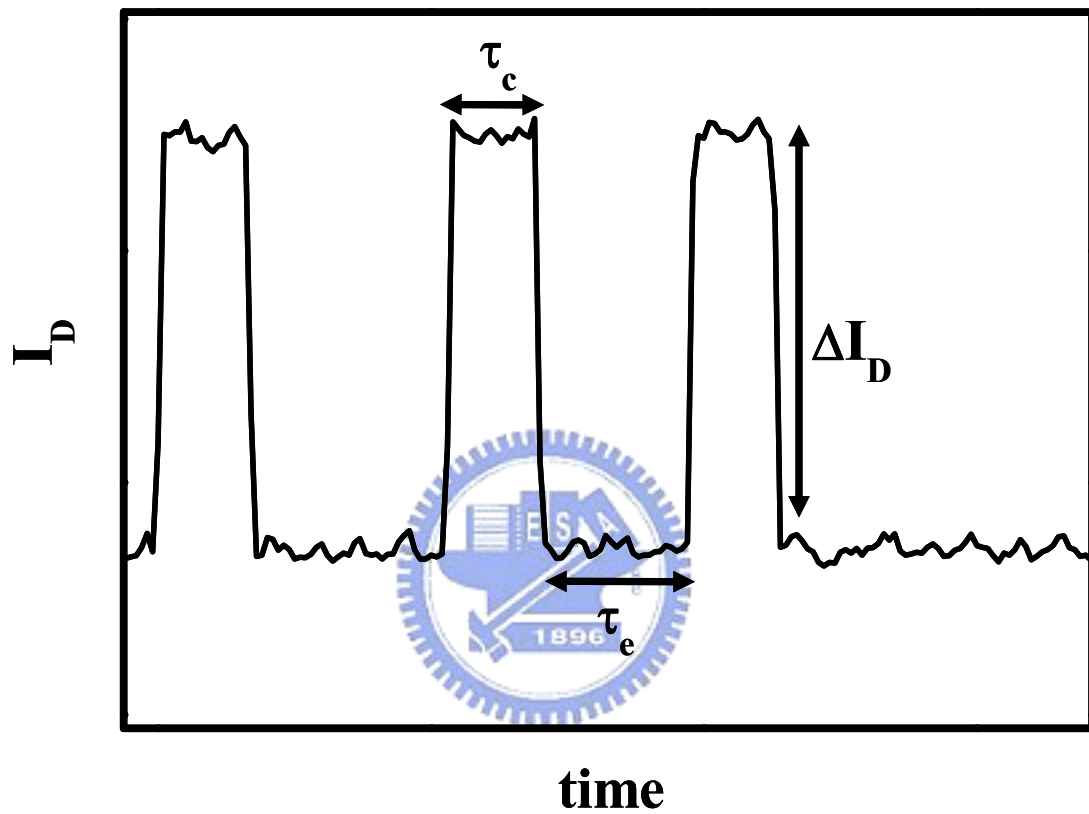


Fig. 2.1 Typical time domain plot of the drain current for RTS noise.

Illustration of the three major parameters of RTS noise.



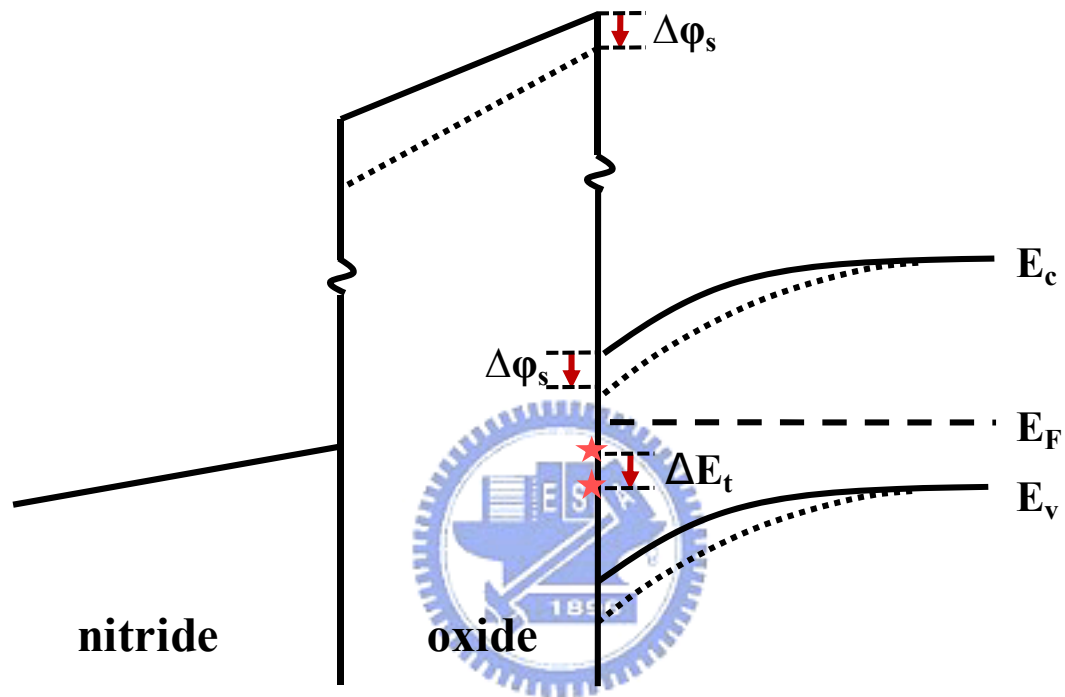


Fig. 2.2 The band diagram showing the energy change of the trap and the surface potential

$\langle \tau_c \rangle / \langle \tau_e \rangle$  can be used to investigate  $\Delta E_t$  and therefore  $\Delta \phi_s$

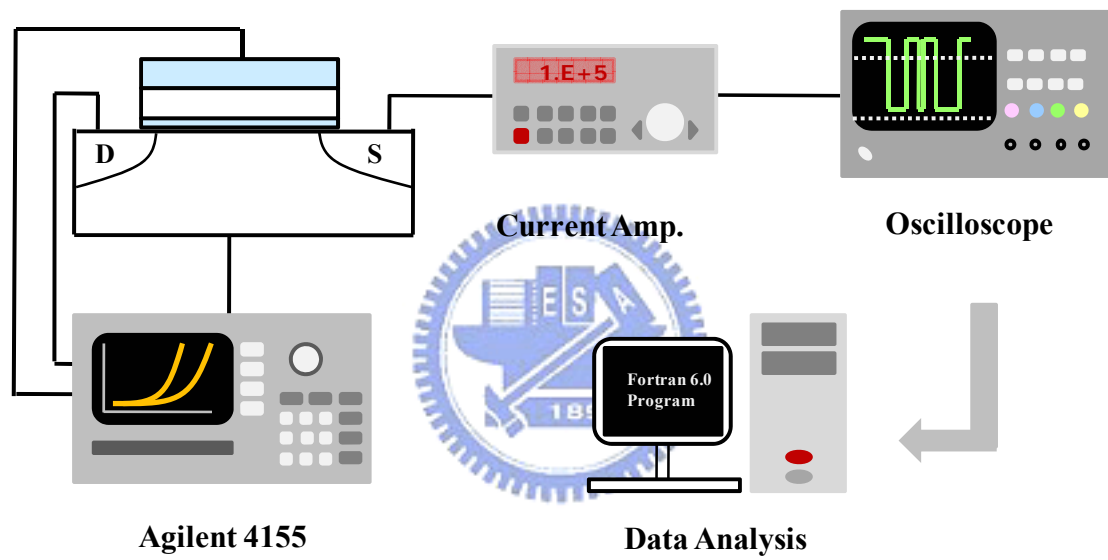


Fig. 2.3 The experimental setup for measuring RTS

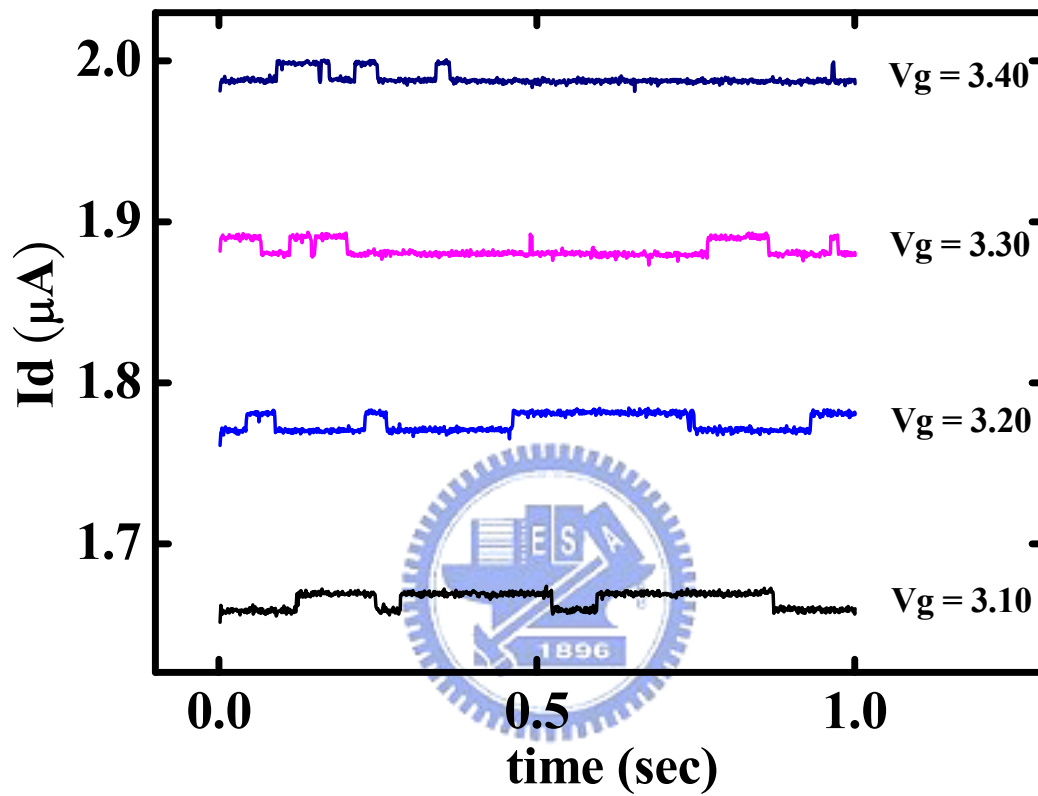


Fig. 2.4 RTN corresponding to different gate voltage.

A larger  $V_g$  makes the capture time ( $\tau_c$ ) shorter.

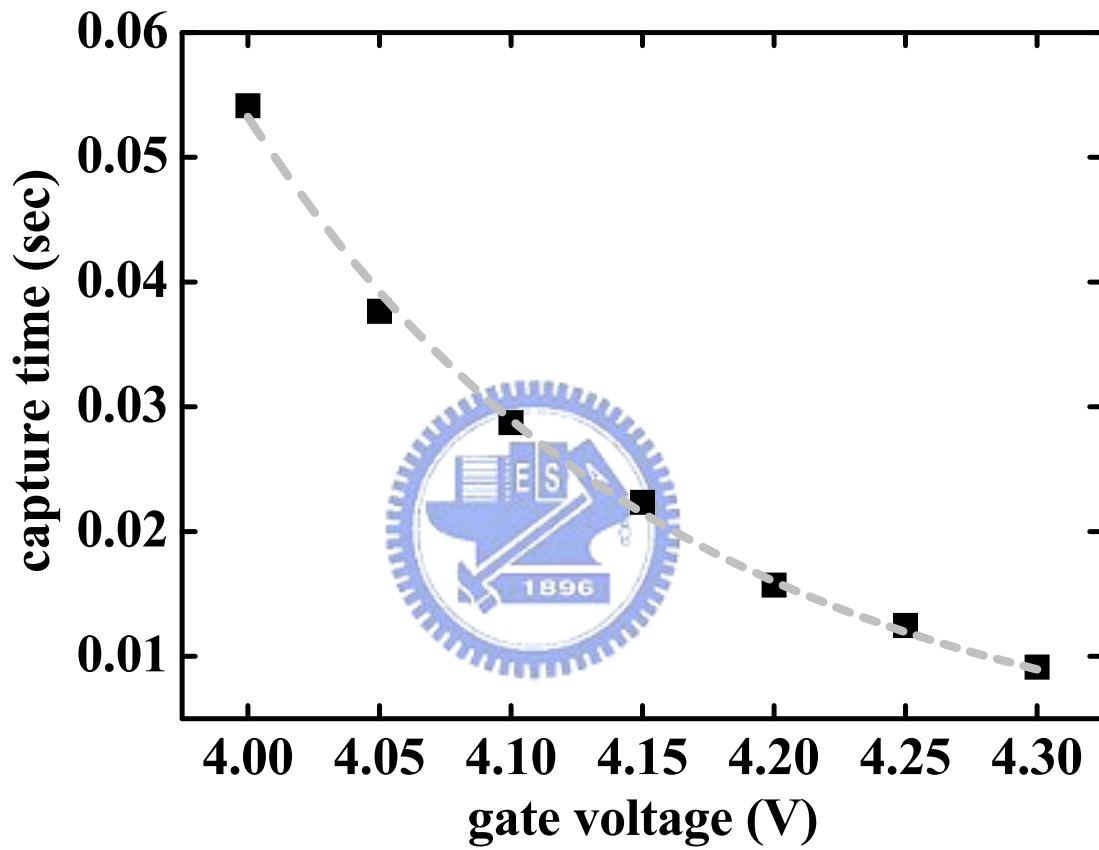


Fig. 2.5 Extracted capture time ( $\tau_c$ ) vs. gate voltage

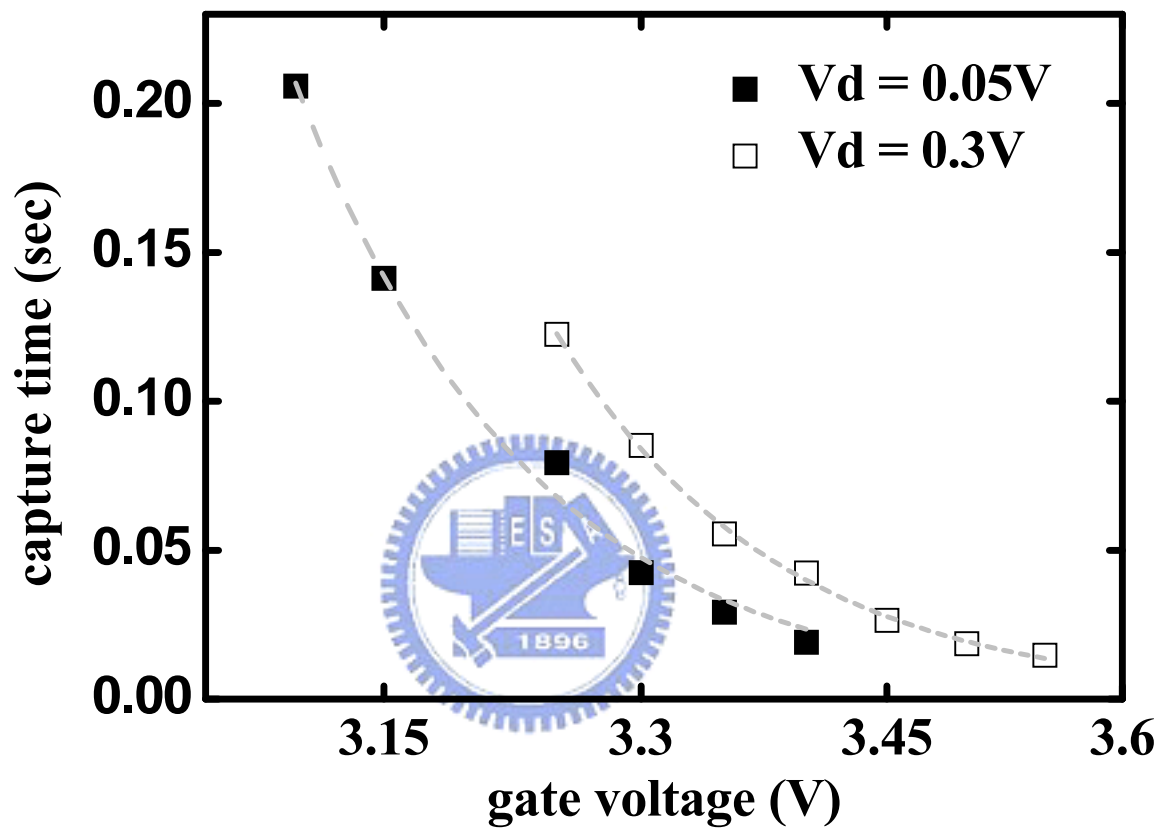


Fig. 2.6 Correlation of capture time and  $V_g$  at different drain voltage

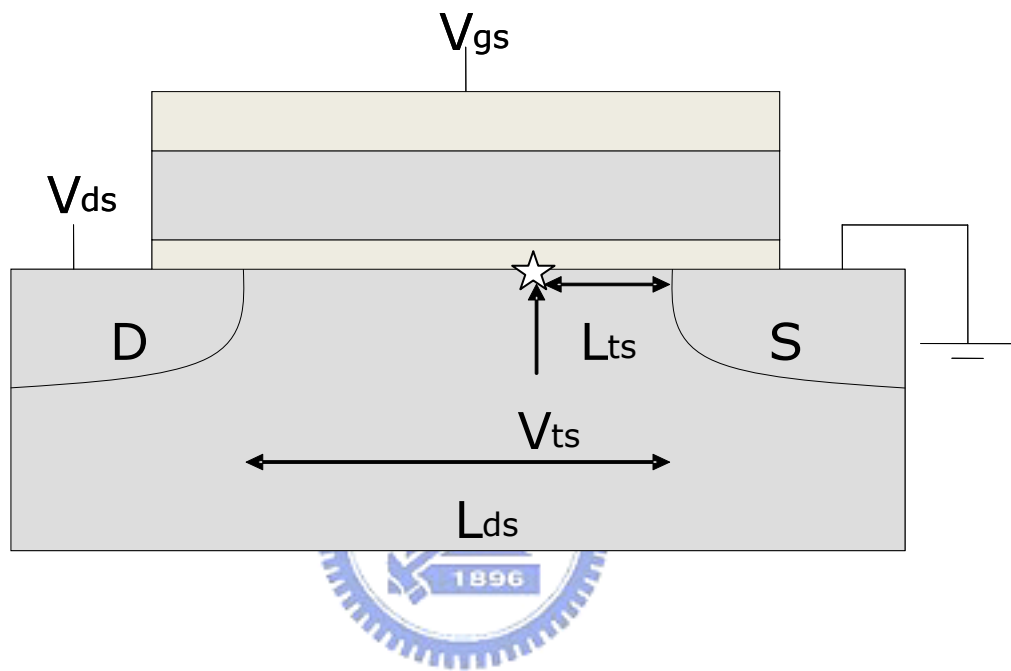


Fig. 2.7 Illustration of the objects meaning in trap position extraction

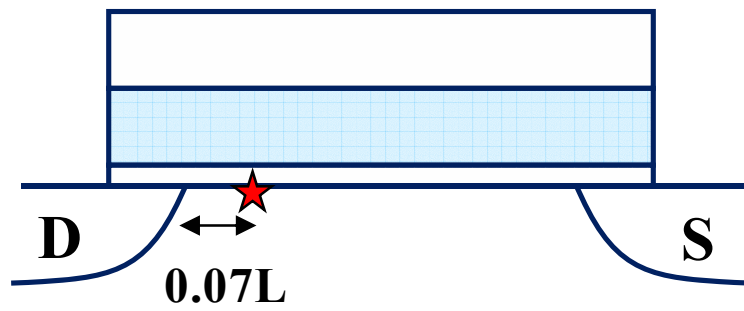
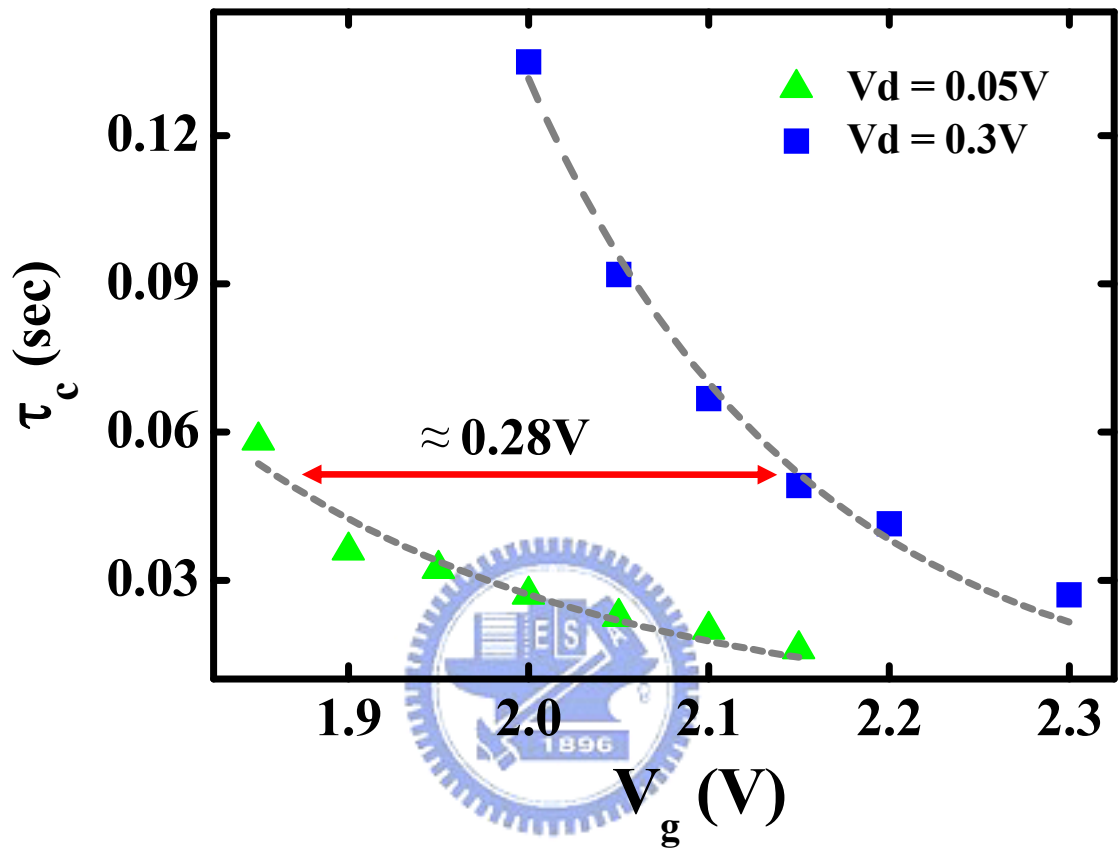


Fig. 2.8 Another example of the extraction of the trap position

# Chapter 3

## Inspection of Programmed Charge Lateral Distribution in SONOS Flash Memory Cell by Using RTS technique

### 3-1 Introduction

In two-bit operation, the control of programmed charge lateral distribution of each bit is a major concern for the scalability of the SONOS cell. Attempts have been made in the past to characterize the trapped charge distribution in a SONOS cell [3.1][3.2]. An inverse modeling approach is applied to extract programmed charge distribution from measured I-V curves [3.1]. This method has some drawbacks, such as lack of precise device doping and extensive numerical calculation. Charge pumping has been used widely to profile the charge distribution in a MOSFET device [3.3][3.4]. A modified charge pumping technique [3.5] is proposed to probe the lateral distribution of programmed charges at the source and drain junctions separately without computer simulation. However, when it comes to an ultra-small device, this method is not able to be utilized due to the ultra-small charge pumping current which could not be detected by the experimental instruments. Whereas RTN is very sensitive to the potential change around the trap, it provides an opportunity to make this mechanism useful to detect the surface potential variation throughout programming. The devices and measurement setup throughout this study will be described. The position of the trap along the channel will be extracted. The inspection of the channel surface potential change at a specific position will be demonstrated by this RTN method.



### 3-2 Devices Structure and Programming Conditions

The devices in our experiment are SONOS flash memories with a top oxide of 8.5nm, a nitride layer of 7nm, a bottom oxide of 6nm, a gate length of 0.1  $\mu$  m and a gate width of 0.1  $\mu$  m. The gate and drain voltages are 8V and 3.7V respectively during CHE programming with source and bulk grounded.

### 3-3 Surface Potential Change during CHE Programming

In order to detect one side of the surface potential change during CHE programming in a SONOS flash memory, the trap is needed to be located near the junction so that the program charge could be sensed by the trap. We conducted RTS measurement across the whole wafer and found few RTS events for later use. The trap we used is estimated to be at the position of 0.2L from the drain side where L is the channel length as plotted in Fig. 3.1. Due to the fact that the capture time is related to the electron density under the trap and the emission time is sensitive to the electric potential at the trap location owing to the average vertical electric field in the oxide [3.6][3.7]:

$$\langle \tau_c \rangle = \frac{1}{\sigma v n} \quad \text{Eq (3.1)}$$

$$\langle \tau_e \rangle = \frac{1}{\sigma v N_c} \exp\left(\frac{\Delta E_{CT}}{kT}\right) \quad \text{Eq (3.2)}$$

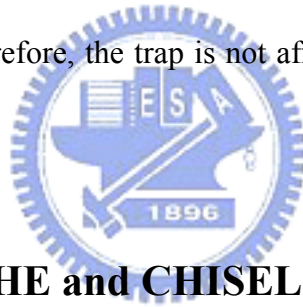
where  $N_c$  is the effective density of states in the conduction band and  $\Delta E_{CT}$  refers to the additional energy required to move the electron from the trap to the conduction band, it could be predicted that the capture time would increase and the emission time would decrease during the programming process. Our result is shown in Fig. 3.2,

which is quite similar to our prediction. Fig. 3.3 shows the variation of the capture time over the emission time ( $\tau_c / \tau_e$ ) during programming in which a conversion can be made into the surface potential change ( $\Delta E_t$ ) by Eq (3.3)[3.8] as shown in Fig. 3.4:

$$\frac{\tau_c}{\tau_e} = g \exp\left(\frac{E_t - E_F}{kT}\right) \quad \text{Eq (3.3)}$$

where  $E_t - E_F$  represents the trap energy relative to the Fermi level and  $g$  is the degeneracy factor which is equal to one in our case.

The other side has also been programmed, the source side in this case, to make a double confirmation that the trap is indeed located near the drain side. The result is shown in Fig. 3.5. It could be seen that the capture time remains almost constant during programming, and therefore, the trap is not affected by the program charge at the source side.



### 3-4 Comparison of CHE and CHISEL Programming

The program charge distribution in a flash cell is a crucial issue for two-bit operation scheme. It has been indicated in the previous simulations that the distribution of the program charge by channel initiated secondary electron (CHISEL) injection is different from CHE [3.9][3.10]. Therefore, utilizing our RTS method to observe the surface potential during programming by CHISEL has also been demonstrated as a comparison with the case programmed by CHE.

Each mechanism is illustrated in Fig. 3.6. It could be seen that the hole generated at the first impact ionization will flow to the bulk and results in a secondary impact ionization. The electron from the secondary impact ionization, accordingly, would be accelerated by the minus bulk voltage and be injected into the nitride layer.

It was reported that a wider program charge distribution is observed in CHISEL mechanism and the way of CHE has a narrower distribution [3.11] as shown in Fig. 3.6. Thus, it can be predicted that the capture time would be raised more rapidly in CHISEL than in CHE programming method if the trap is assumed to be not too close to the junction. The trap in this case is at the position of  $0.2L$  from the drain side, which is located at a little distance from the junction.

The programming condition of CHISEL is 4V to the gate, 3.3V to the drain, -2V to the bulk with source grounded, and the device we used is the same as the one in CHE experiment previously. The results are shown in Fig. 3.7, and it could be seen that the capture time over the emission time certainly increases more quickly as programmed by CHISEL than CHE. Consequently, the difference of program charge distribution between CHE and CHISEL is verified again with our RTS method.



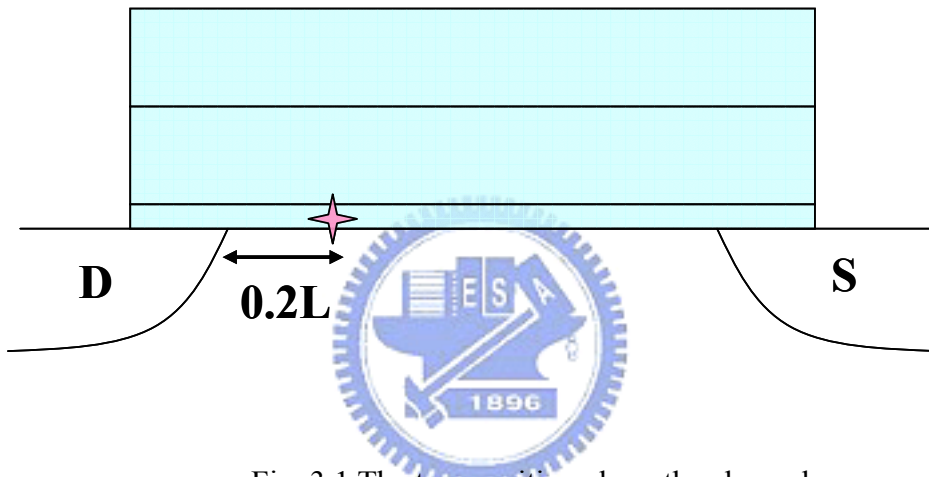


Fig. 3.1 The trap position along the channel

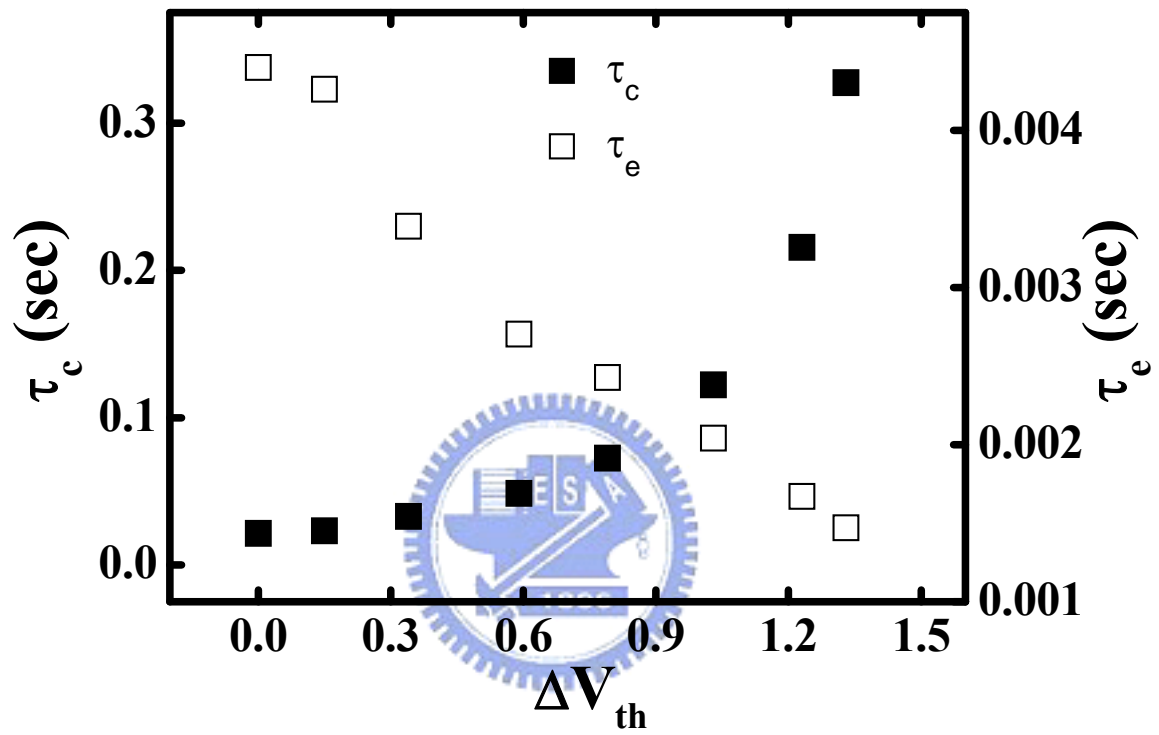


Fig. 3.2 The capture time and emission time after programming

The measuring condition is  $V_g = 6V$ ,  $V_d = 0.1V$ .

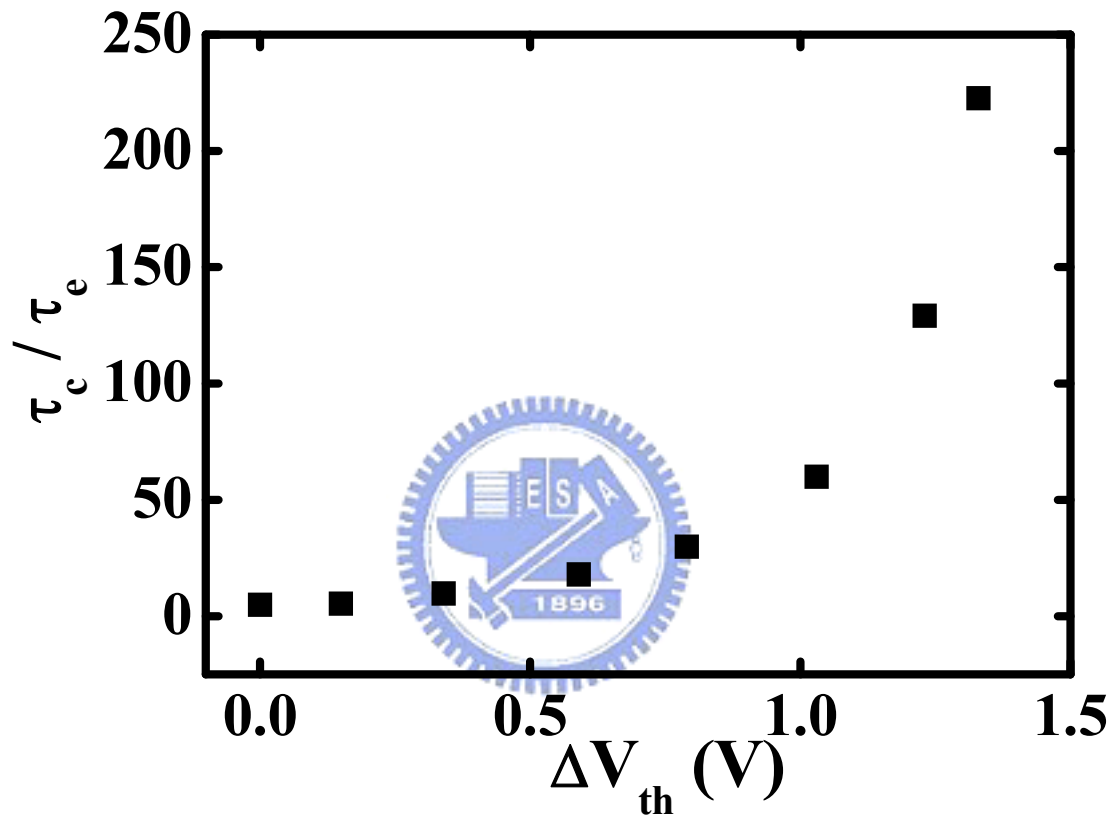


Fig. 3.3 The variation of capture time over emission time after programming

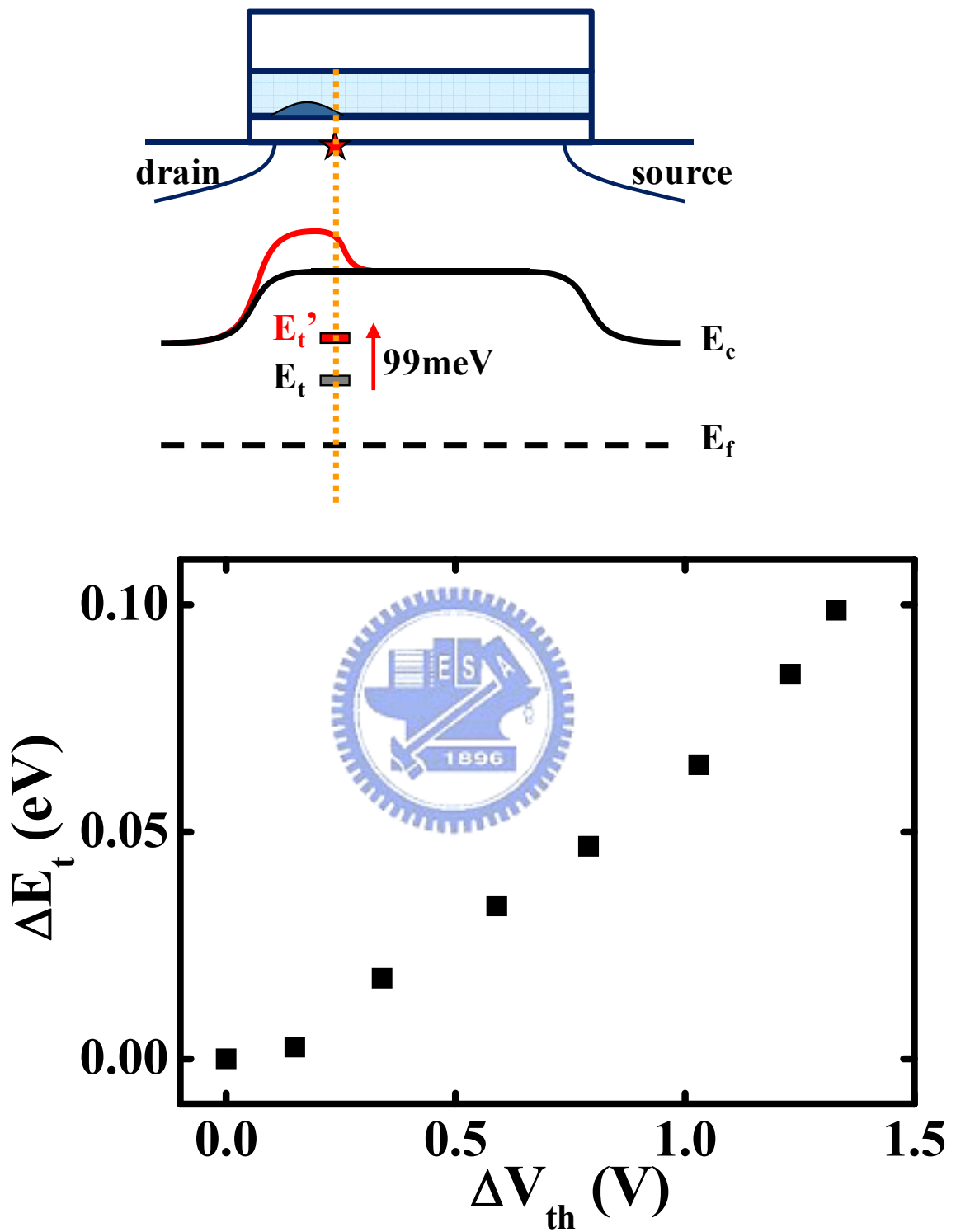


Fig. 3.4 The change of surface potential after programming

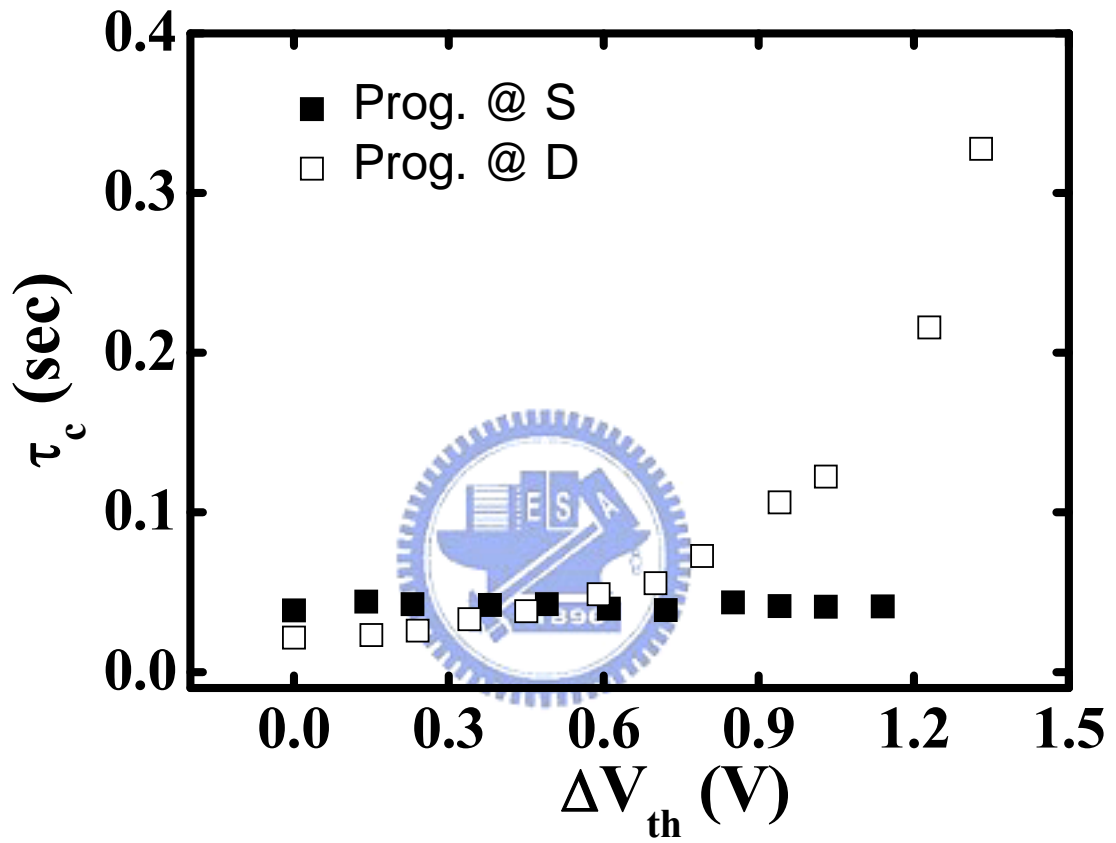


Fig. 3.5 Capture time after programming at different side



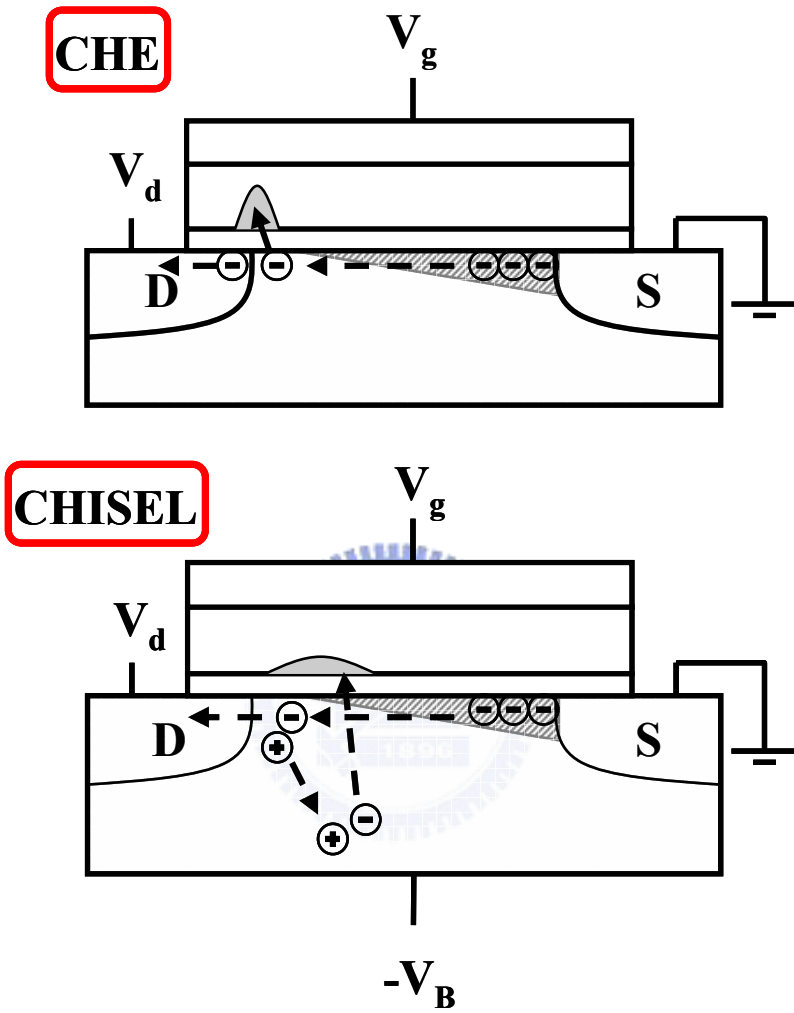


Fig. 3.6 Illustration of CHE and CHISEL mechanisms

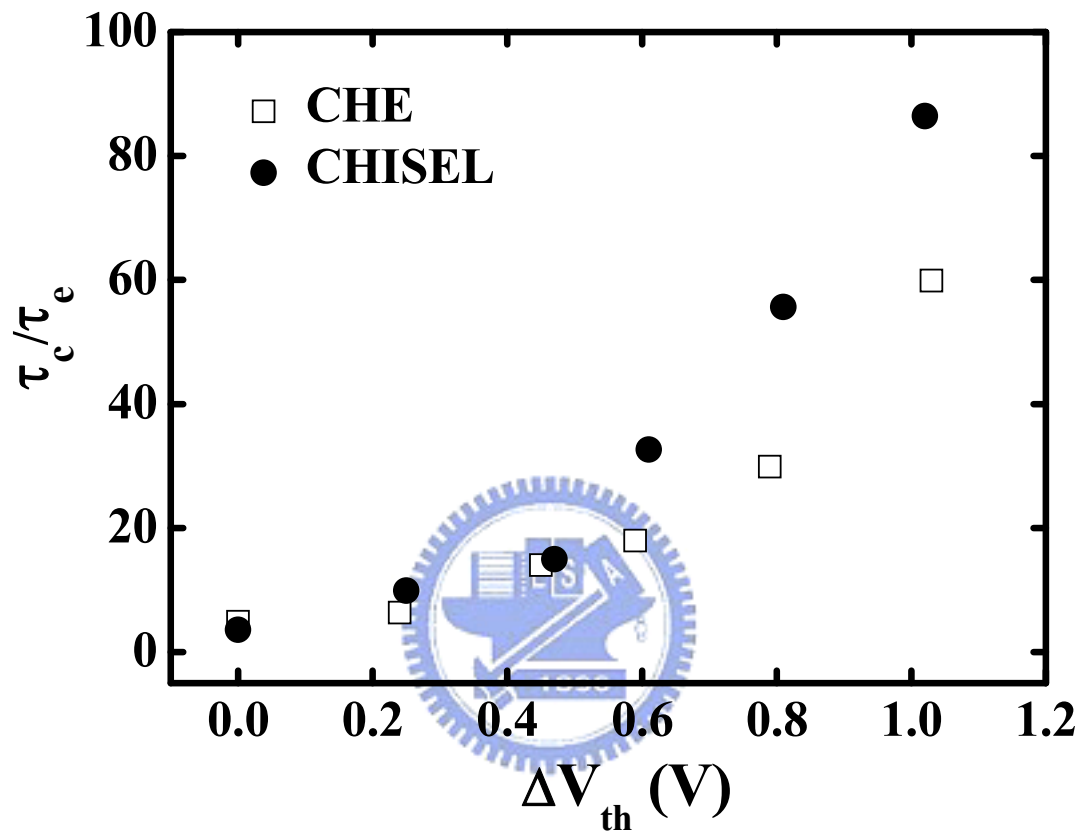


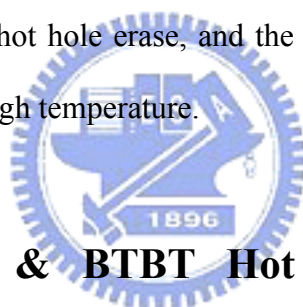
Fig. 3.7 The variation of capture time after programming by CHE and CHISEL

## Chapter 4

# Other Applications Utilizing Individual Traps as Internal Probes

### 4-1 Introduction

Inasmuch as the trap is very sensitive to the change of local potential, it could be applied to detect the surface potential variation at a specific position along the channel. In this chapter, two other applications with our method employed are introduced. One is the observation of the charge misalignment between CHE program and band-to-band-tunnel (BTBT) hot hole erase, and the other is the investigation of the hole lateral migration under high temperature.



### 4-2 CHE Program & BTBT Hot Hole Erase Charge Misalignment

In SONOS flash memories, the misalignment between program and erase charge has been studied for the last few years, which could lead to a reliability issue as charge accumulating around the junction [4.1]. No matter using the charge pumping or the Monte Carlo simulation method, it has been indicated in previous works that BTBT hot hole erase has a narrower charge distribution, i.e., closer to the junction, and the distribution of CHE program is wider as depicted in Fig. 4.1.

The devices in our experiment are SONOS flash memories with a top oxide of 85Å, a nitride layer of 70Å, a bottom oxide of 60Å, a gate length of 0.1  $\mu\text{m}$  and a gate width of 0.1  $\mu\text{m}$ . The programming condition is the same as before which is 8V

to the gate, 3.7V to the drain with source and bulk grounded. The condition for BTBT hot hole erase is chosen to be -4V to the gate, 5V to the drain with source and bulk grounded.

Utilizing the trap position extraction technique, the locations of the traps used in this experiment are shown in Fig. 4.2(a) and Fig. 4.3(a), which are at the position of 0.3L and 0.05L from the drain side respectively. Since the charge injected by BTBT hot hole erase has a narrower distribution, it could be predicted that only the region in the vicinity of the junction could be affected by the injected charge. Therefore, as a result, the potential change induced by the injected charge could only be sensed by the trap at the position of 0.05L from the drain side. On the contrary, the program charge injected by CHE with a wider distribution could affect the area further from the junction, and thus, the potential change could be sensed by both two traps at different positions as shown in Fig. 4.2(b) and Fig. 4.3(b).

Fig. 4.4 and Fig. 4.5 show the shift of the trap relative energy ( $\Delta E_t$ ) of the two traps during program and erase. It could be seen clearly that both the program and erase charge are sensed by the trap closer to the junction (0.05L to the drain side). However, only the program charge was sensed by the trap at a further position from the junction (0.3L from the drain side). Therefore a wider charge distribution of CHE program is verified again.

### **4-3 Hole Lateral Migration**

The negative threshold voltage ( $V_t$ ) shift of a nitride storage flash memory cell in the erase state will result in an increase in leakage current. By utilizing a charge pumping method, it has been reported that the lateral migration of trapped holes is responsible for this  $V_t$  shift due to the channel shortening[4.2]. Also the temperature

dependence of the hole migration has been pointed out. In this section, the lateral movement of the positive charges will be monitored by our RTN method through the surface potential variation sensed by the trap.

In Fig. 4.6(a), the trap position is extracted by the method proposed in Chapter 2, which is at the position of  $0.1L$  from the drain side. Since the trap is quite close to the junction, it is expected that the potential change would be sensed immediately by the trap as the holes are injected into the nitride layer as shown in Fig. 4.6(b). Accompanied with the heating time, the lateral migration of the holes will result in a less effect of positive charge on the trap as in Fig. 4.6(b) as well. Therefore the relative trap energy is predicted to be increased because of the less positive charge right above the trap.

The devices we used in this experiment are SONOS flash memories with a top oxide of 8nm, a nitride layer of 6nm, a bottom oxide of 3nm, a gate length of  $0.1 \mu\text{m}$  and a gate width of  $0.065 \mu\text{m}$ . The erase condition is a gate voltage of -5V and a drain voltage of 4V with source and bulk grounded for 30 millisecond. The temperature is controlled to be under  $85^\circ\text{C}$ .

The results are shown in Fig. 4.7, and we could see that the relative trap energy ( $\Delta E_t$ ) increases with the heating time which is in agreement with what we have predicted. It is also noted that  $\Delta E_t$  changes quickly at the beginning and becomes stable after about 10 minutes which indicates that the holes move fast at the very start but almost stop migrating in the end.

Another case is shown in Fig. 4.8(a) in which the trap is at a longer distance from the junction ( $0.25L$ ). We could first predict that there would be a different outcome of this situation based on Fig. 4.8(b). The result is depicted in Fig. 4.9, and the surface potential decreases instead of increasing as the former case.

A comparison is also made that electrons are barely moving under high

temperature as shown in Fig. 4.10 in which the trap is located at the source junction.



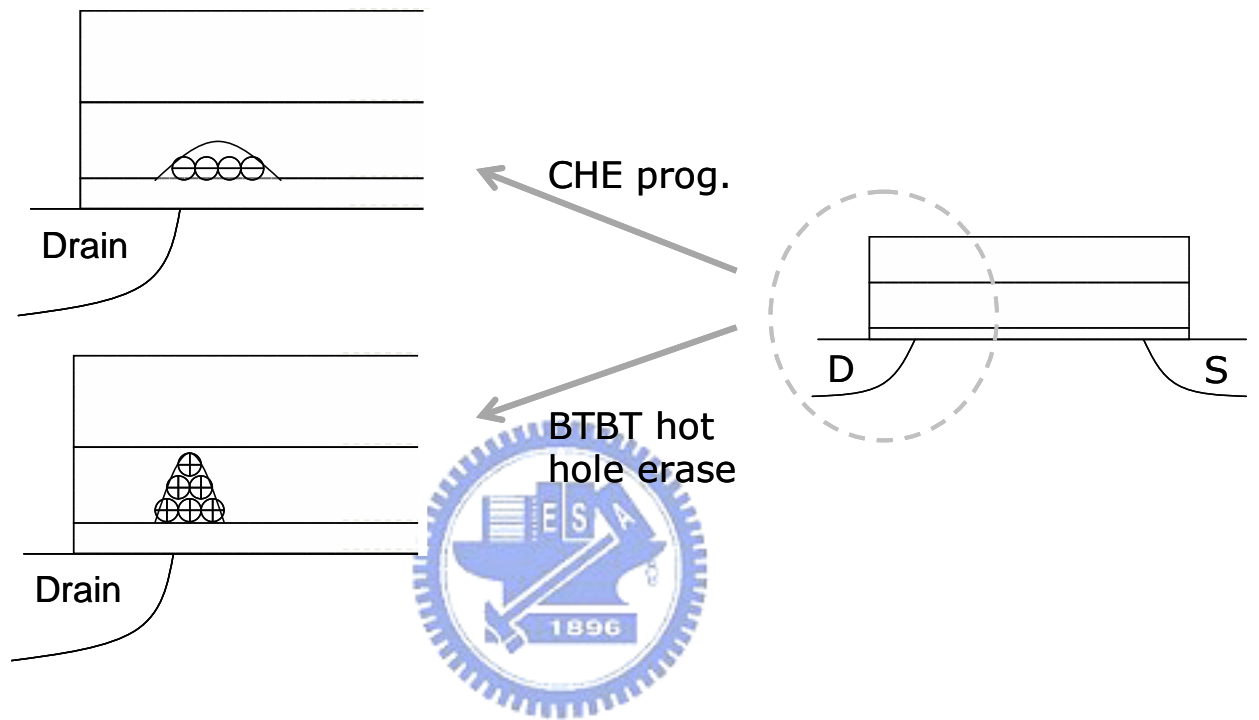


Fig. 4.1 The charge distribution of CHE program and BTBT hot hole erase

The distribution of electrons is wider than the distribution of holes.

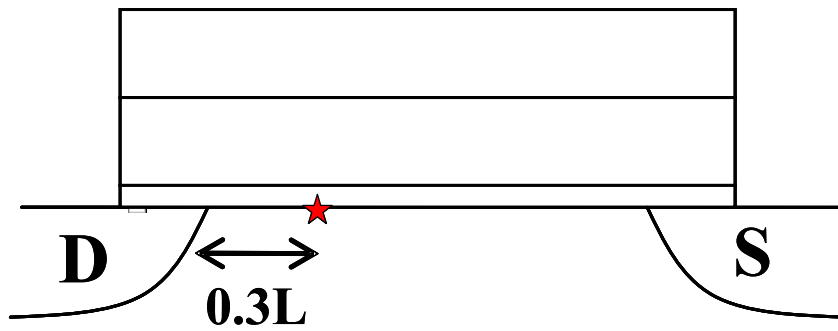


Fig. 4.2(a) The position of the trap used in charge misalignment

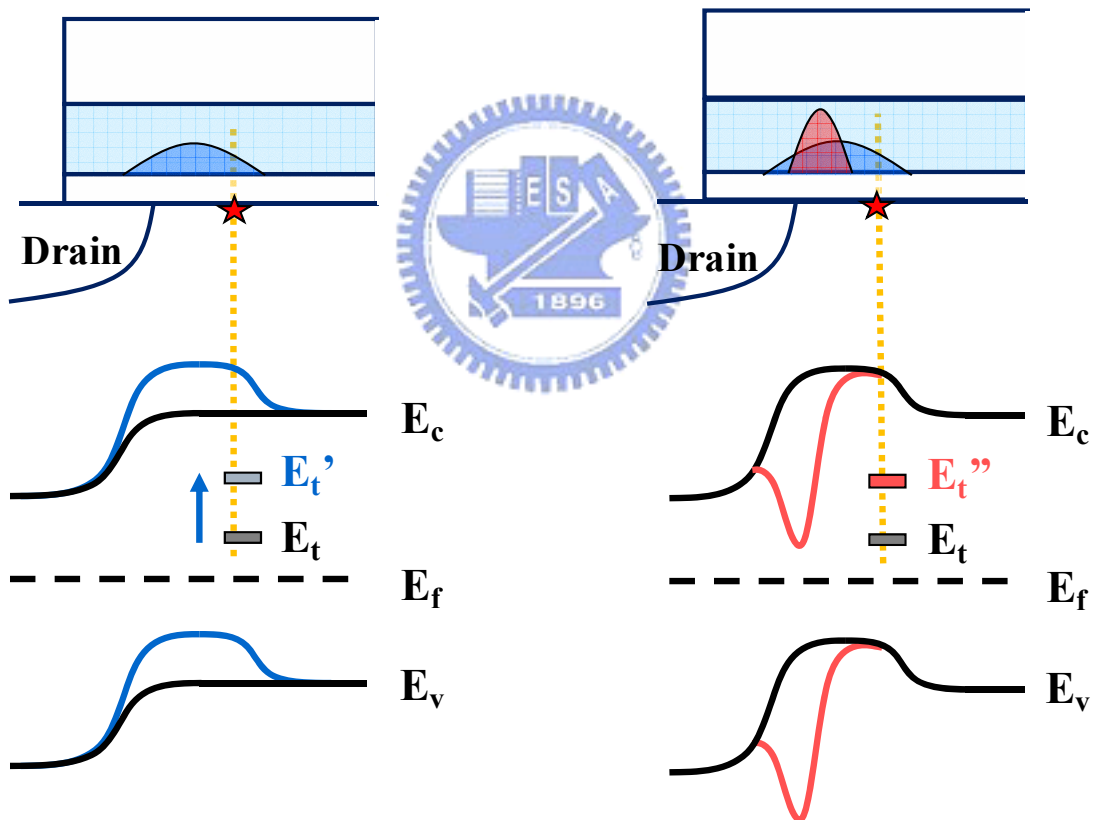


Fig. 4.2(b) The prediction of the surface potential variation during program and erase



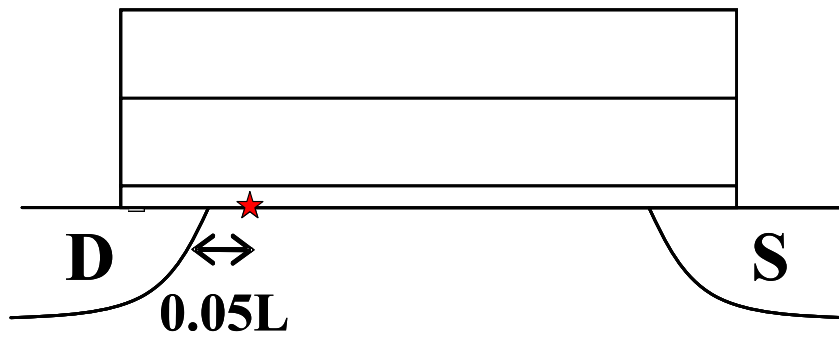


Fig. 4.3(a) The position of the other trap used in the experiment

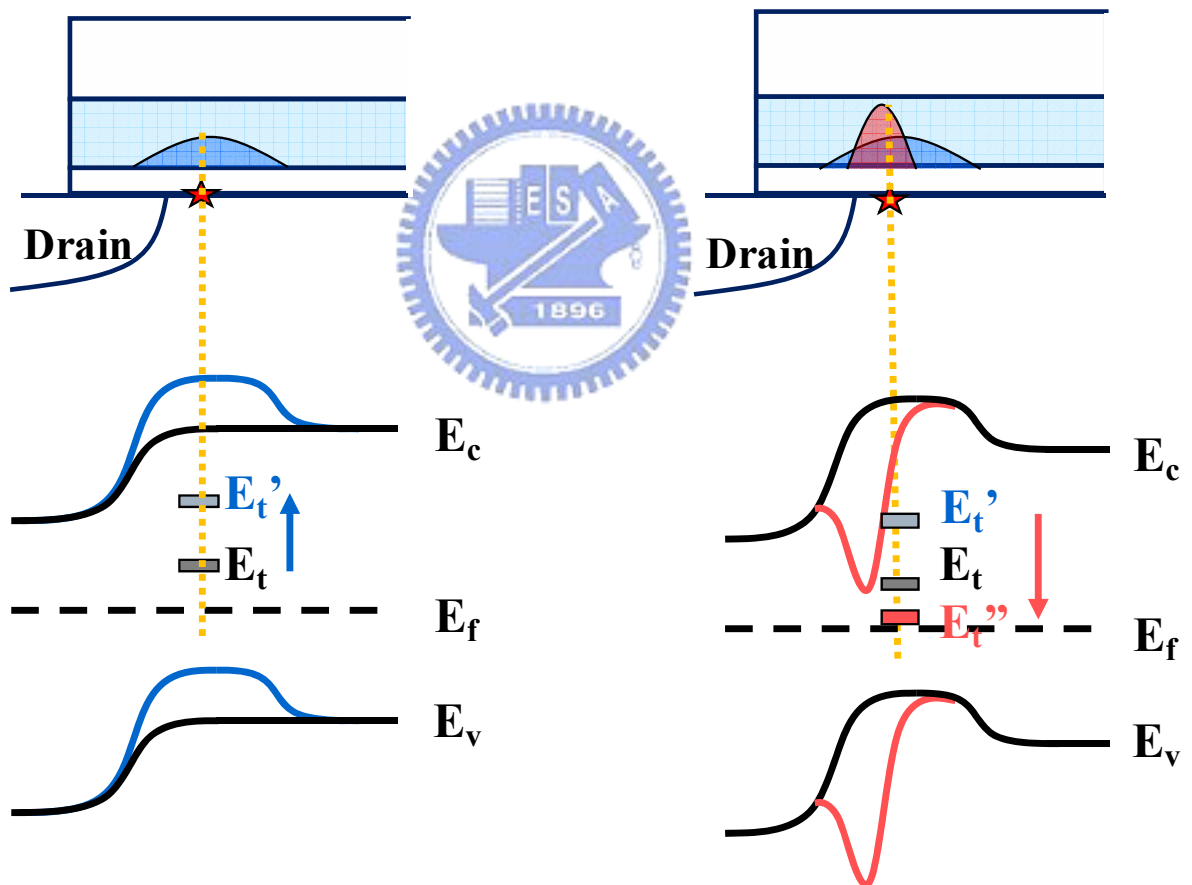


Fig. 4.3(b) The prediction of the surface potential variation during program and erase

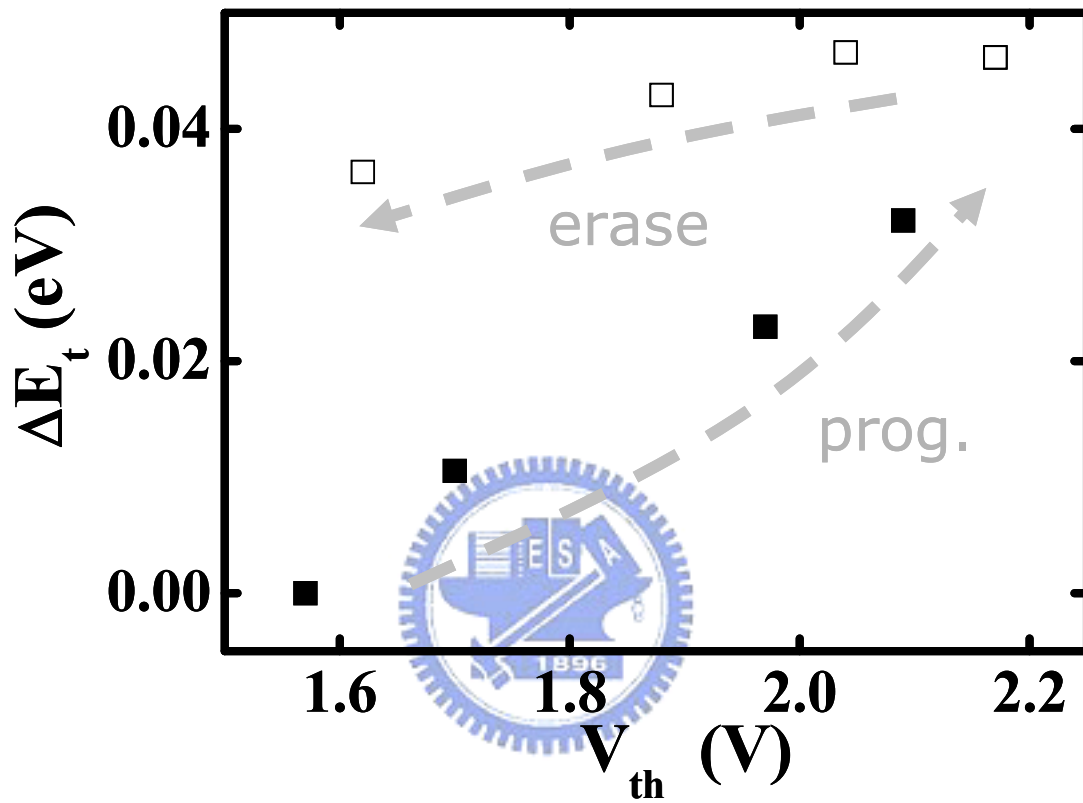


Fig. 4.4 The relative energy of the trap at 0.3L from the drain during program and erase

$\Delta E_t$  is not reversible in this case.

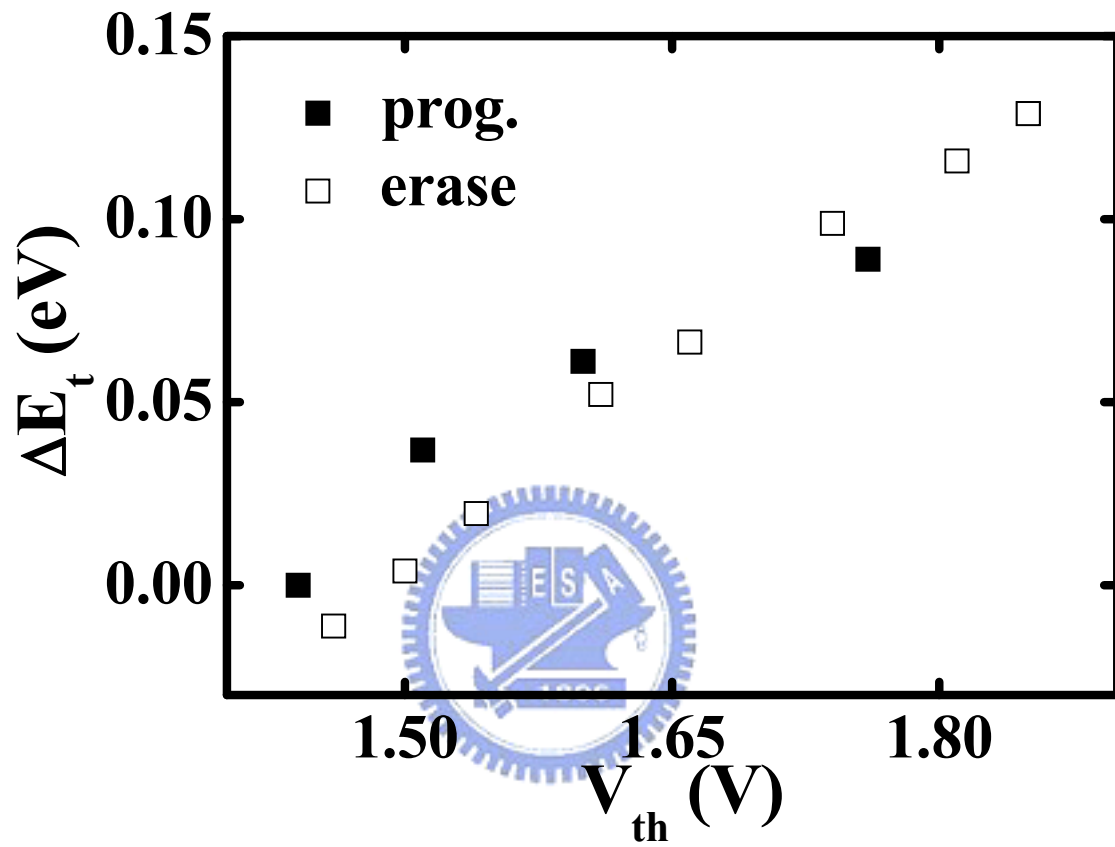


Fig. 4.5 The variation of the relative energy of the trap at 0.05L from the drain side

$\Delta E_t$  is reversible in this case.

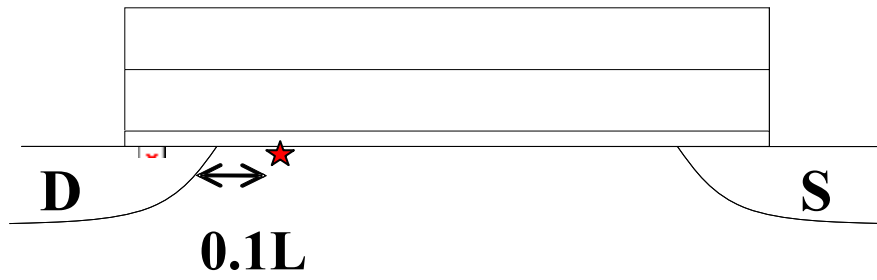


Fig. 4.6(a) The extraction of the trap position used in hole migration experiment

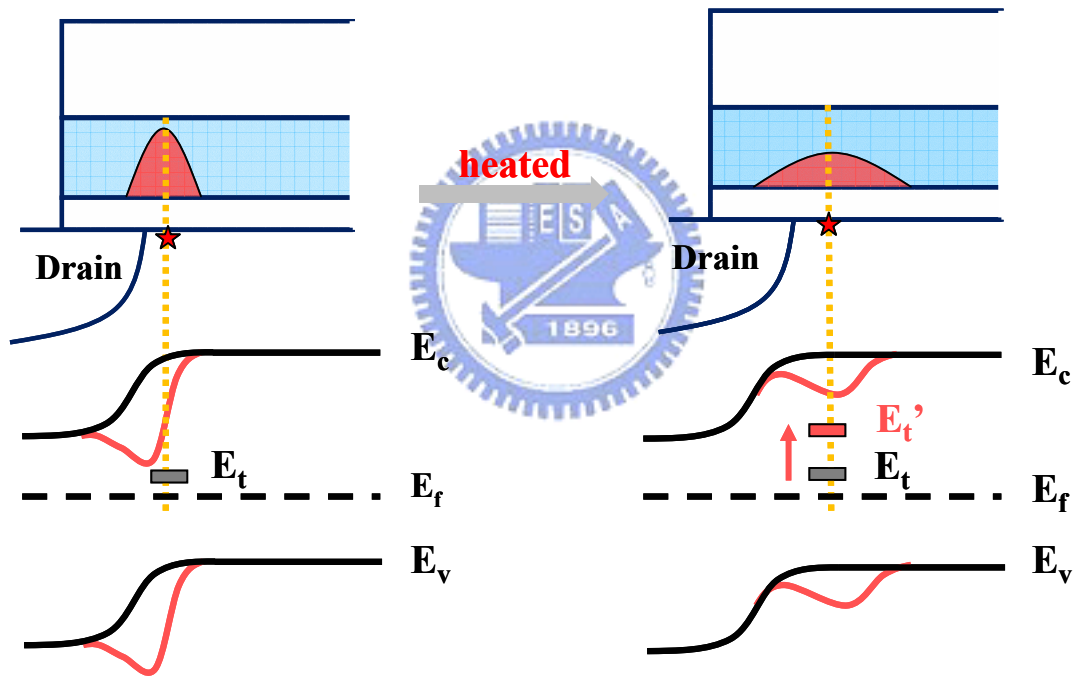


Fig. 4.6(b) The hole distribution and band diagram before and after heating

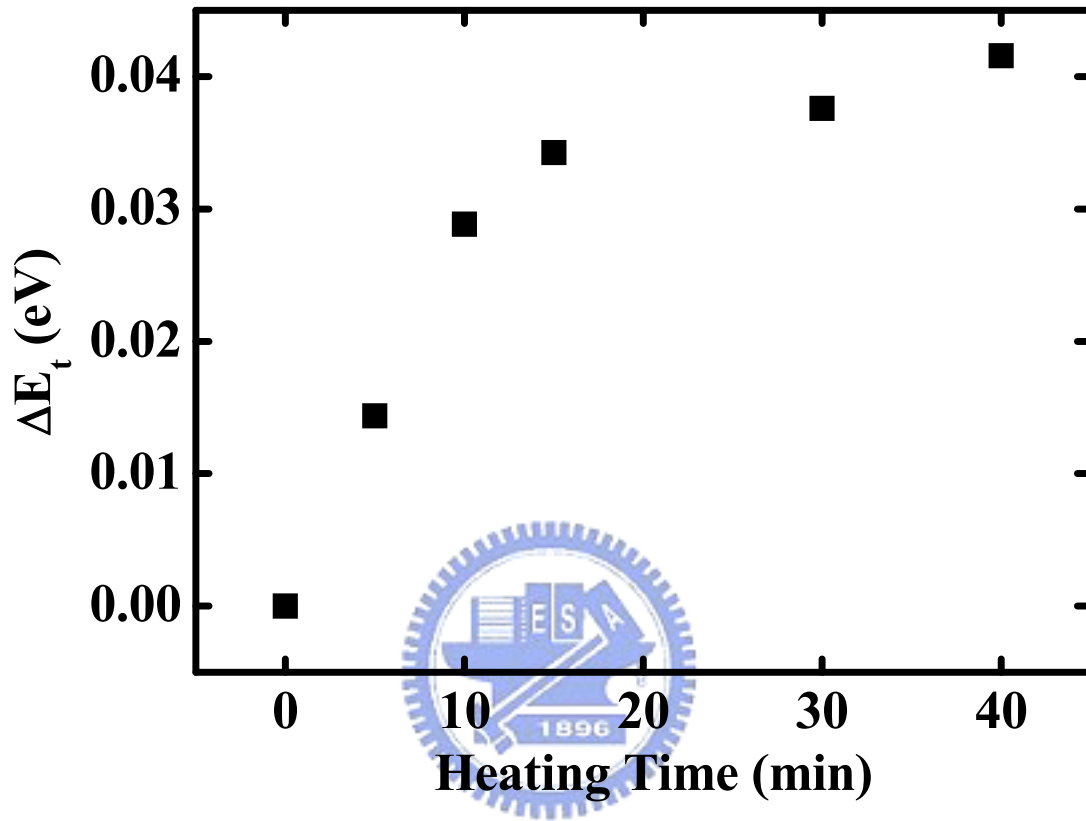


Fig. 4.7 The variation of trap relative energy while heating  $\Delta E_t$  changes rapidly during the first 10 minutes but tends to be stable eventually.

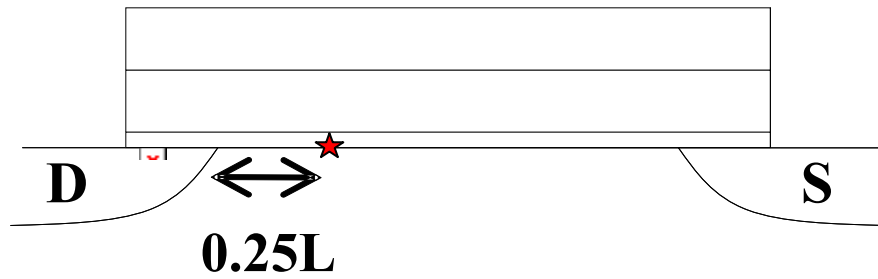


Fig. 4.8(a) The extraction of the trap position used in hole migration experiment

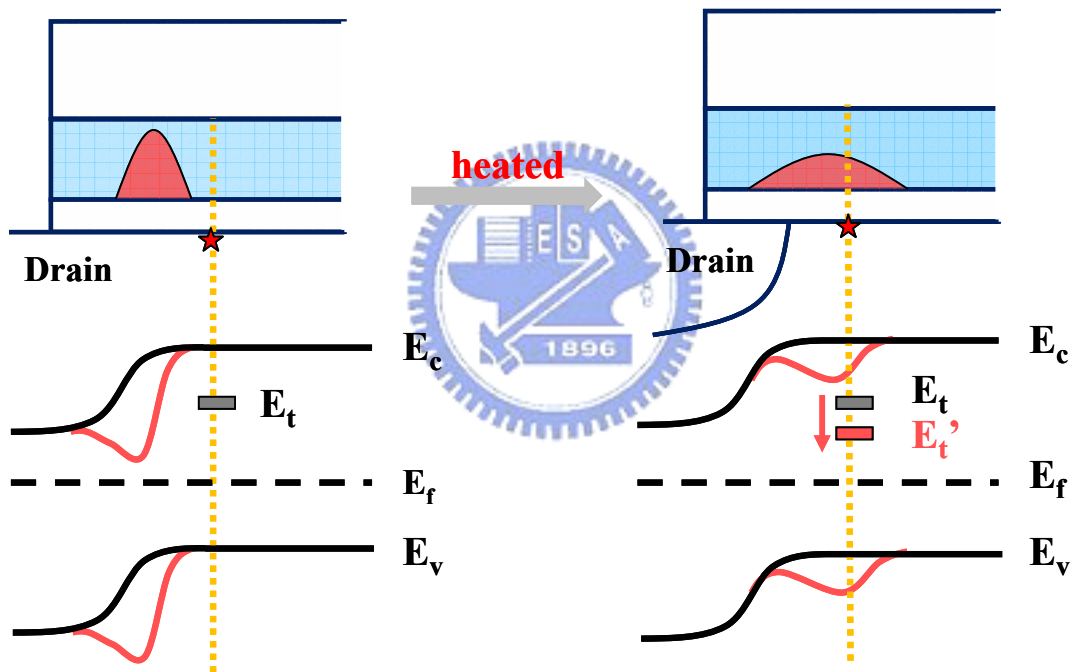


Fig. 4.8(b) The hole distribution and band diagram before and after heating

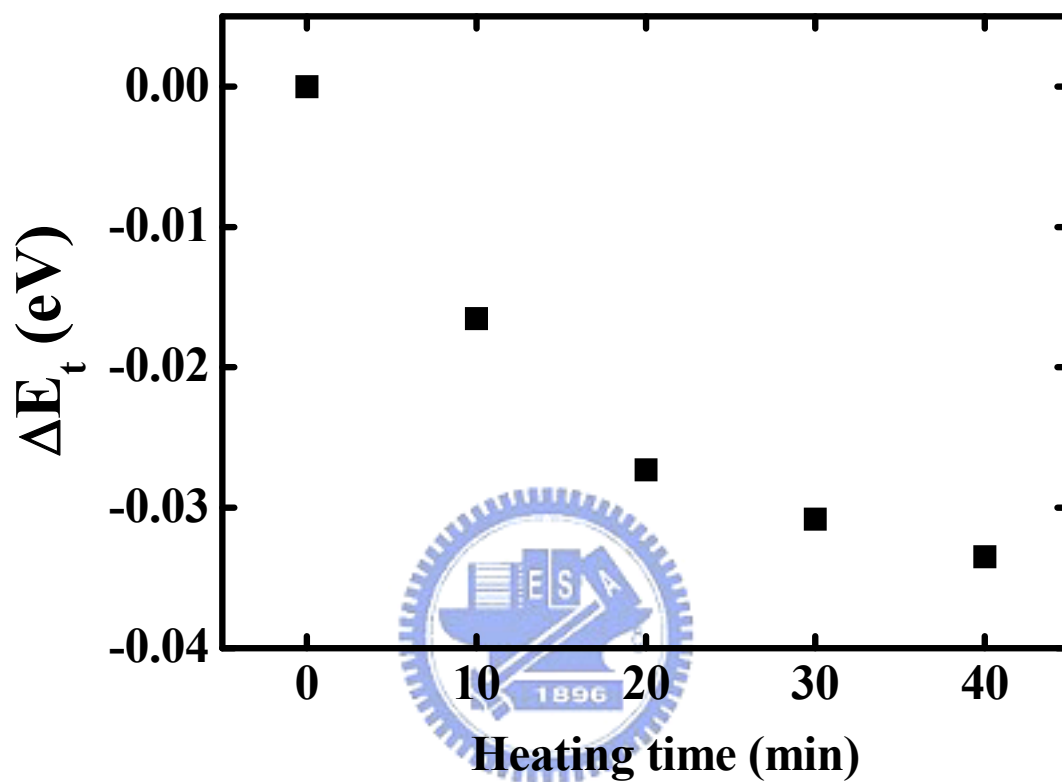


Fig. 4.9 The variation of trap relative energy while heating

$\Delta E_t$  shows a different trend from the former one.

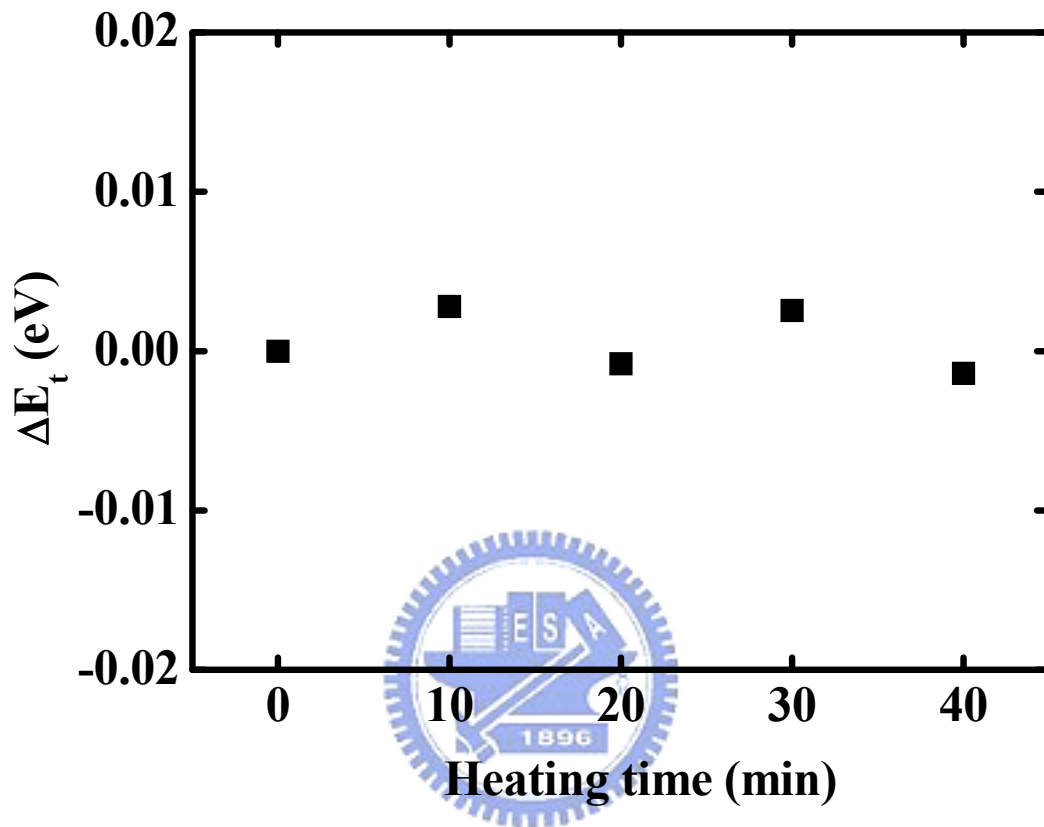


Fig. 4.10 The surface potential change under high temperature after programmed by CHE at the source side



# Chapter 5

## Conclusion

The study has used oxide interface traps as potential probes to detect the surface potential variation. With the trap position extraction technique, the surface potential change at a specific position could be inspected during CHE program. The comparison of CHE and CHISEL indicates that the charge distribution of CHISEL is wider than CHE.

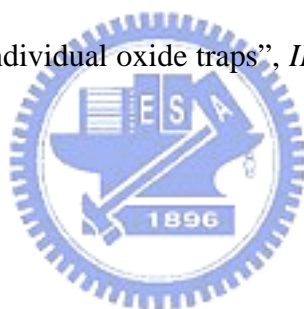
With appropriate trap positions along the channel, the charge misalignment of CHE program and BTBT hot hole erase was also investigated utilizing our method. It is verified again that the charge distribution of BTBT hot hole erase is narrower than CHE. Besides, we have observed the surface potential variation during hole lateral migration in the nitride layer under high temperature.

Due to the sensitivity of RTN to the potential change around the trap, our method is suitable for inspecting the surface potential change throughout the standard operations. Nevertheless, more applications are needed at the present time.

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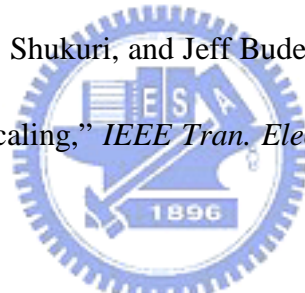
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碩士論文題目:



利用 RTS 方法研究 SONOS 快閃記憶體

寫入/抹除電荷之橫向分佈特性

**Characterization of Program/Erase Charge Lateral  
Distribution in SONOS Flash Memory Cell by Using  
RTS Technique**