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非對稱輕摻雜汲極金屬氧化半導體電晶體
應用於2.4GHz 射頻功率放大器
A 2.4GHz RF CMOS Power Amplifier
Using High Breakdown Voltage
Asymmetric-LDD MOS Transistors

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論文口試委員會審定書

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功率放大器之設計

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非對稱輕摻雜汲極金屬氧化半導體電晶體應用於2.4GHz 射頻功率放大器

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摘要

本論文展示了一種以非對稱輕摻雜汲極金氧半體電晶體作為功率單元的 2.4GHz 射頻功率放大器架構,該放大器可完全以 TSMC 0.18um 的 CMOS 一般製程環境來實現。這個設計可以穩定的操作在 2.5V ~ 2.75V,而不需使用串接電路。較高的操作電壓使得電路有優越的功率特性,根據晶片實際量測的結果,2.5V 工作電壓條件下,功率增益達 20dB,功率增加效率(PAE)達 30%,2.75V 的工作電壓條件下,輸出功率 P1dB 可達 21.5dBm 飽和輸出功率可達 23.2dBm,並且測得 W-CDMA π/4 QPSK 調變下,鄰近通道功率比在 15dBm 的輸出功率為-41dBc,與大約 36dBm 的輸出三階互調截點(OIP3)。

關鍵字:金氧半導體電晶體功率放大器,非對稱金氧半導體電晶體,功率單元,崩潰電壓,功率增加效率,功率增益,1dB 的功率壓縮點,單晶片系統

A 2.4GHz RF CMOS Power Amplifier Using High Breakdown Voltage Asymmetric-LDD MOS Transistors

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Abstract

This thesis presents a 2.4 GHz RF CMOS power amplifier based on two stages amplifiers topology with asymmetric-lightly-doped-drain (LDD) CMOS power cell which is fully embedded in the conventional foundry logic process with only one additional mask but without extra process step. The power amplifier can achieved higher output power and higher power-added efficiency (PAE) and novel linearity. The simulation result demonstrated 20dB power gain, and 30% PAE with 2.5V supply voltage, 21.5dBm at 1-dB compression point (P1dB), 23.2dBm saturate output power, -41dBc ACPR at 15dBm output power point with standard W-CDMA $\pi/4$ QPSK modulation , and ~36dBm OIP3 with 2.75V supply voltage.

Keywords: CMOS power amplifier, asymmetry –LDD CMOS, power cell, break down voltage, PAE, power gain, P1dB, SOC.

誌 謝

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Chapter 1

INTRODUCTION

In RF circuit design, Power Amplifiers are the most power-hungry building blocks of RF transceivers. Large supply voltage is requirement for practical application. CMOS PA design will face the great impact and hard to survive in advance technology implementation with low supply voltage in the future.

The CMOS process reduce the minimum channel length in recent years, unit current gain cut off frequency (ft) has increased, For instance, Tsmc 0.13um technology, ft is above 100GHz and maximum oscillation frequency (fmax) is about 80GHz [1]; for Tsmc 0.18um technology, ft is about 51 GHz, fmax is about 76GHz. These results are suitable for present protocol. CMOS technology has made great progress, it almost has implemented all blocks in system successfully, such as baseband processor, microprocessor, flash memory, VCO, LNA, mixer [Table 1.1]. CMOS technology became the most common back-end system implementation. The approach of system on a chip (SOC) can avoid expensive and individual bulky hardware or complexity system in package (SIP) technique.

However, designers suffered from realizing the direct conversion RF system for several years, especially power amplifier building block. Because something cost trade-offs in performance.

1.2 Challenge of CMOS power amplifier

Fig. 1 show the supply voltage of advance technology that decreases when gate length decrease. The practical supply voltage of power amplifier is 3.3V but the logic-core supply voltage even less than 1.2V after 90nm technology. Therefore, low output power standard like Bluetooth, 0~4dBm can be realized, but large output power would be limited by CMOS characteristic. A fatal drawback of CMOS is low breakdown voltage. The problem limited the supply voltage that limits the maximum output power of power amplifier [Fig. 1.2]. The optimum output loading design becomes a complex and critical issue in power amplifier design. Therefore, CMOS power amplifier has been one of the most challenging circuits and still defied an elegant solution.

Table 1.1. implementation of system with different application

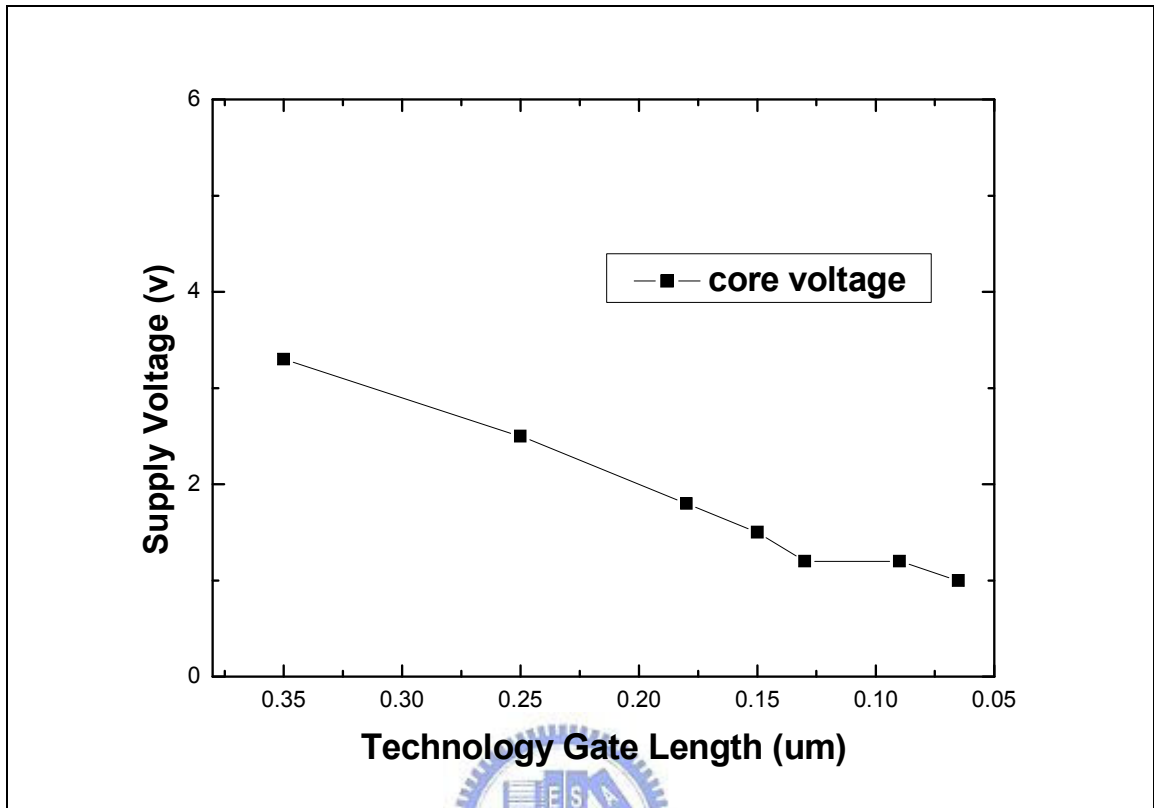| product	PA/switch	IF section	Base band
Cellular Phone	GaAs/SiGe	Bipolar/SiGe/Si BiCMOS	CMOS
WLAN	GaAs/SiGe/CMOS	Bipolar/Si BiCMOS/CMOS	CMOS
Bluetooth	Si BiCMOS/CMOS	Si BiCMOS/CMOS	CMOS
GPS	GaAs/SiGe	Bipolar/Si BiCMOS/CMOS	CMOS

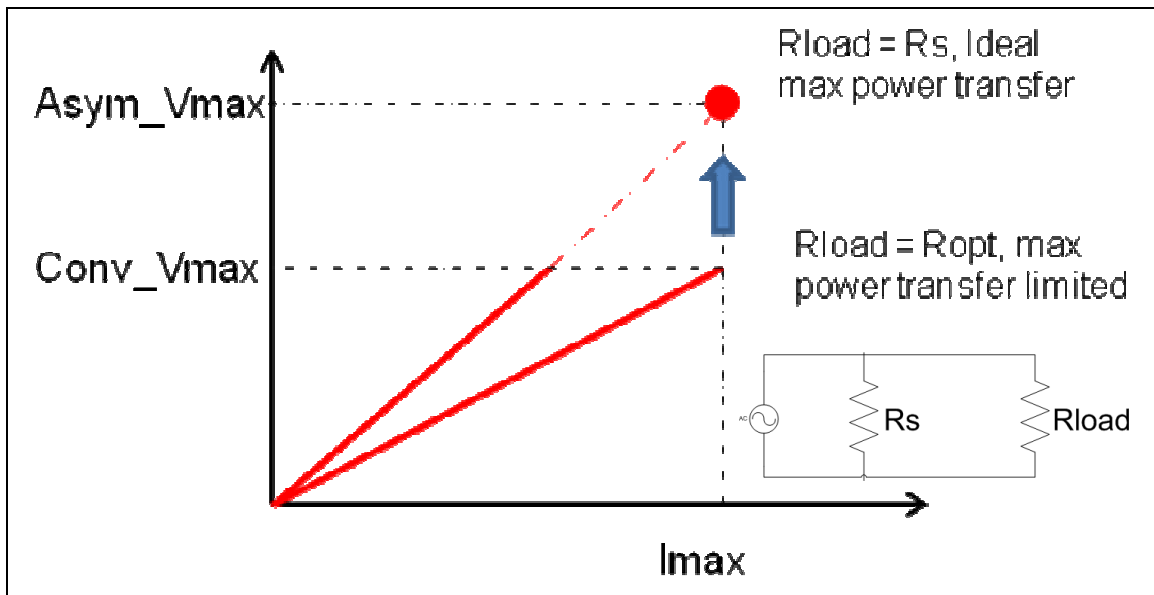Fig.1.1 the core supply voltage to technology gate length

Fig. 1.2 V-I load line show that If increase breakdown voltage, the output power can approach ideal maximum power transfer with $R_{load} = R_s$.

1.3 General statement of CMOS power amplifier

What is the development of the present CMOS power amplifier? In fact, industry had use CMOS power amplifier for lower output power application, such as bluetooth and WLAN, the standard bluetooth is about 0 to 4dBm [2] and WLAN is about 15dBm. But output power is still a limitation and it is rare larger output power application designed by CMOS, the large output power application such as PHS 3G cell phone are almost implemented by GaAs or SiGe. The limitation not only output power but also efficiency, gain etc. If we want to make a break though the bottleneck, high performance power cell would be the solution.

Resent years, our research group presents a new asymmetric-lightly-doped-drain (LDD) MOS transistor [4], [5] that is fully embedded in a CMOS logic without any process modification, so it can be easy implemented without any additional process step or extra cost.
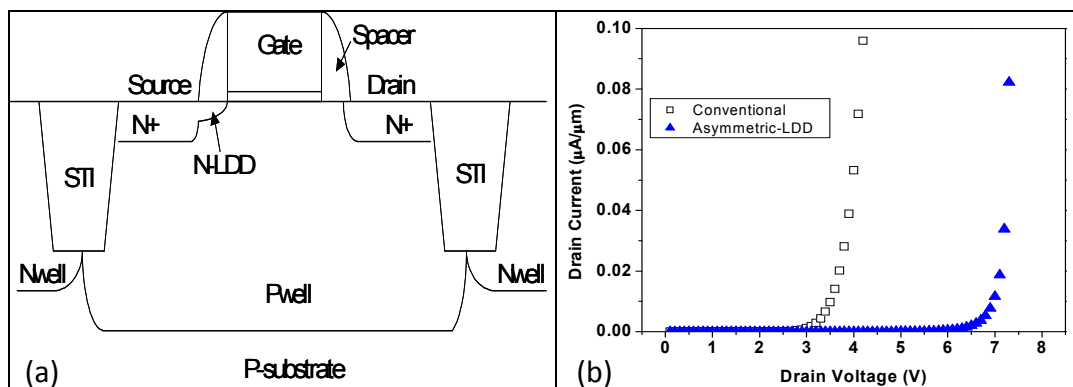

Fig. 1.3   (a)Device structure of asymmetric-LDD MOS transistor .(b)breakdown

voltage of asymmetric –LDD mosfet and conventional mosfet

The major difference to conventional MOS transistor is no n[+]-LDD region at drain side. [Fig. 1.3(a)] The formed depletion region under reverse drain bias can sustain large voltage for RF power application. Based on the research, this new structure can overcome the low breakdown voltage issue and improve the RF power performance [3], the breakdown can be 7.0V [Fig.1.3(b)] with still high unity current gain cut-off frequency (f_t). Focus on full embedded CMOS power cell, we compare three general power cells to asymmetric LDD mos power cell with model simulation, those are nmos unit cell, cascode cell, inverter CMOS push pull power cell. [Table. 1.2]

Table. 1.2 comparison table of different power cell

	Tsmc_unit	Asys_unit (our cell)	Tsmc_Cascode (unit area)	Tsmc_cascode (large area)	Push pull
Area (5x20)	1	1	1	2	1
Ft (GHz)	51	43	35	35	39
Fmax(GHz)	76	100	80	70	59
P1dB(dBm)	13.6	18.34	12.7	18.2	13.3
PAE @P1dB (%)	27.3	39.5	13.4	25.5	35.4

In addition, here shows a data of double area cascode (Two unit area - 6 - cascode) to compare. It shows the asymmetric LDD nmos power cell has larger fmax, output power (even larger than double area cascode output power) and efficiency than others, and it indicates that the asymmetric LDD nmos has constitutional superiority to construct power amplifier.

As technology evolution, the RF gain, cut-off frequency and noise figure of Si MOSFET improve continuously that are widely used for wireless communications. However, the RF power performance of Si MOSFET has little improvement with down-scaling, which is limited by the inherent low breakdown voltage.

This is especially important for RF power amplifier (PA) [6]-[7], where the voltage swing is ~twice of DC bias voltage [9]. This restriction decreases maximum output power, power density and power-added-efficiency (PAE) to a high degree. To add these issues, lateral-diffused MOS (LDMOS) transistors with increased breakdown voltage have been incorporated in CMOS processed [8]-[9], However, for higher frequencies and emerging switch-mode architectures, fundamental limitations, such as comparatively low ft/fmax and high lossy parasitic output capacitance, highly integration complexity and large addition of cost call for alternative technologies. Cascode power cell is an alternative solution to increase output voltage swing without breakdown. However, additional cascode MOSFETs cause extra power

consumption and decrease PAE. To improve the PAE, off-chip matching with higher Q

inductors are usually used but causes additional package complexity [10]-[16].

One method to improve the output power is to use the special transformer

topology even at lower voltage [12]. Nevertheless, the low power gain would be the

problem; besides, the transformer model is difficult to build up for a general purpose

design. Moreover, the insertion loss induces by the low magnetic coupling factor

between the primary and secondary winding has always been the issue.

To sum up, the present PA designers are crying out for a wonderful power cell to

realize more powerful, energy saver and fully integrated CMOS power amplifier

1.4 Motivation

Novel power performance of asymmetric-LDD MOS transistor invites me to further

implement a power amplifier. Does output power really improve with increasing

operation voltage? Is the asymmetric LDD mos power amplifier superior to

conventional PA design? Is the performance still good with high loss on – chip

matching design to realize SOC? Those questions are very interesting, so I make

one step further to realize the power amplifier and finally prove it works with

wonderful performance. I have designed an asymmetric CMOS PA chip, and chapter 2

presents fabricated high performance PA in detail.

Chapter 2

DESIGN FLOW

2.1 Circuit design

In this work, the 2-stage PA adopts a class A operation for driver stage and a class AB for power stage. Such arrangement is optimized for gain and efficiency with good linearity. The simplified schematic of the circuit is shown in Fig. 2.1. To consider the power efficiency issue, the size ratio of driver stage to power stage is 1:4. Besides, the circuit is designed with on-chip matching. Here the impedance of input, inter-stage and output matching to transistors are carefully selected to get a compromise between power, efficiency from load and source pull simulation.

In both stages, asymmetric-LDD MOS transistors have been implemented by foundry standard 0.18μm 1P6M process with only one additional mask but without process modification. The unit cell designed in this work has 10 gate fingers, 0.18 μm gate length and 5 μm width. The BSIM3 model of asymmetric-LDD MOS transistor has been used in PA design, which was confirmed by on-wafer power characterization measurements at 2.4 GHz using an ATN load-pull system. The number of unit cell for the driver and power stage was determined by considering the power-level, gain, matching and linearity. The design procedure of the amplifier

has been carried out through the iteration of ADS and EM simulation.
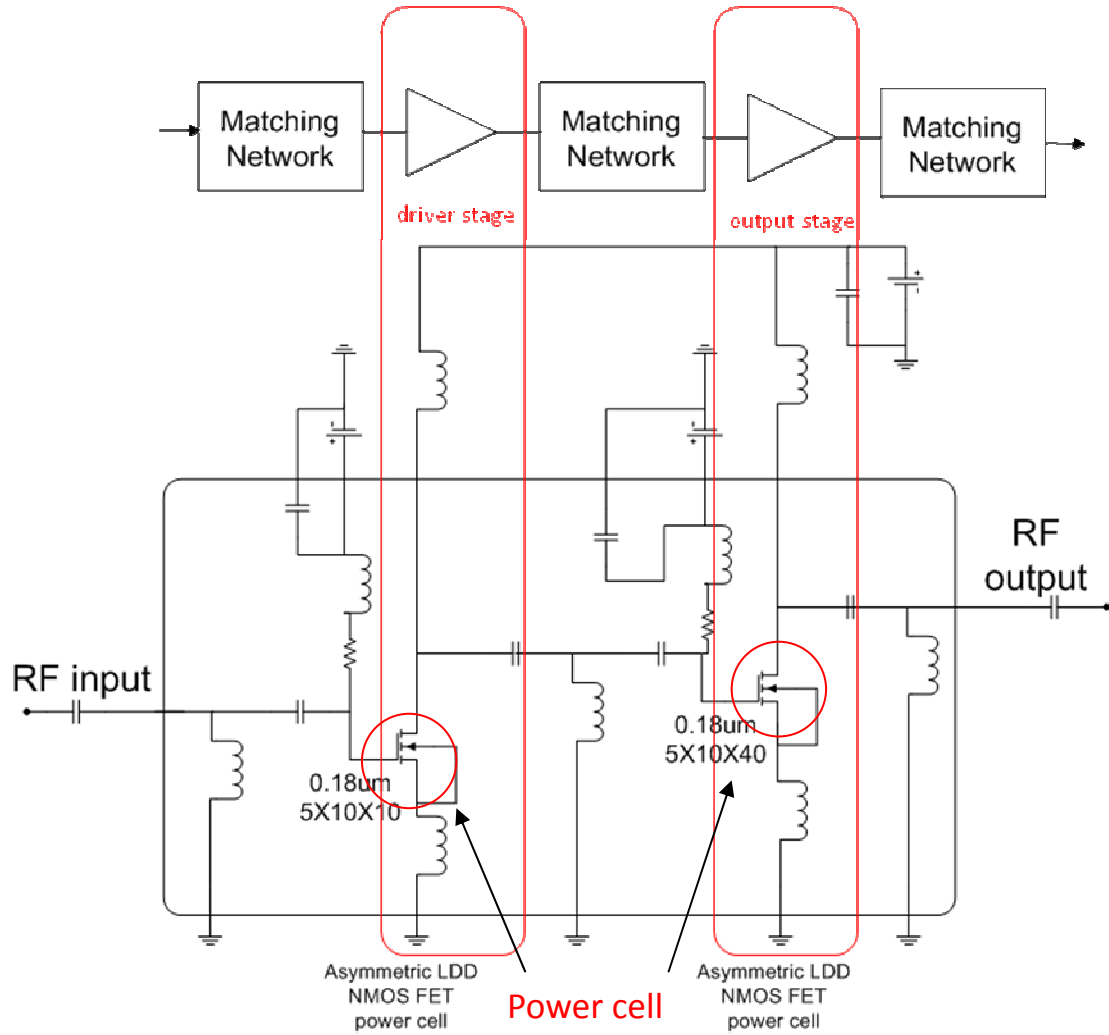
Fig. 2.1 schematic of the two stage amplifier circuit

2.2 Pre-layout simulation process

Ideal lump model design:

First, we have to make a goal table [Table.2.1] and find out the drain bias of power cell.
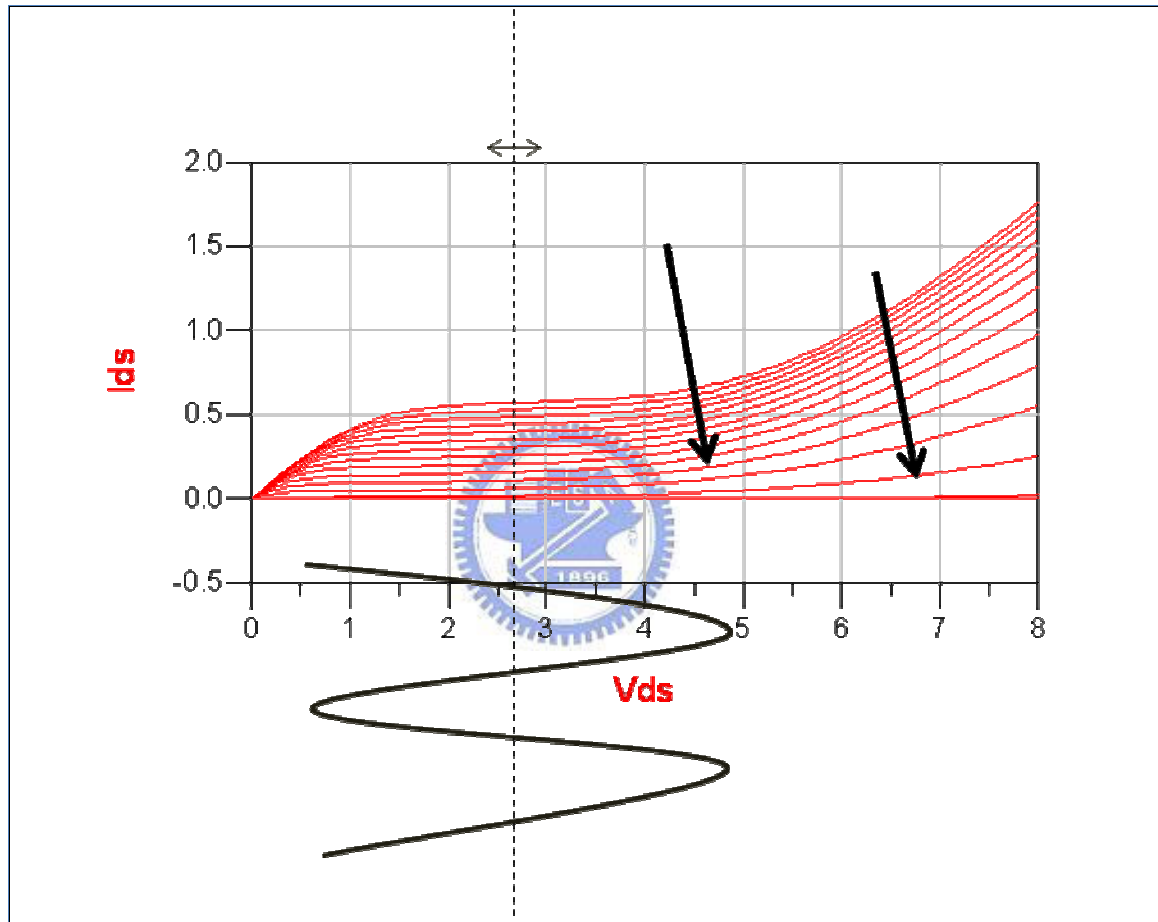

Fig. 2.2 Id-Vd analysis or the a-LDD MOSFET

From the breakdown analysis [Fig.2.2] , The I – V curve show that the breakdown with supply VGS voltage is about 5 V, breakdown without supply VGS voltage is about 7 V. So the optimum DC Vds is about 2.5 to 3V with class A operation. Then, the design was simulated by ideal passive components to examine the power

performance of the structure with ideal result.

table 2.1 shows our goals:

Index	Typical value	Goal value
Output power@P1dB	10 ~ 20dBm	>20dBm
PAE	10 ~ 30%	>30%
Power gain	8~15dB	>20dB
ACPR@15dBm	< -30dBc	>-40dBc
Supply voltage	1.8V	>1.8

First stage design:

To be the first stage, the linearity and gain is the most important index, so first stage

drives in class A operation with Vgs = 1.0V. full swing generate sin wave with good

linearity but poor efficiency. Fig.2.3 show up the bias of class A and output loading

current.

Second stage design:

The second stage, PAE and output power is the most important index, so it drives in

class AB operation with Vgs = 0.7V. by trade of linearity and efficiency, Fig.2.4 shows

that when output swing larger than about 3.2V, the current cut off and save the
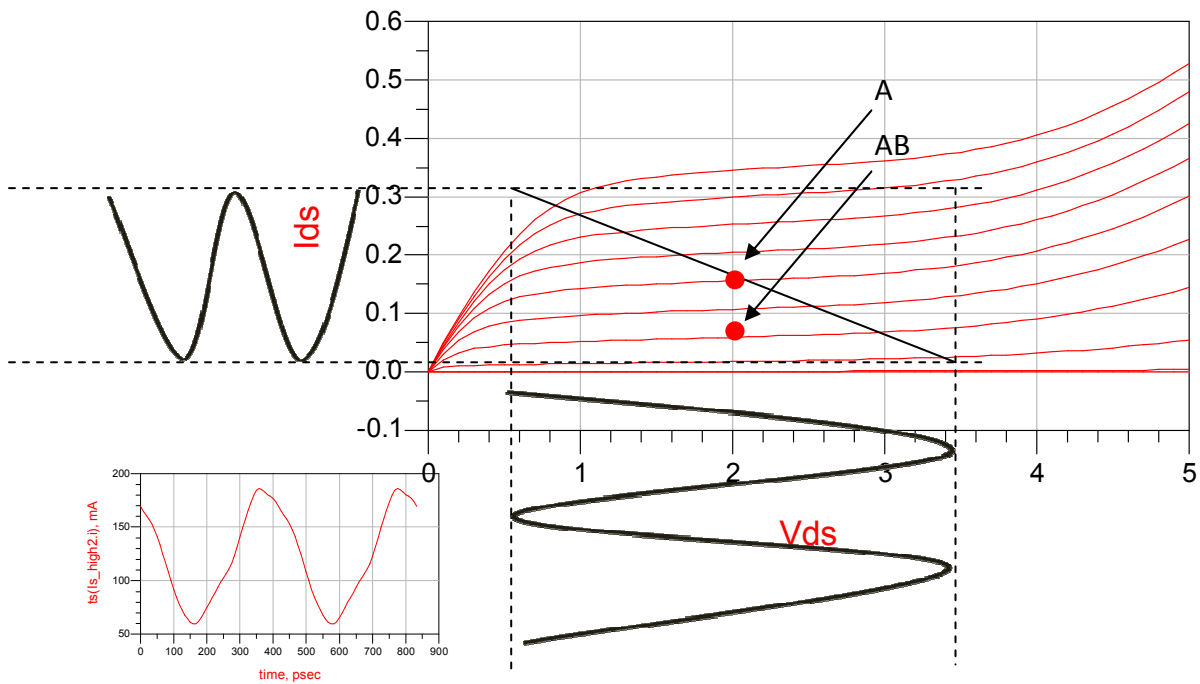
power consumption.

Fig. 2.3 Id-Vd analysis and simulation with load line, gate voltage consideration
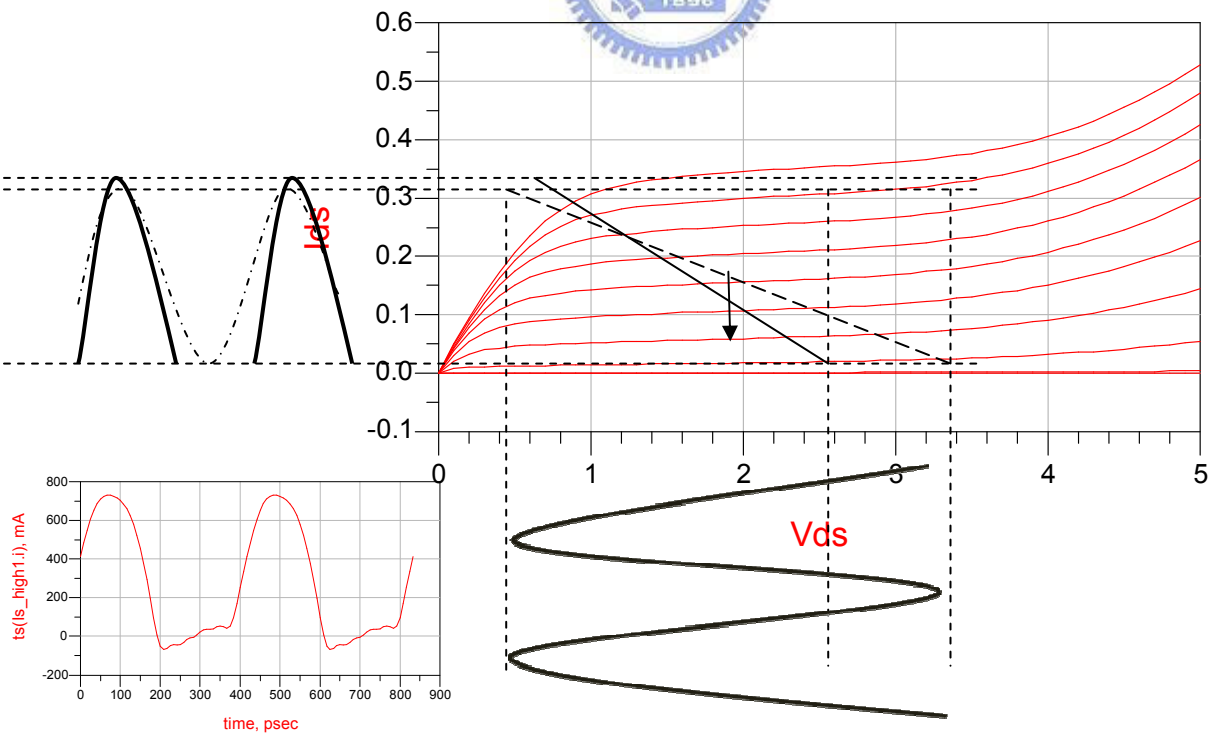

Fig. 2.4 Id-Vd analysis and simulation with class AB operation

The goal of output power is 25dBm, Vdd is about 2.5V, with Vgs 0.7V power added efficiency is about 35%. By equation, determinate output load for initial estimation. We have transistor loading current.[Fig.2.5]
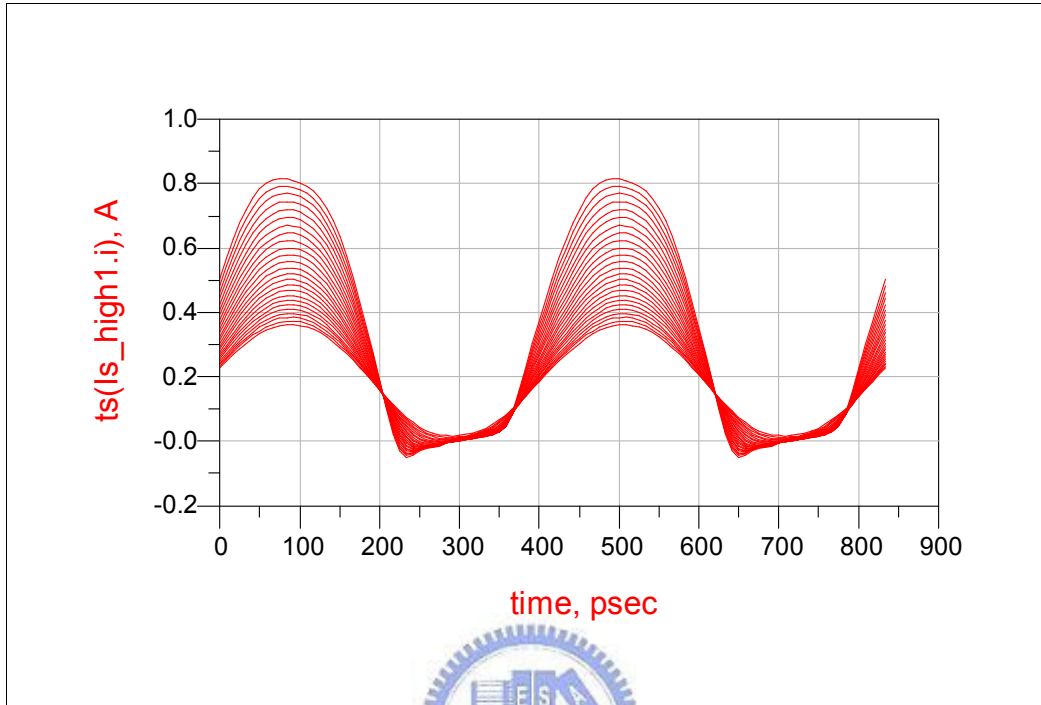

Fig. 2.5 simulation of the transistor loading currents with class AB operation
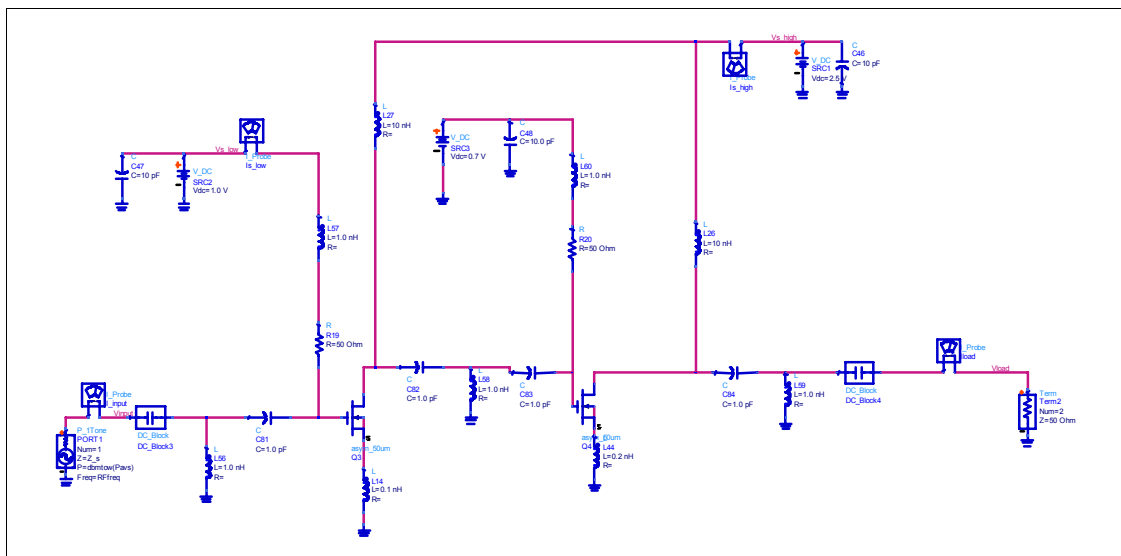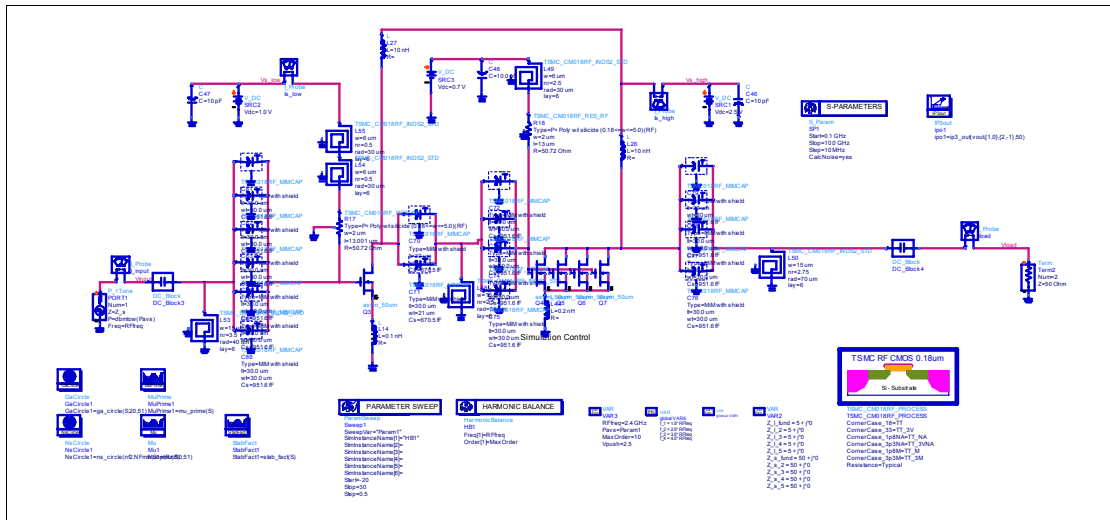

Fig. 2.6 ideal lump schematic

Fig. 2.7 tsmc model schematic

After finding out the value of passive components, replace with tsmc models [Fig.2.7],

finishing the input matching task [Fig.2.8], and trade off output power to PAE on the

load pull simulation system. Fig.2.9 show that constant PAE circle and constant

output power circle, we take the point as the loading impedance between the central

point of maximum constant output power circle and maximum constant PAE circle.

After that, check the stability factor, make sure it is larger than 1[Fig.2.10], and check

the s-parameter prevent oscillation. and the small signal gain larger than 20dB [2.11]

At last, make sure every small signal and large signal within the goal and it was in the
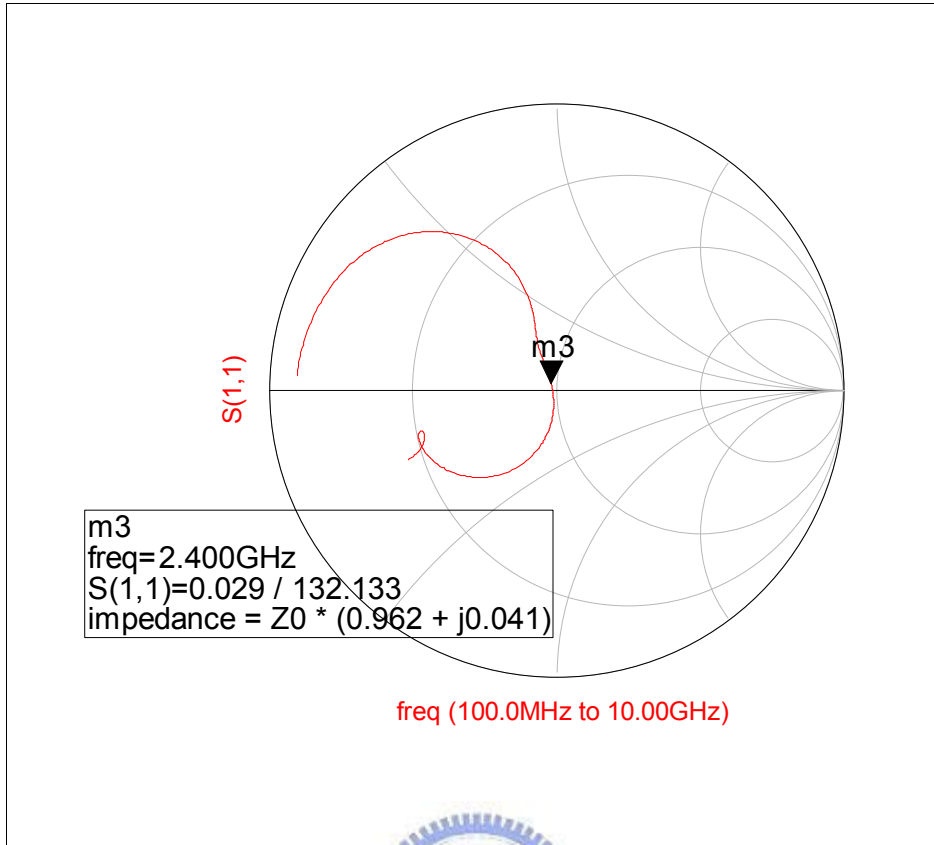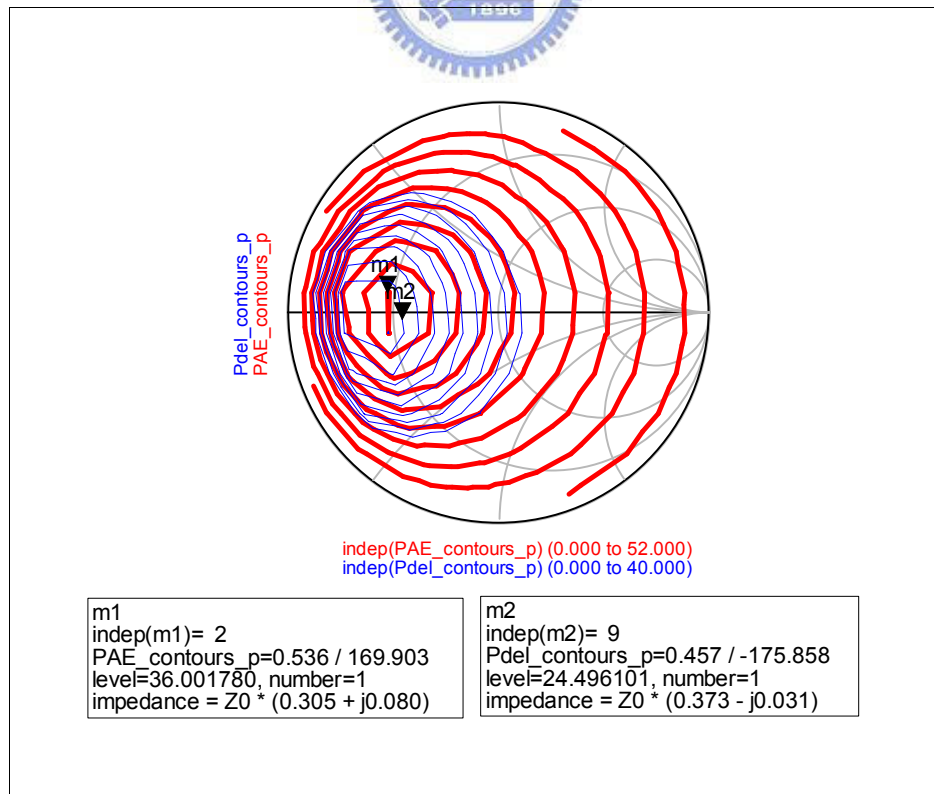
stable condition.

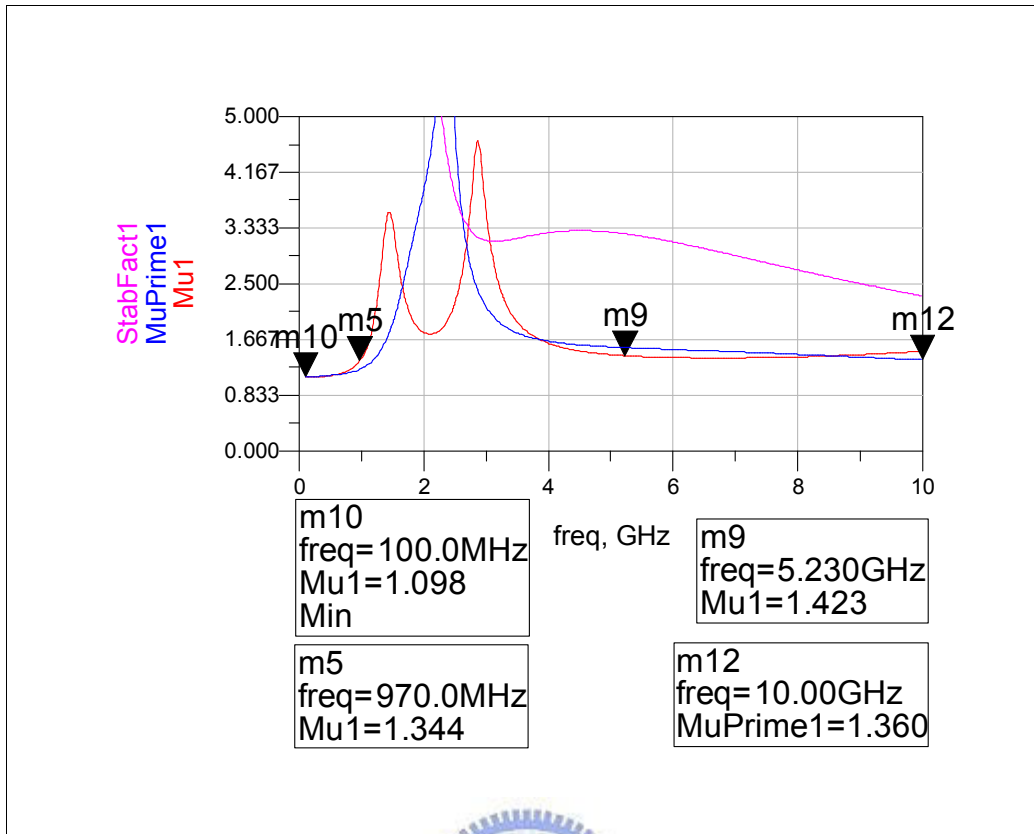Fig. 2.8 Input matching

Fig.2.9 output load pull trade off

Fig. 2.10 stability factor > 1
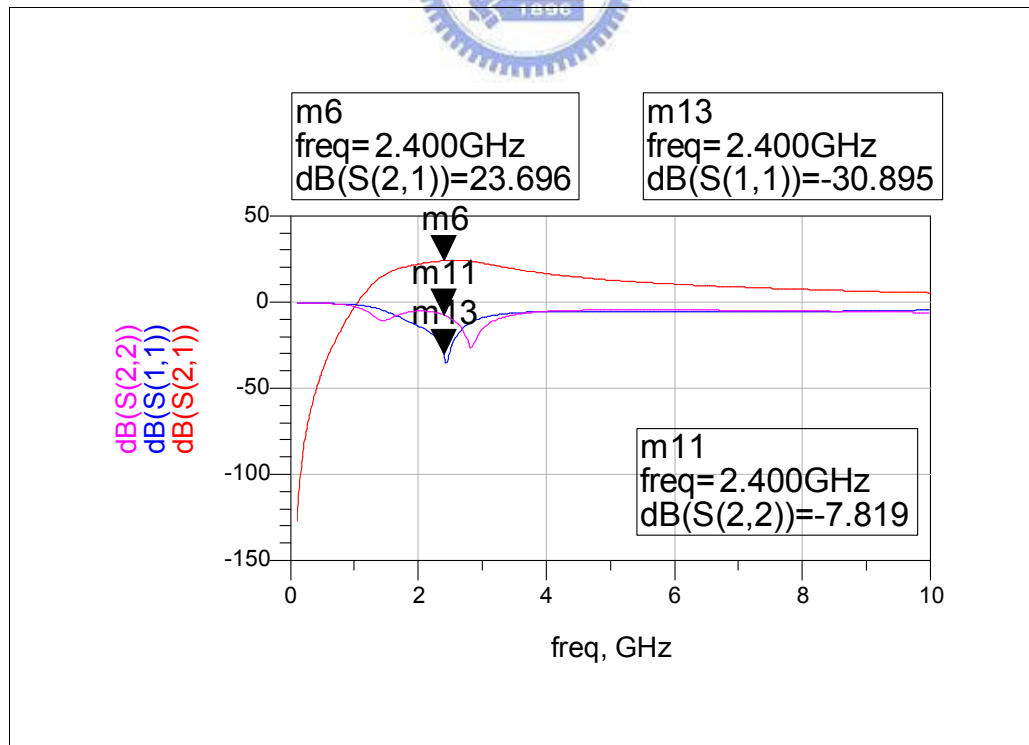
Fig. 2.11 s-parameter of S11 −S21.

After simulation and match the goal, we run the layout flow to implement the chip. Fig. 2.12 show the layout topology, input power comes from the left and symmetrically to two power cells, the signal enlarge in fist stage, after internal matching circuit, the signal drive the second stage with fish bond symmetric wire and combine with output matching network.
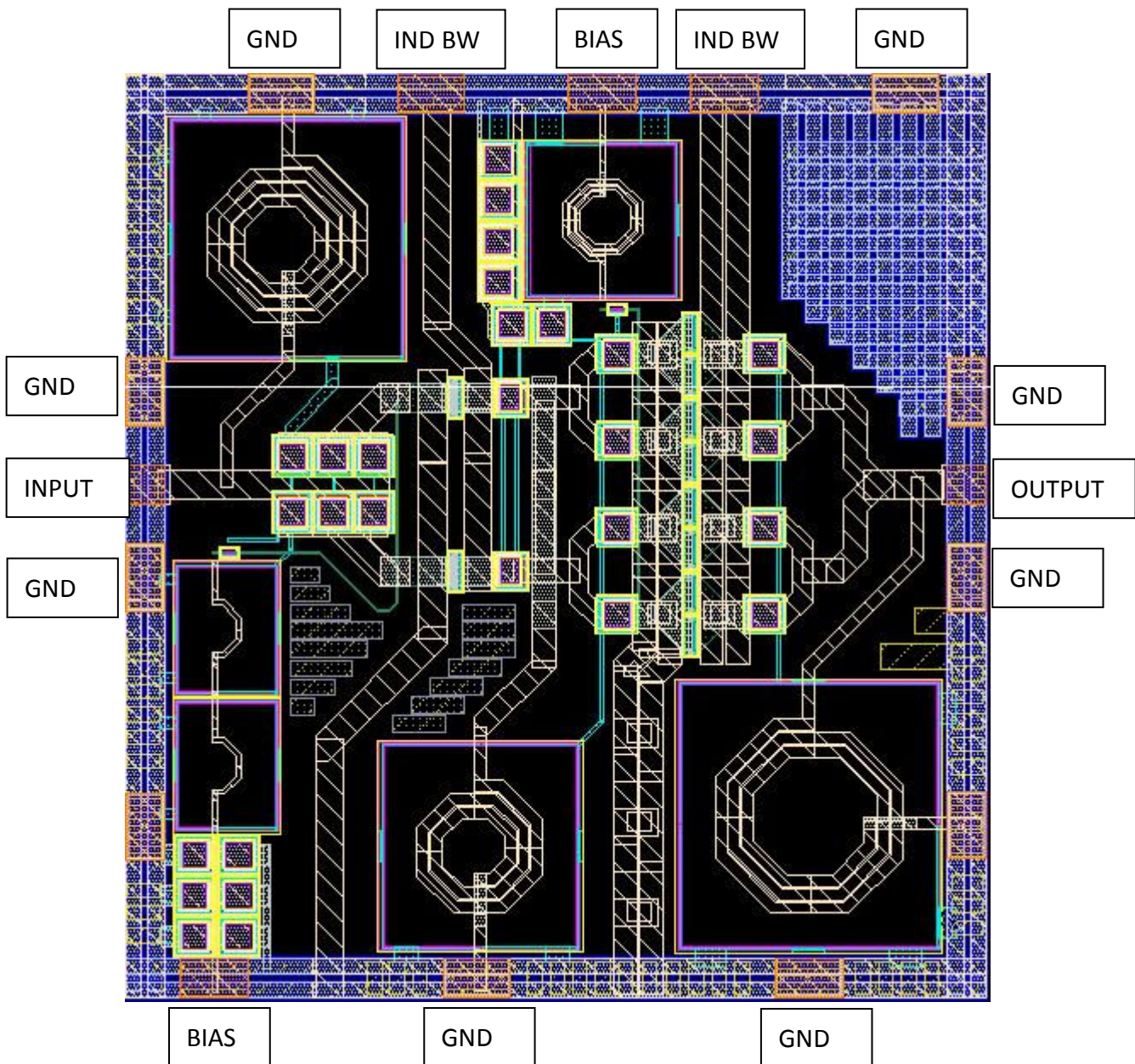

Fig. 2.12 the layout before post layout simulation

2.3 Post-layout simulation
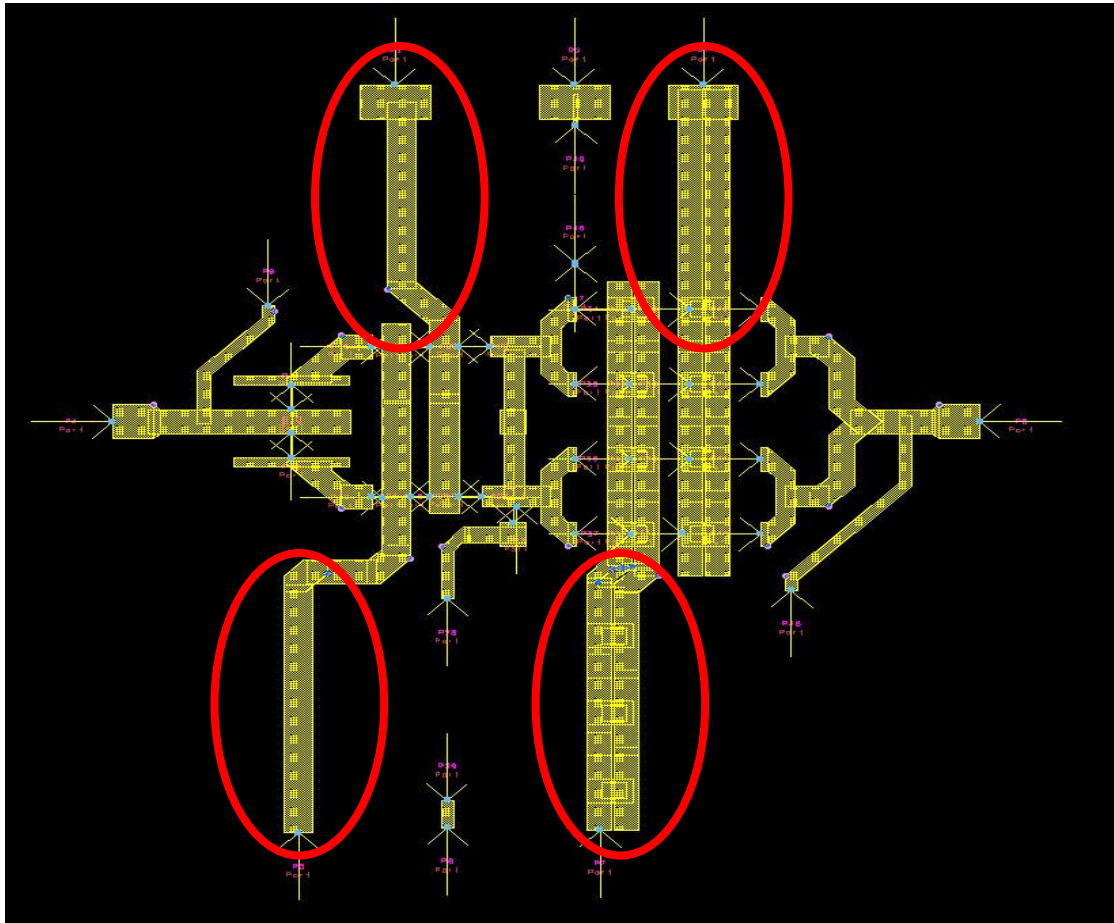
Fig. 2.13 Export the line of layout to momentum ADS system and simulation

Layout is also a very important task for power amplifier design, due to the intersection influence or parasitic, the chip performance cannot match the design in practical, so we have to decrease those effects by post-layout simulation process. Fig.2.13 show the critical DC power line generates parasitic resistance [Fig.2.13 red circle]. To prevent loss, the line has to be widened. After modify the layout simulate the circuit again and find the best layout topology.
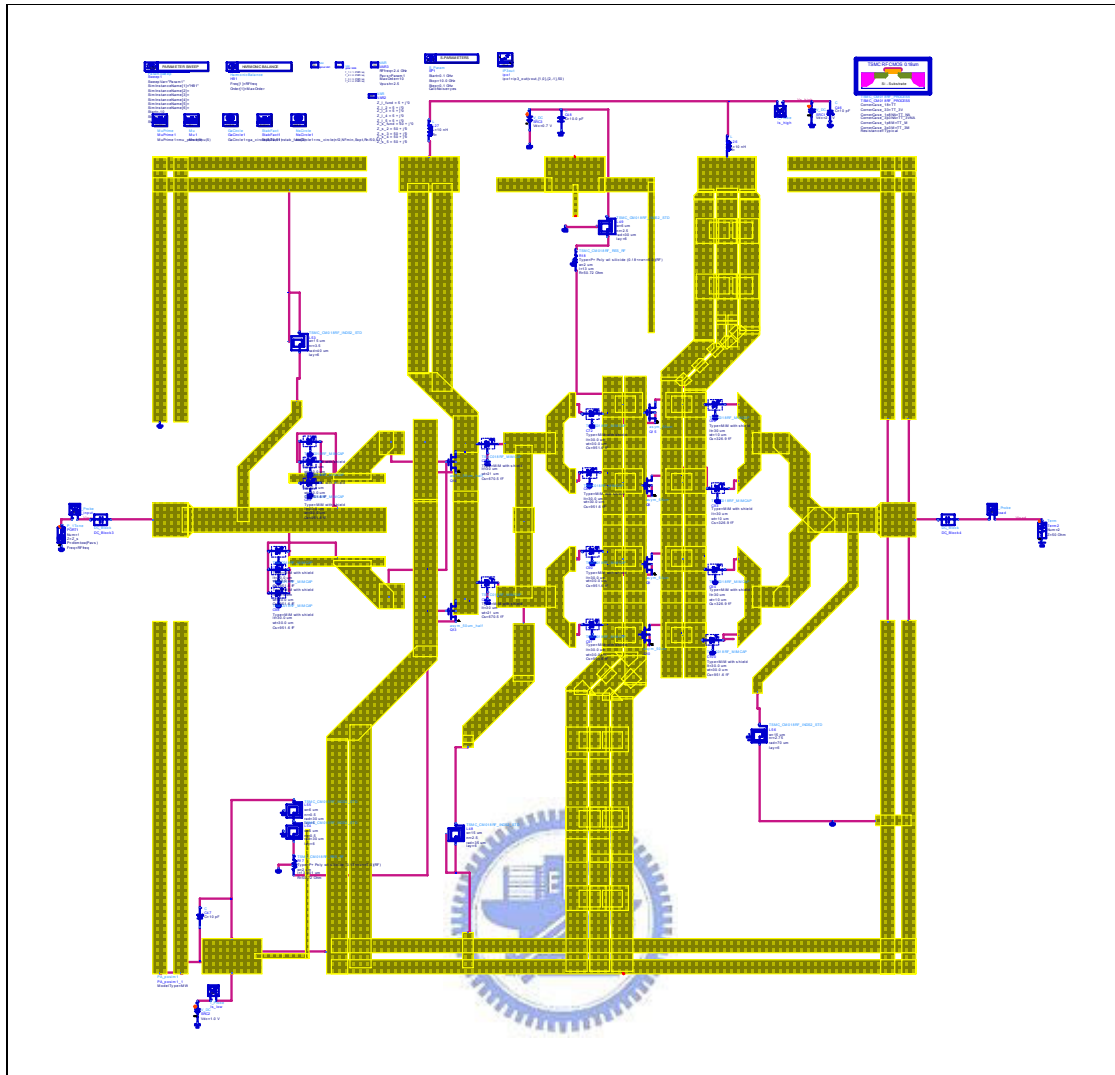
Fig.2.14 post layout simulation with line calculation

To modify the layout with better simulation result, I use ADS momentum system to

generate wire model and use ADS to simulate the result with wire model. [Fig.2.14]

In this way, we can figure out the influence of wire effect. After this task, I can

determinate the best layout topology and tape out. With the simulation, Fig. 2.15

show the final layout version with best result, Fig. 2.16 show the photograph of the

chip after implementation.
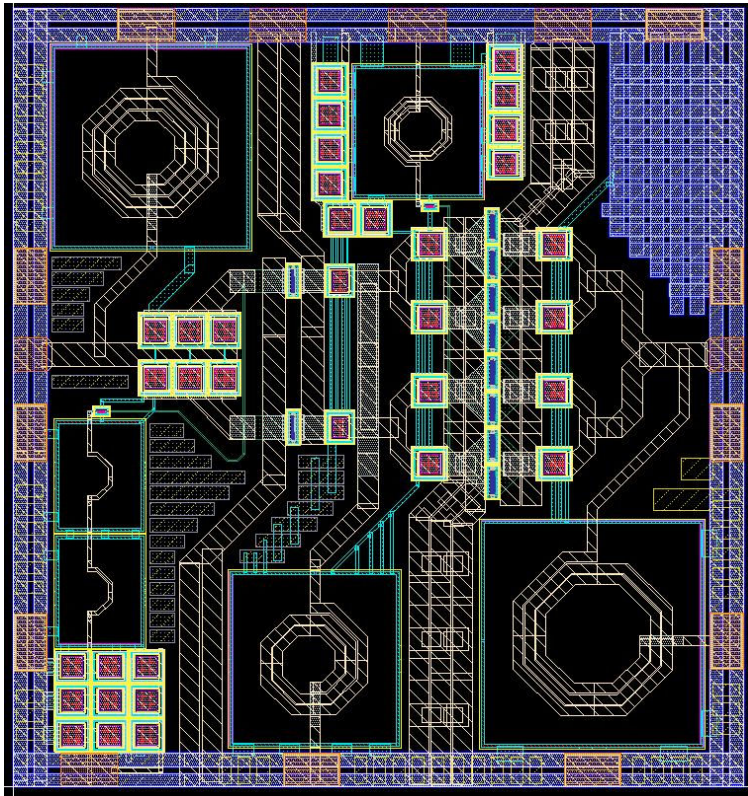
Fig. 2.15   the layout after post layout simulation.
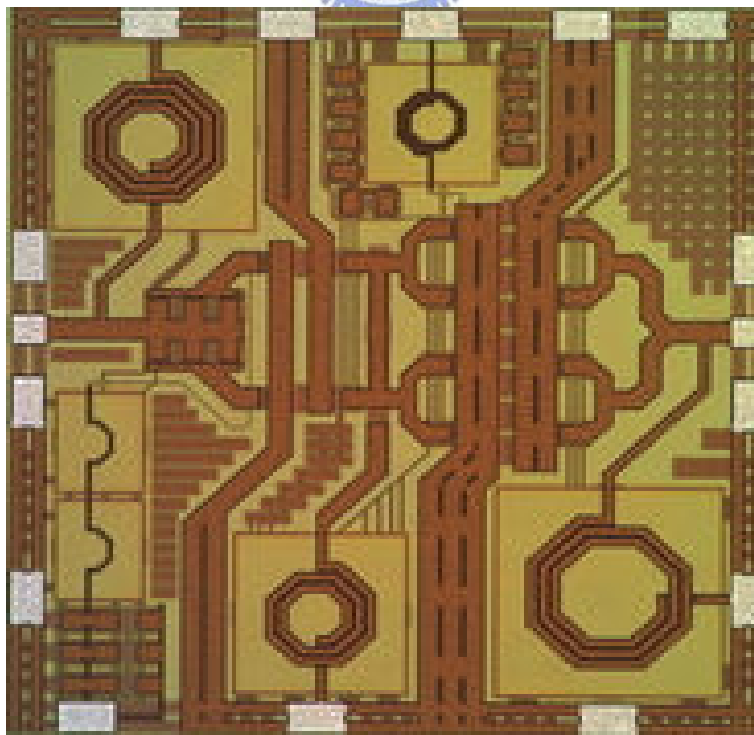
Fig. 2.16 the photograph of the chip

Chapter 3

SIMULATION AND MEASUREMENT RESULT

To verify the chip design, we first measured the small signal S-parameters. Fig. 3.1

shows the on-wafer measurement data, which show a 20 dB gain and 17 dB input

and output return loss- this is consistence with EM post-simulation data.

Fig. 3.1. Measured and simulated gain and return loss for CMOS PA.

Fig. 3.2 shows the measured RF power results of the amplifier. The output power

at 1 dB compression (P_{1dB}) increases with increasing bias voltage from conventional

1.8, 2.5 to 2.75 V. Such increase of desired higher output RF power is consistent with

simulation. Under 2.5 V bias operation, a P_{1dB} of 20.8 dBm and power gain of 20 dB are measured with 30% PAE. The P_{1dB} increases to 21.5 dBm at higher 2.75V bias condition with still compatible 19.6 dB power gain and 29.6% PAE.
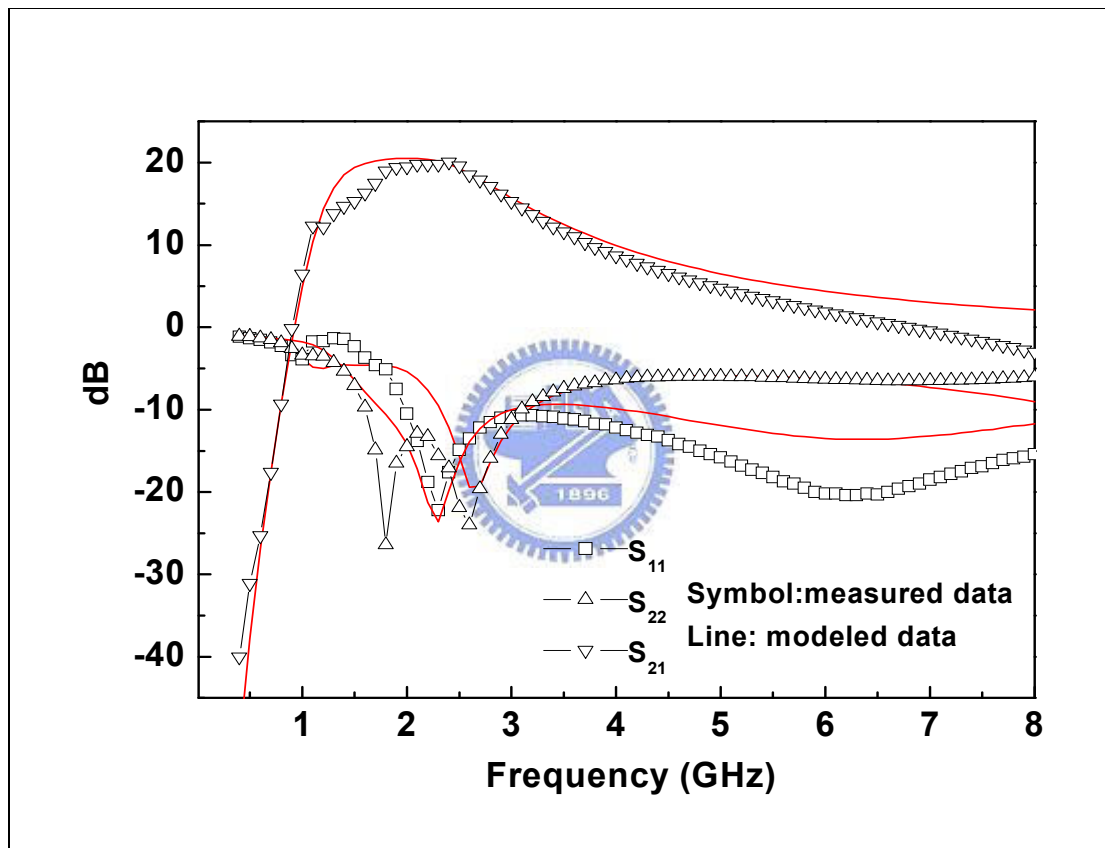
Good adjacent channel power ratio (ACPR) is an important linearity factor for PAs. Fig. 3.3 shows the measured ACPR with standard W-CDMA $\pi/4$ QPSK modulation on different bias voltage. Here the ACPR improves with increasing operation voltage from 1.8, 2.5 to 2.75V monotonically. At the 2.75 V bias voltage, an ACPR of -56 dBc at 0 dBm output power or -30 dBc at 20 dBm output power was measured, which is competitive to the data of the power amplifiers designed for better linearity [15]. In addition, IP3 point is an important factor, the Fig.3.4 ~ Fig.3.6 show up the IP3 point with different supply voltage. The output IP3 point of 1.8V, 2.5V and 2.75V is 22dBm, 26dBm and 36dBm. So it shows that the linearity increases with larger supply voltage.
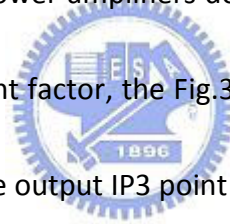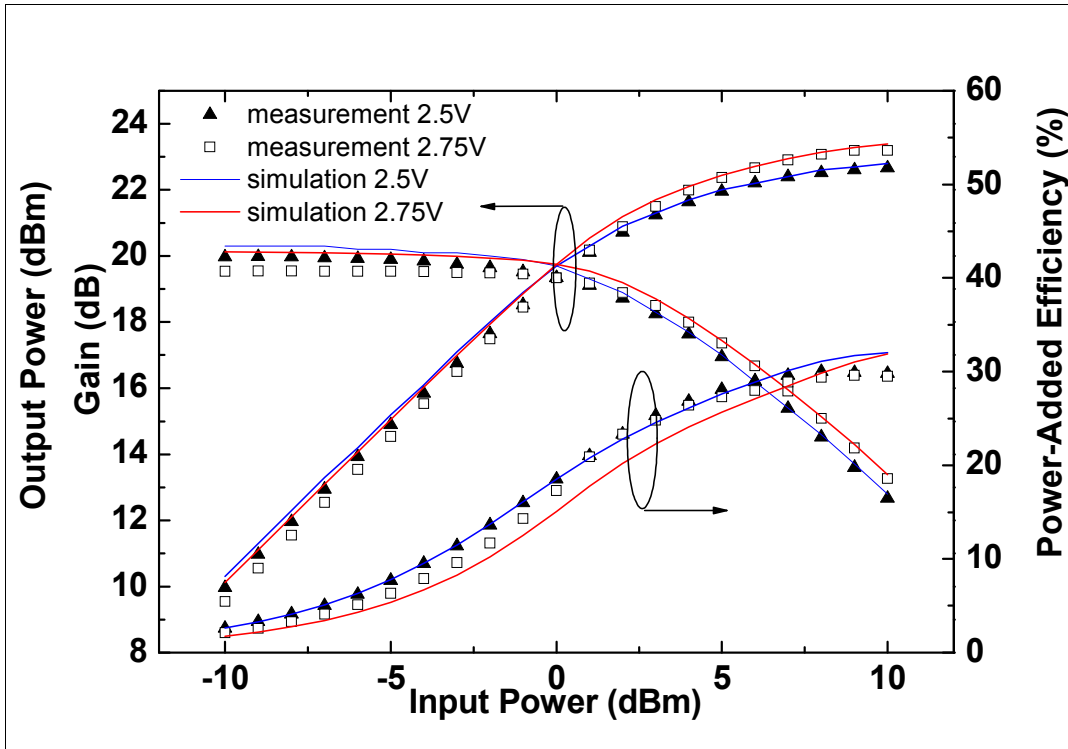
Fig. 3.2. Measured and simulated RF output power, gain and PAE of designed PA using high breakdown voltage asymmetric-LDD MOSFETs.
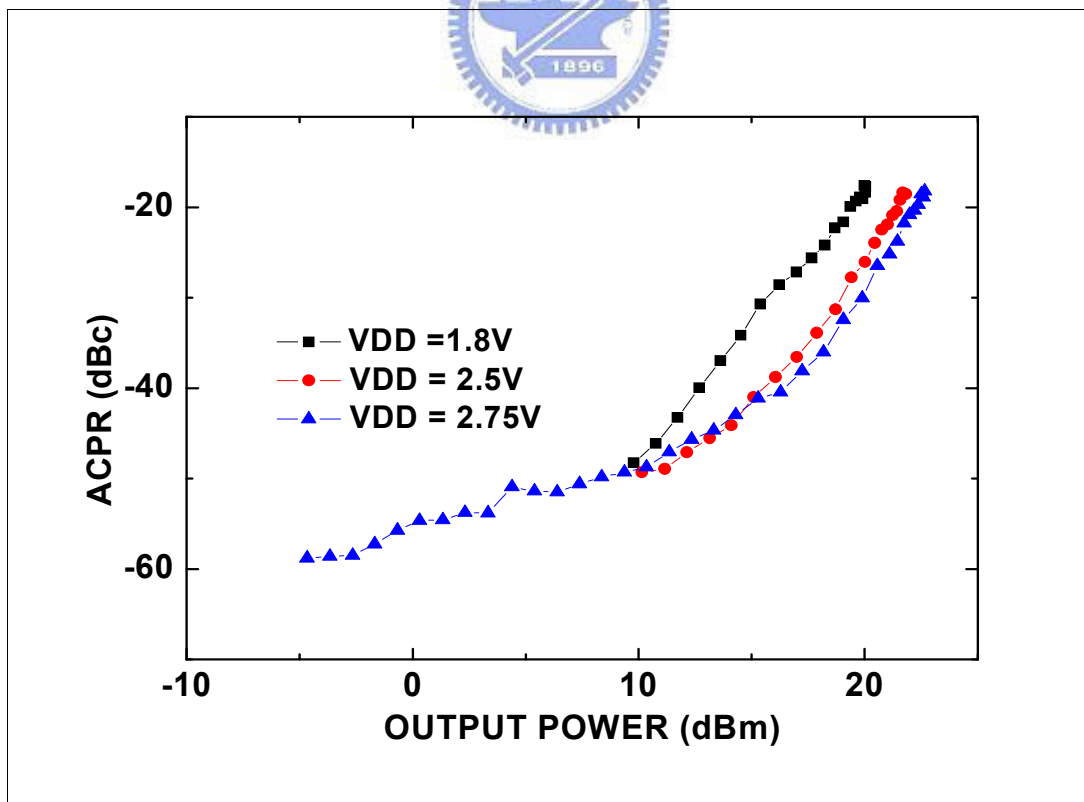
Fig. 3.3. Measured ACPR of designed PA using high breakdown voltage asymmetric-LDD MOSFETs.
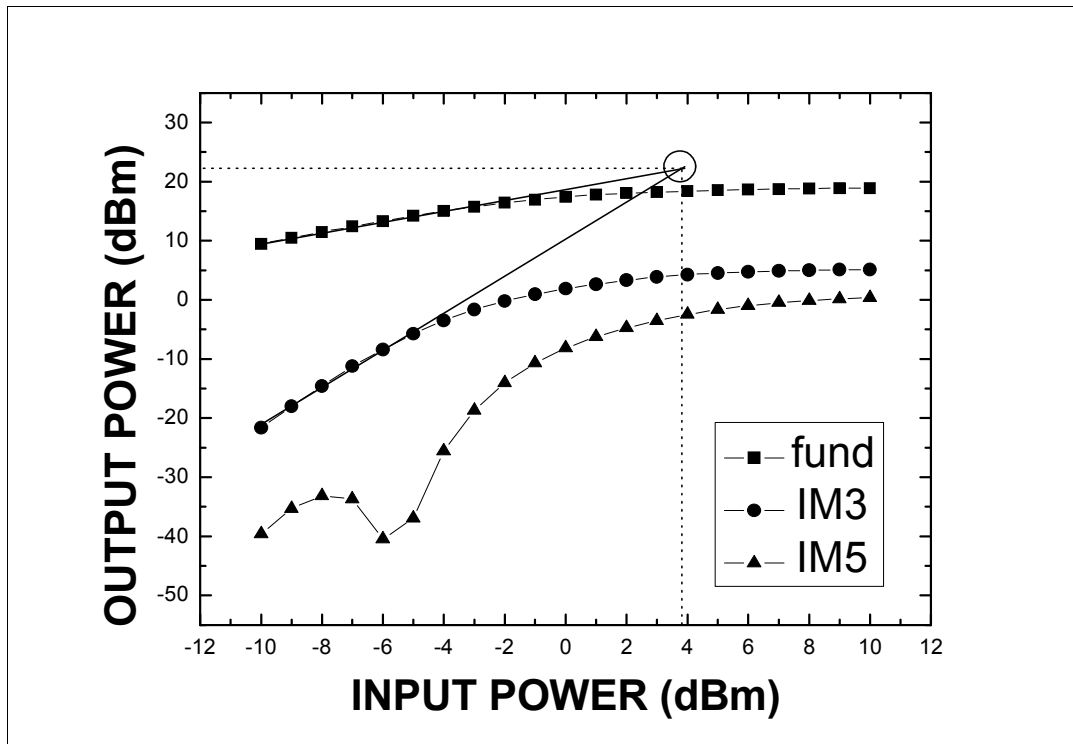
Fig. 3.4 measurement data of third order inter modulation with 1.8V supply voltage.
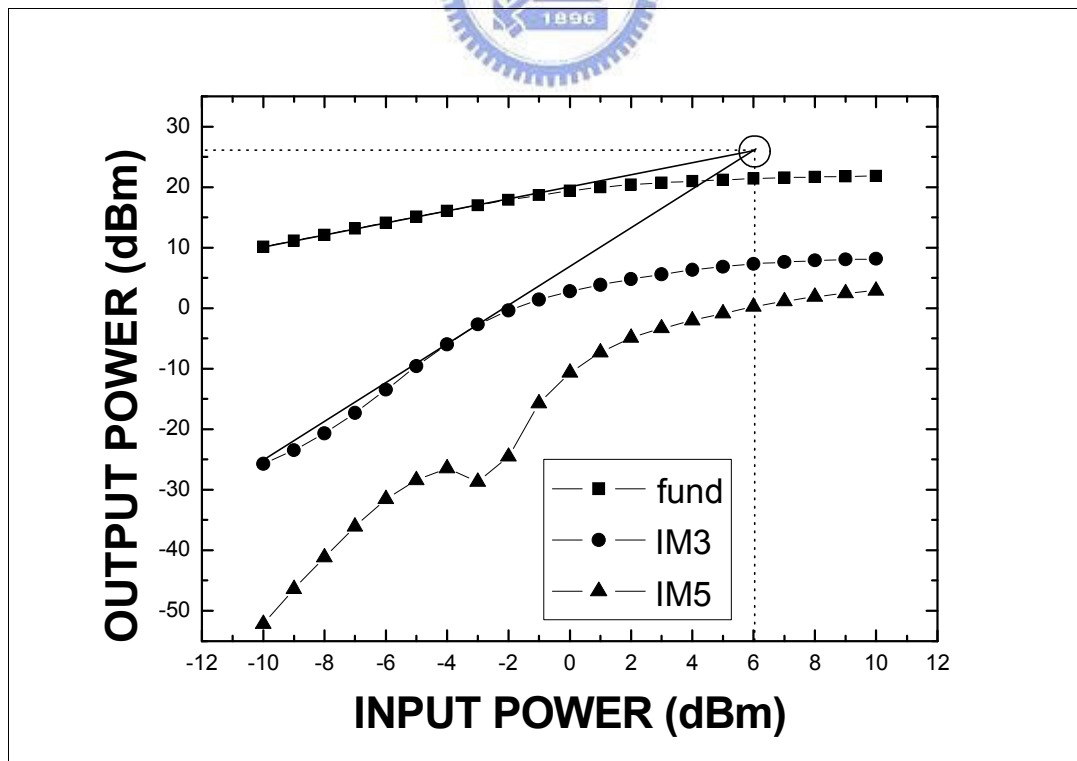
Fig.3.5 measurement data of third order inter modulation with 2.5V supply voltage.
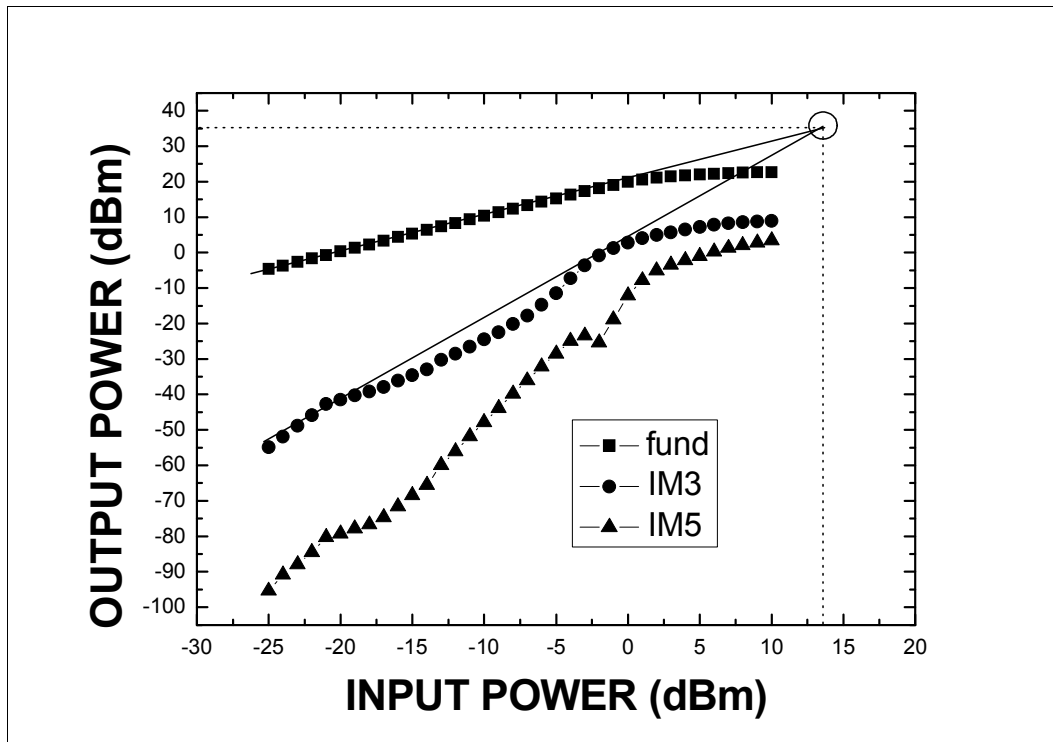
Fig. 3.6 measurement data of third order inter modulation with 2.75V supply voltag
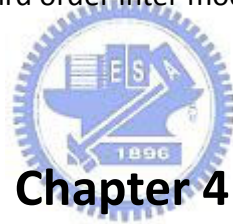
Chapter 4

COMPARISON

The die photo of fabricated CMOS PA is shown in Fig. 2.16, which has a chip area of

1m×1.1m. Table 4.1 summarizes the performance comparison with reported CMOS

PA [10]-[16]. The fabricated PA using high breakdown voltage asymmetric-LDD

MOSFETs shows the large P_{1dB} of 21.5 dBm, high gain of 20.4 dB, and good 29.6%

PAE at 2.4 GHz. Those power performances are better than other reported designs

shown in Table 4.1, with added merits of simple single-ended design, using standard

foundry technology and compact on-chip matching.

Table 4.1 The comparison table of Asymmetry MOS and conventional PAs.

Ref.	Freq. (GHz)	voltage	Pout (dBm)	Gain (dB)	PAE (%)	Width/Power density by P1dB(W/mm)	Matching	technology
[10]	5	1.8	19.2@1dB	7.1	17.5	1.28mm/0.065	On chip	0.18um
[11]	5.2	1.8	17.4/15.4@1dB	15.1	27.1	0.6mm/0.058	On chip	0.18um
[12]	5.8	1	20.5@1dB	~8	27 (Drain)	9.6mm/0.012	On chip	90nm
[13]	2.4/5.2	1.8	9.7@2.4GHz 19.5@5.2GHz	3.7@2.4GHz 24@5.4GHz	15.3@5.2 GHz	1.92mm/0.046	On chip	0.18um
[14]	3.7~8.8	1.8	19 15.6@1dB	8.24	25	0.96mm/0.038	On chip	0.18um
[15]	2~2.45	2.5	16.3@1dB	18	-------	4.2mm/0.01	Off chip	0.13um
[16]	2.4	2.5	20@1dB	11.2	28	0.96mm/0.1	Off chip	0.25um
This work	2.4	2.5	22.7 20.8@1dB	20	30	2mm/0.071	On chip	0.18um
		2.75	23.2 21.5@1dB	19.6	29.6			

Chapter 5

CONCLUSION

We have designed an asymmetric-LDD MOS transistor which has ~twice drain breakdown voltage to the conventional one. Besides, the power amplifier has been designed by single ended on chip design and fabricated by TSMC 0.18um 1P6M process without any process modification. The excellent power performance shows 20dB power gain, and 20.8dBm P_{1dB} compression power and 22.7dBm saturate output power with 30% PAE under 2.5V bias operation. And 20.4dB power gain, 21.5dBm P_{1dB} compression power and 23.2dBm saturate output power with 29.6% PAE under 2.75V bias operation. -41dBc ACPR at 15dBm output power, ~36dBm OIP3 with 2.75V supply voltage. The output power and linearity increase with larger supply voltage, and PAE and power gain saturate at 2.75V. This research demonstrated that the asymmetric-LDD MOS transistor successfully implemented on a CMOS power amplifier with wonderful performance even with on chip matching design. This design method has great opportunity to be future trend and realize SOC of PA.

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