利用特殊接觸電極進行橫向擴散元件之

特性分析與 SPICE 模型建立

Characterization and SPICE Modeling of Lateral Diffused MOS by using a Novel Metal Contact Structure

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摘要

在此論文中，將觀察自發熱效應(self-heating effect)所引發的內部電壓(internal voltage)退化現象。我們提出一個具有特殊接觸電極之LDMOS(橫向兩次擴散之金氧半場效電晶體)結構，藉以量測高閘極脈波造成之內部電壓暫態變化。接著，我們將自發熱效應所造成之內部電壓退化與集極電流退化情形作一比較，最後證明內部電壓是觀察自發熱效應之較好方法。

我們將建立一個具有兩個組成元件之LDMOS SPICE模型，此模型也會納入自發熱效應的模擬。模擬結果準確描述了LDMOS在高閘極脈波下集極電流之暫態變化，顯示我們已成功建立了自發熱模型。在不同閘極和集極偏壓下，有/無自發熱效應之電流模擬結果，都將在論文中呈現。

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Abstract

Self-heating induced internal voltage degradation is observed. A novel lateral diffused MOS transistor with an additional metal contact for internal voltage measurement is introduced. An internal voltage transient at high gate voltage pulse is measured. A comparison of self-heating characterization by the internal voltage method and the conventional drain current method is presented. The internal voltage method is demonstrated to be more sensitive than drain current method for self-heating characterization.

A two-component V_I-based LDMOS SPICE model including self-heating effect is proposed. Our model accurately depicts the LDMOS drain current transient at high gate voltage pulse, demonstrating successful use of the self-heating model. Modeling results of the

self-heating and non-self-heating currents at various V_G and V_D are also shown.

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Chapter 1
Introduction

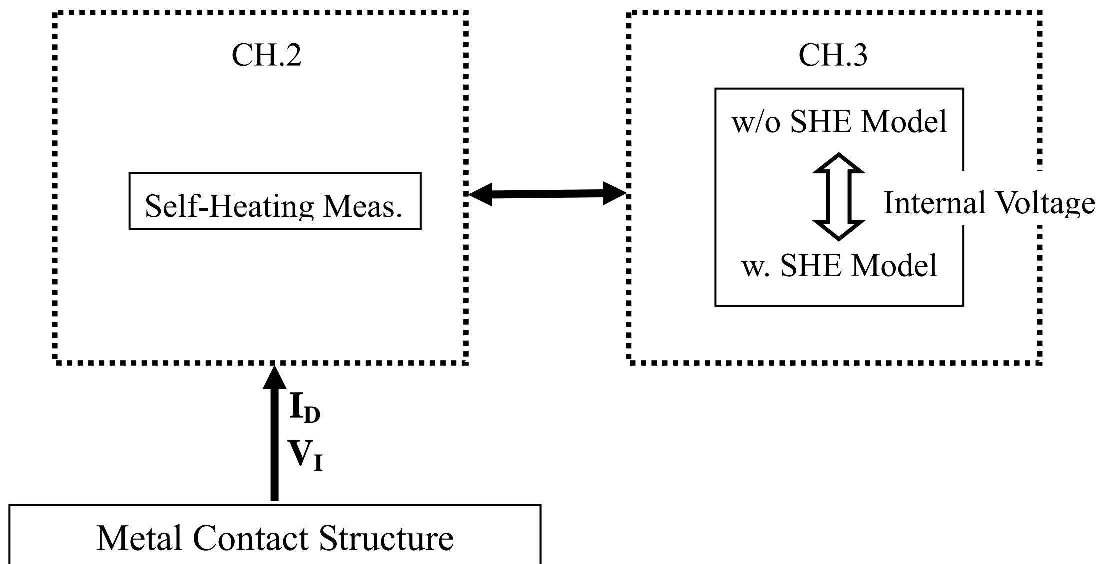
The continuous scaling down of CMOS technology is accompanied by the reduction of the power supply voltages. Power MOSFETs, with their high-voltage capabilities, were first introduced in the 1970s [1] to enable low-voltage integrated circuits to work together with power devices. Among the wide variety of power MOSFETs, lateral diffused metal-oxide-semiconductor (LDMOS) is the device of choice because of its great compatibility with standard CMOS process flow. By incorporating LDMOS transistors with low-voltage integrated circuits, the high-voltage integrated circuits (HVICs) [2] are developed and vastly utilized in numerous applications such as automotive electronics, display drivers and aircraft controls.

In order to withstand large voltage drop, a drift region is included in a typical LDMOS structure. This region is covered with field oxide, making heat dissipation very difficult. During high voltage operations, heat starts to build up in the drift region and self-heating effect (SHE) ensues. In the first part of this thesis, we will present a new SHE characterization method—the internal voltage (V_I) method. A novel LDMOS structure with an extra metal contact is fabricated and self-heating induced internal voltage transient is studied. In addition, the internal voltage measurement data will also reveal properties of the channel region of LDMOS.

Despite being widely utilized, the LDMOS device still lacks a simple and accurate model. Many studies regarding this subject has been put forth [3-8], however, the effect of self-heating is not considered. Therefore, in the second part, we emphasize on developing an internal-voltage-based SPICE model including

self-heating effect.

This thesis is organized as follows: Chapter 1 is introduction. Chapter2 demonstrates a new LDMOS characterization method by using a novel metal contact structure. Chapter3 presents a SPICE model including self-heating effect. A brief conclusion is given in Chapetr4. The organization of thesis is illustrated in Fig. 1.1.



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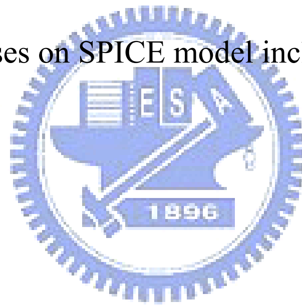


Chapter 2
A Novel Metal Contact Structure for Self-Heating and Device Characterization

2.1 Introduction

Self-heating effect has been recognized as one of the major reliability issues in LDMOS [9], particularly when the device is utilized in today's high-voltage/high-current operations. This effect results in an increase of device temperature and a reduction of drain-current [10]. To characterize SHE, a conventional drain-current method [11] is generally used to monitor self-heating effect and the corresponding thermal time constant. In this method, a short voltage pulse is applied to gate, and drain-current is extracted from a voltage drop of an external resistor [11]. The varying drain-current in self-heating condition, however, results in a varying voltage drop across the resistor and thus an ambiguous thermal time constant. This may lead to an unreliable SHE study or SPICE model. Therefore, a new characterization method, which avoids the issue of varying voltage drop, is essential for a more accurate self-heating study.

2.2 A Novel LDMOS Structure for Internal Voltage Measurement

2.2.1 Device Structure

A cross section of the LDMOS is shown in Fig. 2.1(a). It consists of two regions, the MOS region and drift region. The voltage at the junction of two regions is indicated as the internal voltage. This internal voltage is equal to the drain voltage of

the intrinsic MOS. Probing the internal voltage enables us to directly extract properties of the intrinsic MOS. To this purpose, an n+ implant is formed near the bird's beak. The contact area is very small and thus does not affect the overall device electrical characteristics. The device used in this work was processed in a 0.18μm CMOS technology with width=20μm and channel length=3μm. The gate oxide thickness and field-oxide thickness are 110nm and 450nm respectively. The operational voltages are V_G/V_D =40V/40V.

2.2.2 Internal Voltage Transient

A fast transient measurement setup including a digital oscilloscope is built, as shown in Fig. 2.1(b). A gate voltage pulse and constant drain voltage (V_D=40V) are applied in the V_I transient measurement. The transient measurement result is shown in Fig. 2.2. At V_G=40V, V_I is independent of pulse time in the beginning and then decreases with pulse time. The decrease of V_I is attributed to self-heating induced mobility degradation in the drift region [12][13], thus resulting in a larger drift region resistance and a smaller V_I. As the applied voltage pulse is long enough, the V_I becomes stable and is independent of pulse time again. Since heat in the LDMOS can be dissipated through the silicon substrate toward the backside of the wafer, heat generation/dissipation rates will reach equilibrium and thus a stable V_I at a longer pulse time can be observed. In addition, at smaller gate pulse there is less power consumption and thus a smaller V_I decrease.

2.3 Comparison of the V_I Method and Conventional I_D Method

For a comparison, the V_I method and the conventional I_D method [11] are both presented in Fig. 2.3(a) and (b) respectively. The V_I in transient measurement (equal to V_I w/o SHE) is extracted at gate pulse=5μs and the V_I in DC measurement (equal to V_I w/ SHE) is measured by Agilent 4156. At V_G/V_D=40V/40V, self-heating induces an 8% change in I_D and a 23% change in V_I, as indicated by an arrow in Fig. 2.3. A larger reduction in the V_I method than in the I_D method is noticed. The possible reason for a larger V_I reduction can be explained by plotting the relation between I_D and V_I, as shown in Fig. 2.4. When self-heating occurs, the device is operating in high V_G/V_D. A V_I reduction of 23% (ΔV_I) at V_G/V_D=40V/40V and the corresponding I_D reduction (ΔI_D) are indicated. It shows clearly that a large change in V_I only corresponds to a small change in I_D in the saturation region. Consequently, the V_I method is more sensitive than then the conventional I_D method for self-heating characterization.

2.4 Comparison of LDMOS/MOS Characteristics

One of the purposes of measuring V_I, as we have mentioned in section 2.2.1, is to obtain characteristics of the intrinsic MOS. Therefore, a comparison of the I-V of the LDMOS (I_D-V_D) and the intrinsic MOS (I_D-V_I) in the low-V_G region is shown in Fig. 2.5(a). We observe that the I-V of the intrinsic MOS and the LDMOS in linear region and saturation regions are almost identical. This implies that V_I is close to V_D and the LDMOS performance is dominated by the intrinsic MOS at low V_G.

A similar comparison of the characteristics of the intrinsic MOS and the LDMOS in the high-V_G region is presented in Fig. 2.5(b). At small V_D, the drain current of the intrinsic MOS and the LDMOS are very close, indicting that the intrinsic MOS still

dominates the LDMOS characteristics in the linear region. However, a significant current difference is observed in the saturation region, implying a large voltage drop in the drift region. Thus, the saturation characteristics of the device are controlled by both the intrinsic MOS and the drift region. This is commonly known as the quasi-saturation effect [7].

The characterization leads to a possible LDMOS modeling technique: We may use an intrinsic MOS model to control the low-V_G LDMOS characteristics and another component to model the device I-V in the high V_G region.

2.5 Summary

In summary, a novel internal-voltage method has been developed to characterize self-heating effect in an n-LDMOS. A self-heating induced V_I transient is characterized for high gate voltage pulse. This method shows higher sensitivity than the conventional drain current method. Finally, a possible two-component LDMOS model has emerged from our comparison of LDMOS/MOS characteristics.

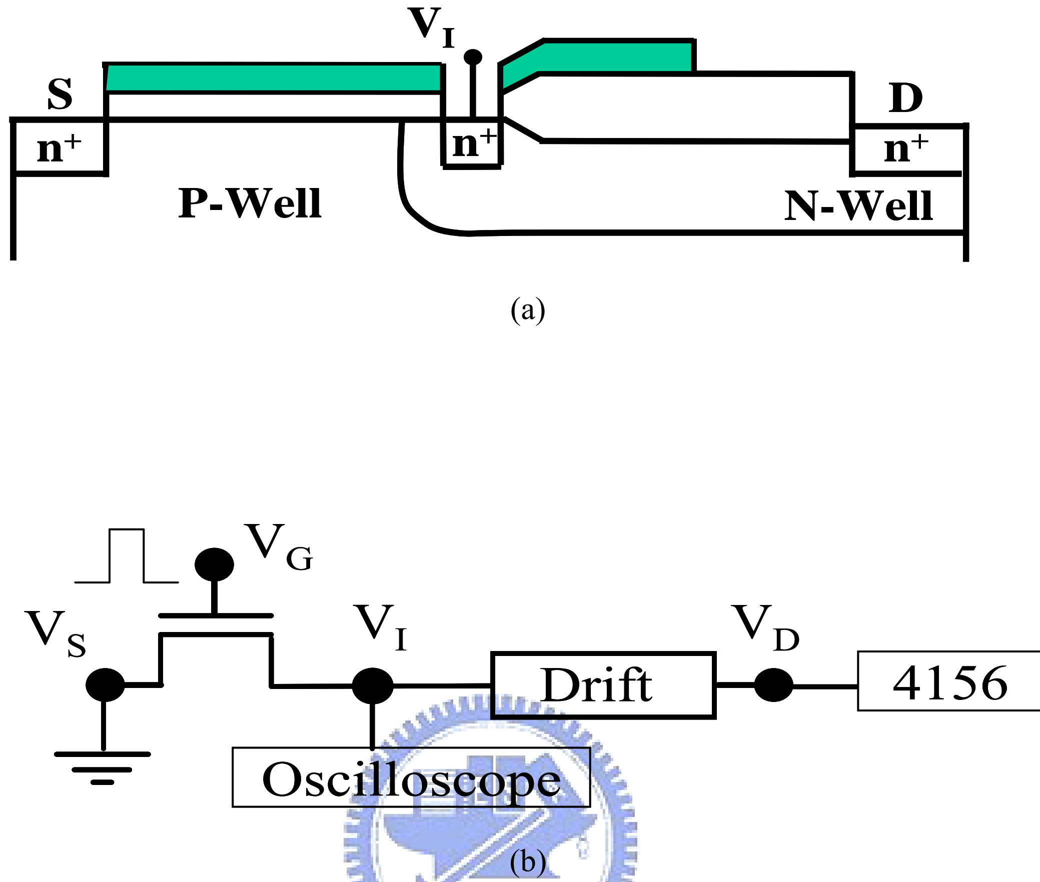


Fig. 2.1 (a) Cross-section of a novel LDMOS structure. The metal contact (V_I) is arranged in the bird's beak region with an n+ implant.

(b) Transient measurement setup for internal-voltage characterization.

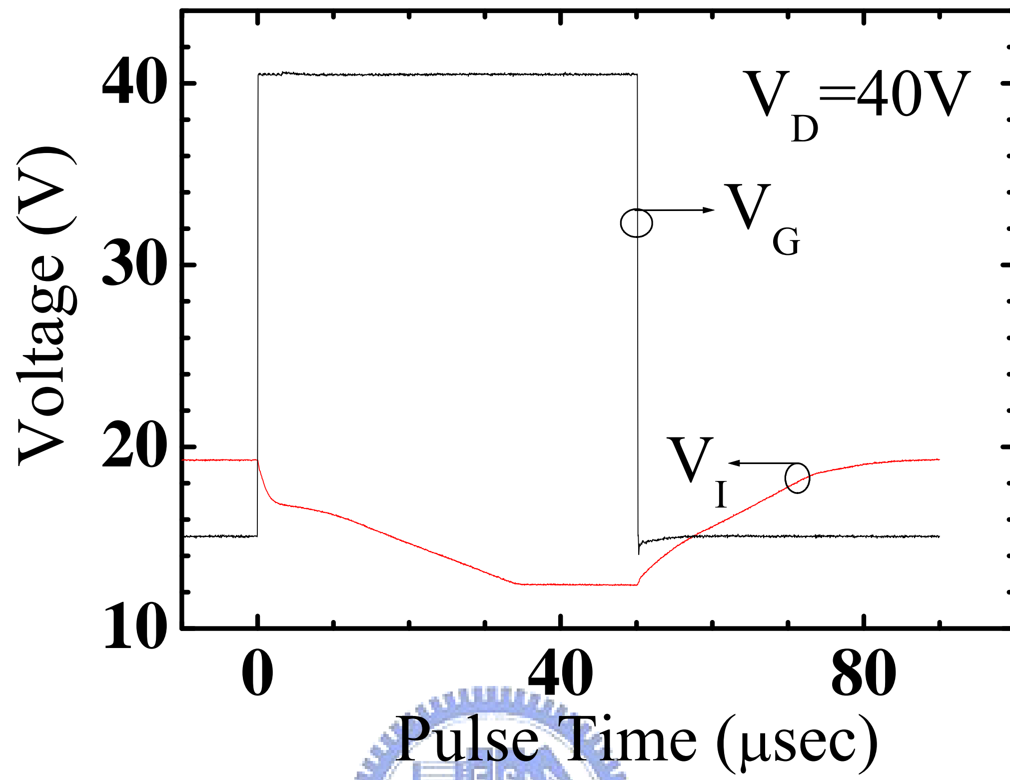
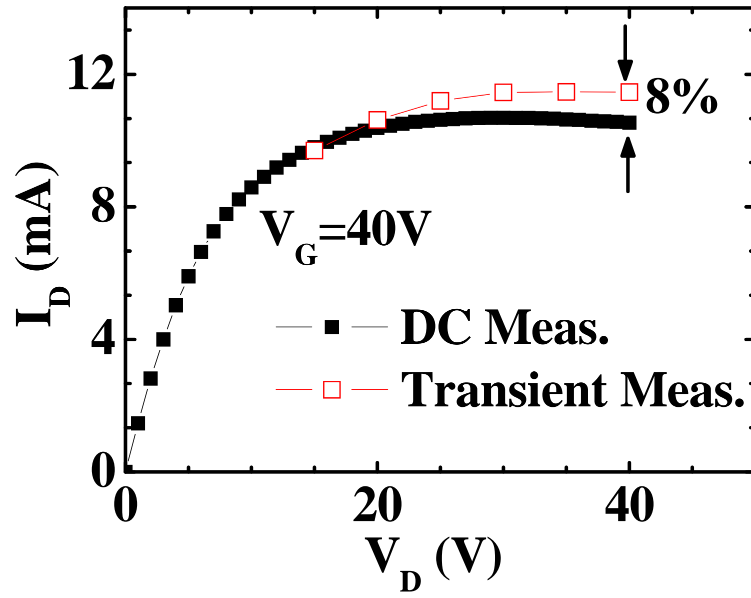
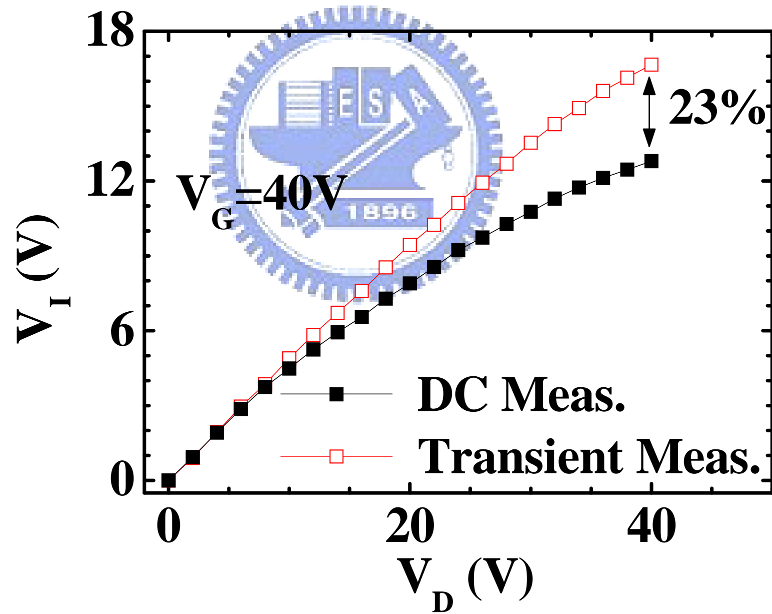


Fig. 2.2 Transient V_I measured at high gate voltage pulse. Self-heating induced V_I decrease is observed.



(a)



(b)

Fig. 2.3 (a) I_D versus V_D in SHE (DC Meas.) and SHE-free (Transient Meas.) conditions. At V_G/V_D=40V/40V, SHE induces 8% change in drain current.

(b) V_I versus V_D in SHE and SHE-free conditions. A 23% change caused by SHE is seen at V_G/V_D=40V/40V.

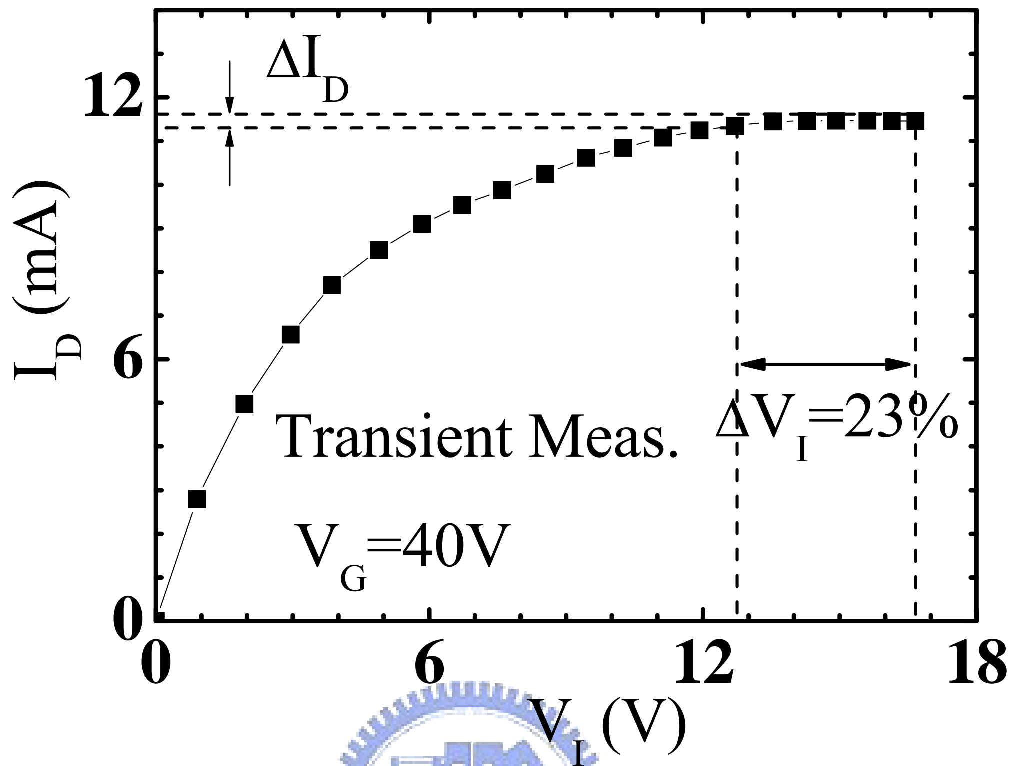
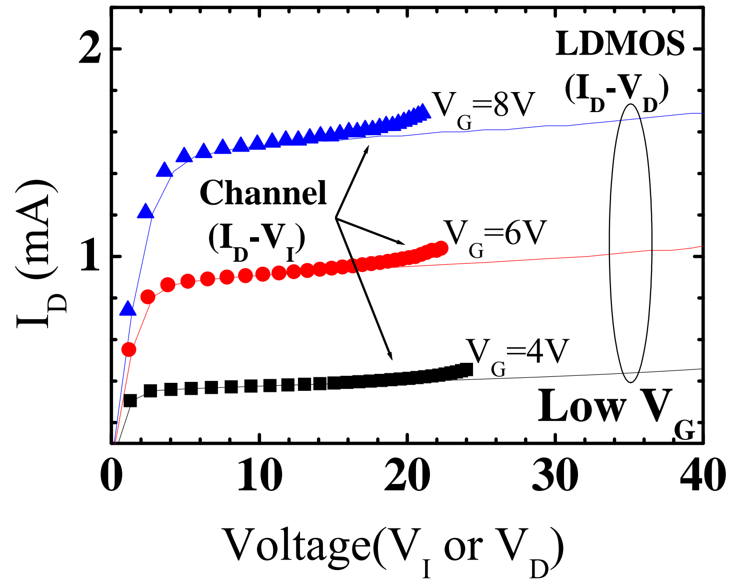
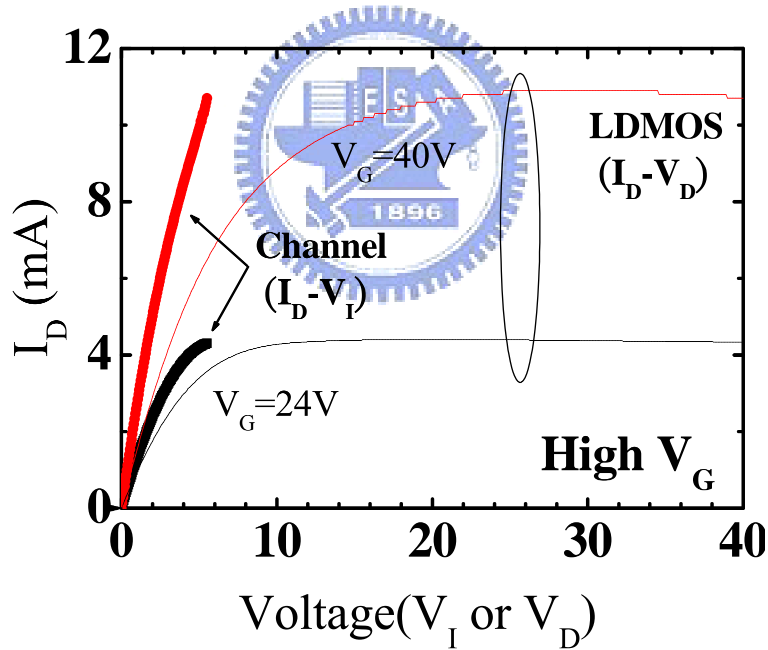


Fig. 2.4 I_D versus V_I at V_G=40V. In the saturation region, a V_I change of 23% corresponds to a relatively small change in I_D.



(a)



(b)

Fig. 2.5 (a) Current versus voltage of the LDMOS (I_D-V_D) and the intrinsic MOS (I_D-V_I) in the low-V_G region. The I-V of the intrinsic MOS and the LDMOS in linear region and saturation regions are almost identical.

(b) High-V_G current versus voltage of the LDMOS and the intrinsic MOS. A significant current difference is observed in the saturation region.

Chapter 3
An Internal-Voltage-Based SPICE Model Including Self-Heating Effect

3.1 Introduction

The efficiency of the LDMOS circuit depends tremendously on the device model. A precise model greatly enhances the device performance. However, characterization of LDMOS is rather difficult compared to conventional MOSFET due to the diverse nature of the channel region and drift region. A major obstacle is the characterization of drift region because of its complex dependence on external terminal voltages. A common approach to cope with this issue is by using the internal voltage to separate the channel and drift region and model the two regions independently. Many modeling approaches have been developed to solve the internal voltage [3-8]. Most of them used a numerical iteration procedure to solve the internal voltage with numerous fitting parameters [3-6]. Others solve for the internal voltage explicitly by equating the channel current with the drift region current [7-8]. However, none of the studies take into account the correlation between the internal voltage and self-heating effect.

In this chapter, a V_I-based LDMOS model including self-heating effect is presented. We have also developed a V_I simulation method, which produces the corresponding internal voltage of each drain current. Hence, our V_I-based model can be applied without actual fabrication of a special structure for V_I measurement. A simplified V_I equation with four fitting parameters is given explicitly in terms of the external terminal voltages. The model is finally simulated by an HSPICE simulator.

3.2 Model Description

3.2.1 Model Components

An equivalent circuit of the LDMOS is shown in Fig. 3.1(a). The circuit model consists of two components, an intrinsic MOS and a V_I controller. We denote the current flow through the MOS model as I_{ch} to distinguish it from the drain current I_D. Fig. 3.1(b) illustrates the operation regions controlled by the two components respectively. The low-V_G region and the linear high-V_G region are controlled by the MOS model. The saturation high-V_G region is controlled by the MOS model and the V_I controller.

3.2.2 Model Process

Fig. 3.2 is an illustration of our SPICE model process. First, the external gate and drain voltages are the input to the V_I controller. The V_I controller generates the corresponding V_I, which is then set as the input drain voltage of the MOS model. After that, the MOS model produces the final I_D according to its input voltages. The operation of the MOS model is well understood. Hence, we will explain how the V_I controller generates the correct V_I.

The process of the V_I controller is specified in Fig. 3.3. When a pulse gate or drain voltage is applied and self-heating is induced, V_I controller generates two terms. One is the V_I at pulse time t=0, which equals the non-self-heating V_I. The other term is the self-heating induced V_I change at pulse time t>0. In this way, a model value of V_I at any pulse time t is obtained.

After introducing our model concept, we will demonstrate in detail how the model is built in the next section.

3.3 Modeling Flow

A specially-designed LDMOS modeling flow is shown in Fig. 3.4, including five steps: (1) and (2) MOS parameters extraction, (3) V_I simulation, (4) V_I model, and (5) LDMOS model.

3.3.1 MOS Parameter Extraction

In step 1, the measurement I-V data of LDMOS is divided into the low-V_G data and the high-V_G data. The low-V_G MOS model is built on the MOS parameters extracted from the LDMOS low-V_G data. A comparison of the measurement data and the fitting results after step 1 is shown in Fig. 3.5. Then, the MOS model is extended to high-V_G using the high-V_G data in the linear region in step 2. Fitting results after step 2 is shown in Fig. 3.6. Step 1 and 2 are actually carried out at the same time, using built-in MOSFET model in BSIM3v3. At this point, we have completed the MOS model, which will be utilized in the next step—V_I simulation.

3.3.2 V_I Simulation

In this step we will deal with the LDMOS I-V in the high V_G/V_D region, which is supposed to be controlled by both the MOS model and the V_I controller. Our goal is to obtain the corresponding V_I of each I_D, so that in the next step we can build the V_I model based on the simulation V_I data. The V_I simulation method is illustrated in detail in Fig. 3.7. Using the LDMOS drain current as an input current source to the MOS model, we can obtain the corresponding output V_I. A typical V_I simulation result is illustrated in the inset of Fig. 3.7. Note that the V_I-V_D simulation result has the same saturation characteristics of the LDMOS I_D-V_D measurement. Consequently, V_I is limited in the saturation region and the current produced by the MOS model will also

exhibit the same saturation characteristics as the LDMOS measurement current.

3.3.3 V_I Model

The V_I model describing the internal voltage transient is established by integrating a non-self-heating V_I model with a self-heating induced V_I change. The non-self-heating V_I model is denoted by V_I (t=0), implying the V_I at pulse time t=0. V_I equations with both V_G and V_D dependence are used in the non-self-heating model, which are derived as follows. First, an LDMOS current equation with two fitting parameters, θ_{md} and n, is expressed as:

$$I_D(V_G,V_D) \approx \frac{W}{L}\cdot C_{ox}\cdot\frac{\mu_0}{1+\theta_{md}\cdot(V_G-V_t)^n}\cdot(V_G-V_t-\frac{V_D}{2})\cdot V_D$$

The MOS model current in the linear region is expressed as:

$$I_{ch}(V_G,V_I) \approx \frac{W}{L}\cdot C_{ox}\cdot\mu_0\cdot(V_G-V_t-\frac{V_I}{2})\cdot V_I$$

Since the LDMOS current is equal to the intrinsic MOS current, equating the currents we get an expression for V_I:

$$V_I(V_G,V_D) \approx (V_G-V_t)-\sqrt{(V_G-V_t)^2-2\cdot\frac{(V_G-V_t-\frac{V_D}{2})\cdot V_D}{1+\theta_{md}\cdot(V_G-V_t)^n}} \qquad (1)$$

We arrive at an expression for the LDMOS current:

$$I_D(V_G,V_I)=\begin{cases}\frac{W}{L}\cdot C_{ox}\cdot\mu_0\cdot(V_G-V_t-\frac{V_I}{2})\cdot V_I & V_D\leq V_{Dsat}\\ \frac{W}{L}\cdot C_{ox}\cdot\mu_0\cdot(V_G-V_t-\frac{V_{Isat}}{2})\cdot V_{Isat} & V_D>V_{Dsat}\end{cases}$$

The linear drain current is simply obtained using equation 1 for V_I. For the current in the saturation region, V_I is substituted by V_{Isat},

where $V_{Isat}(V_G)=V_I|_{V_D=V_{Dsat}}=(V_G-V_t)-\sqrt{(V_G-V_t)^2-2\cdot\frac{(V_G-V_t-\frac{V_{Dsat}}{2})\cdot V_{Dsat}}{1+\theta_{md}\cdot(V_G-V_t)^n}}$ (2)

and $V_{Dsat}(V_G)=\frac{(V_G-V_t)}{1+\gamma\cdot(V_G-V_t)}$, with fitting parameter γ.

So far we have acquired an expression for linear region V_I (equation 1) and an expression for saturation region V_I (equation 2). We now introduce an effective V_I [14] to express V_I in both linear and saturation regions as a single equation:

$$V_{I,eff}(V_G,V_D)=V_{Isat}-\frac{1}{2}\cdot[V_{Isat}-V_D-\Delta+\sqrt{(V_{Isat}-V_D-\Delta)^2+4\Delta\cdot V_{Isat}}] \quad (3)$$

There is a fitting parameter Δ determining the degree of smoothness in the quasi-saturation transition. Equation 3 includes four fitting parameters: θ_{md}, n, γ and Δ. Equations 1, 2 and 3 are plotted in Fig. 3.8 to further explain the concept. Fig. 3.9 shows the resulting non-self-heating V_I model built by the model equations.

The LDMOS transient characteristics when a gate or drain voltage pulse is applied are controlled by the ΔV_I transient model. Fig. 3.10 shows the transient I_D and the corresponding transient V_I obtained by V_I simulation method. In an attempt to

describe the transient V_I by an exponential decay function, our model utilizes an RC sub-circuit shown in Fig. 3.11. The sub-circuit is composed of three components: a current source, R and C. RC is the time constant of the V_I transient. The voltage drop across RC is modeled as the SH-induced V_I change, denoted as $\Delta V_I(t)$. In transient operation, the current source starts to charge the capacitor C and $\Delta V_I(t)$ increases. When the capacitor becomes fully-charged, $\Delta V_I(t)$ maintains a constant value, which is equal to the value β extracted from Fig. 3.10. Also extracted from Fig. 3.10 is the time constant τ_C.

A comparison between the simulation and model $\Delta V_I(t)$ and $V_I(t)$ is shown in Fig. 3.12. The $V_I(t)$ is modeled as $V_I(t) = V_I(t{=}0) - \Delta V_I(t)$. Time-dependent V_I and ΔV_I equations can be expressed as

$$V_I(t) = V_I(\infty) + \beta \cdot \exp\left(-\frac{t}{\tau_C}\right)$$

$$\Delta V_I(t) = \beta \cdot \left[1 - \exp\left(-\frac{t}{\tau_C}\right)\right]$$

By incorporating the MOS model and the V_I model, the macro model is finally acquired. The model is performed by an HSPICE simulator and the modeling results will be presented in the next section.

3.4 Results and Discussions

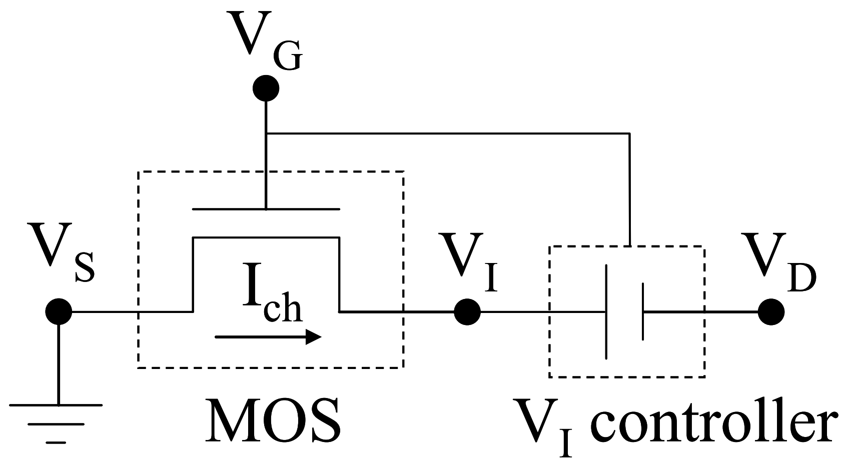
In the following figures, symbols correspond to the measurement data, while the solid lines represent the LDMOS model.

Fig. 3.13 shows the drain current transient when a gate voltage pulse is applied. Since our V_I model has described the V_I simulation transient correctly, the macro model can also successfully describe the I_D measurement transient.

The model I_D transient at t=0 and t=30μs are extracted as the model drain current w/o SHE and w/ SHE respectively at various V_G/V_D to form the I_D versus V_D results in Fig. 3.14. In the low-V_G region, no self-heating is observed and only one curve is shown for each gate voltage. By a comparison with the MOS model in step 1, we notice that the macro model current level is slightly lower than the MOS model current level in the low V_G region, which is due to subsequent use of the V_I controller. In the high V_G region, both SHE-free and SHE drain currents are shown for V_G=24V and V_G=40V. Once again, at V_G=40V the model current is largely suppressed compared to the MOS model current and matched with the LDMOS measurement current level. This again is due to the V_I controller which limits the V_I value and restricts the MOS model output current.

In Fig. 3.15(a), modeling results of the linear characteristics of the LDMOS device are presented. An accurate linear drain current and transconductance G_m are achieved and thus the V_{TH} of the model is matched with that of the device. Note that as V_D is small, model equation 2 becomes $V_I \approx V_D$, implying that the device characteristic is dominated by the MOS model. Fig. 3.15(b) depicts the saturation characteristics of the LDMOS device. The drain current in the SHE condition exhibits serious quasi-saturation effect, indicating the effect of drift region on the saturation characteristics of the high-V_G region.

The drain currents in both high-V_G and low-V_G regions are well described by our model. A good agreement between model and measurement results has proven that the V_I controlled self-heating model is successfully used in the LDMOS device.



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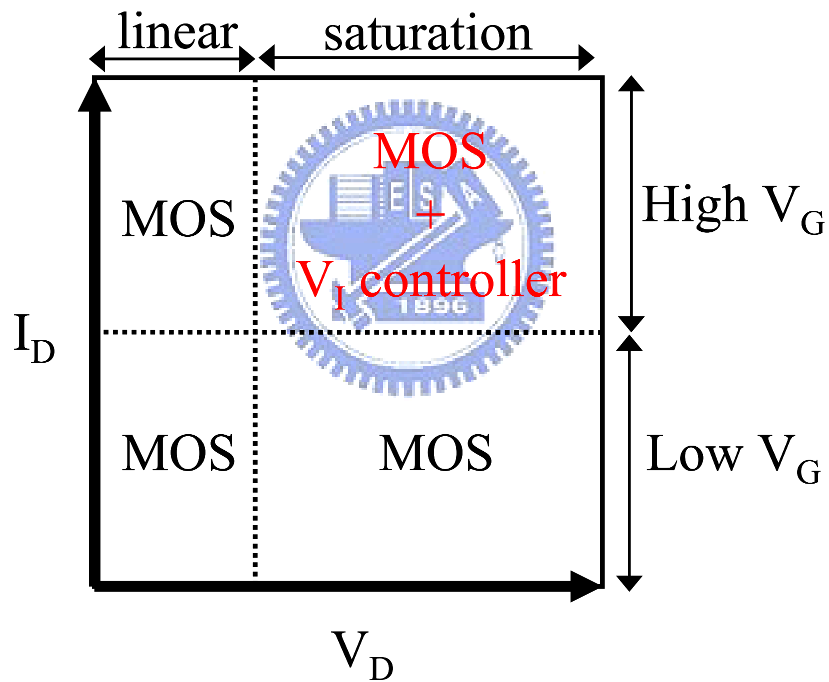


(b)

Fig. 3.1 (a) Equivalent circuit model of the LDMOS device. The MOS represents the channel region while the V_I controller accounts for the drift region. (b) Illustration of different operation regions controlled by each component.

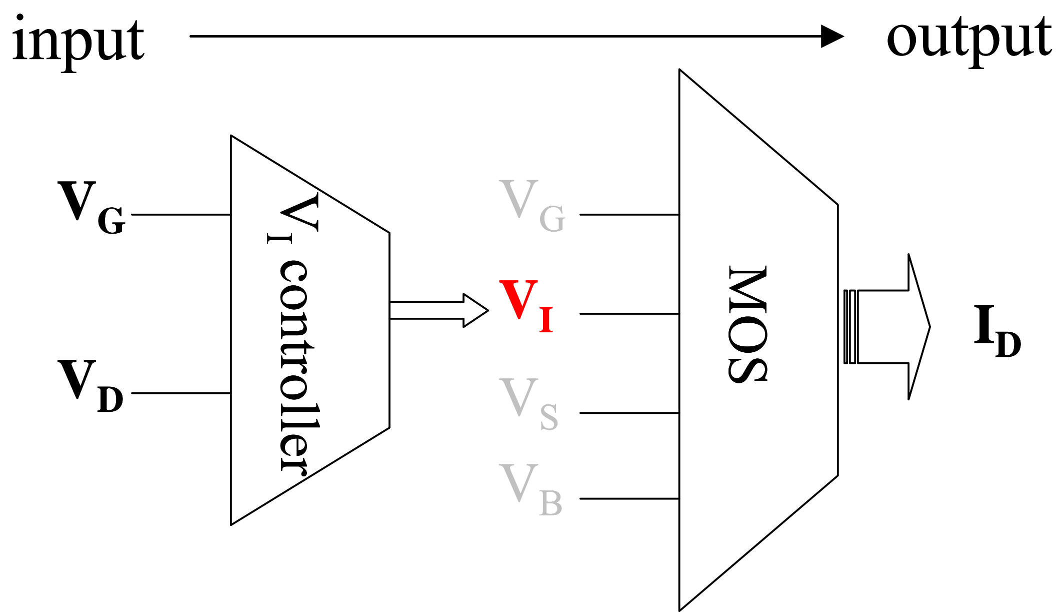


Fig. 3.2 Process of the V_I-based LDMOS model.

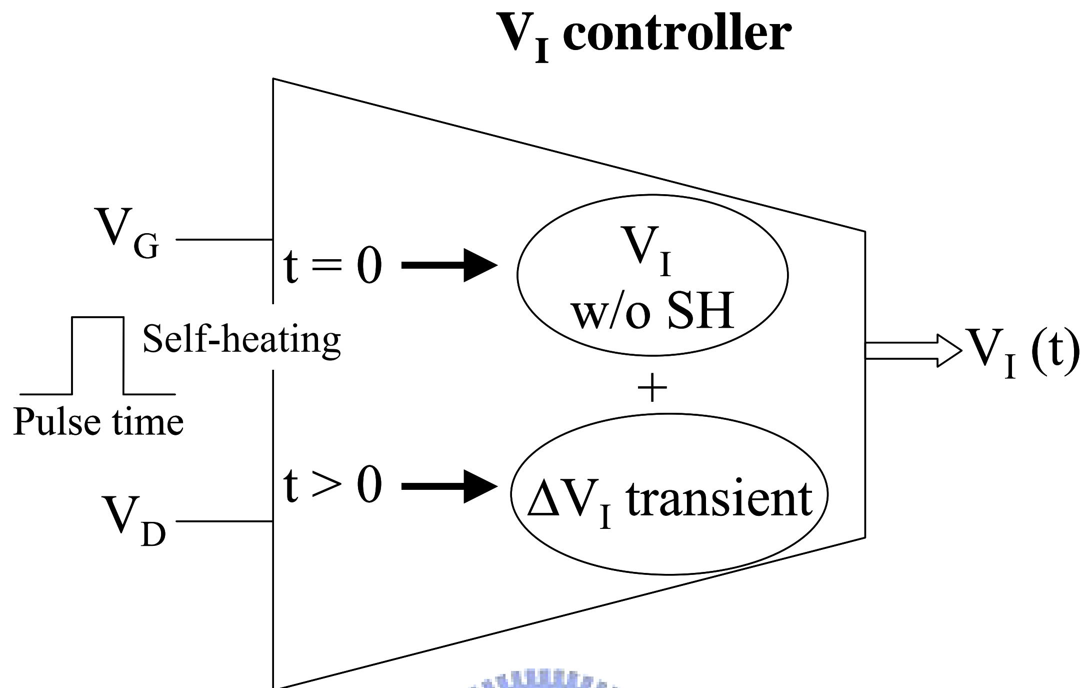


Fig. 3.3 Process of the V_I controller. Here self-heating effect is taken into account.

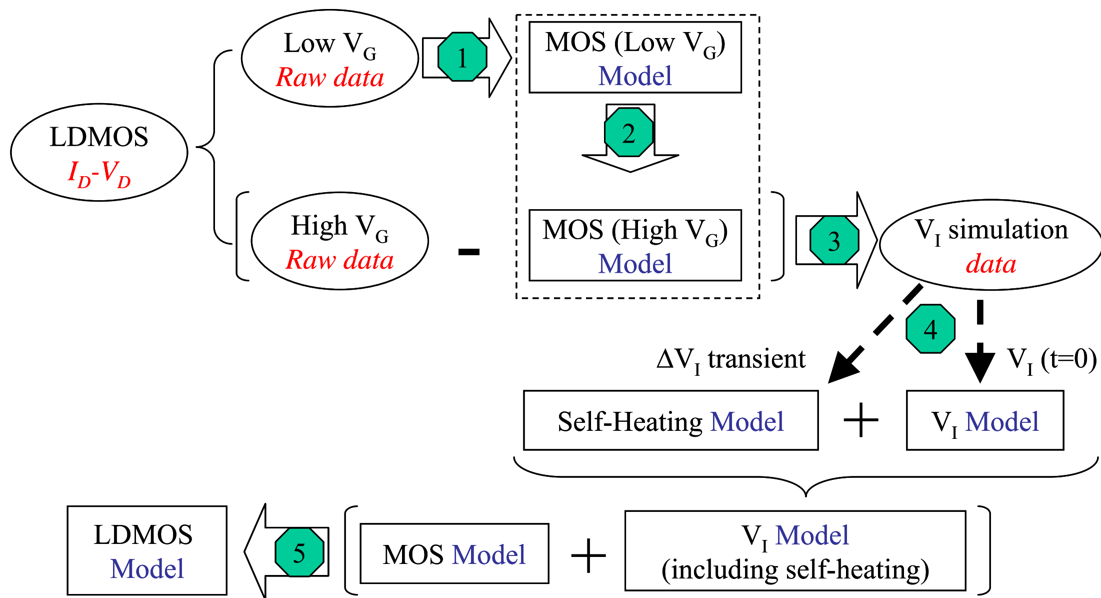
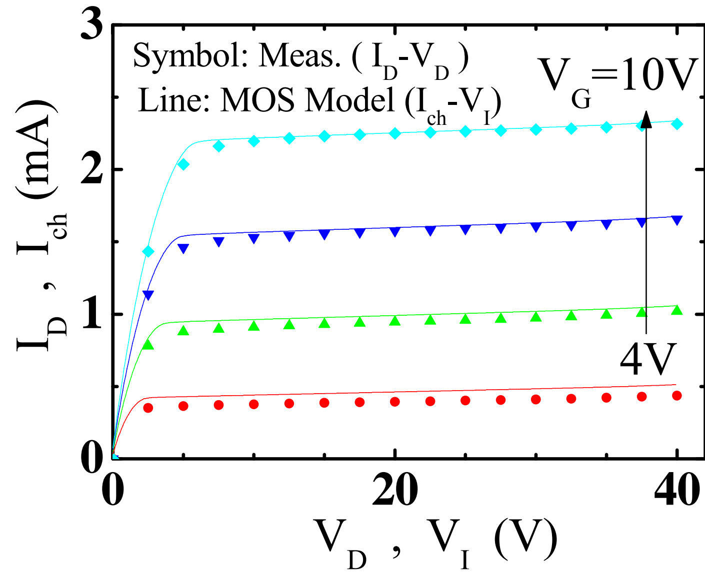


Fig. 3.4 A specially-designed modeling flow to set up the MOS model and the V_I model. Five steps are indicated, including (1) and (2) MOS parameter extraction, (3) V_I simulation, (4) V_I model, and (5) LDMOS macro model.



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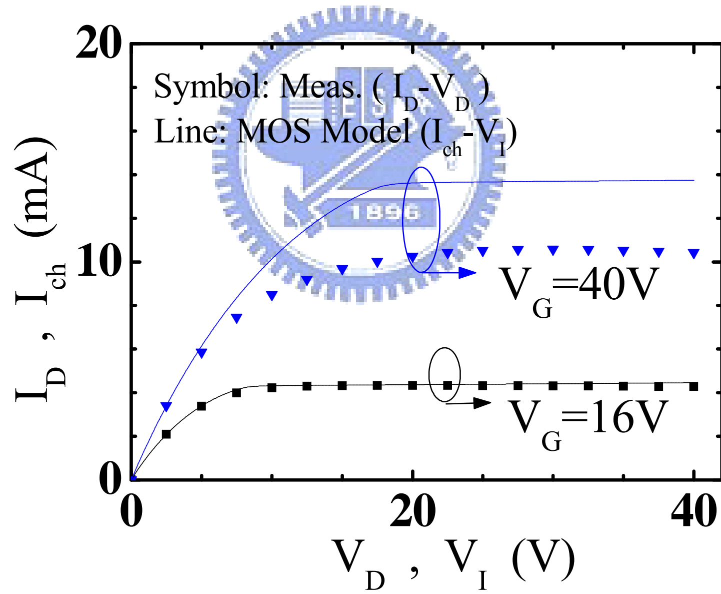

(b)

Fig. 3.5 A comparison of measurement data and model fitting results after step 1.

(a) Low-V_G and (b) High-V_G.

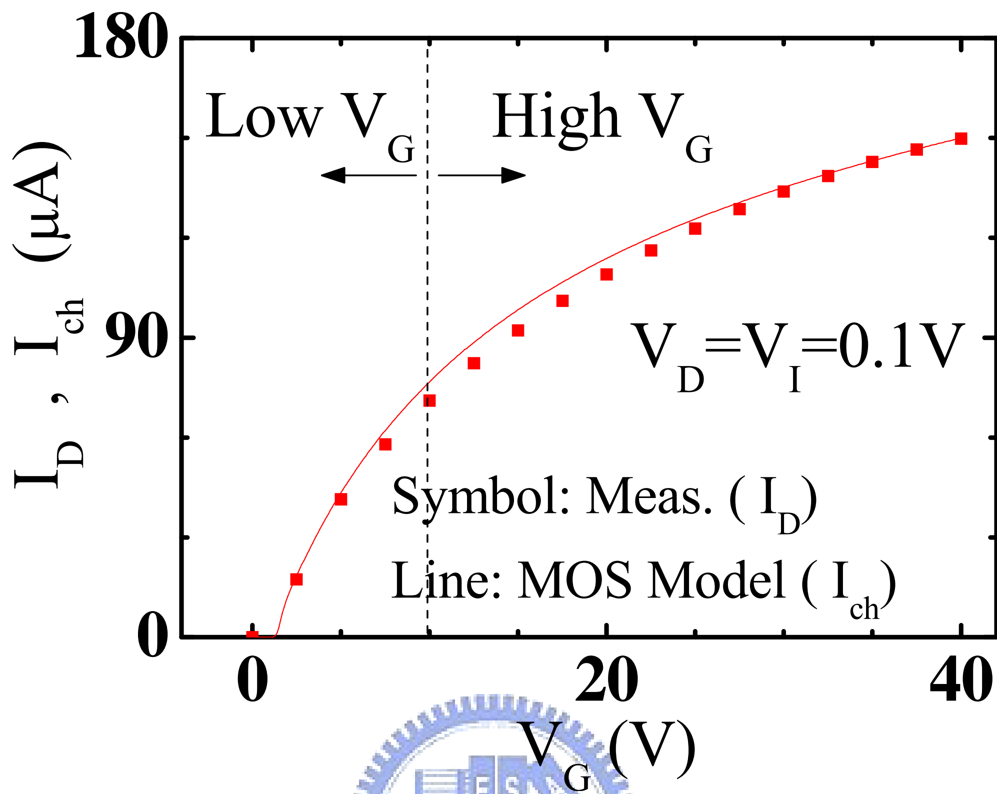

Fig. 3.6 A comparison of measurement data and model fitting results after step 2.

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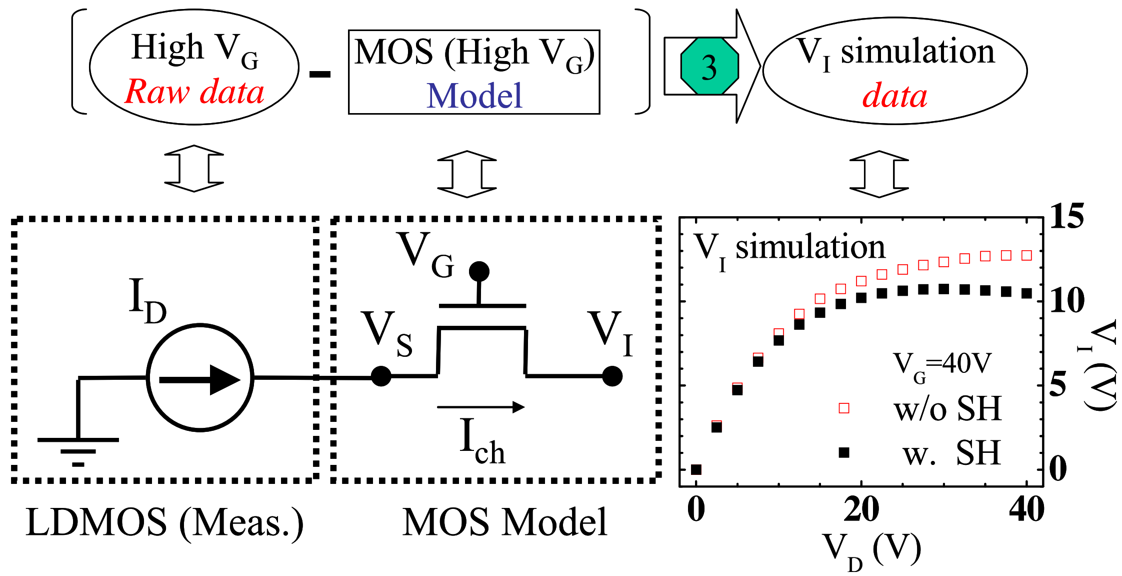


Fig. 3.7 A special simulation method to obtain internal voltage data from the input drain current. The MOS parameters are extracted from step 1 and 2. Typical V_I simulation result is plotted under self-heating (w. SH) and non-self-heating (w/o SH) conditions.

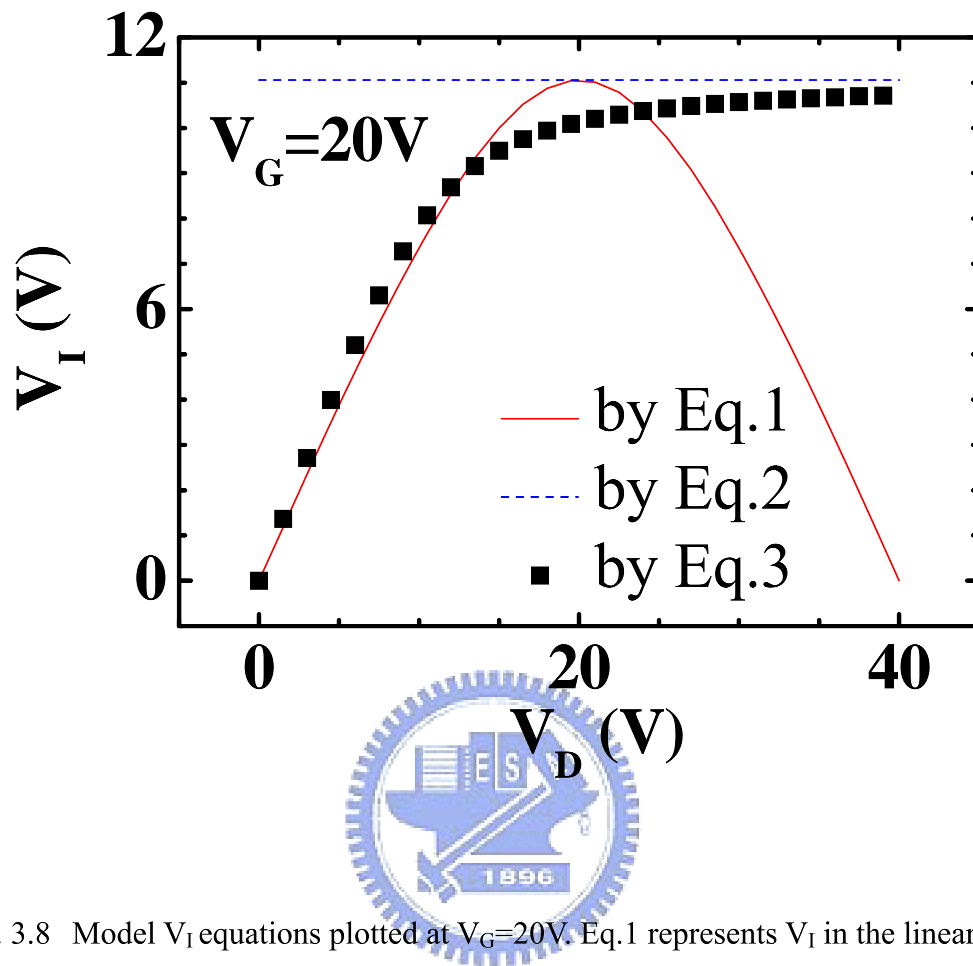
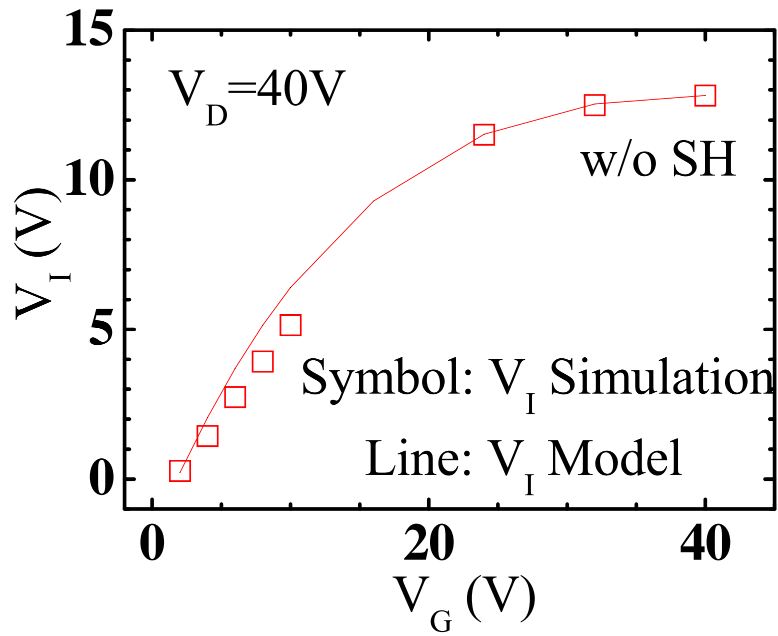


Fig. 3.8 Model V_I equations plotted at V_G=20V. Eq.1 represents V_I in the linear region while Eq.2 depicts saturation V_I. Eq.3 is the effective V_I for both linear and saturation regions.



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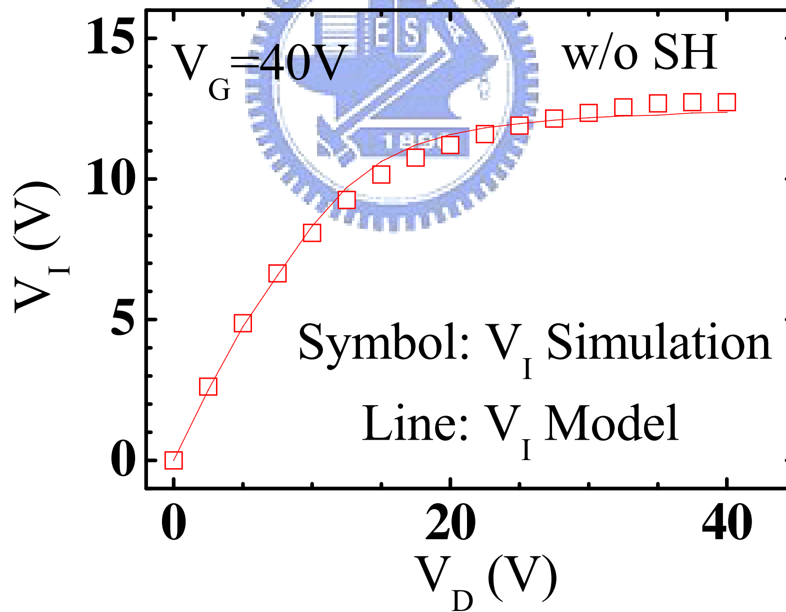


(b)

Fig. 3.9 Comparison of the non-self-heating V_I simulation data and the V_I model built by model equations. (a) V_I-V_G and (b) V_I-V_D.

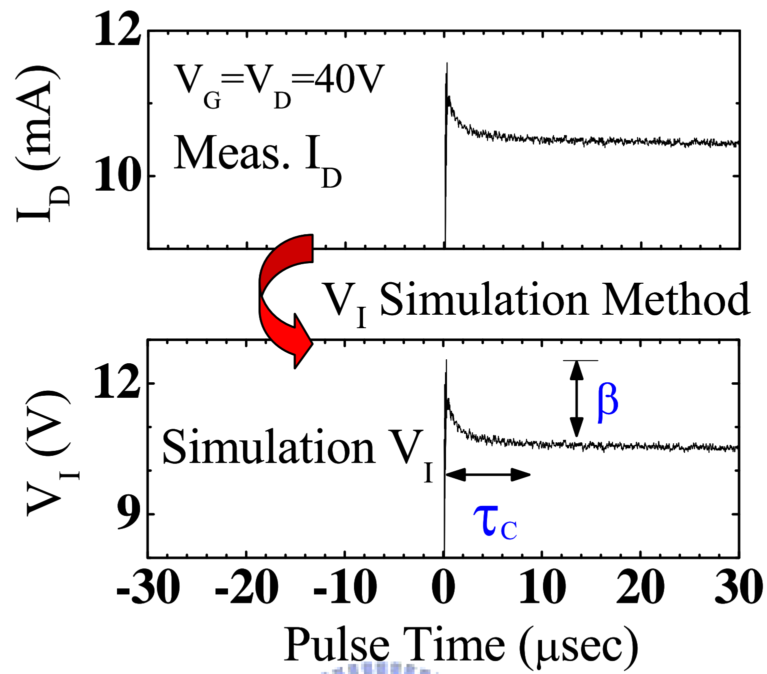
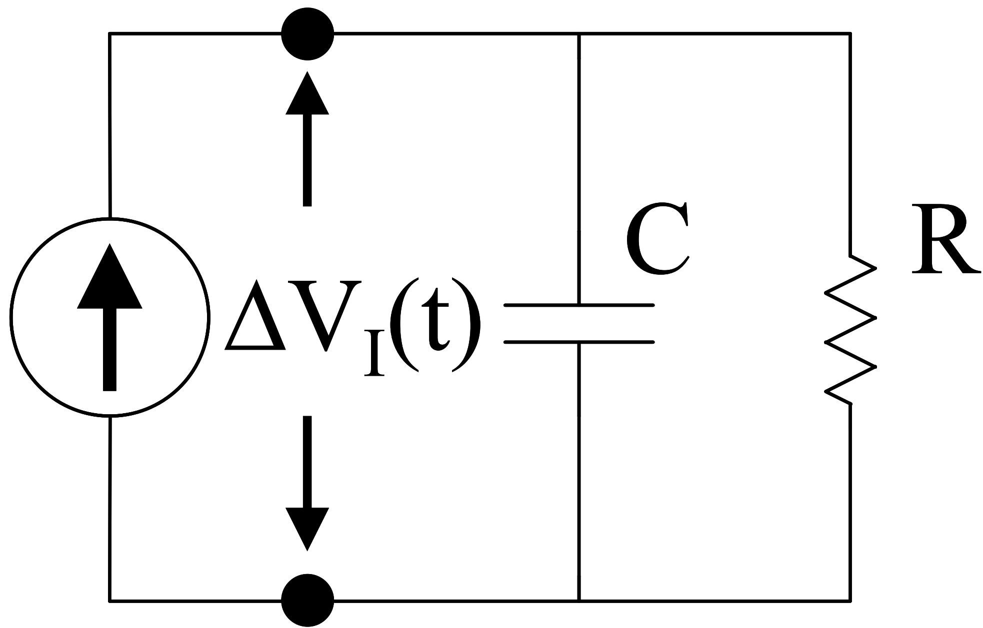


Fig. 3.10 I_D transient and the corresponding simulation V_I transient. The SH-induced total V_I change β and the time constant τ_C are extracted from the transient V_I.



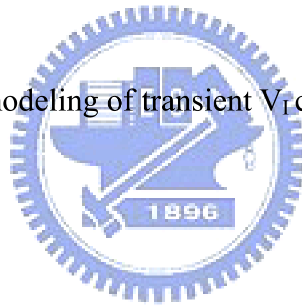


Fig. 3.11 RC sub-circuit for modeling of transient V_I change.

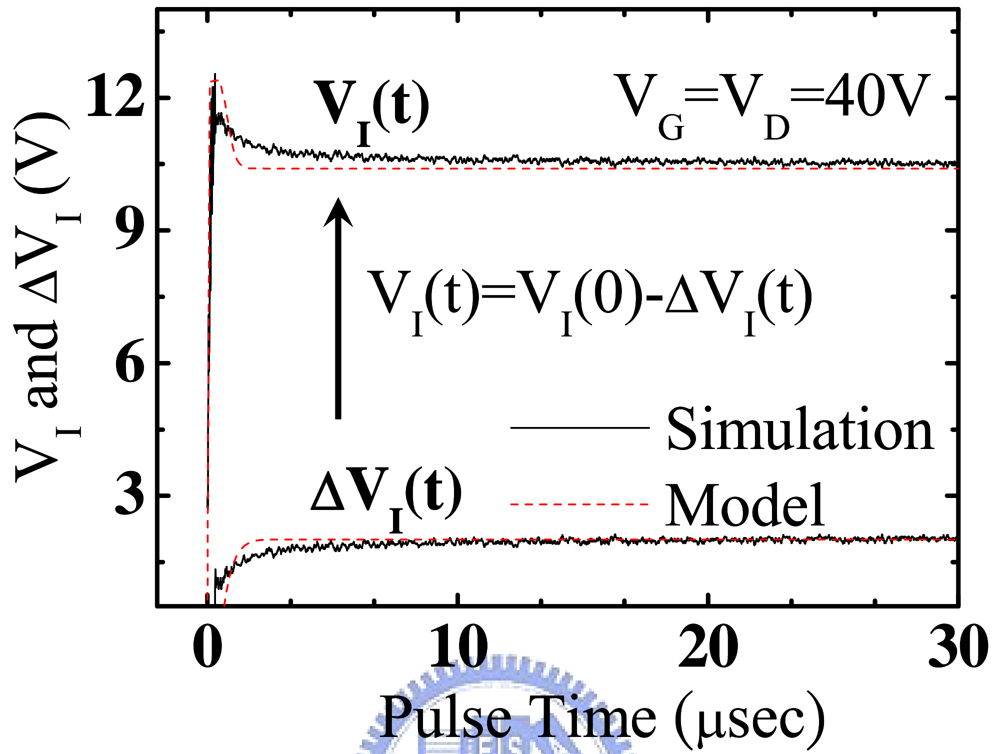


Fig. 3.12 Simulation and model $\Delta V_I(t)$ and $V_I(t)$.

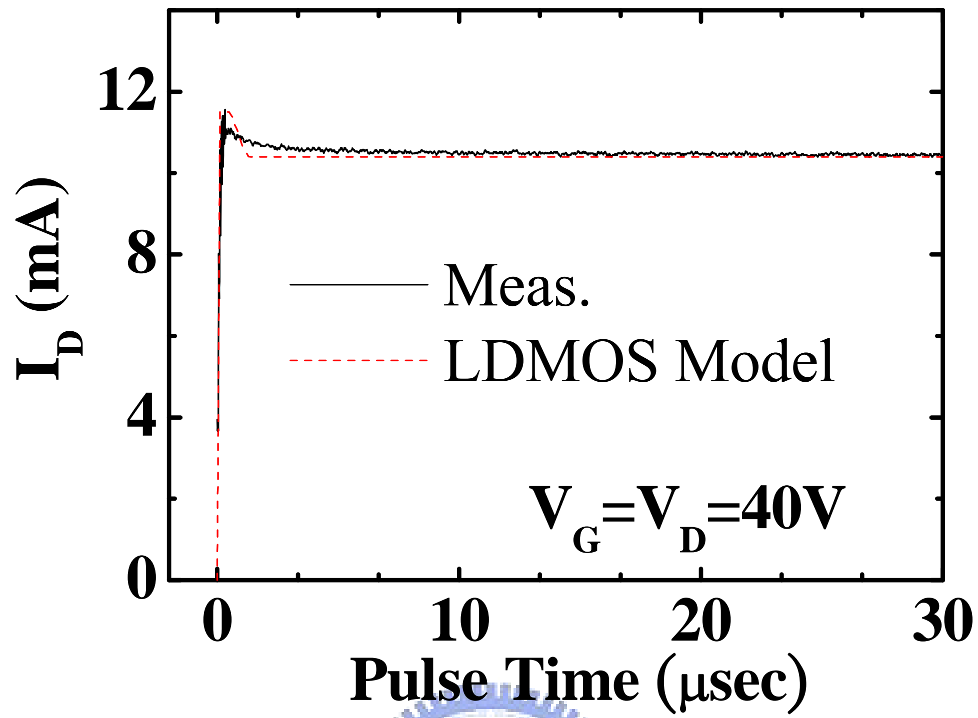
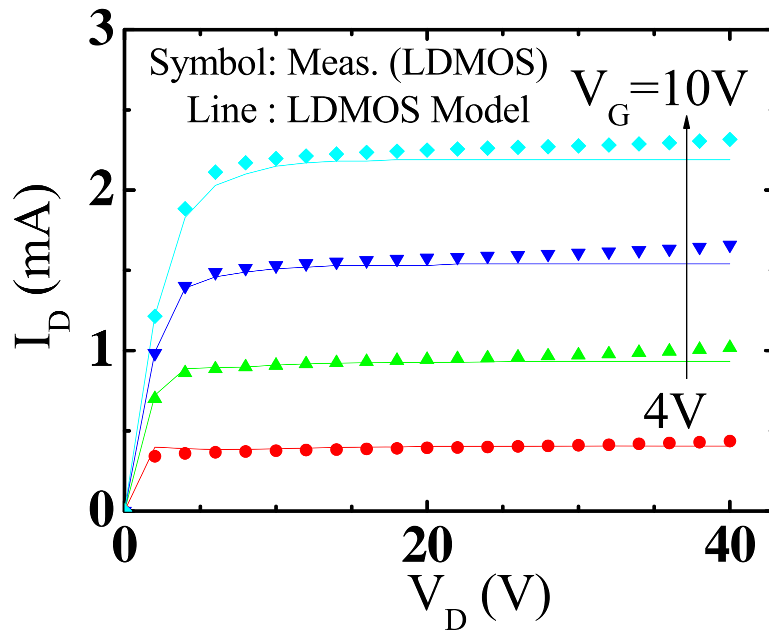


Fig. 3.13 Modeling result of the drain current transient at V_G=V_D=40V.



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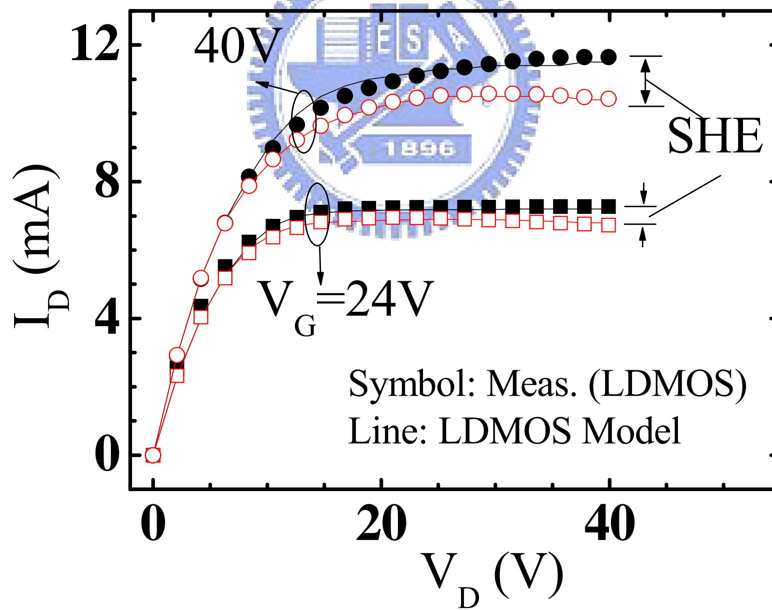
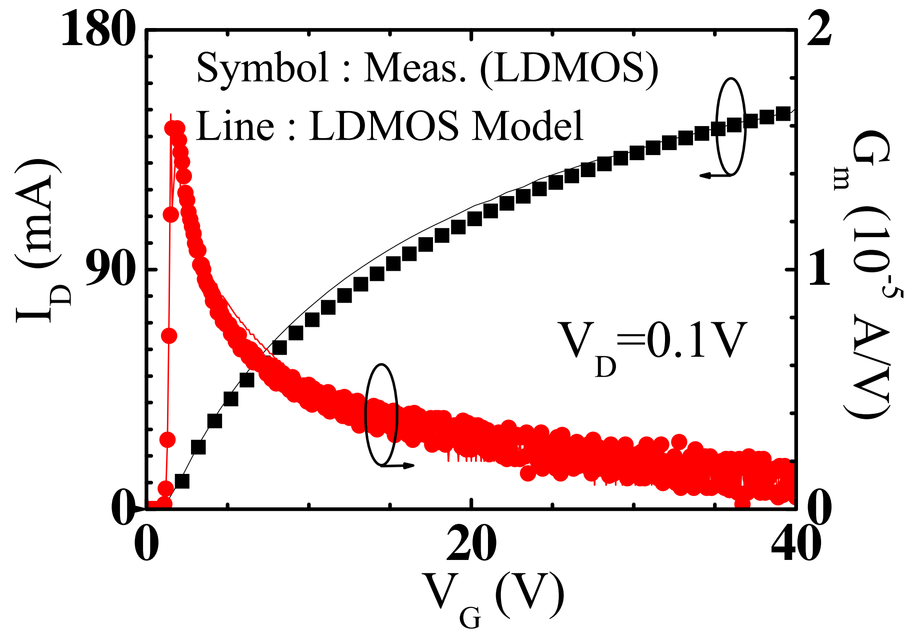


(b)

Fig. 3.14 Comparison of measurement and model I_D versus V_D at (a) Low-V_G and (b) High-V_G. The model drain current values w/o SHE and w/ SHE are extracted from the model I_D transient at t=0 and t=30μs respectively.



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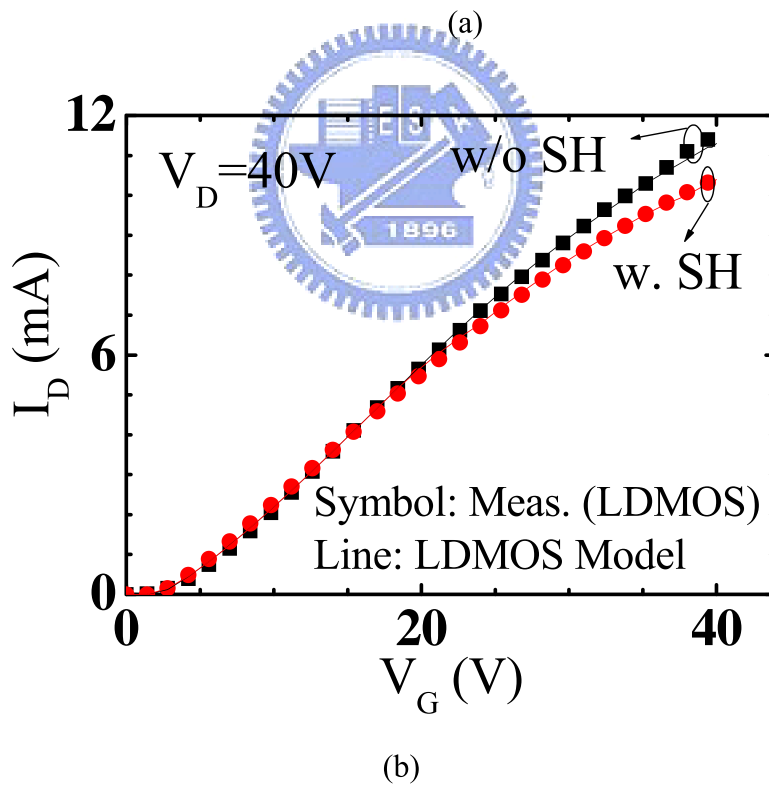

(b)

Fig. 3.15 Modeling results of I_D versus V_G in (a) linear region and (b) saturation region.

Chapter 4
Conclusion

A special LDMOS structure with an extra metal contact for internal voltage measurement has been fabricated and self-heating effect characterization by the internal voltage method is demonstrated. Self-heating induces more change in V_I than in I_D because of the nature of the device in the saturation region. A comparison of the intrinsic MOS and the LDMOS characteristics is presented. The intrinsic MOS dominates the low-V_G region of the device properties, whereas drift region dominates the high V_G/V_D region.

A complete V_I-based LDMOS model including self-heating effect is presented. Self-heating induced transient V_I change is accurately described by an RC sub-circuit. We also put forth simplified explicit V_I equations with only four major fitting parameters (Δ, γ, θ_{md}, n). Successful use of the LDMOS model in HSPICE simulator has proven that our LDMOS model can reach a very good agreement between measurement and model.

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碩士論文題目:

利用特殊接觸電極進行橫向擴散元件之
特性分析與 SPICE 模型建立

Characterization and SPICE Modeling of
Lateral Diffused MOS by using
a Novel Metal Contact Structure

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Appendix MOS Model Parameters extracted by BSIM3v3

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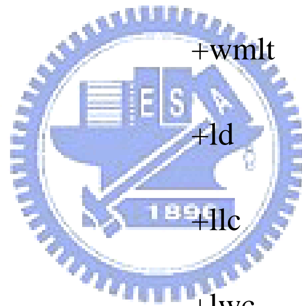

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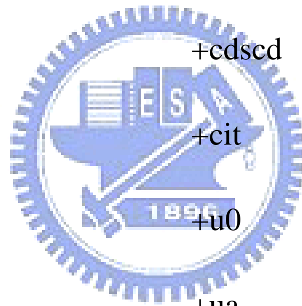

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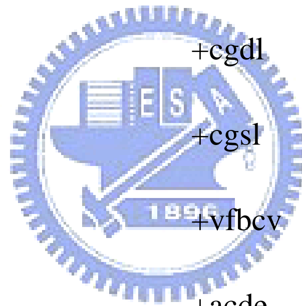

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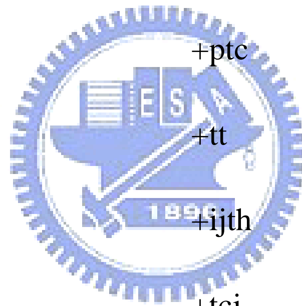

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