國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

一種改良的介面缺陷之橫向剖面分析應用於奈米級應變矽CMOS元件之可靠度探討

An improved Interface Traps Profiling on the Study of Reliability in Strained CMOS Devices

研 究 生 ：謝易叡

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中華民國 九十七 年 七 月

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摘要

本論文首次提出一種改良的新式直流電流-電壓量測法-βDC-IV(Boosted DC-IV)，此方法可成功地應用在EOT小於或等於 13 A^0以下的CMOS元件。另一方面，我們也首次完成氧化層之介面缺陷之橫向分佈，此法被成功地應用於偵測從通道至閘極邊緣的介面缺陷之可靠度研究。

本論文中，吾人利用上述所提及的量測方法來探討各種應變矽元件技術之可靠性分析， 並且獲致以下兩點主要的結論: (1) 對於應變矽 nMOSFET 元件而言，介電層覆蓋式(CESL)元件擁有較好的可靠度以及性能表現。應變絕緣層上矽(Strained Silicon-on-insulator, SSOI)元件擁有較好的熱載子抵抗能力，但其通道介面品質有待提升。矽碳化物(SiC)元件的效能提昇是明顯的，但是其汲極（drain）之接面品質必須改善。SiGe 元件擁有很好的性能提昇表現，但是其 Ge-out diffusion 的問題卻是必須克服的。 (2) 對於應變矽 pMOSFET 元件而言，SiGe 在 S/D 元件擁有較好的可靠度以及性能提昇表現。而 SiGe 在 channel 元件有較差的負偏壓不穩性(Negative Bias Temperature Instability, NBTI)表現。

隨著 CMOS 元件技術持續地演進，應變矽技術將越形重要，本論文對於如何利用應變矽技術設計一兼具可靠性與性能的優越 CMOS 元件提供重要設計準則。

An Improved Interface Traps Profiling on the Study of Reliability in Strained CMOS Devices

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Abstract

For the first time, an improved DC-IV measurement has been developed for the reliability study of devices with EOT down to $13A^0$, and also a new interface-trap lateral-profiling technique has been built. It can be used to accurately profile the interface traps distributions along the device channel.

By performing the above characterization and measurements, the reliabilities of the strain CMOS have been studied, from which two conclusions have been provided: (1) **For strained nMOSFETs,** nitride-capped devices are appreciated in terms of reliability and performance. SSOI devices have good hot-carrier immunity and performance, but its channel interface quality has to be improved. The performance of SiC devices is good, but the junction quality is worse. The SiGe on substrate devices exhibit very good performance, but the Ge-out diffusion effect is so serious that these

devices are unreliable. (2) **For strained pMOSFETs**, SiGe on S/D devices will be appreciated in terms of performance and reliability. Also, SiGe on channel devices have worse NBTI property.

As a consequence, from the future perspective, it is necessary to make a trade-off and to find the best strategy to improve the performance and, meanwhile, keep reliability. All the results in this thesis will be valuable to provide a design guideline for designing advanced CMOS devices with both good performance and reliability.

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Contents

Chinese Abstract		i
English Abstract		ii
Acknowledgements		iv
Contents		v
Figure Captions		vii
Table Captions		xii
Chapter 1	**Introduction**	1
1.1	The Motivation of This Work	1
1.2	Organization of This Thesis	2
Chapter 2	**Experimental Measurement Setup and Basic Theory**	**4**
2.1	Introduction	4
2.2	Experimental Setup	4
2.3.1	Basic Experimental Setup	5
2.3.2	Basic Theory	6
2.3.3	Principle of the Low Leakage IFCP Method	8
2.3.4	Extraction of the Effective Channel Length	10
Chapter 3	**A New Direct-Current Current-Voltage (DC-IV) Method, boosted DC-IV (βDC-IV)**	**14**
3.1	Introduction	14
3.2	The Experimental Setups of Gated-Diode (GD) and Direct-Current Current-Voltage (DC-IV) Measurements	16
3.3	The Theory of Gated-Diode (GD) Measurements	17
3.4	The Theory of Boosted DC-IV(βDC-IV)	21
3.5	The Methodology of Boosted DC-IV(βDC-IV)	27
3.6	Summary	31
Chapter 4	**New Direct-current Current-Voltage (DC-IV) Profiling Measurement**	**32**
4.1	Introduction	32

4.2 Concept of New Lateral Profiling Technique 34
4.3 Derivations of Relationship Between Lateral Positions and Surface Potentials 38
4.4 Theory of Surface potentials on Gated-Diode Systems 44
4.5 Modulation of Junction Depletion Width with Varying Surface Potentials 49
4.6 Result and Summary 50
Chapter 5 Analysis of Reliability Issues in Strained CMOS Devices 55
5.1 Introduction 55
5.2 Device Preparation 56
5.3 Strained Device Physics 58
5.4 The Analysis of Reliability in Strained nMOSFETs 63
5.5 The Analysis of Reliability in Strained pMOSFETs 79
5.6 The Analysis of NBTI Degradation of Strained pMOSFETs 86
5.7 Summary 87
Chapter 6 Summary and Conclusion 94
References 96

Figure Captions

Fig. 2.1 The experimental setup and environment of the basic I-V measurement. 5

Fig. 2.2 The experimental step of charge pumping method. 7

Fig. 2.3 The schematic of charge pumping (CP) for (a) nMOSFET measurement (b) pMOSFET measurement. Induced leakage current(I_G) occurs when tox< $20A^0$ 9

Fig. 2.4 Demonstration of the result of IFCP Technique. Note that the green circle shows the gate leakage current. 11

Fig. 2.5 Illustration of ΔL_0 extraction from CP data. (a) Parameter definition and extraction method.(b) Interface traps distribution in short and long channel length devices. 12

Fig. 2.6 Calculated (a) $\Delta L_0 \approx 0.03\mu m$ for nMOSFET, (b) $\Delta L_0 \approx 0.05\mu m$ for pMOSFET in this work. 13

Fig. 3.1 The experimental setup of GD measurement. 17

Fig. 3.2 The experimental setup of DC-IV measurement. 17

Fig. 3-3 The schematic diagram of gate voltage modulating the depletion region of drain to bulk diode. 19

Fig. 3-4 (a) The SCR form of the junction with channel accumulation under suitable gate bias. Note the SCR near the surface is bended into the drain region. (b) The SCR form of the junction with channel depleted under suitable gate bias. Note the SCR near the surface is extended to the bulk region. 19

Fig. 3-5 (a) The comparison of the gate, drain, well (bulk) currents under V_D= 0.4V, and V_G= -0.5 to 3.0V, and V_B is ground. Note the well and gate currents are comparable. (b) The comparison of the gate, drain, well currents under V_D= 0.3V, from V_G= -1 to 3.0V, and V_B is ground. Note the well and gate currents are not comparable any more. 23

Fig. 3-6 The twin gated-diode measurement. Note, after subtracting the currents with different but approached bulk voltages, we can find the gated-diode current peaks. 25

Fig. 3-7	A higher V_{DB} is set to boost the current level of forward and recombination current to exceed gate leakage current level so that the latter can be disregarded.	25
Fig. 3-8	The explanation of how to extract the net recombination current from the junction current, including the forward and recombination currents.	27
Fig. 3-9	The comparison of the current levels of drain, well, and gate on junction voltage-V_{DB} equivalent to 0.8V.	29
Fig. 3-10	The experimental result of the DC-IV measurements at V_{DB}= 0.805V (the black curve) and V_{DB}= 0.795V (the red curve), respectively. The red-dot curve is directly shifted to match the black-solid curve.	29
Fig. 3-11	(a) The calculated result of β DC-IV is presented, but this result is not the final DC-IV result. Because the junction is biased to a higher level, DC-IV current is boosted. We have to diminish the boosted DC-IV current to the original level by eq. 3-10. (b) By using eq. 3-10, the boosted DC-IV current is diminished to the original DC-IV current.	30
Fig. 4-1	The comparison of the distributions of the local threshold voltages for LDD and extensive highly doping respectively. Note, in Fig. 4-1 (b), the extensive highly doping on drain or source side makes the local threshold voltages drop rapidly.	33
Fig. 4-2	The main idea of our new DC-IV profiling. Based on HSR theory, there are higher probability of R-G current to happen when the carrier concentrations are the lowest, that is, E_{fs}= E_i The blue curve is E_i, and the green curve is E_{fs}.	36
Fig. 4-3	In (a) the field near the surface is controlled by the gate and junction voltages under a low level gate bias; in (b) the filed is governed mainly by the gate under a high level gate bias. The black curves are the electric field lines.	37
Fig. 4-4	The gated-diode system includes three regions, including the depleted, diffusion, and quasi-neutral regions.	38
Fig. 4-5	The derivation of our lateral profiling in the case of depleted region. The red dot is what we find in terms of the blue and green curves.	39

Fig. 4-6	The derivation of our lateral profiling in the case of diffusion region. The red dot is what we found in terms of the blue and green curves.	40
Fig. 4-7	In the quasi neutral region, the R-G current can not be contributed any more due to the formation of channel.	42
Fig. 4-8	The band diagram for gated-diode systems under equilibrium (without junction voltages), (a) and (b), and non- equilibrium (with junction voltages,) (c) to (e).	45
Fig. 4-9	The surface potentials versus gate voltages under gated-diode system for n and p regions, respectively.	48
Fig. 4-10	The lateral positions versus gate voltages plot in a gated diode system.	52
Fig. 4-11	The interface-traps versus lateral-positions plot taking Fig. 3-12 (b) as an example, based on Eq. (4-22).	53
Fig. 4-12	The three main components of the traps centers exist in the gated-diode system, including the trap-centers in the metallurgical junction, the trap-centers in the depleted region induced by surface fields, and, as well known, the trap-centers on surface. In this figure, the blue triangles stand for the trap-centers in the metallurgical junction, and the green circles stand for the trap-centers in the depleted region induced by surface fields, and the red crosses stand for the trap-centers on surface.	54
Fig. 5-1	(a) Bulk-Si device, (b) SiC on Source/Drain devices (uniaxial-strain), (c) CESL (contact etching stopping layer) capped device (uniaxial-strain), (d) SSDOI (strained silicon directly on insulator) device (biaxial-strain), and (e) strained-Si/SiGe on substrate device (biaxial-strained). All nMOSFETs are <100> channel on (100) substrate.	57
Fig. 5-2	(a) Bulk-Si device, (b) SiGe on source/drain devices (uniaxial strain), and (c) SiGe on substrate device. All pMOSFETs are <110> channel on (100) substrate.	58
Fig. 5.3	(a) Ellipsoids of constant electron energy in reciprocal ("k") space. (b) Energy splitting between the Δ_2 (2-fold degenerate)	61

	and Δ4 (4-fold degenerate) conduction bands for strained-Si device and bulk Si device.	
Fig 5.4	Hole constant energy surfaces obtained from six band kp calculations for common types of stresses: (a) unstressed and (b) compression stress on (100) wafer.	62
Fig. 5.5	Simplified schematic of valence-band splitting of strained-Si in the inversion region.	62
Fig. 5-6	The I_{on}-I_{off} characteristics of all the strained splits and control nMOSFETs.	65
Fig. 5-7	The I_B-V_{GS} curves and impact ionization rates of all the strained splits and control nMOSFETs.	66
Fig. 5-8	The I_D degradation behaviors of uniaxial strained nMOSFETs after (a) FN and (b) HC stresses.	67
Fig. 5-9	The I_D degradation behaviors of biaxial strained nMOSFETs after (a) FN and (b) HC stresses.	68
Fig. 5-10	The charge pumping current curves of strained splits and control nMOSFETs after hot carrier stress.	69
Fig. 5-11	The charge pumping current curves of strained splits and control nMOSFETs after hot carrier stress.	70
Fig. 5-12	The I_D degradation behaviors of SiC, SiC with pocket, and control nMOSFETs after I_{off}-state stress.	74
Fig. 5-13	The experimental results of β DC-IV measurement for strained nMOSFETs after FN stress.	75
Fig. 5-14	The calculated results of the interface-traps lateral-profiling.	76
Fig. 5-15	The experimental results of β DC-IV measurement for strained nMOSFETs after HC stress.	77
Fig. 5-16	The calculated results of the interface-traps lateral-profiling.	78
Fig. 5-17	The I_{on}-I_{off} characteristics of all the strained splits and control nMOSFETs.	81
Fig. 5-18	The I_B-V_{GS} curves and impact ionization rates of all the strained splits and control pMOSFETs.	82
Fig. 5-19	The I_D degradation for those pMOSFETs after HC stress.	83

Fig. 5-20 The charge pumping currents of strained splits and control pMOSFETs after HC stress. 84

Fig. 5-21 The charge pumping currents of strained splits and control pMOSFETs after FN stress. 85

Fig 5-22 The schematic diagram of the electrochemical reaction model. 89

Fig 5-23 The experimental results of β DC-IV measurement for strained nMOSFETs after FN-like NBTI stress. 90

Fig. 5-24 The calculated results of the interface-traps lateral-profiling. 91

Fig 5-25 The experimental results of β DC-IV measurement for strained nMOSFETs after HC-like NBTI stress. 92

Fig. 5-26 The calculated results of the interface-traps lateral-profiling. 93

Tables Captions

Table 1-1	The comparison of strained CMOS family.	3
Table 3-1	The comparison of the three main kinds of the interface states quality evaluation.	15
Table 3-2	The comparison of DC-IV and GD measurements.	21
List 4-1	The derivations of the relationship between surface potentials and positions.	43
Table 5-1	The summary of the degradation of all strained splits and control nMOSFETs after FN and HC stresses in terms of charge pumping current and $I_{D,\ on}$.	71
Table 5-2	The comparison of the values of I_D degradation and charge pumping current increment for strained pMOSFETs and the control sample after HC stress.	80
Table 6-1	The summary of strained CMOS devices in terms of performance and reliability in this thesis.	95

Chapter 1
Introduction

1.1 The Motivation of This Work

How to enhance the drain current for MOSFETs? In the recent years, various approaches have been employed to achieve this goal, such as to reduce the channel length and to increase the gate oxide capacitance by reducing the gate oxide thickness or using high-k. In advanced CMOS devices, strained silicon technology plays an important role of improving the device performance. In ITRS report 2007[1], it is pointed out that strained-Si technology has to enhance the driving current of CMOS devices to 180% ultimately. It encourages many more strain-engineering approaches. In Table 1-1, there are several strain schemes listed [2-10]. In this table, we categorize strain schemes into global, local, and hybrid strains. Global strain is almost a biaxial strain made by epi-growth strained layer on substrate. But significant dislocation issues are encountered due to a large area strain. Also, it is high cost. On the other hand, the local strain is usually unaxial strain and is induced by the process. There are many stressors to implement local strain, such as SiGe eS/D, SiC eS/D, and capping layer. Different from global strain, dislocation issues are less for local strain. Finally, it is low cost due to small area strain comparing to global strain. The last scheme is hybrid strain. Hybrid strain means that one combines the benefits of global and local strains to construct an idea case. But it faces the big challenge of manufacturing.

As nano-scale CMOS technology moves into 45 nm and beyond, leakage current issues have been more significant than ever. As a consequence, novel device structures and materials have been widely pursued, such as FinFETs [11]–[12], vertical MOSFETs [13]-[14], and high-*k* gate dielectric [15].

Although there are a lot of exciting strain schemes introduced, even improving driving current near 80%[9], the reliability issues of strained silicon CMOS devices are rarely reported. In [16,17], they reported the importance of reliability for strained devices and the hybrid substrate technology, and it was emphasized that a *large enhancement of mobility will adversely degrade the device reliability.* In [18], it was first reported that, for nMOSFETs, tensile cap stressor device is much better in terms of reliability and performance. Besides, for pMOSFETs, SiGe on S/D devices with EDB[6] is most promising in terms of performance and reliability.

For the first time, in this work, we will accurately calculate the interface states on the channel lateral direction by ***our new modified DCIV, boosted DCIV (β-DCIV)*** with high resolution, which provides useful information of degradation mechanism of stressed devices for strained silicon devices. In order to effectively investigate the strained CMOS devices and to establish a good device design methodology, it is necessary to clarify the reliability issues of strained devices. For this reason, we perform the low leakage charge pumping (CP) [19]-[20] to analyze the reliability of the measured devices, in which the hot carrier and NBTI reliabilities of the strained silicon devices are important.

1.2 Organization of This Thesis

This thesis is divided into six chapters. Chapter 1 is the introduction. Chapter 2 describes the experiment setups and the analysis methods used in this study. In Chapter 3, we will introduce our new novel modified DC-IV method: ***boosted DC-IV (β-DCIV)***, to characterize the interface states of strained silicon devices. In order to develop the relationship between interface states and positions on the channel direction, for the first time, a new profiling technique based on β-DCIV by direct

measurement will be demonstrated in Chapter 4. In Chapter 5, we will introduce the uniaxially-strained and biaxially-strained nMOSFETs and pMOSFETs technologies. Then, we will discuss interface state analysis and its correlation to the hot carrier reliabilities of these CMOS devices with various strained devices. Moreover, we will study the temperature dependence reliability from the influence of uniaxially and biaxially-strained pMOSFETs. Finally, a summary and conclusion will be given in Chapter 6.

	nMOSFET				pMOSFET				Hybride
Strain Direction	**Local**		**Global**		**Local**			**Global**	
Strain Approach	CESL	SiC on S/D FinFET	Relaxed SiGe sub	SSOI	SiGe on S/D +EDB	CESL	Diamond -like carbon cap	SiGe-channel + cap	T-CESL for nFET C-CESL for pFET
ΔI_{on}(%)	+12	+30	+13	+18	+25	+14	+69	+80	nFET→60% pFET→55%
Lg(nm)	37	25	60	25	45	60	70		40
EOT(A^0)	18.8	20	22	17.5 (TiN/HfO_2)		14			
Ref.	[2]	[3]	[4]	[5]	[6]	[7]	[8]	[9]	[10]

Table 1-1 The comparison of Properties of strained CMOS family.

Chapter 2
Experimental Measurement Setup and Basic Theory

2.1 Introduction

In order to achieve high performance of advanced CMOS devices, strained silicon technology has been one of the mainstreams to extend the CMOS device scalability for several generations. To investigate the relationship between performance and reliability properties of strained CMOS devices, we perform several skills of experimental measurements performed in this thesis. In this chapter, the measurement setup and basic theory of the measurement methods will be introduced.

This chapter is divided into several sections. First, we will illustrate the fundamental experimental setup to characterize strained CMOS devices. Second, the charge pumping method used in this thesis will be introduced, and its experimental setup, fundamental theory, and improved method will be described.

2.2 Experimental Setup

The experimental setup for the direct current I-V measurement of semiconductor devices is illustrated in Fig. 2.1.

Based on the PC programmable instrument environment, the complicated and long-term characterization procedures for analyzing the intrinsic and degradation behavior in MOSFETs can be achieved. As shown in Figure 2.1, the characterization equipment, including semiconductor parameter analyzer (HP4156C),

dual channel pulse generator (HP8110A), low leakage switch mainframe (HP E5250A), cascade guarded thermal probe station and thermal controller, provides an adequate capability for measuring the device I-V characteristics. Besides, the PC program used to control all the measurement process is HT-basic.

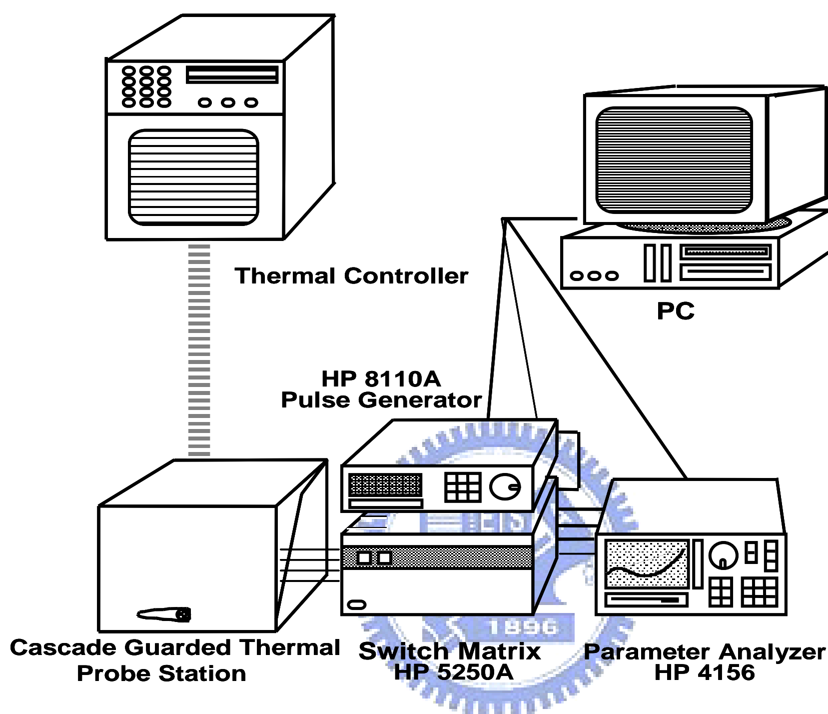


Fig. 2.1 The experimental setup and environment of the basic I-V measurement.

2.3 Charge Pumping Measurement

2.3.1 Basic Experimental Setup

The experimental setup of the charge pumping measurement is shown in Fig. 2.2. The source, drain, and bulk electrodes of tested devices are grounded. A 1MHz square pulse waveform provided by HP8110A with fixed base level (V_{gl}) is applied to the NMOS gate or with fixed top level (FTL) to the PMOS gate. We keep V_{gl} at –1.0V

while increasing FTL from –1.0V to 1.0V by steps for NMOS devices or keep FTL at 1.0V while decreasing V_{gl} from 1.0V to –1.0V by steps for PMOS devices. The frequency of charge pumping can be modulated for different devices, and basically the larger the frequency is, the larger the vale of the charge pumping current is. Meanwhile the parameter analyzer HP4156C is used to measure the charge pumping recombination-generation current (I_{CP}).

2.3.2 Basic Theory

The charging pumping principle for MOSFETs has been applied to characterize the fast and deep interface traps at the oxide interface. The original charge pumping concept was found by Brugler and Jespers, and the technique was developed by Heremans [21]. This technique is based on a recombination-generation process at the Si/SiO_2 interface involving the surface traps and fixed oxide traps. It consists of applying a constant reverse bias at the source and drain while sweeping the base level of the gate pulse train from a low accumulation level to a high inversion level. Meanwhile the frequency and the rising/falling time are kept constant. When the base level is lower than the flat-band voltage, and the top level of the pulse is higher than the threshold voltage, the maximum charge pumping current occurs.

This means that a net amount of charge is transferred from the source and drain to the substrate each time while the device is pulsed from inversion toward accumulation. Moreover, the charge pumping current is caused by the repetitive recombination-generation at interface traps. As a result, the recombination current measured from the bulk (substrate) is the so-called charge pumping current [22]. The CP current can be given by:

$$I_{CP} = q \cdot f \cdot W \cdot L \cdot N_{IT}. \quad (2.1)$$

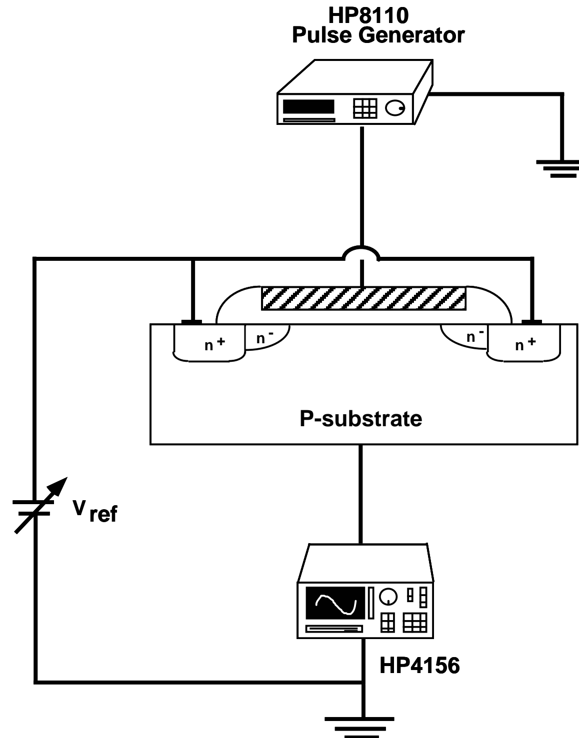


Fig. 2.2 The experimental step of charge pumping method.

Based on this equation, the charge pumping current is proportional to the interface trap density under the oxide layer, the frequency, and the area of the tested devices. However, when the top level of the pulse is lower than the flat-band voltage, or the base level is higher than the local threshold voltage, the interface traps are permanently filled with holes in accumulation state or electrons in inversion state in n-MOSFET, which no holes reach the surface. As a result, there is no recombination current, and hence, the charge pumping current cannot be found.

Charge pumping measurements can be performed by several different ways. For our experimental requirement, we perform the charge pumping measurement by applying a gate pulse with the fixed base voltage (V_{gl}) and increasing the pulse amplitude. While the channel operates between accumulation and inversion of channel carriers with the fixed base voltage lower than flat-band voltage and high

voltage above the threshold voltage, respectively. This gives rise to the charge pumping current (I_{CP}) from the bulk and reaches saturation situation. If we use another method which changes base voltage while with a fixed pulse amplitude, the current saturation region is not extensive enough for research because of the limitation that the saturation current occurs only when the gate pulse changes carriers from a low accumulation level to a high inversion level.

2.3.3 Principle of the Low Leakage IFCP Method

Figures 2.3 (a) and (b) show the schematic of a low leakage IFCP measurement for CMOS developed by our group in [23]. With both S/D grounded and by applying a gate pulse with a fixed base level (V_{gl}) and a varying high-level voltage (Fig) for NMOS, the channel carriers will be switched between the accumulation and inversion state. This gives rise to the charge pumping current I_{CP} (= I_B) measured from the bulk. From Fig. 2.3, when t_{ox} >30Å, the leakage current I_G in I_{CP} is not obvious. However, when t_{ox} is small down beyond 20Å, the leakage current I_G is significent. The unexpected leakage current will influence charge pumping current. In order to diminish this effect, our group suggest a bright way. Its details will be described in the following. In the first place, the I_{CP}s are measured at two different frequencies, f_1 and f_2. They can be expressed as

$$I_{CP,\ f1\ \text{with-leakage}} = I_{CP,\ f1\ \text{correct}} + I_{CP,\ \underline{\text{leakage}@f1}} \qquad (2.1)$$

and

$$I_{CP,\ f2\ \text{with-leakage}} = I_{CP,\ f2\ \text{correct}} + I_{CP,\ \underline{\text{leakage}@f2}}. \qquad (2.2)$$

When the frequency is sufficiently high, the leakage components in these two frequencies are almost the same ($I_{CP,\ leakage@f1} \approx I_{CP,\ leakage@f2}$). We then take the difference of I_{CP} ($\Delta I_{CP,\ f1-f2}$) between two frequencies. From equations (2.1) and (2.2), the difference of these two CP curves gives

$$\Delta I_{CP,\ f1-f2} = I_{CP,\ f1\ with\text{-}leakage} - I_{CP,\ f2\ with\text{-}leakage}. \tag{2.3}$$

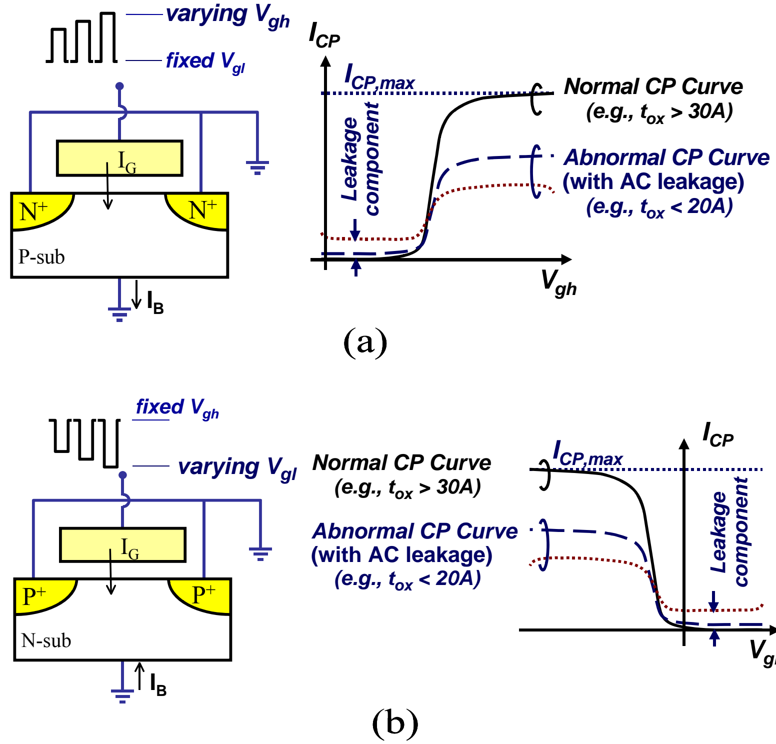


Fig. 2.3 The schematic of charge pumping (CP) for (a) nMOSFET measurement (b) pMOSFET measurement. Induced leakage current(IG) occurs when tox< 20A

Since the correct CP curve is directly proportional to the frequency, it will be equal to the difference of two CP curves. Therefore, in IFCP method, the correct CP curve at frequency ($f1$- $f2$) can be given by

$$I_{CP,\ f1-f2} = \Delta I_{CP,\ f1-f2}. \tag{2.4}$$

For example $I_{CP(2MHz)} - I_{CP(1MHz)}$ is regarded as the I_{CP} at their difference frequency, 1MHz. The result of the charge pumping measurement for the strain-Si device is shown in Fig. 2.4, curve (1) and curves (2). From this figure, we can find a

huge gate leakage current appears in the charge pumping cure when the voltage of gate pulse is higher than 1V. Because the correct charge pumping current is directly proportional to the frequency of gate pulse and the leakage of current is irrelevant to the frequency, we can receive the correct charge pumping current by taking the difference of the measured I_{CP} between two frequencies theoretically. To see the result, we finally get a correct curve with commonly known saturation charge pumping current, curve (3), in Fig. 2.4.

2.3.4 Extraction of the Effective Channel Length

Figure 2.5 shows the non-uniform interface trap distribution for the extraction of effective channel length. Using two different channel lengths, the interface traps can be represented by

$$N_{it,\,1,\,total} = N_{it,\,11}(edge) + N_{it,\,12}(center) \tag{2.5}$$

and

$$N_{it,\,2,\,total} = N_{it,\,21}(edge) + N_{it,\,22}(center). \tag{2.6}$$

Since the mechanical stress in the edge region of channel is more critical than the center region of channel, the interface traps in the edge is larger than that in the center region, and therefore, the mechanical stress in two different channel devices are almost the same, i.e., $N_{it,\,11}$ is approximately equal to $N_{it,\,21}$. To eliminate the traps generated at the edge region, the difference of these two interface traps can be used, which is directly proportional to the ΔL. Hence, we have

$$\Delta I_{CP,\,max} \propto \Delta N_{it,\,total} = N_{it,\,1,\,total} - N_{it,\,2,\,total} = N_{it,\,12} - N_{it,\,22} \propto \Delta L. \tag{2.7}$$

Figure 2.5 (a) shows the definitions of ΔL_1, ΔL_2, and ΔL_0, which can be expressed as

$$\Delta L_1 = L_{MASK} - L_{gate},$$

$$\Delta L_2 = L_{gate} - L_{eff},$$

and

$$\Delta L_0 = L_{MASK} - L_{eff} = \Delta L_1 + \Delta L_2. \quad (2.8)$$

Figures 2.6 (a) and (b) show the calculated interface traps, N_{it}, per unit width and offset length, $\Delta L_0 = L_{MASK} - L_{eff}$, from the measured 20 devices with nMOSFET and pMOSFET in this work.

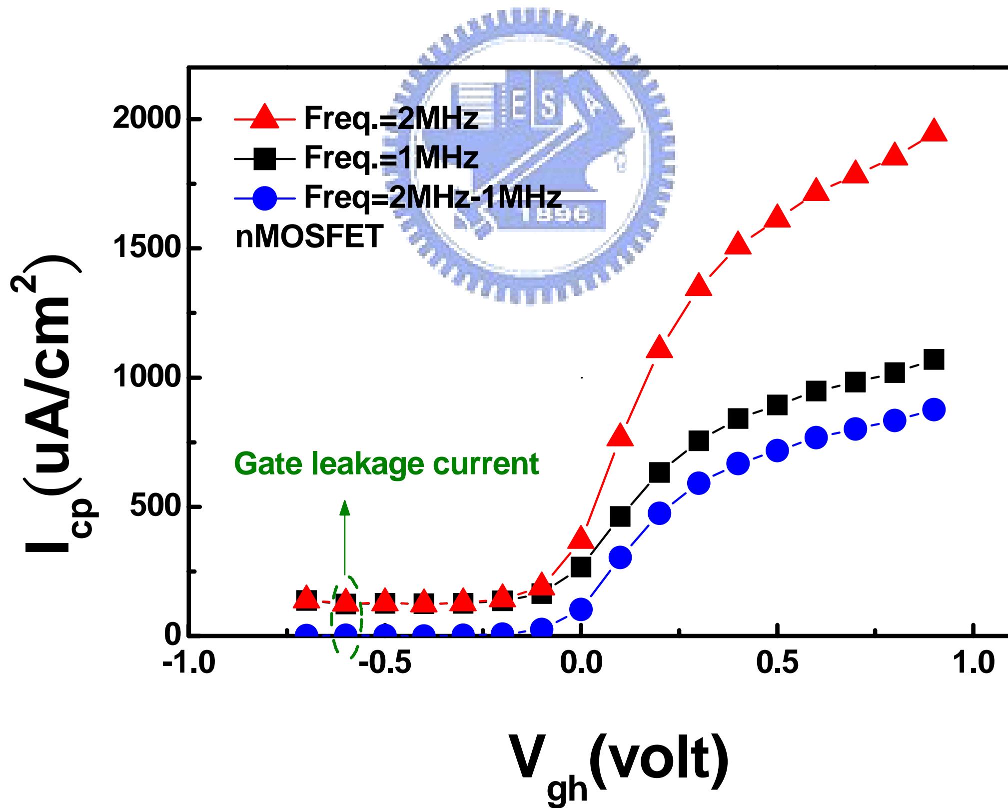
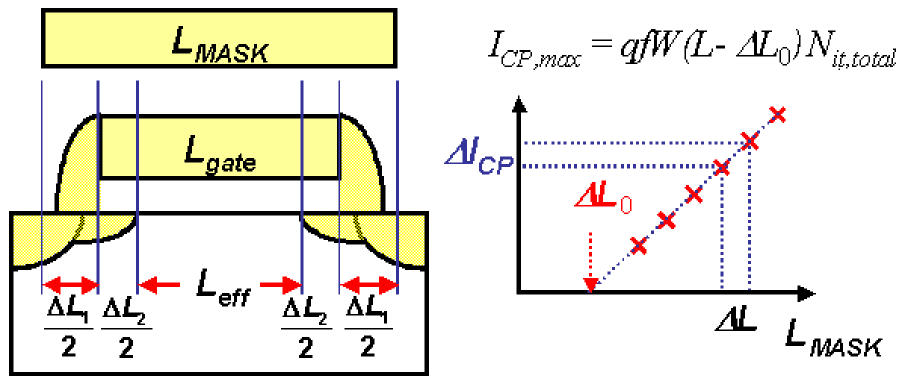
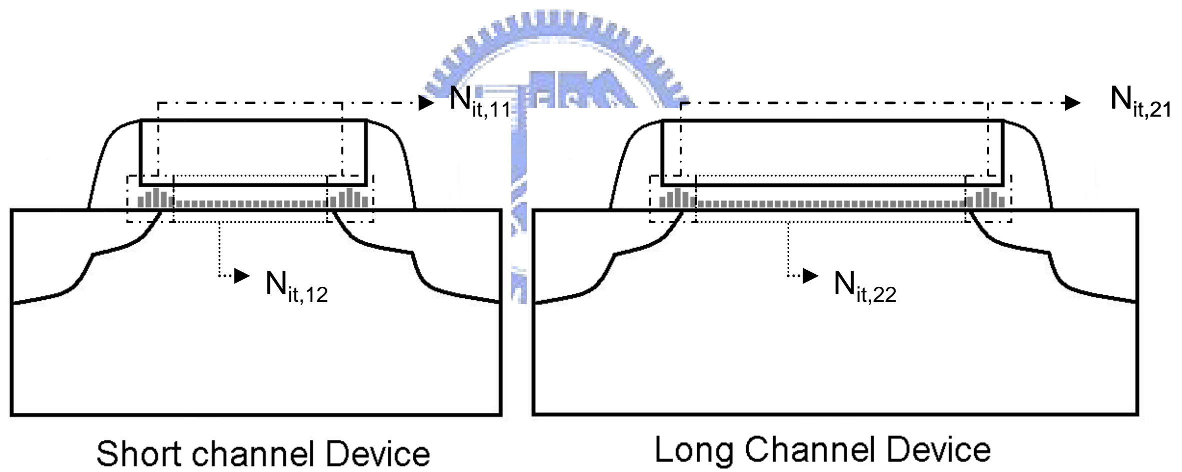


Fig. 2.4 Demonstration the result of IFCP Technique. Note that the green circle shows the gate leakage current.

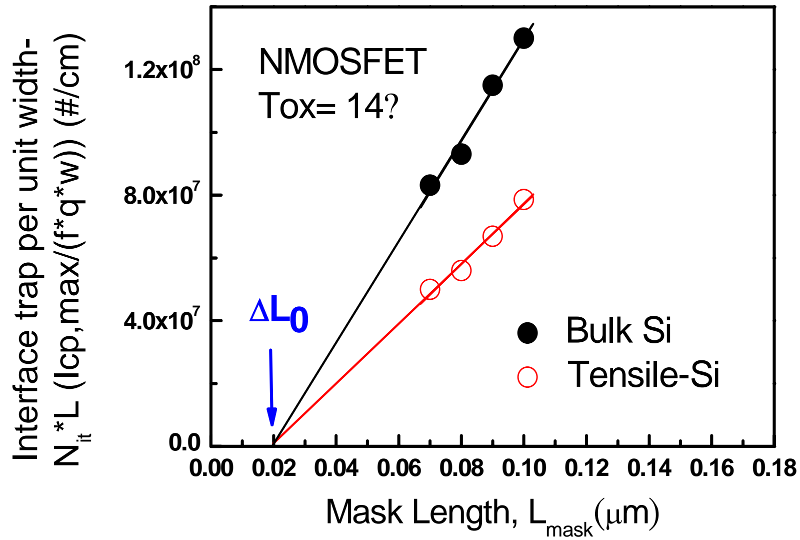


(a)

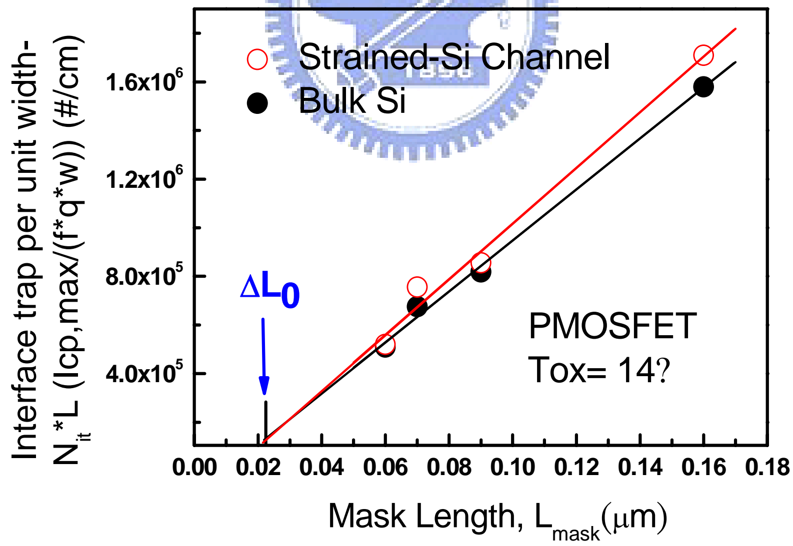


(b)

Fig. 2.5 Illustration of ΔL_0 extraction from CP data.
(a) Parameter definition and extraction method.
(b) Interface traps distribution is short and long channel length devices.



(a)



(b)

Fig. 2.6 Calculated (a) $\Delta L_0 \approx 0.03\mu m$ for nMOSFET, (b) $\Delta L_0 \approx 0.05\mu m$ for pMOSFET in this work.

Chapter 3

A New Direct-Current Current-Voltage (DC-IV) Method-Boosted DC-IV (β DC-IV)

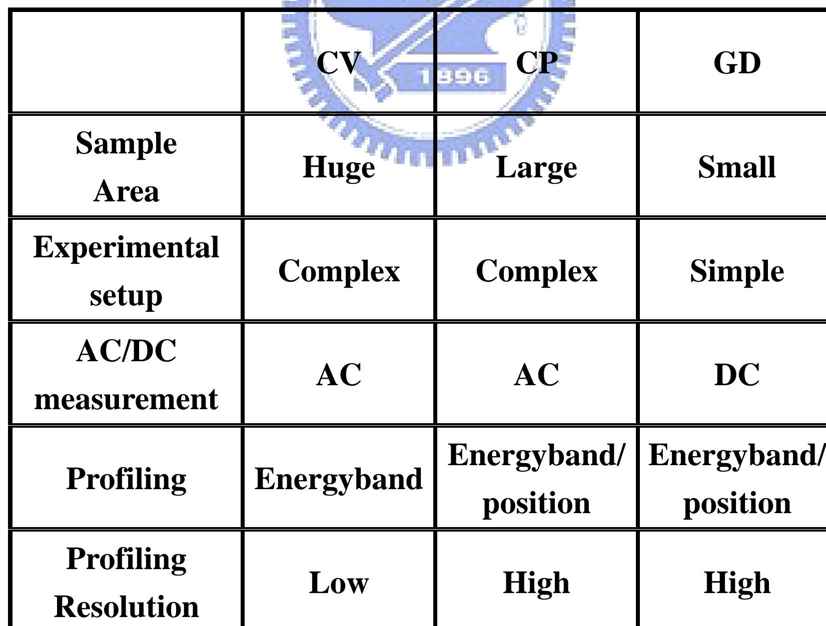
3.1 Introduction

The interface states play important rules in the performance and reliability of all oxide-semiconductor-system devices, especially SiO_2-Si-system devices. There are three main approaches to characterize the interface quality, including capacitance-voltage (C-V) measurement, Charge-Pumping (CP) measurement, and Gate-controlled Diode (GD) measurement, as shown in Table 3-1. For the comparison of these three approaches, the limitation of CV measurement for the interface-states characterization is the huge sample area because the gate capacitance is proportioned to the sample area, and it is suitable for MOS-CAP study only. The sample area limitation for CP measurement is not as strict as that for CV measurement. However, the interface states are proportional to the sample area so it is appreciated for CP measurement to be employed in larger area samples. For GD measurement, the sample area does not play an important role, and thus it is allowed for GD measurement to be implemented in small area samples. Moreover, CV and CP measurements involve AC measurement environments, and the experimental setups of these two measurements are more complex than that of GD measurement since the measurement environment of GD is only DC measurement environments. Besides, the profiling methods for CV and GD measurements were only reported in terms of energy-band, but that for CP was reported in terms of not only energy-band but also positions. In this work, ***for the first time***, we first reported the profiling method for GD measurement in terms of lateral positions.

Owing to a simple experimental setup and small sample-area of GD measurement, GD measurement is more important in interface states evaluation in

nano CMOS technology.

The Gated-Diode properties were observed by C. T. Sah, for the first time in 1962, when he studied on the effect of surface recombination on P-N junction [24], and two peaks of Gated-Diode current were found. In his astonishing efforts on this work then, Sah placed importance on the relationship of surface effect and Bipolar transistor. In 1966, A. S. Grove made a total understanding on the surface effects on p-n junctions [25]. This work first related the surface effects of p-n junction to the MOS-cap surface effect. The latter was first introduced by C. G. B. Garrett and W. H. Brattain[26]. Gated-diode measurement has been successfully applied on the evaluation of surface of pn junction [25]. Recently Gated-diode technique has been widely used to characterize the hot-carrier degradation in MOSFETs [27].



	CV	**CP**	**GD**
Sample Area	**Huge**	**Large**	**Small**
Experimental setup	**Complex**	**Complex**	**Simple**
AC/DC measurement	**AC**	**AC**	**DC**
Profiling	**Energyband**	**Energyband/ position**	**Energyband/ position**
Profiling Resolution	**Low**	**High**	**High**

Table 3-1 The comparison of the three main kinds of the interface states quality evaluation.

Direct-Current Current-Voltage (DC-IV) was first introduced by Neugroschel and Sah.[28] DC-IV is as similar to Gated-diode measurement. It can also be used to

monitor the oxide and interface traps on gate-controlled surface. Different from the gate-controlled surface-effect of pn junction, the concept of DC-IV is based on gate-controlled surface-effect of BJT.

In this chapter, we will introduce the experimental setups of GD and DC-IV measurements and describe the main mechanism of these two measurements. Furthermore, we will make the comparison of these two measurements. At the end of this chapter, we will demonstrate a new modified approach of DC-IV measurement. This new method can avoid the leakage current from gate and extracts pure DC-IV current results.

3.2 The Experimental Setups of Gated-Diode (GD) and Direct-Current Current-Voltage (DC-IV) Measurements

The experimental setup of GD measurement is shown in Fig. 3-1. GD only needs three terminals, including drain (or source,) gate, and well. The operating conditions of GD measurement are almost the same as those of DC-IV. The only difference from DC-IV measurement is that the GD current is measured at the drain terminal with gate sweeping, while the DC-IV current is at the well terminal.

The experimental setup of DC-IV measurement is shown in Fig. 3-2. DC-IV needs four terminals, including drain (or source,) gate, well, and substrate. The drain terminal is biased at voltage forwardly but less than turn-on voltage, and the well and substrate terminals are grounded. When the gate-voltage sweeps and makes the channel from inversion to accumulation, the DC-IV current is measured from the well terminal.

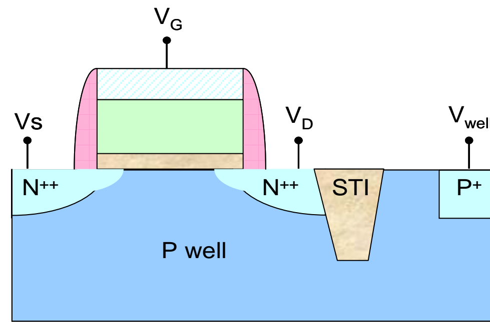


Fig. 3-1 The experimental setup of GD measurement.

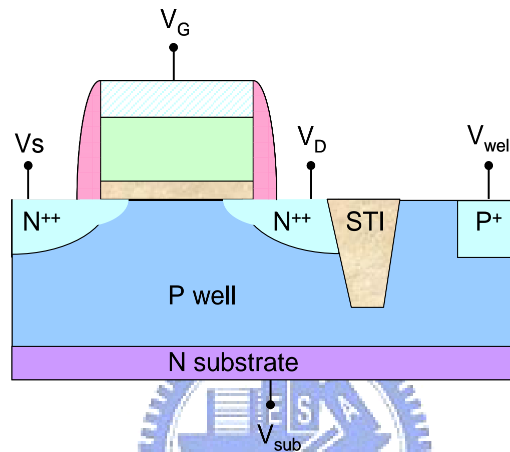


Fig. 3-2 The experimental setup of DC-IV measurement.

3.3 The Theory of Gated-Diode (GD) Measurements

The theory of Gated-Diode measurement is based on the SRH recombination and generation process of p-n Junction, but the gate terminal is added to control the form and position of the surface depletion region of p-n junction. Fig. 3-3 shows the schematic diagram of this concept. When drain-to-bulk (p-n) junction is formed, the space charge region (SCR) is set. With a junction bias (a reverse or forward bias), the recombination current contributed by the defects in SCR will flow. We can monitor the SCR quality of the junction by the amount of the recombination current. The higher the recombination current is, the worse the junction quality becomes. If we assume that a board and uniform energy distribution of the defects around the intrinsic

level $-\Phi_i$, and the defect capture cross section for electrons is the same as that for holes (i.e., $\sigma_n = \sigma_p = \sigma$), the distribution of defects will be set as a Gaussian distribution from Φ_h to Φ_e, and the maximal value will exist at Φ_i. Thus, we can simply assume the main place where the recombination-generation process happens in the maximal probability is at the intrinsic level, which is the narrow region- $\triangle$X in Fig. 3-3.

As the gate bias is applied on the surface of the junction, the position of SCR near this surface will be modulated by the gate bias. When the channel under the Si/SiO_2 is accumulated with a suitable gate bias, the SCR of p-n junction near the surface will be bended into the drain region due to the distribution of the electric field from gate to drain, as shown in Fig. 3-4(a). Thus, we can monitor the recombination current caused by defects in SCR of the drain side. When the channel under the Si/SiO_2 is depleted with a suitable gate bias, the SCR of p-n junction near the surface will be extended to the bulk region, as shown in Fig. 3-4(b), and then we can monitor the recombination current conduced by the defects around the intrinsic level in SCR of the channel region. If the gate bias is further increased so that the channel is inversed, SCR under the interface of Si/SiO2 will be drowned by the minority carriers in bulk, and the recombination and generation process beneath surface will stop. Therefore, the recombination current can not be observed. As a result, we can control where the recombination-generation process happens through the modulation of the form and position of SCR with the sweep of the gate bias.

The excess recombination current can be expressed as, [29]

$$I_{R-G} = \frac{1}{2} q W \triangle s(x) \triangle x(V_G) n_i \exp\left(\frac{qV_{pn}}{2kT}\right) \qquad (3\text{-}1)$$

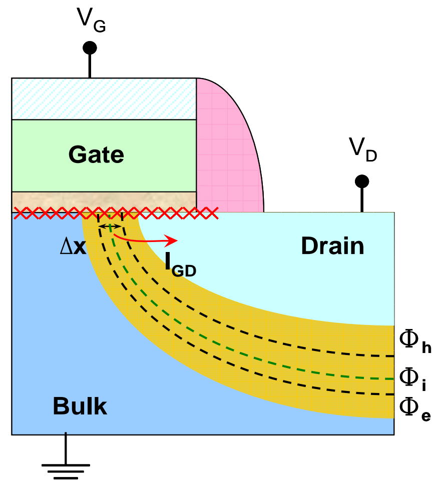


Fig. 3-3 The schematic diagram of gate voltage modulating the depletion region of drain to bulk diode.

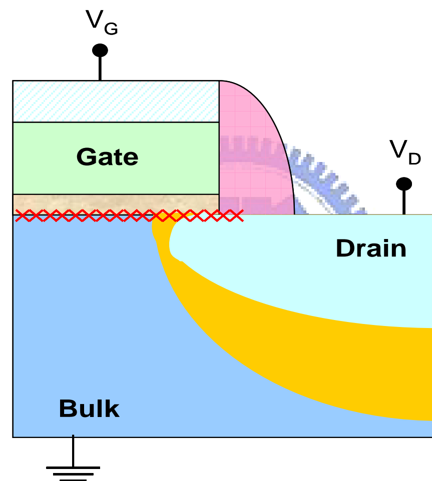


Fig 3-4(a) The SCR form of the junction with channel accumulation under suitable gate bias. Note the SCR near the surface is bended into the drain region.

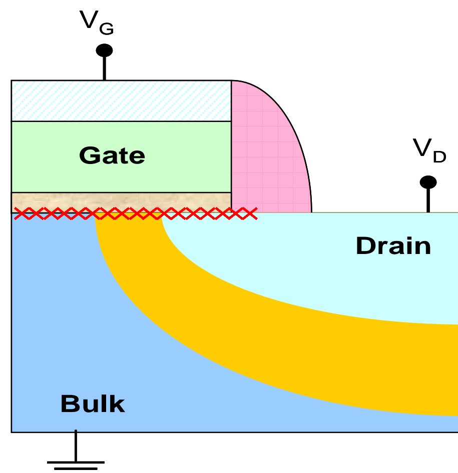
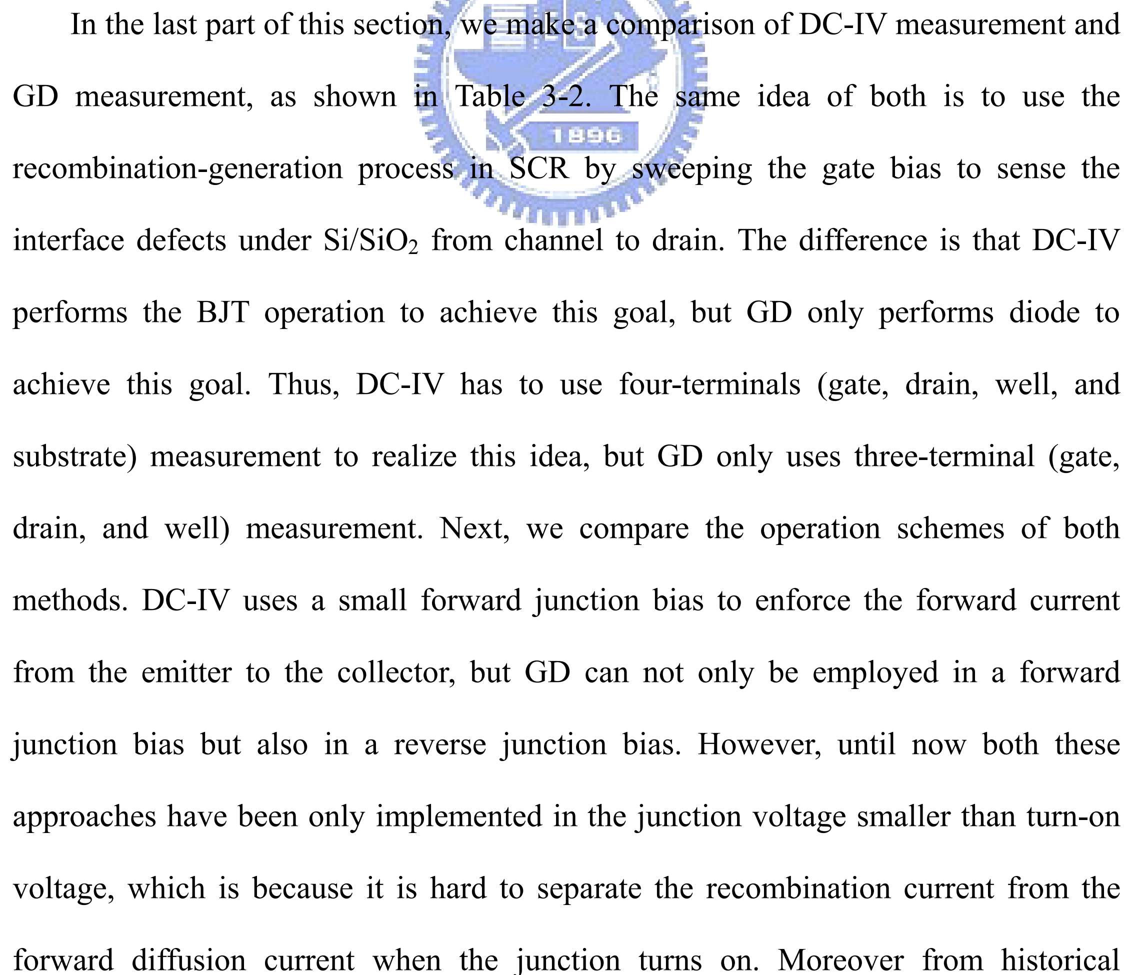


Fig 3-4(b) The SCR form of the junction with channel depleted under suitable gate bias. Note the SCR near the surface is extended to the bulk region.

where W is the device channel width, and q is the unit charge, and $\triangle s(x)$ is the surface recombination rate, and x is the position where the electron and hole concentrations are equal, and n_i represents the intrinsic concentration of the material. Note $\triangle s(x)$ is proportional to the interface N_{it} around mid-gap which acts as the recombination centers, e.g.,

$$\triangle s(x) = \sigma v_{th} \triangle N_{it}(x) \tag{3-2}$$

where v_{th} is the thermal velocity. The values of σ and v_{th} used here are 1×10^{-15} cm^2 and 1×10^{-17} cm/sec, respectively. From equations (3-1) and (3-2), we can relate the N_{it} to the gated-diode recombination current in terms of where recombination and generation process occurs. By comparing the gated-diode current after stress with that before stress, we can understand the stress degradation mechanism of the interface for the tested device.

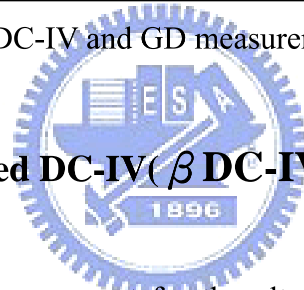


In the last part of this section, we make a comparison of DC-IV measurement and GD measurement, as shown in Table 3-2. The same idea of both is to use the recombination-generation process in SCR by sweeping the gate bias to sense the interface defects under Si/SiO_2 from channel to drain. The difference is that DC-IV performs the BJT operation to achieve this goal, but GD only performs diode to achieve this goal. Thus, DC-IV has to use four-terminals (gate, drain, well, and substrate) measurement to realize this idea, but GD only uses three-terminal (gate, drain, and well) measurement. Next, we compare the operation schemes of both methods. DC-IV uses a small forward junction bias to enforce the forward current from the emitter to the collector, but GD can not only be employed in a forward junction bias but also in a reverse junction bias. However, until now both these approaches have been only implemented in the junction voltage smaller than turn-on voltage, which is because it is hard to separate the recombination current from the forward diffusion current when the junction turns on. Moreover from historical

reasons, the recombination current of DC-IV is measured from the well terminal, but that of GD is measured from the drain terminal. In fact, it is okay once can measure the DC-IV or GD either from the well terminal or the drain terminal.

	GD	DC-IV
Physic Mechanism	SRH Theory	
Device Model	Gate-controlled -surface **Diode**	Gate-controlled-surface **BJT**
Operation Scheme	**3** terminals-G,D,W. **Sense from D**	**4** terminals-G,D,W,S. **Sense from W**

Table 3-2 The comparison of DC-IV and GD measurements.



3.4 The Theory of Boosted DC-IV(β DC-IV)

The challenge of GD measurement for the ultra-thin gate oxide devices is the gate-leakage during the measurement. When the thickness of the gate oxide is thinner than $20A^0$, the current level of gate leakage current is comparable to or even higher than the gated-diode current. Many researches have put much effort on how to suppress the gate leakage current so that the gated-diode current can be observed. In 2002, Chung and Lo developed a smart technique, “Low leakage Gated-Diode, [20]” which has been applied in the gate oxide reliability study whose gate thickness of the tested devices is thinner than $20A^0$. Furthermore, in 2005, Chung and Lee[30] also reported another bright measurement, “Twin Gated-Diode,” which has been implemented in the gate-oxide reliability study whose gate thickness of the tested device is thinner than $16A^0$. In this section another measurement technique is

introduced in the first time, and we will demonstrate that this new DC-IV measurement works in the gate-oxide reliability study whose gate thickness is thinner than $12A^0$.

First, we make a comparison of the current levels of gate, well, and drain for different gate oxide thicknesses, $20A^0$ and $13A^0$ under gated-diode operation, as shown in Fig. 3-5(a) and Fig. 3-5(b), respectively. Fig. 3-5(a) shows that the current levels of I_{well} and I_G are comparable when the junction is biased by a *higher* voltage but smaller than turn-on voltage. Thus, according to "Low Leakage Gated Diode," we can subtract them, and then the net gated-diode current can be extracted, that is,

$$I_{L^2_GD} = I_{well} - I_{gate} \tag{3-3}$$

But, on the other hand, from Fig. 3-5(b), we observe that the current levels of I_{well} and I_G are not comparable any more, and I_G is even much higher than I_{well}. Hence, in this case, equation (3-3) can not be used anymore, and something different has to be figured out to solve this problem.

A brilliant solution, suggested by Chung and Lee, "Twin Gated-Diode[30]," is able to suppress the gate-leakage, and the gated-diode current peaks can be observed, as shown in Fig. 3-6. After subtracting the currents with different but approached bulk voltages, we can find the gated-diode current peaks, e.g.,

$$I_{tw-GD} = I_{well@V_{B1}} - I_{well@V_{B2}}, \quad V_{B1} \text{ and } V_{B2} \text{ are approached} \tag{3-4}$$

This method can suppress some part of gate-leakage current but not all. Moreover, it is hard to choose two suitable closed bulk voltages.

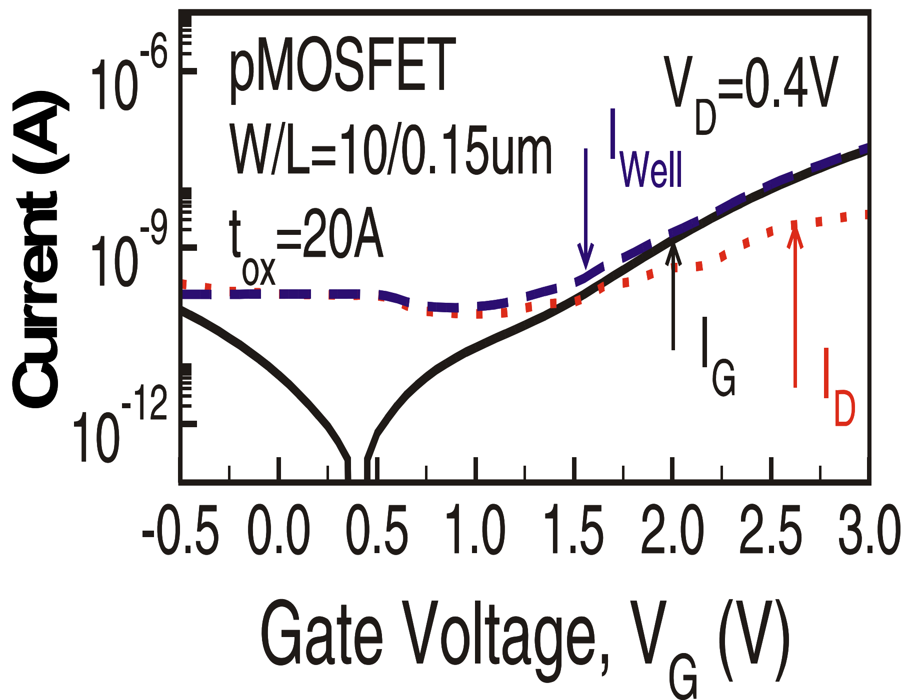


Fig. 3-5(a) The comparison of the gate, drain, well (bulk) currents under V_D= 0.4V, and V_G= -0.5 to 3.0V, and V_B is ground. Note the well and gate currents are comparable.

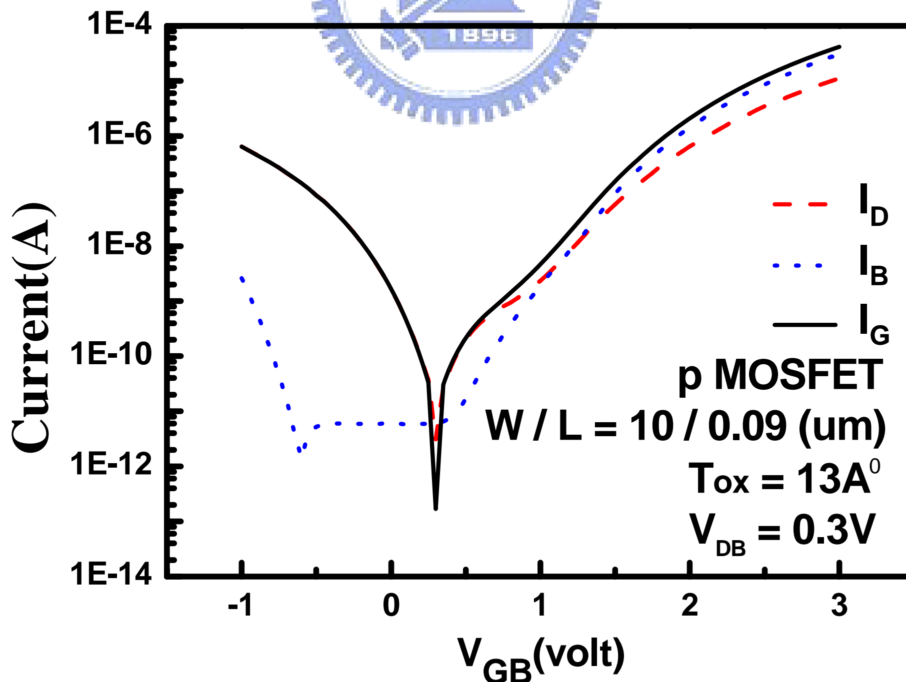
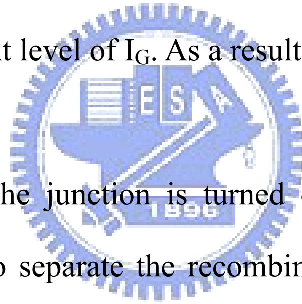


Fig. 3-5(b) The comparison of the gate, drain, well currents under V_D= 0.3V, from V_G= -1 to 3.0V, and V_B is ground. Note the well and gate currents are not comparable any more.

Based on these two modified methods, we may conclude that: (1) the junction voltage is set at a higher level to make the measured GD current level boosted. (2) By biasing two approached junction voltages on the tested device, two measured GD currents are subtracted, and then the calculated current subtracted from these two measured current will exclude the gate-leakage. In short, the keys to suppress the gate-leakage are *to boost* and *to subtract* the measured current. Therefore, based on this idea, we figure out a new method, called *boosted DC-IV(βDC-IV).*

Consequently, we can boost the current level to a higher level by setting a higher junction voltage, as shown in Fig. 3-7. Fig. 3-7 shows that, when the junction voltage is higher than the turn-on voltage, the junction current level will be boosted to a very high level to exceed the current level of I_G. As a result, I_G can be neglected.



But, at the same time, the junction is turned on, and the forward current is contributed. Thus, we have to separate the recombination current (GD current) and forward current from the junction current, which can be expressed as,

$$J_{junction} = J_{rec} + J_{for} = J_{rec,0} \exp(\frac{qV_{pn}}{2kT}) + J_{for,0} \exp(\frac{qV_{pn}}{kT}) \quad (3\text{-}5)$$

But how could we separate the recombination current and forward current?

In order to extract the recombination current from the junction current, we choose two very close junction voltages, that is,

$$V_{pn2} = V_{pn1} + \Delta V > V_{pn1}$$
$$\Delta V \to 0 \quad (3\text{-}6)$$

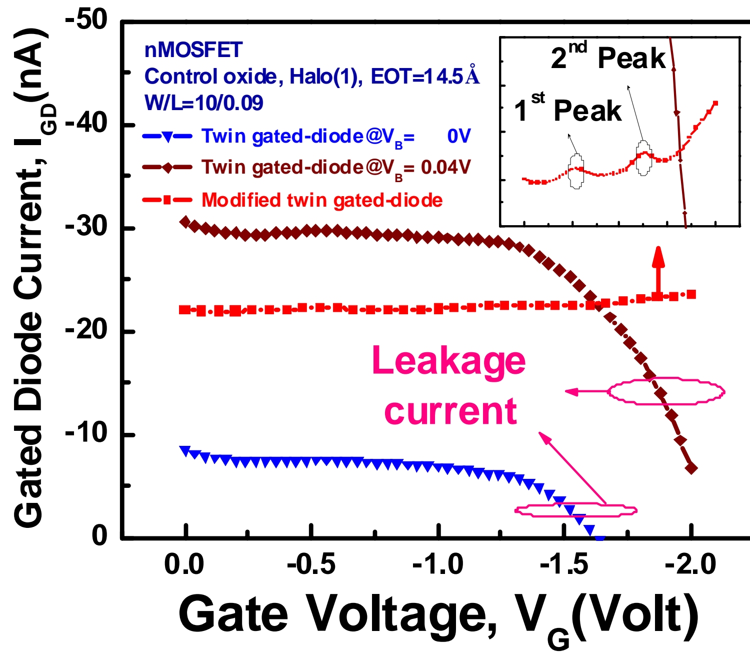


Fig. 3-6 The twin gated-diode measurement. Note, after subtracting the currents with different but approached bulk voltages, we can find the gated-diode current peaks.

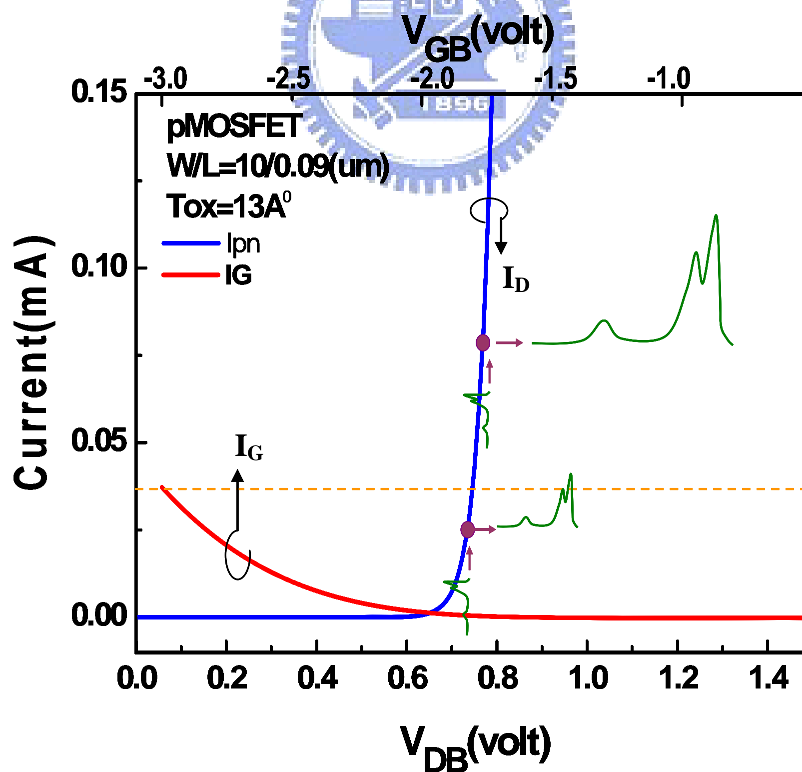


Fig. 3-7 A higher V_{DB} is set to boost the current level of forward and recombination current to exceed gate leakage current level so that the latter can be disregarded.

Then, we subtract the current at V_{pn2} and the current at V_{pn1}, e.g.,

$$I_{pn2} - I_{pn1} = I_{rec,0}[\exp(\frac{\beta V_{pn2}}{2}) - \exp(\frac{\beta V_{pn1}}{2})] + I_{for,0}[\exp(\beta V_{pn2}) - \exp(\beta V_{pn1})], \quad \beta = \frac{q}{kT}$$

$$= I_{rec,0}[\exp(\frac{\beta(V_{pn1} + \triangle V)}{2}) - \exp(\frac{\beta V_{pn1}}{2})] + I_{for,0}[\exp(\beta V_{pn1} + \triangle V) - \exp(\beta V_{pn1})] \qquad (3\text{-}7)$$

Because $\triangle$V is approaching to zero, $\exp(\beta V_{pn1} + \triangle V) - \exp(\beta V_{pn1})$ can be extended by Taylor expansion as,

$$\exp(\beta(V_{pn1} + \triangle V) - \exp(\beta V_{pn1}))$$

$$= 1 + \beta(V_{pn1} + \triangle V - V_{pn1}) + \frac{1}{2!}\beta^2[(V_{pn1} + \triangle V)^2 - V_{pn1}{}^2] + \frac{1}{3!}\beta^3[(V_{pn1} + \triangle V)^3 - V_{pn1}{}^3] + \ldots$$

$$\approx 1 + \Delta V \sum_{n=1}^{\infty} \beta^n \times \frac{V_{pn1}^{n-1}}{(n-1)!} = 1 + \Delta V \beta \sum_{n=1}^{\infty} \beta^{n-1} \times \frac{V_{pn1}^{n-1}}{(n-1)!} = \Delta V \beta \sum_{n=0}^{\infty} \frac{(\beta V_{pn1})^n}{n!}$$

$$= \Delta V \beta \exp(\frac{\beta V_{pn1}}{2})$$

Then, equation (3-7) can be re-arranged as,

$$I_{pn2} - I_{pn1} \simeq I_{rec,0} \triangle V \frac{\beta}{2} \exp(\frac{\beta V_{pn1}}{2}) + I_{for,0} \triangle V \beta \exp(\beta V_{pn1}) = \left(I_{rec,0} \frac{\beta}{2} \exp(\frac{\beta V_{pn1}}{2}) + I_{for,0} \beta \exp(\beta V_{pn1}) \right) \triangle V$$

=>

$$I_{pn2} - I_{pn1} = \triangle V \cdot I_{pn1}, \qquad \text{as } \triangle V \to 0 \qquad (3\text{-}8)$$

From equation (3-8), we conclude that if $\triangle$V is very close to zero, I_{pn2} is just simply the value that I_{pn1} pluses $\triangle V \cdot I_{pn1}$. Based on this conclusion, as shown in Fig. 3-8, we can directly shift the value of I_{pn1}@V_{pn1} (the red-dot curve in this figure) to match the current level of I_{pn2}@V_{pn2} (the blue-solid curve in this figure). The different value of the blue curve and the red-dash curve is the subtracted recombination current (the green-oblique area). At the end, we subtract the shifted I_{pn1}@V_{pn1} (the red-dash curve) from I_{pn2}@V_{pn2} (the blue-solid curve), and then the net gated-diode current can be extracted from the junction current, which can be expressed as,

$$I_{\beta DC-IV} = I_{DC-IV} \cdot \triangle V \frac{q}{kT} \exp(\frac{qV_{pn1}}{kT}) \qquad (3\text{-}9)$$

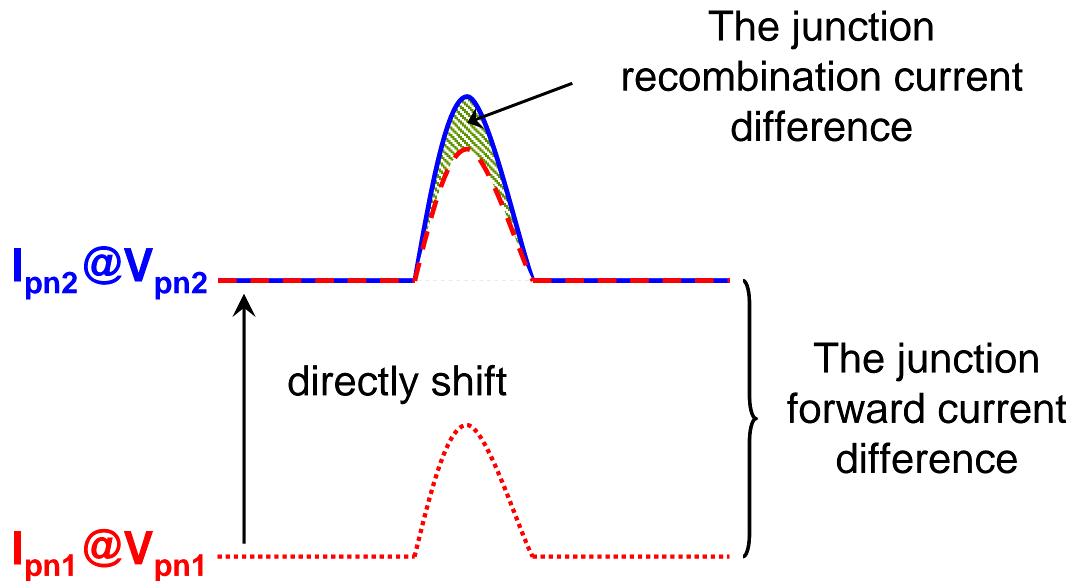


Fig. 3-8 The explanation of how to extract the net recombination current from the junction current, including the forward and recombination currents.

The pure gated-diode current can be calculated from equation (3-9), given by,

$$I_{DC-IV} = \frac{I_{\beta DC-IV}}{\triangle V \frac{q}{kT} \exp(\frac{qV_{pn1}}{2kT})} \tag{3-10}$$

3.5 The Methodology of Boosted DC-IV(β DC-IV)

In this section, we demonstrate how β DC-IV current is extracted:

1st step: *To boost*- we choose an appropriate forward operating voltage (usually larger than the turn-on voltage) forcing on drain(or source)-to-bulk junction so that the current level of the junction can exceed to the current level of the gate-leakage. As shown in Fig. 3-9, when the junction is forward biased on 0.8V, the current levels of bulk and drain are much higher than that of gate-leakage. Hence, the latter can be neglected. But, at the same time, we turn on the junction so the forward current is much larger than the recombination current.

2nd step: Around the operating voltage chosen in the 1st step, we select two voltages which are much close to each other, in this case, 0.805V and 0.795V, respectively. Next DC-IV measurement is performed under junction biased forwardly and gate sweeping from -1 to 2.5V~3V, as shown in Fig. 3-10. In this figure, because the junction is biased forwardly at the voltages higher than the turn-on voltage, the forward diffusion current level is much higher than the recombination current level. Therefore, the peaks of DC-IV current can not be observed.

3rd step: *To shift and to subtract*- as shown in Fig. 3-10, we shift directly the smaller value (the red-dot curve) of these two currents to match the larger value (the black-solid curve) of these two currents and then subtract the black-solid curve and the shifted curve (the red-dash curve.) The calculated result is given in Fig. 3-11(a). This calculated result is not the final DC-IV curve because the junction is biased on a higher forward voltage, and the DC-IV is boosted. Thus, we have to diminish the boosted DC-IV level to the original DC-IV level by using equation 3-9, as shown in Fig. 3-11(b).

Finally, pure DC-IV is extracted, from which three peaks in Fig. 3-11(b) can be observed. These peaks stand for that the relative larger probability of recombination and generation process occurring since the interface defects corresponding to those peaks are more obvious. But where are the positions corresponding to these peaks in the channel lateral direction under Si/SiO_2 interface? This profiling question is important because if we know where these peaks happen, we will understand on which region the interface is damaged the most.

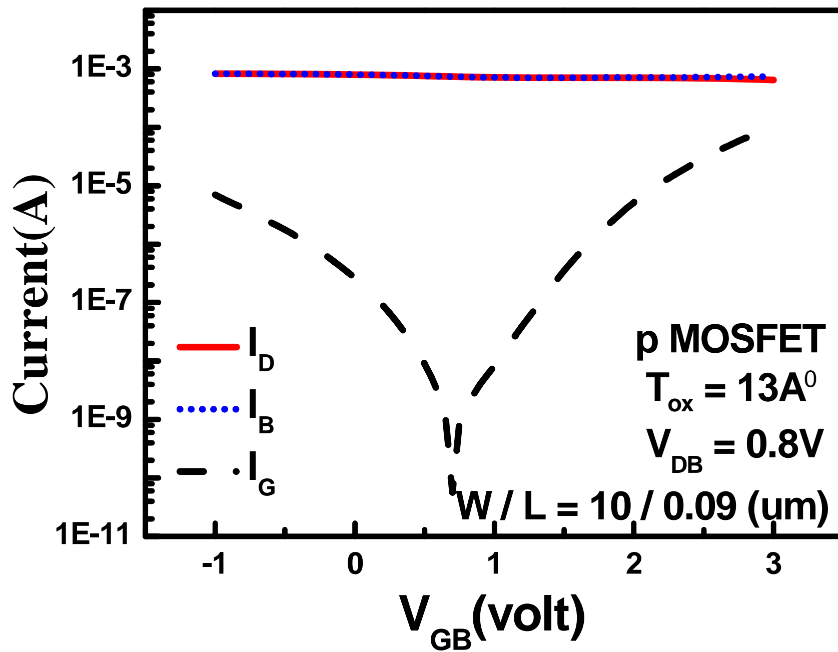


Fig. 3-9 The comparison of the current levels of drain, well, and gate on junction voltage-V_{DB} equivalent to 0.8V.

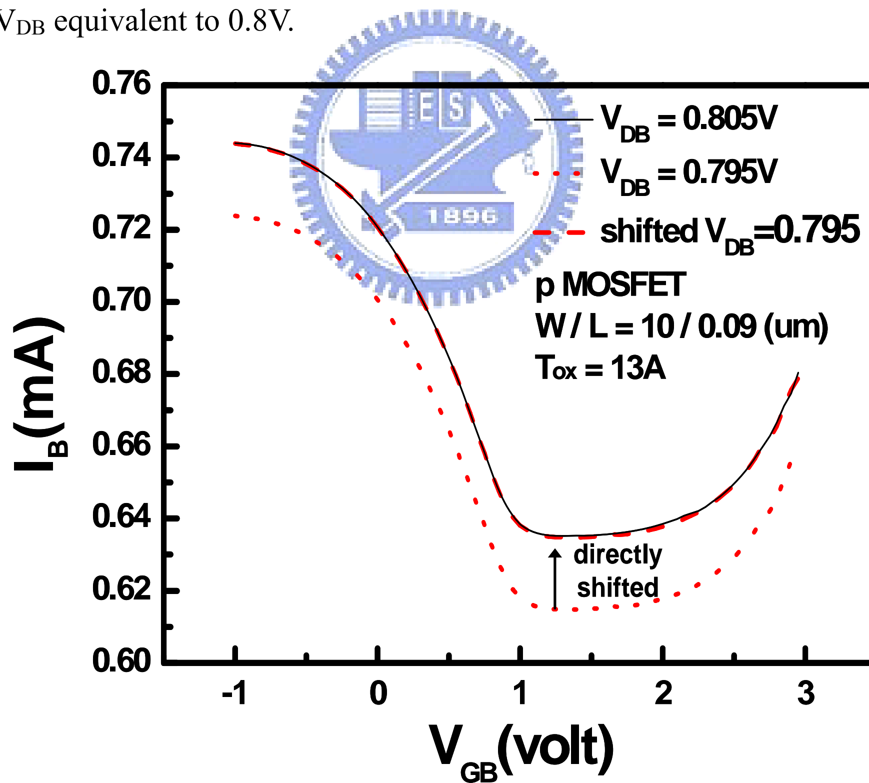


Fig. 3-10 The experimental result of the DC-IV measurements at V_{DB}= 0.805V (the black curve) and V_{DB}= 0.795V (the red curve), respectively. The red-dot curve is directly shifted to match the black-solid curve.

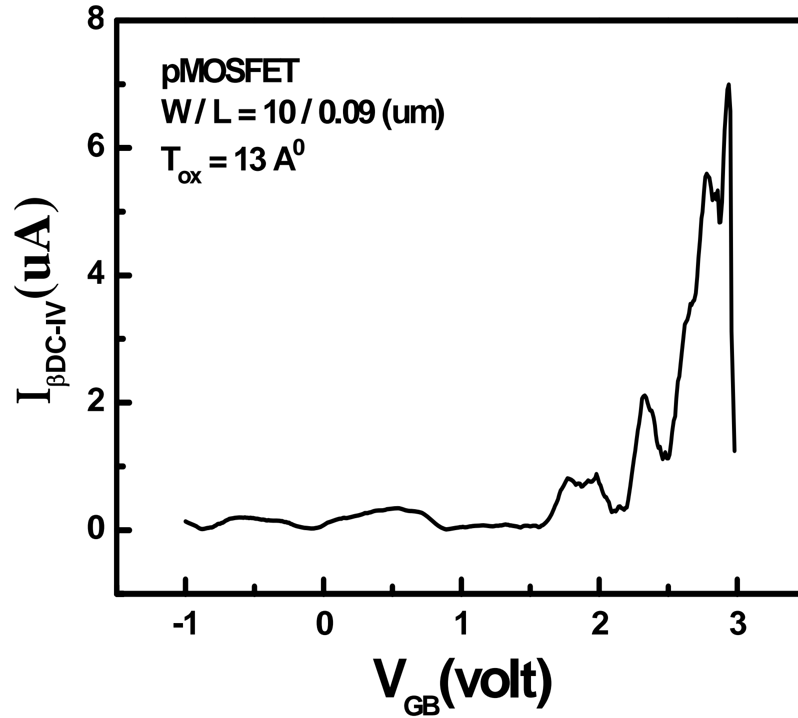


Fig. 3-11(a) The calculated result of βDC-IV is presented, but this result is not the final DC-IV result. Because the junction is biased to a higher level, DC-IV current is boosted. We have to diminish the boosted DC-IV current to the original level by eq. 3-10.

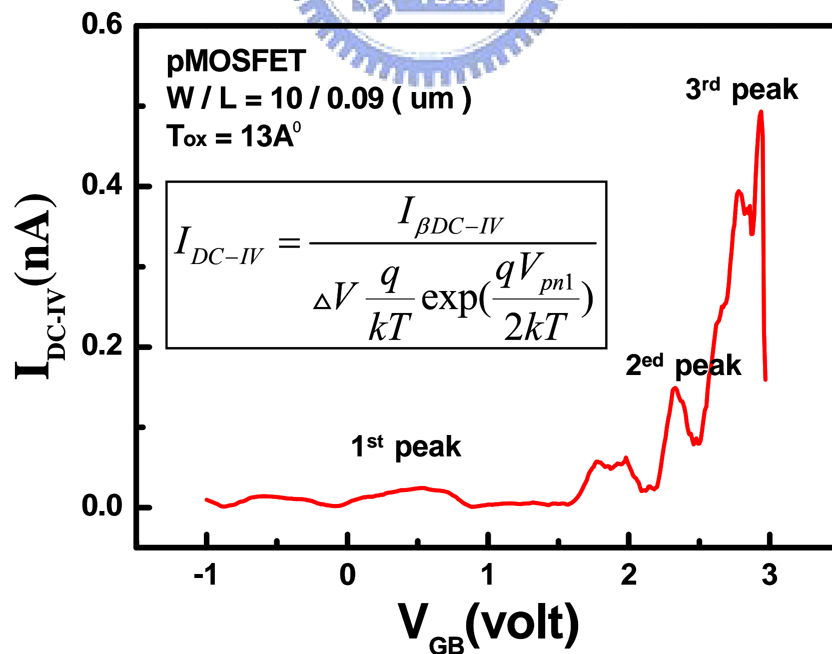


Fig. 3-11(b) By using eq. 3-10, the boosted DC-IV current is diminished to the original DC-IV current.

3.6 Summary

In this chapter, we first introduced the theory of gated-diode measurements. Gated-diode measurement is based on SRH recombination and generation process. For a gate-controlled diode or BJT, by the gate-voltages sweeping, the SCR will be varied in terms of the position. At the end, we can measure the recombination current contributed from the interface defects in the SCR.

Secondly, we introduced DC-IV and gated-diode measurements. Both these measurements are based on SRH theory. But the device model of DC-IV measurement is BJT; the device model of gated-diode measurement is diode. Thus, DC-IV needs four terminals, but gated-diode measurement only needs three terminals. Moreover, for DC-IV, the recombination current is measured from the bulk terminal; for gated-diode measurement, the recombination current is measured from the drain terminal.

Finally, we introduced a new modified DC-IV measurement, boosted DC-IV(β DC-IV), which can be applied in the investigation of the gate-oxide interface reliability with the gate thickness down to 13 A^0. This new modified technique needs a higher junction voltage than the turn-on voltage to boost the junction current to exceed the gate-leakage current and use *to shift and to subtract* method to extract the pure DC-IV current. In the next chapter, we will develop a new DC-IV profiling method to relate the interface traps to the lateral positions.

Chapter 4
New Direct-current Current-Voltage (DC-IV) Profiling Measurement

4.1 Introduction

The lateral profiling of gate oxide interface-traps is the most important issue in gate-oxide reliability. The lateral profiling results help us on the evaluation of the mechanism of the gate-oxide interface reliability. Many groups have done a lot of work on this topic [31]-[32]. The most useful and popular method was built by Chung and Chen [31]. They used the relationship between the local threshold voltage and charge pumping current to derive the relationship between the interface traps and the lateral positions.

$$N_{it}(x) = \frac{1}{f \cdot q \cdot W} \cdot \frac{d\triangle I_{cp}}{dV_{th}} \cdot \frac{dV_{th}}{dx} \tag{4-1}$$

In this equation, f is the frequency used in charge pumping measurement, q is the unit electron charge, W is the width of the device, and V_{th} is the local threshold voltage. Furthermore, the relationship between the positions of the channel length and the local threshold voltage can be found by direct measurement by applying the equation below [31],

$$x = \frac{L \times I_{cp}(V_{gh})}{I_{cp,\max}} \tag{4-2}$$

But, for nano-CMOS devices, instead of LDD doping on the source and drain, the extensive highly doping is employed, which makes the distribution of the local threshold voltage near the drain or source side will be descended much sharply. Therefore, we cannot monitor the profiling of the interface traps into the deep drain side any more by the charge pumping profiling measurement, as shown in Fig. 4-1.

In this chapter, for the first time, we develop a new lateral profiling technique based on the DC-IV measurement. This technique can monitor the lateral distribution of the interface traps into the deep drain side and even through the gate-edge, which is difficulty for the present approaches. Moreover, this new profiling technique helps us realize the evaluation of the reliability mechanism of the gate oxide during stress.

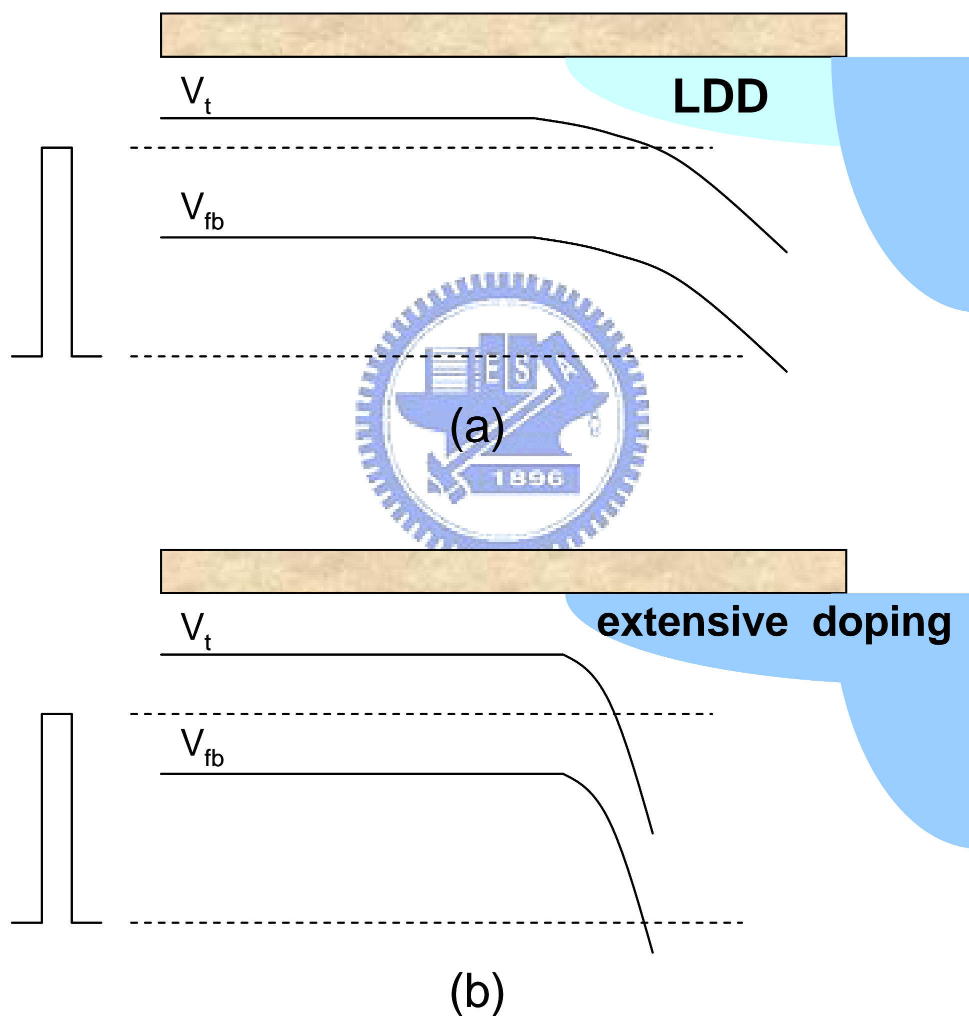


Fig. 4-1The comparison of the distributions of the local threshold voltages for LDD and extensive highly doping respectively. Note, in Fig. 4-1 (b), the extensive highly doping on drain or source side makes the local threshold voltages drop rapidly.

4.2 Concept of New Lateral Profiling Technique

As mentioned in chapter 3.3, we knew that the theory of Gated-Diode measurement is based on the SRH recombination and generation process in SCR beneath surface. Moreover, we also assumed that the main place in which the recombination-generation process happens in the maximal probability is at the intrinsic band-gap level. Besides, the steady-state recombination rate per unit surface area can be obtained from the SRH statistics. It is given by

$$E_{fs} = n_i \sqrt{S_{po} S_{no}} \sinh\left(\frac{qV_{pn}}{2kT}\right) \bullet \{\cosh[E_{fs} - \frac{E_{fp}+E_{fn}}{2} + \frac{1}{2}\ln(\frac{S_{no}}{S_{po}})] + \exp(-\frac{qV_{pn}}{2kT})\cosh[E_{fs} - E_{fi} + \frac{1}{2}\ln(\frac{S_{no}}{S_{po}})]\}^{-1} \quad (4\text{-}3)$$

In this equation, E_{fs} is the surface potential, and E_{fs}-E_{fi} is the energy level of trap centers measured from the intrinsic Fermi level. E_{fn} & E_{fp} are the quasi-Fermi levels for electrons and holes on the surface, respectively, and S_{no} & S_{po} are the surface-recombination velocities on the n and p surface, respectively. From calculations, we can verify that the maximal probability of surface recombination occurs when the surface potential, in eq. (4-3), is obeyed,

$$E_{fs} = \frac{E_{fp} + E_{fn} - \ln\left(\frac{S_{n0}}{S_{p0}}\right)}{2} \quad (4\text{-}4)$$

For most cases, we can further assume S_{no}=S_{po}, and then eq. (4-4) can be re-written as

$$E_{fs,avg} = \frac{E_{fp} + E_{fn}}{2} \quad (4\text{-}5)$$

As a result, we set two conditions for where the recombination and generation process occurs based on SRH theory. The first is the main places in which the recombination-generation process happens at the intrinsic band-gap level in the maximal probability. The second is that the surface recombination occurs in the maximal probability when the surface potential is equal to the average of the sum of

the quasi-Fermi levels for electrons and holes on surface, $E_{fs,avg}$. Hence, we can relate these two conditions and express them as,

$$E_{fs,avg} = \frac{E_{fn} + E_{fp}}{2} = E_{fi} \tag{4-6}$$

The idea of eq. (4-6) is shown in Fig. 4-2. In a gated-diode system, with the same junction voltage but different gate biases, the surface potentials (the green-solid curve) for n and p regions will be modulated, but, due to the unchanged intrinsic band-gap level (the blue-dash curves), the equation (4-6) will set on different positions (the red dots.) As a result, we can explain where the maximal probability of recombination-generation processes happen in terms of different gate biasing by this concept.

For real MOSFETs, the doping profile of the drain and source are complicated in nano CMOS technology, but to be simplified, we take the doping profile for those regions as simple rectangle forms, which eliminates geography effects. Thus, we can treat this lateral profiling technique as only a one-dimensional problem. Furthermore, the electric field distribution near the surface will be co-controlled by the gate bias and junction voltage. But under higher levels of gate biases, the electric field distribution will be mainly governed by gate biases, which makes the electric field distribution near surface more complex, as shown in Fig. 4-3. Depending on electric field distribution near surface, the surface potential will also become more complex. To be simplified, this model does not include this phenomenon, and we assume that the electric fields governed by gate and drain voltages do not be affected to each other, which means they are independent. In short, in this model, the electric field governed by drain voltage only affects the region of SCR; the electric field controlled by gate voltage only influences the surface potentials of n and p regions.

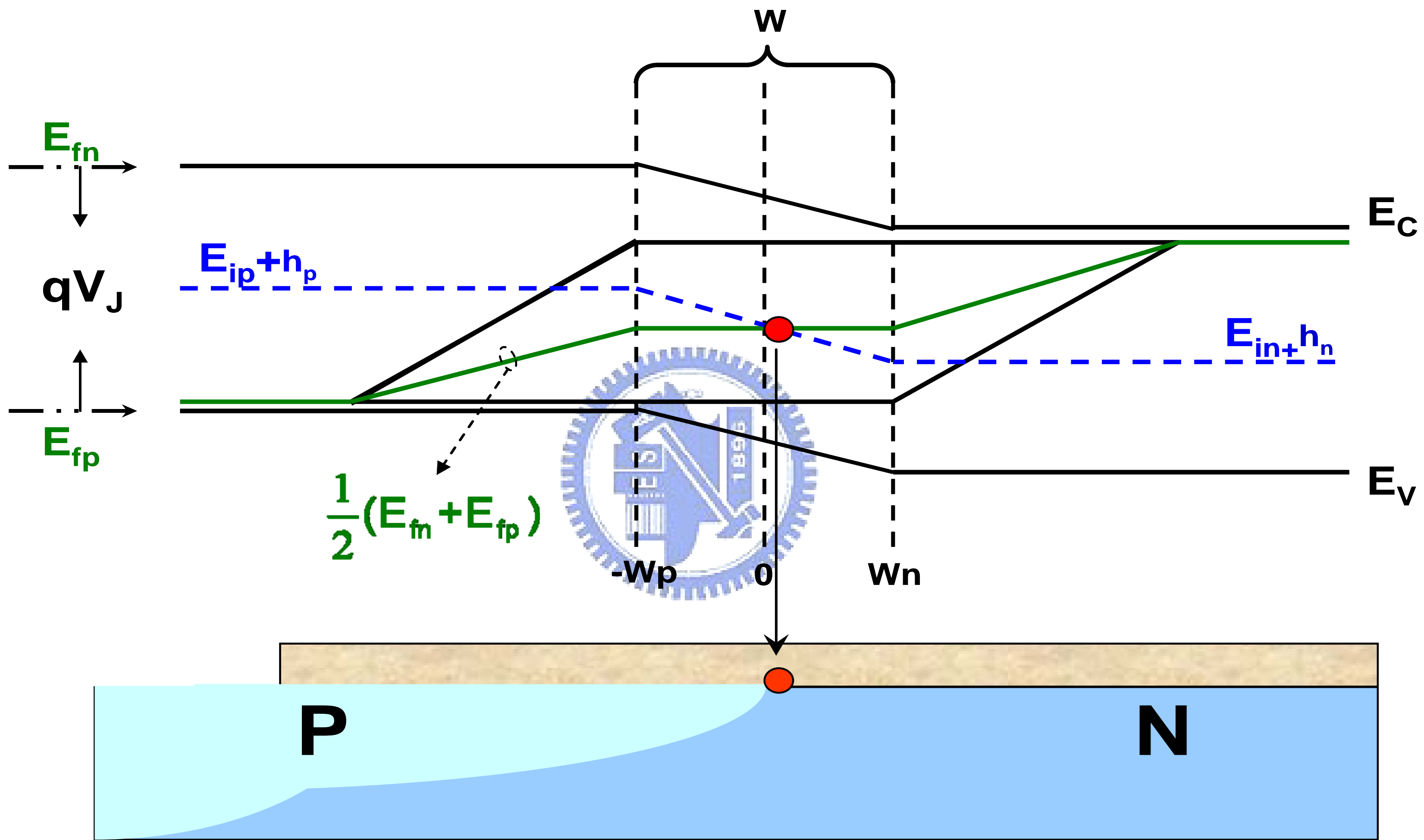


Fig. 4-2 The main idea of our new DC-IV profiling. Based on HSR theory, there are higher probability of R-G current to happen when the carrier concentrations are the lowest, that is, $E_{fs}= E_i$ The blue curve is E_i, and the green curve is E_{fs}.

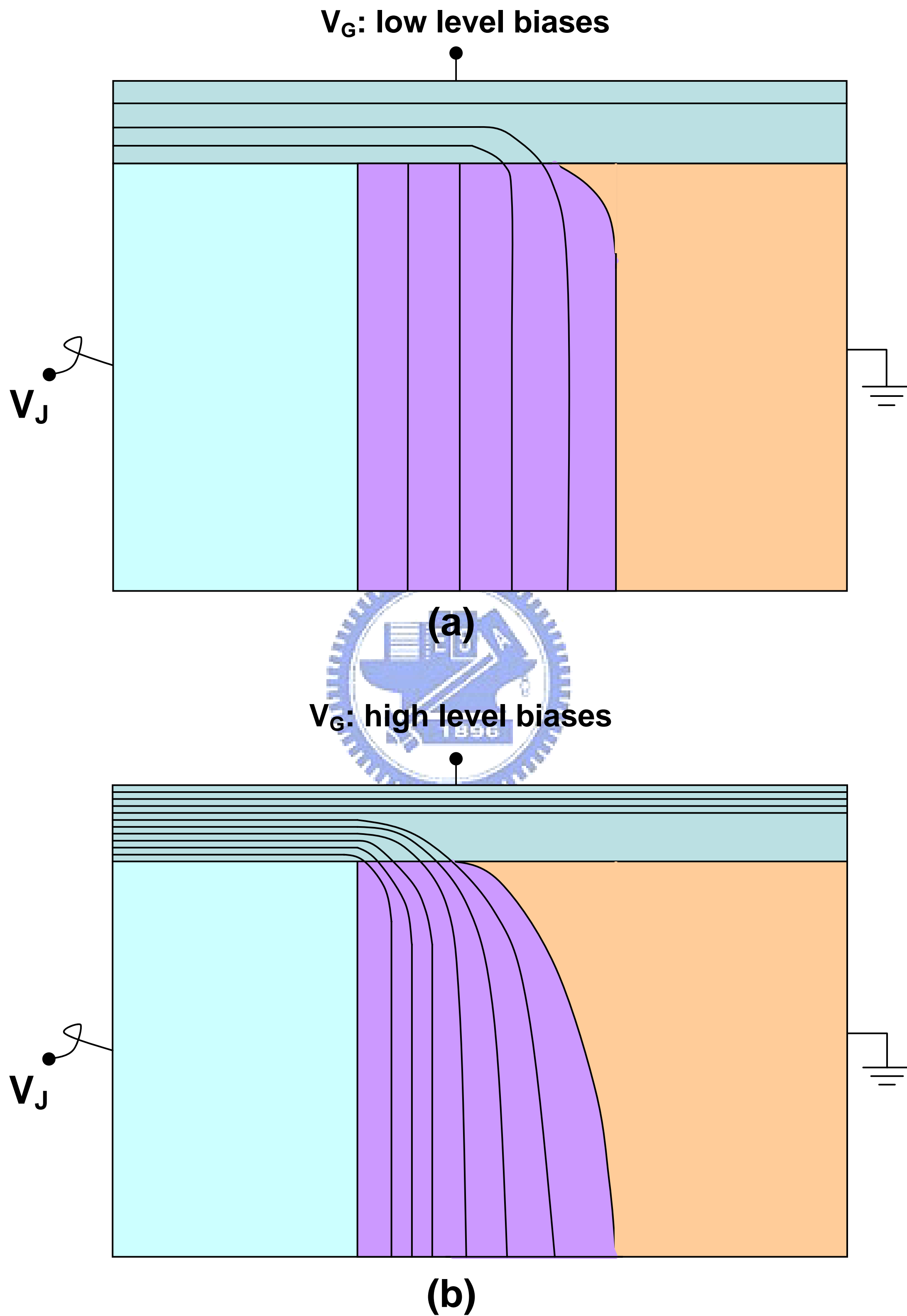


Fig. 4-3 In (a) the field near the surface is controlled by the gate and junction voltages under a low level gate bias; in (b) the filed is governed mainly by the gate under a high level gate bias. The black curves are the electric field lines.

4.3 Derivations of Relationship Between Lateral Positions and Surface Potentials

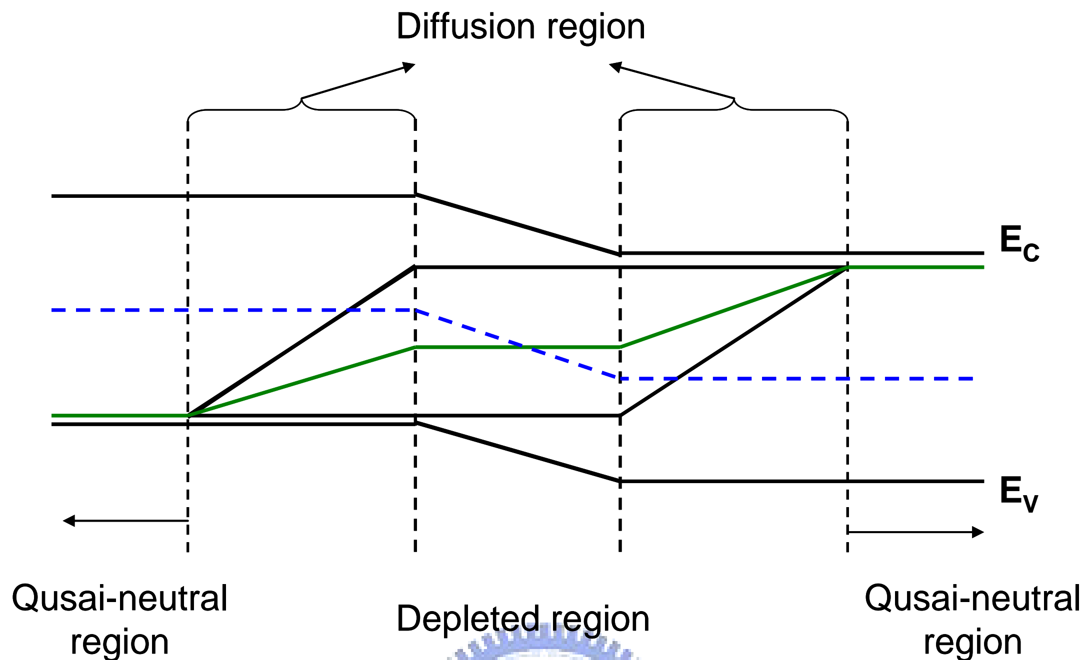


Fig. 4-4 The gated-diode system includes three regions, including the depleted, diffusion, and quasi-neutral regions.

In order to derive the relationship between the surface potentials and lateral positions more specifically, we divide the gated-diode system into three regions, including the depleted, diffusion, and quasi-neutral regions, as shown in Fig. 4-4. The blue-dash curve stands for the intrinsic level, and the green-solid curve stands for the average of sum of the surface potentials for n and p sides in this diagram. The goal of our lateral profiling method is to find the relationship between the blue-dash and green-solid curves in different gate biases in term of positions.

First, we consider the case for the depleted region, as shown in Fig. 4-5. In this figure, the blue-dash line is the intrinsic band-gap level under different surface potentials for n and p regions. For an abrupt junction, it is supposed to be a parabolic curve, but if the width of the depleted region is very narrow, and the carrier

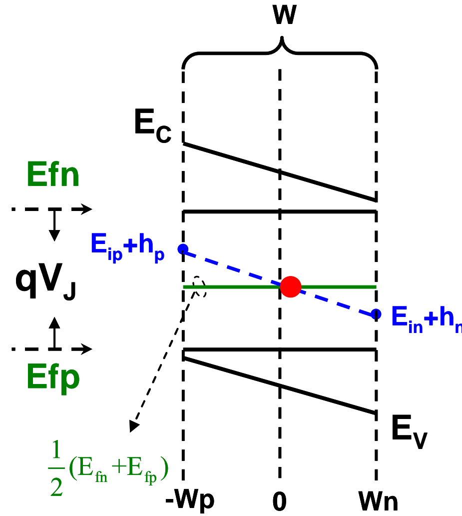


Fig. 4-5 The derivation of our lateral profiling in the case of depleted region. The red dot is what we find in terms of the blue and green curves.

concentrations for n and p sides are strong, the first order approximation for this case is obeyed. Then it can be expressed as,

$$E_i(x)=\frac{1}{W}\left\{\left[(E_{in}-E_{ip})+(h_n-h_p)\right]\cdot x+\left[W_p\cdot(E_{in}+h_n)+W_n\cdot(E_{ip}+h_p)\right]\right\} \qquad (4\text{-}7)$$

Besides, the green line in this figure is the average of the sum of the surface potentials for n and p sides. Because the built-in electric field is very strong, it will keep constant in SCR and can be expressed as,

$$E_{fs,avg}=\frac{1}{2}\cdot\left(E_{fn}+E_{fp}\right) \qquad (4\text{-}8)$$

By using eq. 4-6, eq. 4-7 will be equal to eq. 4-8, and the equator can be re-organized as,

$$x=\frac{\frac{1}{2}W\left(E_{fn}+E_{fp}\right)-\left\{W_p\left[E_{in}+h_n\right]+W_n\left[E_{ip}+h_p\right]\right\}}{E_{in}-E_{ip}+h_n-h_p} \qquad (4\text{-}9)$$

when $h_n\le\left(\frac{E_{fn}+E_{fp}}{2}-E_{in}\right)$ & $h_p\ge\left(\frac{E_{fn}+E_{fp}}{2}-E_{ip}\right)$

As a result, the correlation between the lateral positions and surface potentials in the depleted region has been set.

Next, the case for the diffusion region will be considered, as shown in Fig. 4-6. We take p region as an example, and n region can be taken in the same way. In this case, the quasi Fermi-level is a constant, and the average of sum of surface potentials for n and p regions is dependent on the lateral positions, that is,

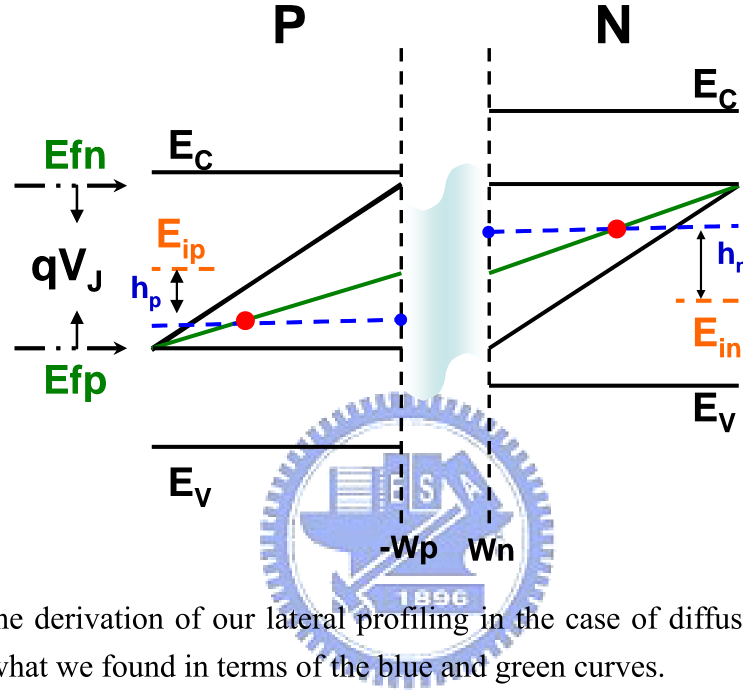


Fig. 4-6 The derivation of our lateral profiling in the case of diffusion region. The red dot is what we found in terms of the blue and green curves.

$$E_{fs,avg} = \frac{1}{2}\left(E_{fp} + E_{fn}\right) = \frac{1}{2}\cdot\left(E_{fp} + E_{fn}(x)\right) \tag{4-10}$$

$$E_{fi} = E_{ip} + h_p \tag{4-11}$$

In eq. (4-10), because the majority carrier of p region is holes, the quasi Fermi level for holes is constant. Additionally, the quasi Fermi level for electrons is dependent on the minority concentration, which can be expressed as,

$$E_{fn}(x) = E_{ip} + kT\left[\ln\left|\frac{n_{p0}}{n_i}\right| + \ln\left|K_n \cdot \exp(-\frac{x}{L_n}) + 1\right|\right]$$
$$K_n = \exp(\frac{qV_J}{kT}) - 1 \tag{4-12}$$

In eq. (4-12), E_{ip} is the intrinsic Fermi level for p region, and n_{p0} is the minority

carrier concentration in p region, and n_i is the intrinsic concentration, and L_n is the electron surface diffusion length. To make this equation simplified, we use the first order approximation to simplify $E_{fn}(x)$ by observing the differentiation of $E_{fn}(x)$,

$$\frac{dE_{fn}(x)}{dx} = \frac{kT}{K_n \exp(-\frac{x}{L_n})+1} \cdot \left(-\frac{K_n}{L_n} \right) \exp(-\frac{x}{L_n}) \approx -\frac{kT}{L_n} \tag{4-13}$$

$$if \ K_n \exp(-\frac{x}{L_n})+1 \gg 1$$

The derivation in eq. (4-13) will be hold only as $K_n \exp(-x/L_n)+1 \gg 1$, which is set in general cases when V_J>>the thermal voltage. Based on the result of eq. (4-13), we can simplify eq. (4-12) by the first order approximation, that is,

$$E_{fs,avg} = \frac{1}{2} \cdot \left(E_{fp} + E_{fn} - \frac{kT \cdot (x + W_p)}{L_n} \right) \tag{4-14}$$

By using eq. (4-6), eq. (4-11) will be equal to eq. (4-14), which can be re-written as,

$$x = \frac{L_n}{kT} \left[2 \cdot (E_{ip} + h_p) - (E_{fp} + E_{fn}) \right] - W_p, \quad \text{for p region}$$

$$\text{when} \ \ h_p < \frac{E_{fn} - E_{fp}}{2} - E_{ip} \ \& \ h_p \geq E_{fp} - E_{ip} \tag{4-15}$$

In the same way, the case for n region can be represented as,

$$x = \frac{L_p}{kT} \left[2 \cdot (E_{in} + h_n) - (E_{fp} + E_{fn}) \right] + W_n, \quad \text{for n region}$$

$$\text{when} \ \ h_n < (E_{fn} - E_{in}) \ \& \ h_n \geq \frac{E_{fn} + E_{fp}}{2} - E_{in} \tag{4-16}$$

As a result, the relationship between the lateral positions and surface potentials for n and p sides in the diffusion region has been set.

Next, we consider the case for the quasi neutral region, as shown in Fig. 4-7. We take n region as an example, and p region can be taken in the same way. When $E_{fn}= E_{in}$, the region beneath n surface will be depleted, and that beneath p surface will be accumulated by majority carriers, holes, as shown in Fig. 4-7(a). When $E_{fn}< E_{in}$, the region beneath n surface will be inverted, and the accumulating holes in p region will flow into the region beneath n surface. At the end the channel is formed, and recombination-generation current can not be contributed any more beneath the surface in this case.

As a result, we derive the relationship between the surface potential and the lateral positions by considering about the relationship between the surface potential and the average of the sum of the quasi-Fermi levels for electrons and holes on surface. In order to derive the relationship between the surface potentials and lateral

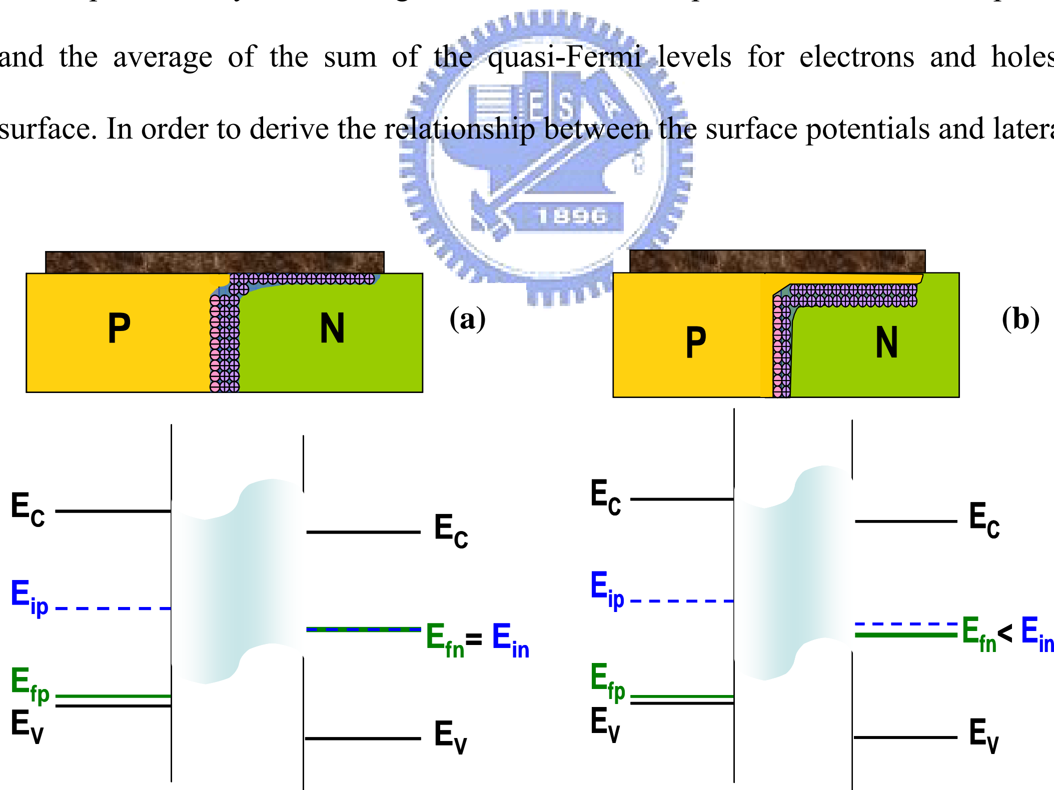


Fig. 4-7 In the quasi neutral region, the R-G current can not be contributed any more due to the formation of channel.

positions more specifically, we divide the gated-diode system into three regions, including the depleted, diffusion, and quasi-neutral regions. Moreover, the first order

approximation can be used to simplify the expression of equations.

At the end of this section, we summarize the above equations in List 4-1:

1. Quasi neutral p region:

When $h_p > E_{fp} - E_{ip}$, channel formed; no R-G current contributed near suface

2. Diffusion p region:

$$x = \frac{L_n}{kT}\left[2\cdot(E_{ip}+h_p)-(E_{fp}+E_{fn})\right]-W_p, \quad \text{for p region}$$

$$\text{When } h_p < \frac{E_{fn}-E_{fp}}{2}-E_{ip} \ \& \ h_p \geq E_{fp}-E_{ip} \qquad (4\text{-}15)$$

3. Depleted region:

$$x = \frac{\frac{1}{2}W\left(E_{fn}+E_{fp}\right)-\left\{W_p\left[E_{in}+h_n\right]+W_n\left[E_{ip}+h_p\right]\right\}}{E_{in}-E_{ip}+h_n-h_p}$$

$$\text{When } h_n \leq \left(\frac{E_{fn}+E_{fp}}{2}-E_{in}\right) \ \& \ h_p \geq \left(\frac{E_{fn}+E_{fp}}{2}-E_{ip}\right) \qquad (4\text{-}9)$$

4. Diffusion n region:

$$x = \frac{L_p}{kT}\left[2\cdot\left(E_{in}+h_n\right)-(E_{fp}+E_{fn})\right]+W_n, \quad \text{for n region}$$

$$\text{When } h_n < (E_{fn}-E_{in}) \ \& \ h_n \geq \frac{E_{fn}+E_{fp}}{2}-E_{in} \qquad (4\text{-}16)$$

5. Quasi neutral n region:

When $h_n > E_{fn} - E_{in}$, channel formed; no R-G current contributed near surface

List 4-1 The derivations of the relationship between surface potentials and positions.

This list describes the correlation of the surface potentials and the lateral positions, but it is difficult to measure the surface potential of a device directly in

electric measurements. Instead of that, we can only measure the gate voltage. Hence, in the next section, we will find the relationship between the gate voltage and surface potentials. Through this relationship, the relationship between the gate voltage and positions can be connected, which is what really we want.

4.4 Theory of Surface Potentials on Gated-Diode Systems

The theory of surface potentials for MOSCAP was first introduced by C.G. B. Garrett and W. H. Brattain in their great article, "Physical Theory of Semiconductor Surfaces[26]," published in 1955. For general cases, they revealed that the net surface charge can be described by,

$$\begin{aligned} Q_s &= -2qn_i L_D[\exp(u_{Fp}-u_s)-\exp(u_{Fp}) \\ &\quad +\exp(u_s-u_{Fn})-\exp(-u_{Fn})+2u_s\sinh u_{Fp}]^{1/2} \\ &\text{where} \\ u_s &= \frac{q\phi_s}{kT},\ u_{Fp}=\frac{q\phi_{Fp}}{kT},\ u_{Fn}=\frac{q\phi_{Fn}}{kT},\ \text{and } L_D=\left[\frac{kT}{q}\frac{K_s\varepsilon_0}{2qn_i}\right]^{1/2} \end{aligned} \qquad (4\text{-}16)$$

In eq. (4-16), we take p-type substrates as an example, and n-type substrates can be taken in the same way. ϕ_s is the surface potential, and ϕ_{Fp} and ϕ_{Fn} are the potentials at the quas-Fermi levels for holes and electrons, respectively, and L_D is the intrinsic Debye length. Based on this equation, the conditions of surface charges can be defined, which are accumulation, depletion, and inversion. In 1966, A. S. Grove and D. J. Fitzgerald considered the theory of surface potentials on gated-diode systems based on Garrett and Brattain's theory and achieved triumph [25].

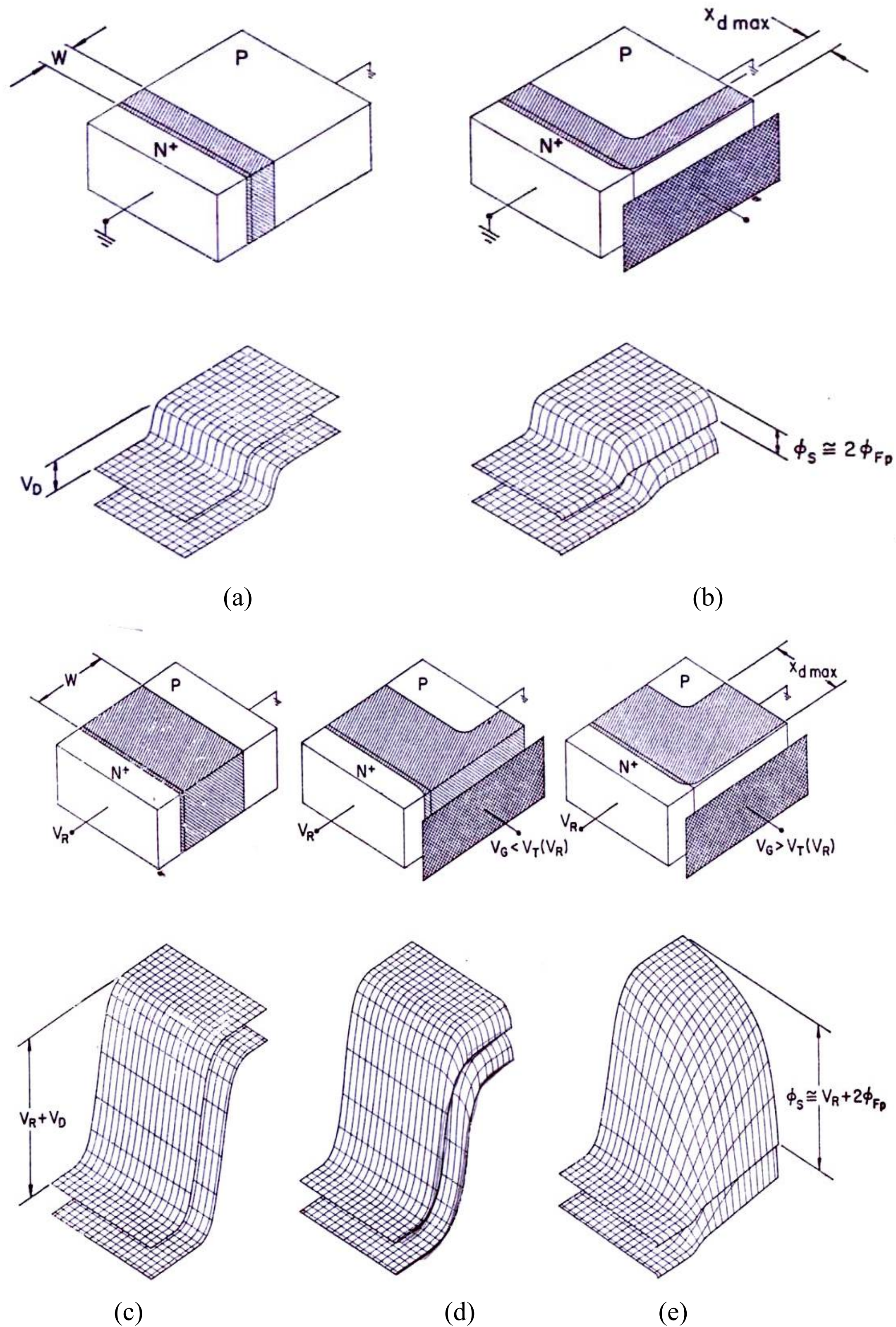


Fig. 4-8 The band diagram for gated-diode systems under equilibrium (without junction voltages,) (a) and (b), and non- equilibrium (with junction voltages,) (c) to (e).[25]

For a gated-diode system, first we consider the equilibrium case, which means the absence of junction voltages, as shown in Fig. 4-8 (a) and (b). As a function of the two directions- x and y axes, electron energy is represented by the conduction and valence bands. Because surface potentials is not present, the energy bands do not change in the x axis, and only the carriers vary because of the diffusion and built-in voltage in the y axis, which is simply a diode, as shown in Fig. 4-8 (a). When surface voltages is present without junction voltage, this case can be thought as a MOSCAP by Grove and Fitzgerald's theory, as shown in Fig. 4-8 (b). Note the strong inversion condition can be given by $\phi_s = 2\phi_{Fp}$ well approximately, where ϕ_{Fp} is the substrate Fermi potentials.

On the other hand, Figs. 4-8 (c) to (e) show the case for the non-equilibrium condition. This case exists when junction voltages are presented. In Fig. 4-8 (c), without the presentation of surface potentials, this case is simply a non-equilibrium diode, and the depleted region is modulated by junction voltages. In Fig. 4-8 (d), for a p substrate, a small positive gate voltage forces on surface but is not large enough to make the surface inverted but only depleted. Fig. 4-8 (e) illustrates the case that the gate voltage applied on surface is large enough to overcome the effect of the junction voltage, and the surface is inverted in the p region. In terms of band diagram, the bands of the p-region surface are bent deeply enough to match the bands of the n-region surface, which makes the majority carriers on the conduction band edge in the n-region surface is easy to transport to that in the p-region. Thus, the channel is formed.

In one word, we make the comparison of the cases for equilibrium and non-equilibrium on gated-diode systems. For the equilibrium case, the condition for

the formation of channel for carriers is to overcome the strong-inversion condition, that is, $\phi_s=2\phi_{Fp}$. When junction voltages is applied, for the non-equilibrium case, the condition for the formation of channel for carriers has to be overcome not only by the original strong-inversion condition but also the junction voltage, e.g.,

$$\phi_s = V_J + 2\phi_{Fp}, \qquad \text{for p substrates} \tag{4-17}$$

Based on Garrett and Brattain's theory combined with Grove and Fitzgerald's theory, the net surface charge for gated-diode systems can be described by eq. (4-16) and eq. (4-17), and if we substitute eq.(4-17) into eq. (4-16), the net surface charge for gated-diode systems can be expressed as,

$$Q_s = -2qn_iL_D[\exp(u_{Fp} - u_s) - \exp(u_{Fp}) + \exp(u_s \underline{- u_{Fp} - v_j}) - \exp(\underline{-u_{Fp} - v_j}) + 2u_s \sinh u_{Fp}]^{1/2} \tag{4-18}$$

where

$$u_s = \frac{q\phi_s}{kT},\ u_{Fp} = \frac{q\phi_{Fp}}{kT},\ v_j = \frac{qV_J}{kT},\ \text{and } L_D = \left[\frac{kT}{q}\frac{K_s\varepsilon_0}{2qn_i}\right]^{1/2}$$

Eq. 4-16 is set when two assumptions below hold [25],

(1) The quasi-Fermi level for the majority carriers of the substrate does not vary in the substrate. When the surface is depleted or inverted, this assumption introduces little errors since majority carriers are then only a negligible part of the surface space-charge.

(2) The quasi-Fermi level for the minority carriers of the substrate is separated by the applied junction voltages from the quasi-Fermi level for majority carriers, that is $\phi_{Fn}= \phi_{Fp}+ V_J$ for a p-type substrate.

Eq. (4-18) is involved to be applied in n and p regions in a gated-diode system, respectively, to describe the surface potentials in our lateral profiling technique, and

we use the equation below to connect surface potentials and gate voltages,

$$h_n = -q \cdot (V_G - V_{ox-n} - V_{fb-n}) \quad \text{for n region} \tag{4-19}$$

$$h_p = -q \cdot (V_G - V_{ox-p} - V_{fb-p}) \quad \text{for p region} \tag{4-20}$$

where h_n & h_p are the surface electron energies for n and p regions, respectively; V_{ox-n} and V_{ox-p}: the insulator voltage drops for n & p regions, respectively; V_{fb-n} and V_{fb-p} are the flat-band voltages for n & p regions, respectively. Fig. 4-9 illustrates the calculated results for n and p regions according to eq. (4-19) and eq. (4-20), respectively.

Until now, the theory of this lateral profiling technique based on gated-diode systems has almost been described. In the next section, some details will be considered, which lets this model more complete. These details will be the most important part to build the final results of this lateral profiling technique.

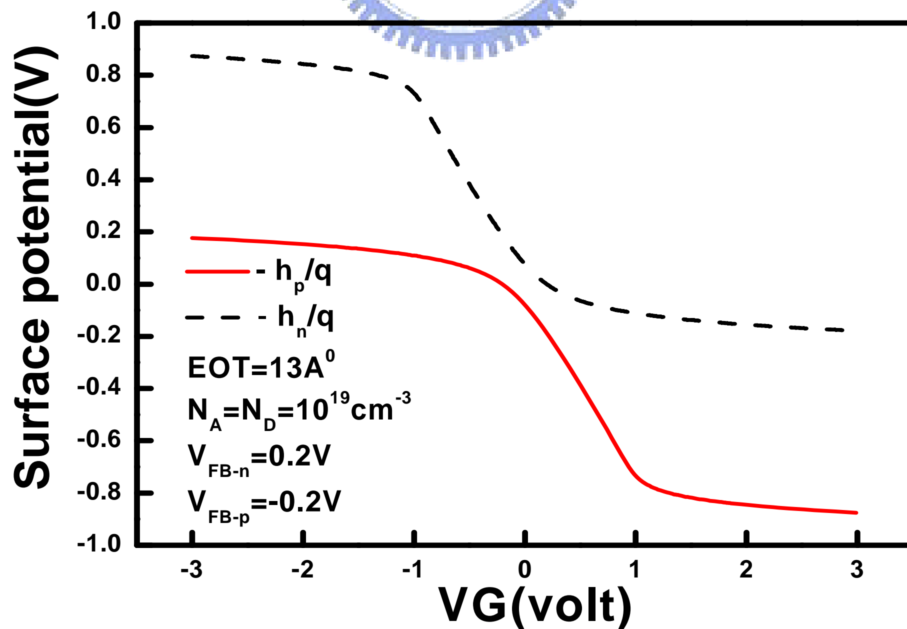


Fig. 4-9 The surface potentials versus gate voltages under gated-diode system for n and p regions, respectively.

4.5 Modulation of Junction Depletion Width with Varying Surface Potentials

In section 4.2, in order to simplify this model, we assume that the electric field governed by drain voltages only affects the region of SCR; the electric field controlled by gate voltages only influences the surface potentials of n and p regions. However, in fact, this assumption is wrong. In Fig. 4-3, we observe that the electric field near surfaces will be affected by gate voltages, and so does the depleted region of junctions. Thus, the width of depleted region is modulated by gate voltages and junction voltages.

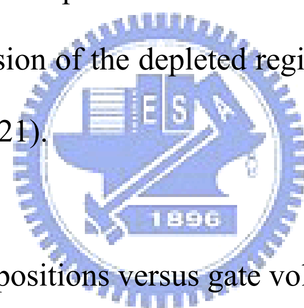
When gate voltages are applied on the surfaces of n and p regions, the surface potentials of n and p regions is corresponded to the applied gate voltages. Because the quasi-Fermi levels for n and p regions are different, the surface potentials of them will be different, as shown in Fig. 4-8. Therefore, the voltage drop will be set when the difference of the surface potentials for p and n region is present. This extra voltage drop as well as the junction bias will re-build a new junction depletion region. The depletion width equation of p-n junction for a gated-diode system can be re-written as,

$$W_{dep} = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_A + N_D}{N_A \cdot N_D}\right)\left(\psi_{bi} + V_J + \left[\frac{h_p(V_G)}{q} - \frac{h_n(V_G)}{q}\right]\right)} \qquad (4\text{-}21)$$

In eq. (4-21), Ψ_{bi} is the built-in potential of junctions, and V_J is the junction voltages (positive for reverse bias, negative for forward bias,) and $-h_p(FIG)/q$ and $-h_n(FIG)/q$ are the surface potentials for n and p regions, respectively. By using this equation, we can explain why the width of the depleted region of the junction is varied driven by the gate voltages.

4.6 Result and Summary

In this chapter, we introduced a new interface-traps lateral-profiling technique based on DC-IV measurement. The main concept of this technique is that where the recombination and generation process happens in the maximal probability is the positions that the intrinsic Fermi level equaling to the average of the sum of the quasi-Fermi levels for n and p regions, respectively. Based on this concept, List 4-1 can be derived. Next, we adopted Garrett and Brattain's theory and used eq. (4-18) in n and p regions to describe the surface potentials in gated-diode systems and used eq. (4-19) and (4-20) to connect surface potentials and gate voltages. At the end, in order to explain the modulation of the depleted width with the vibration of the gate voltages, we have re-written the expression of the depleted region width by involving the terms of surface potentials as eq. (4-21).



Consequently, the lateral positions versus gate voltages diagram can be plotted, as shown in Fig. 4-10. Through this diagram, we can monitor the interface traps in terms of the lateral positions by sweeping gate voltages. But there are two boundary conditions when we use this lateral profiling technique. The first boundary condition, as mentioned before, is the case of quasi-neutral regions. In this case, the channel is formed, and the recombination current beneath surfaces will be never contributed. The second boundary condition is the breakdown under high level of gate voltages.

Based on Fig. 4-9 and using eq. (4-22) as followed,

$$\Delta I_{GD}(V_G) = \left(\frac{1}{2} q W \sigma v_{th} n_i\right) \Delta N_{it}(x) \qquad \text{4-22}$$

we may transform I_{GD} to N_{it} in terms of the lateral positions. In eq. (4-22), q is the unit

charge, W is the channel width, σ is the defect capture cross section, v_{th} is thermal velocity, and N_{it} is interface states. The values of σ and v_{th} are 1×10^{-15} cm^2 and 1×10^7 cm/sec, respectively[33]. The interface-traps versus lateral-positions plot taken Fig. 3-12 (b) as an example based on eq. (4-22) is shown in Fig. 4-11. We find that, for a fresh device, the region around the gate edge is damaged most, and the position on drain junction edge will also be damaged. This diagram helps us realize more about the damaged positions induced by process or stress by monitoring the interface traps accurately in high resolution.

At the end of this section, we will introduce other recombination current sources, expect for the interface traps on the surface. This is important because the recombination currents measured by DC-IV (gated-diode) measurement are not only contributed by the interface traps on surfaces. In fact, the three main components of the traps centers exist in a gated-diode system, including the trap-centers in the metallurgical junction, the trap-centers in the depleted region induced by surface fields, and, as well known, the trap-centers on surface, as shown in Fig. 4-12. In this figure, the blue triangles stand for the trap-centers in the metallurgical junction, and the green circles stand for the trap-centers in the depleted region induced by surface fields, and the red crosses stand for the trap-centers on surface. All of them may contribute to the recombination currents. But, for general cases, the interface of surface is damaged the most during the operation and the process, and thus the recombination current contributed by this component will dominate in these three components. Depending on how the regions are damaged by the operation or the process, the other components may contribute more the recombination current than the trap centers on surfaces do.

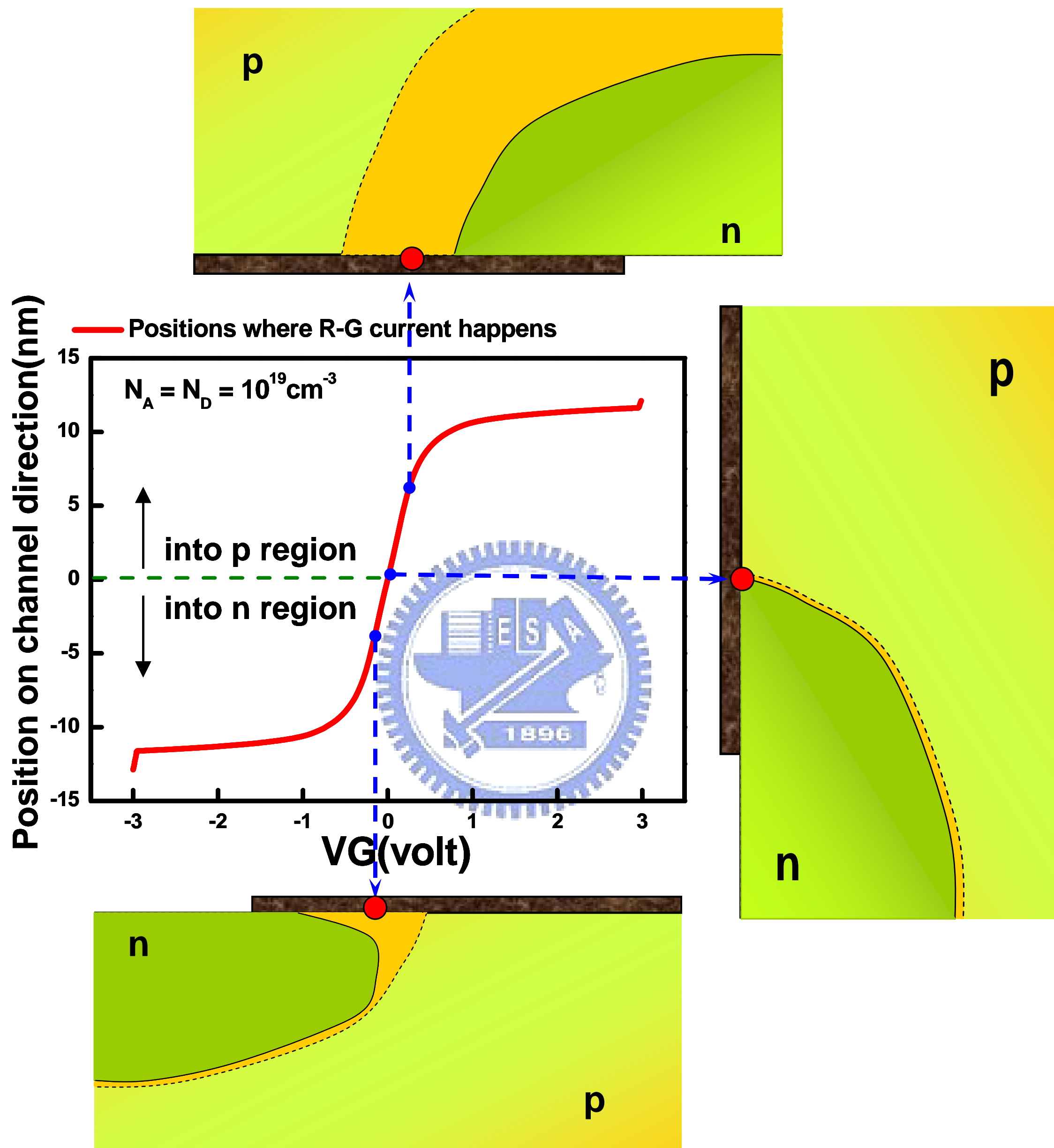


Fig. 4-10 The lateral positions versus gate voltages plot in a gated diode system.

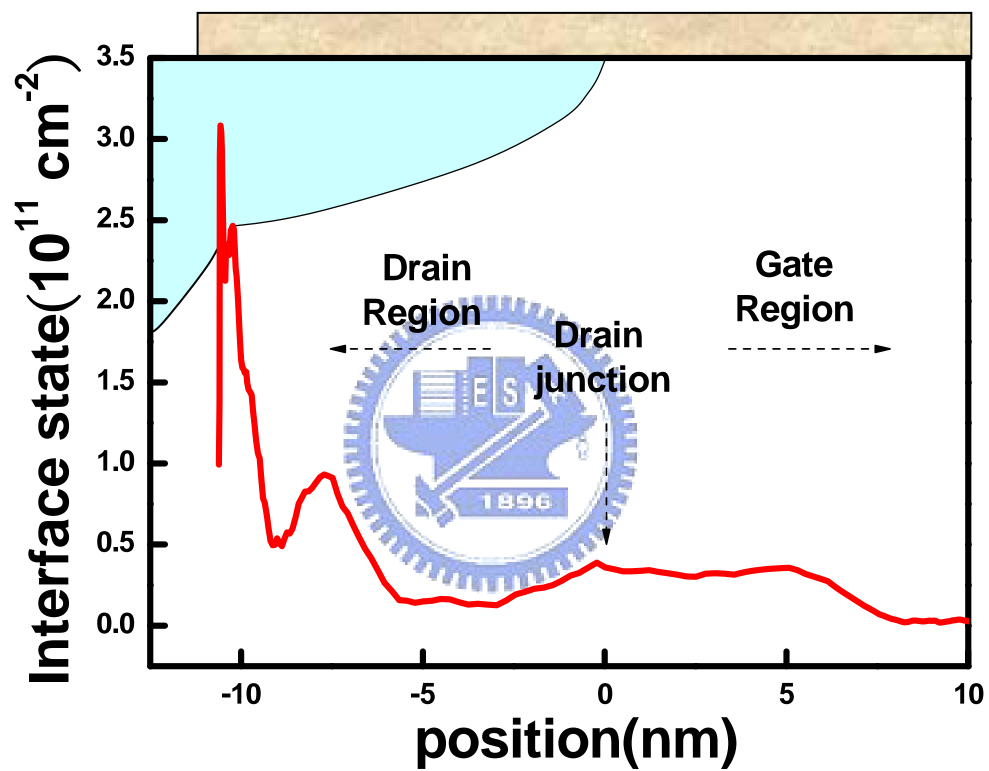


Fig. 4-11 The interface-traps versus lateral-positions plot taking Fig. 3-12 (b) as an example, based on Eq. (4-22).

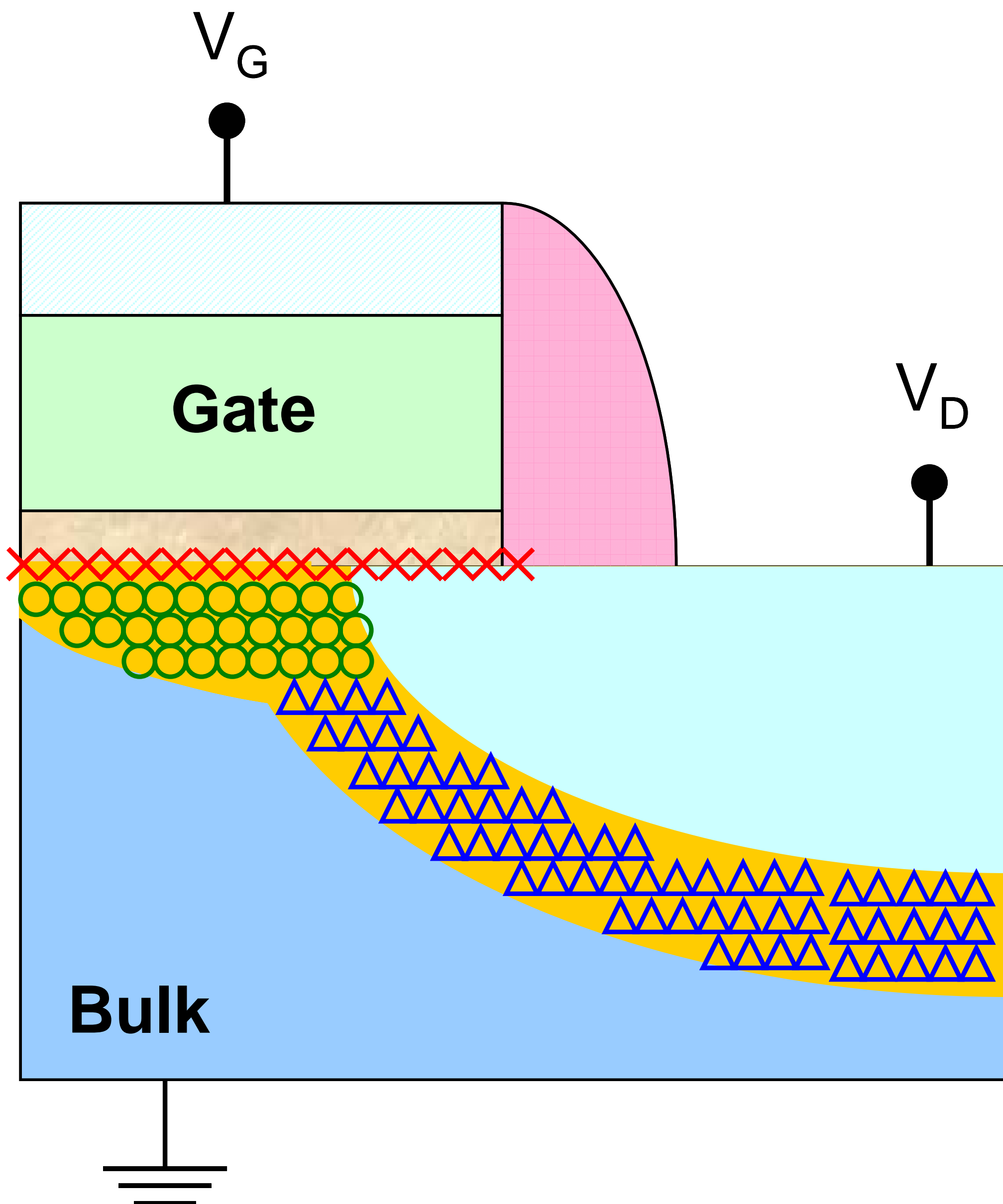


Fig. 4-12 The three main components of the traps centers exist in the gated-diode system, including the trap-centers in the metallurgical junction, the trap-centers in the depleted region induced by surface fields, and, as well known, the trap-centers on surface. In this figure, the blue triangles stand for the trap-centers in the metallurgical junction, and the green circles stand for the trap-centers in the depleted region induced by surface fields, and the red crosses stand for the trap-centers on surface.

Chapter 5
Analysis of Reliability Issues in Strained CMOS Devices

5.1 Introduction

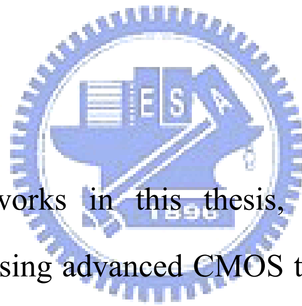
Mobility-enlargement technology is an important approach to realize high-speed scaled CMOS devices. Recently various mobility-enhancement technologies have been developed to reach this goal, such as uniaxial strain induced by the nitride-cap stressor[2], uniaxial strain induced by SiGe source/drain[6], biaxial strain induced by SiGe on substrate[4], the hybrid substrate technology incorporating germanium on various substrate orientations[10], and so on. Those advanced strain technologies can achieve significant drive current enhancement. Although many technologies have been developed to boost the drive current, the reliability issues for those technologies have been rarely studied.

In [16,17], Chung and Liu reported the importance of reliability for strained devices and the hybrid substrate technology, and it is emphasized that a large enhancement of mobility will adversely degrade the device reliability. In [18], Chung and Huang first reported that, for nMOSFETs, tensile cap stressor device is much better in terms of reliability and performance. Besides, for pMOSFETs, SiGe S/D devices with EDB[6] is most promising in terms of performance and reliability. Based on those significant results, we will characterize the reliabilities of strained CMOS devices developed in the recent years and investigate them by our new DC-IV method and its lateral profiling technique. We divide the contents into two main components. The first part is to investigate hot carrier degradation for strained nMOSFETs. The other part is to analysis NBTI degradation for strained pMOSFETs. Hot carrier degradation for nMOSFET's and Negative Bias Temperature Instability (NBTI)

degradation for pMOSFETs are very important reliability issues of the recent aggressively scaled down devices. In hot carrier and NBTI degradation, threshold voltage shift, drain current degradation and trans-conductance degradation will be observed by electric measurement. These stresses generate the interface trap and fixed oxide charges.

After those stresses, an improved charge pumping method will be employed to exactly analyze the interface state situation after hot carrier stress and FN stress. We will explain the mechanism of the devices degradations after those stresses by interface traps lateral profiling based on β DC-IV measurement.

5.2 Device Preparation



For the experimental works in this thesis, two splits of nMOSFETs or pMOSFETs were fabricated using advanced CMOS technology. The schematic cross section diagram of nMOSFET splits is shown in Fig. 5-1. In this figure, Fig. 5-1(a) is the bulk-Si device, and Fig. 5-1(b) is the SiC on Source/Drain devices(uniaxial-strain,) and Fig. 5-1(c) is the CESL(contact etching stopping layer) capped device (uniaxial-strain,) and Fig. 5-1 (d) is SS(D)OI(strained silicon (directly) on insulator) device (biaxial-strain,) and Fig. 5-1(e) is the SiGe on substrate device (biaxial-strained). All nMOSFETs are <100> channel on (100) substrate. The schematic cross sections of pMOSFETs splits are shown in Fig. 5-2. In this figure, Fig. 5-2(a) is the bulk-Si devices, and Fig. 5-2(b) is the SiGe on source/drain devices (uniaxial strain,) and Fig. 5-2(c) is the SiGe on substrate device. All pMOSFETs are <110> channel on (100) substrate. All these test devices have 14Å~ 13 Å EOT of SiON gate oxide and with different channel lengths.

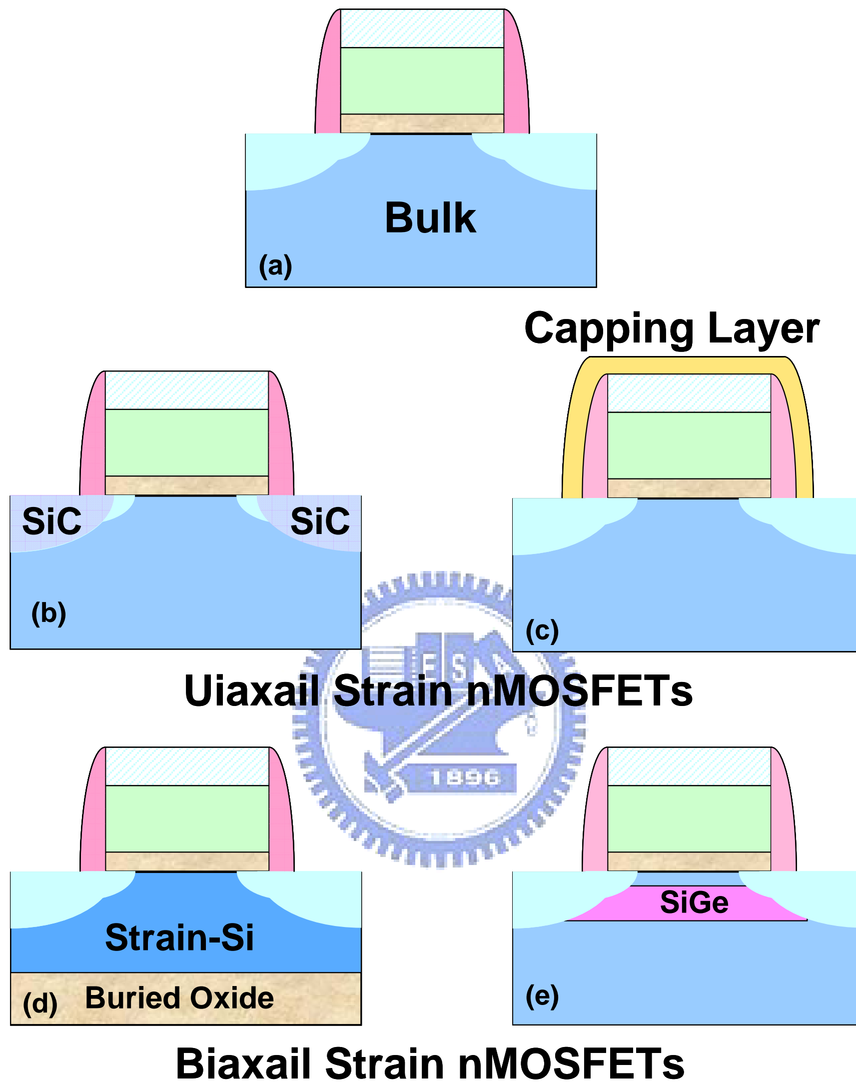


Fig. 5-1 (a) Bulk-Si device, (b) SiC on Source/Drain devices (uniaxial-strain), (c) CESL (contact etching stopping layer) capped device (uniaxial-strain), (d) SSDOI (strained silicon directly on insulator) device (biaxial-strain), and (e) strained-Si/SiGe on substrate device (biaxial-strained). All nMOSFETs are <100> channel on (100) substrate.

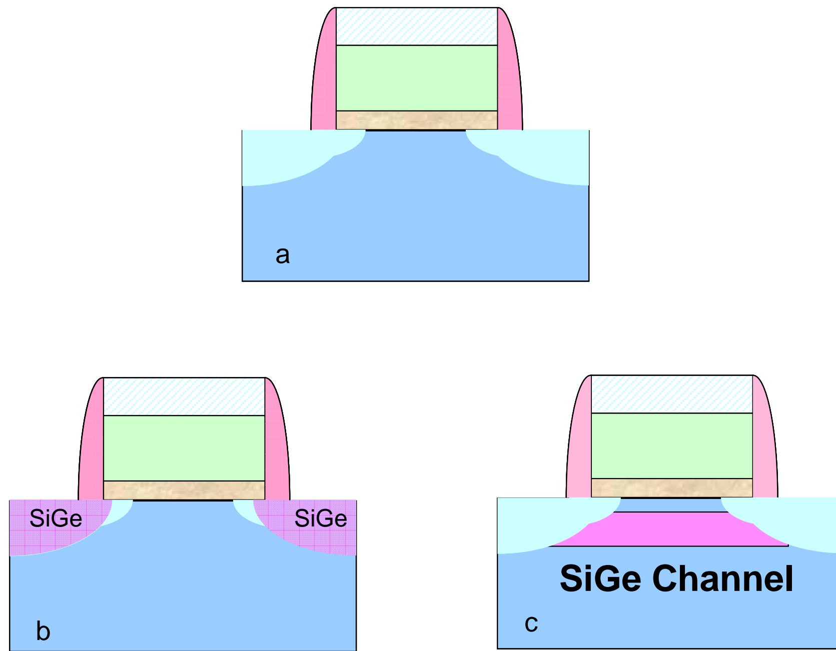


Fig. 5-2 (a) Bulk-Si device, (b) SiGe on source/drain devices (uniaxial strain), and (c) SiGe on substrate device. All pMOSFETs are <110> channel on (100) substrate.

5.3 Strained Device Physics

The carrier mobility in a semiconductor device is given by

$$\mu = \frac{q\tau}{m^*} \tag{5.1}$$

where $1/\tau$ is the scattering rate and m^* is the conductivity effective mass. Strain technologies enhance the speed of carrier transport by reducing the conductivity effective mass or the scattering rate. For electrons, both the modulations of effective mass and scattering events are generally accepted as the important reasons for mobility enhancement [34]. However, for holes, only the modulation of effective mass is due to band warping and carriers repopulation [35]. Although there has been much focus on reducing the in-plane effective mass to improve the mobility, increasing the out-of-plane effective mass for electrons and holes plays an important role to maintain the mobility enhancement at high vertical electric fields.

For electron transport in bulk Si at room temperature, the conduction band is composed of six degenerate valleys, as shown in Fig 5.3(a). These valleys have equal energy, as shown by $\Delta 6$ in Fig 5.3(b), which is because of the cubic symmetry for Si crystal-lattice. The effective mass for any direction is the reciprocal of the curvature of the electron energy function in that direction. Consequently, the effective mass of each ellipsoid is anisotropic, with the transverse mass (perpendicular to the axis) given by $m_t = 0.19\ m_o$ being significantly smaller than the longitudinal mass (parallel to the axis) given by $m_l = 0.98\ m_o$, where mo is the free electron mass.

For un-strained bulk Si, the effective conductivity mass for electrons, $m*$, is obtained by considering the contributions of the six degenerate valleys and is given by

$$m^* = \left[\frac{1}{6}\left(\frac{2}{ml}\right) + \left(\frac{4}{mt}\right)\right]^{-1} \tag{5.2}$$

For nMOSFETs on a (100) wafer, advantageous strain effect splits the original degenerate valleys into the four in-plane valleys ($\Delta 4$) and the two out-of-plane valleys ($\Delta 2$), as shown in Fig 5.3(b). The lower energy for the $\Delta 2$ valleys means that they are more stable and preferentially occupied by electrons. The electron mobility partly improves by decreased in-plane and increased out-of-plane $m*$ due to the lower effective mass of the $\Delta 2$ valleys, which results in more electrons with an in-plane transverse effective mass ($mt = 0.19\ mo$) and out-of-plane longitudinal mass ($ml = 0.98\ mo$). Furthermore, due to the conduction valleys splitting into two sets of energy levels, the probability of inter-valley phonon scattering events between the $\Delta 2$ and $\Delta 4$ valleys is decreased, which will also enlarge the electron mobility. Many types of strain schemes increase the electron mobility by increasing carrier-population on the $\Delta 2$ valley. In-plane biaxial, uniaxial tensile and out-of-plane uniaxial compressive strains are the some examples.

For holes, in the un-strained Si at room temperature, holes occupy the top two bands: the heavy and light hole bands. The constant energy surfaces of un-strained valence band and the x-y contours of the highest energy surface for holes in the MOSFET conduction plane are shown in Fig 5.4(a) [36]. With the application of strain technologies, the hole effective mass becomes highly anisotropic due to band warping, and the strained energy bands become mixtures of the original heavy, light, and split-off energy bands.

Thus, the light and heavy hole bands lose their meaning, and holes increasingly occupy the top band under strain effect due to the energy splitting. The constant energy surfaces of the valence band and x-y contours in the MOSFET conduction plane under strain effect are shown in Fig 5.4(b). It is important to achieve higher mobility for holes by lowering the in-plane effective conductivity mass of the top energy band. In addition to a lower in-plane mass, a high density-of-states on the top energy band and enough band splitting to populate the top energy band are also required to boost the hole mobility. Moreover, when the top-most occupied energy band has a lower out-of-plane mass in comparison of the second-top occupied energy band, the energy splitting will be reduced with surface confinement. Fig 5.5 shows the energy-level shift and represents the top band with larger out-of-plane effective mass under application of strain technologies. The top band will have a smaller energy shift because it is confined by uniaxial strain, and, as a result, the strain-induced band splitting ($E_{top} - E_{bottom}$) will increase under application of uniaxail strain technologies.

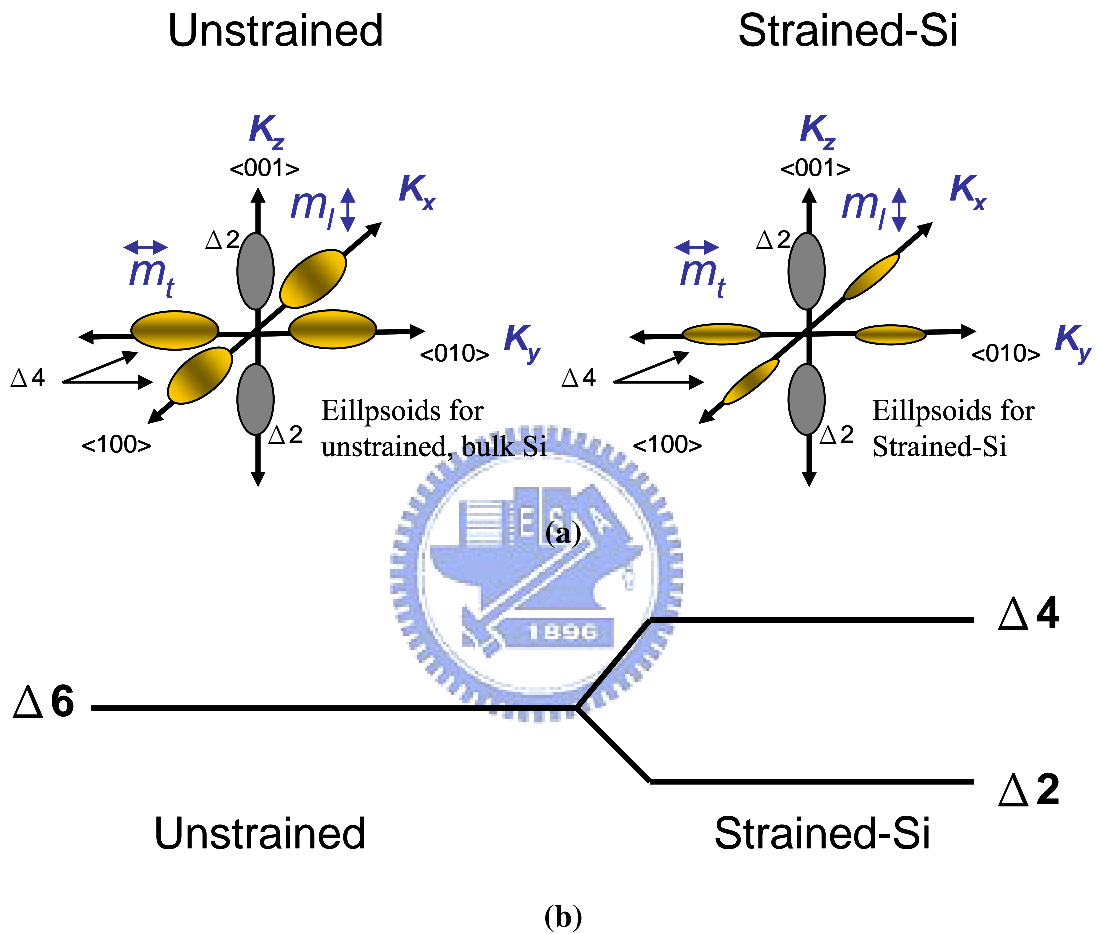


Fig. 5.3 (a) Ellipsoids of constant electron energy in reciprocal ("k") space. (b) Energy splitting between the Δ_2 (2-fold degenerate) and Δ_4 (4-fold degenerate) conduction bands for strained silicon devices and bulk si devices.

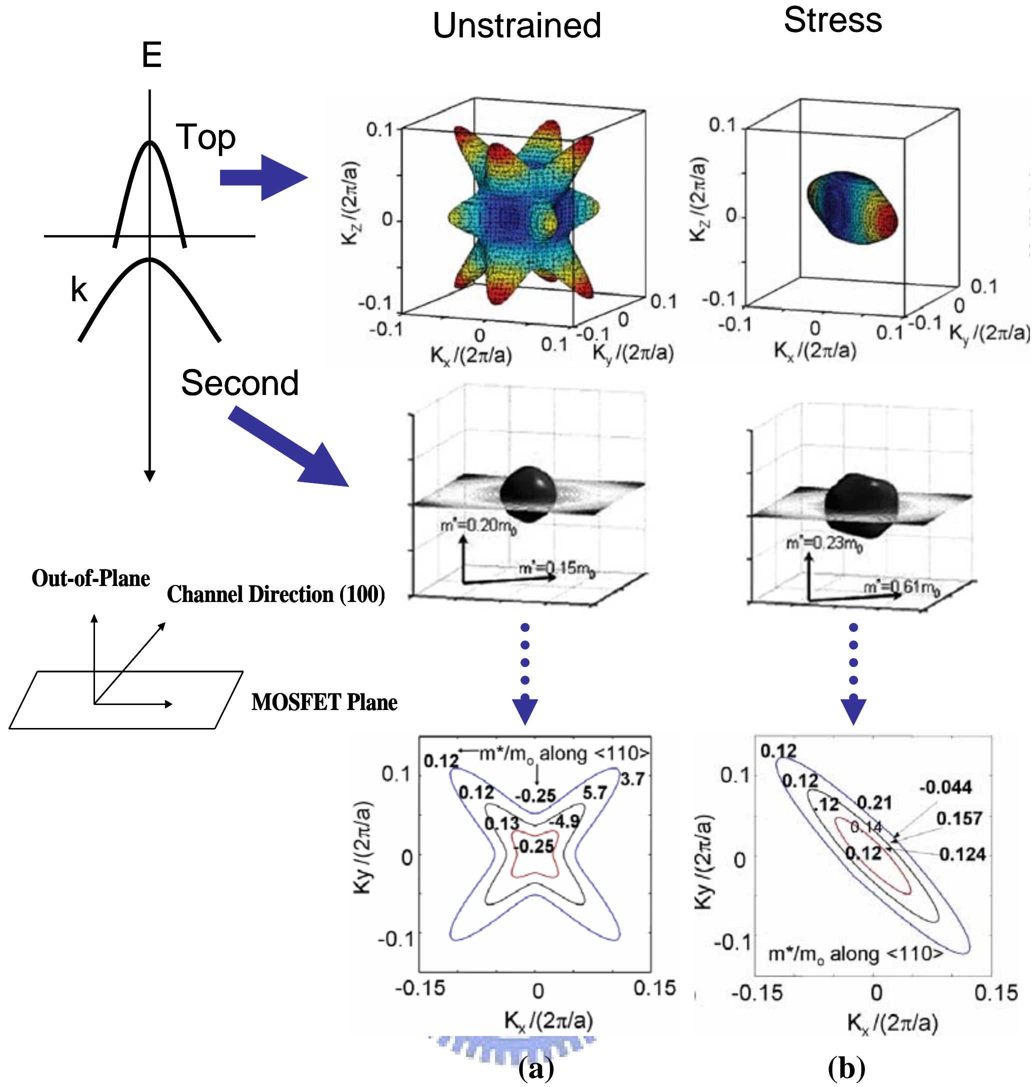
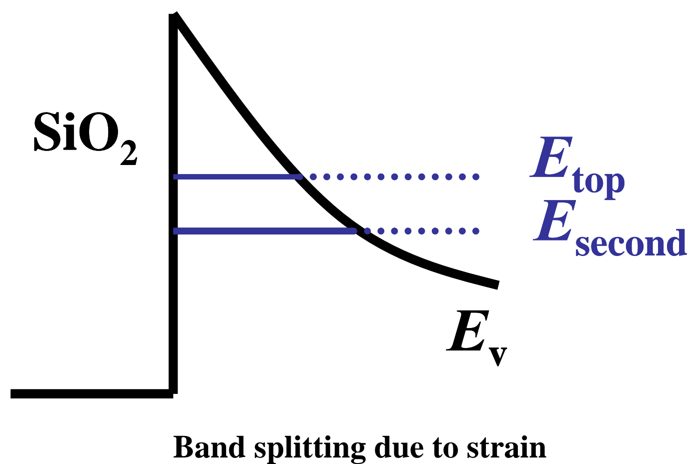


Fig 5.4 Hole constant energy surfaces obtained from six band kp calculations for common types of stresses: (a) unstressed, (b) compression stress on (100) wafer [35]-[36].



Band splitting due to strain

Fig. 5.5 Simplified schematic of valence-band splitting of strained silicon in inverse region. [36].

5.4 The Analysis of Reliability in Strained nMOSFETs

Fig. 5.6 shows the Ion-Ioff characteristics of all the strained splits and control nMOSFETs[37]. We may categorize all the splits into two groups. The first group is SiGe on substrate devices and CESL capping layer devices with excellent performance up to 34% and 30%, respectively, in comparison with that of bulk devices at the same value of I_{off} for each device. The other group is SiC on S/D devices and SSOI devices, which exhibit good performance around 15% by comparing to bulk devices in the same value of I_{off} for each device.

In order to characterize the hot-carrier effect for those devices, we perform the I_BV_{GS} and impact-ionization rates (I_B/I_D) measurement, as shown in Fig. 5-7. We observe that SiC on S/D, SSOI, and CESL devices, shows comparable values of I_B and impact-ionization rates to each other. In addition to those devices, SiGe on substrate devices have higher values of them, but SSOI devices own lower values of them, which means that SiGe on substrate device suffers from more serious hot-carrier effect, but SSOI devices do less with comparing to others.

Next the hot carrier and FN stresses are employed on uniaxail and biaxial strained nMOSFETs, respectively, to investigate the stress mechanism deepened on time, as shown in Fig. 5-8 for uniaxial devices and Fig. 5-9 for biaxial devices. Fig. 5-8 (a) is the uniaxial devices under HC stress, and Fig. 5-8 (b) is the biaxial devices under FN stress. We found that SiC on S/D devices exhibit worse degradation than CESL capping layer devices no matter after which stress case. It is due to the defects on the interface between SiC and Si for SiC on S/D devices. For biaxial strained nMOSFETs, SiGe on substrate devices have much worse degradation than SSOI devices after HC stress, which may be due to the channel interface damaged by Ge

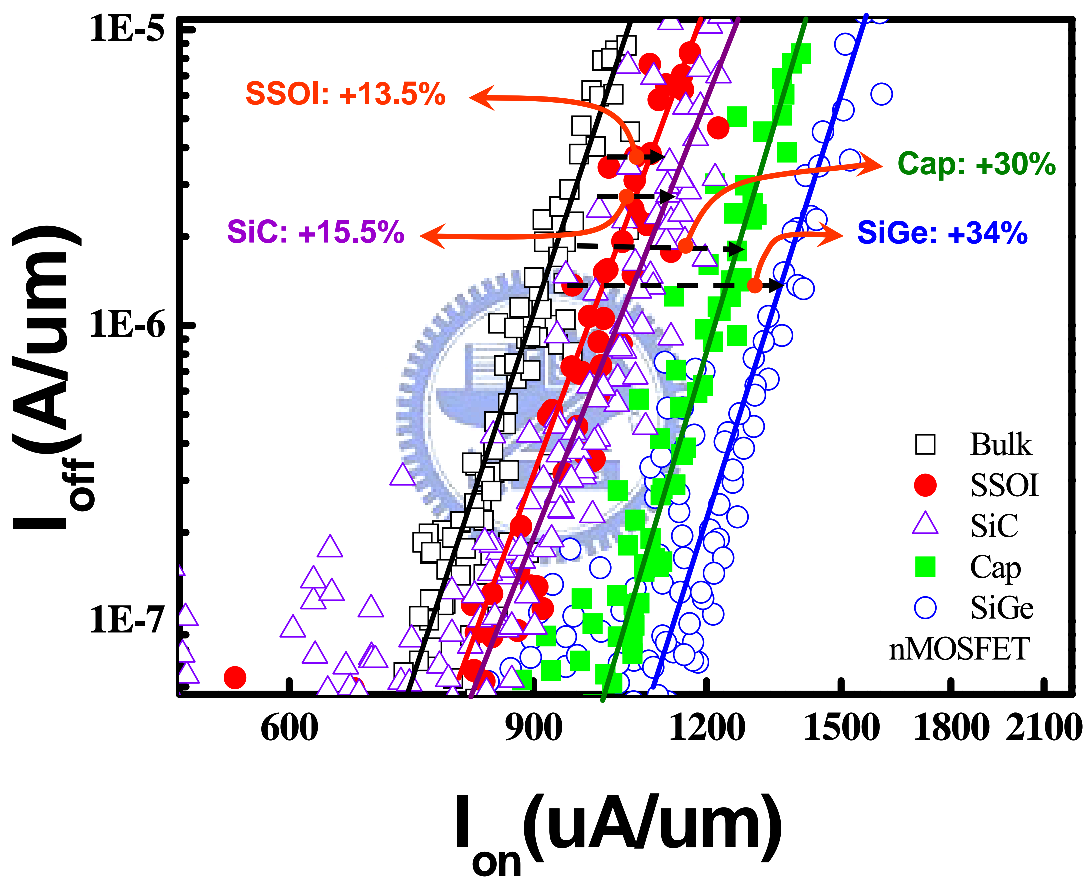


Fig. 5-6 The Ion-Ioff characteristics of all the strained splits and control nMOSFETs.

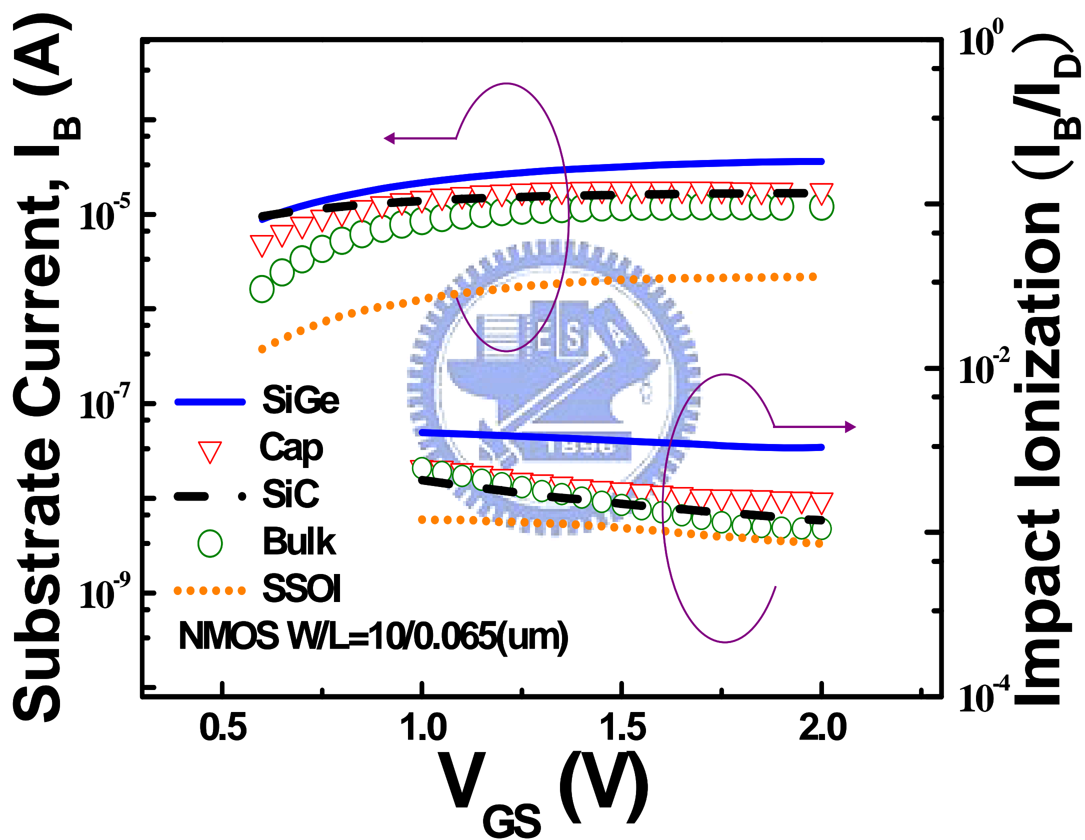


Fig. 5-7 The I_B-V_{GS} curves and impact ionization rates of all the strained splits and control nMOSFETs.

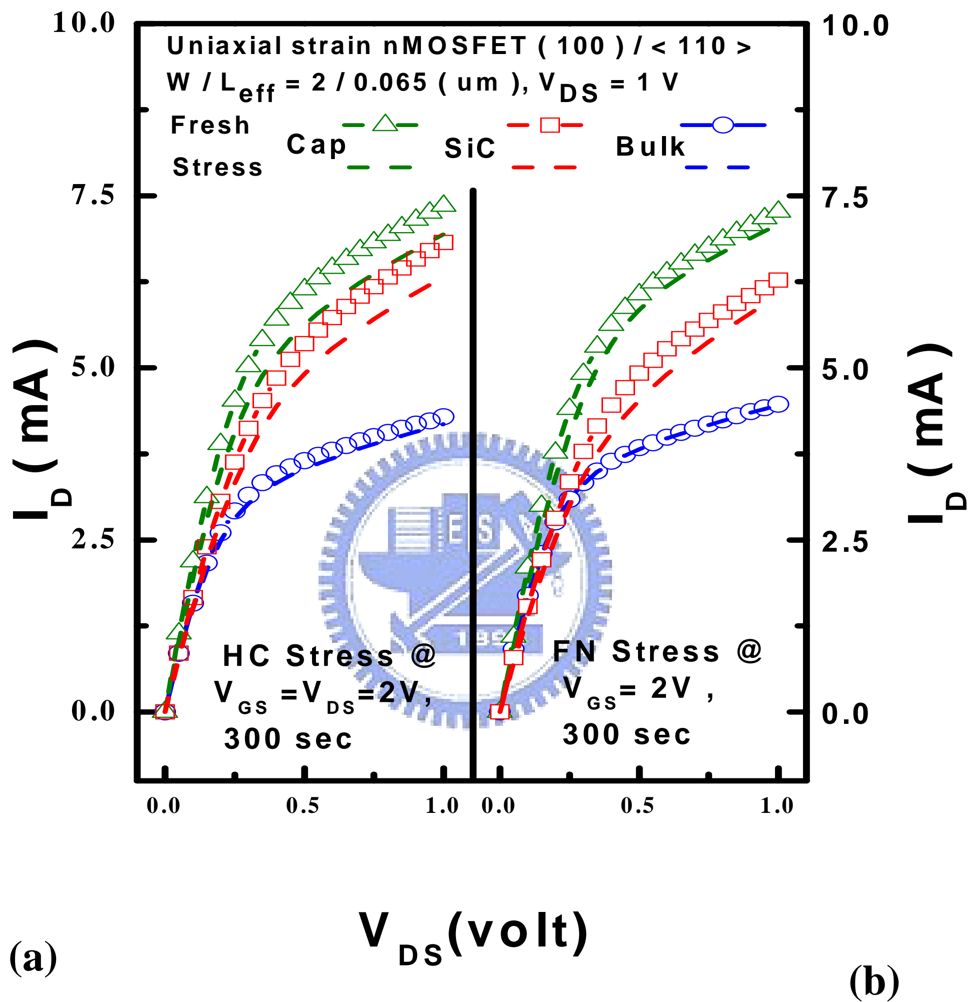


Fig. 5-8 The I_D degradation behaviors of uniaxial strained nMOSFETs after (a) FN and (b) HC stresses.

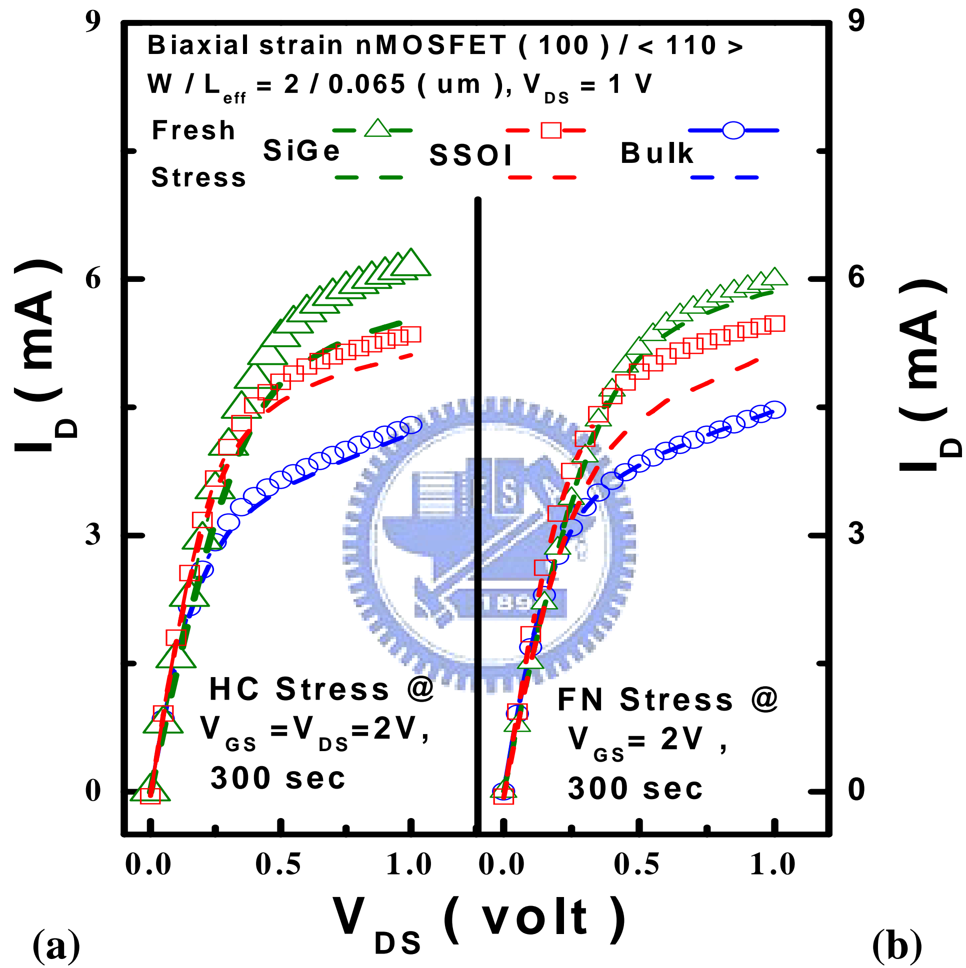


Fig. 5-9 The I_D degradation behaviors of biaxial strained nMOSFETs after (a) FN and (b) HC stresses.

out-diffusion. However, on the contrary, SSOI devices perform much worse degradation than SiGe on substrate devices after FN stress, which may be due to the channel interface defects induced by the process.

In order to realize strained nMOSFETs reliability, we take advantage of the charge pumping method, which was presented in the experimental setup paragraph in chapter 2 previously, the sophisticated reliability evaluation technique, low leakage charge pumping (CP) - *incremental frequency charge pumping method* has been employed, which was also described in Chapter 2. The results are shown in Fig. 5-10 for the case after HC stress and Fig. 5. 11 for the case after FN stress. Fig. 5-10 shows that, after the HC stress, SiGe on substrate devices exhibit the highest value of I_{CP} at 1MHz, and SiC on S/D devices reveal the second high value of I_{CP}. On the other hand, SSOI and CSEL capping layer devices have the lower values of I_{CP}. Thus, based on the measured result, SSOI and CESL capping layer devices have better immunities for hot carrier effect than SiGe on substrate devices and SiC on S/D devices. Furthermore Fig. 5-11 demonstrates that, after FN stress, SSOI devices shows the highest value in comparison of other devices, which points out that SSOI devices suffer most channel-interface damage.

As a result, although SSOI devices exhibit good hot-carrier immunity, their channel-interface quality will be critical due to the higher value of I_{CP} after FN stress. Next, for SiC on S/D devices, the defects on the interface between Si and SiC cause higher values after HC or FN stress, which may be a significant issue to improve their reliability. Moreover, for SiGe on substrate devices, although they have a great enhancement on the drive current as shown in Fig. 5-6, they encounter serious Ge-out-diffusion problems, which make their reliability not appreciated. CESL capping layer devices may be a better choice in terms of performance and reliability.

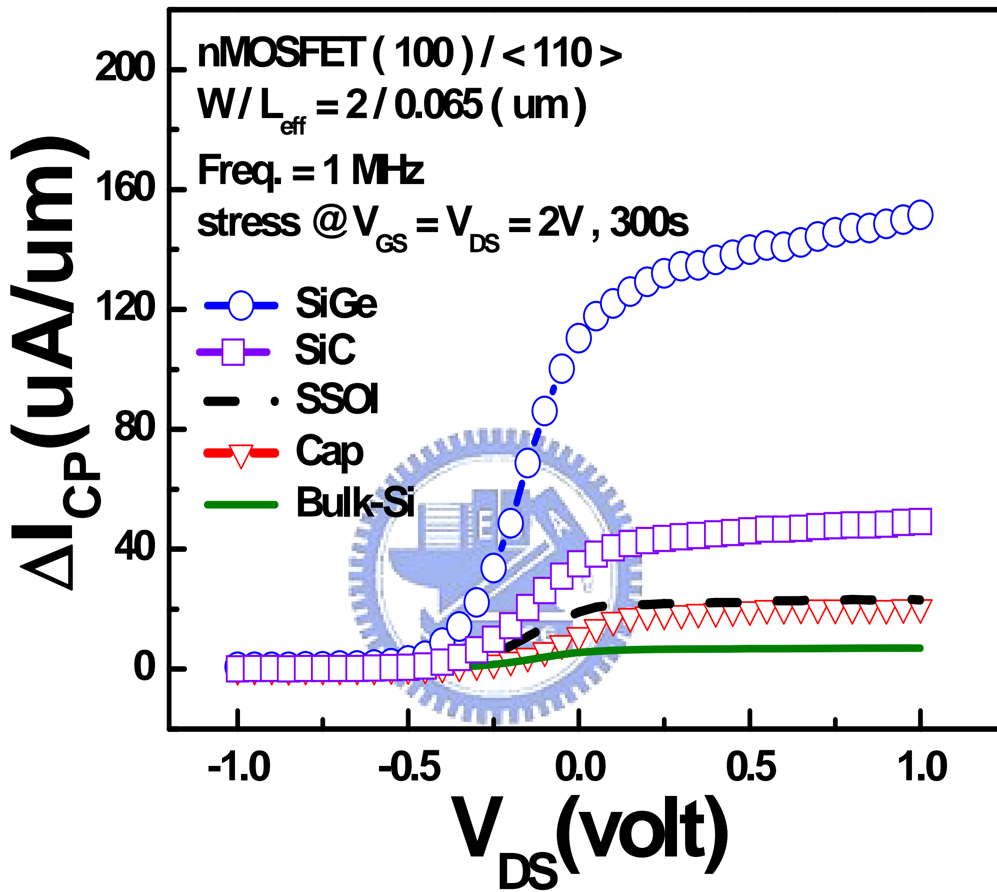


Fig. 5-10 The charge pumping current curves of strained splits and control nMOSFETs after Hot carrier stress.

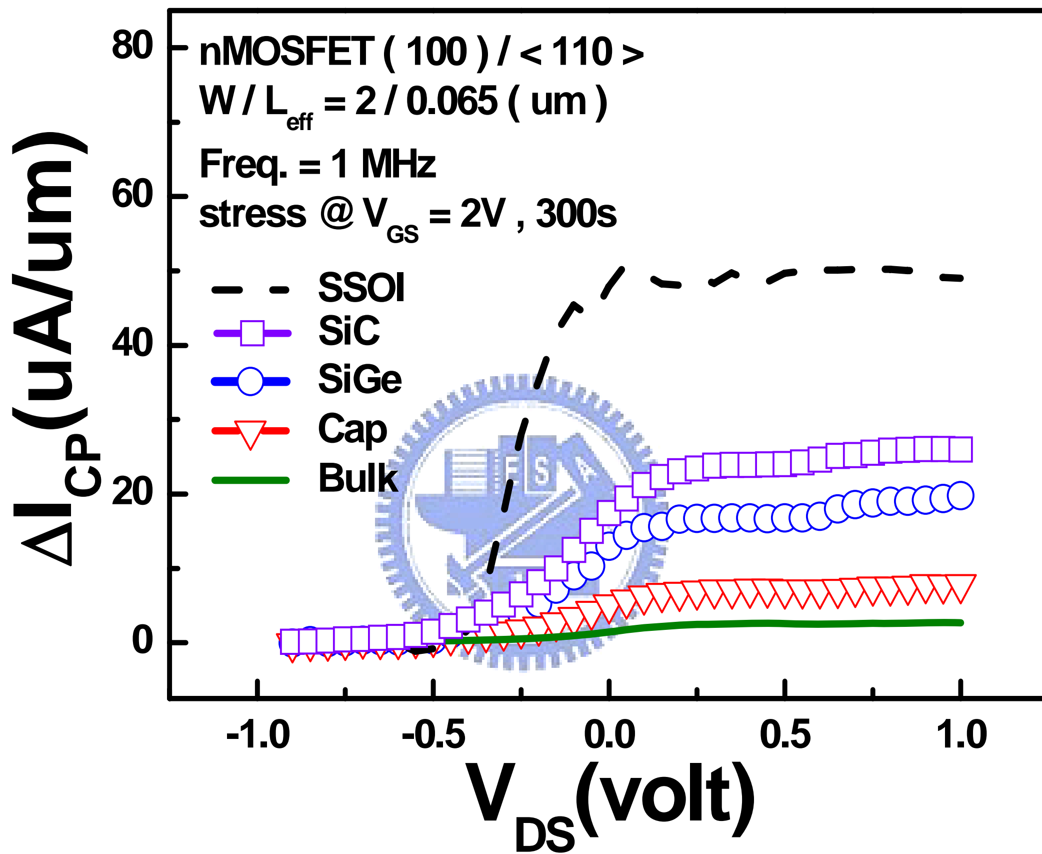
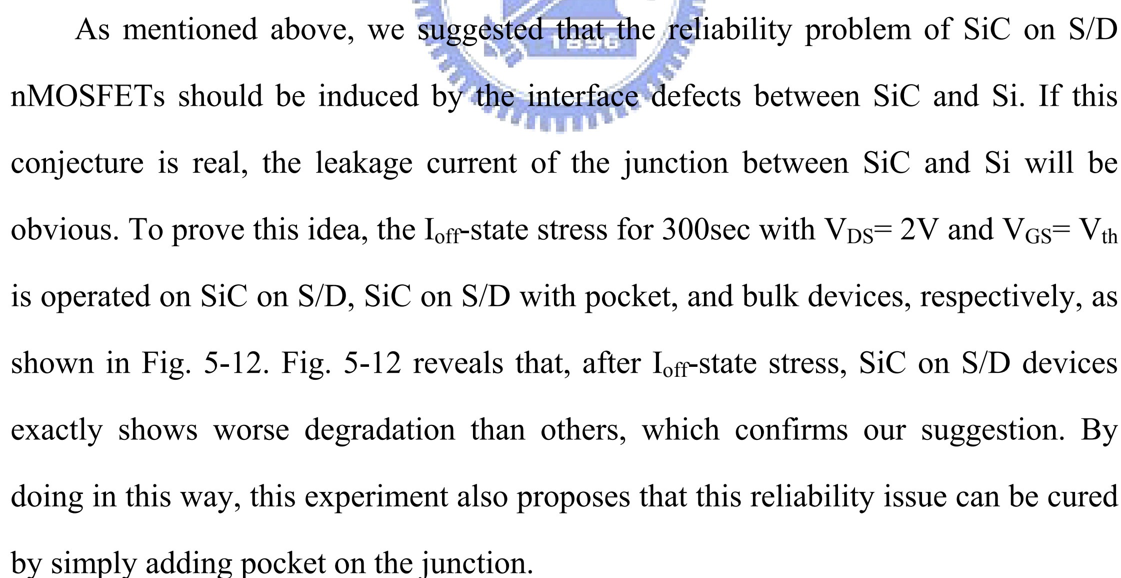


Fig. 5-11 The charge pumping current curves of strained splits and control nMOSFETs after Hot carrier stress.

		Bulk	Biaxial		Uniaxial	
			SiGe	SSOI	SiC	Cap
FN	$\triangle I_{cp}$(uA/um)	2.73	19.5	**49.78**	**24.5**	7.33
	$\triangle ID_{on}$(%)	0.22	2.39	**6**	**3.16**	2.51
HC	$\triangle I_{cp}$(uA/um)	8.12	**151.7**	26	**50.7**	20.8
	$\triangle ID_{on}$(%)	2.56	**10.15**	4.48	**7.2**	5.51

Table 5-1 The summary of the degradation of all strained splits and control nMOSFETs after FN and HC stresses in terms of charge pumping current and $I_{D,\,on}$.

In Table 5-1, we categorize these four devices into two groups, biaxial devices and uniaxial devices, and summarize some observations as followed: (1) the degradation is more significant for biaxial devices than that for uniaxial devices, which will be reasonable because the biaxial-strained is a two-dimensional strain and therefore, poses much larger stress to the devices. However, SSOI seems to modify this drawback for biaxial devices if the channel interface quality can be taken care with. (2) From another point of view, these four kinds of devices can be divided into two groups dependent on the level of degradation. In other words, SiGe on substrate and SiC on S/D devices will be the first group, and the others will be the second group because, no matter after which stress, the first group perform much degraded than the second group. (3) By comparing each device individually, we found that SiGe on substrate devices have the worst reliability, and the second worst will be SiC on S/D devices, the third are SSOI devices, and the last are CESL capping layer devices.



As mentioned above, we suggested that the reliability problem of SiC on S/D nMOSFETs should be induced by the interface defects between SiC and Si. If this conjecture is real, the leakage current of the junction between SiC and Si will be obvious. To prove this idea, the I_{off}-state stress for 300sec with V_{DS}= 2V and V_{GS}= V_{th} is operated on SiC on S/D, SiC on S/D with pocket, and bulk devices, respectively, as shown in Fig. 5-12. Fig. 5-12 reveals that, after I_{off}-state stress, SiC on S/D devices exactly shows worse degradation than others, which confirms our suggestion. By doing in this way, this experiment also proposes that this reliability issue can be cured by simply adding pocket on the junction.

To define where the damaged positions are, β DC-IV and its lateral profiling technique will be implemented for strained nMOSFETs after HC and FN stress, respectively. Fig. 5-13 demonstrates the experimental results of β DC-IV

measurement for strained nMOSFETs after FN stress, and the calculated results of the interface-traps lateral-profiling based on Fig. 5-13 are also given in Fig. 5-14. Fig. 5-14 (a) shows that SSOI devices have the worst degradation after FN stress, and we observe that the region near channel exhibits high DC-IV current, which means there are obvious interface traps existing in this region, and this result matches to our proposal above. Moreover, Fig. 5-14 (b), the enlarged plot of the dash area of Fig. 5-14(b) shows that SiC on S/D devices are damaged much in this region near the drain edge, which can be imputed to the defects near the interface between Si and SiC.

Next, the experimental results of β DC-IV measurement for strained nMOSFETs after the HC stress and its calculated lateral profiling are also revealed in Fig. 5-15 and Fig. 5-16, respectively. Fig. 5-16(a) shows that SiGe on substrate devices exhibits more degradation after HC stress, and we observe that there are three main damaged regions on interface for SiGe on substrate devices after HC stress. They are the areas around the channel, the drain side, and the gate edge, and, especially, the area around the gate edge is damaged most. This phenomenon is caused by the Ge-out diffusion effect. Fig. 5-16 (b) is the enlarged diagram of the dash area in Fig. 5-16 (a). It shows that SSOI and CESL capping layer devices have good immunity to hot carrier stress, but, on the other hand, SiC on S/D devices have a bad reliability property under hot carrier stress.

As a result, by using this interface-trap lateral-profiling technique with high resolution, for the first time, we have interpreted where and how the regions on interface for strained nMOSFETs are damaged after HC and FN stress, respectively. We conclude that, SiGe on substrate devices are damaged on the most regions, including the regions around channel, junction edge, and gate edge, after HC stress,

which is caused by the Ge-out diffusion effect. SSOI devices are damaged on the region around channel after FN stress, which means the channel interface quality for SSOI devices has to be improved. Moreover, for SiC on S/D devices, the regions around junction and gate edges are damaged obviously, which is due to the defects on junction. Finally, the CSEL capping layer devices seem to be a good candidate for strained silicon technologies, because of their less damaged no matter after HC or FN stress. All those results match with the results given from the analysis of charge-pumping measurement.

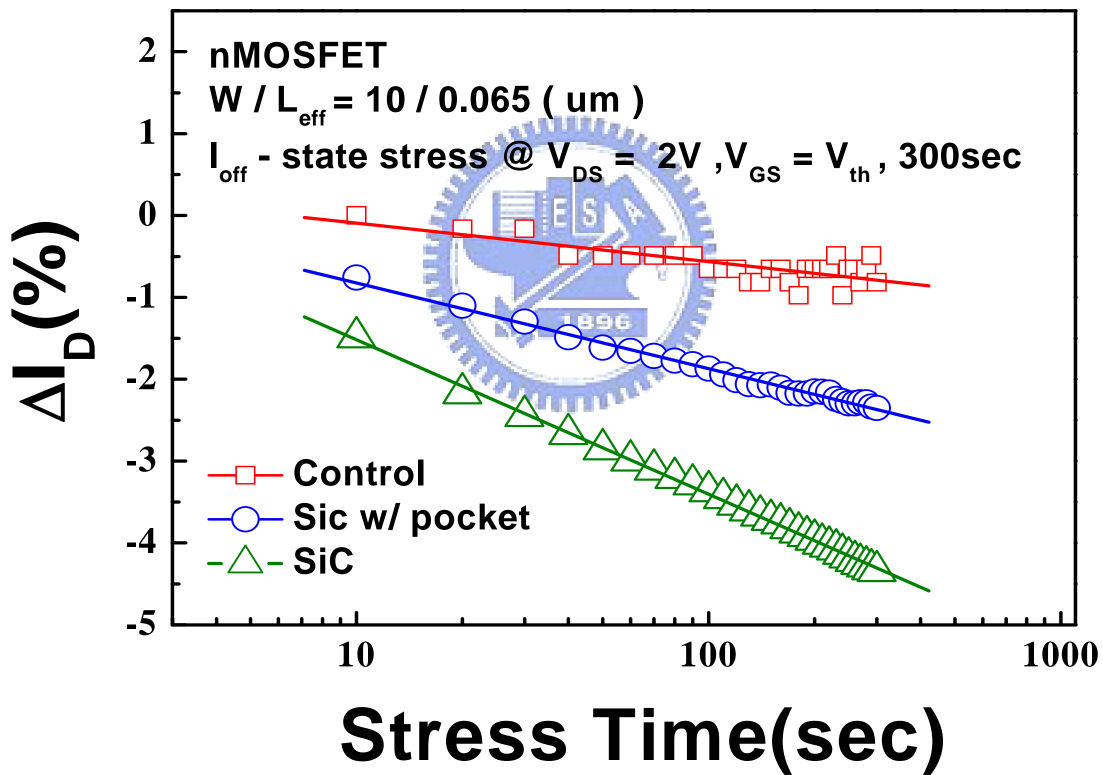


Fig. 5-12 The I_D degradation behaviors of SiC, SiC w/ pocket, and control nMOSFETs after I_{off}-state stress.

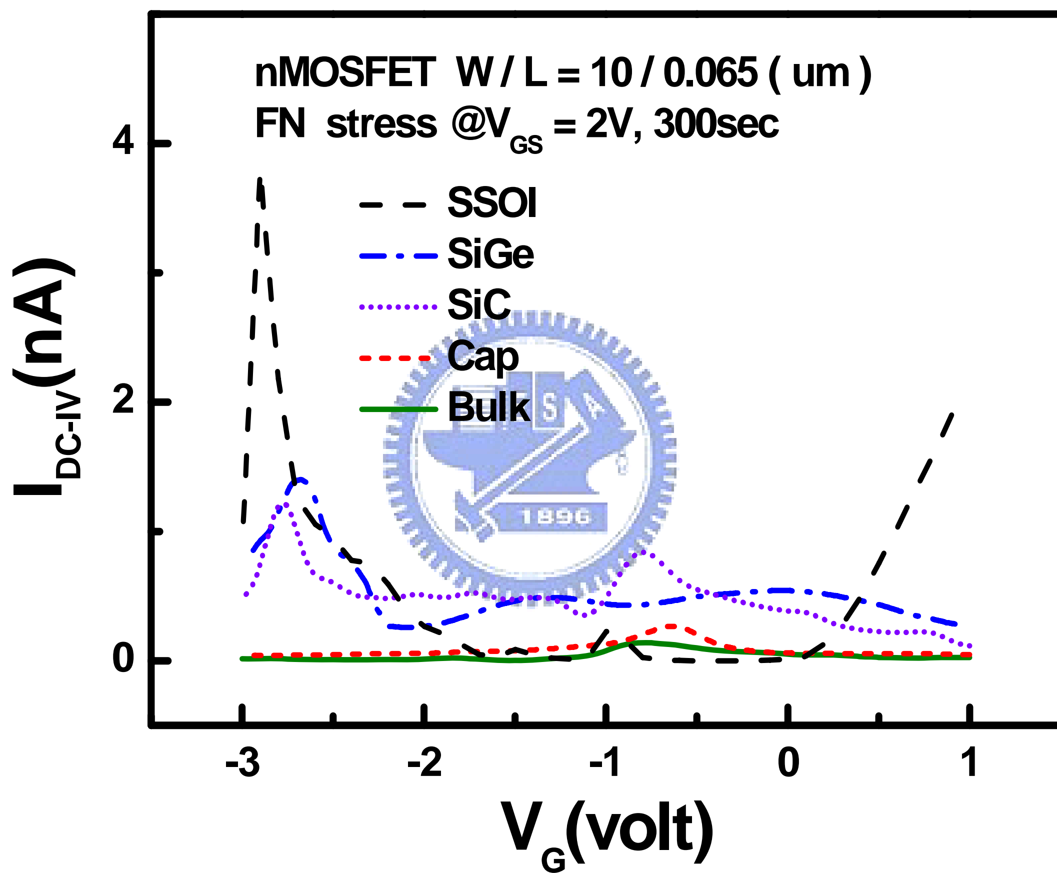


Fig. 5-13 The experimental results of β DC-IV measurement for strained nMOSFETs after FN stress.

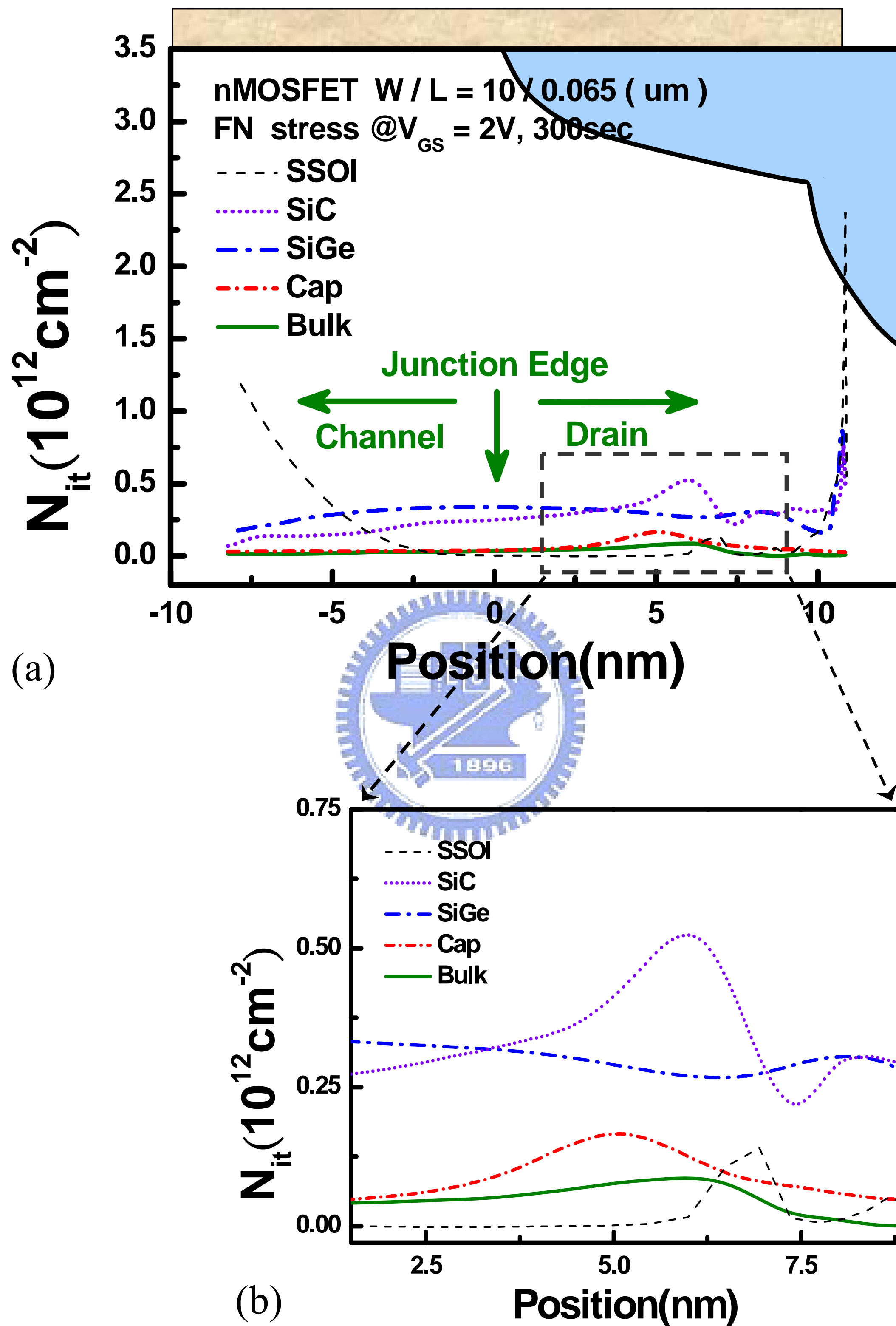


Fig. 5-14 The calculated results of the interface-traps lateral-profiling.

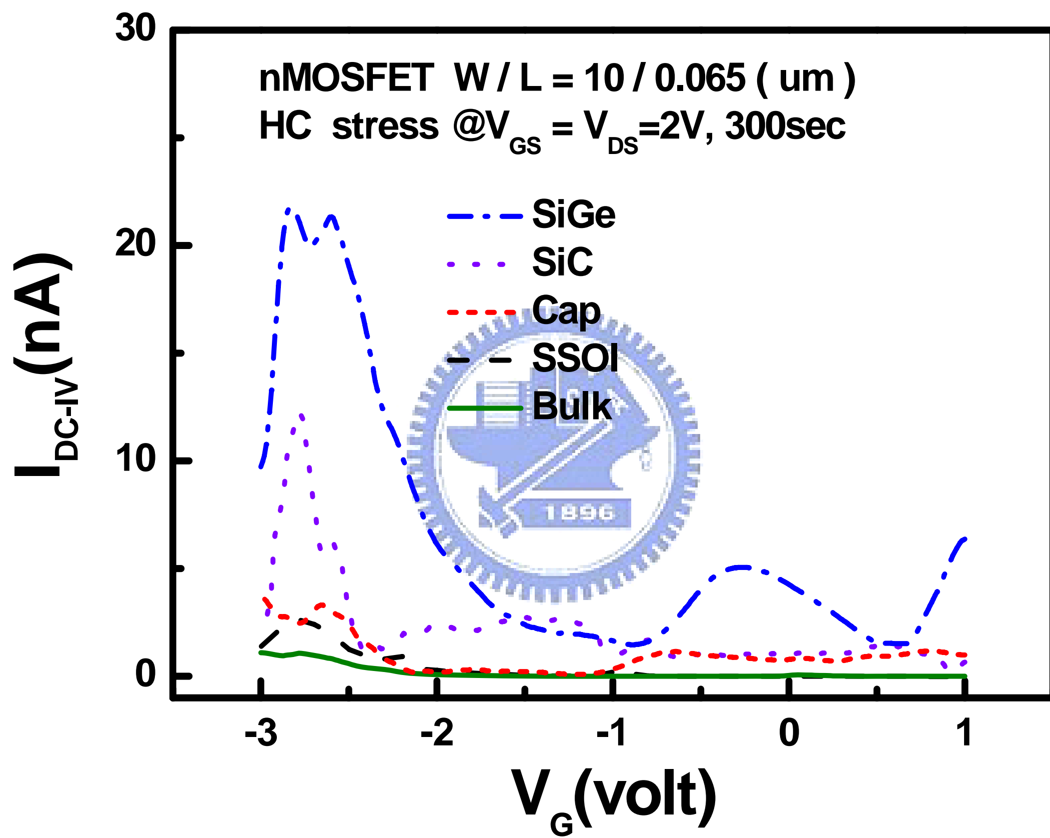
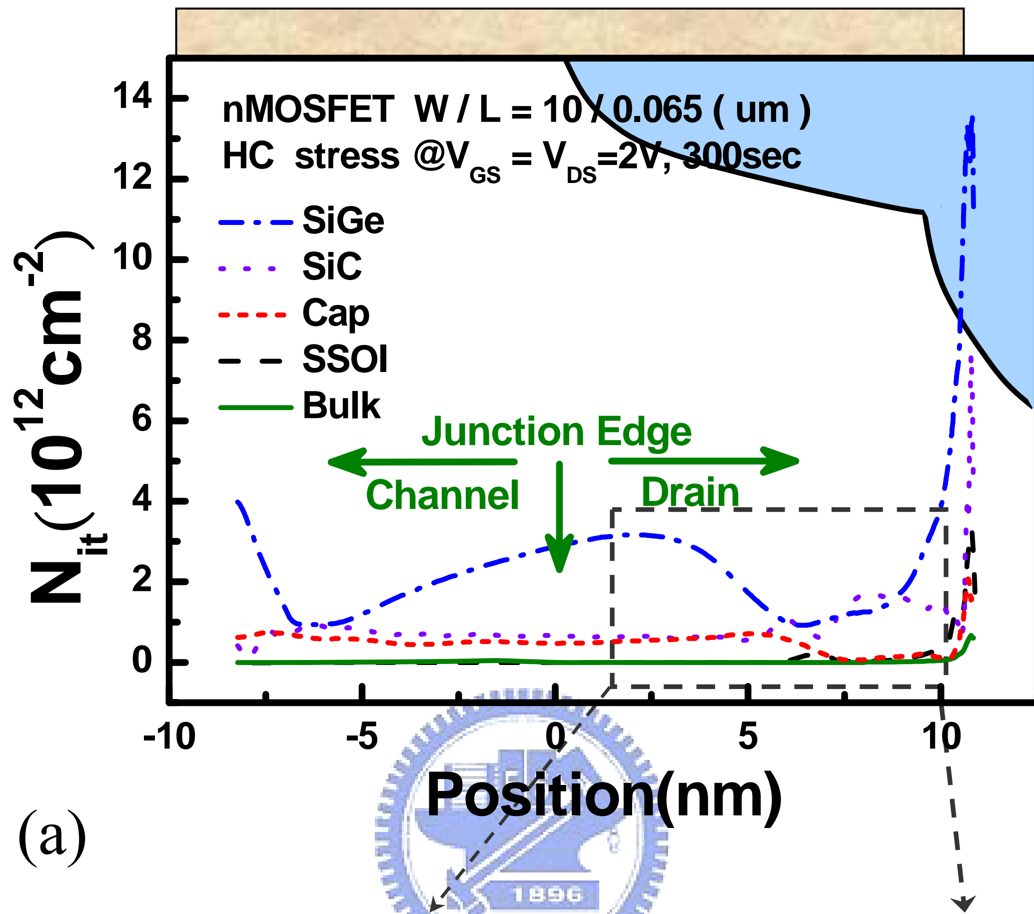
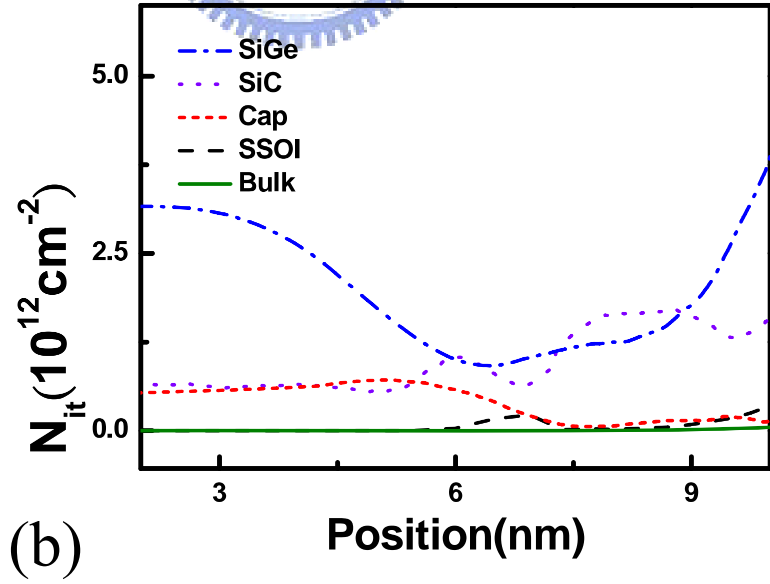


Fig. 5-15 The experimental results of β DC-IV measurement for strained nMOSFETs after HC stress.



(a)



(b)

Fig. 5-16 The calculated results of the interface-traps lateral-profiling.

5.5 The Analysis of Reliability in Strained pMOSFETs

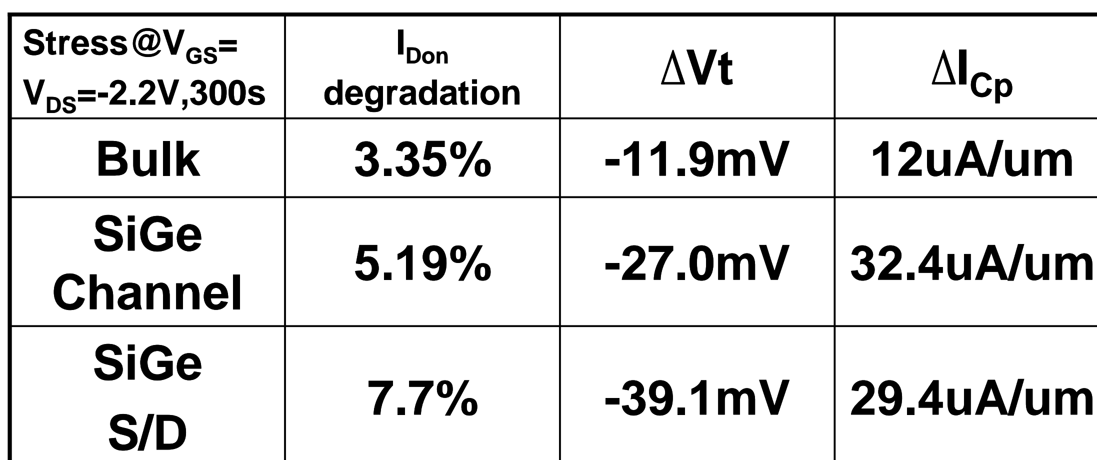
In this section, we will analyze the reliability of strained pMOSFETs, whose splits are shown in Fig. 5-2. They are the bulk, SiGe on channel (biaxial) and SiGe on S/D (uniaxail) devices, and all devices are <110>/(100) directions. The I_{on}-I_{off} characteristics of both the splits and control sample are given in Fig. 5-17[37]. We can find SiGe on S/D devices have higher drive current by comparing to SiGe on channel in the same value of I_{off}, which is because the stressor of SiGe on S/D devices is closer to channel than that of SiGe on channel devices. The closer the stressor is to the channel, the higher the effect of strain is. Hence, SiGe on S/D devices have higher performance than SiGe on channel devices.

Next, in order to describe the hot-carrier effect for those devices, the I_BV_{GS} and impact-ionization rates (I_B/I_D) measurement are measured in Fig. 5-18, and the I_D degradation for those devices after HC stress is also give in Fig. 5-19. We found that both the values of I_B and impact-ionization rates and I_D degradation for SiGe on S/D are larger than those for SiGe on channel and the control sample, which is because the larger the current enhancement is, the more the values of I_BV_{GS} and impact-ionization rates (I_B/I_D) are, and the more seriously the drain current is degraded.

Moreover, the results of charge pumping measurement for those devices after HC stress are employed in Fig. 5-20, and we can find that the value of charge pumping current for SiGe on channel device is a little larger than that of SiGe on S/D device. If we compare this result to the result of Fig. 5-19, a confliction is found. Why is the value of charge pumping current for SiGe on channel devices larger than that for SiGe on S/D, but the value of I_D degradation for the former smaller than that for the latter? Due to the misfit in a biaxial strain, SiGe on channel devises generate larger defects

than SiGe on S/D devices, which makes a higher charge pumping current for SiGe on channel devices. However, for SiGe channel devices, thin epi-layer is formed as the channel, which serves as a good quality $Si\text{-}SiO_2$ interface for carrier conduction, and hence the I_D degradation for SiGe channel devices will be reduced. Next, the results of charge pumping measurement for those devices after FN stress are given in Fig. 5-21. We found that all these devices have the same value of charge pumping current, which shows that the channel interface is not a critical issue for strained pMOSFETs.

As a result, based on the hot carrier and FN stress analyses, some conclusions are made: (1) SiGe on S/D devices have a better immunity for hot-carriers stress, but, due to its higher drive current, the I_D degradation is worse, which matches the results of the impact ionization rate. (2) SiGe channel devices exhibits a little more defects than SiGe on S/D devices, and this drawback can be compensated by the formation of a good quality epi-layer channel. (3) Both the devices have the good channel interface quality as the same to that for the control sample. Table 5-2 is the summary of these results.



Stress@V_{GS}= V_{DS}=-2.2V,300s	I_{Don} degradation	ΔVt	ΔI_{Cp}
Bulk	3.35%	-11.9mV	12uA/um
SiGe Channel	5.19%	-27.0mV	32.4uA/um
SiGe S/D	7.7%	-39.1mV	29.4uA/um

Table 5-2 Comparison of the values of ID degradation and charge pumping current increment for strained pMOSFETs and the control sample after HC stress.

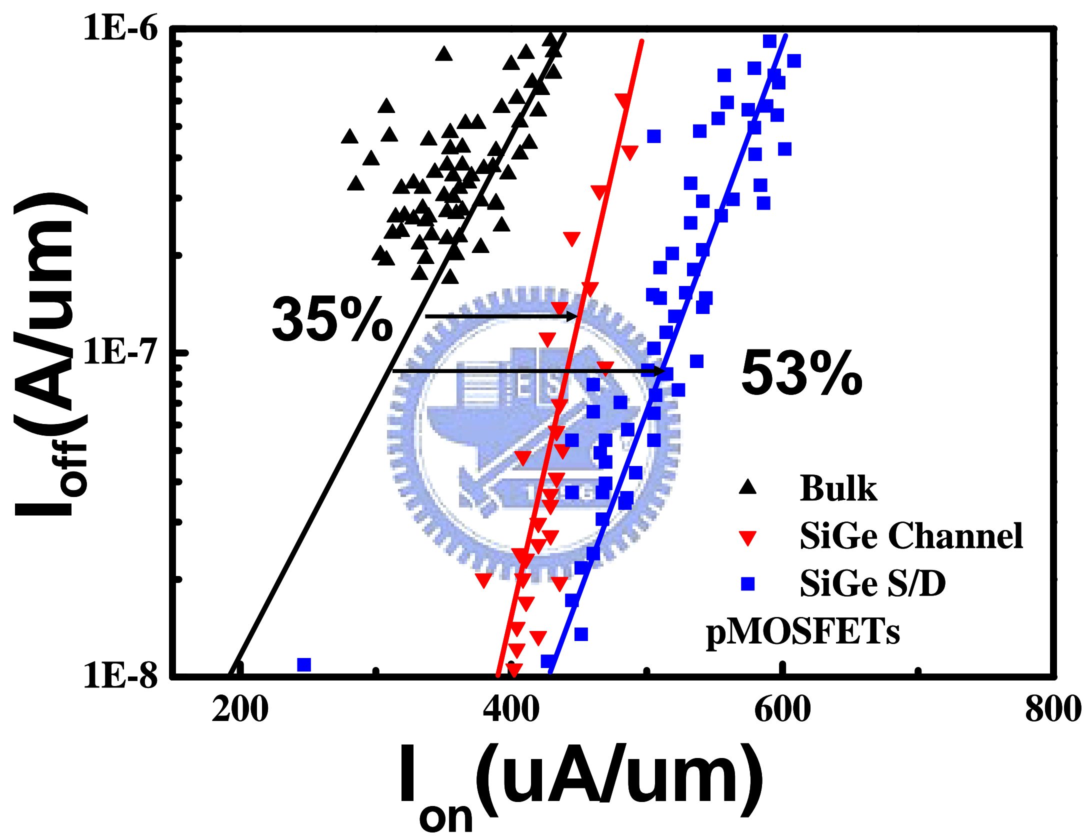


Fig. 5-17 The Ion-Ioff characteristics of all the strained splits and control nMOSFETs.[37]

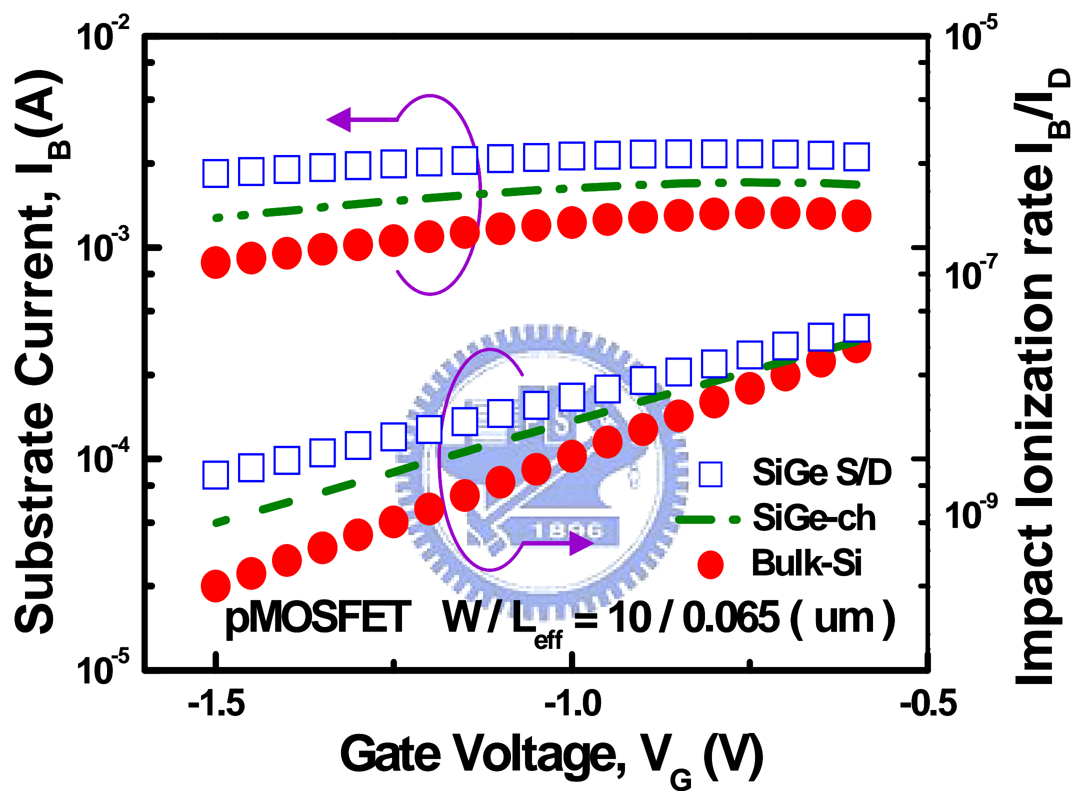


Fig. 5-18 The I_B-V_{GS} curves and impact ionization rates of all the strained splits and control pMOSFETs.

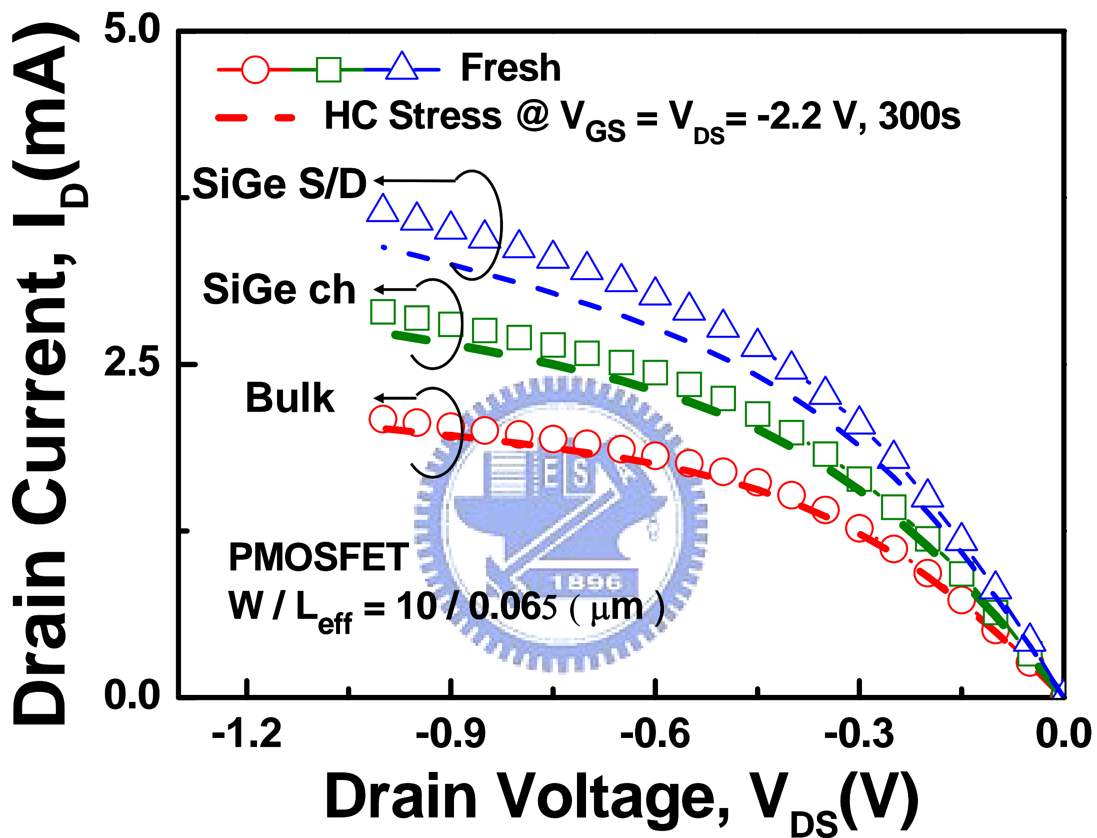


Fig. 5-19 The ID degradation for those pMOSFETs after HC stress.

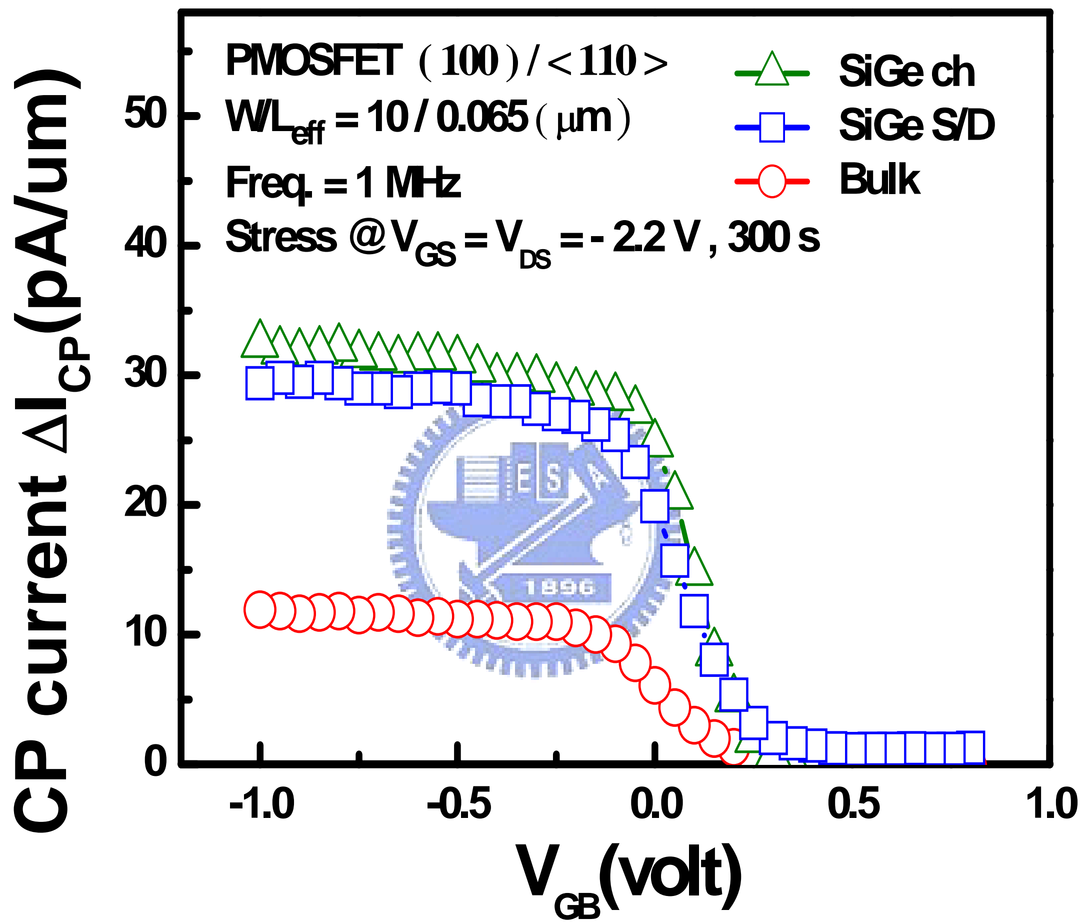


Fig. 5-20 The charge pumping current curves of strained splits and control pMOSFETs after HC stress.

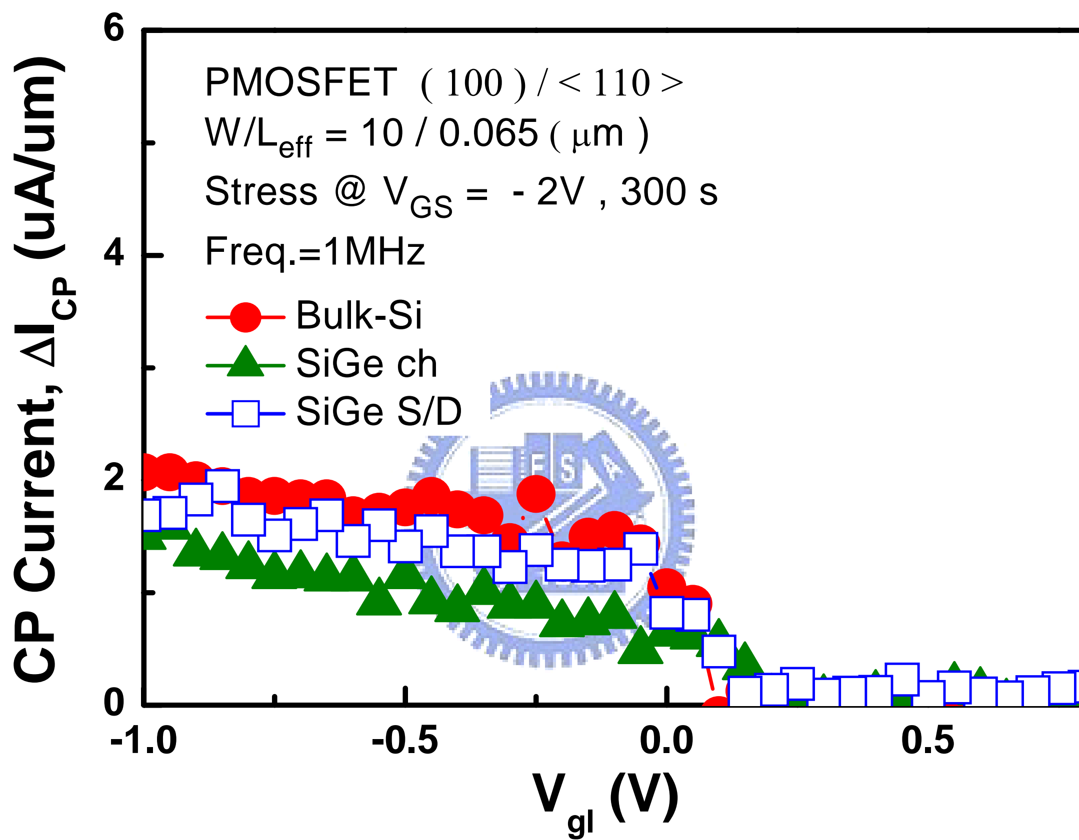


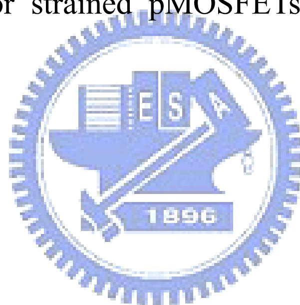
Fig. 5-21 The charge pumping current curves of strained splits and control pMOSFETs after FN stress.

5.6 The Analysis of NBTI Degradation in Strained pMOSFETs

Negative bias temperature instability (NBTI) reveals serious reliability problem in device scaling to nano technology since NBTI manifests itself as absolute drain current and trans-conductance decrease, and absolute threshold voltage increase for pMOSFETs at elevated temperatures[38]. Several models have been proposed to explain the mechanism of NBTI. In all of them, the most popular model accepted to explain the mechanism of NBTI is the electrochemical reaction model [39]. Fig 5-22 is a schematic diagram of the electrochemical reaction model. On the interface between Si and SiO_2 in MOSFETs, $S_i \equiv S_i - H$ is presented due to the surface preservation by high temperature annealing. This bonding is easy to be broken by introducing the h+ ions at the high temperature and field environment. As it is broken, dangling bonds ($S_i^{\bullet}$), hydrogen ions (H_i^{+}), and hydrogen atoms (H_i.) will be produced, which are believed to contribute the creation of interface and fixed oxide traps. As a result, those traps will enhance the tunneling current through the trap assisted tunneling mechanism, and limit the lifetime of devices.

In order to investigate the influence of NBTI to strained pMOSFETs, the analysis of temperature-dependent hot-carrier like NBTI stress and FN-like NBTI stress at 85^0C are performed, respectively. After stresses, β DC-IV is measured, and then the interface-traps lateral-profiling is implemented to characteristic where and how the interface is damaged. Fig. 5-23 is the experimental result of β DC-IV measurement for strained pMOSFETs and the control sample after FN-like NBTI stress, and the calculated result of interface traps lateral profiling based on Fig. 5-23 is shown in Fig. 5-24. On the other hand, Fig. 5-25 is the experimental result of β DC-IV measurement for strained pMOSFETs and the control sample after HC-like NBTI stress, and the calculated result of interface traps lateral profiling based on Fig. 5-25 is

shown in Fig. 5-26. Then we make the comparison of Fig. 5-24, the case after FN-like stress, and Fig. 5-26, the case after HC-like stress. First, no matter after which stress, SiGe on channel devices show worse properties than SiGe on S/D devices. Moreover, Fig. 5-26 points that, after FN-like stress, the main damaged region for SiGe on channel devices is the region around the drain side, and the main damaged region for the same devices after HC-like region is not only the region around the drain side but also the gate-edge. These results can be explained by the Ge-out diffusion from SiGe substrate at an elevated temperature, and additionally the defects induced by misfit dislocations in a biaxial strain assist Ge-out diffusion. These two factors further enhance the NBTI degradation for SiGe on channel devices. On the other hand, those results shows that SiGe on S/D devices have much better NBTI characteristic, which may be a good candidate for strained pMOSFETs in terms of performance and reliability.



5.7 Summary

In this chapter, we have analyzed the reliability issues for strained nMOSFETs and pMOSFETs, respectively.

In the front of this chapter, the reliability issues for strained nMOSFETs have been studied under HC and FN stresses, and the charge pumping measurement, the I_D degradation, and the interface-traps lateral-profiling based on DC-IV measurement have been implemented to characterize the properties of reliability for strained nMOSFETs. Based on these results, several conclusions include: (1) The degradation is more significant for biaxial devices than that for uniaxial devices. However, SSOI devices seem to modify this drawback for biaxial devices if the channel interface quality can be taken care with. (2) No matter after which stress, SiGe on substrate and

SiC on S/D devices perform much degraded than SSOI and CESL capping layer devices. (3) By comparing each device individually, SiGe on substrate devices have the worst reliability, and the second worst are SiC on S/D devices, the third are SSOI devices, and the last are CESL capping layer devices.

In the latter half of this chapter, the reliability issues for strained pMOSFETs have been studied under HC-like and FN-like NBTI stresses, respectively, and the similar measurements as those applied in strained nMOSFETs have been also performed. Some conclusions can be drawn: (1) SiGe on S/D devices have a better immunity for hot-carriers stress, but, due to its higher drive current, the I_D degradation is worse, which matches the results of the impact ionization rate. (2) SiGe channel devices owns a little more defects than SiGe on S/D devices, and this drawback can be compensated by the formation of a good quality epi-layer channel. (3) Both the devices have the good channel interface quality as the same to that for the control sample. (4) SiGe on S/D devices have much better NBTI properties than SiGe on channel devices which may be a good candidate for strained pMOSFETs in terms of performance and reliability. Table 5-2 is the summary of these results.

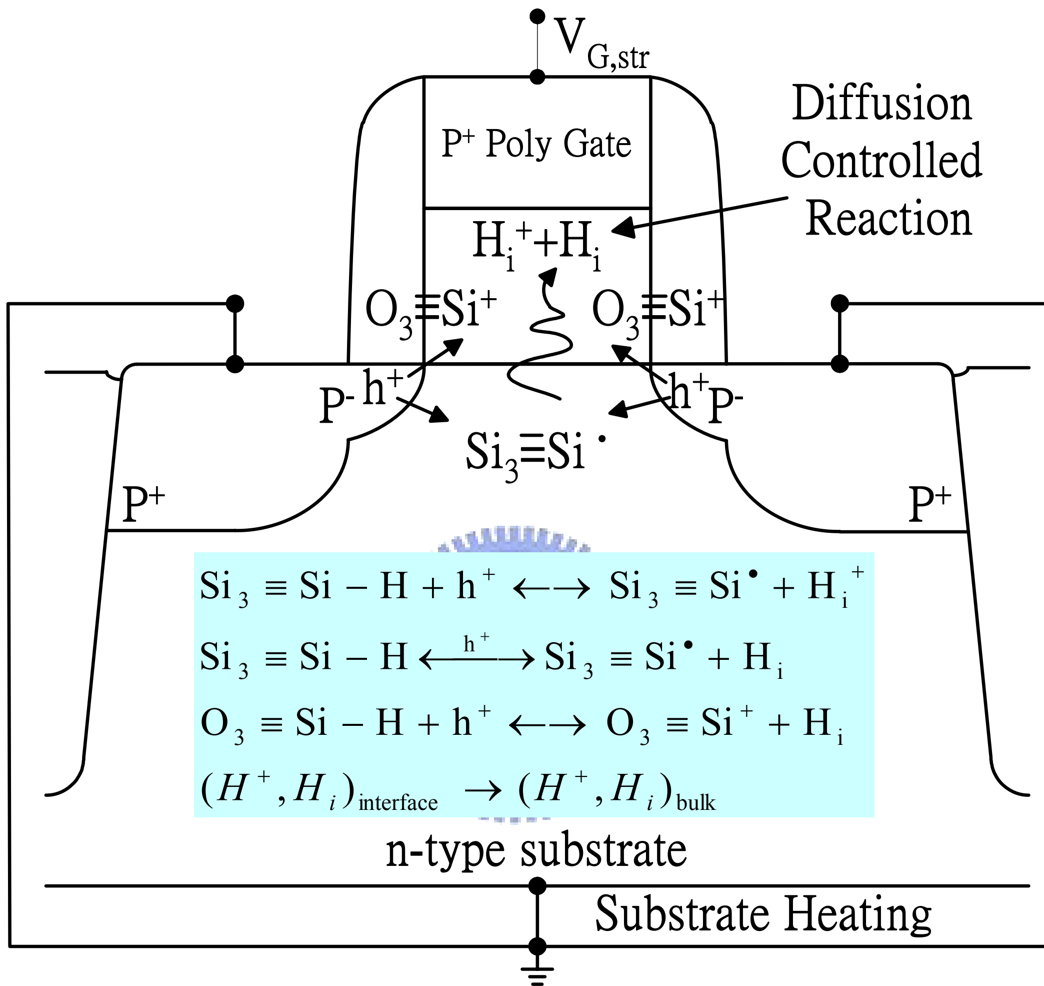


Fig 5-22 The schematic diagram of the electrochemical reaction model.

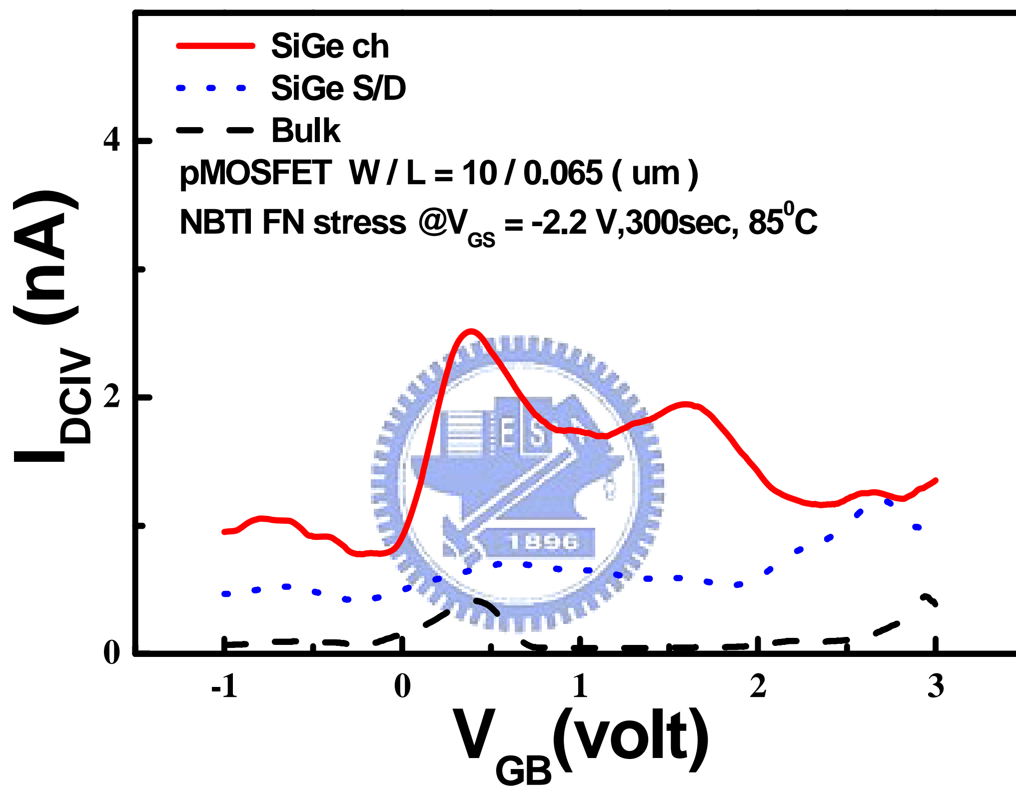


Fig 5-23 The experimental results of β DC-IV measurement for strained nMOSFETs after FN-like NBTI stress.

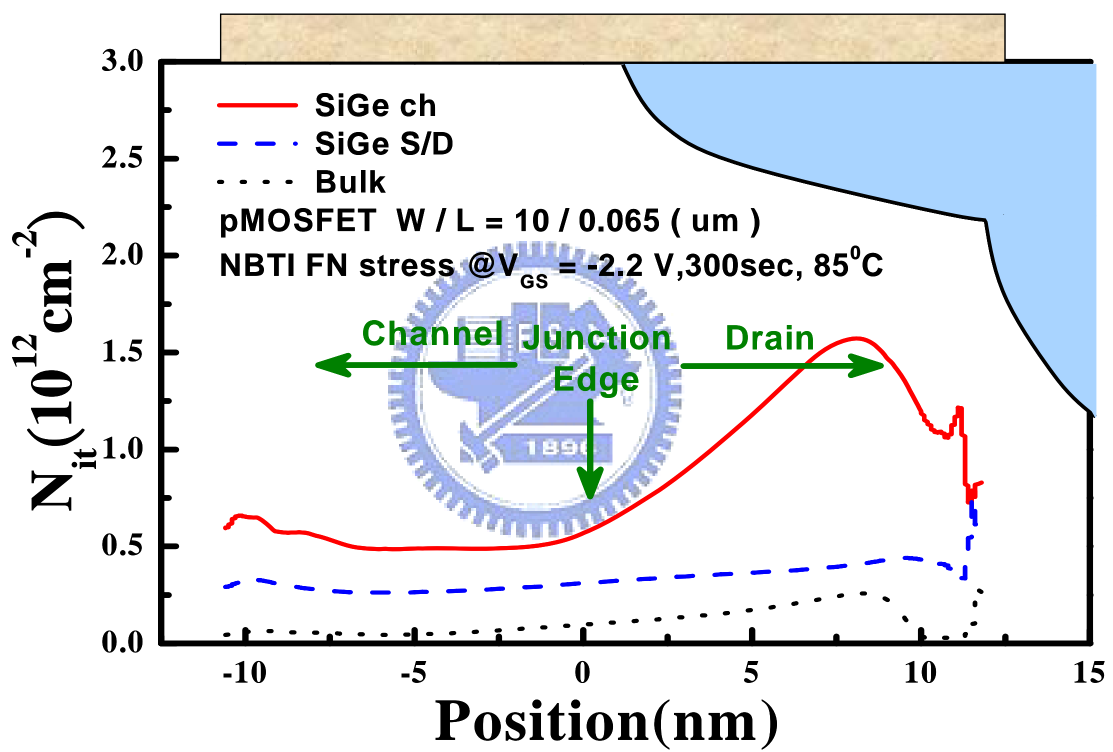


Fig. 5-24 The calculated results of the interface-traps lateral-profiling.

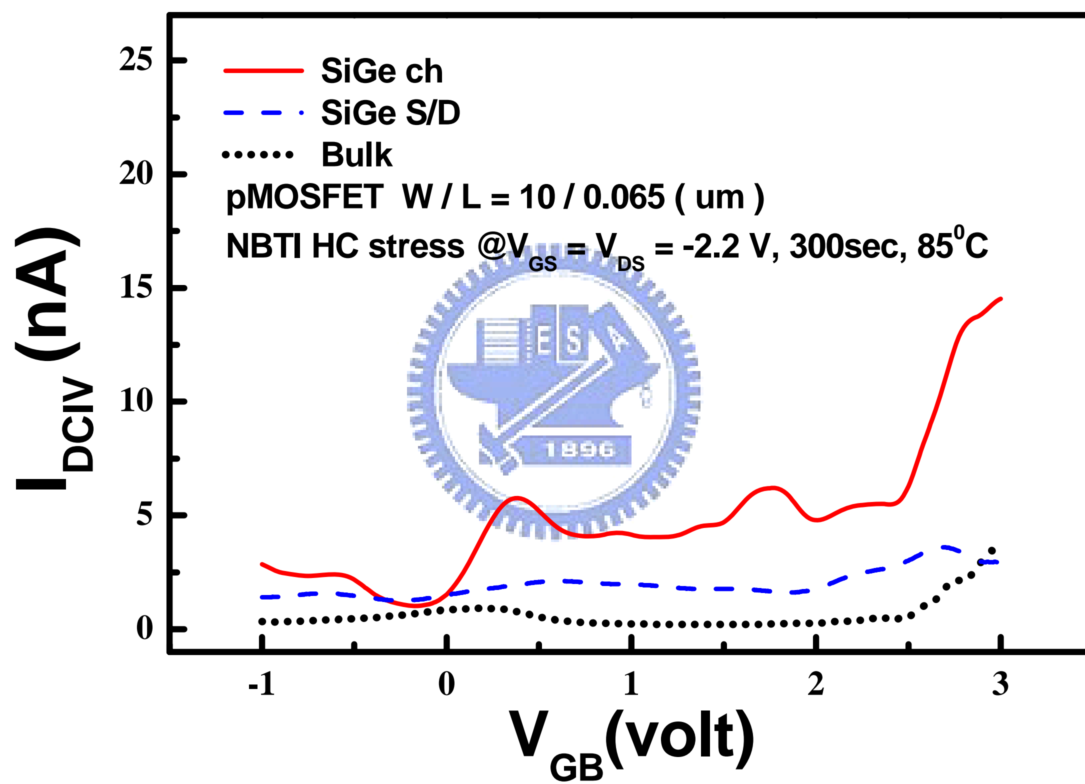


Fig 5-25 The experimental results of β DC-IV measurement for strained nMOSFETs after HC-like NBTI stress.

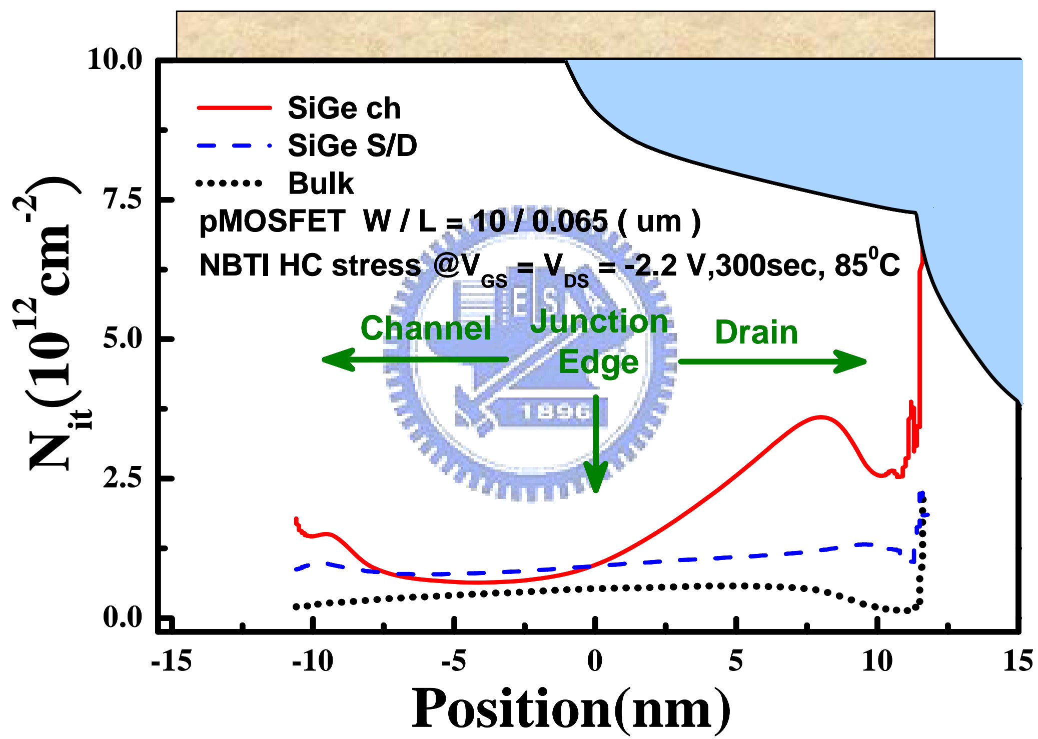


Fig. 5-26 The calculated results of the interface-traps lateral-profiling.

Chapter 6
Summary and Conclusion

In this thesis, ***for the first time***, we have developed a new DC-IV measurement, called β DC-IV measurement. The main idea of this measurement is to boost the DC-IV current level to exceed the gate-leakage current, and then we use *shift and subtract method* to extract the pure DC-IV current. This approach has been demonstrated for the devices with the thickness of gate-oxide down to 13A^0.

Based on β DC-IV measurement, a new interface-traps lateral profiling technique has been built ***for the first time***. The main concept of this technique is to find where the recombination and generation processes happen in the maximal probability, which can be described by the positions in which the intrinsic energy level is equal to the average of the sum of the p and n quasi Fermi levels.

In this thesis, each kind of schemes to design highly reliable CMOS devices by introducing various strain technologies has been proposed. Based on the results given by the experiments of HC stress and FN stress in application of IFCP and interface-traps lateral profiling technique, two main conclusions on the HC for strained nMOSFETs and NBTI for strained pMOSFETs have been provided: (1) **For strained nMOSFETs,** CSEL capping layer devices are much better in terms of reliability and performance than others devices. SSOI devices have good hot-carrier immunity and performance, but its channel interface quality has to be improved. The performance for SiC devices is good, but its defects of interface and junction are its disadvantage. SiGe on substrate devices own appreciated performance, but the Ge-out

diffusion effect is so serious that this kind of devices will be un-reliable. (2) For strained pMOSFETs, SiGe on S/D devices will be much better in terms of performance, HC, and NBTI reliability, but SiGe on channel devices have worse NBTI property and are complex to be made, which makes this kind of devices un-valuable. All of the descriptions above are summarized in Table 6-2. As a result, keeping with the progress of strain technology, it is necessary to make a trade-off and find the best strategy to improve the performance and keep reliable in the same time, which is a challenging task. All these results in this thesis will be valuable to design manufacturable CMOS devices in terms of performance and reliability down to 45 nm technology node and beyond.

<table>
<tr><th></th><th></th><th colspan="3">Strain nMOSFETs</th><th colspan="3">Strain pMOSFETs</th></tr>
<tr><td colspan="2">Direction</td><td colspan="3"><100>/(100)</td><td colspan="3"><110>/(100)</td></tr>
<tr><td rowspan="3">Uni-axial</td><td></td><td>$\Delta I_{D,on}$(%)</td><td>Reliability issues</td><td></td><td>$\Delta I_{D,on}$(%)</td><td>Reliability issues</td></tr>
<tr><td>Cap</td><td>30%</td><td>Not critical</td><td rowspan="2">S/DSiGe</td><td rowspan="2">35%</td><td rowspan="2">Ge-out diffusion on S/D</td></tr>
<tr><td>SiC</td><td>15.5%</td><td>Junction & interface defeats</td></tr>
<tr><td rowspan="2">Bi-axial</td><td>subSiGe</td><td>34%</td><td>Ge-out diffusion on substrate</td><td rowspan="2">chlSiGe</td><td rowspan="2">53%</td><td rowspan="2">Ge-out diffusion on channel & Misfit defeats induced by biaxail strain</td></tr>
<tr><td>SSOI</td><td>13.5%</td><td>Channel Interface quality</td></tr>
</table>

Table 6-1 The summary of strained CMOS devices in terms of performance and reliability in this thesis.

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