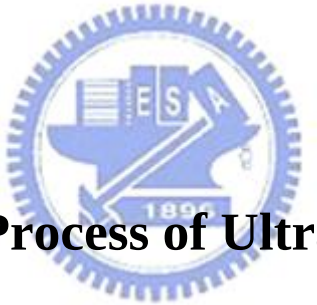
國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩 士 論 文

超薄含氮氧化層創新製程技術應用在 p 型金氧半場效電晶體之特性研究



New Advanced Process of Ultrathin Oxynitride on the Characteristics of pMOSFET

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摘　要

為了延續墨爾定律，元件尺寸的微縮必須持續下去，但是極薄的二氧化矽介電層將伴隨著極大的直接穿遂漏電流，而這個直接穿遂漏電流將對元件的功率消耗有嚴重的影響。在閘極二氧化矽介電層薄到１０奈米以下，將會隨著嚴重的漏電流，為了解決這嚴重的直接穿遂現象，我們將利用高介電係數材料來替換傳統的二氧化矽。我們利用的高介電係數材料在相同的等效二氧化矽厚度下，能擁有較大的實際物理厚度以抵擋直接穿遂的漏電流。

在先前的報告已指出，含氮氧化層擁有許多傳統氧化層所沒有的優點，例如，有好的抵抗硼擴散的能力、能有效的防禦高電場所照成的熱載子破壞、有較高的介電強度等優點。對於深次微米的ＵＬＳＩ的製程來說，含氮氧化層是能有效的去改善傳統氧化層的缺點而成為主流應用。

我們提出了新的方法能在多晶矽和介電層的介面上形成高氮含量的氧化層，更能有效的去抵擋硼的擴散。形成此含氮氧化層有三步驟，首先把晶片浸泡

於雙氧水中，形成化學氧化層，接著在低壓的環境下用氨氣去執行氮化，最後通氧氣用來執行再氧化動作。經過以上三各步驟，就可以在介面上形成高氮含量的氧化層，此法製程簡單而且跟目前的製程技術是相容的。

最後，我們會把此含氮氧化層應用在P型電晶體上，再來探討P型電晶體的電性和可靠度，都擁有低的漏電和對於施加高電場應力有好的忍耐度，且有強的抵抗硼擴散能力和抵抗熱載子能力。

New Advanced Process of Ultrathin Oxynitride on the Characteristics of pMOSFET

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Abstract

According to the scaling rules, aggressive scaling has lead to silicon dioxide (SiO_2) gate dielectrics as ultra thin in state-of-the-art CMOS technologies. As a consequence, static leakage current due to direct tunneling through the gate oxide has been increasing at an exponential rate. As technology roadmaps call for sub-10A° gate oxides within the next five years, a variety of alternative high-k materials are being investigated as possible replacements for SiO_2. The higher dielectric constants in these materials allow the use of physically thicker films, potentially reducing the tunneling current while maintaining the gate capacitance needed for scaled device operation.

Oxynitride(SiON) have been reported to show many advantages over thermal oxide.For example，excellent resistance to penetration of dopant and other impurities such as refractory metal，a higher dielectric strength，and enhanced resistance to damage induced by radiation and high-field stress . As the continuing scaling down of MOS

devices has made high-field-induced device degradation a major concern，thin oxynitride seem promising for applications as a replacement for a thermally grown oxide in submicrometer-range ULSI devices.

The oxynitrides with high nitrogen content distributed close to the surface are considered to be the best candidates for 65 nm CMOS integration or below. We propose an alternative approach for forming a high-nitrogen ultrathin oxynitride gate dielectric is demonstrated. The oxynitride growth included three process stages—chemical oxide growth, nitridation and subsequent dry oxidation. Meanwhile, chemical oxide as a starting oxide can provide a better controllability in film thickness. Following that, the chemical oxide was nitrided using a furnace in low-pressure NH_3 ambient to transfer high-nitrogen oxynitride. The nitrided chemical oxide was then placed in atmospheric O_2 ambient to form a robust oxynitride. The process proposed here is simple and fully compatible with current process technology.

Finally, by this technique, pMOSFET of oxynitride were fabricated to study electrical characteristics. They demonstrate excellent properties in terms of low leakage current, high endurance in stressing, superior boron diffusion blocking behavior and weak SILC effect, and good performance in HCI effect.

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首先很高興能夠進入此實驗室，也很謝謝羅正忠博士在這兩年的教導，提供我最完善的設備以及研究資源，讓我可以全心全力衝刺自己的論文研究，使自己的專業領域知識快速的吸收以及進步，教授也常常指導我平常為人處世以及如何和人溝通，讓我先體驗踏入社會的感覺，讓自己不會在業界和學校有間隔，出社會可以馬上適應，在此對於教授給予一個最誠心的感謝。

再來我要感謝的是柏村學長，學長啟蒙了我碩士研究題目的方向，讓我可以確定目標，全力衝刺並不會三心二意不確定自己的方向，且學長也常常點出問題的所在，讓我可以在最短的時間想出解決的辦法，在兩年內學長也常常陪我們去大潤發補貨，深怕我們作實驗太晚，沒有體力可以繼續衝刺，在此真心的祝福學長在事業上有很高得成就。

在此也很感謝智仁學長這兩年來的指導，如果沒有智仁學長帶領我們去 NDL 作實驗，我們可能要花費更多瑣碎的時間去摸索，有著學長交給我的經驗讓我們可以安心的衝刺研究也減少工安危險的產生，再來也感謝永裕學長每次 meeting 都會準時參加，教導我們如何做研究，如何抓取 paper 的重點，讓我們在學習效率上增進不少，在來要感謝宏春、德安、宏仁、正凱、信智、大峰..學長們，在我碩一時候的教導以及陪伴，讓我有一個快樂的碩一生活，再來感謝同屆同學們元愷、國洲、信富、小陸、晨修、嘉宏、岳展得陪伴，讓我的碩士生活變的多采多姿，考試時大家努力一起熬夜奮鬥，心情不好時大家一起聊天，無聊時大家也

一起出去玩，這是我最快樂的回憶，相信大家在畢業過後都能夠找到自己的喜歡愛的工作，也感謝學弟們再旁協助我們學長作實驗。最後也感謝爸媽還有姐姐的支持，讓我無後顧之憂的完成我碩士學位。

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Chapter 1

Introduction

As the MOS devices are scaled down less than sub-100nm, the oxynitride (SiON) have been reported to show many advantages over thermal oxide. For example, excellent resistance to penetration of dopant and other impurities such as refractory metal, a higher dielectric strength, and enhanced resistance to damage induced by radiation and high-field stress. As the continuing scaling down of MOS devices has made high-field-induced device degradation a major concern, thin oxynitride seem promising for applications as a replacement for a thermally grown oxide in submicrometer-range ULSR device such as RAM and EEPROM [1]. Oxynitride films also have reduced film stress when compare to silicon nitride, and improved thermal stability. In general, the benefit of a oxynitride film is the nitrogen in the film accumulates at the silicon interface to reduce the concentration of strained Si–O, potentially reducing the vreation of hot electron by as much three order of magnitude. An oxynitride later at Si/SiO2 interface of thin gate oxides has been found to be beneficial for improving the device electrical performance. This chapter gives the general background of oxynitride and brief review of process technologies. Oxynitride is a promising gate dielectric, which has potential advantages of ameliorating in the penetration of boron into the channel of the devices, and breakdown during device operation. During the past years, the author took a lot of efforts into this study and obtained moderate accomplishment. The result and discussions are collected and summarized in this dissertation.

1.1Background

The rapid progress of complementary metal-oxide-semiconductor(CMOS) integrated circuit technology since the late 1980's has enabled the Si-base microelectronics industry to simultaneously meet several technological requirements to fuel market expansion. These requirements include performance, for example speed, low static (off-state) power and a wide range of power supply and out voltage [2]. Following the “Moore's law”, doubling about every two or three years since about 1980, this has been accomplished by developing the ability to perform a calculated reduction of the dimensions of the fundamental active device in the circuit，[3]-[5]. Including the market associated with high-performance microprocessors as well as low static-power applications, such as wireless systems, the result has been a dramatic expansion in technology and communications markets. It can be argued that the key element enabling the scaling of the Si-based metal-oxide-semiconductor field effect transistor (MOSFET) is the materials and resultant electrical properties associated with the dielectric employed to isolate the transistor gate from the Si channel for decades: silicon dioxide (SiO2). The use of amorphous, thermally grown SiO2 as a gate dielectric offers several key advantages in CMOS processing including a stable (thermodynamically and electrically), high-quality Si-SiO2 interface as well as superior electrical isolation properties. In modern CMOS processing, defect charge

densities are on the order of $10^{10}\ cm^{-2}$, midgap interface state densities are $\sim 10^{10}\ cm^{-2}\ v^{-1}$ and hard breakdown field of 15 MV/cm are routinely obtained and are therefore expected regardless of the device dimensions. These outstanding electrical properties clearly present a significant challenge for any alternative gate dielectric candidate [6], [7].

Nowadays, advancement of VLSI technologies has resulted in continuous scaling down of metal oxide semiconductor field effect transistor (MOSFET), whose feature size used in IC chips has been reduced to deep-submicron technology node. The continuous shrinkage in MOSFET dimension has engendered a concomitant scaling in gate dielectrics to provide satisfactory circuit performance at low voltage. However, the continuous reduction of the gate-oxide layer thickness in advanced CMOS device leads to excessive gate leakage currents and reliability problem[8],[9]. The p-MOSFET with p+ poly-Si gate, an advanced CMOS structure to achieve low and symmetrical threshold voltages for low voltage operation, suffers from serious boron penetration from p+ poly-Si gate into the underlying Si substrate as devices go into deep submicrometerv regime due to the thin gate dielectrics. It has been shown that boron penetration not only causes a positive shift in threshold voltage but also severely aggravates the time-dependent dielectric breakdown (TDDB) characteristics [10], [11].

In fact, boron penetration depends on gate dielectric thickness, that is, the thickness variation of gate oxide in wafer will change amount of boron that diffuses into the channel. It has been showed that boron penetration exponentially increase with decreasing oxide thickness [12], [13]. K. S. Krisch et al. [14] have reported the correlation between thickness variation and voltage shifts on wafer with intentional thickness non-uniformity (see Fig. 1-1).

The flat-band voltage (V_{FB}) varies insensitively to the n-type gate device with thickness fluctuations, but p-type gate device is very sensitively, as shown in Fig.1-2, and a small gate oxide variation gives rise to large changes in V_{fb} and $V_{th.}$ While V_T variations degrade many aspects of device performance, increased off-state leakage current has critical importance for systems which must minimize power consumption. In order to maintain high performance with decreased power-supply voltages, low threshold voltage is required, which at the same time increases the off-state leakage current. A large spread in V_T will increases this leakage current. Similarly, tight V_T control is essential to minimize off-state power consumption. Thus precise thickness control is needed for the thin gate dielectrics in submicron CMOS processes.

1.2 Processing Techniques for Silicon Oxynitride

Thermally ultrathin oxynitride (SiON) have the better performance and low-voltage operation CMOS devices than thermal oxide. And then nitridation treatment on thin oxide has been used in MOS technology to strengthen the dielectrics robustness for electrical stress and to develop high permittivity gate dielectric stacks. In order to obtain the excellent properties of silicon oxynitride and fulfill the devices, a variety of processing techniques have been developed.

1.2.1 Nitridation of oxide with NH_3 and reoxidation of nitrided-oxide

Oxynitride has more advantages than thermal oxide, but the nitrided oxide that has these excellent properties is depended sensitively on the nitridation conditions such as process temperature, time and atmosphere [15]-[23]. In this process, hydrogen gas produced by the dissociation of ammonia gas deteriorates the quality of SiO_2 at around 900℃. Active hydrogen gas generated at temperatures as high as 900℃ dissolves Si-O bonds in SiO_2 and may result in positively charged silicon ions, proton ions and dangling bonds. The presence of hydrogen is reported to accelerate the formation of SiO especially at the Si/SiO_2 contact [24].

T. Hori et al. [25] reported that the electron trap density is increased in proportion to the hydrogen concentration in nitrided oxides. In their experiments, Fig. 1-3 shows nitrogen Auger electron spectroscopy (AES) depth profile and Fig. 1-4

shows hydrogen secondary ion mass spectroscopy (SIMS) depth profile for oxide nitrided at 950, 1050, 1150℃ for 60s. In figure 1-3, nitrogen piles up at both the Si-SiO_2 interface and the outer surface. As the temperature is raised, the nitrogen concentration increases monotonically through the film. The increasing rate of nitrogen concentration near the surface with the temperature is larger than that near the Si-SiO_2 interface. In Fig. 1-4, it can be seen that the hydrogen concentrations in nitrided oxide are considerably higher than those in a starting oxide.

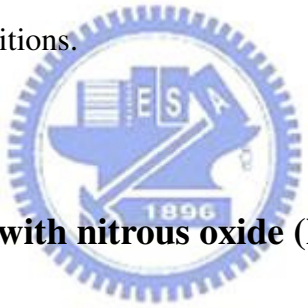
Fig. 1-5 and Fig. 1-6 show the nitrogen concentration near the Si-SiO_2 interface $[N]_{int}$ and the hydrogen concentration [H], respectively, versus the nitridation time for oxides nitrided at 900, 950, 1050, and 1150℃. In addition, Hori et al. [25] also found that the flat-band voltage shift (ΔV_{FB}) for a starting oxide is negative (−0.07 V), and this is considered to be mainly due to largely generated donor-like interface states. On the other hand, all of the ΔV_{FB}'s of nitrided oxides are positive. This indicates that a large number of electron traps have been introduced to nitrided oxides, and the positive shift owing to electron traps overwhelms a negative shift owing to generated interface states.

Fig. 1-7(a) (Fig. 1-7(b)) shows the ΔV_{FB} (the increase of midgap interface state density (ΔD_{itm})) induced by electron injection of 0.1 C/cm^2 versus nitridation time for oxides nitrided at 900, 950, 1050 and 1150℃. ΔV_{FB} increases monotonically as

nitridation proceeds. In contrast, ΔD_{itm} is found for the first time to show a turnaround with nitridation time: it increases at first, reaches a maximum at a certain nitridation time (t_{max}), and then decreases gradually to a certain value. The value is lower by more than one order of magnitude than that of a thermal oxide for a nitridation at a temperature higher than 1050℃. According to the above, it is difficult to make both ΔV_{FB} and ΔD_{itm} of a nitrided oxide small at the same time. While a heavily nitrided oxide has an advantage of small ΔD_{itm}, it shows a disadvantage of significantly large ΔV_{FB}. In fact, ΔV_{FB} can be reduced corresponding to the reduction of [H] by the reoxidation. Fortunately, reoxidation of nitrided oxides is very effective to eliminate the hydrogen-containing species in nitrided oxides while it keeps $[N]_{int}$ unchange (shown in Fig. 1-5 and Fig 1-6). It is striking that the reoxidation can reduce both ΔV_{FB} and ΔD_{itm} significantly at the same time. Based on the turnaround behavior of ΔD_{itm}, a two-factor model is proposed: one factor is [H], which increases $\triangle D_{itm}$, and the other is $[N]_{int}$, which reduces it. There have been proposed two types of centers as the origins of these weak bonds: one is hydrogen-containing centers [26], [27] and the other is the strained Si-O bond near the Si-SiO_2 [28], [29]. The former corresponds directly to one factor of two-factor model, the hydrogen concentration. The latter may correspond to the other factor, $[N]_{int}$, by a postulation that nitrogen incorporation to SiO_2 reduces the strained Si-O bonds: it might be possible that tensile stress due to

nitrogen incorporation counters the compressive stress that was present prior to nitridation [30].

As the mentioned above, studies on furnace nitridation of thermally grown SiO_2 layers at high temperatures with ammonia followed by reoxidation step have shown very promising trends toward reducing instabilities due to electron trapping, interface-state formation, destructive breakdown, and defect. Furthermore, Rapid thermal reoxidation of NH_3-nitrided SiO_2 has been proven to be effective in reducing the formation electron traps. This process, however, is more complicated and strongly dependent on the process conditions.



1.2.2 Oxynitride growth with nitrous oxide (N_2O) or nitric oxide (NO)

Silicon oxynitride films grown thermally using nitrous oxide (N_2O) and nitric oxide (NO) has been studied [31]-[37]. The first report of oxynitride grown with N_2O by H. Fukuda et al. [38] and H. Hwang et al. [39] is published in 1990. Oxynitride grown with N_2O contained nitrogen had drawn attention as candidate gate dielectrics due to its process simplicity and excellent reliability [40]-[47]. The advantages of N_2O-based oxynitride include (1) excellent boron diffusion barrier characteristics compared to pure SiO_2, (2) no significant electron trapping atoms compared to NH_3-based oxynitride due to less hydrogen environment during process, and (3) low

thermal budget compared to nitridation oxide. It is reported that the nitrided oxide using N_2O has the nitrogen piled up preferentially at the Si-SiO_2 interface [46], [48]-[50].

A study of N_2O nitridation kinetics, P. J. Tobin et al. [45] calculated that N_2O fully decomposed to N_2 (64.3%), O_2 (31.0%) and NO (4.7%) as it heated up to the furnace temperature of 950℃. Tobin et al. found that the peak nitrogen concentration (N_p) in the film depends linearly on the NO gas phase concentration and conjectured that NO is the critical species responsible for nitridation or the interfacial nitrogen concentration. In addition, some researchers study nitridation of oxide directly with NO gas. Two significant findings are observed on oxynitrides, which are treated with NO and N_2O. First, at a process temperature of 950℃, the NO treated oxynitride provides much tighter N distribution and slightly higher N_p than that of N_2O oxynitride. Second, the N_p peak is slightly located inside SiO_2 for the N_2O treated oxynitirde. Contrarily, the NO treated oxynitrde shows its N_p position inside the Si substrate (see Fig. 1-8).

In Y. Okada et al. [44], they show that a much lower thermal budget is required for an NO process than that of N_2O process. Thus it produces an oxynitride with useful properties. In submicron technology node, MOSFET's with NO treated oxynitride showed superior current drive characteristics and comparable hot carrier

immunity to those with N_2O treated oxynitride.

1.2.3 Reoxidation of nitride with H_2O

Traditional oxynitride films are formed by nitridation process on an existed oxide film with sequential NH_3, NO or N_2O's treatment. However, this approach has its difficulty in fabricating gate dielectric film thinner than 3nm due to gate dielectrics thickness will also keep increasing during oxynitridation. T. Yamamoto et al. [51] proposed that the thin oxynitride can be formed with direct nitirdizing on bare silicon and following sequential oxidation process. In general, the silicon nitride, formed by nitridizing the silicon with NH_3, can block the oxygen (O_2) penetration efficiently even at low temperature range, such as 900℃. T. Yamamoto et al. utilized the H_2O to oxidize the ultra-thin nitride which is formed thermal nitride, not the CVD nitride. No boron penetration, longer hot-carrier lifetime and high drain current are achieved. It also reported that electron trap density can be reduced by introducing hydrogen into nitride film during wet oxidation. Somehow their statements are contrary to the discussion mentioned before. In this report, they did not show any sample's SIMS data, which had been annealed at 1050℃, to remove hydrogen concentration distribution. It is possible that the high temperature annealing process with large thermal budget has driven the hydrogen away leading to low hydrogen concentration

in oxynitride film. The arguments proposed by T. Yamamoto that low electron trap is due to existed hydrogen in oxynitride during wet conversion with H_2O is debatable.

It is known that the oxynitride which formed by NO, or N_2O, or NH_3 treatment can effectively suppress boron penetration. However, they also come with several degradation of the oxide reliability due to the nitrogen piles up along the interface between silicon substrate and oxynitride. From D. Wristers et. al. [52], they have demonstrated that BF_2–implanted polysilicon gated p-MOS capacitors using ultra-thin nitrided oxide with NO treatment is highly effective in the alleviation the boron penetration-induced flat-band voltage instability (see Fig. 1-9). Unfortunately, such improvements are observed in conjunction with some degradation of the oxide reliability due to the boron-blocking/accumulation inside the gate dielectric (e.g., charge-to-breakdown and electron trapping, Fig. 1-10). Fig. 1-11 shows the schematic of boron diffusion from the heavily doped p^+ gate into the gate dielectric and substrate interface region. In the conventional SiO_2.device (Fig. 1-11(a)) boron diffuses due to the concentration gradient from the heavily doped p^+ gate into the SiO_2/Si interface and Si substrate. On the contrary, in the NO-nitrided device (Fig. 1-11(b)) the nitrogen-rich layer at the SiO_2/Si interface obtained the excellent boron-stopping properties at that interface resulting in additional boron accumulation inside the oxide leading the enhanced dielectric reliability degradation. Thus, there is

a trade-off between device performance stability and gate oxide time-dependent dielectric breakdown (TDDB) reliability.

1.3 The mechanism of oxidation in Reoxidation nitrided-oxide

1.3.1 Nitrogen depletion in reoxidation nitrided-oxide

N. S. Saks et al. [53] also propose a nitrogen-related reaction model which occurs in N_2O furnace oxidation. Via this reaction, nitrogen is removed from the bulk of the oxide during oxidation, while at the same time it is incorporated at the growing Si-SiO_2 interface. Thus, the final nitrogen profile relies on the dynamic equilibrium between competing processes which causes both nitrogen incorporation and removal (as shown in Fig. 1-12). The data in Fig 1-12(c) clearly show that a reaction (Si－N－Si+NO→Si－O－Si+N_2) occurs during N_2O reoxidation which removes nitrogen from oxynitride. Summarily, reactions with NO are probably responsible for the nitrogen depletion effect observed for furnace oxidation.

However, given the unknown time required to heat the N_2O gas to decompose (N_2O→N_2+O), Ellis et al. [54] suspect that some N_2O survived to decompose near the wafer, resulting in exposure of the wafers of Saks et al. to atomic oxygen. Under sufficiently high flow rates, atomic oxygen may survive to reach the wafer. It has been shown previously, with low pressure O_3 annealing, that atomic oxygen is capable of

scavenging N from an oxide [55], Ellis suggest that the species responsible for N removal is atomic oxygen.

Finally, Gusev et al. [56], [57] observed that for NO-grown films the nitrogen is distributed relatively evenly in the film. This implies that nitrogen is incorporated but not removed during NO oxynitridation. Thus, it can be concluded that the nitrogen depletion during oxidation in N_2O is caused by atomic oxygen, not the NO.

1.4 Thesis Organization

This chapter tells us theory of oxynitride .All of previous theory, it is desired to have a simple and excellent way to find the high quality oxynitride film. Nowadays, low thermal budget and thin oxynitride films are preferred to apply in ULSI technology. Chapter 2, we propose a new method to build robust ultrathin oxynitrde with high nitrogen diffusion barrier near its surface which is formed by NH_3 nitridation of chemical oxide (H_2O_2) and reoxidation with O_2, and then we will describe that the basic electrical characteristic research of high-nitrogen oxynitride (12 at. %) reoxidation with O_2 which we proposed. Chapter 3 extends the studies in chapter2. We will discuss the reliability of the p-MOSFET with high nitrogen diffusion barrier near its surface which is formed by NH_3 nitridation of chemical oxide and reoxidation with O_2. Chapter 4, I will conclude the previous three chapters by using summary and Chapter 5 suggests for my future work.

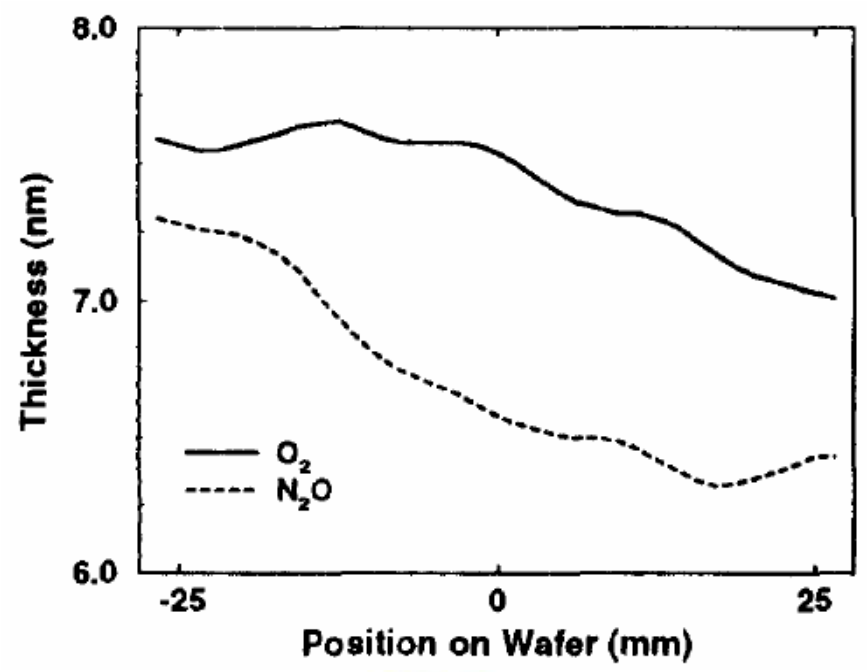


Fig. 1-1 The exaggerated thickness variation as a function of position on wafer for O_2 and N_2O-grown gate dielectrics. (After Krisch et al, Ref. [14])

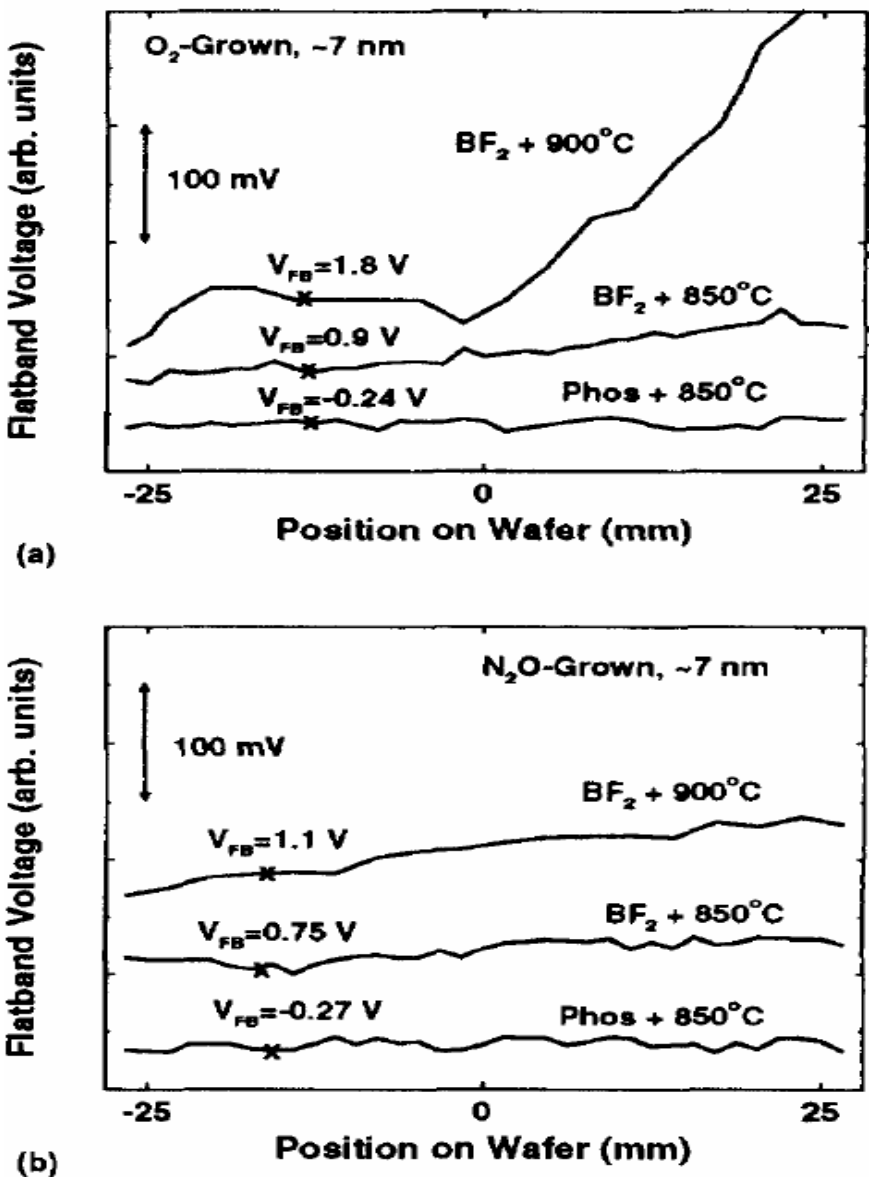


Fig. 1-2 V_{FB} as a function of position on wafer for (a) O_2 and (b) N_2O-grown gate dielectrics with gate electrodes implanted and annealed as indicated. The thickness nonuniformity illustrated in Fig. 1-1 results in a large V_{FB} variation on those samples with substantial boron penetration. (After K.S. Krisch et al, Ref. [14])

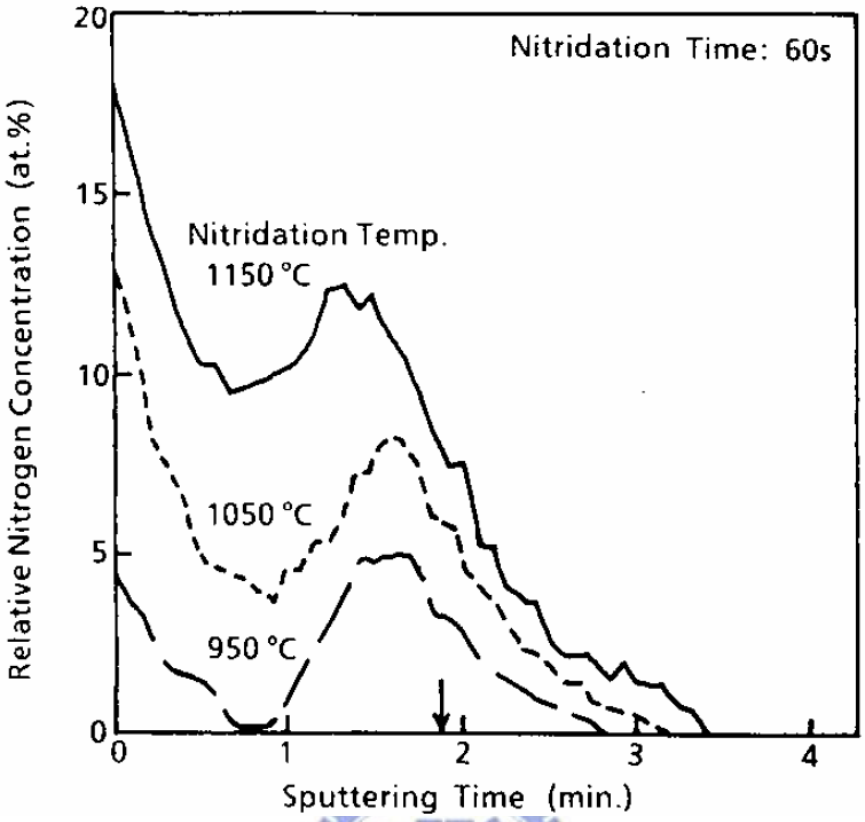


Fig. 1-3 Nitrogen AES depth profiles of 8-nm-thick oxides nitrided at 950, 1050, and 1150℃ for 60 s. The arrow indicates the position of the Si/SiO2 interface. The nitrogen concentration increases monotonically as nitridation proceeds. (After T. Hori et al, Ref. [25])

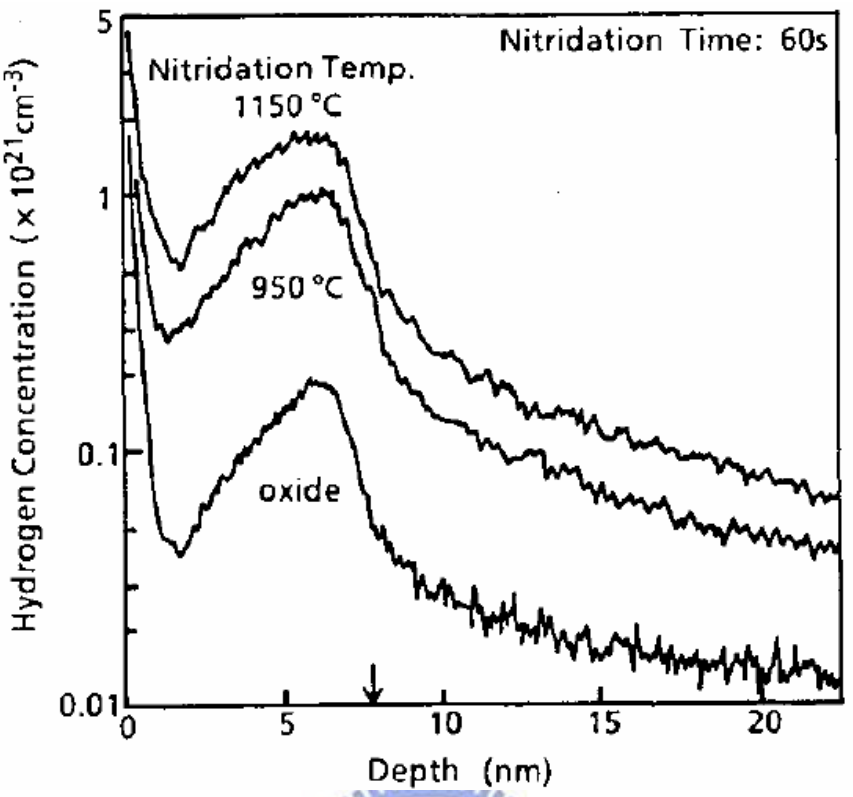


Fig. 1-4 Hydrogen SIMS depth profiles of 8-nm-thick oxide nitrided at 950 and 1150℃ for 60 s. The arrow indicates the position of the Si/SiO2 interface. The hydrogen concentration increases monotonically as nitridation proceeds. (After T. Hori et al, Ref. [25])

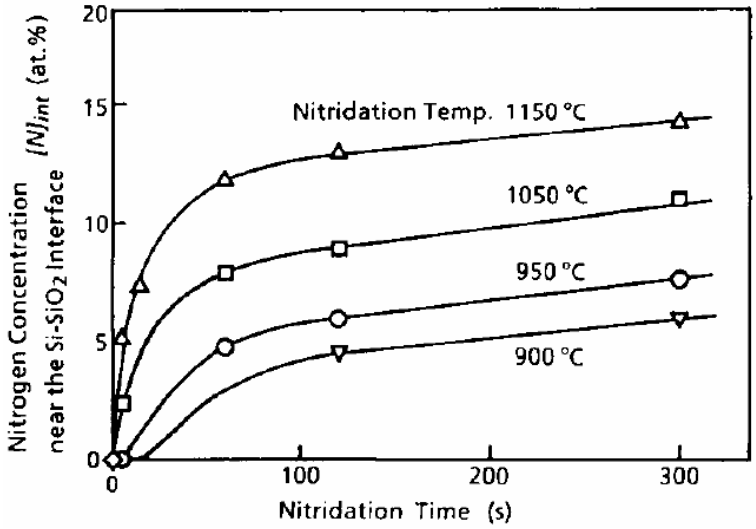


Fig. 1-5 Nitrogen concentration near the Si-SiO_2 interface $[N]_{int}$ versus nitridation time for oxides nitrided at 900, 950, 1050, and 1150℃. $[N]_{int}$ increases monotonically as nitridation proceeds. (After T. Hori et al, Ref. [25])

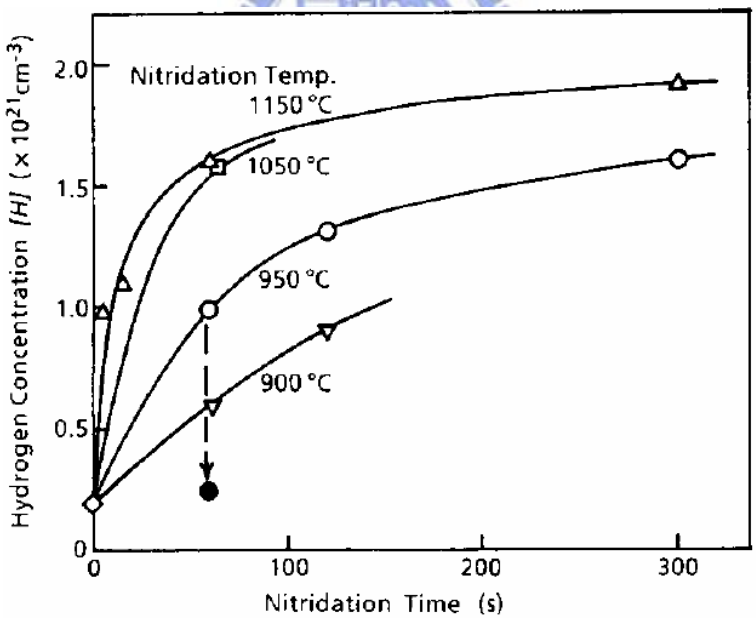


Fig. 1-6 Hydrogen concentration [H] versus nitridation time for oxides nitrided at 900, 950, 1050, and 1150℃. The dashed arrow and • in the figure indicate the effect of re-oxidation at 1150℃ for 60 s following a nitridation at 950℃ for 60 s. (After T. Hori et al, Ref. [25])

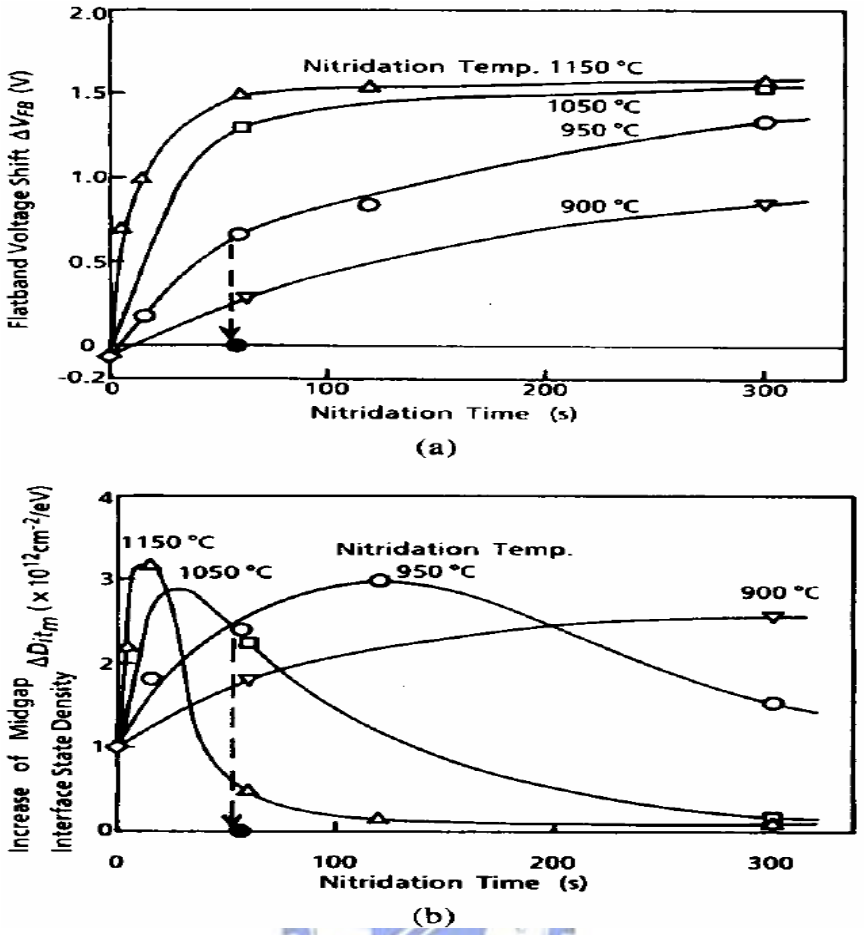


Fig. 1-7 (a) The flat-band voltage shift ΔV_{FB} and (b) the increase of midgap interface state densityΔD_{itm} by 0.1C/cm^2 electron injection versus nitridation time for oxides nitrided at 900, 950, 1050, and 1150℃. The dash arrow and • in each figure indicate the effect of re-oxidation at 1150℃ for 60 s following a nitridation at 950℃ for 60 s. While ΔV_{FB} increase monotonically as nitridation proceeds, ΔD_{itm} shows a turnaround. (After T. Hori et al, Ref. [25])

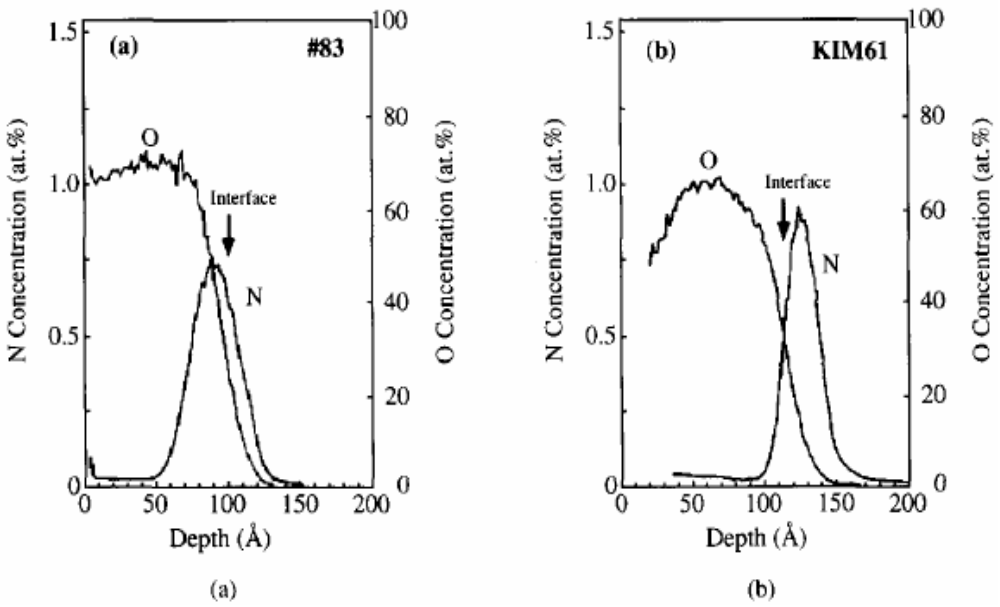


Fig. 1-8 SIMS profiles of (a) N_2O oxynitride grown at 950℃, (b) NO oxynitride processed at 950℃. (After Okada et al, Ref. [44])

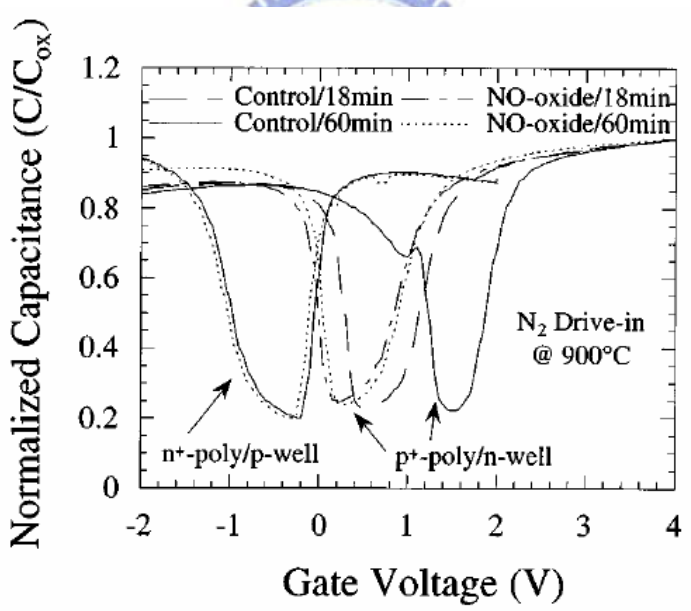


Fig. 1-9 Normalized quasistatic C-V curves for both p^+-poly and n^+-poly MOS capacitors with different gate dielectrics. The drive-in anneal was performed at 900℃ in N_2 for 18 or 60 min (After Wristers et. al, Ref. [51]).

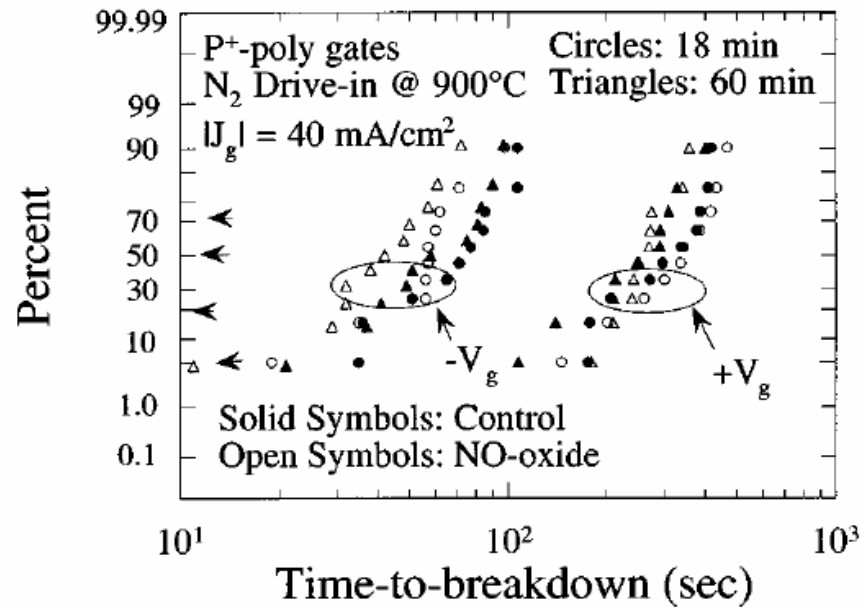


Fig. 1-10 Time-dependent dielectric breakdown (TDDB) distribution for p^+-poly gated PMOS capacitors under ±Vg gate bias stress. (After Wristers et. al, Ref. [51]).

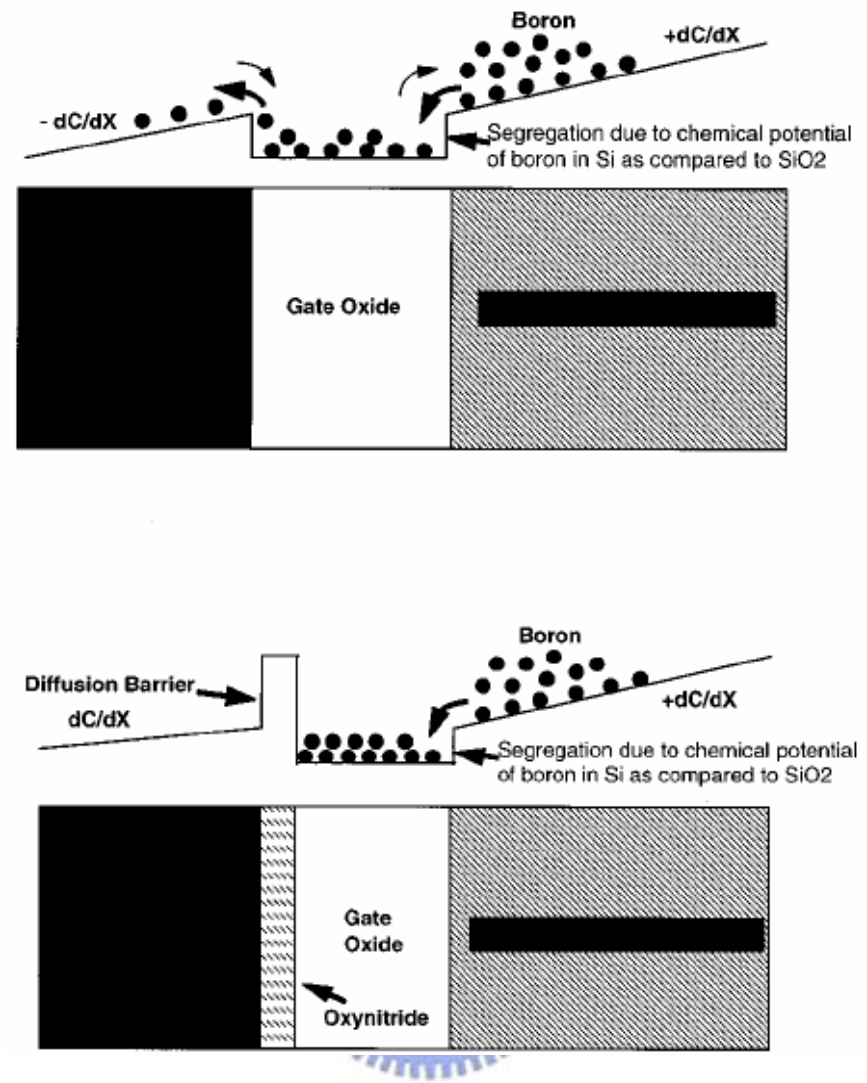


Fig. 1-11 The schematic of boron diffusion from the heavily doped p^+-gate into the gate dielectric and substrate interface region for conventional SiO_2 gate dielectrics (a) and interaction of the boron with the nitrogen at the interface for the NO nitrided gate (b) (After Wristers et. al, Ref. [51]).

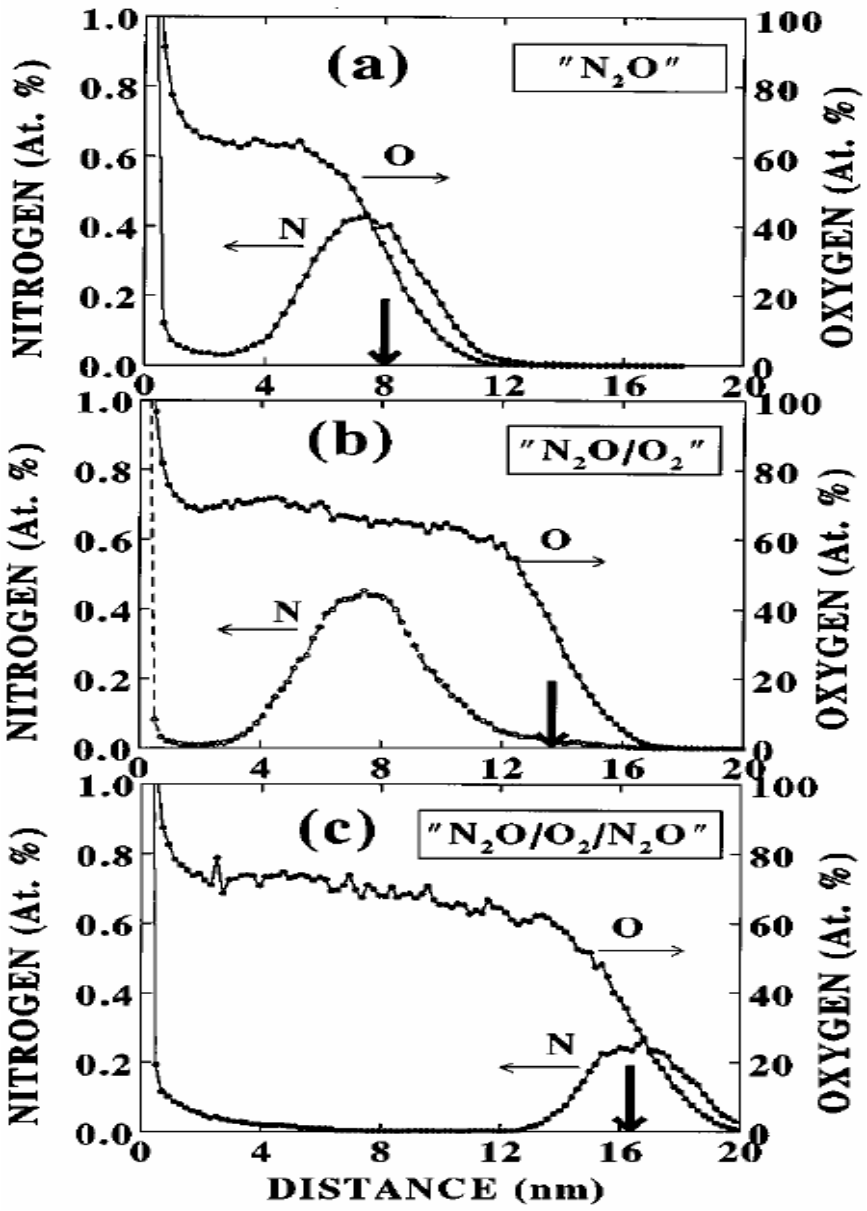


Fig. 1-12 SIMS profiles of nitrogen (N) and oxygen (O): (a) Nitrogen peak is located at Si–SiO_2 interface. (b) Despite the substantial increase in oxide thickness, the nitrogen profile is essentially unchanged. (c) New nitrogen peak has formed at the new Si–SiO_2 interface position. (After Saks et al., Ref. [53])

Chapter 2

Robust Ultrathin Oxynitride with High Nitrogen Diffusion Barrier near its Surface Formed by NH3 Nitridation of Chemical Oxide and Reoxidation with O2

2-1 Introduction

The continuous shrinkage of device dimension below a quarter-micro requires highly reliable ultra-thin dielectric film. In this thickness range, not only breakdown but also wear out of dielectric films is one of the key technology issues. As an alternative gate dielectric, nitrided oxide has drawn considerable attention due to their superior performance and reliability properties over conventional SiO2. For example, in a P^+-gate device, boron can easily diffuse into the channel region through the ultrathin gate oxide layer during the dopant activation process [58], [59], leading to threshold voltage being shifted. In principle, a small voltage shift that results from boron penetration will not cause a problem as long as it is predictable. The situation can be improved with modified threshold-adjusted implants. However, boron penetration not only causes the threshold voltage V_T to be shifted, but also degrades the process margin by increasing the spread of V_T. Since boron penetration is sensitive to gate dielectric thickness, the thickness variation of the gate oxide plays an important role in controlling the degree of boron penetration. In fact, it has been

reported that boron penetration increases exponentially with decreasing oxide thickness. Furthermore, the threshold voltage variation degrades a device's performance and increases its off-state leakage current.

On possible approach to form nitride oxides was post-oxidation annealing, including ammonia (NH3), nitrous oxide (N2O) and nitric oxide (NO) annealing. unfortunately, they usually require specific tools or gas. It is desired to have a simple way to obtain the film and retain its quality. In fact, reoxidized NH_3-oxynitride was proposed in the late 80s to the early 90s, however on thick thermal oxide,. The difference between this process (reoxidized NH_3-oxynitride) and the process mentioned above is that the former technique suffered a much higher thermal budget. The process temperature is around 1050℃ or even higher[60]. The film obtained by such process technology always comes out with a thick film. Compared with that in the case of the new process (developed in this paper), both thin thickness and film quality can be obtained successfully with low thermal budget, i.e., at low reoxidation temperature (900℃). Meanwhile, chemical oxide as a starting oxide can provide a better controllability in film thickness[61]. Nowadays, lower process temperatures and thinner oxynitride films are preferred in ULSI technology.

In addition, it is well known that gate dielectric doped with nitrogen can effectively suppress boron diffusion. However, the side effect is that the gate oxide

suffers from the oxide reliability issue owing to nitrogen piled up along the interface between the silicon substrate and oxynitride [52]. Ideally, we would like to have a nitrogen-doped dielectric with high nitrogen content close to the surface, which can effectively block boron diffusion, while low nitrogen content is distributed in the interface, which would not degrade oxide reliability.

In this chapter, an alternative approach for forming an oxynitride gate dielectric with high nitrogen content distributed close to the surface is demonstrated. The proposed approach is realized by NH_3 nitridation of chemical oxide and reoxidation with O_2. By this technique, the desirable nitrogen concentration profile can be obtained to meet the requirement of device performance. It is noted that the process proposed here is simple and fully compatible with current IC industry fabrication technology.

2-2 Experiment procedure

Standard local oxidation of silicon (LOCOS) process was applied for devices isolation. The pMOSFETs were fabricated on 6-inch p-type (100) Si wafers utilizing conventional self-align process. After dipping sacrificial oxide about seven minutes, standard RCA clean was used to remove organic, particle and metal contamination. At once , The oxynitride growth included three process stages－chemical oxide growth,

nitridation and subsequent dry oxidation. First, the wafers were immediately immersed into H_2O_2 solution at room temperature for 20 min to grow 10-Å-thick chemical oxide. Following that, the chemical oxide was nitrided using a furnace in low-pressure (120 mTorr) NH_3 ambient at 750℃ for 30 min. The nitrided chemical oxide was then placed in atmospheric O_2 ambient at 932℃ and annealed in N_2 at 932℃ for 10 min to form a robust oxynitride. Furthermore, a conventional oxide grown at 800℃ was also prepared to serve as the control sample. A 200nm poly-silicon was deposited by low pressure chemical vapor deposition (LPCVD). Subsequently, gate electrode was defined by I-line lithography stepper and etched by RIE etching system. After removing sidewall polymer, S/D extension implant was executed. Spacer formation was carried out by low pressure chemical vapor deposition (LPCVD). To continue patterning and S/D implant. Then, rapid thermal anneal (RTA) was performed at 950°C for 20 sec in N_2 ambient to activate dopants. Afterwards, SiO_2 capping layer (5000A) was deposited by low pressure chemical vapor deposition (LPCVD). Al-Si-Cu metallization were sputtered by PVD system. Fig.2-1 shows the experimental flow, and Fig.2-2 shows the nMOSFET structure.

Basic electrical characteristic such as I-V and C-V was measured by a 4156C precision semiconductor parameter analyzer and HP4282 LCR meter. The equivalent oxide thickness (EOT) of the gate dielectrics was obtained from I-V accumulation

region without calculating poly depletion and substrate condition.

Besides, Interface state density (N_{it}) conversion was evaluated from charge pumping method. A square-wave generated (f=1MHz) which generated from 8110A was applied to the gate electrode and the base voltage was varied from inversion to accumulation, while keeping the pulse amplitude at 1.5v. From the equation $N_{it} = \frac{\mathrm{Icp}}{qAf}$ whereas A, f and q are the area of gate electrode, the frequency of pulse voltage and electron charge, interface state density (N_{it}) could be extracted.

The hole mobility for pMOSFETs was evaluated by split C-V method. The effective mobility was measured at low drain voltage and then gave

$$\mu_{\mathrm{eff}} = \frac{g_d L}{W Q_p}$$

Where the drain conductance g_d was defined as

$$g_d = \frac{\partial I_D}{\partial V_{DS}} \Big|_{V_{GS}=constant}$$

Q_p was measured from capacitance measurements. The capacitance meter was connected between the gate and the source-drain connected together with the substrate floating. Therefore, Q_p was expressed as follows

$$Q_p = \int_{-\infty}^{V_{GS}} C_{gc} dV_g$$

And effective electric field produced by the gate voltage was express as:

$$E_{eff} = \frac{Q_b + \eta Q_p}{K_s \varepsilon_o}$$

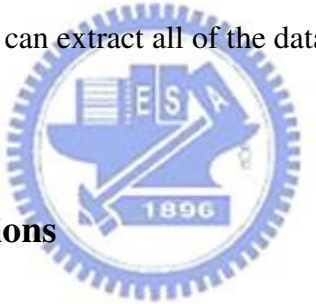
$$Q_b = \int_{Vfb}^{V_{GS}} C_{gb} dV_g$$

$$Q_p = \int_{-\infty}^{V_{GS}} C_{gc} dV_g$$

Where Q_b and Q_p were charge densities in depletion layer and inversion layer, respectively. The parameter η=1/3 was for hole mobility. And subsequently universal mobility was accomplished by this equation.

$$\mu_{eff} = \frac{638}{1 + \left(\frac{\varepsilon_{eff}}{area} \right)^{1.69}}$$

Above all equations, we easily can extract all of the data what we need.



2-3 Results and Disscussions

2-3-1 Extract Tox using Accumulation Direct-Tunneling Currents

As oxide thickness shrinkage down to the direct-tunneling region, tunneling current will strongly dependent on the oxide thickness. For example, tunneling current will be increased by 10 times as oxide thickness decreases from 22A° to 20A°. Therefore, using direct-tunneling current to extract oxide thickness becomes feasible solution. Since gate current in inversion mode is strongly dependent on the poly depletion effect and threshold shifts, using inversion gate current to determine oxide thickness becomes more difficult. On the other hand, using accumulation gate current

to determine oxide thickness is much easier since it will be independent on the poly depletion and substrate condition. As a result, a simple model can be used to evaluate Tox from accumulation gate current at different gate bias, named DTIV [62]:

$$\text{For Vg=-1.5V; Tox}=\frac{[10.1-\log(Jg)]}{6.2}$$

$$\text{For Vg= -1V; Tox}=\frac{[9.6-\log(Jg)]}{6.5}$$

Where Jg is the accumulation gate current density united A/cm^2 and Tox united nm.

2-3-2 Electrical Characteristics of pMOSFETs with Ultrathin Oxynitride has High Nitrogen Concentration near its Surface Formed by NH3 Nitridation of Chemical Oxide and Reoxidation with O_2

A nitrogen distribution profile across the 25Å and 70 Å oxynitride gate dielectric revealed by secondary ion mass spectrometry (SIMS) are shown in Fig. 2-3. Apparently high nitrogen concentration with a peak located at the dielectric surface is observed. Such high nitrogen concentration is more helpful in resisting the boron penetration of the gate dielectric from the P^+ polysilicon electrode. The low nitrogen concentration at the interface also improves reliability [63], [64]. Figure 2-4 shows the C-V shift of P^+-gated samples for the ultrathin oxynitride (23 Å) and conventional oxide (30 Å) with annealing at 900℃ for various times (60, 90 and 120 min).

Comparing oxynitride with conventional oxide, it is apparent that the C-V curve shift in oxynitride is relatively smaller than that in conventional oxide. This implies that boron penetration is highly impeded by this oxynitride film. Meanwhile, the oxidation rates for the wafers, which have an existing oxide film grown by the conventional method or our nitrided-chemical oxide, are compared in Fig. 2-5. The results show that the oxidation rate of the nitrided-chemical oxide is much smaller than that of the conventional oxide. At this point, this implies that the nitrided-chemical oxide provides a wider process window to well control gate oxide thickness if ultrathin oxide is needed.

The measured gate current-voltage (I-V) of the P^+-gated MOSFET with EOT 20Å oxynitride films are shown in Fig.2-6. We can observe that gate leakage current is very small and balance when the device operates in inversion region. When the process of chemical oxide formation proceeds, the clean oxide inhibits defect formation because it does not require a high-temperature process. This means that chemical oxide as a starting oxide is essential in this process. Fig. 2-7 shows the thickness of oxynitride is thinner than oxide. As oxide thickness shrinkage down to the direct-tunneling region, tunneling current will strongly dependent on the oxide thickness. if significant reduction of leakage currents is obtained. Because, effective nitrogen incorporation from NH_3 nitridation the chemical oxide film increases

dielectric constant, which allows physically thicker film with EOT to suppress the direct tunneling leakage current.

For further study, the hysteresis in the C-V characteristics of the P^+-gated sample with 20 Å oxynitride film was also evaluated. The data are shown in Fig.2-8. The figure shows that there is no hysteresis found in the high-frequency C-V curve, indicating that the film has a very low bulk or interface trap density. Fig.2-9 shows that the dominant conduction mechanisms in this oxynitride are direct tunneling and F-N tunneling. Frenkel-Poole conduction mechanism does not exist, because Ig-Vg curve is weak temperature dependence. We believe the limited of traps in this oxynitride is probably responsible for this, because the F-P conduction requires a high density of traps.

Fig. 2-10(a) shows a family of drain current curves of an pMOSFET transistor of oxynitride and oxide. We can find that the oxynitirde has better driving capability than oxide at the same overdrive (Vov). While Fig.2-10(b) shows the corresponding transconductance and current at V_d=-0.1V characteristics. The oxynitride device exhibits high drain current and high transcondance(110uS). The mobility of oxynitride compared to conventional oxide shows at Fig.2-11.

Fig 2-12 shows the Vth-roll-off characteristics. When channel length is less than 1um, Vth-roll-off phenomenon is more serious. Fig 2-13 indicates the sub-threshold

swing of devices with different channel length. And we find that sub-threshold swing is almost the same in different channel length. The Vth Weibull distribution in oxynitride and conventional oxide shows in Fig.2-14. It shows that oxynitride Vth has uniform distribution.

2-4 Summary

From basic electrical characteristics, we can get better performance for oxynitrdie. And we have a special process to achieve the high quality oxynitride. We have proposed an approach for forming high quality ultrathin oxynitride films with a nonuniform nitrogen content distribution, which has high content at the surface and low content at the interface between oxynitride and the silicon substrate, without using extra equipment or gas and which is totally compatible with current semiconductor fabrication technology. Oxynitride has lower leakage current than thermal oxide at the same EOT (equivalent oxide thickness), and have better driving capability, excellent suppression of boron diffusion. The direct tunneling and FN tunneling dominate the current transport in the oxynitride film, which weakens the temperature dependence. And we can control the growth of film precisely. There are many advantage for oxynitride we adopt. So we prove this process of oxynitride is a good candidate in the future.

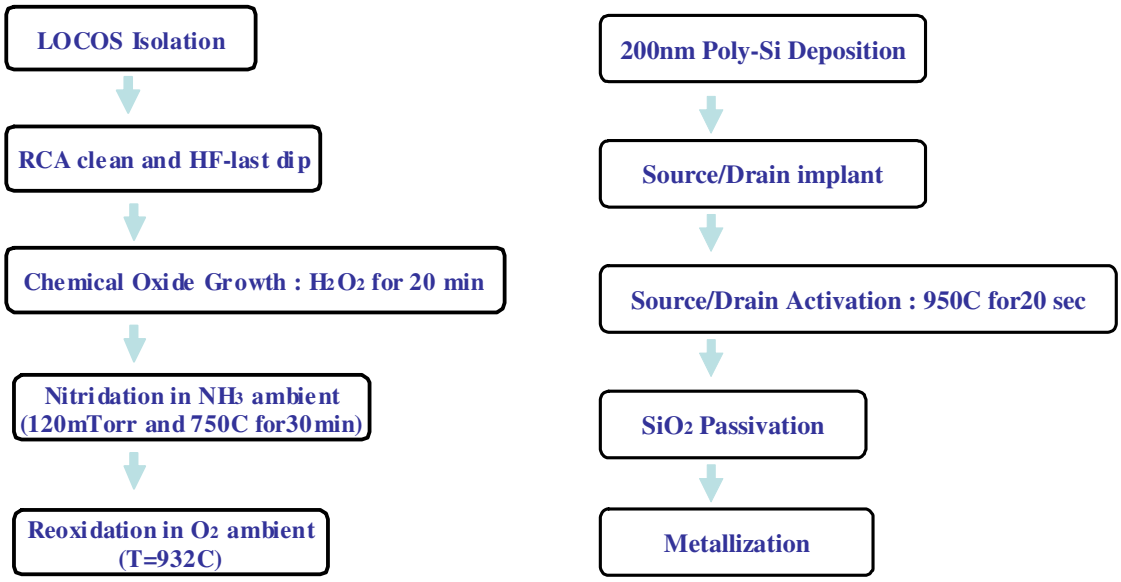


Fig.2-1 Experimental Flow.

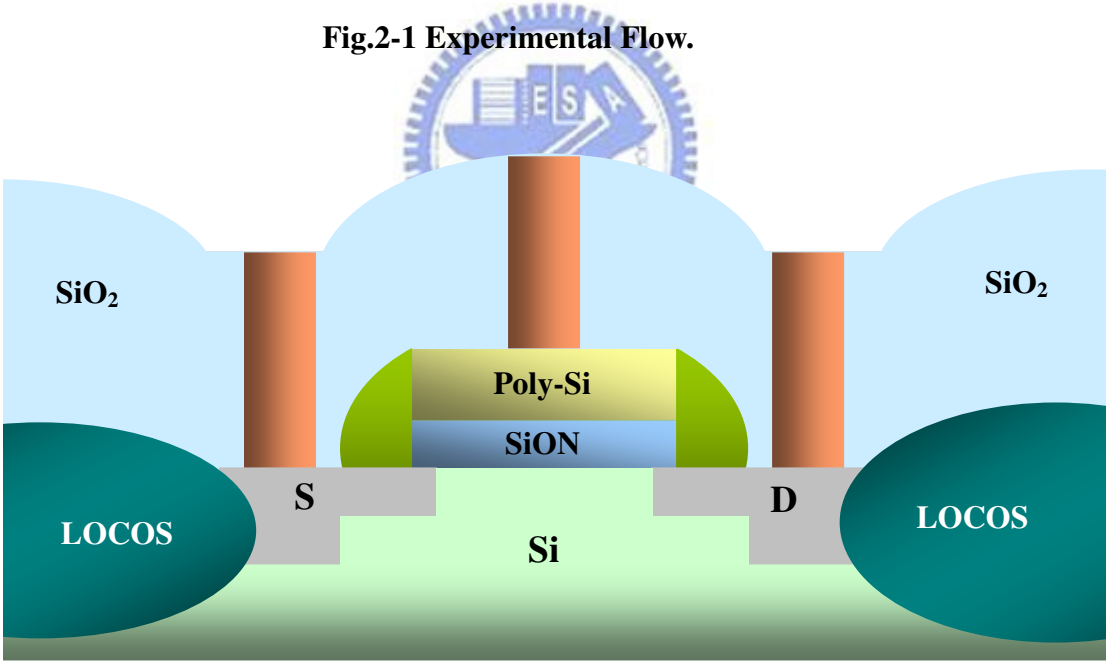
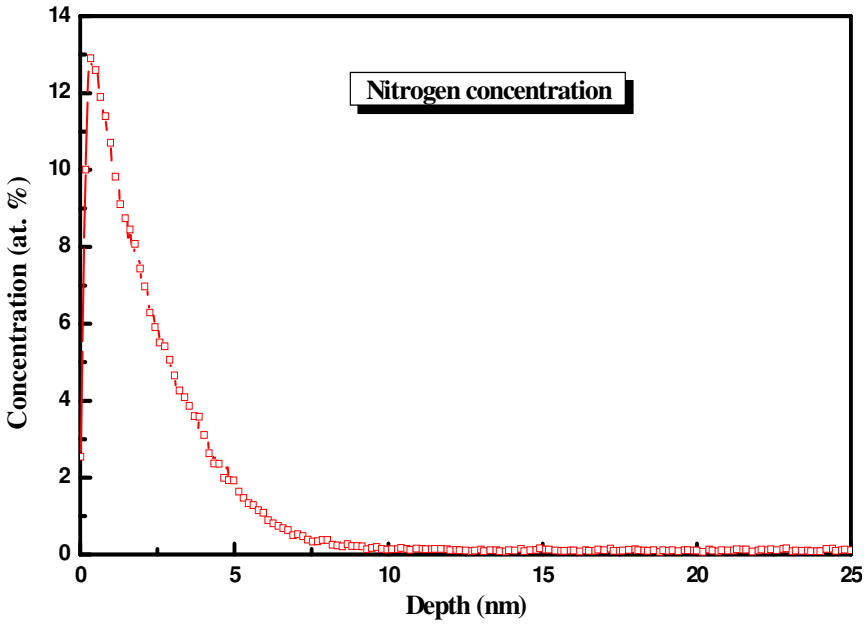
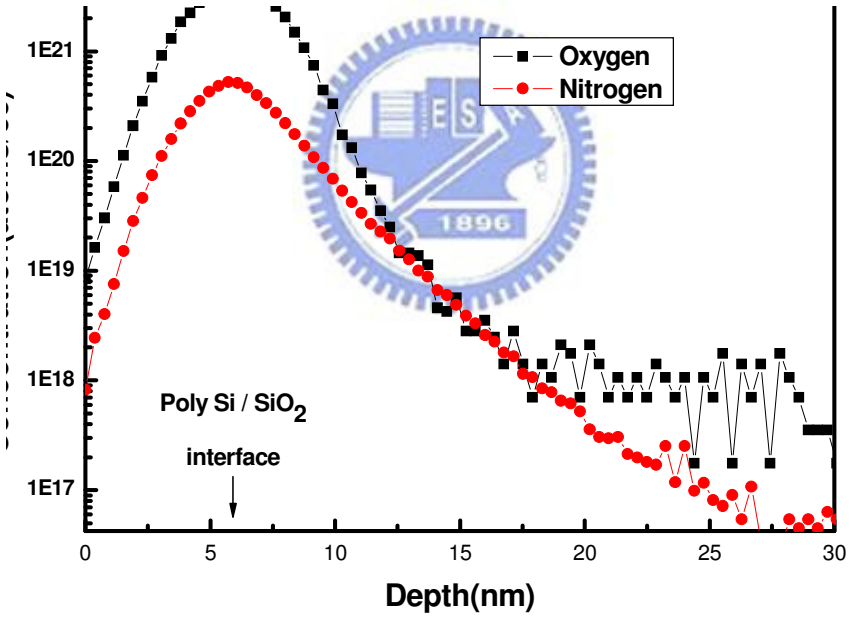


Fig2-2 pMOSFET structrre.



(a)



(b)

Fig.2-3 SIMS profile of oxygen and nitrogen distribution of (a) 70 A° and (b) 25A° oxynitride.

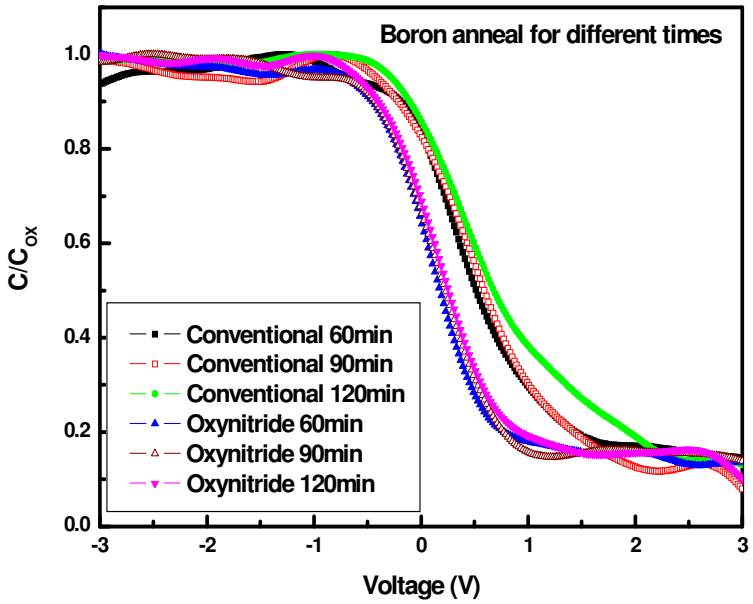


Fig. 2-4 High-frequency C-V characteristics of p^+-gated MOS capacitor for ultrathin oxynitride (23 Å) and conventional oxide (30 Å) with different annealing times.

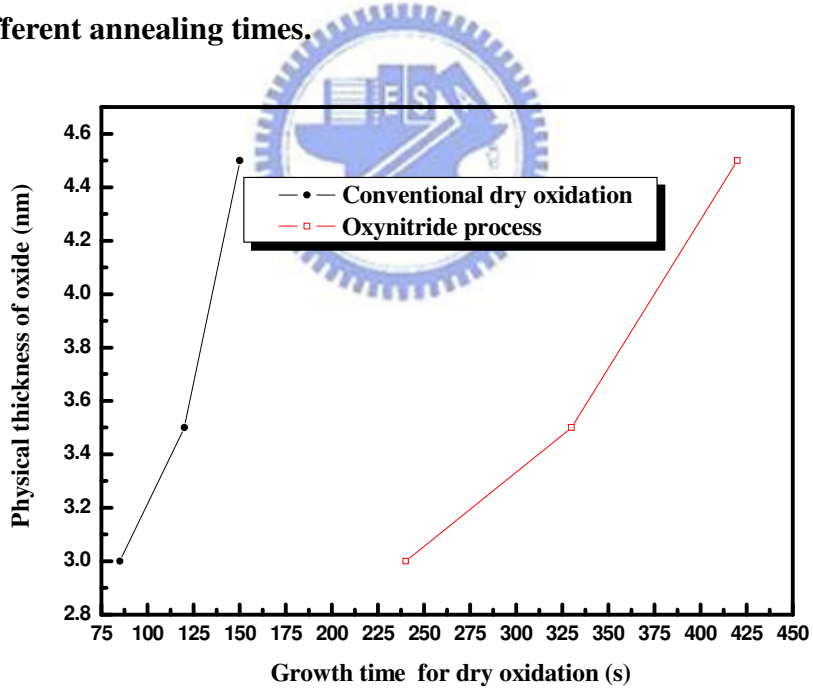


Fig.2-5 Growth time for dry oxidation versus physical thickness of oxide for conventional dry oxidation and oxynitride processes.

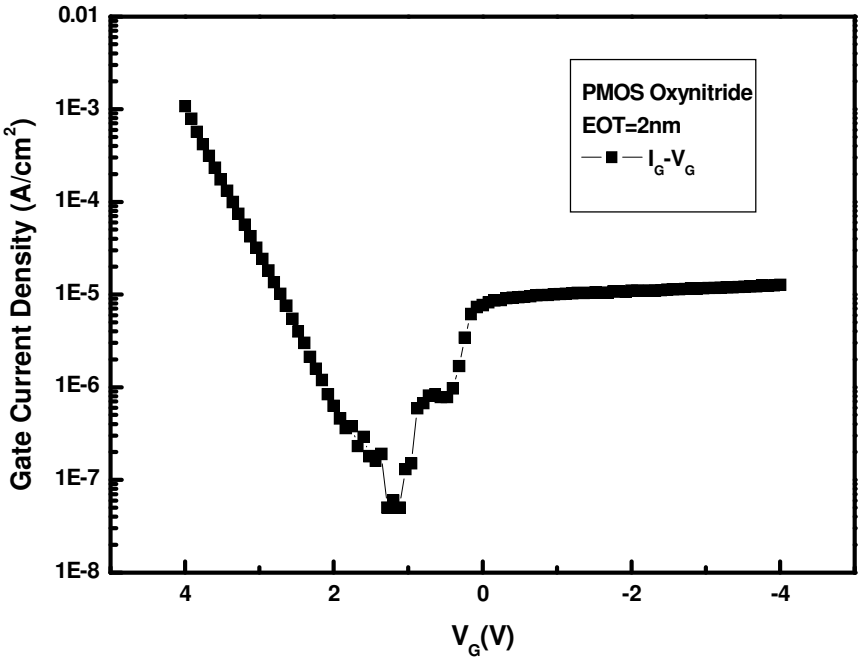


Fig.2-6 Gate leakage current density versus gate bias for fresh p-channel devices at room temperature.

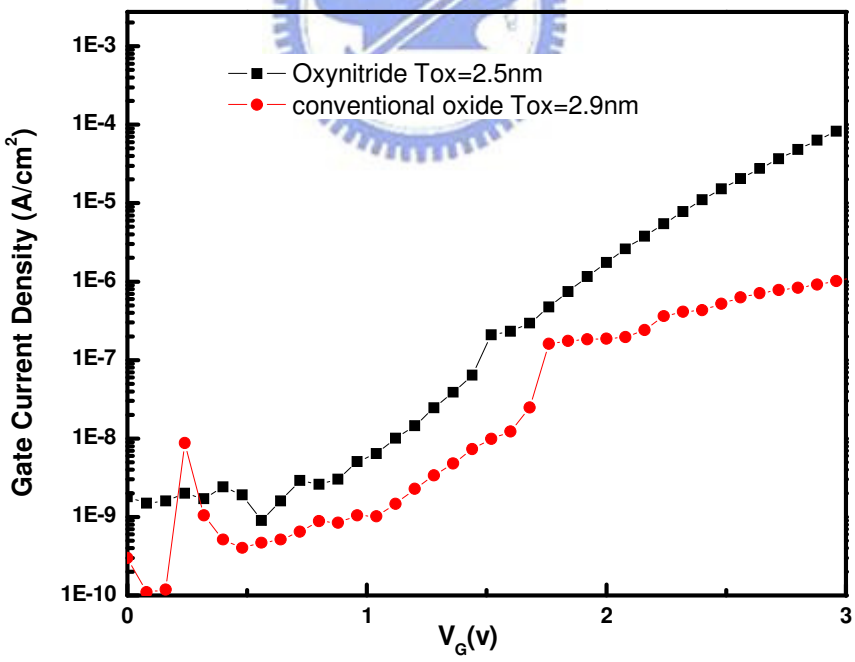


Fig2-7 Gate leakage current density versus electric field of pure thermal oxide and oxynitride.

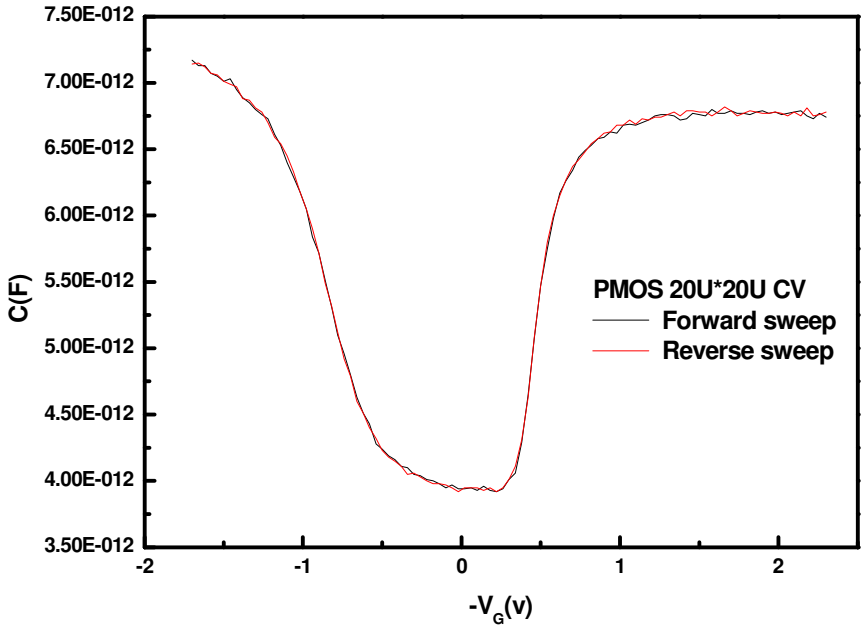


Fig2-8 Hystersis characteristics of oxynitride film with EOT=20A°.

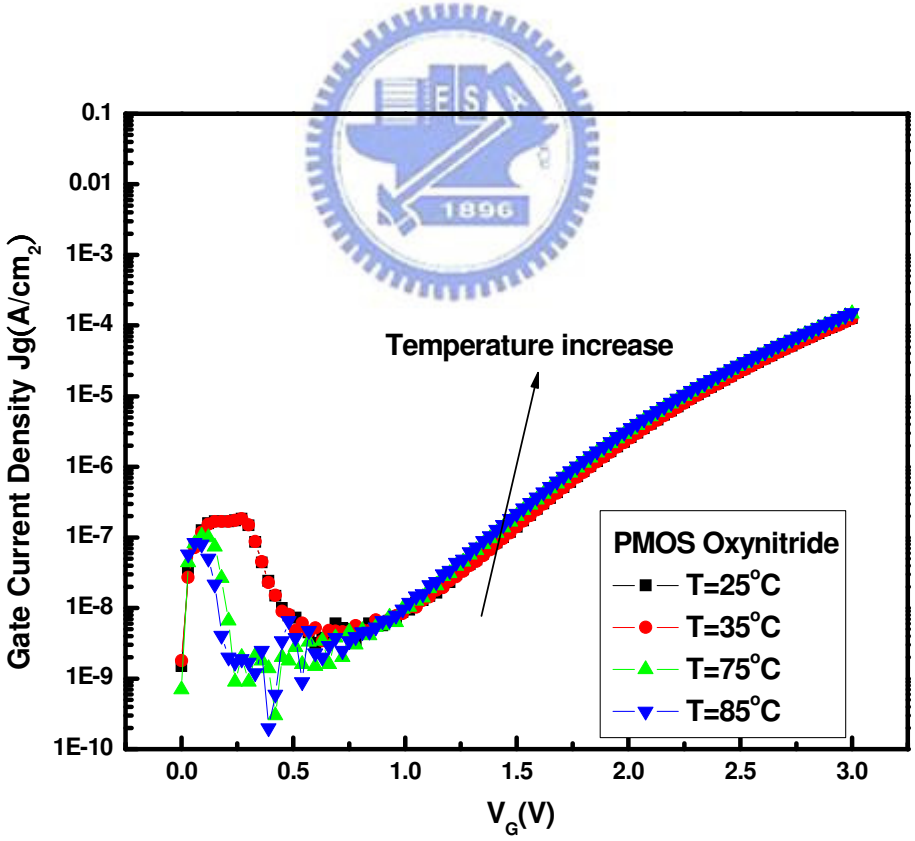
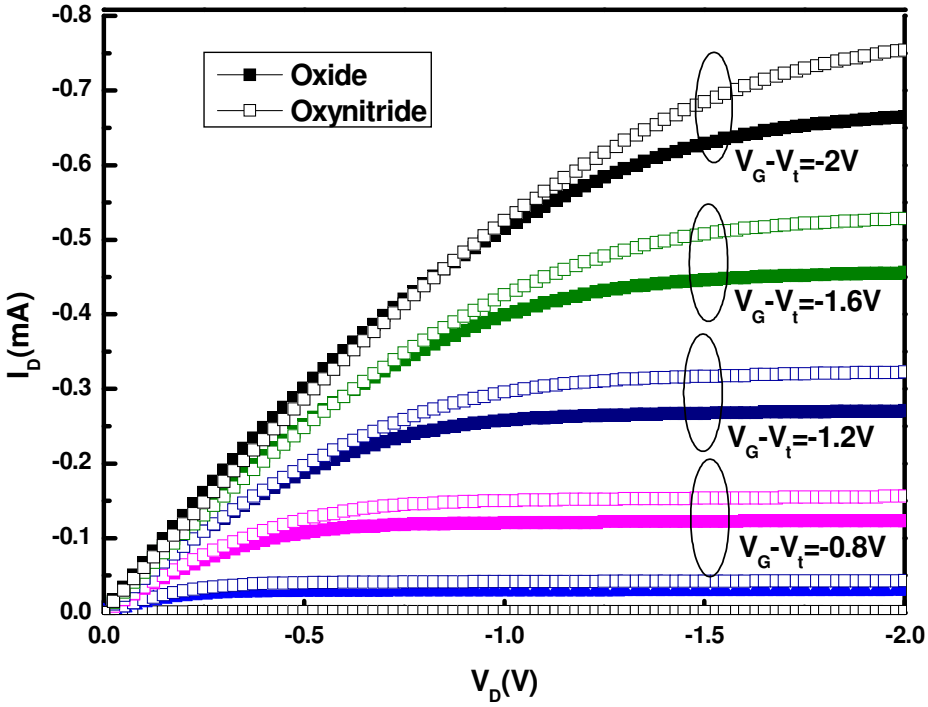
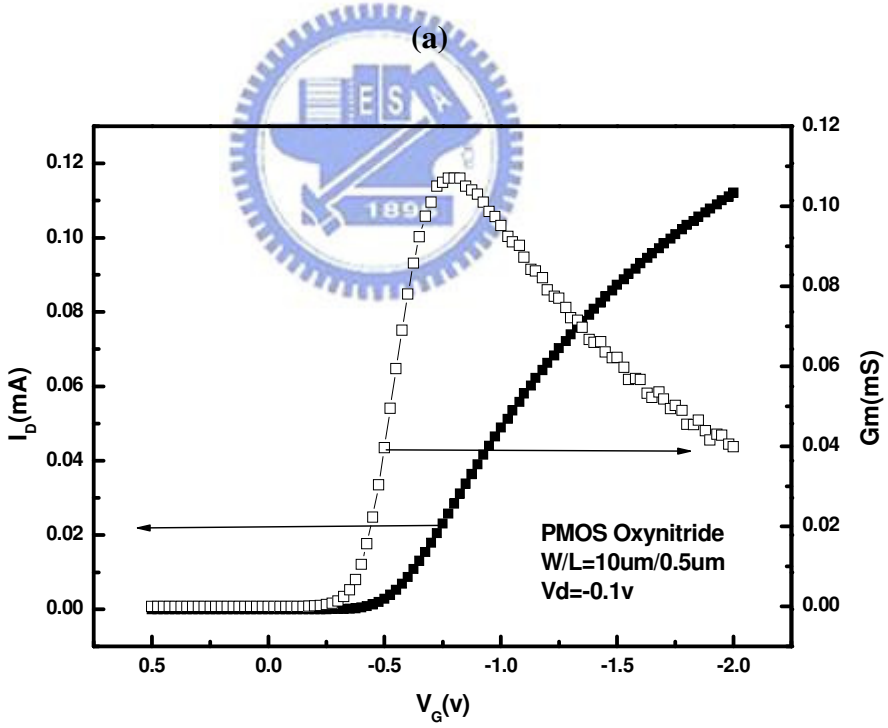


Fig. 2-9 I-V characteristics at various temperature.



(a)



(b)

Fig.2-10 (a) Id-Vd characteristics (b) Gm and Id-Vg characteristic of oxynitride for nMOSFET.

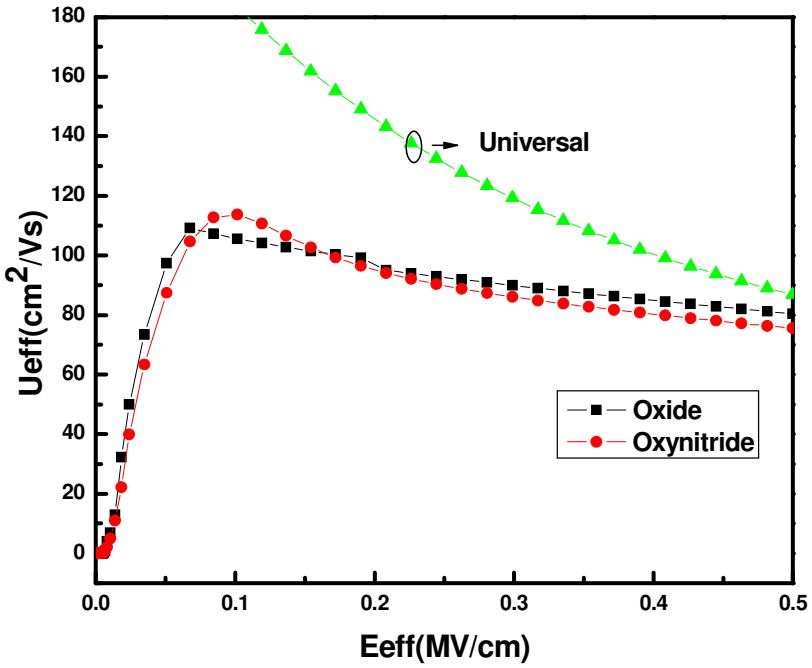


Fig.2-11 Compared electron mobility with oxynitride and oxide measured by split-CV method.

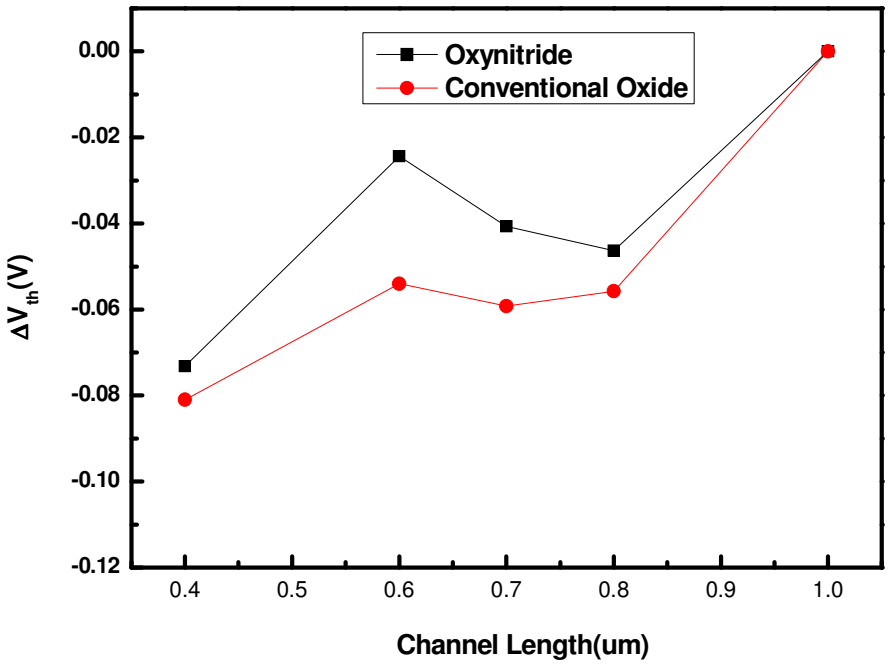


Fig.2-12 Vth roll off characteristic of oxynitride and conventional oxide.

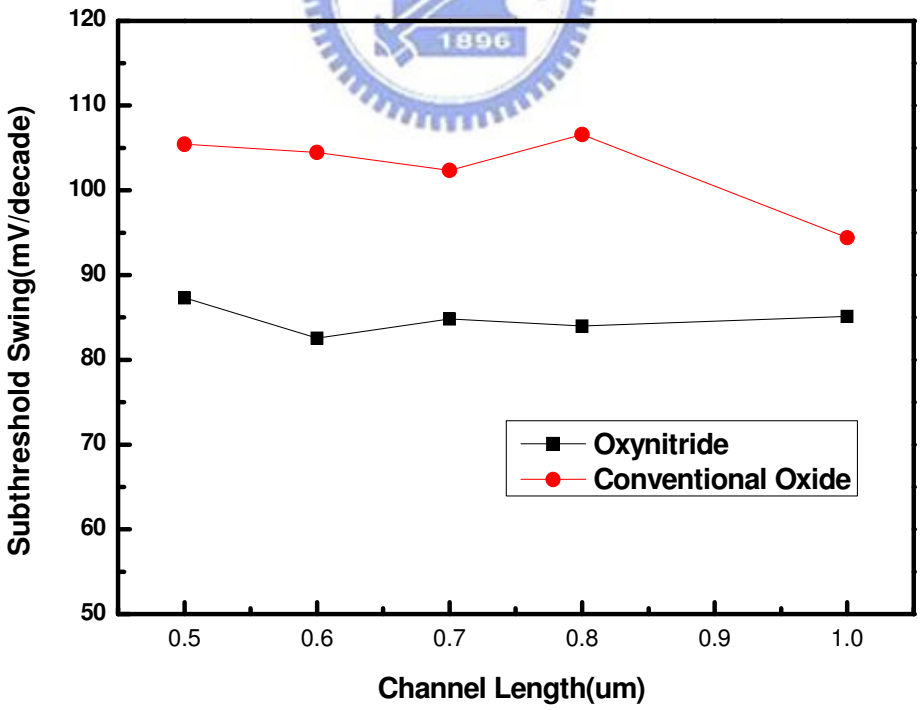


Fig.2-13 Subthreshold swing of devices with different channel length.

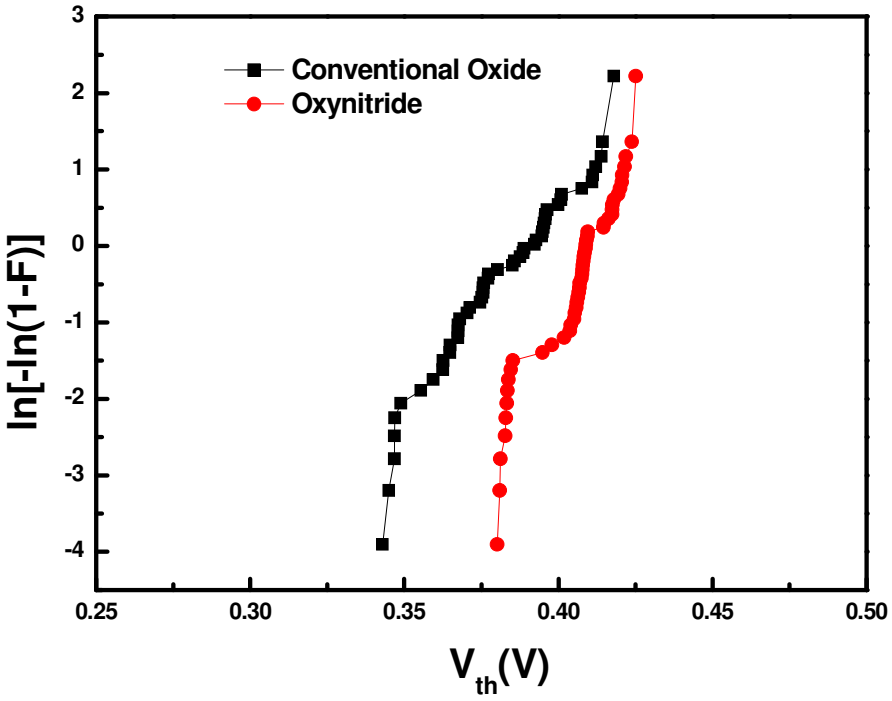


Fig.2-14 Vth Weibull distribution in oxynitride and conventional oxide.

Chapter 3

Reliability characteristic of Robust Ultrathin Oxynitride with High Nitrogen Diffusion Barrier near its Surface Formed by NH3 Nitridation of Chemical Oxide and Reoxidation with O2

3.1 Introduction

The constant increase in integrated circuit densities predicted by Moore's law requires the continued scaling of complementary metal – oxide semiconductor (CMOS) device dimensions. As device dimensions shrink into sub-micron meters, reliability is an important issue in scaled MOSFET, especially PMOSFET. Such as PMOSFET have more serious problems than NMMOSFET on temperature varying. And than during high voltage stress, defects can be generated in the devices, which in turn cause threshold voltage shifts and devices characteristics degradation. The device parameter variation can lead to circuit failures, both for analog and digital application.

Moreover, it has been been reported that the temperature acceleration effect and the stress induced leakage current(SILC) reliability were severe enough to raise concern over the further scaling down of thermal oxide. This SILC phenomenon may be due to enhanced FN tunneling by building of the generated holes similarly to the intrinsic breakdown. As the dielectric film is thinner, it has been a seriously problem

with regard to not only retention characteristic but also read disturb for Flash memories. Ultrathin oxynitride films have been reported with good performance in SILC.

Besides, hot carrier effects in SiO2 gate dielectric has been one of a major concerns for device scaling, especially nMOSFETs while the pMOSFETs has less problematic due to smaller impact ionization formation and the higher valence band barrier height. What hot carriers we mention is near the drain regions where charge carriers are accelerated by the field and become hot, can overcome the oxide barrier and inject into the gate. Hot carriers induce damage to the gate oxide and may be trapped there, thereby degrading the device performances.

We have known various methods to discuss reliability dependent of above theories. So this chapter, We will discuss various reliability of ultrathin oxynitride . We will find the oxynitride which we proposed not only to increase dielectric constant of the resulting film to achieve thinner equivalent oxide thickness(EOT) without degrading SiO_2/Si interface properties, but also to have excellent electrical and reliability characteristics.

3.2 Measurement setup

Constant voltage stress (CVS) is the method to evaluate reliability of devices as it causes threshold voltage to shift with electrical stressing. A constant voltage stress is applied to device gate from V_g = -2~-3V, while source/drain and substrate are grounded. After stress, SILC on pMOSFETs is measured under accumulation and then measures such as IG-VG, ID-VG and charge pumping are concluded. IG-VG can reveal the leakage current increasing after constant voltage stress, because constant voltage stress produces defect in the dielectric. ID-VG measurements are used to evaluate Gm variations and threshold voltage shift and subthreshold swing. And charge pumping measurements are also used to obtain interface density generation.

Analogous method which we measure is applied to HCI (hot carrier injection). Their difference is that using extra high voltage is applied to drain electrode which causes impact ionization in the depletion region near the drain side and electron-hole pairs are generated. At the same time, electrons will flow toward substrate to form substrate current (Isub). For the purpose of application for degradation from HCI, pMOSFETs devices are stressed at the max substrate current corresponding gate voltage which regards as the most efficient generation of hot carriers. Eventually, we exploit the most serious degradation method to evaluate HCI. And Fig 3-1 reveals basic measurement method for SILC and HCI.

3-3-1 Stress Induce Leakage Current on pMOSFET

Fig 3-2(a) and Fig.3-2(b) expresses I_d-V_g characteristics for oxynitride and conventional oxide before stress and after stress 1000s. It can be seen conventional oxide has serious degradation of Vth shift after stress. Relatively, oxynitride has good performance in SILC. Then, Fig 3-3(a) and Fig.3-3(b) shows in detail the threshold voltage shift and interface trap density shift which compares oxynitride with oxide . Besides, we observe that threshold voltage shift becomes huge as constant voltage stress increases. And in Fig 3-4(a) and Fig.3-4(b), we also find out that subthreshold swing variation and Gm variation of oxynitride is smaller than oxide. It may be attributed that more electron-hole pairs which generate in channel region and tunnel to the gate dielectrics which turn to great threshold voltage instability. Fig.3-5(a) shows the result after constant voltage stress at -3V for sample with EOT=20A°. No significant SILC was observed after 1000 sec stressing. In Fig.3-5(b), it shows the sample after different constant voltages stressing during 1000sec stressing. No significant SILC increase of leakage current was observed for these samples, too.

Fig.3-6(a) and Fig.3-6(b) ,respectively, show the threshold voltage shift and interface trap density shift in oxynitride with different temperature. We find that threshold voltage shift and interface trap density shift increase with temperature increasing, so that, the device will accelerate to breakdown. Fig.3-7 shows that the longer time-to-breakdown(Tbd) for the oxynitride film is primarily attributed to its

lower leakage current, which causes less damage to the dielectric and thus contributes to a longer dielectric lifetime.

3-3-2 Hot Carrier Injection on pMOSFETs

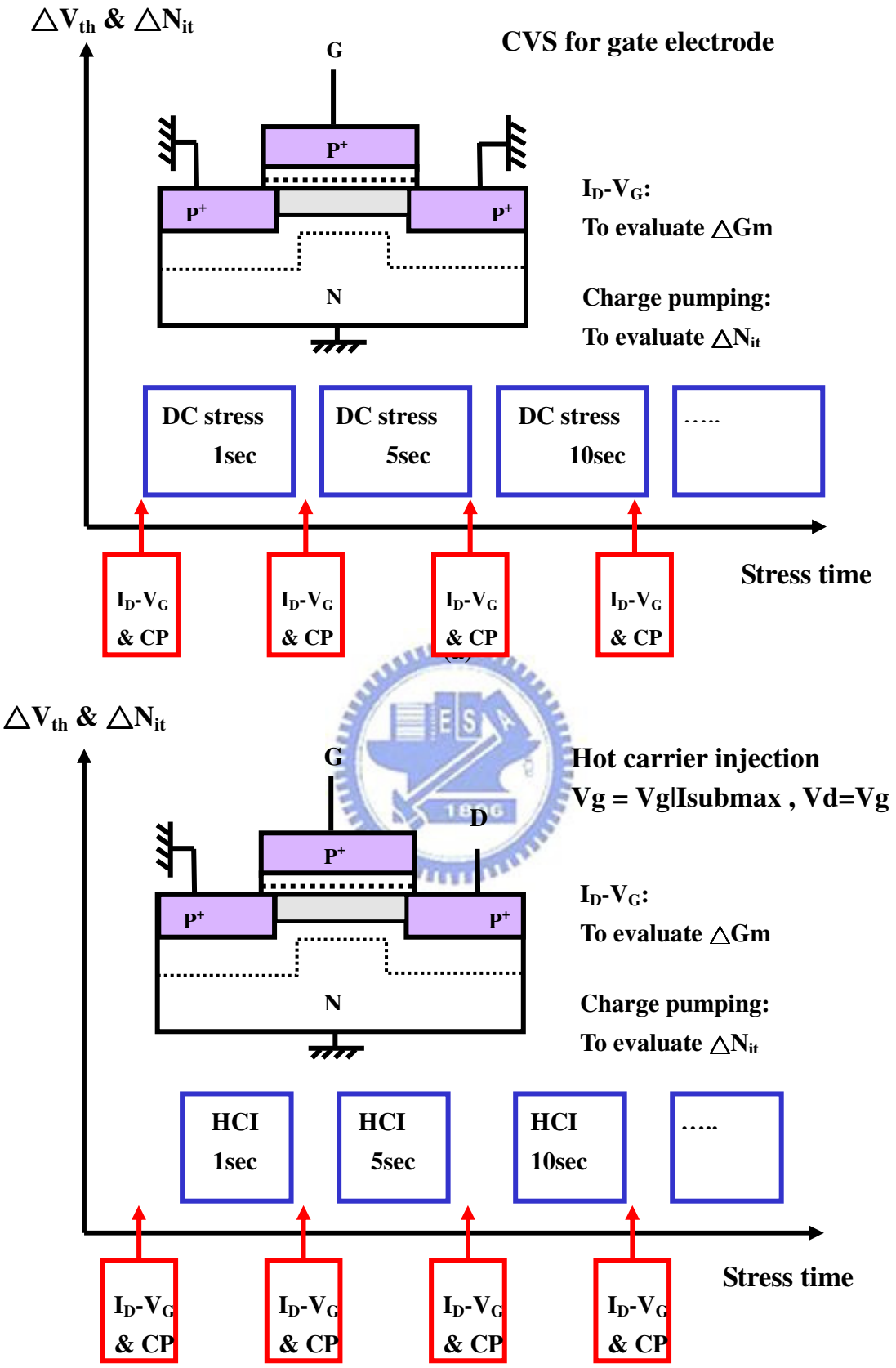
As the channel length shrinks very quickly, the deterioration after hot carrier injection represents one of the most reliability limit. Although hot carrier effect of PMOSFET is smaller than NMOSFET, we could compare the element reliability between oxide and oxynitride. Fig 3-8reveals Isub current versus gate voltage with different channel length. It is clear that the substrate current increase as channel length reduces. Besides, it have been demonstrated that the worst hot-carrier condition varies from Vg = Vd/4 to Vg=Vd. Thus we easily try two conditions Vg= Isub|max and Vg=Vd to obtain the most serious degradation. Fig 3-9(a) and Fig.3-9(b) shows the result with different HCI conditions. The larger degradation of PMOSFET happens at Vg= 1/4Vd. This condition is different from NMOSFET. The larger degradation of NMOSFET usually happens at Vg=1/3Vd. For PMOSFET, we attain larger threshold voltage shift and huge interface state variations at Vg =1/4 Vd condition. Fig.3-10 shows oxynitride suffers hot-carrier-injection in worse case Vg=1/4Vd, and obtains long lifetime.

Besides, Fig 3-11(a) and Fig.3-11(b) shows the comparison HCI with CVS. Both the

larger shift of threshold voltage and interface state for PMOSFET during HC stress are compared to CVS stress. This phenomenon is attributed to the damage by the injection of holes into the oxide during HC injection and CVS stress. [] It hints that the effective mass of hole is lager than electron. So the degradation of gate oxide for PMOSFET is more serious than NMOSFET. This is why less threshold voltage shift obtains with CVS.

3-3-3 Summary

From SILC and HCI characteristics, we can find the film of oxynitride is more robust. And gate oxide failure is shown to be dependent on the limiting factor for the scaling of oxide thickness. Because oxynitride has the higher dielectric constant, we can reduce the leakage current c for oxynitride as the same EOT (equivalent oxide thickness). And oxynitride has lower shift of threshold voltage and interface state than oxide which device operates on CVS or HCL .Owing to its significant reduction of lower leakage current and other reliability issues, it has been proved that oxynitride can extend the scaling limit of SiO_2 in terms of dielectric reliability as well as stand-by power consumption. Again, this implies that this new process can provide a high-quality gate dielectric film.



(b)

Fig 3-1 Basic measurement method for (a) CVS (b)HCI

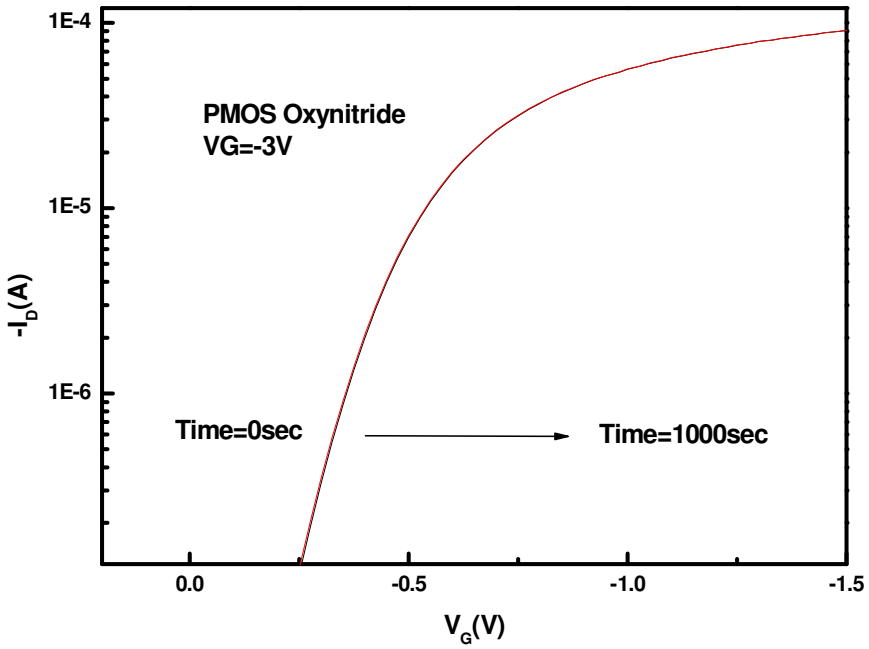


Fig.3-2(a) I_d-V_g characteristics for p^+-gate pMOSFETs before stress and after stress 1000 s at 25 ^oC with oxynitride.

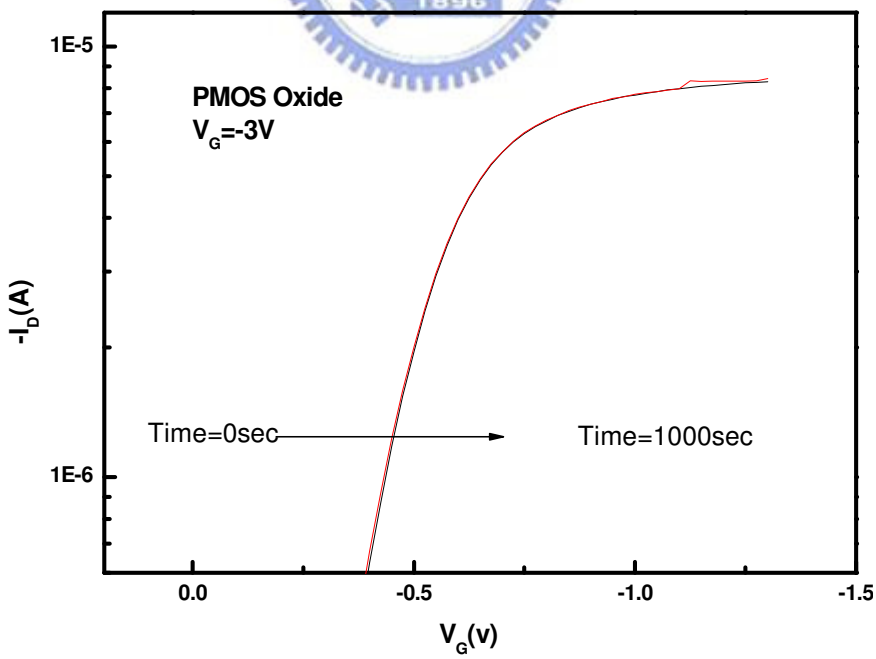
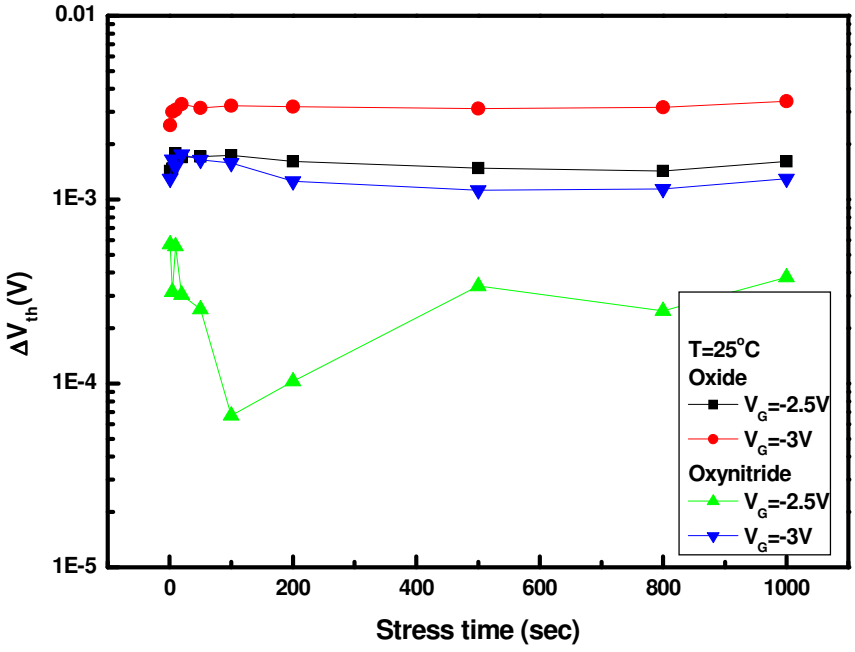
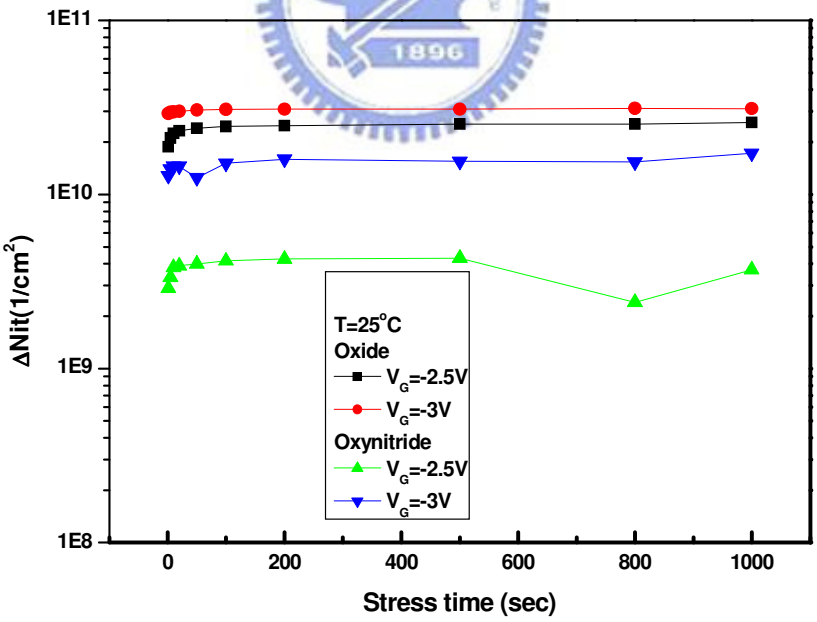


Fig.3-2(b) I_d-V_g characteristics for p^+-gate pMOSFETs before stress and after stress 1000 s at 25 ^oC with conventional oxide.

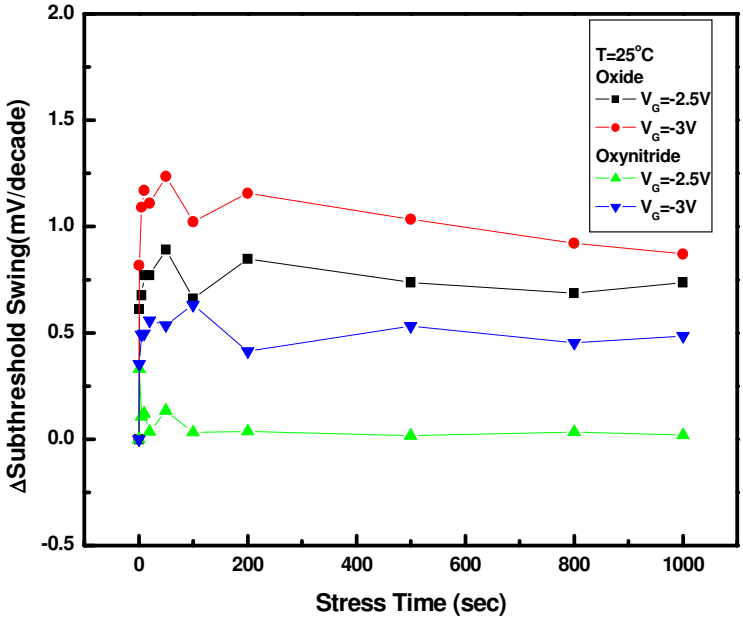


(a)

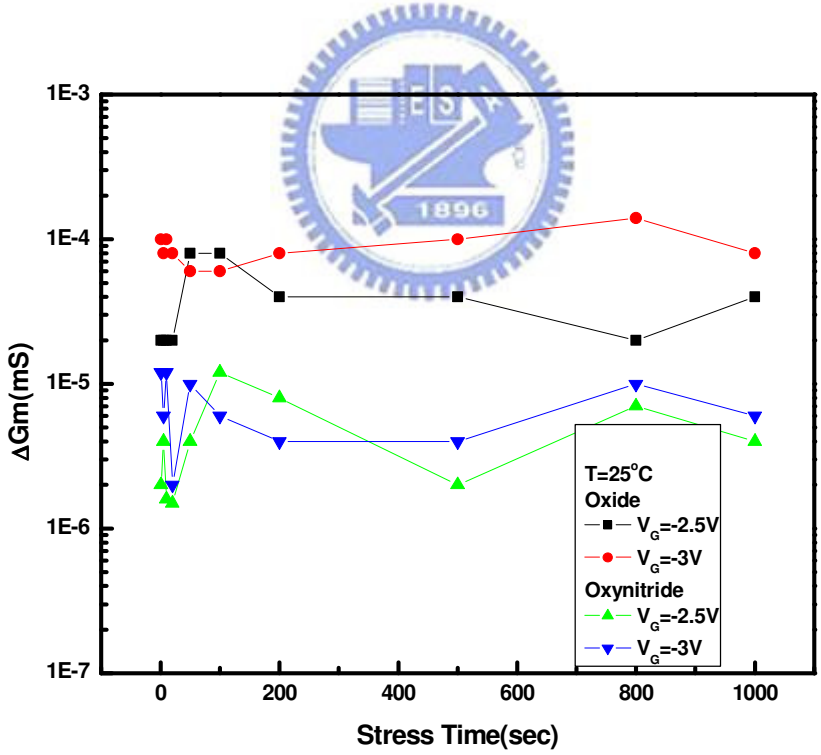


(b)

Fig.3-3 (a) Threshold voltage shift , and (b) Interface trap density shift as a function of stress time which compares oxynitride with oxide.

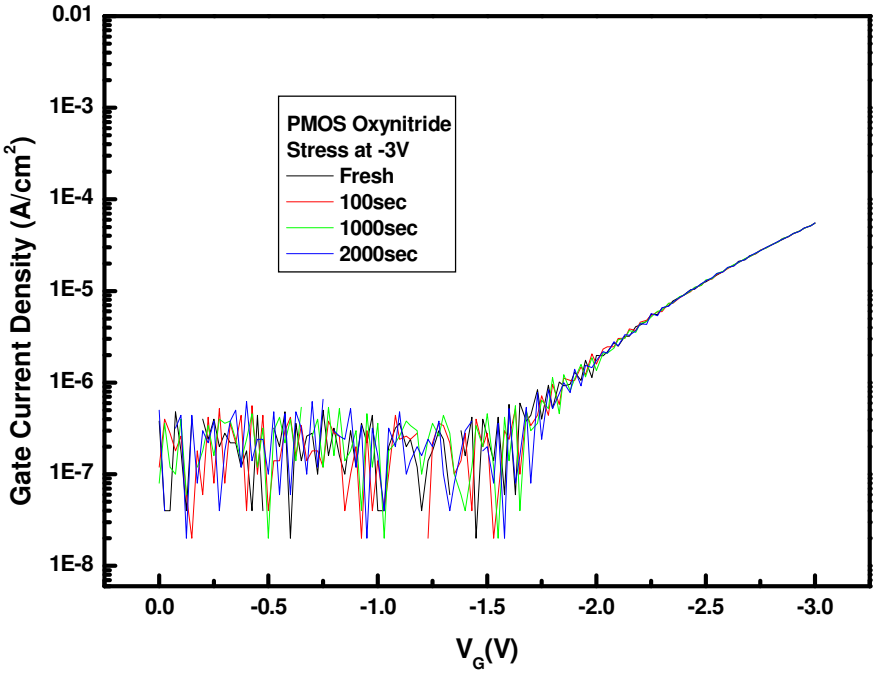


(a)

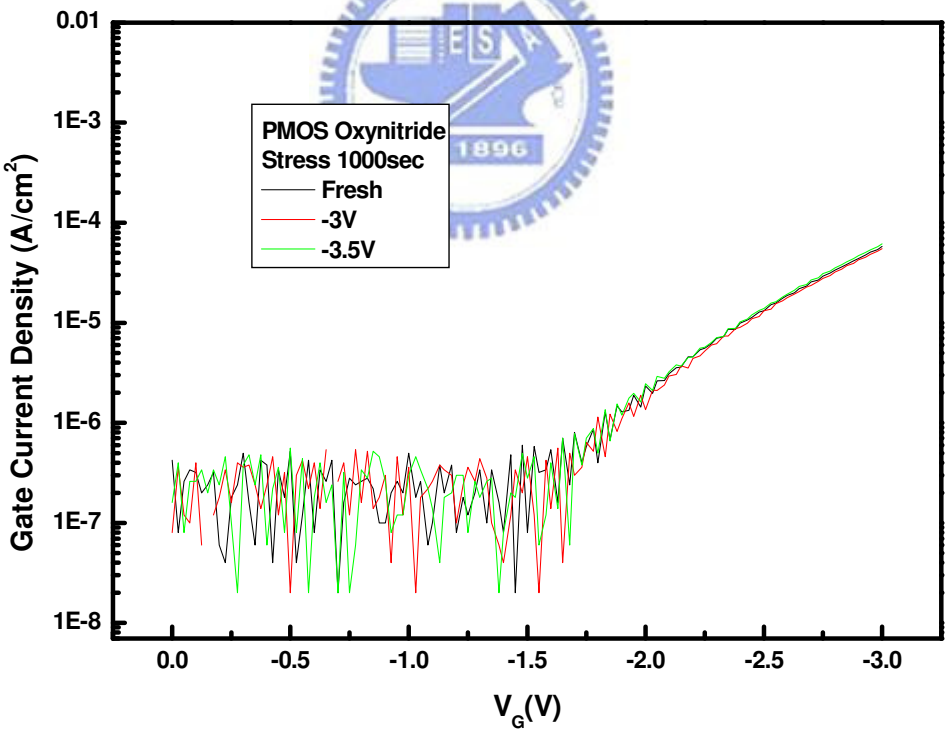


(b)

Fig.3-4 (a) subthreshold swing shift , and (b) transconductance shift as a function of stress time which compares oxynitride with oxide.

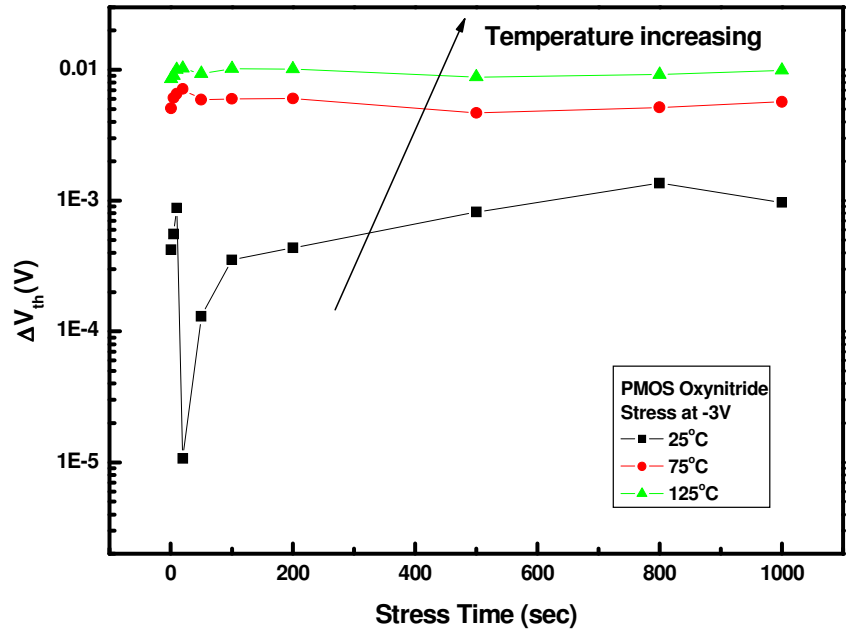


(a)

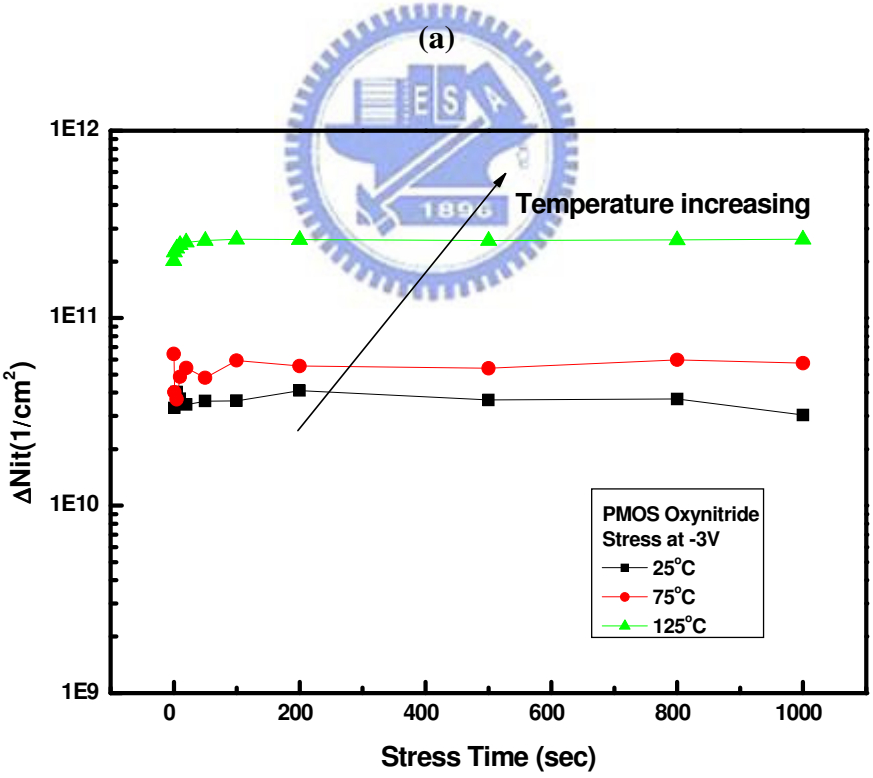


(b)

Fig.3-5 SILC under constant voltage stress during different (a) voltage stress and (b) time stress for oxynitride film.



(a)



(b)

Fig.3-6 (a) Threshold voltage shift , and (b) Interface trap density shift with different temperature in oxynitride.

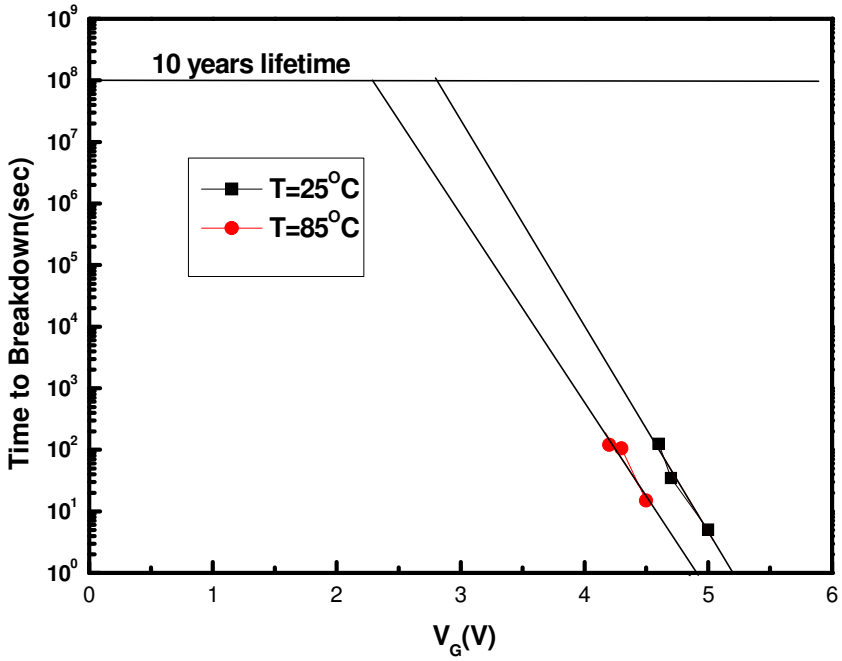


Fig.3-7 Comparison of intrinsic lifetime projection for oxynitride film in different temperature.

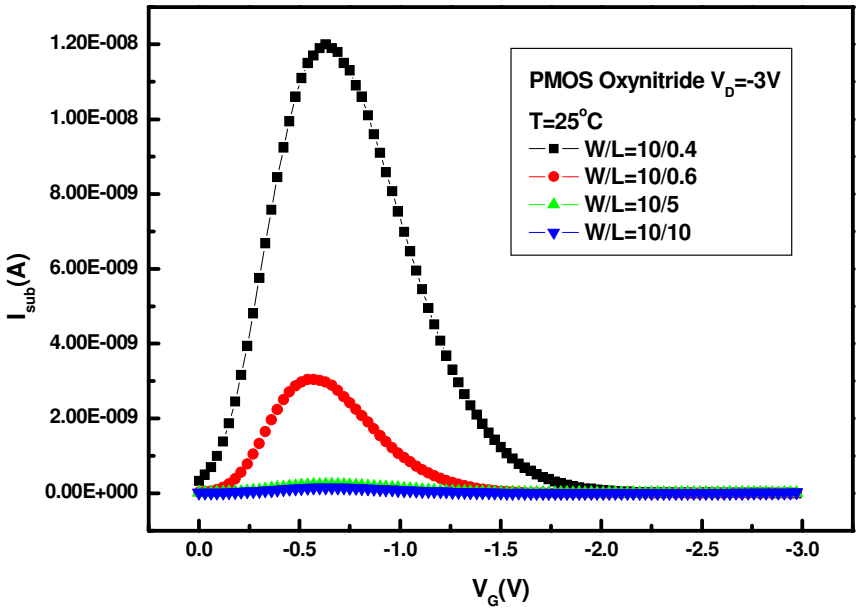
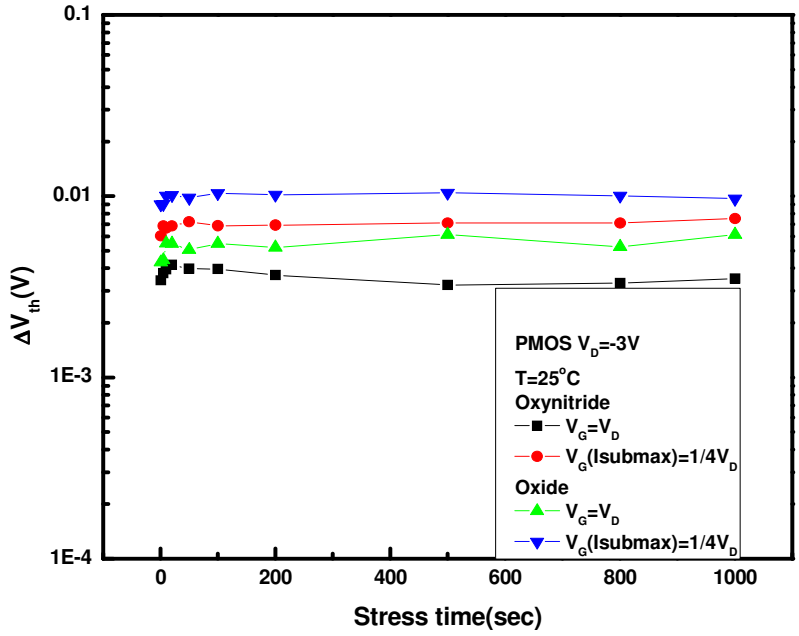
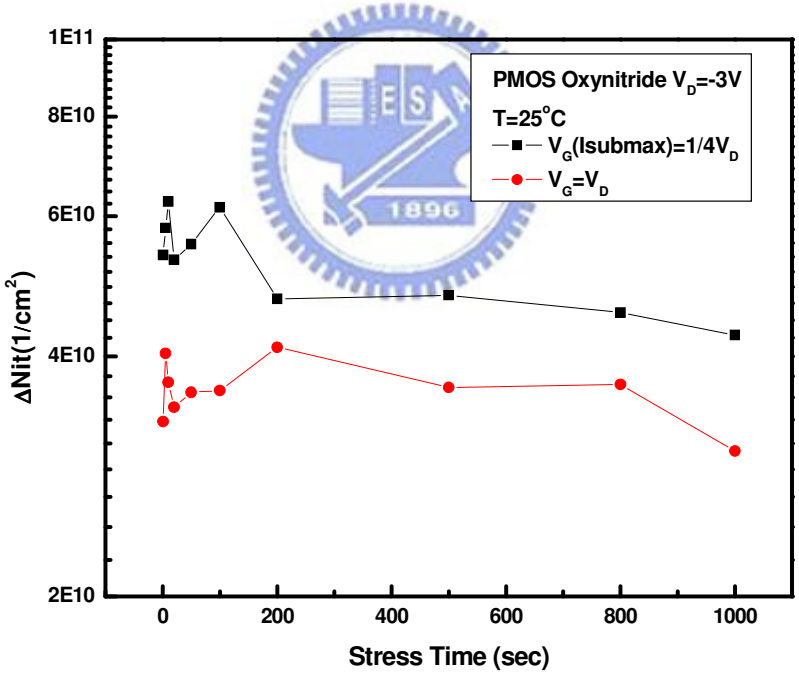


Fig.3-8 Substrate current versus gate voltage with channel lengths of 10um , 5um , 0.6um and 0.4um.



(a)



(b)

Fig.3-9 (a) Threshold voltage shift, and (b) Interface trap density shift with different HCI methods.

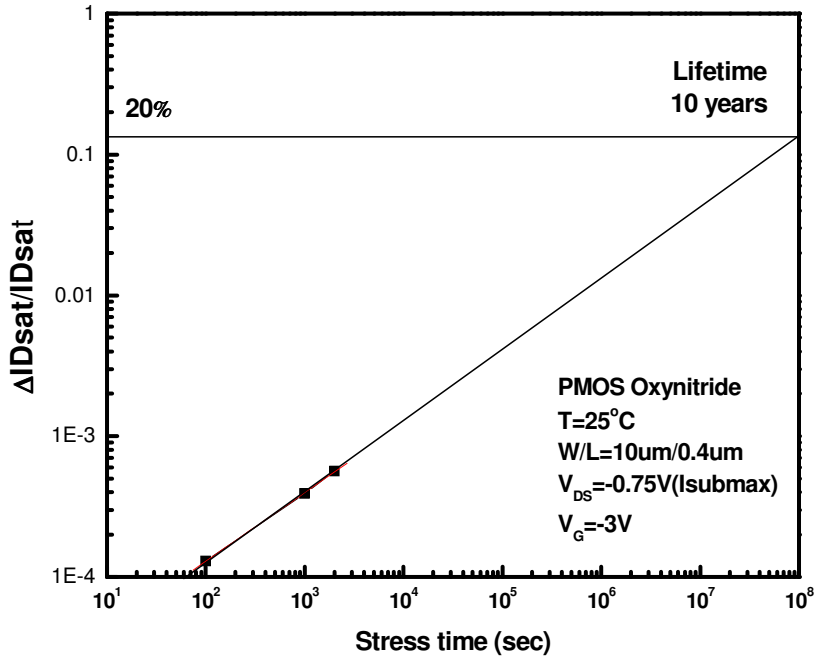
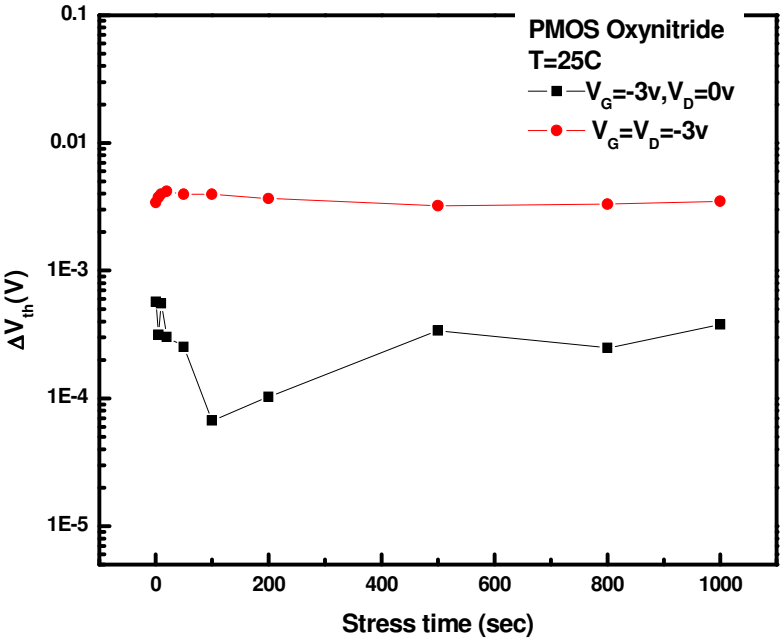
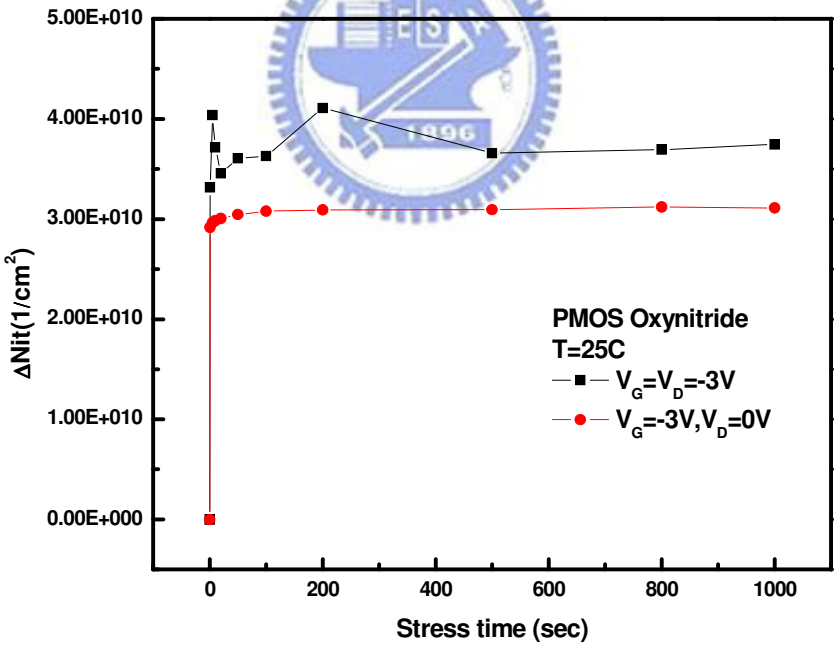


Fig.3-10 HCI lifetime for oxynitride.



(a)



(b)

Fig.3-11(a)Threshold voltage shift, and (b) Interface trap density shift as a function of stress time which compares HCI with CVS.

Chapter 4

Conclusions

The continuous shrinkage in MOSFET dimension has engendered a concomitant scaling in gate dielectrics to provide satisfactory circuit performance at low voltage. However, the continuous reduction of the gate-oxide layer thickness in advanced CMOS device leads to excessive gate leakage currents and reliability problem So we must find new materials to replace traditional silicon oxide. In this thesis, it is believed that oxynitride is a good candidate. And then oxynitrides with high nitrogen content distributed close to the surface has been proven to be the best candidates for 65 nm CMOS integration or below. An alternative approach to form a high-nitrogen ultrathin oxynitride gate dielectric is demonstrated. The oxynitride growth included three process stages – chemical oxide growth, nitridation and subsequent dry oxidation. Meanwhile, chemical oxide as a starting oxide can provide a better control ability in film thickness. Following that, the chemical oxide was nitrided using a furnace in low-pressure NH_3 ambient to transfer high-nitrogen oxynitride. The nitrided chemical oxide was then placed in an atmospheric O_2 ambient to form a robust oxynitride. And we can reduce nitrogen concentration at oxide/silicon interface. Therefore mobility of device will be improved. Furthermore we can put the highest nitrogen concentration at poly/oxide interface. The boron penetration will be retrained.

The process proposed here is simple and fully compatible with current process technology.

Finally, by this technique, pMOSFET of oxynitride were fabricated to study electrical characteristics. These devices demonstrate excellent properties in terms of better growth control, high driving capability, high endurance in stressing, superior boron diffusion blocking behavior and weak SILC effect, also less degradation in CVS effect and good performance in HCI effect.

Chapter 5

Future Work

Less than 3nm gate dielectric with both high drivability and reliability is necessary for realizing high performance CMOS devices. Because nitrogen incorporated oxide can solve these problems, fabrication technology of ultrathin gate dielectrics with high nitrogen concentration is required. Nitridation treatment on ultrathin oxide has been used in MOS technology to strengthen both the dielectrics robustness and electrical stress, meanwhile it also can apply to form high permittivity gate dielectric stacks. Besides, it has its excellent resistance of boron penetration and is a good buffer layer candidate between high-K gate dielectric and Si substrate. There are a number of topics relevant to this thesis, which may deserve further studies. The following topics are suggested for future work:

according to the current results obtained so far, with such good electrical characteristics and reliability properties of oxynitride, it manifests a high competence for a number of applications to deep submicrometer. Among them are the following:

(1) Application of the interfacial layer between high-k and substrate:

High-nitrogen oxynitride has both the ability to withstand the penetration of the oxygen atoms and low density of interface state (D_{it}). For certain high-K materials such as HfO_2 and ZrO_2, they suffer the oxygen atom outdiffusion into substrate during

deposition. Hence, this problem can be improved if oxynitride film can be inserted in between. That is, we grow the oxynitrde film first before the formation of the HfO_2 and ZrO_2. Then, the HfO_2/oxynitride and ZrO_2/oxynitride films will have a large possibility to optimize these high-K materials.

(2) Application of SONOS button oxide:

For Polysilicon-blocking Oxide-silicon Nitride-tunneling Oxide-Silicon (SONOS), one of the mechanisms to degrade the ability of charge retention is by trap to trap tunneling (TTT), which means that electron stored in nitride trap directly tunnel through the tunnel oxide to silicon substrate via the interface state. By our technique, oxynitride with D_{it} could improve the charge retention of SONOS.

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New Advanced Process of Ultrathin Oxynitride on the Characteristics of pMOSFET