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碩 士 論 文

釩摻雜與快速熱退火應用於以濺鍍法製備之鋯酸鍶記憶體元件電阻轉換特性研究

Effects of Vanadium Doping and Rapid Thermal Annealing on Sputter-Deposited $SrZrO_3$ Resistive Switching Memory Device

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摘要

本論文利用鈣鈦礦結構材料（鋯酸鍶）作為電阻式記憶體的材料，首先將介紹新世代非揮發性記憶體之應用、特性以及優點，也將探討各種可能的電阻轉換機制及傳導機制。在實驗的部分，我們利用射頻磁控濺鍍法製備純鋯酸鍶與釩摻雜鋯酸鍶薄膜作為轉換電阻層，且利用此濺鍍法沉積鎳酸鑭作為幫助鋯酸鍶成長優選方向之緩衝層，底電極白金及頂電極鋁則利用蒸鍍法製備，形成一頂電極/電阻層/緩衝層/底電極的結構。首先，將探討釩摻雜對鋯酸鍶薄膜轉態特性之影響，我們製作不同濃度釩摻雜的鋯酸鍶記憶體元件，發現釩摻雜有助於穩定電阻轉換特性，更進一步由實驗結果及佐證來探討可能的電阻轉換機制。第二部份將鋯酸鍶薄膜利用快速熱退火改善其電阻轉換特性並趨於穩定，其中以氧氣在攝氏 600 度進行熱退火可使元件具有穩定的電阻轉換特性，同時也比較及探討不同快速熱退火條件對記憶體元件特性的影響，包含不同熱退火溫度、不同熱退火時間及不同熱退火氣體，由實驗結果推測以氧氣進行快速熱退火可修補鋯酸鍶薄膜中的缺陷，進而穩定電阻轉換特性。

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Abstract

In this thesis, the RRAM devices manufactured based on $SrZrO_3$ (SZO) thin films are studied and developed. At first, I will introduce the applications, fundamental characteristics, and advantages of next-generation nonvolatile memories. The conduction mechanisms of RRAM that have been published are also discussed. In experimental details, pure-SZO and V doped SZO film was deposited on the $LaNiO_3$ buffer layer by RF magnetron sputter. Pt and Al act as bottom electrode and top electrode, respectively. Therefore, electrode/resistive thin film/buffer layer/electrode structure is formed. First, we will discuss the influence of V-doping effect. We fabricate different V-dopant concentration SZO memory devices. The switching property can be stabilized by V-doping. We confer the resistive switching mechanism by experiment results and proofs. Second, we use thermal treatment to improve and stabilize the switching property by rapid thermal annealing (RTA) on SZO film. The SZO memory device has the stable switching property by RTA at 600℃ with O_2. The effects of resistive switching property by different RTA conditions are also compared and discussed. The RTA conditions include different RTA temperature, different RTA time and different RTA gas. We conjecture that the defects of SZO film can be repaired by RTA with O_2. Then, the switching property can be stabilized.

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Chapter 1

Introduction

1.1 Introduction to Memories

Memory can be classified into two main categories, volatile and nonvolatile memory (NVM). First, the volatile memory will be introduced, including dynamic random access memory and static random access memory. And then, many kinds of nonvolatile memories such as read only memory (ROM), programmable ROM (PROM), EPROM, EEPROM, flash memory, phase-change memory, ferroelectric random access memory, magnetoresitive random access memory, and resistance random access memory will be mentioned in this section.

1.1.1 Volatile Memory

Volatile memory is computer memory that requires power to remain the stored information. Most types of random access memory (RAM) are in this category. RAM can be subdivided into two main groups, static RAM (SRAM) and dynamic RAM (DRAM). The difference between them is that the stored information of DRAM memory disappears from the memory within milliseconds, so it has to be refreshed periodically. This makes the operation speed of DRAM much slower than that of SRAM.

I. Dynamic Random Access Memory

Short for Dynamic Random Access Memory, DRAM is one of the most commonly found memory modules in PC compatible personal

computers and workstations. DRAM stores its information in a cell containing a capacitor and transistor. It stores each bit of data in a separate capacitor within an integrated circuit. Since real capacitors leak charge, the information eventually fades unless the capacitor charge is refreshed periodically. Because of this design, these cells must be refreshed with new electricity every few milliseconds allowing the memory to keep its charge and hold the data as long as needed. When using this type of memory, if the computer is powered off, the information within memory will be lost.

Fig. 1-1 shows a simple example with only 4 by 4 cells (modern DRAM can be thousands of cells in length/width). The long lines connecting each row are known as word lines. Each column is actually composed of two bit lines, each one connected to every other storage cell in the column. They are generally known as the + and − bit lines. A sense amplifier is essentially a pair of cross-connected inverters between the bit lines. That is, the first inverter is connected from the + bit line to the − bit line, and the second is connected from the − bit line to the + bit line. This is an example of positive feedback, and the arrangement is only stable with one bit line high and one bit line low.

Typically, manufacturers specify that each row should be refreshed every 64 ms or less, according to the JEDEC (Foundation for developing Semiconductor Standards) standard. Refresh logic is commonly used with DRAMs to automate the periodic refresh. This makes the circuit more complicated, but this drawback is usually outweighed by the fact that DRAM is much cheaper and of greater capacity than SRAM. Some systems refresh every row in a tight loop that occurs once every 64 ms. Other

systems refresh one row at a time -- for example, a system with $2^{13} = 8192$ rows would require a refresh rate of one row every 7.8 µs (64 ms / 8192 rows). A few real-time systems refresh a portion of memory at a time based on an external timer that governs the operation of the rest of the system, such as the vertical blanking interval that occurs every 10 to 20 ms in video equipment. All methods require some sort of counter to keep track of which row is the next to be refreshed. Some DRAM chips include that counter; other kinds require external refresh logic to hold that counter.

II. Static Random Access Memory

Static random access memory (SRAM) is a type of semiconductor memory where the word static indicates that it, unlike DRAM, does not need to be periodically refreshed, as SRAM uses bistable latching circuitry to store each bit. SRAM exhibits data remanence, but is still *volatile* in the conventional sense that data is eventually lost when the memory is not powered. The term SDRAM, which stands for synchronous DRAM, should not be confused with SRAM.

Fig. 1-2 shows a six-transistor CMOS SRAM cell (6T SRAM). Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations. A typical SRAM uses six MOSFETs to store each memory bit. In addition to such 6T SRAM, other kinds of SRAM chips use 8T, 10T, or more transistors per bit -- sometimes to implement more ports in a register file.

Access to the cell is enabled by the word line (WL in fig. 1-2) which controls the two access transistors M_5 and M_6 which, in turn, control whether the cell should be connected to the bit lines: BL and BL. They are used to transfer data for both read and write operations. While it's not strictly necessary to have two bit lines, both the signal and its inverse are typically provided since it improves noise margins.

During read accesses, the bit lines are actively driven high and low by the inverters in the SRAM cell. This improves SRAM speed compared to DRAMs—in a DRAM, the bit line is connected to storage capacitors and charge sharing causes the bitline to swing upwards or downwards. The symmetric structure of SRAMs also allows for differential signalling, which makes small voltage swings more easily detectable. Another difference with DRAM that contributes to making SRAM faster is that commercial chips accept all address bits at a time. By comparison, commodity DRAMs have the address multiplexed in two halves, i.e. higher bits followed by lower bits, over the same package pins in order to keep their size and cost down. The size of an SRAM with m address lines and n data lines is 2^m words, or $2^m \times n$ bits.

SRAM is a little more expensive, but faster and significantly less power hungry (especially idle) than DRAM. It is therefore used where either speed or low power, or both, are principle considerations. SRAM is also easier to control (interface to) and generally more truly random access than modern types of DRAM. Due to a more complex internal structure, SRAM is less dense than DRAM and is therefore not used for high-capacity, low-cost applications such as the main memory in personal computers.

1.1.2 Nonvolatile Memory

Nonvolatile memory (NVM) is computer memory that can retain the stored information even when not powered. The first NVM is floating-gate nonvolatile memory. Kahng and Sze proposed the first floating gate device in 1967 [1].

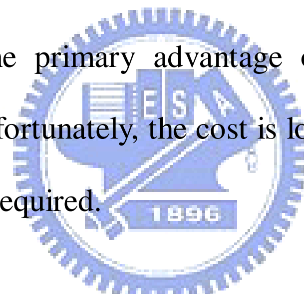
In floating gate memory devices, charge or data is stored in the floating gate and is retained when the power is removed. All floating gate memories have the same generic cell structure. They consist of a stacked gate MOS transistor as shown in Fig. 1-3 [1]. The first gate is the floating gate that is buried within the gate oxide and the inter-polysilicon dielectric (IPD) beneath the control gate. The IPD isolates the floating gate and can be oxide or oxide-nitride-oxide (ONO). The SiO_2 dielectric surrounding the transistor serves as a protective layer from scratches and defects. The second gate is the control gate which is the external gate of the memory transistor. Floating gate devices are typically used in electrically programmable read only memory (EPROM), electrically erasable and programmable read only memory (EEPROM), and Flash memory. The disadvantages of NVM are low operation speed, high operation voltage, poor endurance, and its congenital limit in size due to gate oxide thinning that causing poor retention.

NVM has been widely used to manufacture a broad range of products found in MCU, DSP, smart card, cellular communications, automotive, CPLD, and many personal digital assistant. A perfect NVM should have the properties including low operation voltage, simple structure, low power consumption, non-destructive readout, high operation speed, long retention time, high endurance, and small cell size. Up to now, there are many sorts of nonvolatile

memories. Such as read only memory (ROM), programmable ROM (PROM), EPROM, EEPROM, flash memory, phase-change memory, ferroelectric random access memory, magnetoresistive random access memory, and resistance random access memory.

I. Read Only Memory

The very first ROMs are hardwired devices that contain a preprogrammed set of data or instructions. The contents of the ROM have to be specified before chip production, so the actual data can be used to arrange the transistors inside the chip. Hardwired memories are still used, though they are now called masked ROMs to distinguish them from other types of ROM. The primary advantage of a masked ROM is its low production cost. Unfortunately, the cost is low only when large quantities of the same ROM are required.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II. Programmable Read Only Memory

A programmable read-only memory (PROM) or field programmable read-only memory (FPROM) is a form of digital memory where the setting of each bit is locked by a fuse or antifuse. Such PROMs are used to store programs permanently. The key difference from a strict ROM is that the programming is applied after the device is constructed. They are frequently seen in video game consoles, or such products as electronic dictionaries, where PROMs for different languages can be substituted.

III. Erasable and Programmable Read Only Memory

An EPROM is a type of computer memory chip that retains its data when its power supply is switched off. In other words, it is non-volatile. It is an array of floating-gate transistors individually programmed by an electronic device that supplies higher voltages than those normally used in electronic circuits. Once programmed, an EPROM can be erased only by exposing it to strong ultraviolet light. That UV light usually has a wavelength of 235nm (for optimum erasure time) and belongs to the UVC range of UV light. EPROMs are easily recognizable by the transparent fused quartz window in the top of the package, through which the silicon chip can be seen, and which permits UV light during erasing.

IV. Electrically Erasable and Programmable Read Only Memory

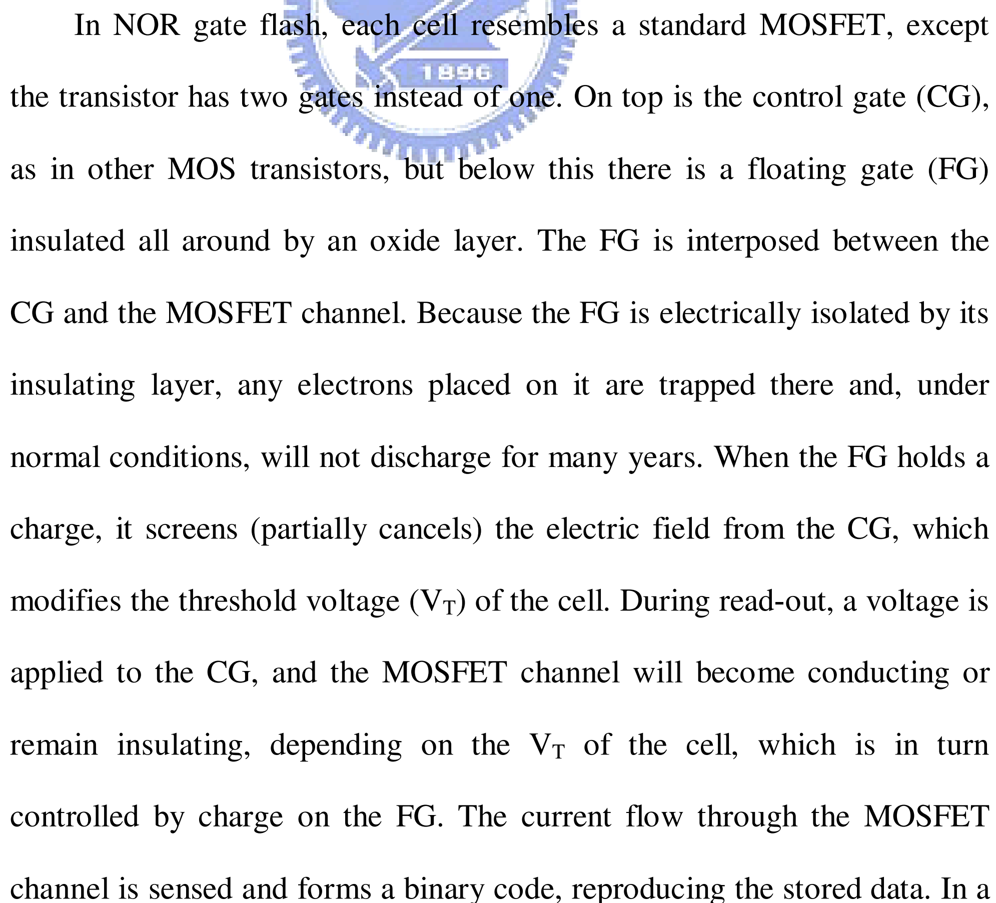
EEPROM's have the advantage of being able to selectively erase any part of the chip without the need to erase the entire chip and without the need to remove the chip from the circuit. While an erase and rewrite of a location appears nearly instantaneous to the user, the write process is slightly slower than the read process; the chip can be read at full system speeds.

The limited number of times a single location can be rewritten is usually in the 10000-100000 range; the capacity of an EEPROM also tends to be smaller than that of other non-volatile memories. Nonetheless, EEPROMs are useful for storing settings or configuration for devices ranging from dial-up modems to satellite receivers.

V. Flash Memory

Flash memory is non-volatile computer memory that can be electrically erased and reprogrammed. It is a technology that is primarily used in memory cards and USB flash drives for general storage and transfer of data between computers and other digital products.

Flash memory stores information in an array of memory cells made from floating-gate transistors. In traditional single-level cell (SLC) devices, each cell stores only one bit of information. Some newer flash memory, known as multi-level cell (MLC) devices, can store more than one bit per cell by choosing between multiple levels of electrical charge to apply to the floating gates of its cells.



In NOR gate flash, each cell resembles a standard MOSFET, except the transistor has two gates instead of one. On top is the control gate (CG), as in other MOS transistors, but below this there is a floating gate (FG) insulated all around by an oxide layer. The FG is interposed between the CG and the MOSFET channel. Because the FG is electrically isolated by its insulating layer, any electrons placed on it are trapped there and, under normal conditions, will not discharge for many years. When the FG holds a charge, it screens (partially cancels) the electric field from the CG, which modifies the threshold voltage (V_T) of the cell. During read-out, a voltage is applied to the CG, and the MOSFET channel will become conducting or remain insulating, depending on the V_T of the cell, which is in turn controlled by charge on the FG. The current flow through the MOSFET channel is sensed and forms a binary code, reproducing the stored data. In a

multi-level cell device, which stores more than one bit per cell, the amount of current flow is sensed (rather than simply its presence or absence), in order to determine more precisely the level of charge on the FG.

NAND gate flash uses tunnel injection for writing and tunnel release for erasing. NAND flash memory forms the core of the removable USB interface storage devices known as USB flash drives, as well as most memory card formats available today.

Flash memory costs far less than byte-programmable EEPROM and therefore has become the dominant technology wherever a significant amount of non-volatile, solid-state storage is needed. Examples of applications include PDAs (personal digital assistants) and laptop computers, digital audio players, digital cameras and mobile phones. It has also gained popularity in the game console market, where it is often used instead of EEPROMs or battery-powered SRAM for game save data.

VI. Phase-change Memory

Phase-change memory (also known as PCM, PRAM, PCRAM, Ovonic Unified Memory and Chalcogenide RAM C-RAM) is a type of non-volatile computer memory. PRAM uses the unique behavior of chalcogenide glass, which can be "switched" between two states, crystalline and amorphous, with the application of heat. Recent versions can achieve two additional distinct states, effectively doubling its storage capacity. The properties of chalcogenide glasses were first explored as a potential memory technology by Stanford Ovshinsky of Energy Conversion Devices in the 1960s. In the September 1970 issue of Electronics, Gordon Moore—co-founder of

Intel—published an article on the technology.

The crystalline and amorphous states of chalcogenide glass have dramatically different electrical resistivity, and this forms the basis by which data are stored. The amorphous, high resistance state is used to represent a binary 0, and the crystalline, low resistance state represents a 1. Chalcogenide is the same material used in re-writable optical media (such as CD-RW and DVD-RW). In those instances, the material's optical properties are manipulated, rather than its electrical resistivity, as chalcogenide's refractive index also changes with the state of the material.

Here the write-read-erase-cycle is affected by an electrical pulse. Figs. 1-4 and 1-5 show the schematic cross section of a PCRAM cell and the corresponding current-voltage curves. The cell is essentially a nonlinear resistor and the readout is performed at low bias (Read region indicated in Fig. 1-5), where the low-field resistance changes by orders of magnitude depending on whether the phase change material in the active region of the device is crystalline or amorphous. To reach the switching regions (SET and RESET shown in Fig. 1-5) the bias is raised above the switching voltage so that enough current can flow through the cell, heating up the active region (Fig. 1-4) resulting in the crystalline-amorphous phase change [10], [11]. At present several manufacturers of RAM chips have initiated research and development projects to explore and use the potential of nonvolatile storage with phase change materials.

Although PRAM has not yet reached the commercialization stage for consumer electronic devices, nearly all prototype devices make use of a

chalcogenide alloy of germanium, antimony and tellurium (GeSbTe) called GST. It is heated to a high temperature (over 600°C), at which point the chalcogenide becomes a liquid. Once cooled, it is frozen into an amorphic glass-like state and its electrical resistance is high. By heating the chalcogenide to a temperature above its crystallization point, but below the melting point, it will transform into a crystalline state with a much lower resistance. This phase transition process can be completed in as quickly as five nanoseconds, according to a January 2006 Samsung Electronics patent application concerning the technology. This is comparable to conventional volatile memory devices, for instance, modern DRAM cells have a switching time on the order of two nanoseconds.

A more recent advance pioneered by Intel and ST Microelectronics allows the material state to be more carefully controlled, allowing it to be transformed into one of four distinct states; the previous amorphic or crystalline states, along with two new partially crystalline ones. Each of these states has different electrical properties that can be measured during reads, allowing a single cell to represent two bits, doubling memory density. [2]

VII. Ferroelectric Random Access Memory

Ferroelectric materials are generally defined by reversible spontaneous polarization in the absence of electric field [3]. The spontaneous polarization is generated from noncentrosymmetric arrangement of ions in unit cell, which produces an electric dipole moment related to the unit cell. Adjacent unit cells are inclined to polarize in the same direction and form a region called a ferroelectric domain. Unit cell of typical ferroelectric material, ABO_3, is illustrated in Fig. 1-6 [4] where A atom, B atom, and

oxygen occupy the corner site, body-centered site, and face-centered site, respectively. The ferroelectric materials exhibit a characteristic hysteresis loop as shown in Fig. 1-7 [4]. When an electrical field is applied to the ferroelectric material, the B atom, which has two thermodynamically stable positions inside oxygen octahedra, is displaced relative to the oxygens upward or downward, depending on the polarity of the electric field. This displacement generates a dipole moment inside the oxygen octahedra, which is called as saturated polarization ($\pm P_s$). When the applied electric field is removed, the B atom remains in the displaced position and generates a residual polarization in the absence of applied electric field, or remanent polarization ($\pm P_r$). In order to reverse the direction of polarization, it needs to apply a coercive electric field ($\pm E_c$), which is defined as a minimum electric field for switching the polarization. Therefore, the basic characteristics of a ferroelectric material that make it suitable for NVM applications are its ability to retain two stable remanent polarization values at zero fields, thus providing nonvolatility. The state of polarization can be controlled and sensed by reversing the polarization from up (+1) to down (0) or vice versa as a function of applied voltage.

VIII. Magnetoresistive Random Access Memory

In 1988, the physicists found giant magnetoresistance (GMR) effect, and from the effect they learnt the following two things. (1) Spin-dependence scattering can make a significant influence to the total resistance. (2) An interlayer coupling is quite strong between ferromagnetic layers separated by a spacing layer. Thus to investigate the interlayer couplings between ferromagnetic layers across a non-magnetic layer

becomes very interesting. One sort of the investigation is tunneling magnetoresistance (TMR) effect. TMR effect is observed on magnetic tunnel junction (MTJ). A MTJ is a layered structure of magnetic and non-magnetic materials. There are many kinds of MTJs, for instance, ferromagnet/insulator /ferromagnet trilayer junction, spin-valve-type junctions with an exchange-biased layer, double and triple barrier layers junctions and so on. Among the various structures they have a common feature that the spacing layer between the ferromagnetic layers is an insulator.

At room temperature (RT), the change of magnetoresistance in GMR is less than that in TMR, so MTJs are often used as the memory cells in MRAM. In a MTJ, the spacing layer which is an insulator is between two ferromagnetic electrodes. One electrode is free to rotate under the external field and the other creates a powerful pinning field to the magnetic layer in one specific direction.

In writing process, the magnetic moment of the free layer is rotated to be parallel or anti-parallel the pinned layer by controlling the two orthogonal magnetic fields. The resistance of the MTJ is lower when the magnetic moments of the free and pinned layer are parallel than the resistance when the moments are anti-parallel. Thus, the parallel and anti-parallel states are arbitrary chosen to present 0 or 1. In general, 0 is corresponding to the parallel state and 1 is corresponding to the anti-parallel state.

In reading process, by passing the current into a MTJ, a low or high

resistance is obtained to determine what the data is.

IX. Resistive Random Access Memory

Resistive Random Access Memory (RRAM) is a new non-volatile memory type being developed by Sharp, Samsung, Fujitsu, Spansion, Macronix, Winbond and other companies.

Different forms of RRAM have been disclosed, based on different dielectric materials, spanning from perovskites to transition metal oxides to chalcogenides. Even silicon dioxide has been shown to exhibit resistive switching as early as 1967.

The basic idea is that a dielectric, which is normally insulating, can be made to conduct through a filament or conduction path formed after application of a sufficiently high voltage. The conduction path formation can arise from different mechanisms, including defects, metal migration, etc. Once the filament is formed, it may be reset (broken, resulting in high resistance) or set (re-formed, resulting in lower resistance) by an appropriately applied voltage. Recent data suggest that probably many current paths, rather than a single filament, are involved. [8]

1.2 Resistive Random Access Memory

Among new NVMs, such as SONOS, MRAM [12], FeRAM [13], PCRAM [14], and RRAM [15]-[16], RRAM shows superior advantages such as simple device structure, low operation voltage, low power consumption, long retention time, small cell size, high operation speed, low cost, good endurance, and non-destructive readout.

Its resistive switching phenomenon presents two different current values at the same applying voltage. H-state stands for higher current state and the L-state is lower state. The current states of device can be changed by applying a bias voltage or a voltage pulse. Because the resistance ratio of two current states can reach 3~5 orders of magnitude, it is easy to distinguish two current states by applying reading voltage.

1.2.1 The Structure and Operation Method of RRAM

In Fig. 1-8 [16], the RRAM is composed of a transistor and a resistor. In order to write the specific resistor to H-state, a dc voltage is applied on the word line which can turn on the bit transistor and a negative voltage pulse is applied to the bit line while the source of the transistor is grounded in Fig. 1-9 [17]. In order to erase the specific resistor to L-state, a dc voltage is also applied on the word line which can turn on the transistor and a positive voltage pulse is applied on the source of the bit transistor while the bit line is grounded. For the read operation, the word line of the memory cell is selected and a read voltage is applied on the bit line to obtain the current value while the source of the bit transistor is grounded. Therefore, the data comparing the current value with the reference value is determined and do not change the current state of the device during the read operation.

The issue of RRAM is read error. Figs. 1-10(a) and (b) [24] describe how leakage current paths make cell resistance misread. When the resistance is measured with all the unselected lines open, (3,3) cell, for example, has been changed from high to low resistance state after 3 neighboring cells are switched on because of the leakage path described in Fig. 1-10(b). Theoretically this kind of misreading and misprogramming issues can be avoided by proper biasing

method, but the amount of necessary current becomes unreasonably large as memory density increases [25]. Accordingly, it is very important to find suitable rectifying elements to realize an ultra high density cross-point memory device.

1.2.2 Material Groups of RRAM

Resistive switching behaviors have been investigated in PCRAM, doped $SrZrO_3$ (SZO) and $SrTiO_3$ (STO) [17]-[20], binary metal oxide, $Pr_xCa_{1-x}MnO$ (PCMO) [21], and organic material [22], [23], and so on. The resistive switching behavior based on current-induced bistable resistance effect or voltage-controlled negative resistance phenomena has been studied in metal/insulator/metal (MIM) structure. The operation voltage of the PCRAM memory cell is large in order to change the phase between the amorphous phase and the crystalline phase. The application limitation of the PCMO device is that the resistance ratio of two current states is too small to be distinguished. In the aspect of the binary oxide materials, they are still unstable and the resistance ratio is not large enough for application. The resistance switching behaviors also have been reported in the polymer thin film, but it has drawback in stability as well as the binary oxide device.

1.3 Resistive Switching Properties of Doped $SrZrO_3$ Films

In A. Beck's study [16], [19], he declared that the MIM structure device manufactured with 0.2% Cr-doped SZO films as dielectric layer, $SrRuO_3$ (SRO) and Au as bottom and top electrode, respectively has resistive switching behavior. The previous research of our lab also uses (100)-oriented $LaNiO_3$ (LNO) which could enhance the preferred orientation of the SZO films to make 0.2% V-doped SZO films have resistive switching properties [26]. According to Robertsona simulation, Cr, Mn,

Fe, V, Co, Cu transition elements, which could provide over two valences in doped SZO thin films, the density of the defects could be modulated by the doping concentration. In addition, the defects are associated with different valences transformed by the applied voltage. Clearly, slight dopant concentration in SZO thin films could induce resistive switching phenomenon, and the V-doped SZO film had better resistive switching behavior. However, the effect of dopant concentration for V-doped SZO film is still unclear. This is because perovskite oxide consists of more than moments, and it's hard to find optimal recipe to normal manufacturing process because their crystal structure and stoichiometry are hardly controllable.

From the previous research of our lab, V-doped SZO films deposited on LNO/SiO_2/Si substrate have good performance in resistance switching. The resistive switching of Al/V-doped SZO/LNO device can be operated by bias voltage and voltage pulse. However, the drawbacks of Al/V-doped SZO/LNO device are high operation voltage more than 10V.

In this thesis, the physical and electrical properties of the SZO films deposited by sputter method are reported. The SZO film is deposited on the LNO buffer layer, which is also deposited by sputter method. Pt bottom electrode is deposited on Ti/SiO_2/Si substrate by electron beam evaporation method. Ti deposited by E-Gun is acted as adhesion layer for Pt. Al is evaporated as top electrode by thermal coater. The resistive switching phenomenon can be observed in electrode/resistive thin film/buffer layer/electrode (four-layer) structure.

Four-layer structure compared with electrode/resistive thin film/electrode (tri-layer) structure could enhance the forming voltage, the switching voltage, switching speed, and improving the resistance ratio of two current states. Moreover, based on the current-voltage (I-V) curves and resistive switching phenomena, it is proposed the resistive switching mechanism is local property of SZO films. The

conduction mechanisms, reliability, and retention time, are also investigated.

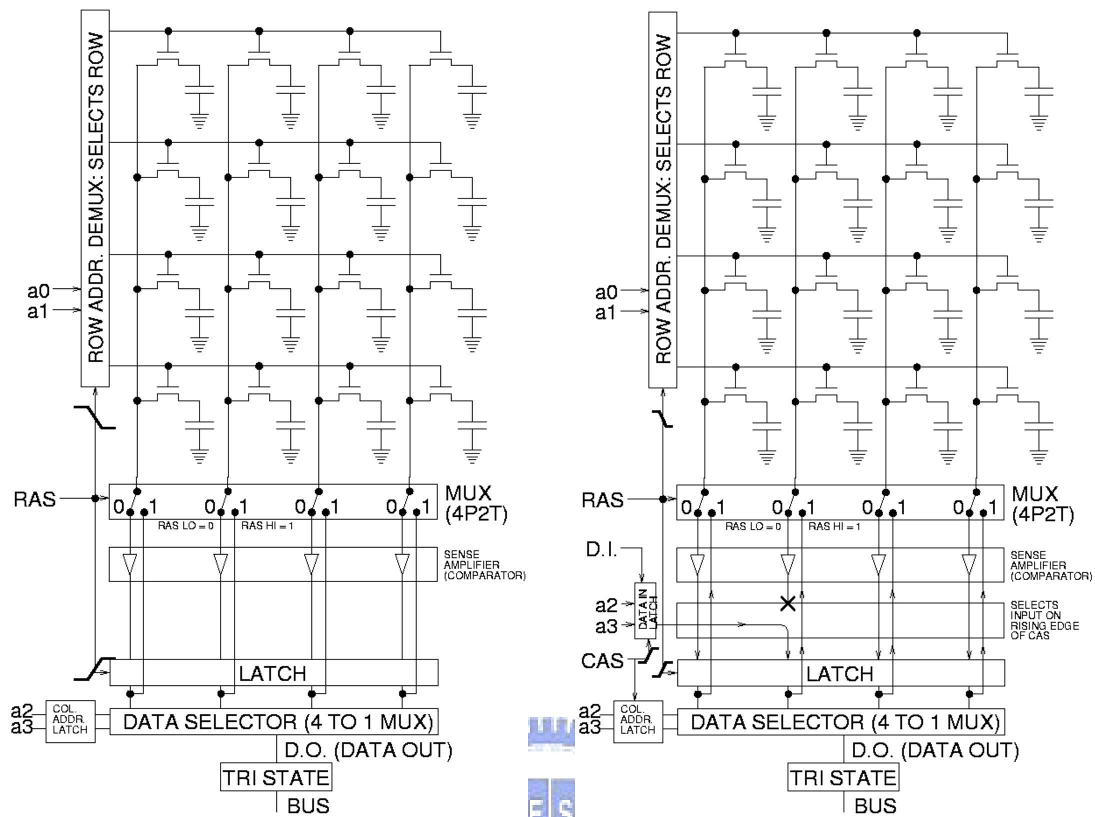


Fig. 1-1 Principle of operation of DRAM read (left) and write (right), for simple 4 by 4 array [5].

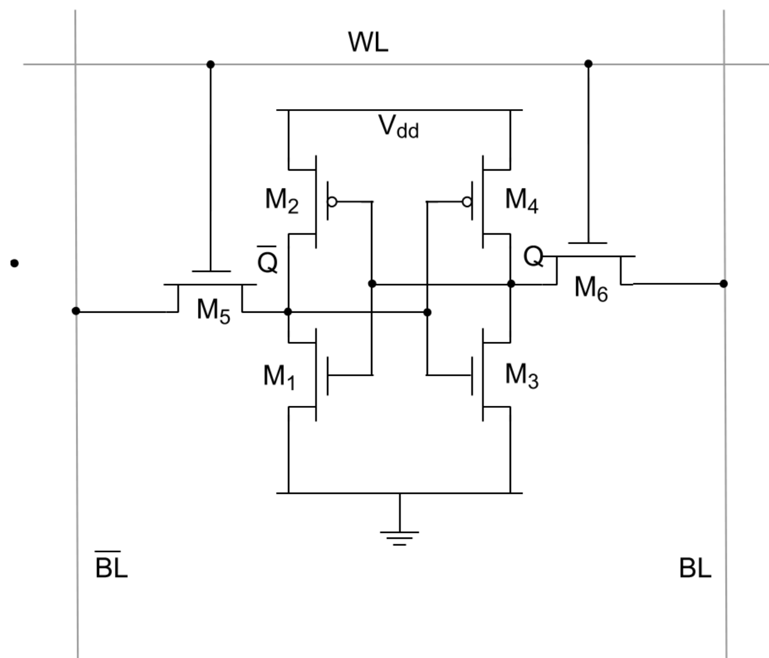


Fig. 1-2 A six-transistor CMOS SRAM cell [6].

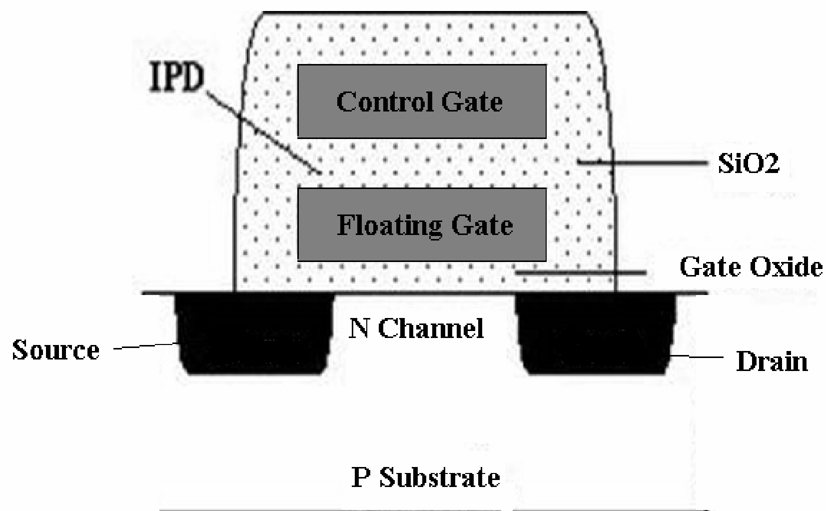


Fig. 1-3 Typical floating gate memory structure.

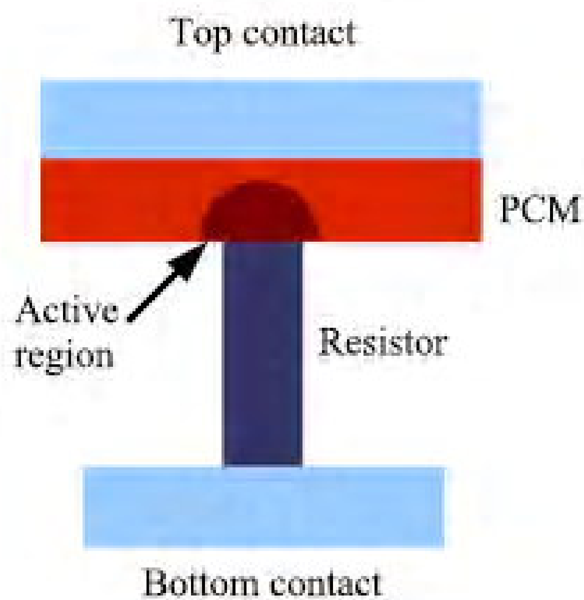


Fig. 1-4 Schematic plot of a PCRAM cell. Depending on the state of the active region (crystalline or amorphous) the resistance of the cell changes by several orders of magnitude.

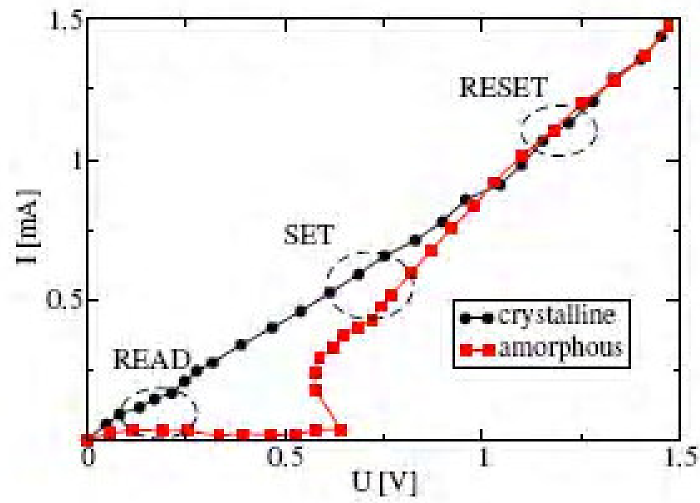


Fig. 1-5 I-V curve of a PCRAM cell. SET and RESET denote the switching regions, while READ denotes the region of readout.

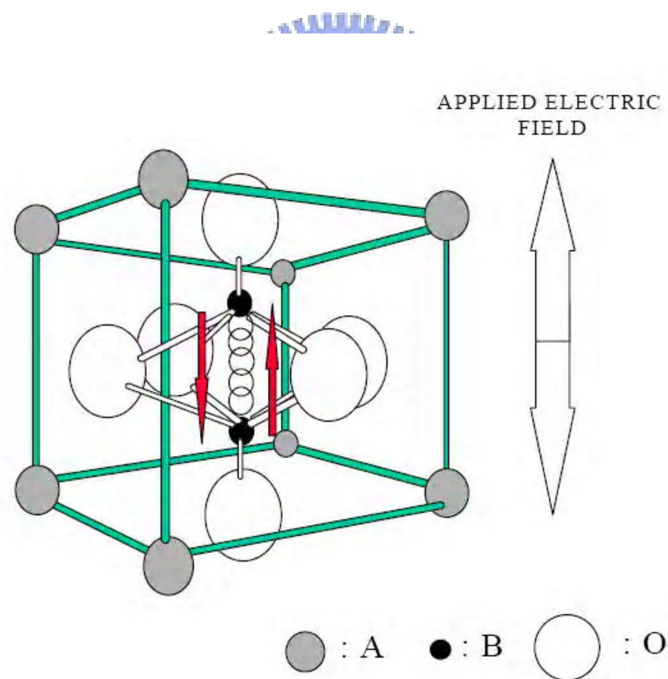


Fig. 1-6 ABO_3 perovskite unit cell [4].

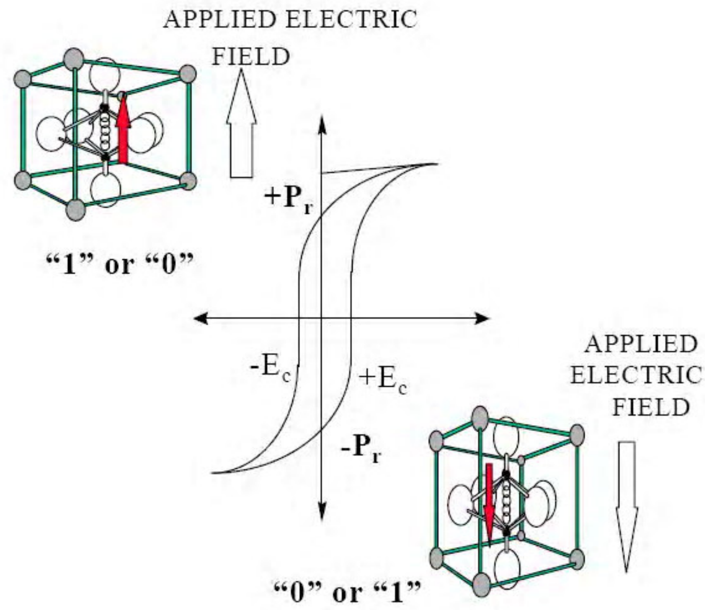


Fig. 1-7 Hysteresis loop of the ferroelectric material [4].

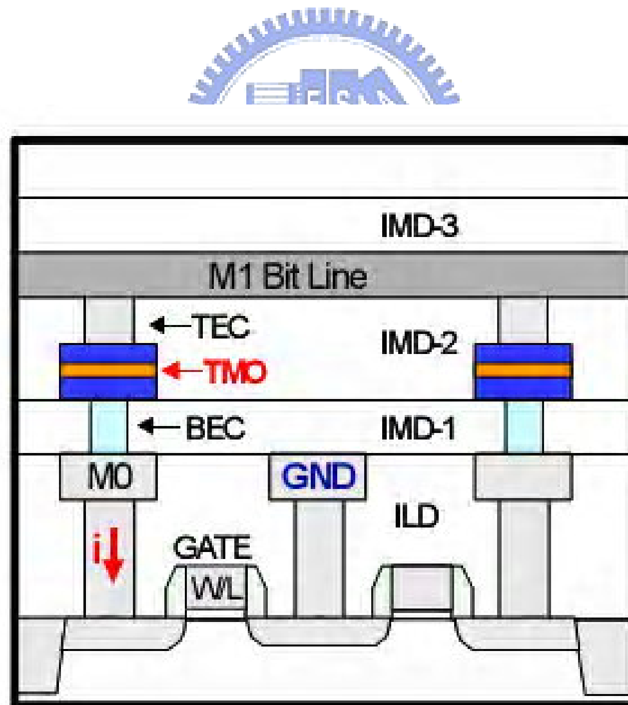


Fig. 1-8 Cross section schematic diagram of the RRAM. The transistor is fabricated in the front and the resistor in the back end [16].

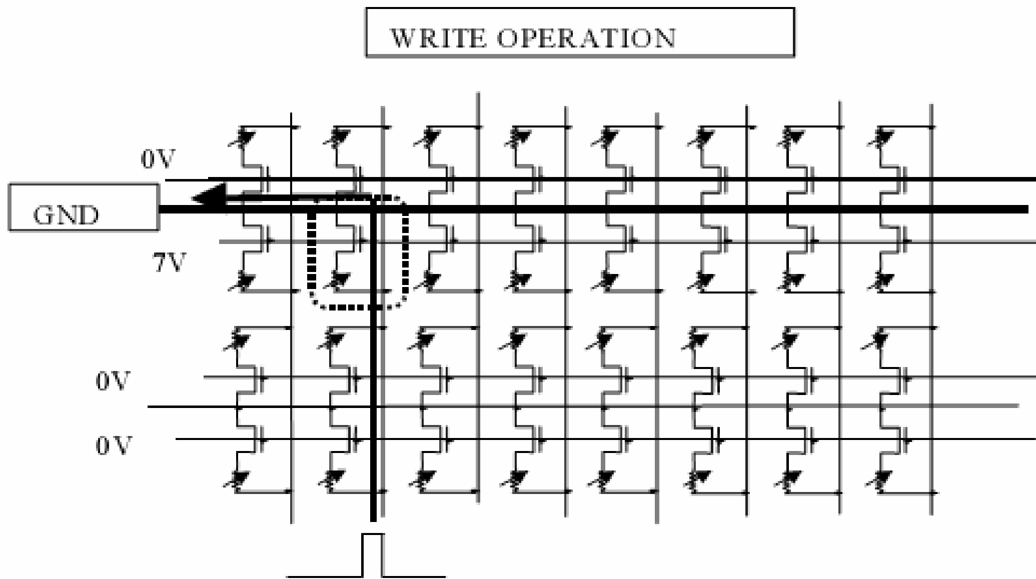


Fig. 1-9　Equivalent circuit of an array for the write operation of a given bit resistor [17].

(a)

B/L \ W/L	1	2	3	4
1	29M	20M	34M	48M
2	67M	25M	21M	46M
3	64M	21M	74M	24M
4	36M	55M	19M	38M
5	23M	46M	47M	39M

B/L \ W/L	1	2	3	4
1	28M	7.4M	7.4M	27M
2	28M	770	1.1K	7.6M
3	34M	690	950	7.6M
4	35M	7.1M	7.2M	19M
5	23M	18M	18M	22M

(b)

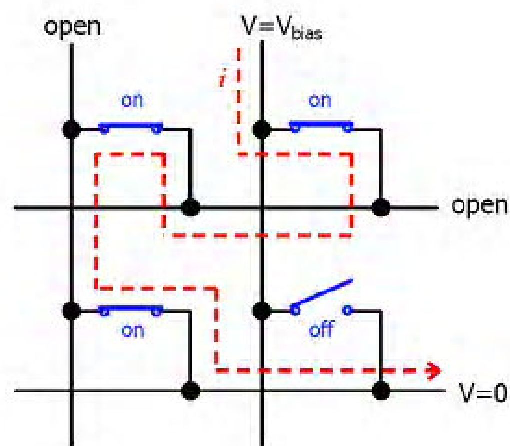


Fig. 1-10　Describing how leakage current paths make cell resistance misread [24].

Chapter 2

Experiment Details

2.1 Experiment Process Flow

There are two parts of the experimental flow, including sample preparation and device property analyses as shown in Fig. 2-1. At first, we prepare the samples and make sure these samples have switching characteristics. If not, we will modify the experimental parameters and investigate the switching characteristics again until the suitable experiment parameters are obtained.

There are many steps of sample preparation as shown in Fig. 2-2. First, 4 inch boron-doped (100) silicon substrates were cleaned by standard RCA clean, and then a 200-nm-thick SiO_2 layer was thermally grown on the substrates by wet oxidation process. The SiO_2 layer is acted as the isolation layer to prevent the leakage current from the substrate. Ti deposited by electron beam evaporation is acted as adhesion layer for Pt. Then, Pt bottom electrode layer was deposited on the Ti layer also by electron beam evaporation. Synthesis of the LNO powder and the doped SZO powder were prepared previously. The powders were made to the disk-shaped target for sputtering. After that, the 100-nm-thick LNO films were deposited on the Pt bottom electrode layer to form a (100)-orientated buffer layer by radio frequency (RF) magnetron sputter. Then, the LNO buffer layer was treated by rapid temperature annealing (RTA). After that, the SZO films were deposited on the LNO buffer layer also by the RF magnetron sputter. Then, some of the SZO films were treated by rapid temperature annealing (RTA). Finally, 300-nm-thick Al top electrodes were evaporated on the SZO films by a thermal coater. The four-layer structure sample was

accomplished and the probe was detected on Al top electrode and Pt bottom electrode as shown in Fig. 2-3.

The scanning electron microscope system (SEM) and X-ray diffraction system (XRD) were used to obtain the micro-structure and the crystallization of the films, respectively. XRD analyses were helpful to confirm the orientation of the films. Field emission transmission electron microscope (FETEM) was used to analyze the interface between LNO and SZO films. Focus ion beam (FIB) was used to prepare FETEM sample. Energy dispersive X-ray analyzer (EDS) can analyze the components of LNO and SZO. An Agilent 4155C semiconductor parameter analyzer was used to record I-V curves. By the results of electrical measurement, the manufacturing process was modified to improve the performance of the device.

2.2 Radio-Frequency Magnetron Sputter Systems

In this study, a set of RF magnetron sputter system was utilized to deposit LNO and doped SZO films. The illustration of the sputter system is displayed in Fig. 2-4. The components of the sputter system are indicated as follows.

2.2.1 Vacuum System

It includes a mechanism pump and a diffusion pump. The chamber base pressure was evacuated to 10^{-5} Torr before deposition process. There are several valves to control the atmosphere and the pressure in the chamber and tubes.

2.2.2 Pressure System

There are two digital gauges in the system to present the chamber pressure in different working condition. One is Granville-Phlips Co.'s product with a

display range from atmosphere to 0.1 mTorr to show the higher chamber pressure for rough vacuum or sputtering condition. The other is an ion gauge with an accurate display of a high vacuum from 10^{-3} to 10^{-7} Torr. Accordingly, the vacuum situation under sputtering can be precisely controlled and the diffusion pump is working in the safe pressure.

2.2.3 Temperature Controlling System

It contains two thermal couple sensors, a set of four quartz lamps used as heater, and a temperature controller. During the heating process, the lamps just located above the wafer holder could heat the sample directly by radiation in lower pressure. At the same time, the change of the thermal couple could be detected and sent back to temperature controller to modify the heating power. Further, it could help to setup the temperature rising time, holding time, and falling time by a temperature program.

2.2.4 Gas Flow Controlling System

In general, the percentage of oxygen in the sputtering ambience plays an important role in oxide ceramics. Gas mass flow controller (MFC) is used to control the flow rate and atmosphere contents during the sputtering process. Therefore, it could find out that the dependence on the mass ratio of the device performance by tuning recipe.

2.2.5 Plasma Controlling System

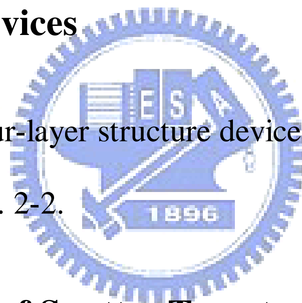
This system consists of a RF power generator, a network-matching box, and a 3-inch magnetron gun. The RF power generator has only one working

frequency at 13.56MHz, and the network-matching box has minimum reflection power by adjusting the capacitance of the whole circuit. It is able to gain the stable plasma by the controlling system.

2.2.6 Cooling System

There is cooling water which flows in the pipe welded on the chamber and in the magnetron gun. During the sputtering process, the heating lamps and plasma always produce a lot of redundant heat energy in the chamber, so the cooling water is to prevent from mechanical breakdown and maintain the sample uniformity.

2.3 Preparation of Devices



In the experiment, the four-layer structure device was fabricated. The preparation flow of device is shown in Fig. 2-2.

2.3.1 Preparation of Sputter Targets

Because the LNO and SZO thin films are deposited by the sputter system, it needs two kinds of disk-shaped sputter targets, including the LNO and the doped SZO powder targets.

I. Synthesis of the $LaNiO_3$ Powder Target

The LNO and SZO targets are prepared by the conventional solid-state powder-mixing method. There are six steps in the synthesis processes. First, two kinds of the oxide powders, La_2O_3 and NiO, were mixed by the rule of stoichiometry. It should be especially careful of the equivalent mol because

1 mol of the LNO is composed of 0.5 mol of the La_2O_3 and 1 mol of the NiO. Second, the mixed powder was put into a jar with anhydrous alcohol and rolling glass balls, and then was mixed adequately by a grinder. Third, the mixture was dried by an 85°C oven. The fourth step was the sintering step. It was the most critical process, because the sintering temperature and the heating time would affect on the LNO qualities including the resistance and orientation of the LNO sputtered films. The dried mixture was put into a furnace to execute a sequence of sintering, 600°C for 2 hours and 1300°C for 10 hours. In the fifth step, the mixed powder was put in the beaker and baked it in the oven at 150°C for 2 hours. Finally, the mixed powder put in the disk-shaped target was squeezed by a high pressure of 2000 pounds for 60 seconds such that a compact target was produced for sputtering work. The preparation flow of the LNO target was showed in Fig. 2-5.

II. Synthesis of the $SrZrO_3$ Powder Target

The SZO powder was synthesized from two kinds of oxide powder, $SrCO_3$ and ZrO_2. In order to substitute Zr atom, it was considered the suitable ionic radius compared with Zr atom. Considering all the conditions, transition metal oxide V_2O_5 was added to form the doped SZO powder. Because V has freaky oxidation number, it could show more effect on the electric properties of our memory thin films. For example, when it is expected to synthesize 0.2 mol% V-doped SZO powder, it should use 1 mol of $SrCO_3$, 0.997 mol of ZrO_2, and 0.00075 mol of V_2O_5. After mixing above elements of the doped SZO powder, the same steps were followed as synthesis of LNO powder. The mixed powder was put into a furnace of a sequence of sintering process. In the last step, a disk-shaped target was

made by a high pressure of 2000 pounds for 1 min. The manufacturing process was showed in Fig. 2-5. In this study, we prepared pure (undoped), 0.1%, 0.2%, 0.3% and 0.4% V-doped SZO powder.

2.3.2 Thin Film Depositions

The LNO bottom electrode and the doped SZO films were deposited by RF magnetron sputter sequentially. To meet our demands for different process recipe, several parameters were controlled to deposit the films based on the plasma theorem and the models of the thin film growth. There were many parameters including the chamber pressure, the RF power, the working temperature, the ambient conditions, and the deposition time. In general, chamber pressure affected the mean free path (MFP) of plasma which is relative to the deposition rate. The lower pressure was choice to create the larger MFP in the chamber, which leads to the higher deposition rate. Moreover, the deposition rate is dependent on the RF power as well. In the experiment, while depositing both the LNO and doped SZO films, the RF power was set 100 or 150W and the chamber pressure at 10 mTorr. In addition, the temperature and the ambient condition could have influence on the density of the defects, the crystallization, the conductivity, the stoichiometry, and the dielectric constant of thin films.

For the accuracy of the atmosphere, it needs the base pressure about 3×10^{-5} Torr before sputtering. Next, to maintain the ambient condition, the flow rate of Ar and O_2 by MFC was controlled, and the working pressure was kept by the valves among low pressure where the plasma was generated.

2.3.3 Heat Treatment after Thin Film Depositions

There were two purposes for the experiment using the RTA systems. One is in order to get stronger crystallization orientation or better conductivity of the LNO buffer layer. The other is to control the properties of our sample by changing the heating profile of RTA temperature. The RTA model was FE-004A made by JETFIRST.

2.3.4 Deposition of the Top Electrode

Before the Al top electrodes were deposited on the doped SZO films, the sample had been adhered to a metal mask. The metal mask had different hole with three kinds of diameters that are 150, 250, and 350μm. So the different areas are defined for the top electrodes, which are 1.767×10^{-4}, 4.908×10^{-4}, and 9.612×10^{-4} cm^2.

Al used as the top electrode was deposition by a thermal evaporation coater (EBX-6D) manufactured by ULVAC. The samples were loaded with metal masks on the spinning holder, which made the deposition rate more uniform. Then, the rough pump and the turbo pump would work in term in order that the base pressure before deposition reached 5×10^{-6} Torr.

2.4 Measurements and Analyses

2.4.1 X-Ray Diffraction (XRD)

Generally, thin films are classified according to its crystallization. There are three types of crystallization, including amorphous, polycrystalline, and crystalline. XRD analysis was used to investigate the crystal structure and orientation of our sample. Furthermore, the crystallization dependence of the

samples could be identified for heat treatment. In the experiment, the thin films were grown between amorphous type and poly type. By Scherrer's formula, $D = \frac{0.9 \times \lambda}{B \times \cos\theta}$, this could estimate the average grain size from XRD illustration. Where the background information of the XRD analysis is that λ =1.5405Å (K_α), B is the full width at half maximum (FWHM) of the XRD peak and θ is the diffraction angle. In this analysis, X-ray was made with 0.02 degree beam divergence and operation configuration at 30KV, 20mA.

2.4.2 Scanning Electron Microscope (SEM)

Comprehensively, the surface morphology issue is also a quite important character compared with the character of bulk for the thin films. The surface micro-morphology and cross section of our sample could be observed by SEM analysis. Besides, the crystallization of the thin films needed to be investigated directly by XRD analysis. So, SEM analysis is helpful to get enough information to support our illustration. The SEM model is S4700I with high resolution of 15Å made by Hitachi.

2.4.3 Focus Ion Beam (FIB)

FIB is a scientific instrument that resembles a scanning electron microscope. However, the SEM uses a focused beam of electrons to image the sample in the chamber, whereas a FIB instead uses a focused beam of gallium ions. Gallium is chosen because it is easy to build a gallium liquid metal ion source (LMIS). In a Gallium LMIS, gallium metal is placed in contact with a tungsten needle and heated. Gallium wets the tungsten, and a huge electric field (greater than 10^8V per centimeter) causes ionization and field emission of the gallium atoms.

Unlike an electron microscope, the FIB is inherently destructive to the specimen. When the high-energy gallium ions strike the sample, they will sputter atoms from the surface. Gallium atoms will also be implanted into the top few nanometers of the surface, and the surface will be made amorphous.

Because of the sputtering capability, the FIB is used as a micro-machining tool, to modify or machine materials at the micro- and nano-scale.

The FIB is commonly used to prepare samples for the transmission electron microscope. The TEM requires very thin samples, typically ~100 nanometers. The nanometer-scale resolution of the FIB allows the exact thin region to be chosen.

2.4.4 Field Emission Transmission Electron Microscope and Energy Dispersive X-Ray Spectrometer

The state-of-the-art JEOL JEM-2100F field emission transmission electron microscope is equipped with an Oxford INCA Energy TEM 200 EDS (energy dispersive X-ray spectrometer) system, a Gatan GIF Tridiem EELS (electron energy loss spectrometer) system and a Fischione high-angle annular dark field detector. Features of the JEM-2100F include a high-brightness Schottky field emission electron gun producing a probe size of less than 0.2 nm. Ultra-high point-to-point TEM resolution is 0.19 nm; atomic scale resolution of 0.136 nm can be achieved using high angle annular dark field (HAADF) scanning transmission electron microscopy (STEM) imaging. The facilities are ideally suited for crystallographic and chemical analyses at a sub-nanometer scale, including high-sensitivity EDS and EELS.

Both EDS and EELS are analytical TEM (ATEM) techniques and can provide elemental composition and distribution information. The Oxford INCA Energy TEM 200 EDS system has the following features: automatic peak ID and labeling; element maps and linescans using SmartMap data acquisition; ability to define a line or grid of points for automatic data acquisition; absorption correction for samples of finite thickness and Sitelock image drift correction.

2.4.5 Auger Electron Microscopy (AEM)

Auger Electron Spectroscopy (*Auger spectroscopy* or AES) was developed in the late 1960's , deriving its name from the effect first observed by Pierre Auger, a French Physicist, in the mid-1920's. It is a surface specific technique utilizing the emission of low energy electrons in the *Auger process* and is one of the most commonly employed surface analytical techniques for determining the composition of the surface layers of a sample.

2.4.6 Secondary Ion Mass Spectrometer (SIMS)

SIMS is a technique used to analyze the composition of solid surfaces and thin films by sputtering the surface of the specimen with a focused primary ion beam and collecting and analyzing ejected secondary ions. While only charged secondary ions emitted from the material surface through the sputtering process are used to analyze the chemical composition of the material, these represent a small fraction of the particles emitted from the sample. These secondary ions are measured with a mass spectrometer to determine the elemental, isotopic, or molecular composition of the surface. SIMS is the most sensitive surface analysis technique, being able to detect elements present in the parts per billion range.

2.4.7 Current-Voltage Measurements

The most important part of all is current-voltage measurement. It could understand the electrical properties of the device from current-voltage curve. The electrical measurement system consisted of a probe station, an Agilent 4155C semiconductor parameter analyzer, an Agilent E5250A low leakage switch which are controlled by personal computer with the Agilent VEE software, and GPIB controller.

Our electrical measurements were sorted into five items, static conductivity switching measurement, retention test, stress test, endurance test, and other electrical phenomenon measurement. The aforementioned four items were tested for criteria of our memory device and the last item was executed to understand the fundamental mechanism of our samples.

I. Static Resistive Switching Measurement

The measurement was performed by Agilent 4155C which applied a dc voltage sweeping between two specified voltages to observe the resistive switching of the sample. The measured results could observe the relation of the switching voltage and the H-state or L-state current. Use Agilent 4155C to execute the double voltage sweep function, current-voltage curve was determined with two different-current states associated with the positive applied voltage or the negative one.

II. Retention Test

Retention time is the time of information keeping. The data (1 or 0) is

not able to be distinguished beyond retention time. The current of the sample in the H-state or L-state was measured after fixed period. The retention time of the V-doped SZO film was very long. By applying the higher temperature on the device, the retention test is accelerative.

III. Non-Destructive Readout Test

The sample stressed smaller voltage than the switching voltage was able to stay in the same conductivity state. The smaller positive and the smaller negative sweep voltage were applied on the sample all the time and observed that the current changed with sweeping cycles.

IV. Endurance Test

The device applied the enough voltage (positive or negative voltage) was able to change the resistance between two states. Of course, the resistance ratio of the device increased after repeat sweeping cycles. The phenomenon, which was the decrease of the H-state current and the increase of the L-state current, was useful for us to explain the conduction mechanism.

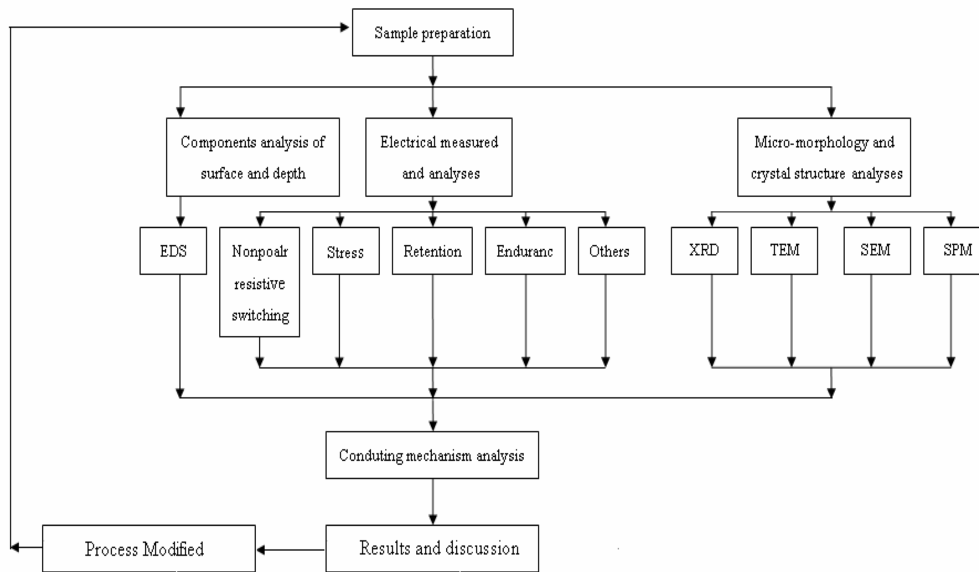


Fig. 2-1 Illustration of the experimental flow.

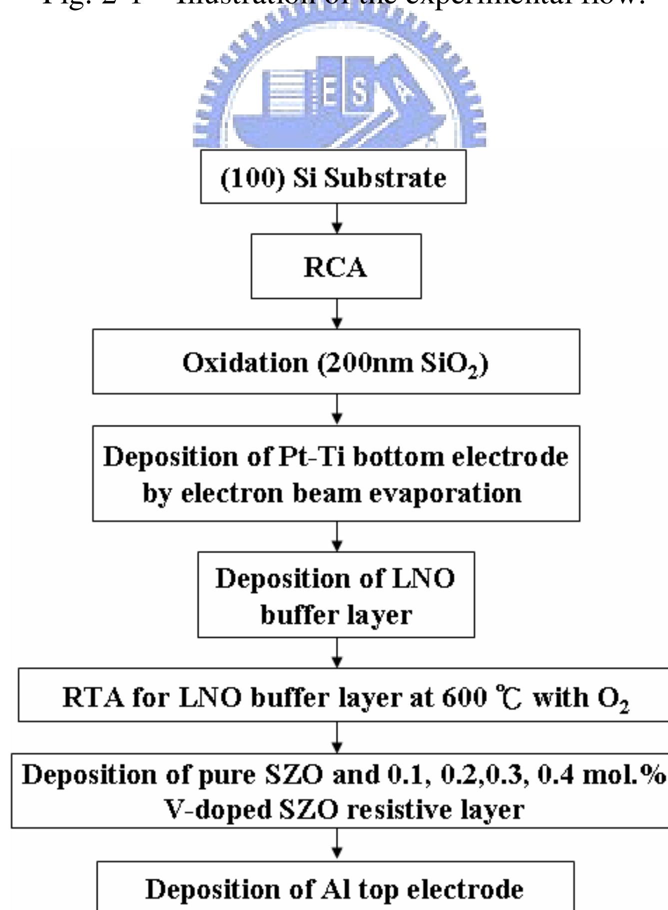


Fig. 2-2 Preparation flow of the device.

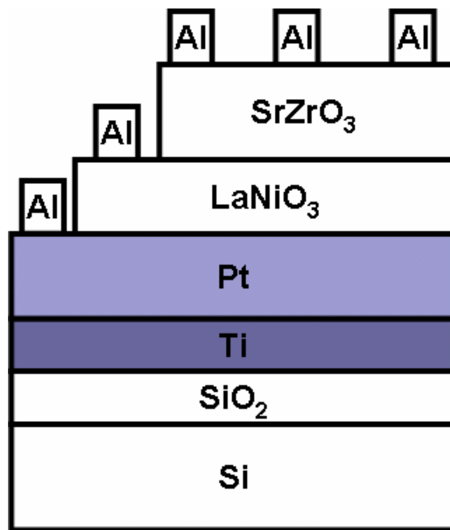


Fig. 2-3 Cross section of the four-layer structure device.

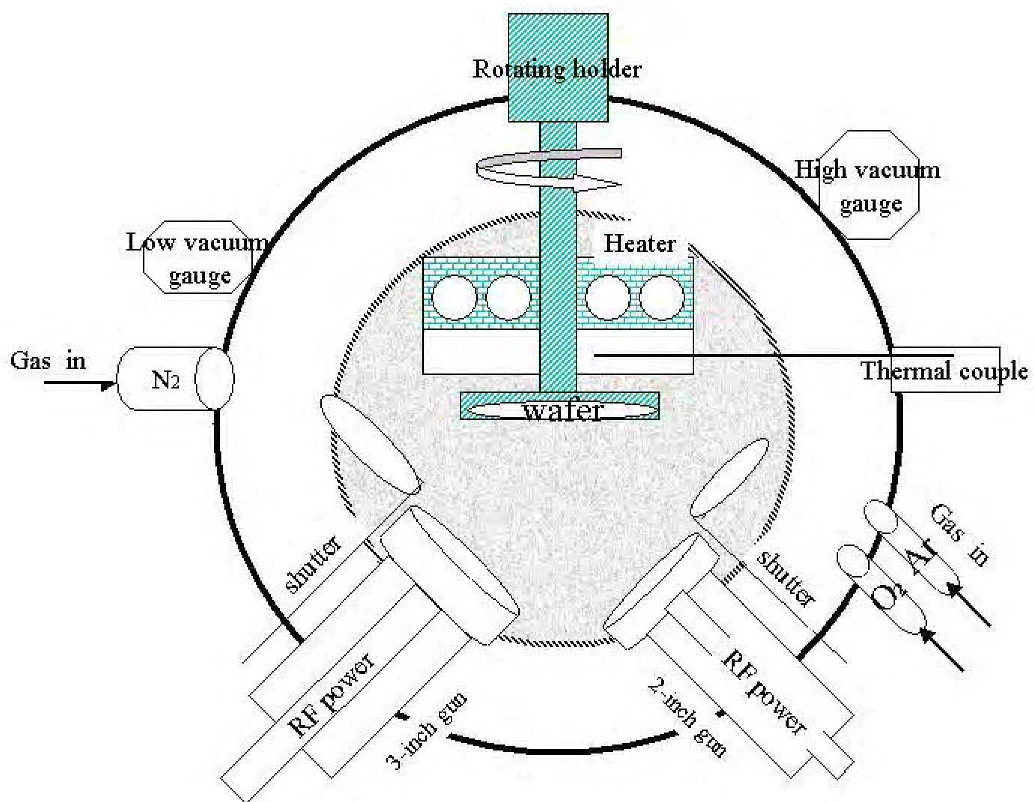


Fig. 2-4 Illustration of the sputter system.

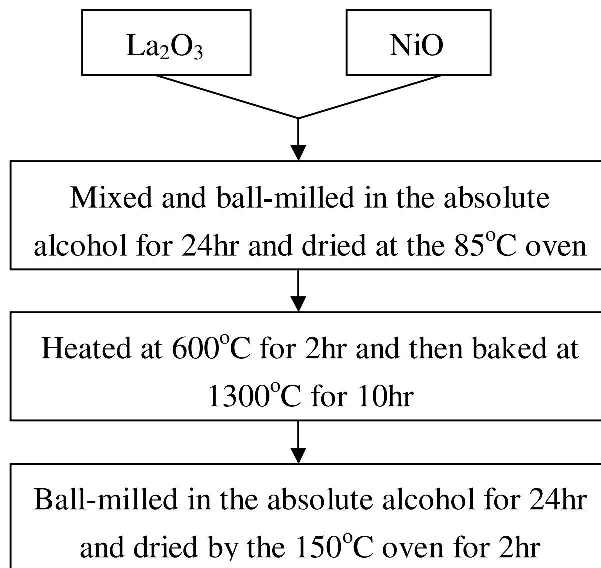


Fig. 2-5 Synthesis flow chart of LNO powder.

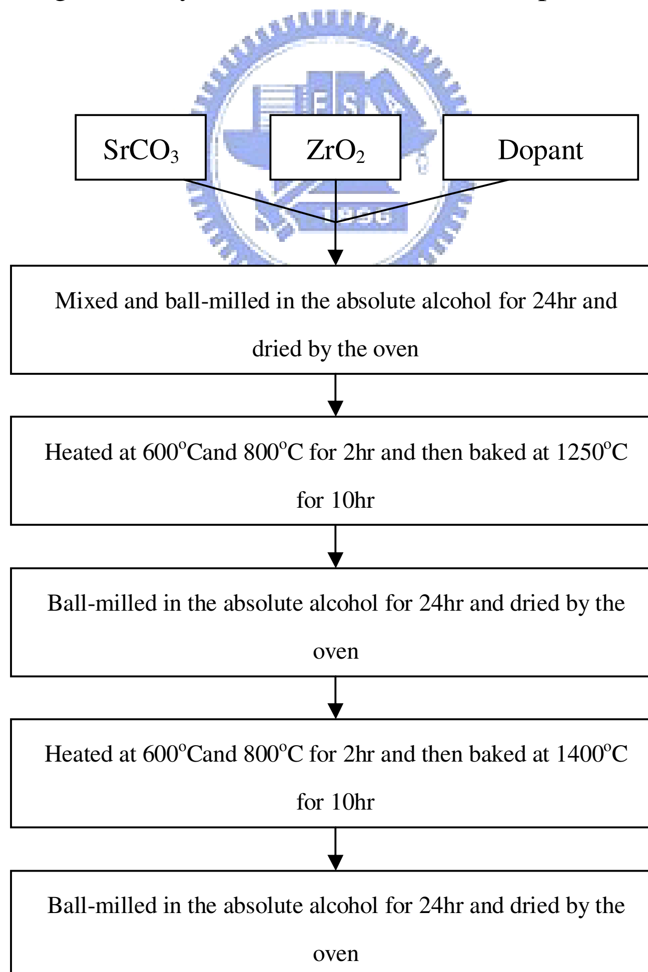


Fig. 2-6 Synthesis flow chart of doped SZO powder.

Chapter3

Results and Discussion

3.1 Experiment Contents

There are two parts of experiment results and discussion in this chapter. First, we investigate the electrical properties of undoped and V-doped $SrZrO_3$ memory films. The SZO films with higher V dopant concentration shows stable switching properties. And the operated voltages and resistance ratio are increased with V dopant concentration. By these results, we analysis the effects of V-doped SZO memory films, and make a model to discuss the doping effects.

Secondly, we investigate that the pure-SZO (undoped SZO) memory film has the smallest operated voltages, but the switching property is unstable. According to these results, the pure-SZO film was treated by rapid temperature annealing (RTA) to improve the unstable switching property. Then, we discuss the RTA effects by electrical properties and material analysis.

3.2 Properties and Analyses of the $LaNiO_3$ Buffer Layer and $SrZrO_3$ Resistive Films

3.2.1 X-Ray Diffraction and Scanning Electronic Microscope of the $LaNiO_3$ Buffer Layer and $SrZrO_3$ Thin Film

In accordance with the previous studies, the Al/0.3% V-doped SZO/LNO/Pt structure device had good resistive switching properties while the preferred orientations of the SZO film are (100) and (200) [26]. Fig. 3-1 shows the expected

crystallization of the LNO buffer layer grown on the Pt bottom electrode. LNO has (100) and (200) preferred orientations. The peaks of LNO shift toward large angle after SZO deposition process. This indicates that the lattice constant of LNO has been decreased in SZO deposition process. This is due to the SZO film was deposited at high temperature for 1 hour. Then, the expected crystallization of the pure-SZO and V-doped SZO films was grown on the LNO film. The pure-SZO and V-doped SZO has (200) preferred orientation to have obvious resistive switching properties. The device is expected to have good resistive switching properties. Figs. 3-2 and 3-3 show that the surface morphology of the LNO films in 600 and 700°C RTA, respectively. The surface morphology of the LNO annealed at 600°C is flat, but that of the 700°C-annealed film exist some precipitates at the LNO surface. According to the XRD and SEM analyses, in order to avoid the LNO (110) orientation and precipitates to influence electrical properties of the device, RTA treatment temperature was set at 600°C in O_2 ambience in this thesis.

3.2.2 Transmission Electron Microscope

HRTEM analysis shown in Fig. 3-4 is helpful to recognize the interface between the LNO and SZO films and understand the thickness of respective LNO and SZO films. The LNO buffer layer was sputtered at 250°C in a gas pressure of 10 mTorr with an Ar:O_2 mass ratio of 24:16, and in a period of 85 min. The thickness of LNO buffer layer is about 100nm. The SZO was sputtered at 500°C in a gas pressure of 10 mTorr with an Ar:O_2 mass ratio of 24:16, and in a period of 60 min. The thickness of the SZO film is about 18nm. Fig. 3-4 also shows the interface clearly between the LNO and SZO films. It proves no inter-diffusion between LNO and SZO films.

3.3 Electrical and Physical Properties of the Pure and V-doped $SrZrO_3$ memory films

3.3.1 Nonpolar Switching Property of $SrZrO_3$ Resistive Film

At beginning, the sample is at an Original-state (O-state) lower than L-state. As shown in Fig. 3-5, when the voltage sweeps to a voltage about -4.3V, the leakage current suddenly increases and switches to the H-state. Then, the nonpolar resistance switching properties can exist without any delay time between every voltage sweep cycles. The first resistive switching process is called the forming process.

After forming process, while the negative voltage is applied on the top electrode from 0 to -6V, the current rapidly increases at -2.4V, and then the device is switched from L-state to H-state. During the measurement, the current is restricted to 1mA to prevent the degradation of the device. While the device is switched from L-state to H-state and limited at 1mA, it does not influence the H-state current of the device. The device altered from L-state to H-state is called as turn-on process. Subsequently, the bias voltage sweeps from 0V to -2V and the device is switched from H-state back to L-state at -1V. The device altered from H-state to L-state is called as off process. When the positive voltage is applied on the top electrode from 0 to 7V, the device is altered from L-state to H-state at 2.7V. Then, the bias voltage sweeps from 0V to 2V and the device is changed from H-state to L-state at 1.2V. The resistance ratio between two current states is over 10^4 measured at -1V. The resistive switching properties of the device altered by either positive or negative bias voltage are called nonpolar resistive switching characteristic.

3.3.2 Forming Process of the Pure and V-doped $SrZrO_3$

Fig. 3-6 shows the forming process of pure-SZO film and 0.1%, 0.2%, 0.3%, 0.4% V-doped SZO films by negative bias voltage. When the voltage sweeps to a voltage about -4.6V, -5.1V, -5.4V, -5.6V and -6.7V for pure-SZO, 0.1%, 0.2%, 0.3% and 0.4% V-doped SZO, the leakage current suddenly increases and switches to the H-state. The statistics of forming voltages for each SZO film is shown in Fig. 3-7. We can investigate the forming voltage was increased with V dopant concentration.

3.3.3 Electrical Properties of the Pure and V-doped $SrZrO_3$

Fig. 3-8 shows the resistive switching I-V curves of pure-SZO film and 0.1%, 0.2%, 0.3%, 0.4% V-doped SZO films in turn-on by negative bias voltage and turn-off by negative bias voltage mode, which is called -on-off mode. While the negative voltage is applied on the top electrode from 0 to -7V, the current rapidly increases at -2.6V, -4.3V, -5.4V, -5.6V and -5.7V, and then the device is switched from L-state to H-state, which was explained due to the formation of current paths by electrical induced defects. During the measurement, the current is restricted to 1mA to prevent the degradation of the device. While the device is switched from L-state to H-state and limited at 1mA, it does not influence the H-state current of the device. The device altered from L-state to H-state is called as on process, and the voltage value is called turn-on voltage. Subsequently, the bias voltage sweeps from 0V to -2V and the device is switched from H-state back to L-state at -0.7V, -1V, -1.1V, -1.3V and -1.5V. The device altered from H-state to L-state is called as off process, and the voltage value is called turn-off voltage. We can investigate that the L-state current was decreased with V dopant concentration, which is due to the

formation of oxygen vacancies was suppressed by Zr^{4+} sites being substituted by V^{5+}[48].

Fig. 3-9 shows the statistics of switching voltages for each SZO film in -on-off mode. We take twenty samples in each film to calculate the average of switching voltages and compile statistics of switching voltages. The turn-on voltages were increased with V dopant concentration. And the pure-SZO has the lowest operation voltages.

The resistance statistics of H-state and L-state for each SZO film is shown in Fig. 3-10. We measure the resistance at 0.3V in H-state and L-state. Correspond to L-state current, the resistance of L-state is increased with V dopant concentration, and the resistance ratio is also increased with V dopant concentration.

3.3.4 Endurance of the Pure and V-doped $SrZrO_3$

Several SZO memory film devices are measured to calculate the uniformity of the device. The variation switching voltage of SZO memory film devices are shown in Fig. 3-11. The variation of turn-on voltage for pure-SZO memory film device is probably within ±1.5V around -3.5V. The turn-on voltages of V-doped SZO films are stable. The variation of turn-off voltage is almost unchanged for each SZO film. Fig. 3-12 shows that the variation of two current states of each SZO memory film device. The H-state current is light change for each SZO memory film device. But the variation of L-state current for pure-SZO is the worst. The stability of L-state current would be improved with V-doping. This indicates that the resistive switching property of SZO memory film device would be stabilized by V-doping. Corresponding to Fig. 3-10, the resistance ratio increases with V dopant concentration.

3.3.5 Retention

For a NVM, the data storage time is also called retention time as an important index. It means how long time the current state can be kept in an acceptable range, once the memory cell is written in one state. As shown in Fig. 3-13, retention test of the pure-SZO memory film device measured at RT after 10^6s is performed. It is no doubt that there is no current variation after 10^6s, and the resistance ratio is over 10^4. It shows good retention performance at RT. Besides, thermal test is executed in order to accelerate degeneration speed of memory device. First, the devices are switched to H-state and L-state, respectively. After 1000s the devices are kept at 85°C and also measured at 85°C. Fig. 3-13 also shows that the retention test of the devices kept at 85°C. H-state and L-state currents are stable at least 10^6s and the resistance ratio between two state is about 10^3. The retention is not affected while measured at 85°C. According to previous statement, our device shows good retention performance and thermal reliability.

3.3.6 Non-Destructive Readout

Voltage stress test is performed to check reliability for reading data frequently and for affection of unexpected voltage noise. Voltage stress is measured with two applied voltage modes, sweep and pulse voltages. Fig. 3-14 shows that the two states of our device stressed at -0.3V for 3hr are stable and kept the resistance ratio over 10^4. Voltage stress test of the device switched by sweep or pulse voltage is stable. The device has great non-destructive readout performance. The device is also measured voltage stress of the device at 85°C in order to accelerate degeneration speed of memory device. As shown in Fig. 3-14, the device is still stable at 85°C and keeps the resistance ratio over 10^4. At 85°C, the device also has great

non-destructive readout performance.

3.3.7 Conduction Mechanisms of Pure and V-doped $SrZrO_3$

Figs. 3-15 to 3-19 show the I-V curves of H-state and L-state in double logarithmic plots for each SZO film. The insets of Figs. 3-15 to 3-19 show the plots of Ln(|I/V|) as a function of $|V|^{1/2}$ of H-state at high field region. For each SZO film, the slope of H-state curve is close to unity, indicating that the H-state current is dominated by Ohmic conduction, which is related to thermally excited electrons hopping from one isolated state to the next one [27]. The slope of the L-state curve at low field is close to unity. This indicates that the L-state current at low field is dominated by Ohmic conduction. The inset shows the plot of Ln(|I/V|) as a function of $|V|^{1/2}$ of L-state at high field region. The linear fittings of the device indicate that the L-state current at high filed region follows the Frenkel-Pool (F-P) emission, which is corresponding to field-enhanced thermal excitation of trapped electrons into the conduction band [27]. Therefore, both H- and L-state conductions are bulk controlled.

3.3.8 Barrier Height

The barrier height of conducting defects for each SZO film was calculated as shown in Fig. 3-20. Φ_B represents the barrier gap between conduction band and the trapping level of defects. Φ_B of pure-SZO and 0.1%, 0.2%, 0.3%, 0.4% V-doped SZO film is respective 0.44eV, 0.57eV, 0.63eV, 0.64eV, 0.62eV. The barrier height of defects is increased with V dopant concentration. This result indicates that the shallow trapping level defects are suppressed by V doping.

3.3.9 High-Temperature Measurement

We measure the pure-SZO current of L-state and H-state at room temperature (RT) and high-temperature. Fig 3-21 shows the L-state I-V curves in double nature logarithmic plots at low field region, which were measured at different temperature. The L-state current at low field increases with measured temperature. The linear fittings indicate that the L-state current at low field is dominated by Ohmic conduction at different temperature. The activation energy (Ea) of L-state measured at -0.3V is about 0.05 eV at low field as shown in Fig. 3-22.

The plots of Ln(|I/V|) as a function of $|V|^{1/2}$ of L-state at high field region with different temperature are shown in Fig. 3-23. The L-state current at high field increases with measured temperature. The linear fittings indicate that the conduction mechanism of L-state at low field is dominated by F-P emission at different temperature. And we plot Ln(|I/V|) versus 1/KT 1/(eV) at -1V for L-state current as shown in Fig. 3-24.

Fig 3-25 shows the H-state I-V curves in double nature logarithmic plots at low field region, which were measured at different temperature. The L-state current at low field increases with measured temperature. The H-state current is dominated by Ohmic conduction at different temperature. And the Ea of H-state measured at -0.3V is about 0.13 eV at low field as shown in Fig. 3-26.

The Ea of H-state is larger than L-state. This indicates that the carriers transport through the defects in H-state and L-state are different. And we make a model to explain the resistive mechanism in next paragraph.

3.3.10 Resistive Switching Mechanism

Compare the I-V curves of O-state and L-state as shown in Fig. 3-5. The O-state current is much lower than L-state current. The O-state current is since like a straight line increased with sweeping voltage, and the L-state current is a curved. For this reason, the conduction mechanism in O-state and L-state are not the same. The carrier transports through the different conduction path in O-state and L-state. Therefore, we assume that there is not any defect in the O-state of SZO film effectively as shown in Fig. 3-27(a). After forming or electrical switching process by negative bias voltage, the electrical induced defects would be formed. The carriers would transport through these electrical induced defects as shown in Fig. 3-27(b)-(d). Corresponding to last paragraph, the Ea of L-state at low field is about 0.05 eV, and the Ea of H-state is about 0.13 eV. So, the trapping levels of electrical induced defects are different. The small circle represents the electrical induced defect whose trapping level is close with conduction band (shallow defect). And the big circle represents the electrical induced defect whose trapping level is distant with conduction band (deep defect). Fig. 3-27(b) shows the conduction mechanism of L-state at low field region, the carriers are hopping through the small circles from one isolate state to next. The L-state current at low field is dominated by Ohmic conduction. In Fig. 3-27(c), when the bias voltage is increased, the carriers are more and more plenty. The L-state at low field region, carriers transport through the big circles mainly. The L-state current at high filed region follows the Frenkel-Pool emission. In Fig. 3-27(d), the bias voltage is increased ceaselessly until switching from L-state to H-state, the big circles would line-up to form the conduction paths. Carriers transport by these current paths in H-state, and the H-state current is dominated by Ohmic conduction. Then we use voltage bias without current

compliance to switch from H-state to L-state by joule heating to rupture the current paths [49].

3.3.11 Summaries of Vanadium Doping Influence

First, the forming voltage increases with V-doping concentration. The pure-SZO has the lowest forming voltage. Second, the turn-on voltage increases with V-doping concentration. This is due to the formation of shallow defects would be suppressed by V-doping. And the pure-SZO has the lowest turn-on voltage. L-state resistance and resistance ratio are increased with V dopant concentration. The conduction mechanism of H-state is dominated by ohmic conduction. L-state at low field is dominated by ohmic conduction, and at high field is dominated by Frenkel-Poole emission. The turn-on voltage of pure-SZO is the lowest, and the power consumption is also the lowest. But the turn-on voltage is unstable. In next section, the switching property of pure-SZO was improved by thermal treatment.

3.4 Effects of Rapid Thermal Annealing on Pure-$SrZrO_3$ Thin Film

In last section, the pure-SZO has the lowest operation voltages, but the variation of turn-on voltage is larger than V-doped SZO. The unstable switching property sometimes would lead to miss error for memory device application. In order to improve the unstable switching property, the pure-SZO film with post thermal treatment is adapted. The post thermal treatment is performed by rapid thermal annealing (RTA) at various temperatures in O_2 ambient for 60 seconds. The post thermal treatment temperature is varied from 600℃ to 800℃. The RTA temperature at 600℃ has the best characteristics. The electrical properties are going to be discussed in this section.

3.4.1 X-Ray Diffraction of the $SrZrO_3$ Thin Film by Rapid Thermal Annealing

Fig. 3-28 shows the XRD patterns of SZO films with different RTA temperature in O_2 ambient for 60 seconds. We can investigate that the peaks of LNO (100) and (200) shift toward large angle after SZO deposition and RTA process. In previous paragraph, the shift of LNO peaks is due to the SZO deposition process at high temperature for 1 hour. LNO (110) orientation appeared after RTA 800℃ process. In previous study, we consider that the crystallization of the (110) LNO are the precipitates. The SZO (200) orientation is since like unchanged by RTA process. It seems that RTA process has little impact on crystallization of SZO film.

3.4.2 Scanning Electron Microscope Analyses of the $SrZrO_3$ Thin Film

Fig. 3-29 shows surface micro-morphology of the as-deposited pure-SZO film. The sputter-deposited pure-SZO film is flat and uniform. Fig. 3-230, Fig. 3-31, and Fig. 3-32 show that the surface morphology of the pure-SZO films with O_2 RTA 600, 700 and 800°C for 60 sec, respectively. The surface morphology of the pure-SZO films annealed are flat. The grain size is since like increased with RTA temperature.

3.4.3 Transmission Electron Microscope

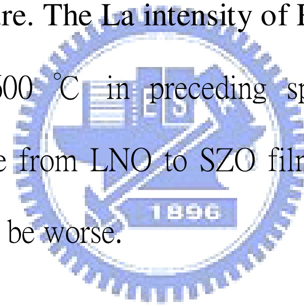
Fig. 3-33 shows the pure-SZO thin film after O_2 600℃ RTA for 60 sec. The SZO surface is smooth after RTA 600℃. This indicates that the sputter-deposited SZO films are flat. The thickness of SZO film is about 20nm. Compare with Fig. 3-4, the thickness of as-deposited SZO film and RTA-600℃ SZO film are almost the same.

3.4.4 Auger Electron Spectroscopy

Fig. 3-34 shows the AEM of Lanthanum intensity for pure-SZO and LNO film with different RTA temperature. The sputter time represents the deepness from pure-SZO to LNO film. The La intensity of RTA 700 and 800 ℃ are higher than W/O RTA and RTA 600 ℃ in preceding sputter time. This indicates that the Lanthanum would diffuse from LNO to SZO film with RTA 700 and 800℃, and the switching property would be worse.

3.4.5 Secondary Ion Mass Spectrometer

Fig. 3-35 shows the SIMS of Lanthanum intensity for the pure-SZO film with different RTA temperature. The La intensity of RTA 700 and 800 ℃ are higher than W/O RTA and RTA 600 ℃ in preceding sputter time. This indicates that the Lanthanum would diffuse from LNO to SZO film with RTA 700 and 800℃, and the switching property would be worse.



3.4.6 Endurance

Fig. 3-36 shows the variation of switching voltage of pure-SZO with O_2 RTA 600℃ for 60 sec. The variation of turn-on voltage for RTA 600 ℃ pure-SZO memory film device is probably within ±1V around -2.5V. Fig. 3-37 shows the variation of two current state of pure-SZO with O_2 RTA 600℃ for 60 sec. The H-state current is light change. The variation of L-state current is about one order. The resistance ratio of the device is kept at 10^4 and it is enough to be distinguished in memory application.

Fig. 3-38 shows the switching voltage cumulative probability of pure-SZO without(W/O) RTA and with O_2 RTA 600℃ for 60 sec. The line similar to straight line

indicates that the switching property is stable. The turn-off voltage is stable for W/O RTA and RTA 600℃. The turn-on voltage of RTA 600℃ is greater than W/O RTA. So, the switching property can be stabilized by thermal treatment with O_2 RTA 600℃ for 60 sec.

Fig. 3-39 shows the variation of switching voltage of pure-SZO with O_2 RTA 700℃ for 60 sec. The variation of turn-on voltage is worse than RTA 600℃. Fig. 3-40 shows the variation of two current state of pure-SZO with O_2 RTA 700℃ for 60 sec. The H-state current is light change. The variation of L-state current is greater than 5 orders. Fig. 3-41 shows the variation of switching voltage of pure-SZO with O_2 RTA 800℃ for 60 sec. The variation of switching voltage is worse than RTA 600℃. Fig. 3-42 shows the variation of two current state of pure-SZO with O_2 RTA 800℃ for 60 sec. The variation of L-state current is greater than 5 orders. The unstable switching property of RTA 700℃ and RTA 800℃ is due to the Lanthanum diffuse from LNO to SZO film after RTA 700℃ and RTA 800℃ process.

We calculate the device Yield of W/O RTA, RTA 600, 700 and 800℃ with O_2 for 60 sec as shown in Fig. 4-43. The device with O_2 600℃ RTA for 60 sec has the best device Yield, which is achieved to 82%. The comparison of switching property for each thermal treatment device is shown in Table 3-1. The device with O_2 600℃ RTA for 60 sec has the best resistive switching property.

3.4.7 The Switching Property in Different Operation Mode

From last paragraph, the unstable switching property of pure-SZO film would be improved after thermal treatment by O_2 RTA 600℃ for 60 sec. We tried other operation mode for RTA 600℃ device.

Table 3-2 defines the four operation modes. Turn-on by negative bias voltage and turn-off by negative bias voltage is called -on-off mode. Turn-on by positive bias voltage and turn-off by negative bias voltage is called +on-off mode. Turn-on by positive bias voltage and turn-off by positive bias voltage is called +on+off mode. Turn-on by negative bias voltage and turn-off by positive bias voltage is called -on+off mode.

Fig. 3-44 and Fig. 3-45 show the statistics of four mode switching voltage for W/O RTA and O_2 RTA 600℃ 60 sec pure-SZO. The turn-on voltage squares of RTA 600℃ is smaller than W/O RTA. This indicates that the stability of turn-on voltage in four mode is improved after O_2 RTA 600℃ for 60 sec. Fig. 3-46 and Fig. 3-47 show the statistics of four mode switching cycle. The cycle number of +on+off and +on-off mode were increased after RTA 600℃ thermal treatment. The +on-off mode has the longest cycle number.

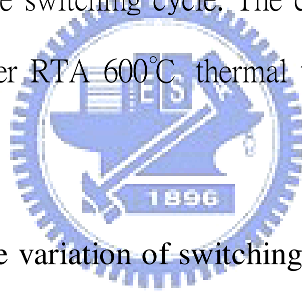


Fig. 3-48 shows the variation of switching voltage of pure-SZO with O_2 RTA 600℃ for 60 sec in -on+off mode. The variation of turn-on voltage is probably within ±1V around -2.5V. The variation of turn-off voltage is probably within ±0.5V around 1V. . Fig. 3-49 shows the variation of two current state of pure-SZO with O_2 RTA 600℃ for 60 sec in -on+off mode. The variation of L-state and H-state current are about two orders. The resistance ratio of the device is kept at 10^4 and it is enough to be distinguished in memory application.

Fig. 3-50 shows the variation of switching voltage of pure-SZO with O_2 RTA 600℃ for 60 sec in +on+off mode. The variation of turn-on voltage is probably within ±1.5V around 3V. The variation of turn-off voltage is probably within ±0.5V around 1V. . Fig. 3-51 shows the variation of two current state of pure-SZO

with O_2 RTA 600℃ for 60 sec in +on+off mode. The variation of H-state current is about two orders, and the variation of L-state current is less than one order. The resistance ratio of the device is kept at 10^3 and it is enough to be distinguished in memory application.

Fig. 3-52 shows the variation of switching voltage of pure-SZO with O_2 RTA 600℃ for 60 sec in +on-off mode. The endurance can achieve 127 times. The variation of turn-on voltage is probably within ±1V around 2.5V. The variation of turn-off voltage is probably within ±0.8V around -1.2V. . Fig. 3-53 shows the variation of two current state of pure-SZO with O_2 RTA 600℃ for 60 sec in +on+off mode. The variation of H-state and L-state current is about one order. The resistance ratio of the device is kept at 10^3. The +on-off operation mode has the long endurance and stable switching property.

3.4.8 Different RTA Time

From last paragraph, we tried RTA 600℃ with O_2 for 60 sec to pure-SZO film, which has the obvious improvement for switching property. Then, we tried different RTA time with O_2 at 600℃ for pure-SZO film. The RTA time includes 5 sec, 30 sec, 120 sec. Fig. 3-54 and Fig. 3-55 show the statistics of four mode switching voltage of pure-SZO with O_2 RTA 600℃ for 5 and 30 sec. Correspond to W/O RTA and O_2 RTA 600℃ for 60 sec, the stability of switching voltage would be improved by O_2 RTA 600℃ for longer period. But the switching property of pure-SZO with O_2 RTA 600℃ for 120 sec was decayed. The device failed after forming process and a few switching cycle. And the compliance current must be increased. This is due to the defects in pure-SZO were almost repaired by O_2 RTA 600℃ for 120 sec. The conduction path must be formed by higher energy, and the device failed easily.

Fig. 3-56 and 3-57 show the statistics of cycle number of pure-SZO with O_2 RTA 600℃ for 5 and 30 sec. Correspond to W/O RTA and O_2 RTA 600℃ for 60 sec, the cycle number of turn-on by positive bias voltage mode increased with RTA period.

Fig. 3-58 shows the variation of switching voltage of pure-SZO with O_2 RTA 600℃ for 5 and 30 sec. The turn-off voltage was lightly changed. The turn-on voltage of pure-SZO with O_2 600℃ for 5 sec was random, and RTA for 30 sec device could investigate the obvious stabilizing turn-on voltage. But it was inferior to O_2 600℃ for 60 sec device. Fig. 3-59 shows the variation of two current state of pure-SZO with O_2 RTA 600℃ for 5 and 30 sec. The variation of H-state current is about two orders, and the variation of L-state is larger than three orders. The resistance ratio of the device is kept at 10^2 to 10^4.

3.4.9 Different Gas RTA

From last paragraph, 60 sec is the best period for RTA 600℃ with O_2. Then we tried N_2 and Ar RTA 600℃ for pure-SZO. Fig. 3-60 and 3-61 show the statistics of four mode switching voltage of pure-SZO with N_2 and Ar RTA 600℃ for 60 sec, which could not investigate the obvious stabilizing turn-on voltage. This is due to the defects repairing ability of N_2 and Ar is inferior to O_2.

Fig. 3-62 and 3-63 show the statistics of cycle number of pure-SZO with N_2 and Ar RTA 600℃ for 60 sec. Correspond to O_2 RTA 600℃ for 60 sec, the cycle number of turn-on by positive bias voltage mode increased by RTA 600℃ for 60 sec thermal treatment. The best operation mode is +on-off, which has the longest endurance cycle.

Fig. 3-64 shows the variation of switching voltage of pure-SZO with N_2 and Ar RTA 600℃ for 60 sec. The turn-off voltage was lightly changed, and the turn-on voltage was random. Fig. 3-65 shows the variation of two current state of pure-SZO with N_2 and Ar RTA 600℃ for 60 sec. The variation of H-state current is about one order, and the variation of L-state is larger than four orders. The resistance ratio of the device is kept at 10^2 to 10^6. Table 3-3 shows the comparison of switching property of pure-SZO for RTA 600℃ thermal treatment. RTA 600℃ with O_2 for 60 sec is the best thermal treatment condition for pure-SZO film.

3.4.10 Retention

Fig. 3-66 shows retention of the O_2 RTA 600℃ for 60 sec pure-SZO memory film device at RT and 85℃. The memory device measured at RT after 10^6s is performed. It is no doubt that there is no current variation after 10^6s, and the resistance ratio is over 10^3. It shows good retention performance at RT. Besides, thermal test is executed in order to accelerate degeneration speed of memory device. First, the devices are switched to H-state and L-state, respectively. After 1000s the devices are kept at 85°C and also measured at 85°C. Fig. 3-66 also shows that the retention test of the devices kept at 85°C. H-state and L-state currents are stable at least 10^6s and the resistance ratio between two state is about 10^3. The retention is not affected while measured at 85°C. According to previous statement, our device shows good retention performance and thermal reliability.

3.4.11 Non-Destructive Readout

Voltage stress is measured with two applied voltage modes, sweep and pulse voltages. Fig. 3-67 shows the voltage stress of O_2 RTA 600℃ for 60 sec pure-SZO memory film device measured at RT and 85°C. The two states stressed at bias 0.3V

for 3hr are stable and kept the resistance ratio over 10^3. Voltage stress test of the device switched by sweep or pulse voltage is stable. The device has great non-destructive readout performance. The device is also measured voltage stress of the device at $85^{o}C$ in order to accelerate degeneration speed of memory device. As shown in Fig. 3-67, the device is still stable at $85^{o}C$ and keeps the resistance ratio about 10^3. At $85^{o}C$, the device also has great non-destructive readout performance.

3.4.12 Conduction Mechanism

Fig. 3-68 shows the I-V curves of H-state and L-state in double logarithmic plots for positive and negative bias voltage of O_2 RTA 600℃ for 60 sec pure-SZO film. The insets of Fig 3-68 shows the plots of Ln(|I/V|) as a function of $|V|^{1/2}$ of H-state at high field region. The slope of H-state curve is close to unity, indicating that the H-state current is dominated by Ohmic conduction. The slope of the L-state curve at low field is close to unity. This indicates that the L-state current at low field is dominated by Ohmic conduction. The inset shows the plot of Ln(|I/V|) as a function of $|V|^{1/2}$ of L-state at high field region. The linear fittings of the device indicate that the L-state current at high filed region follows the Frenkel-Pool (F-P) emission. Therefore, both H- and L-state conductions are bulk controlled.

3.4.13 Forming Process

Fig. 3-69 and Fig. 3-70 show the forming process by negative and positive bias voltage for W/O RTA and RTA 600℃ pure-SZO. In W/O RTA pure-SZO, the forming process I-V curves has rectifying characteristics, which is similar to a Schottky-like behavior between SZO and LNO interface [48]. In RTA 600℃ pure-SZO, the rectifying characteristics is since like disappeared. This is possible due to the barrier between SZO and LNO would be modulated after RTA 600℃

thermal treatment. The hypothetical diagram of barrier modulation by RTA thermal treatment is shown in Fig.3-71.

3.4.14 Possible Mechanism of Thermal Treatment

First, the stability of resistive switching property is improved after thermal treatment by RTA 600℃ with O_2. Especially, the turn-on voltage is stable. This is due to the defects would be repaired in SZO film by RTA 600℃ with O_2. The hypothetical diagram of RTA process and possible effects is shown in Fig. 5-72. Then, the switching property would be stabilized. Secondly, the cycle number of +on+off and +on-off mode is increased by thermal treatment. This is probably due to the barrier between SZO and LNO interface would be modulated after RTA 600℃. The defects of LNO/SZO interface are decreased by RTA 600℃, and the barrier of LNO/SZO interface would be reduced. The carriers can transport easily through LNO/SZO interface. So, the turn-on by positive voltage mode can be operated well.

Table 3-1 The comparison of switching property for W/O, RTA 600℃, RTA 700℃ and RTA 800℃ with O_2 for 60 sec.

Condition / Properties	W/O	600°C	700°C	800°C
Switching voltage variation	●	★	▲	▲
Memory state variation	●	★	▲	▲
Endurance	●	●	●	●

★:better ●:medium ▲:worse

Table 3-2 The definition of operation mode.

Turn-on voltage / Turn-off voltage	Positive voltage	Negative voltage
Positive voltage	+on +off	-on +off
Negative voltage	+on -off	-on -off

Table 3-3 The comparison of switching property of pure-SZO with different gas RTA 600℃ for 60 sec and O_2 RTA 600℃ for different time.

Compare	Different gas RTA 600℃			O_2 RTA 600℃ for different time				
Condition / Properties	O_2	N_2	Ar	W/O	5 sec	30 sec	60 sec	120 sec
Switching voltage variation	★	●	●	●	●	◆	★	fail
Memory state variation	★	●	●	●	●	◆	★	fail
Endurance	★	●	●	●	●	●	★	▲

★:best ◆:better ●:medium ▲:worse

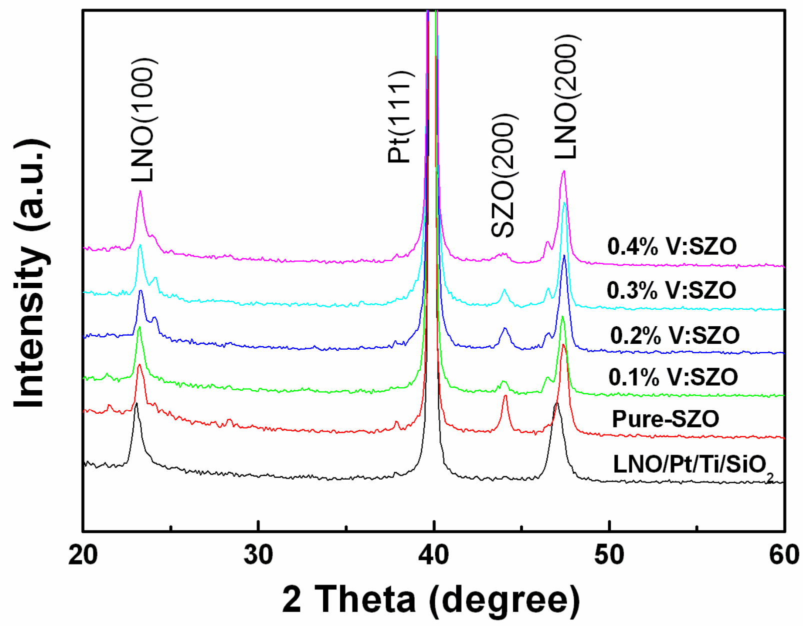
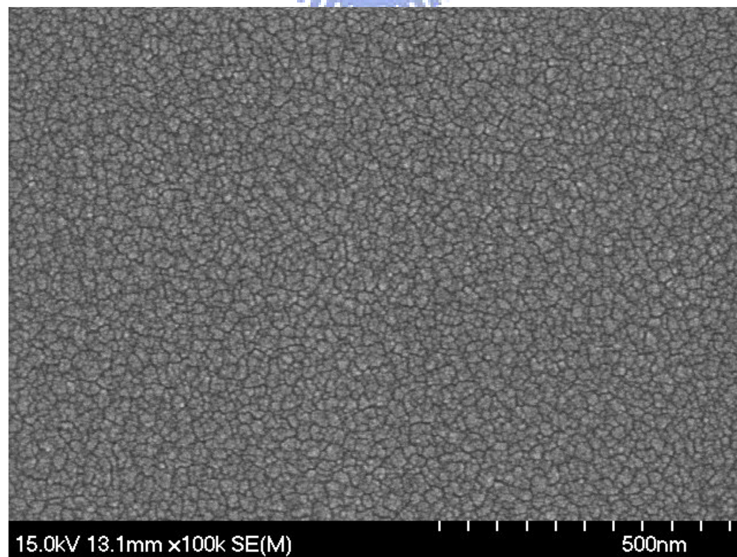
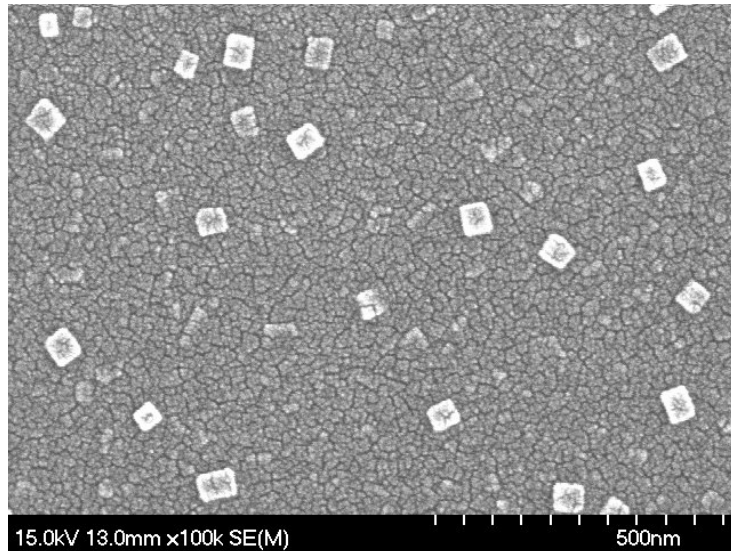


Fig. 3-1 XRD of LNO buffer layer and SZO thin film.



Figs. 3-2 SEM surface morphology of the LNO after 600°C RTA treatment.



Figs. 3-3 SEM surface morphology of the LNO after 700°C RTA treatment.

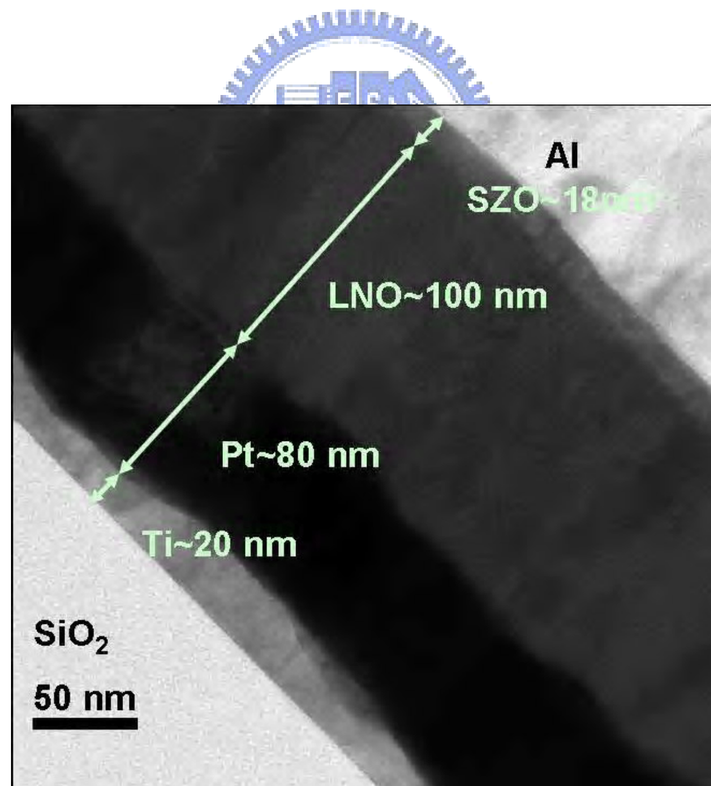


Fig. 3-4 TEM cross section image of the pure-SZO thin film.

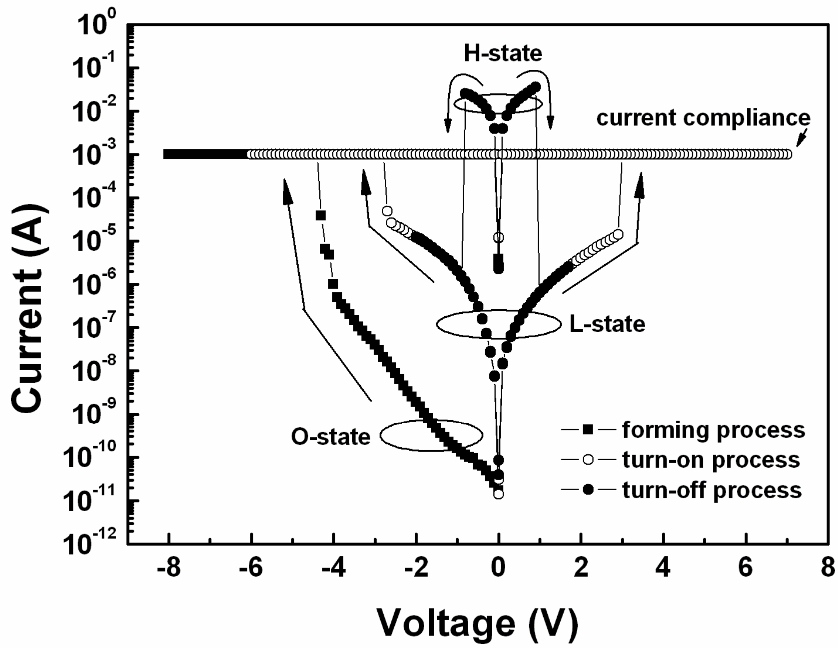


Fig. 3-5 The nonpolar switching property of $SrZrO_3$ Resistive Film.

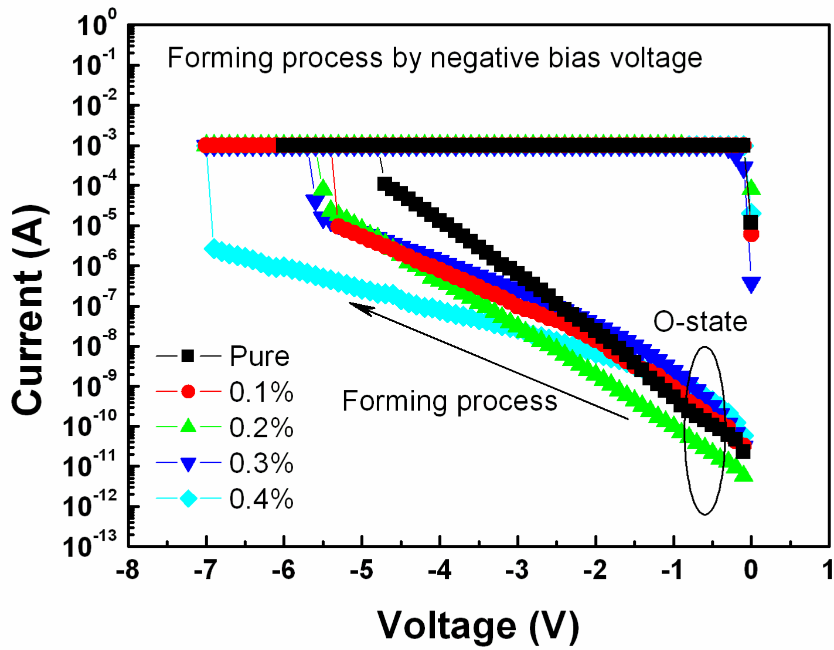


Fig. 3-6 The forming process by negative bias voltage for each SZO film.

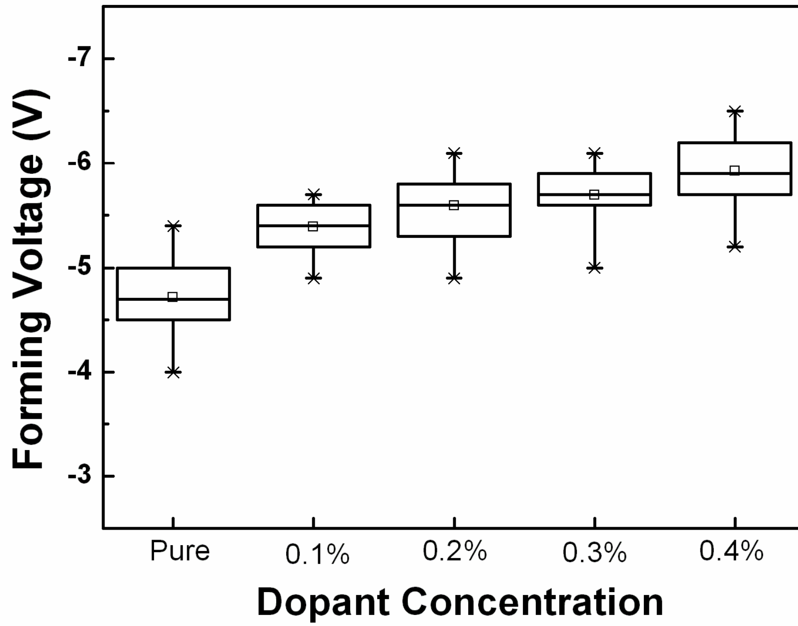


Fig. 3-7 The statistics of forming voltages for each SZO film.

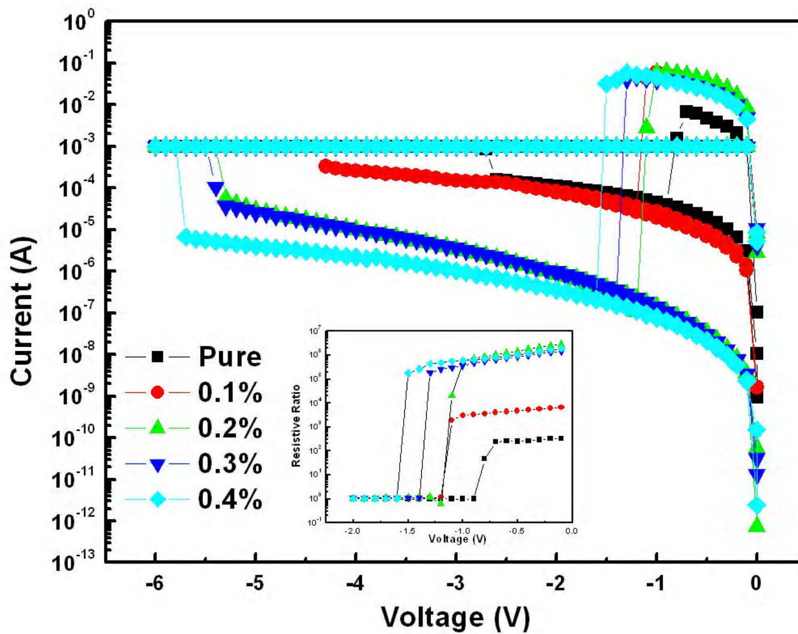


Fig. 3-8 The resistive switching I-V curves of each SZO film.

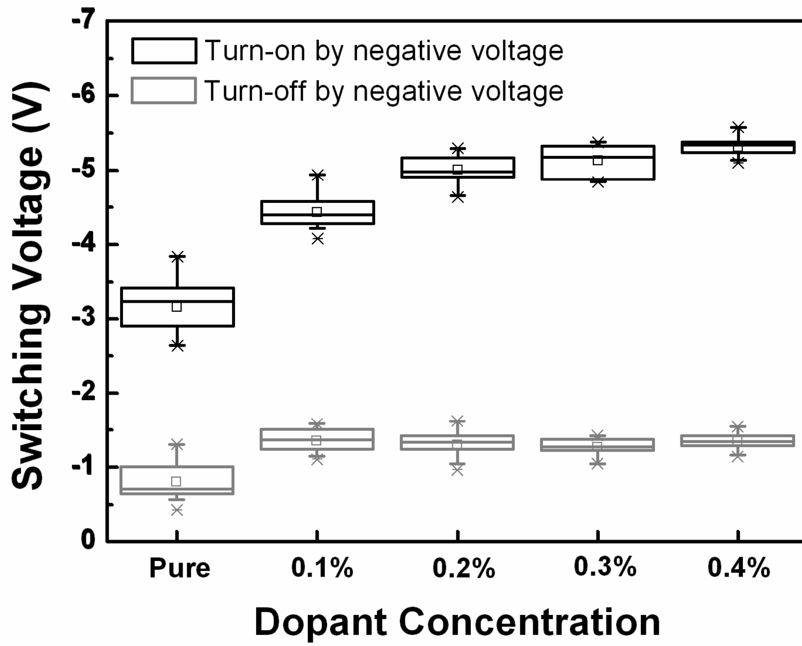
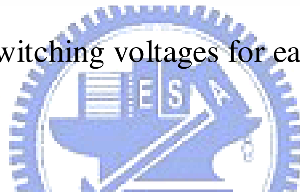


Fig. 3-9 The statistics of switching voltages for each SZO film in –on-off mode.



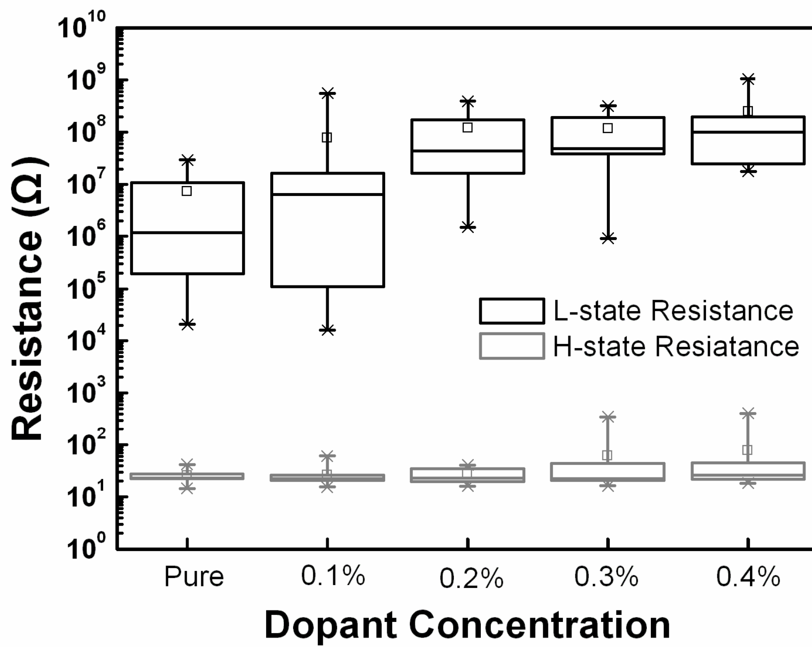


Fig. 3-10 The resistance statistics of H-state and L-state for each SZO film.

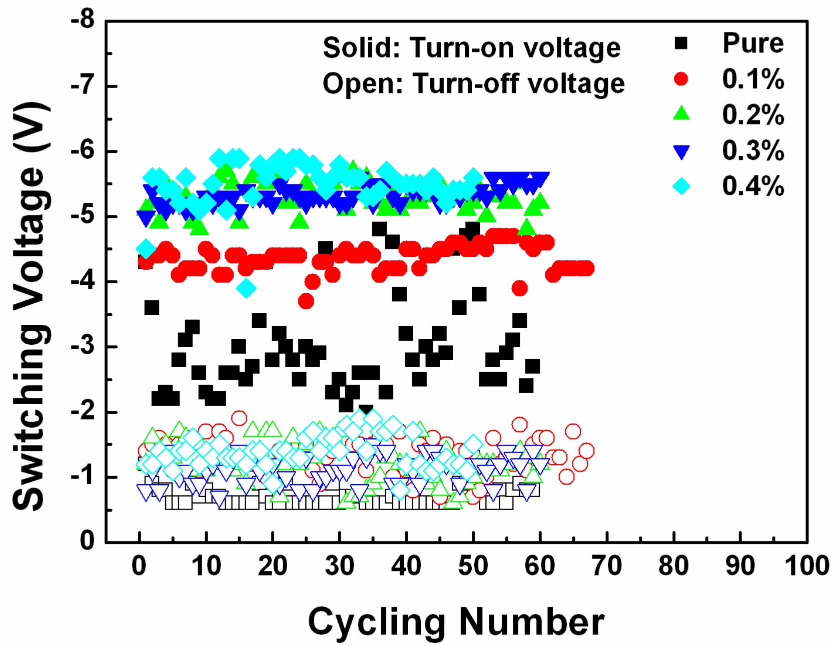
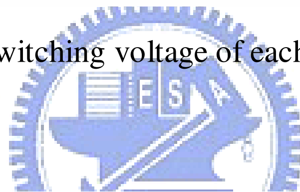


Fig. 3-11 Variation of switching voltage of each SZO memory film device.



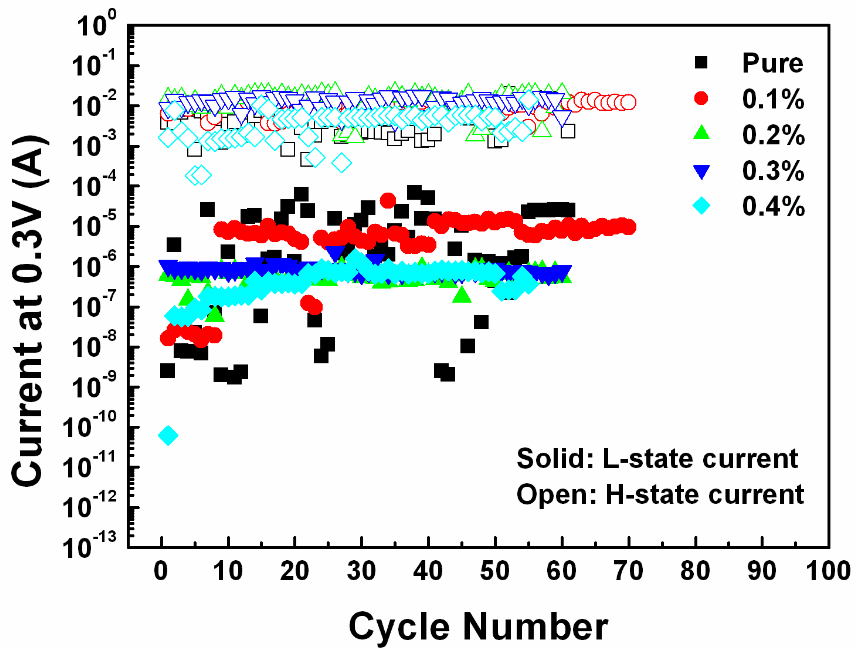


Fig. 3-12 Variation of two current state of each SZO memory film device.

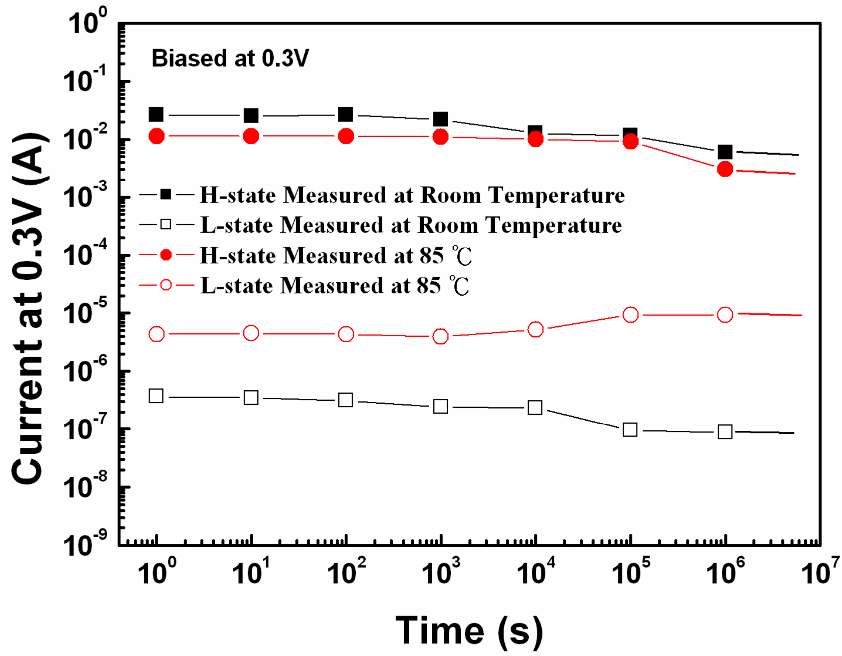


Fig. 3-13 Retention of the pure-SZO memory film device at RT and 85℃.

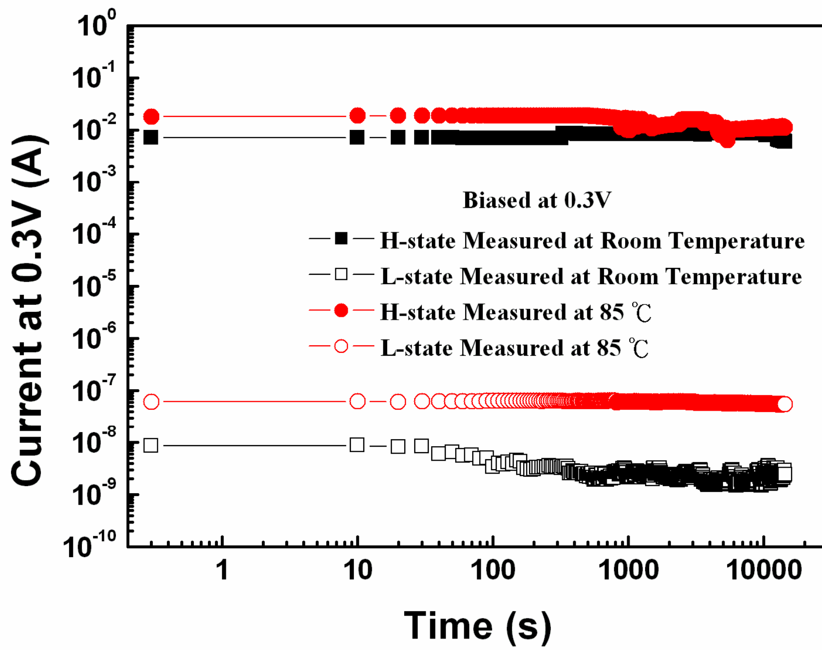


Fig. 3-14 Voltage stress of pure-SZO memory film device measured at RT and 85°C.

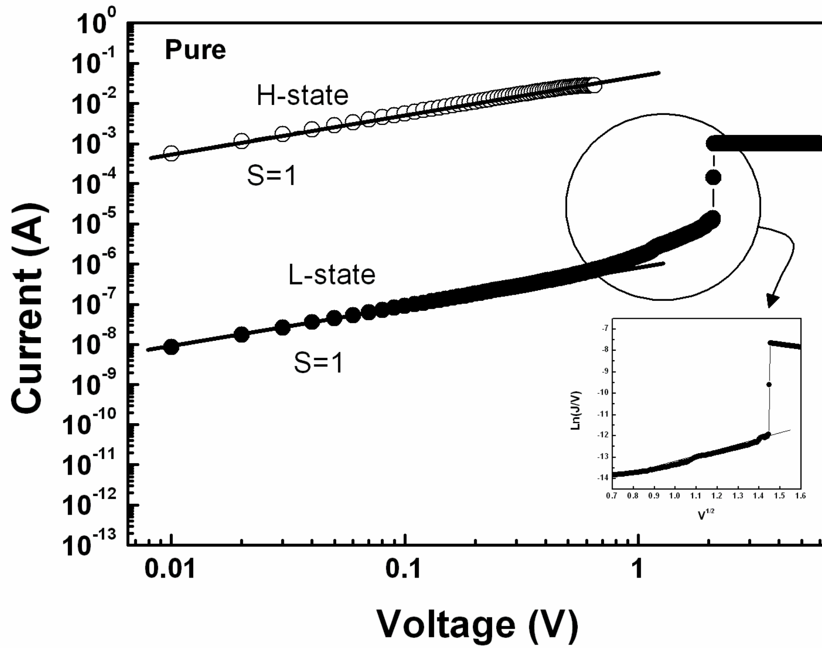


Fig. 3-15 The I-V curves of H-state and L-state in double logarithmic plots, and the inset shows the plots of Ln(|I/V|) as a function of $|V|^{1/2}$ of L-state at high field region for the pure-SZO.

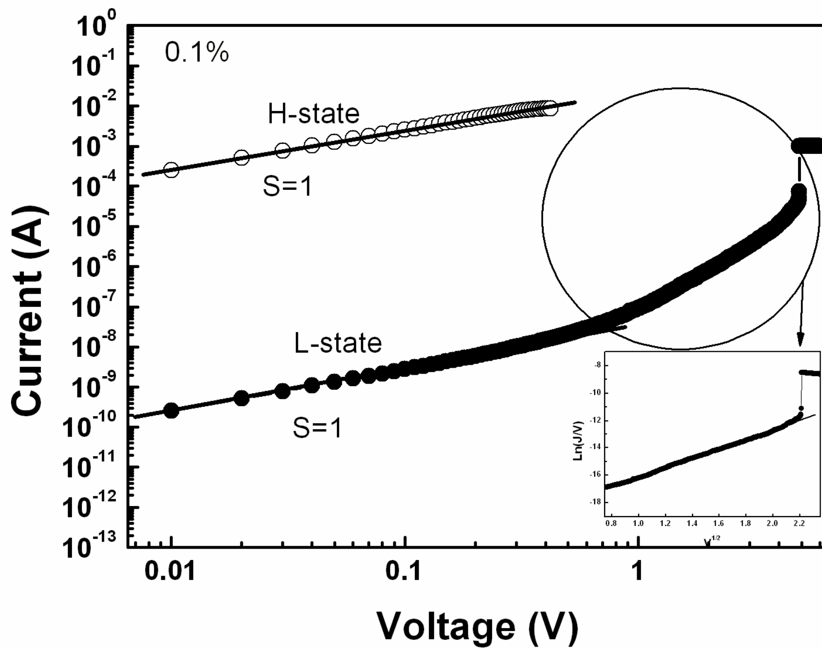


Fig. 3-16 The I-V curves of H-state and L-state in double logarithmic plots, and the inset shows the plots of Ln(|I/V|) as a function of $|V|^{1/2}$ of L-state at high field region for the 0.1% V-doped SZO.

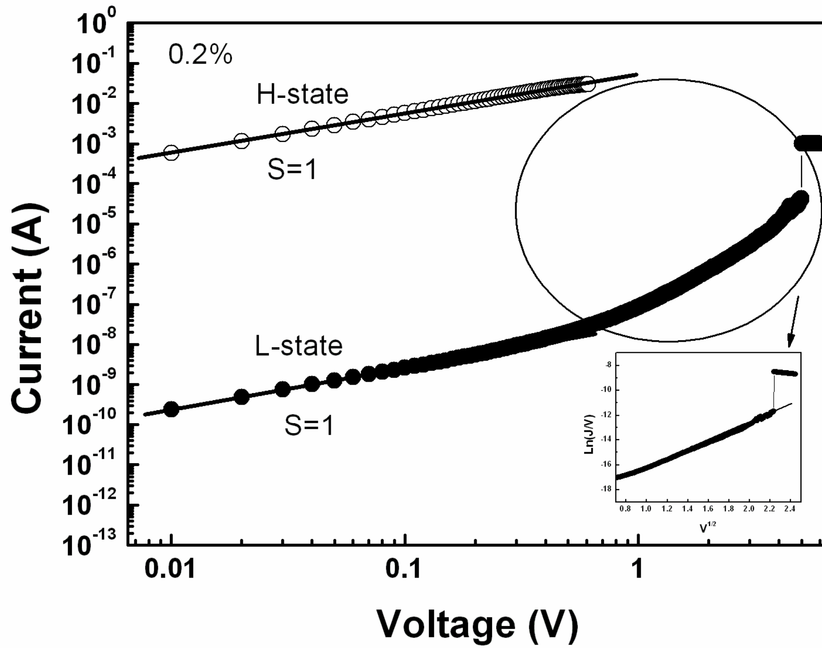


Fig. 3-17 The I-V curves of H-state and L-state in double logarithmic plots, and the inset shows the plots of Ln(|I/V|) as a function of $|V|^{1/2}$ of L-state at high field region for the 0.2% V-doped SZO.

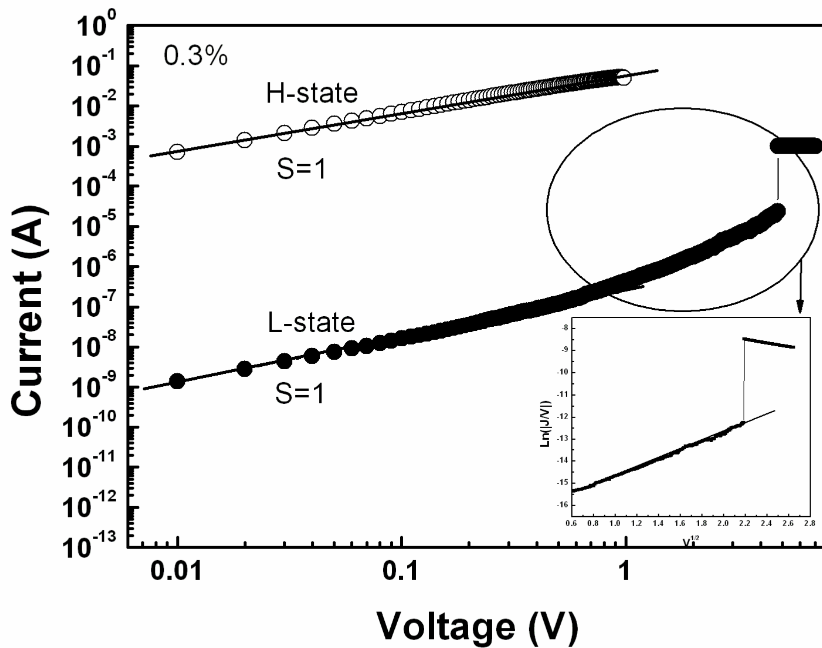


Fig. 3-18 The I-V curves of H-state and L-state in double logarithmic plots, and the inset shows the plots of Ln(|I/V|) as a function of $|V|^{1/2}$ of L-state at high field region for the 0.3% V-doped SZO.

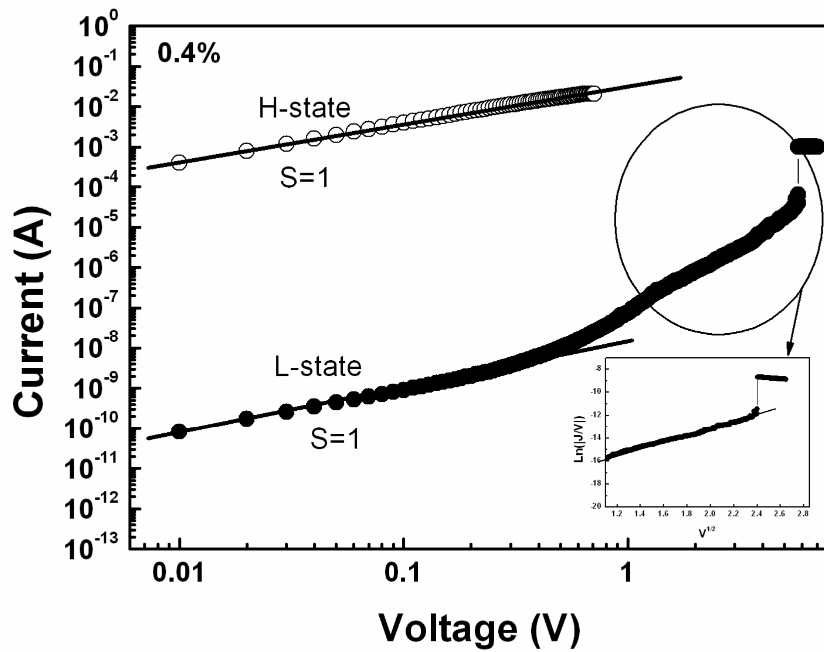


Fig. 3-19 The I-V curves of H-state and L-state in double logarithmic plots, and the inset shows the plots of Ln(|I/V|) as a function of $|V|^{1/2}$ of L-state at high field region for the 0.4% V-doped SZO.

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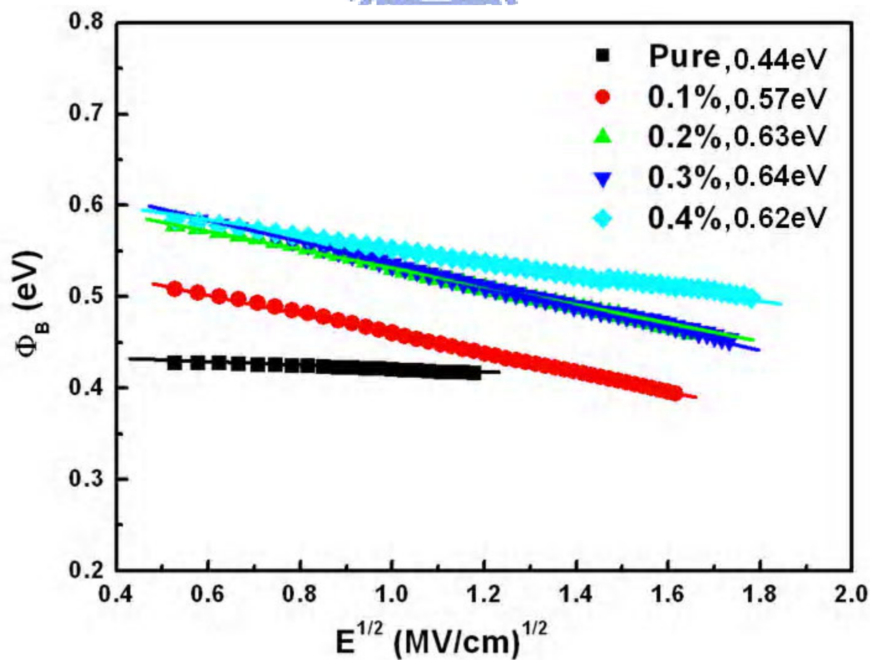

Fig. 3-20 Barrier height of each SZO film.

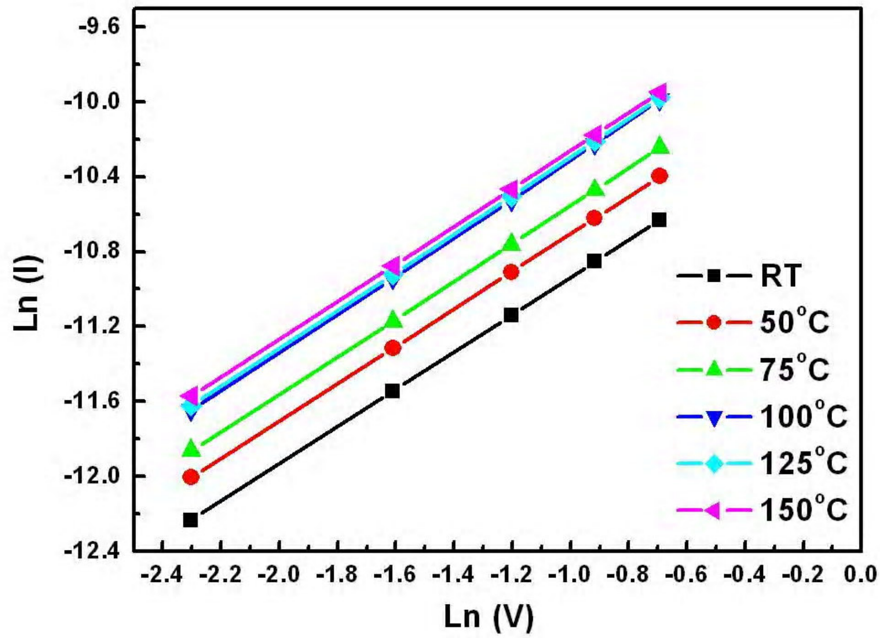

Fig. 3-21 The L-state I-V curves in double nature logarithmic plots at low field region at different temperature.

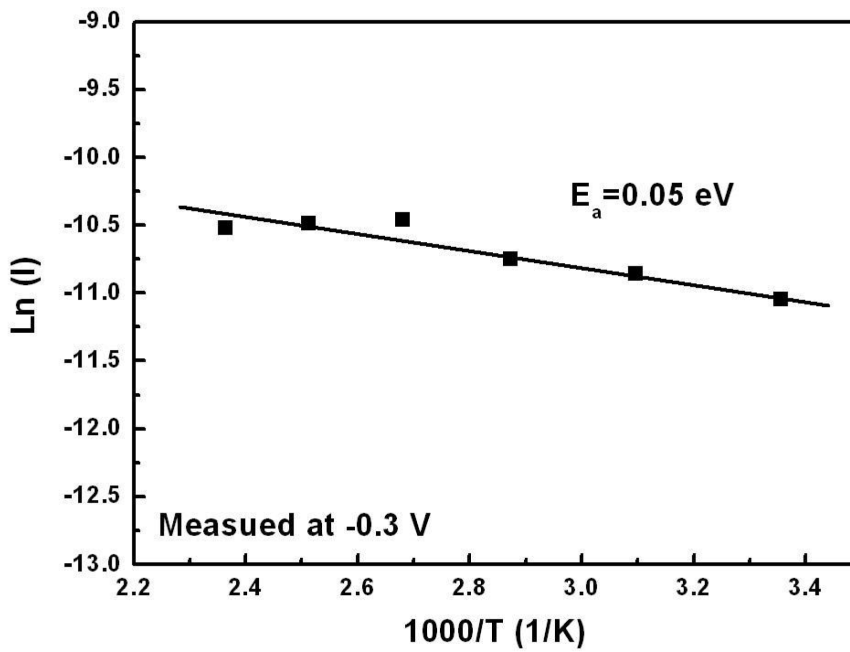

Fig. 3-22 The activation energy of L-state measured at -0.3V.

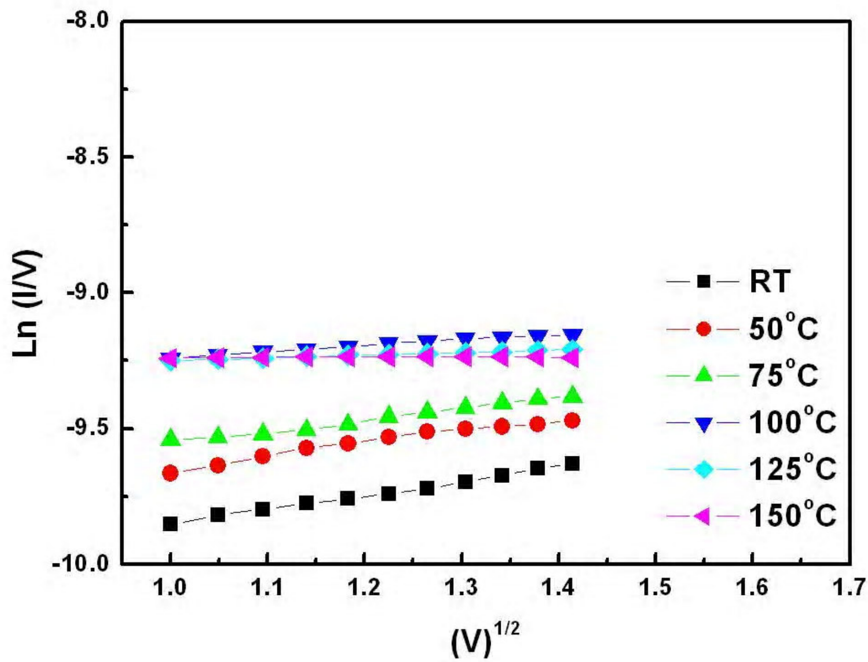

Fig. 3-23 The plots of Ln(|I/V|) as a function of $|V|^{1/2}$ of L-state at high field region at different temperature.

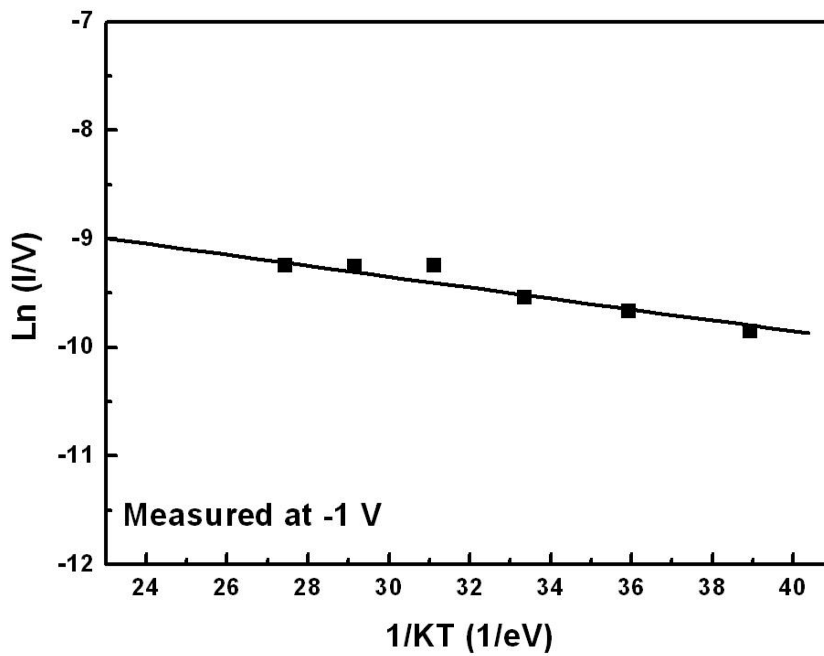

Fig. 3-24 The plots of Ln(|I/V|) as a function of 1/KT (1/eV) of L-state measured at -1V.

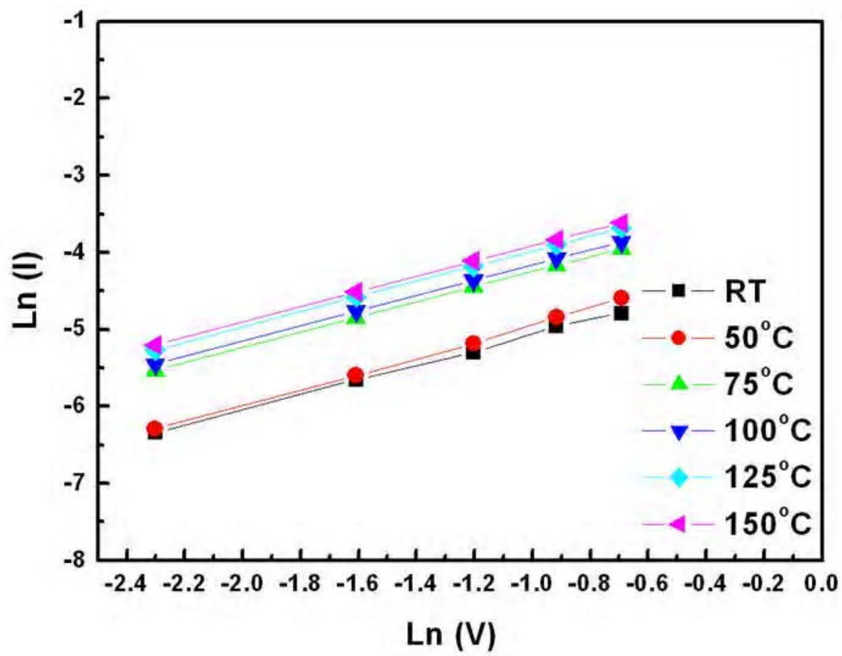

Fig. 3-25 The L-state I-V curves in double nature logarithmic plots at low field region at different temperature.

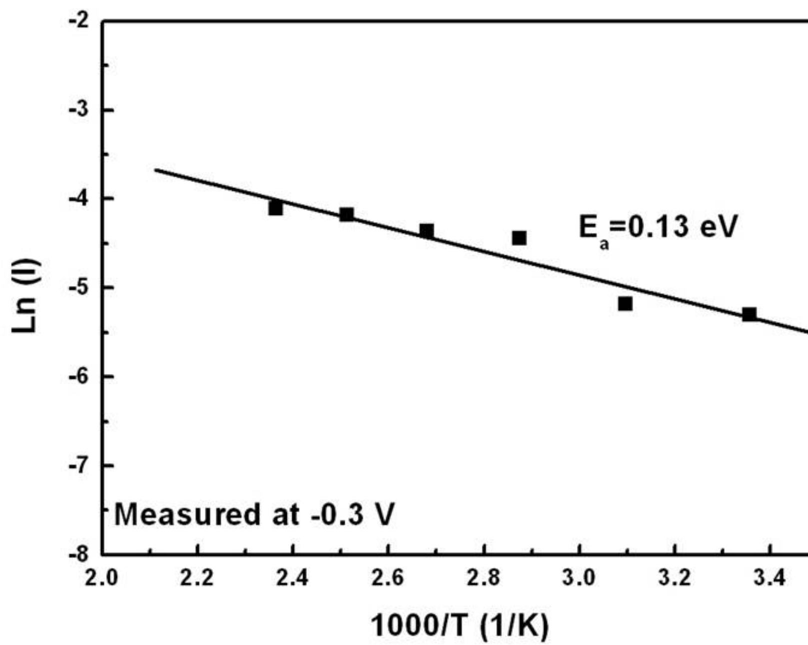

Fig. 3-26 The activation energy of H-state measured at -0.3V.

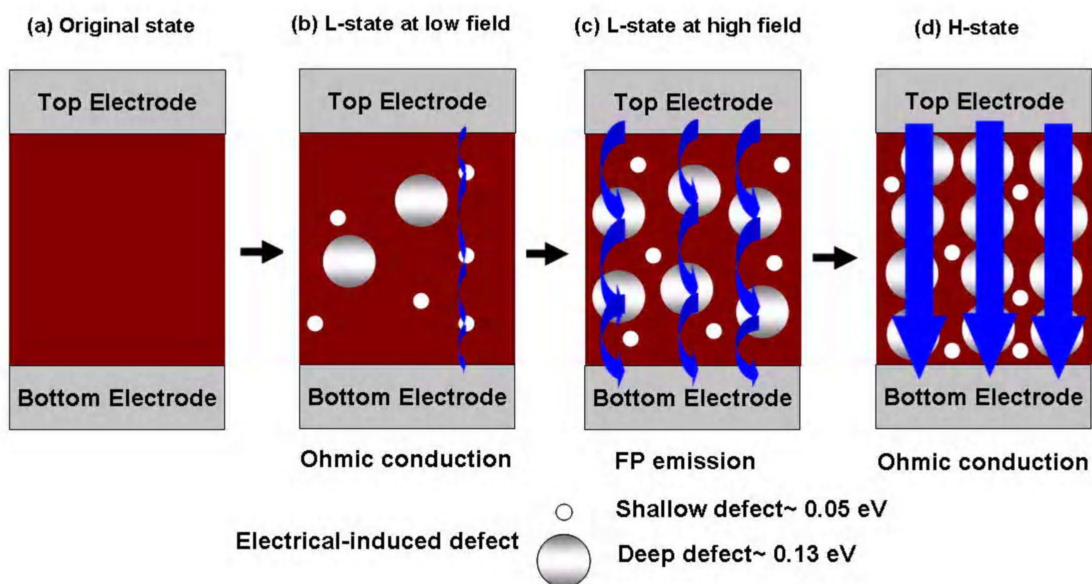

Fig. 3-27 Hypothetical diagram of resistive switching mechanism: (a) Original state, (b)L-state at low field, (c) L-state at high field, and (d) H-state.

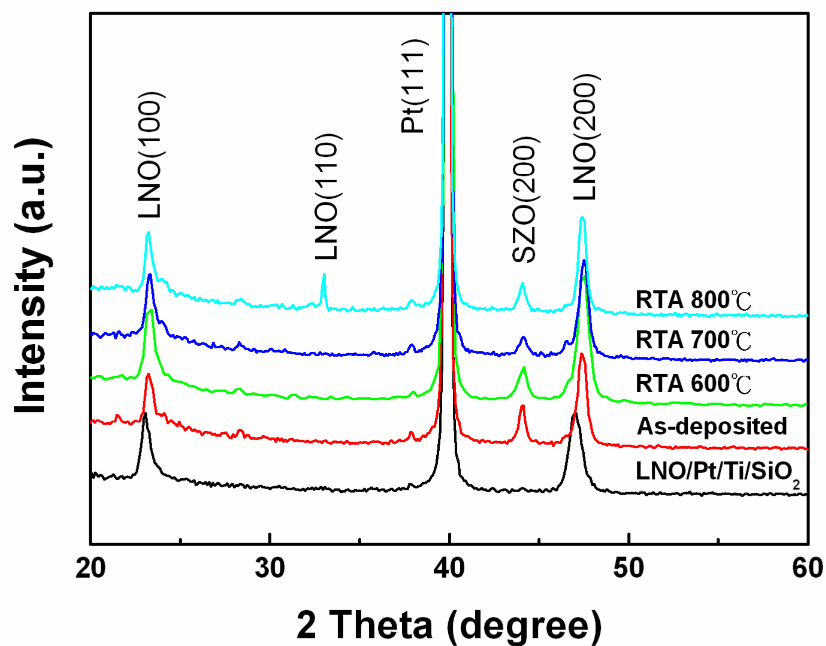

Fig. 3-28 XRD patterns of SZO films with different O_2 RTA temperature.

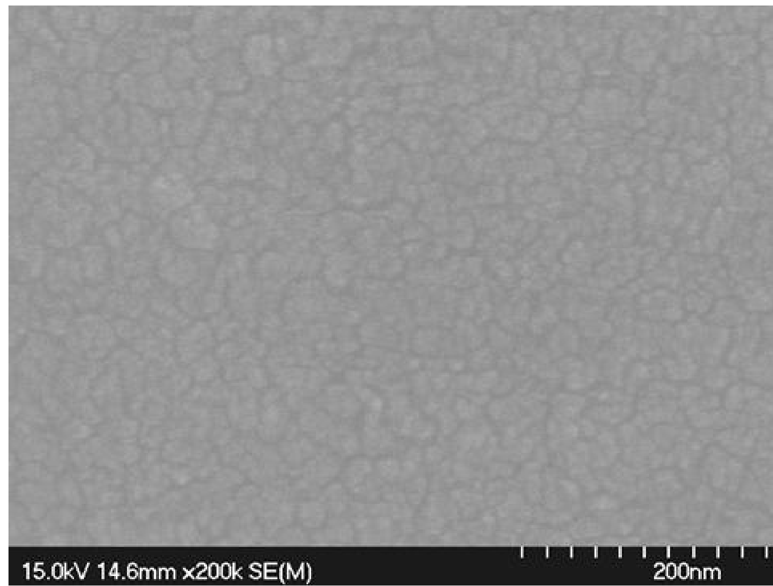

Fig. 3-29 SEM surface micro-morphology of the as-deposited pure-SZO film.

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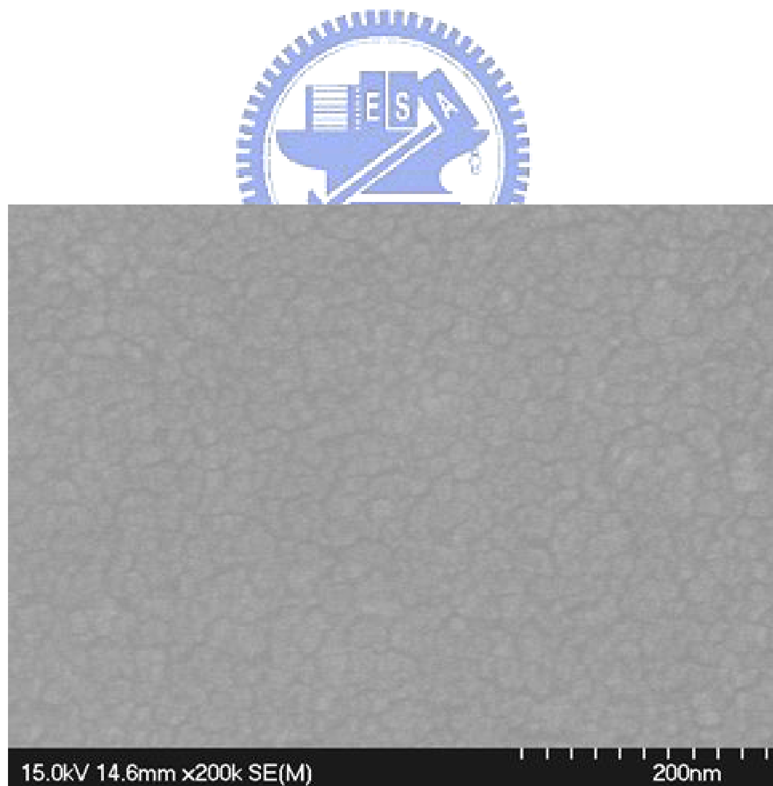

Fig. 3-30 SEM surface micro-morphology of the pure-SZO after O_2 600°C RTA treatment.

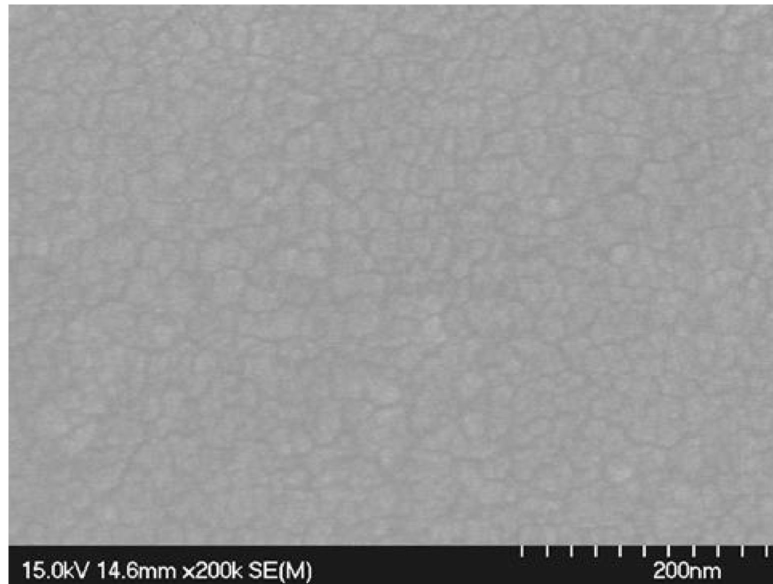

Fig. 3-31 SEM surface micro-morphology of the pure-SZO after O_2 700°C RTA treatment.

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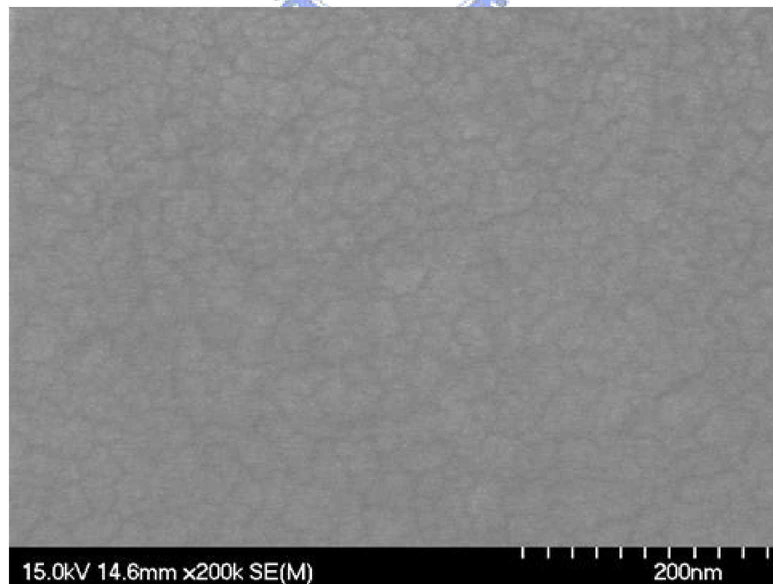

Fig. 3-32 SEM surface micro-morphology of the pure-SZO after O_2 800℃ RTA treatment.

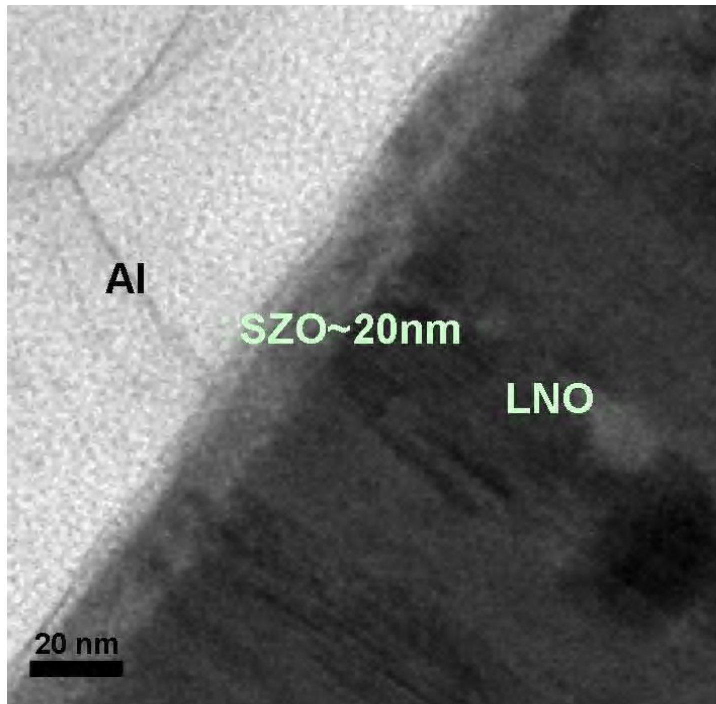

Fig. 3-33 TEM cross section image of the pure-SZO film after O_2 600℃ RTA treatment.

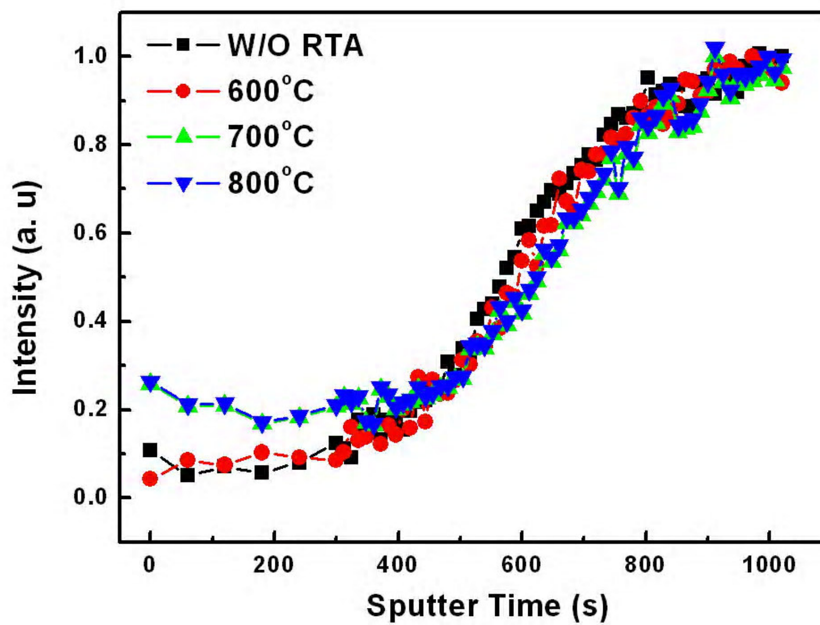

Fig. 3-34 AEM of Lanthanum intensity for pure-SZO and LNO film with different O_2 RTA temperature.

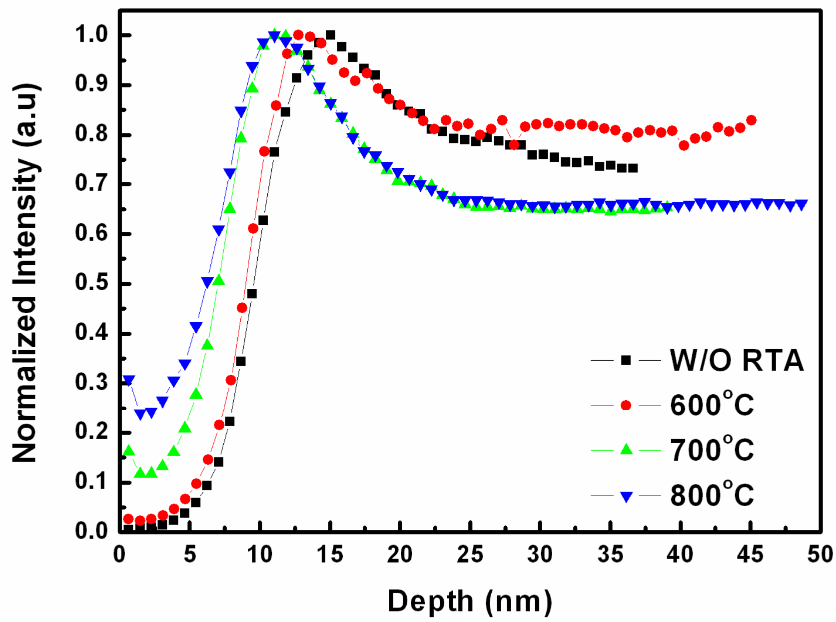

Fig. 3-35 SIMS of Lanthanum intensity for the pure-SZO film with different O_2 RTA temperature.

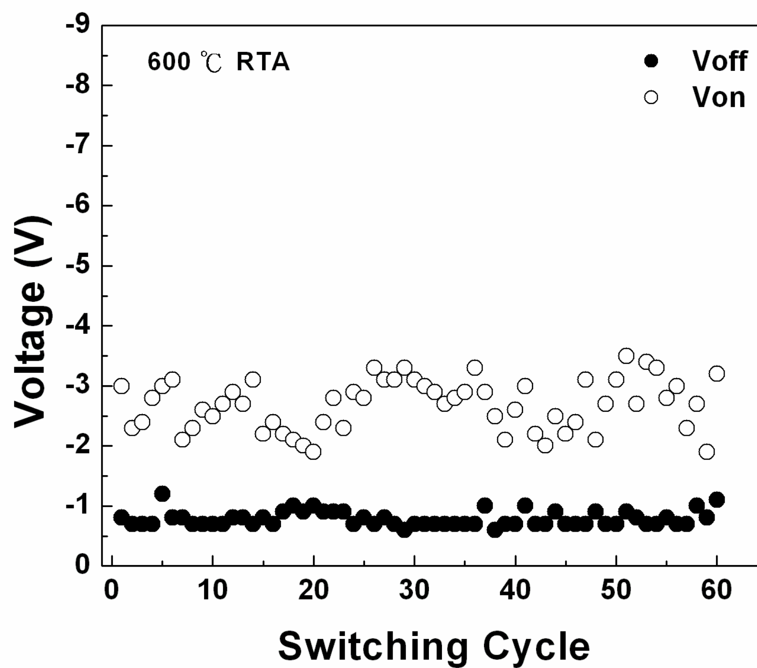

Fig. 3-36 Variation of switching voltage of pure-SZO with O_2 RTA 600℃ for 60 sec.

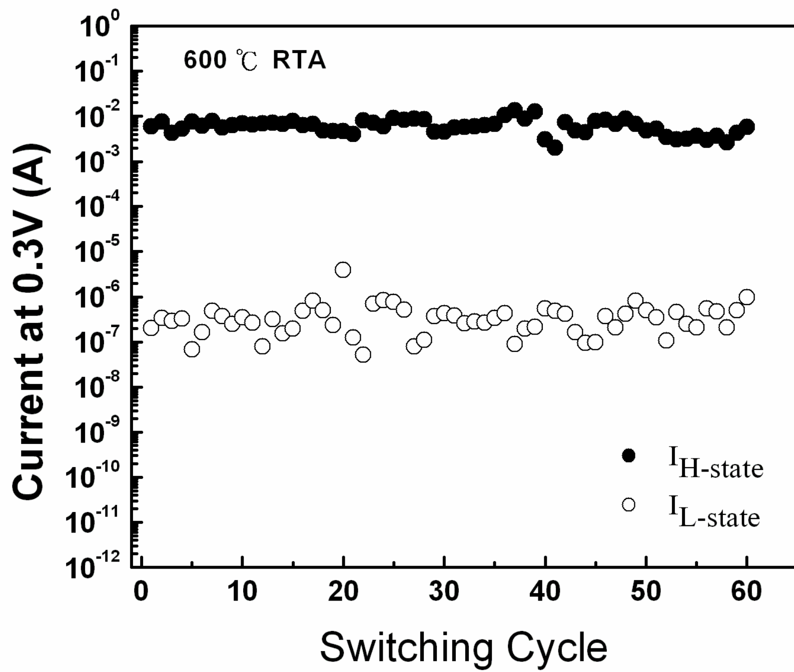

Fig. 3-37 Variation of two current state of pure-SZO with O_2 RTA 600℃ for 60 sec.

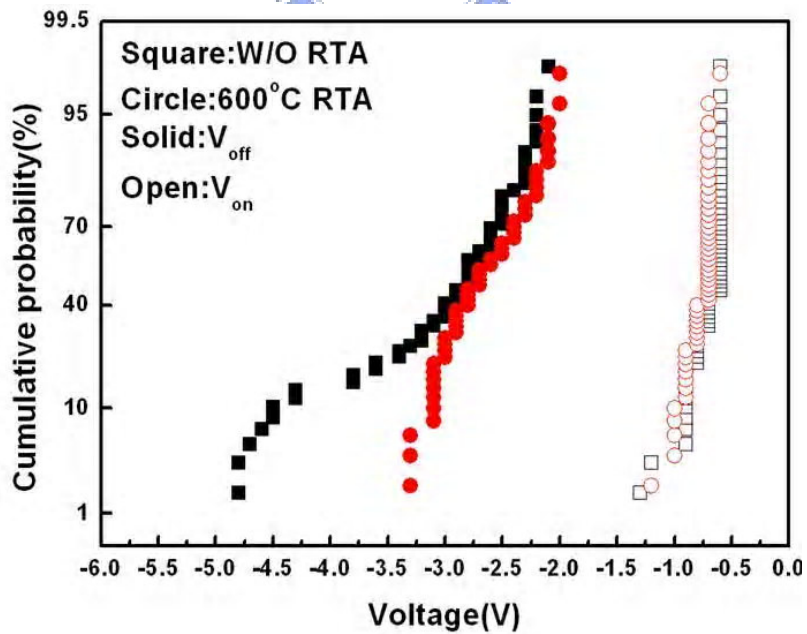

Fig. 3-38 Cumulative probability of pure-SZO without RTA and with O_2 RTA 600℃ for 60 sec.

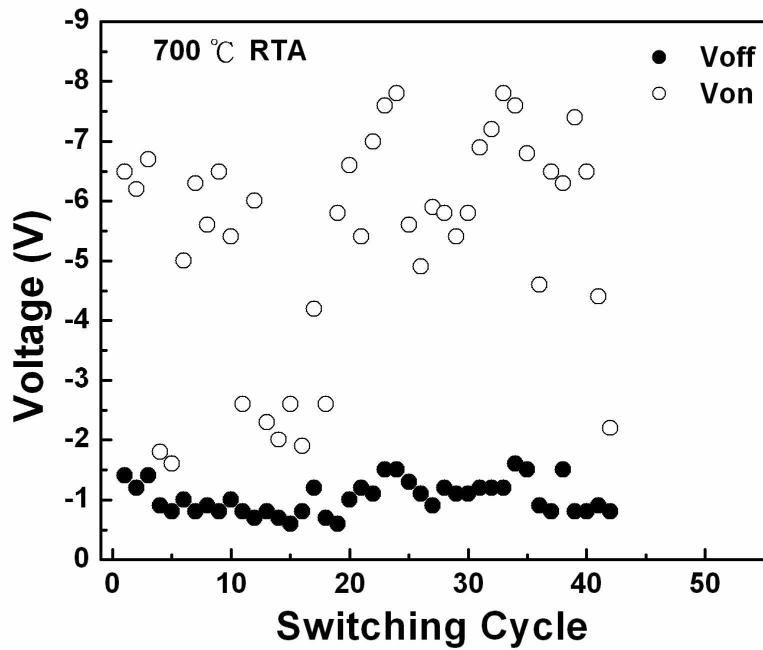

Fig. 3-39 Variation of switching voltage of pure-SZO with O_2 RTA 700℃ for 60 sec.

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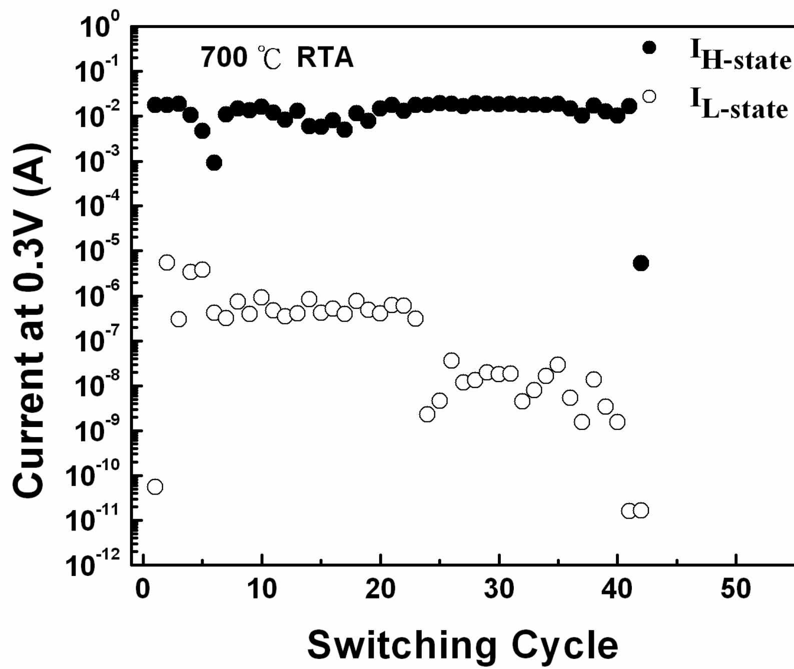

Fig. 3-40 Variation of two current state of pure-SZO with O_2 RTA 700℃ for 60 sec.

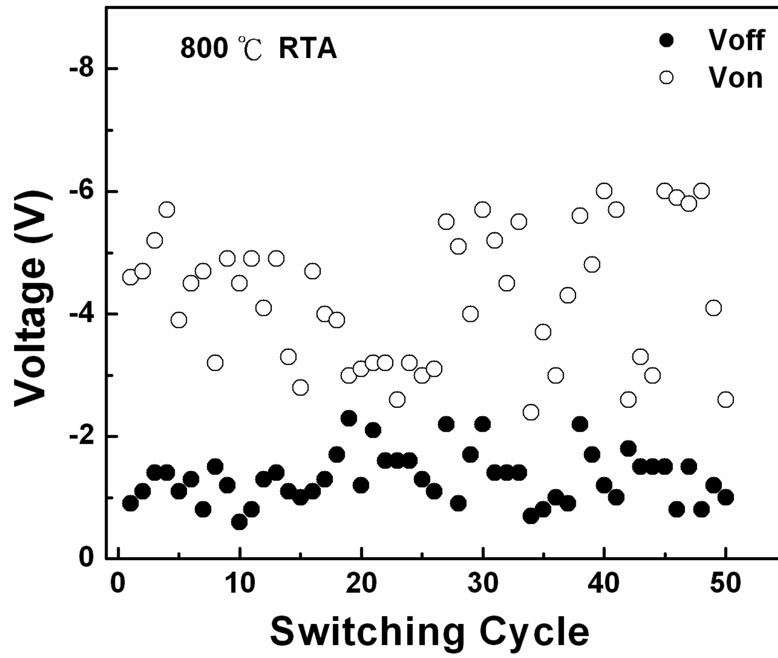

Fig. 3-41 Variation of switching voltage of pure-SZO with O_2 RTA 800℃ for 60 sec.

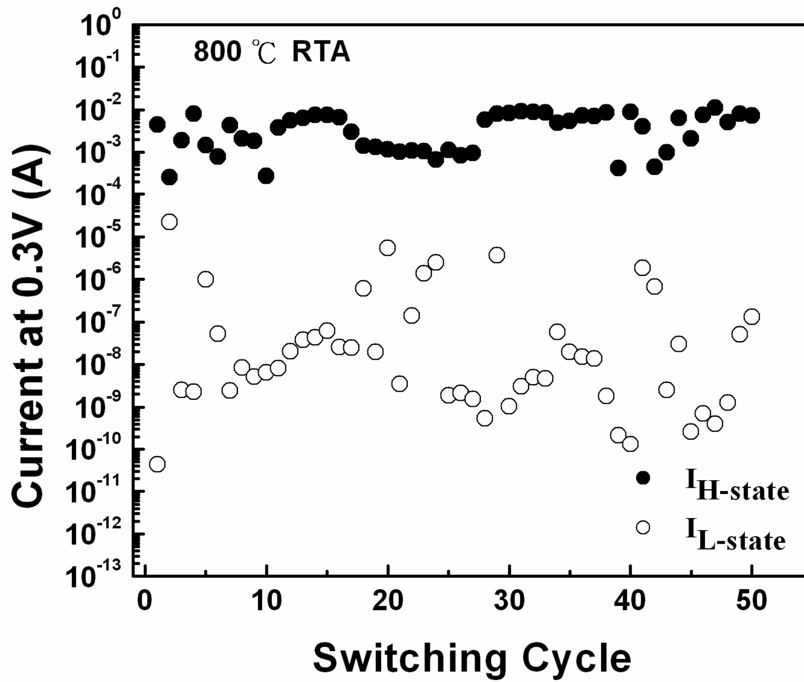

Fig. 3-42 Variation of two current state of pure-SZO with O_2 RTA 800℃ for 60 sec.

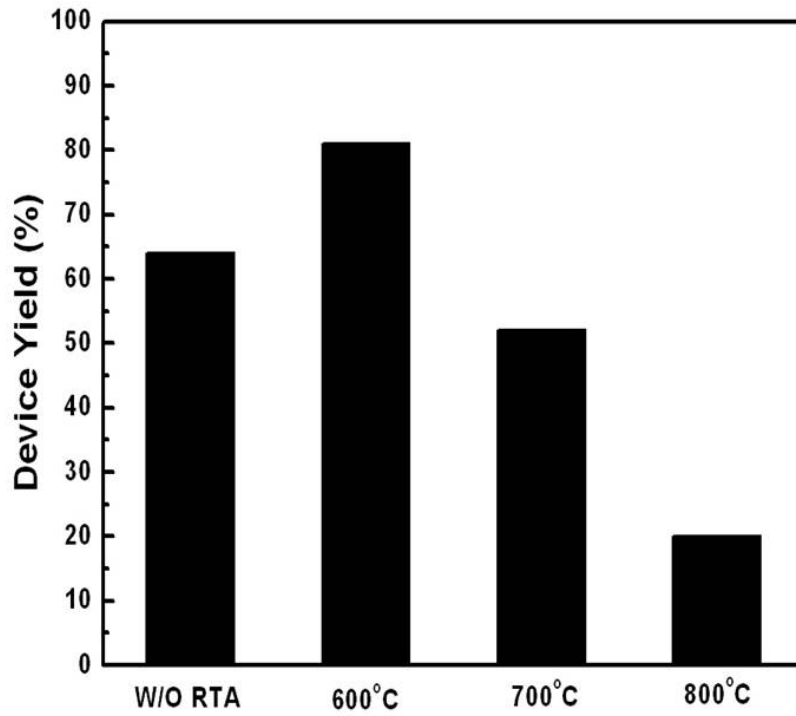

Fig. 3-43 Device Yield of pure-SZO without RTA and with O_2 RTA for 60 sec.

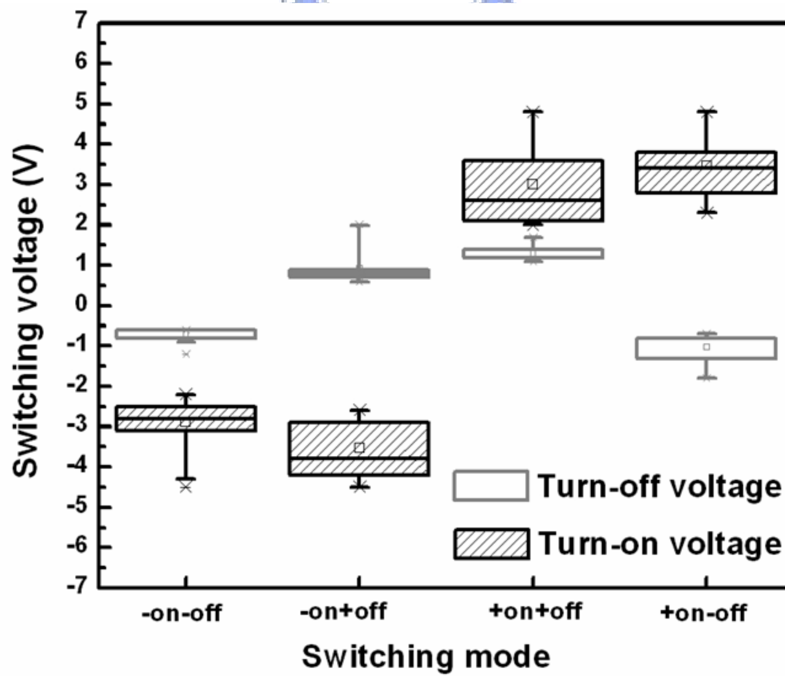

Fig. 3-44 The statistics of four mode switching voltage for W/O RTA pure-SZO.

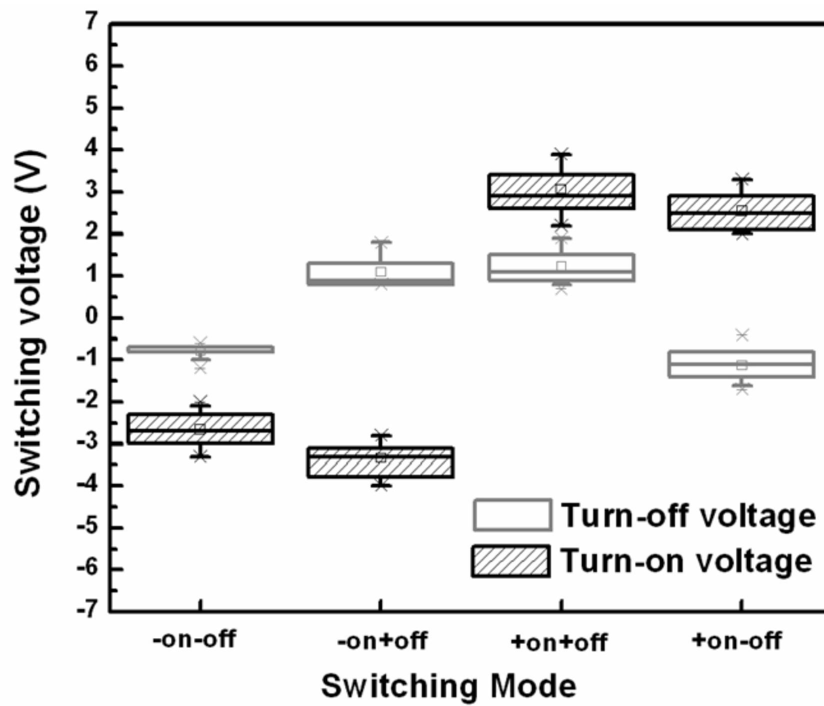

Fig. 3-45 The statistics of four mode switching voltage for O_2 RTA 600℃ for 60 sec pure-SZO.

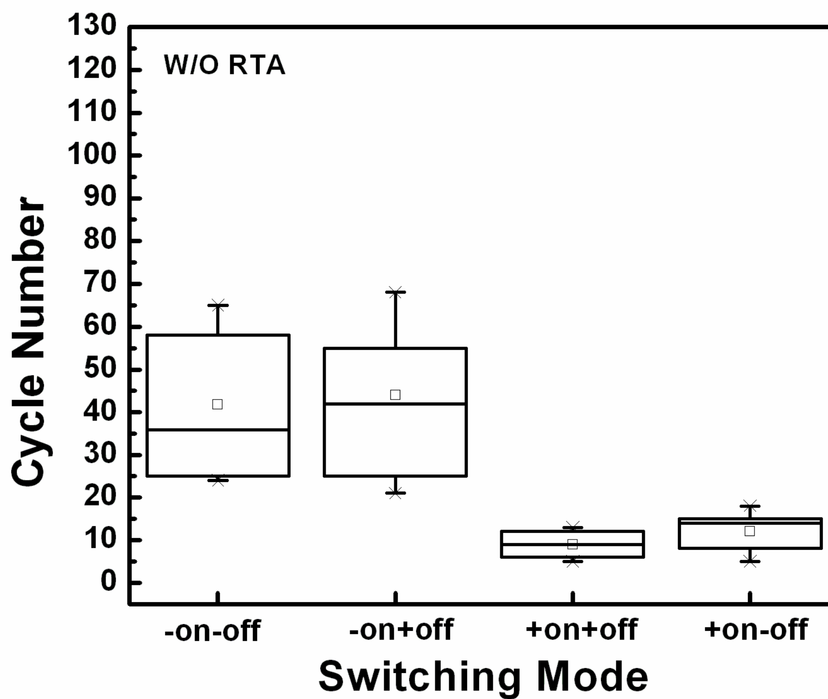

Fig. 3-46 The statistics of cycle number for W/O RTA pure-SZO.

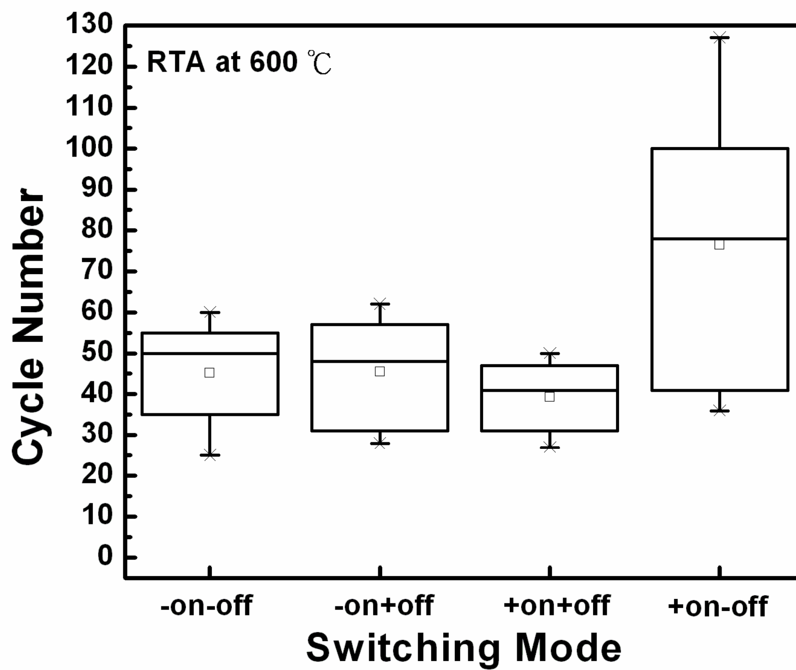

Fig. 3-47 The statistics of cycle number of pure-SZO with O_2 RTA 600℃ for 60 sec.

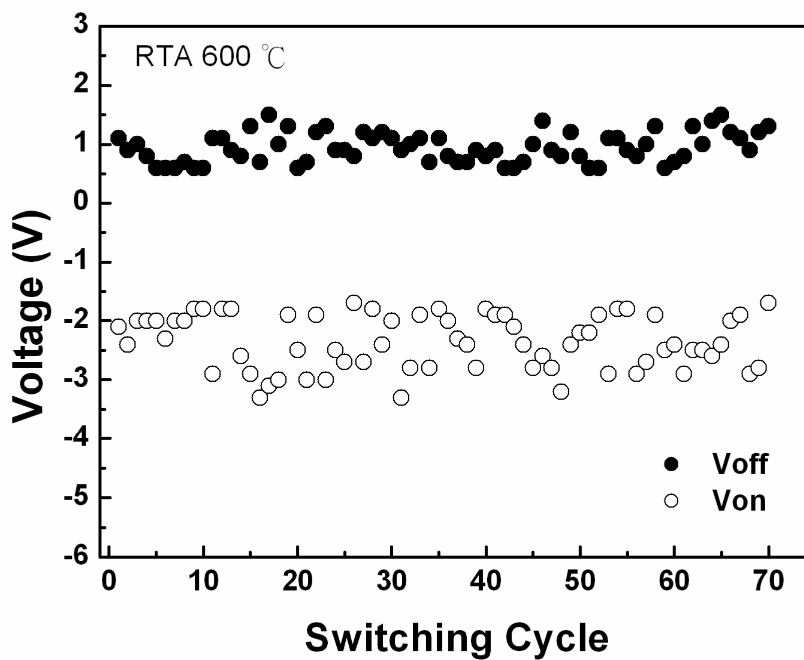

Fig. 3-48 Variation of switching voltage of pure-SZO with O_2 RTA 600℃ in -on+off mode.

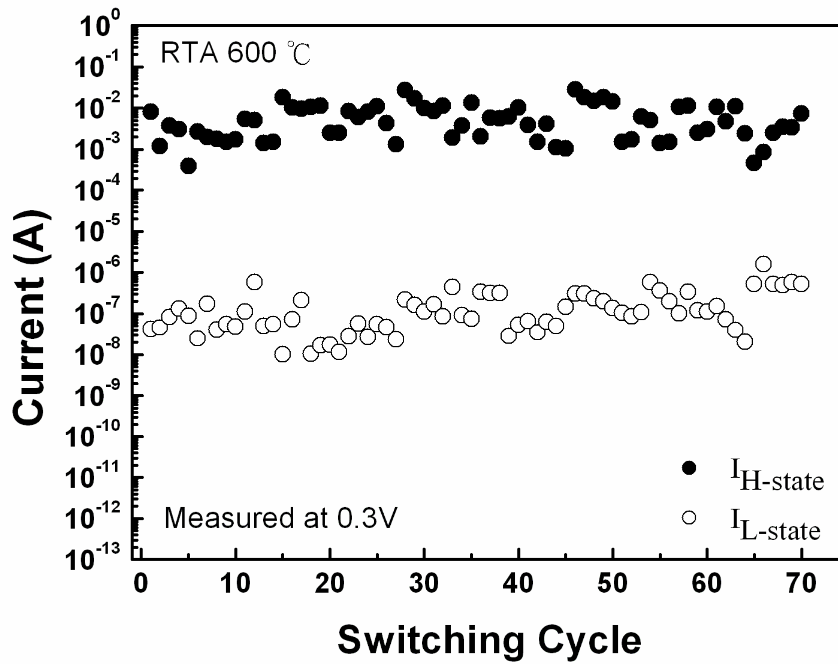

Fig. 3-49 Variation of two current state of pure-SZO with O_2 RTA 600℃ in -on+off mode.

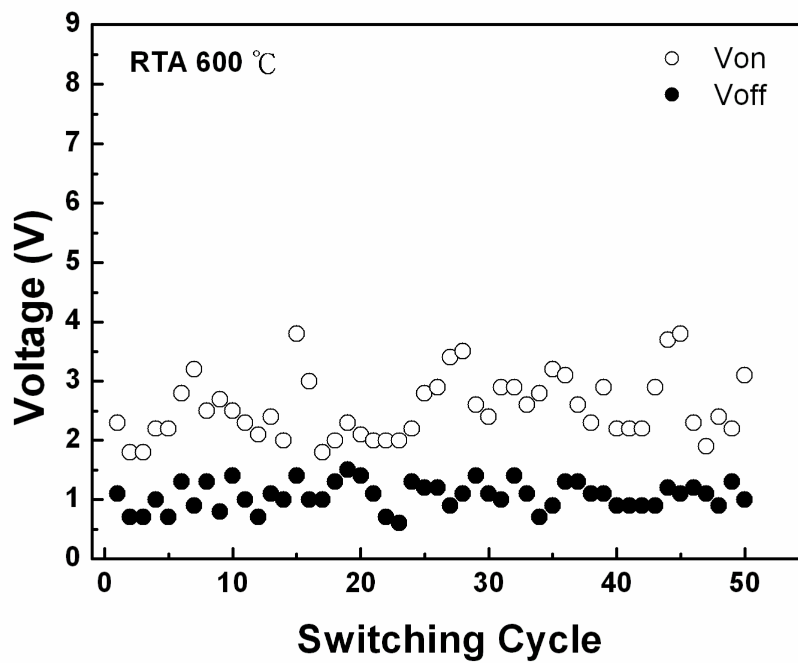

Fig. 3-50 Variation of switching voltage of pure-SZO with O_2 RTA 600℃ in +on+off mode.

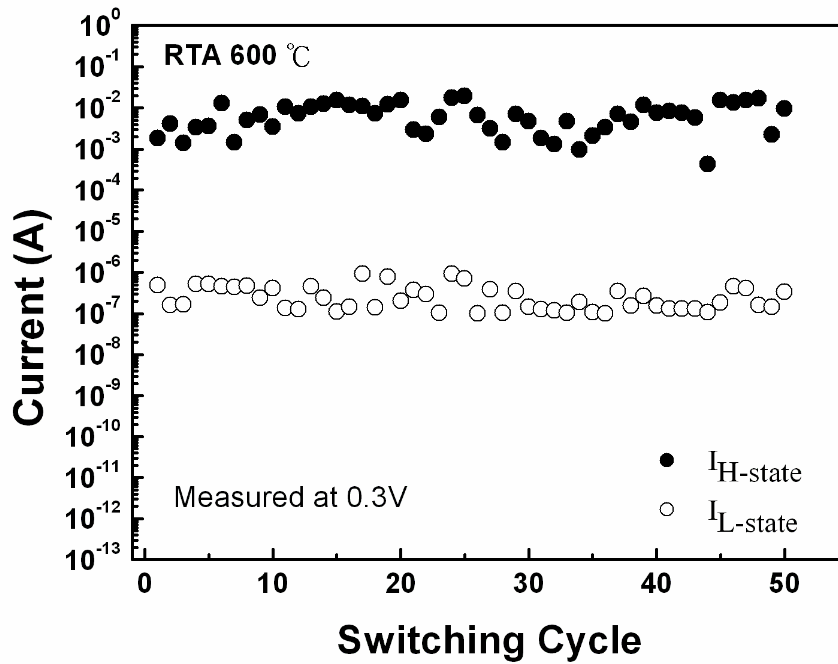

Fig. 3-51 Variation of two current state of pure-SZO with O_2 RTA 600℃ in +on+off mode.

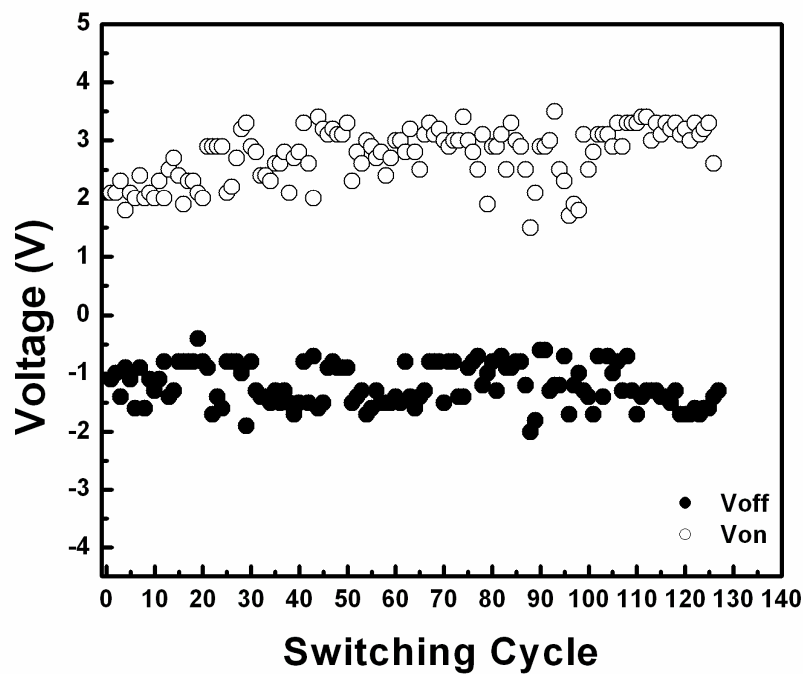

Fig. 3-52 Variation of switching voltage of pure-SZO with O_2 RTA 600℃ in +on-off mode.

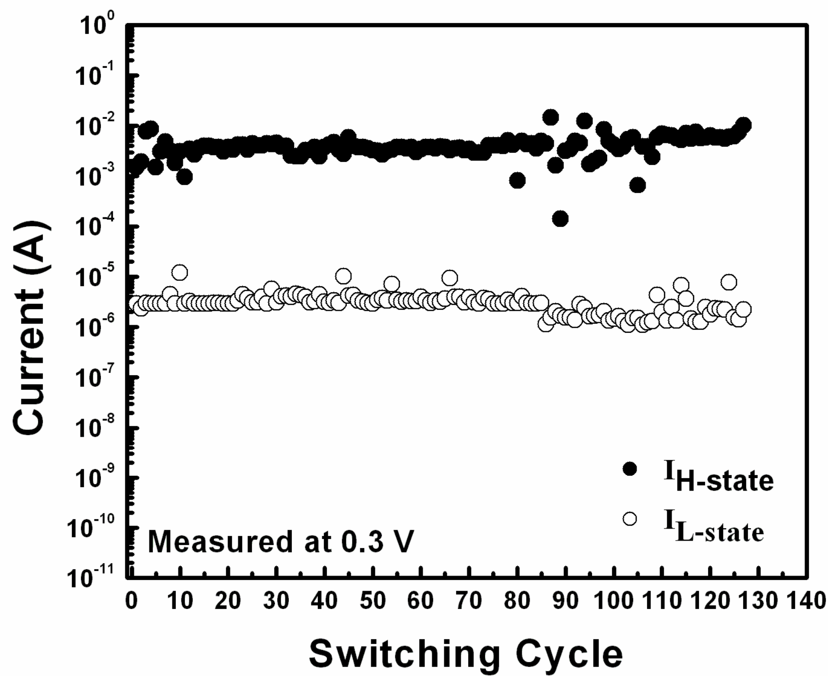

Fig. 3-53 Variation of two current state of pure-SZO with O_2 RTA 600℃ in +on-off mode.

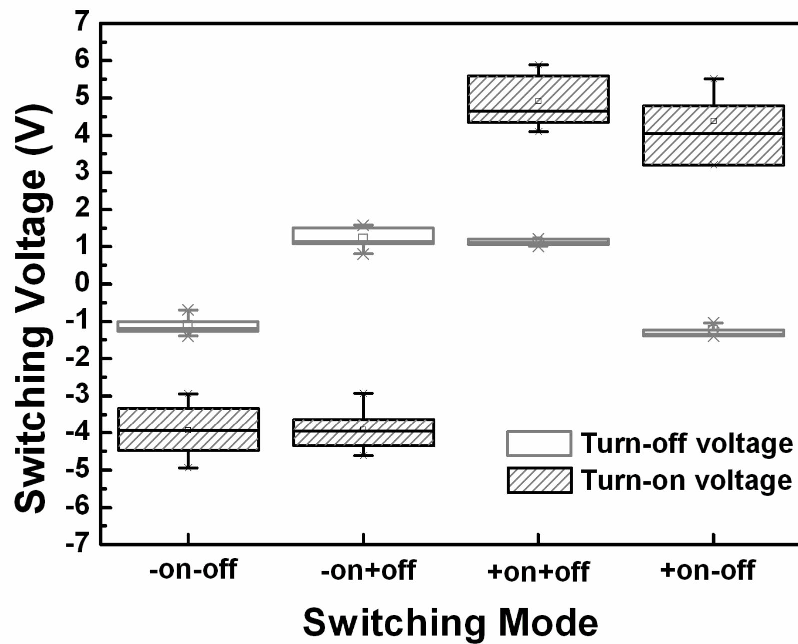

Fig. 3-54 The statistics of four mode switching voltage of pure-SZO with O_2 RTA 600℃ for 5 sec.

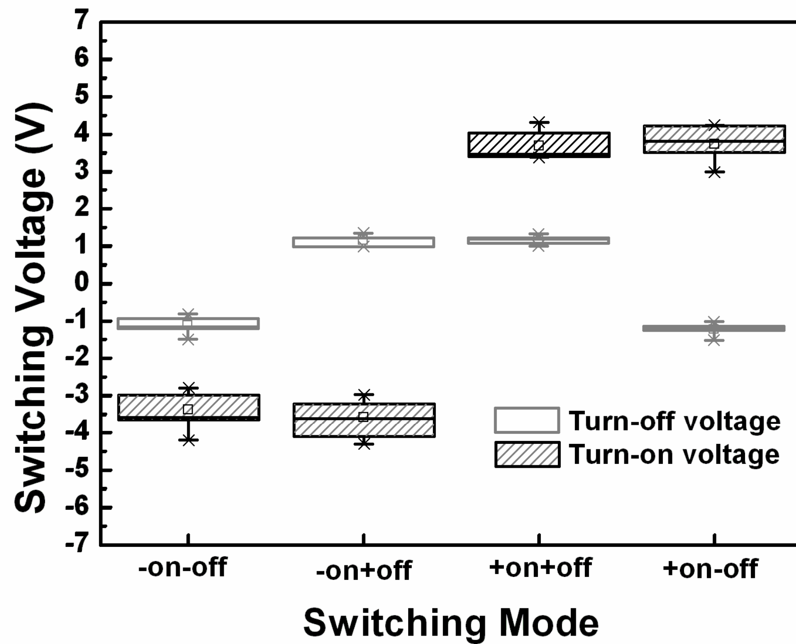

Fig. 3-55 The statistics of four mode switching voltage of pure-SZO with O_2 RTA 600℃ for 30 sec.

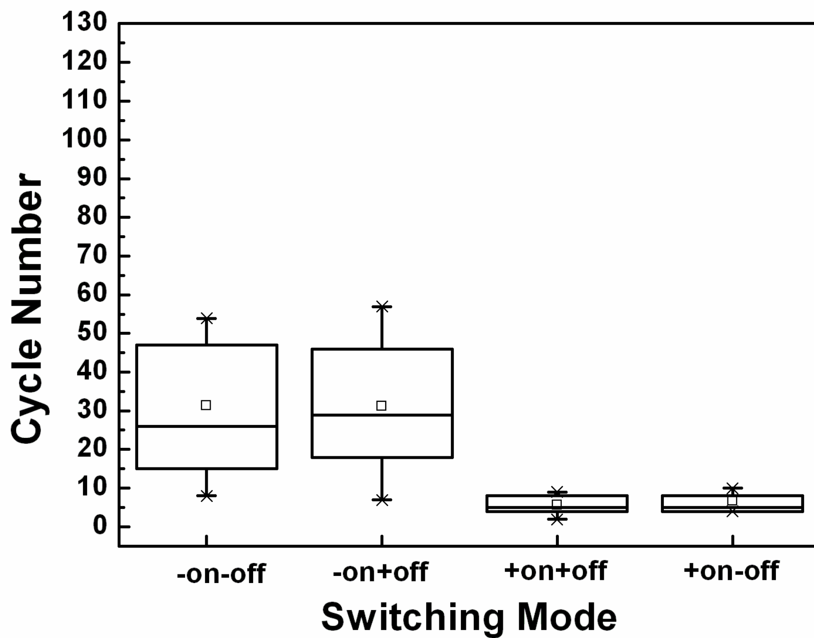

Fig. 3-56 The statistics of cycle number of pure-SZO with O_2 RTA 600℃ for 5 sec.

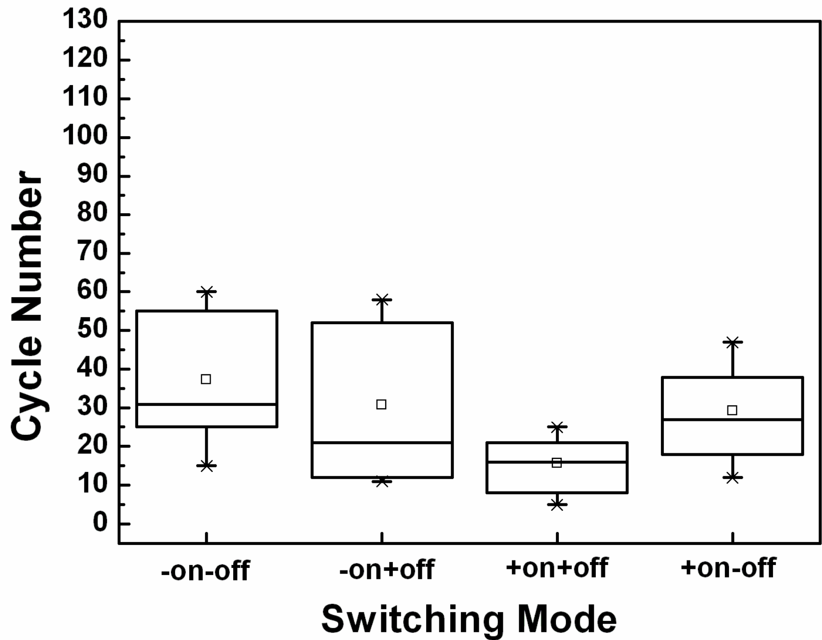

Fig. 3-57 The statistics of cycle number of pure-SZO with O_2 RTA 600℃ for 30 sec.

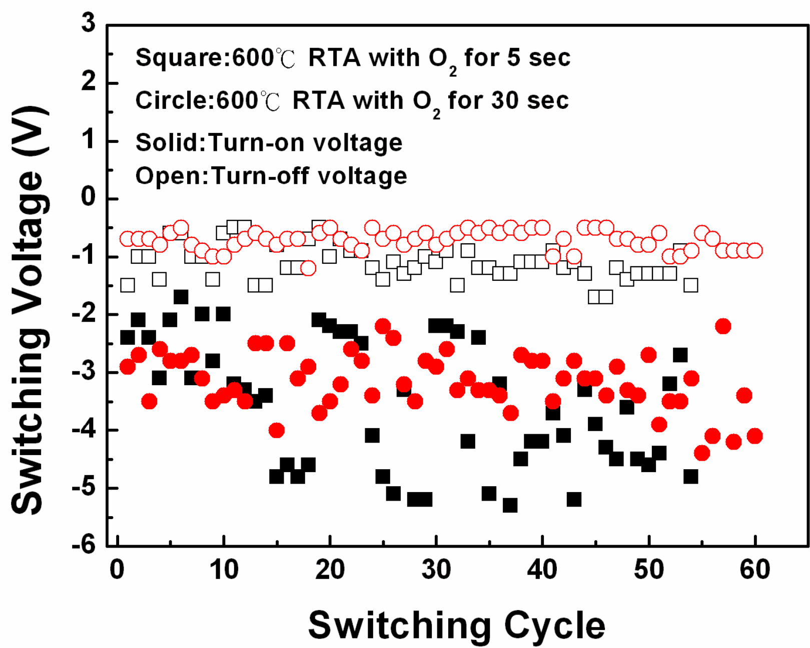

Fig. 3-58 Variation of switching voltage of pure-SZO with O_2 RTA 600℃ for 5 and 30 sec.

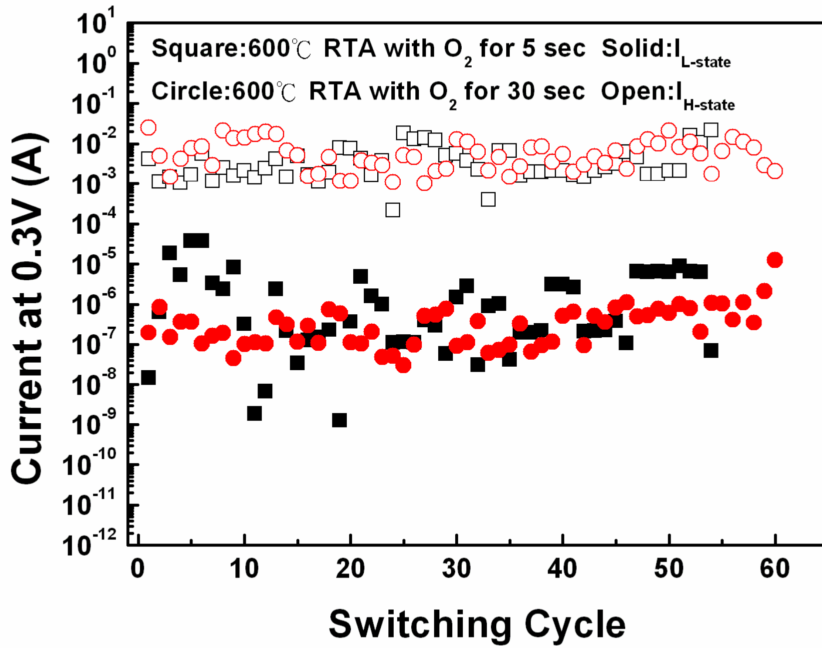

Fig. 3-59 Variation of two current state of pure-SZO with O_2 RTA 600℃ for 5 and 30 sec.

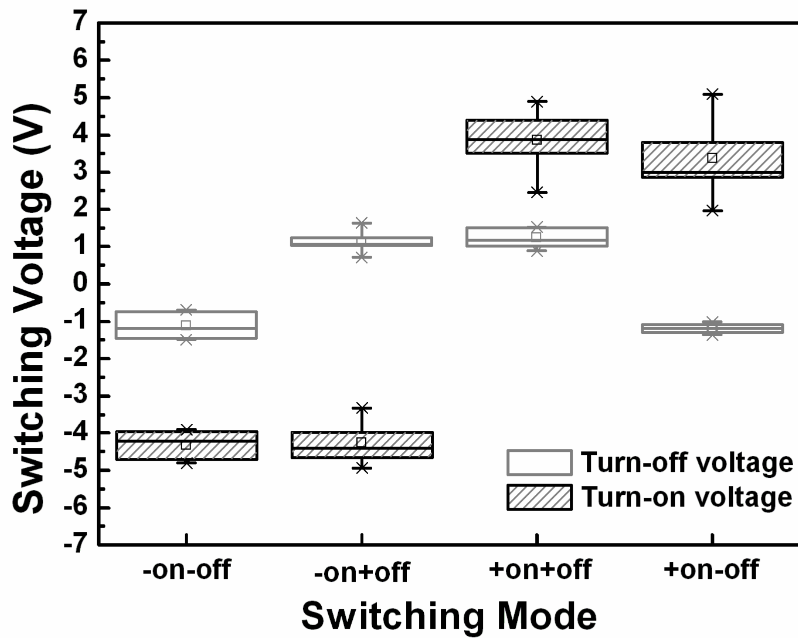

Fig. 3-60 The statistics of four mode switching voltage of pure-SZO with N_2 RTA 600℃ for 60 sec.

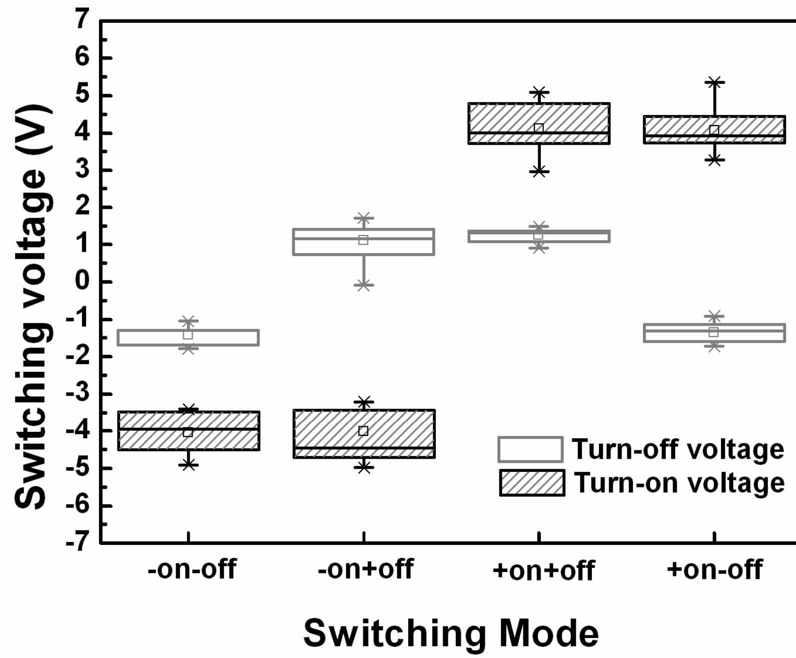

Fig. 3-61 The statistics of four mode switching voltage of pure-SZO with Ar RTA 600℃ for 60 sec.

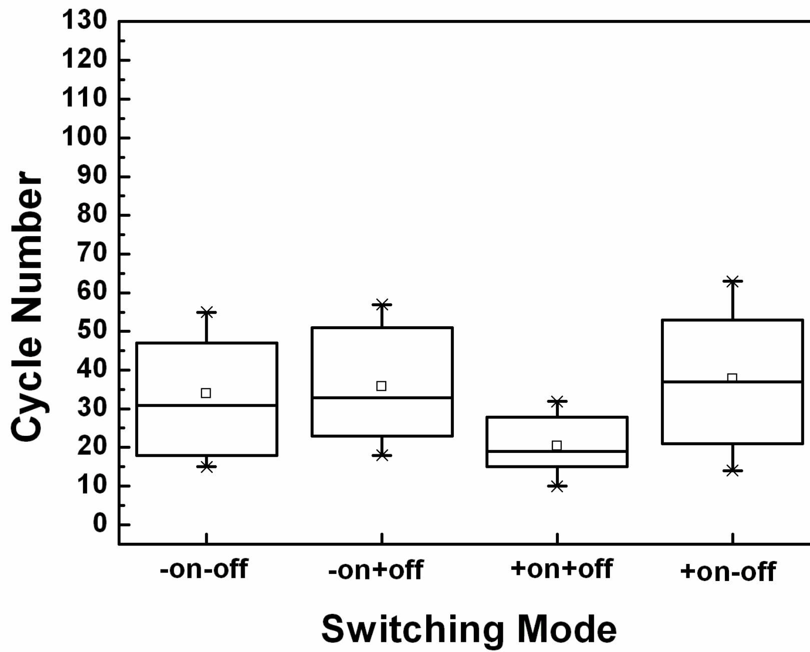

Fig. 3-62 The statistics of cycle number of pure-SZO with N_2 RTA 600℃ for 60 sec.

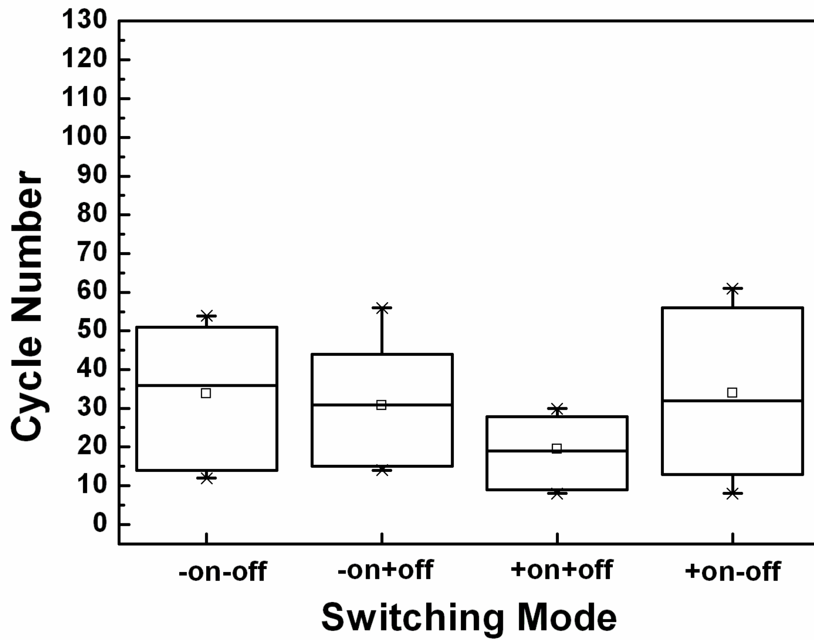

Fig. 3-63 The statistics of cycle number of pure-SZO with Ar RTA 600℃ for 60 sec.

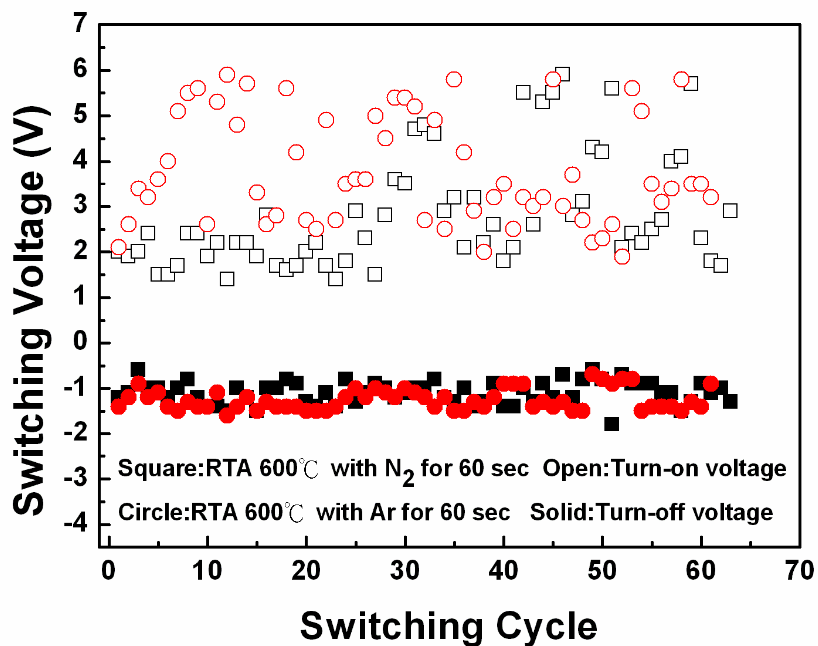

Fig. 3-64 Variation of switching voltage of pure-SZO with N_2 and Ar RTA 600℃ for 60 sec.

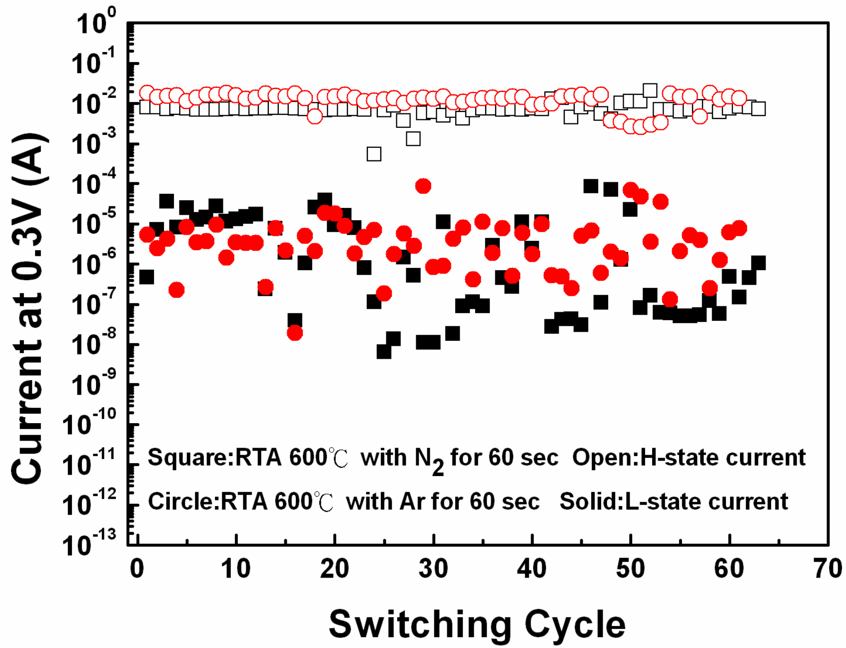

Fig. 3-65 Variation of two current state of pure-SZO with N_2 and Ar RTA 600℃ for 60 sec.

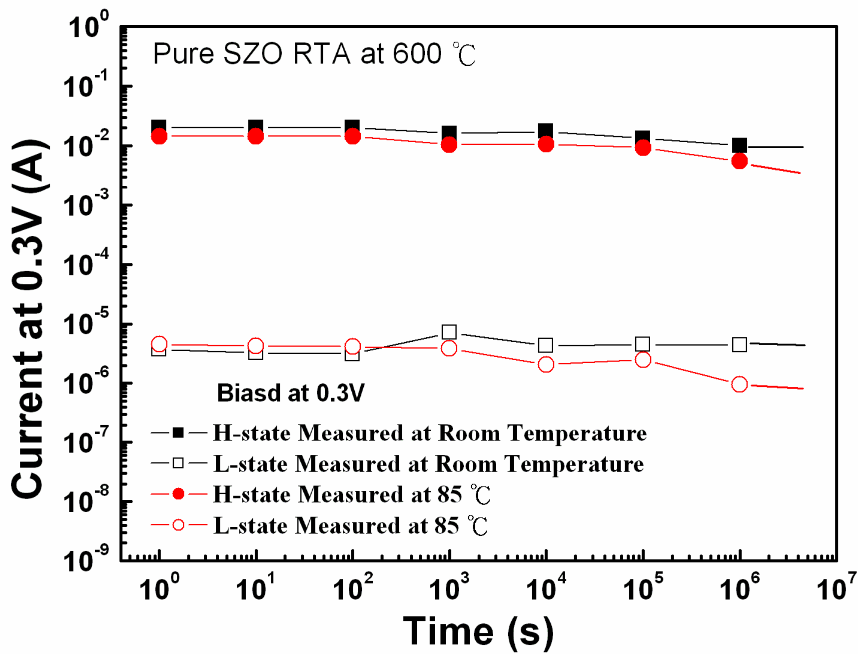

Fig. 3-66 Retention of O_2 RTA 600℃ for 60 sec pure-SZO memory film device at RT and 85℃.

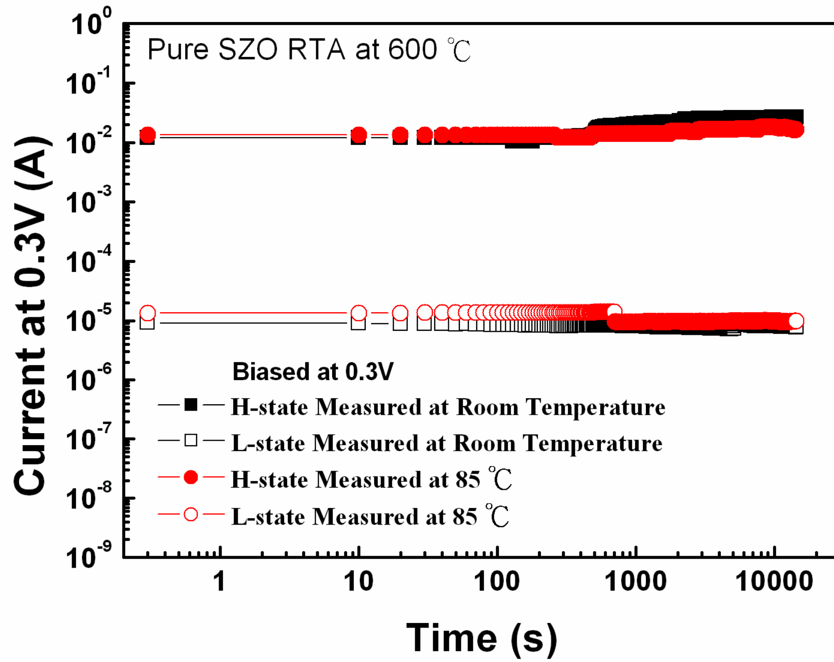

Fig. 3-67 Voltage stress of O_2 RTA 600℃ for 60 sec pure-SZO memory film device measured at RT and 85°C.

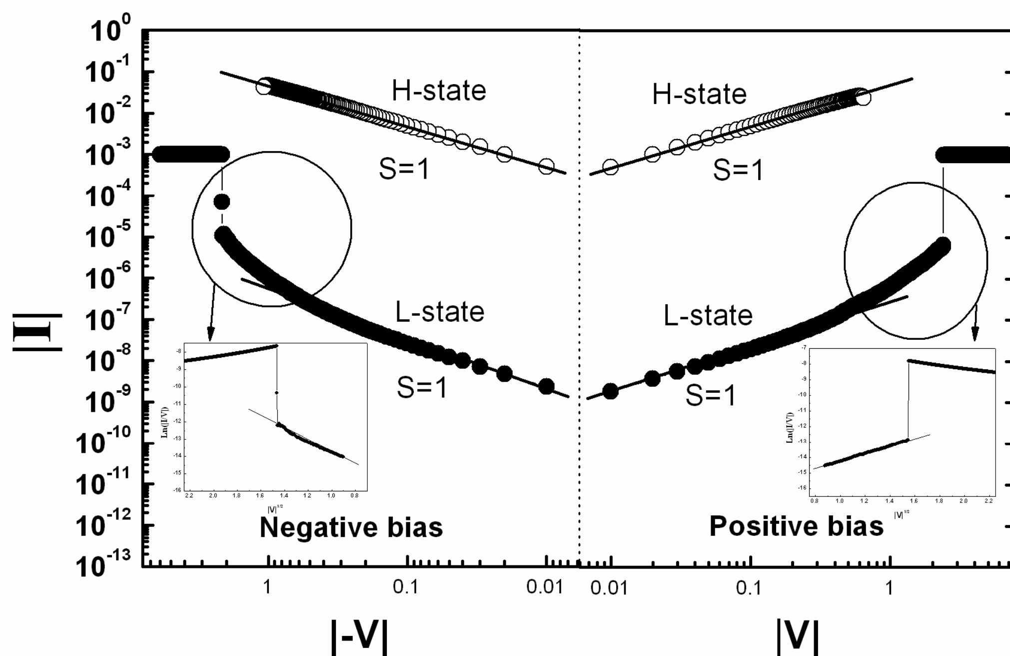

Fig. 3-68 The I-V curves of H-state and L-state in double logarithmic plots for positive and negative bias voltage, and the inset shows the plots of Ln(|I/V|) as a function of $|V|^{1/2}$ of L-state at high field region for the O_2 RTA 600℃ for 60sec pure-SZO film.

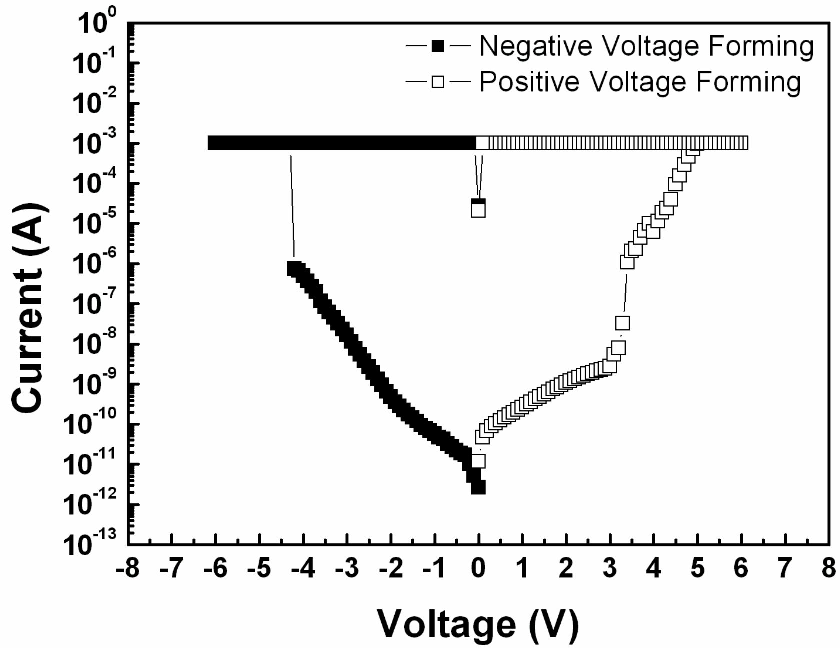

Fig. 3-69 The forming process of W/O RTA pure-SZO by negative and positive bias voltage.

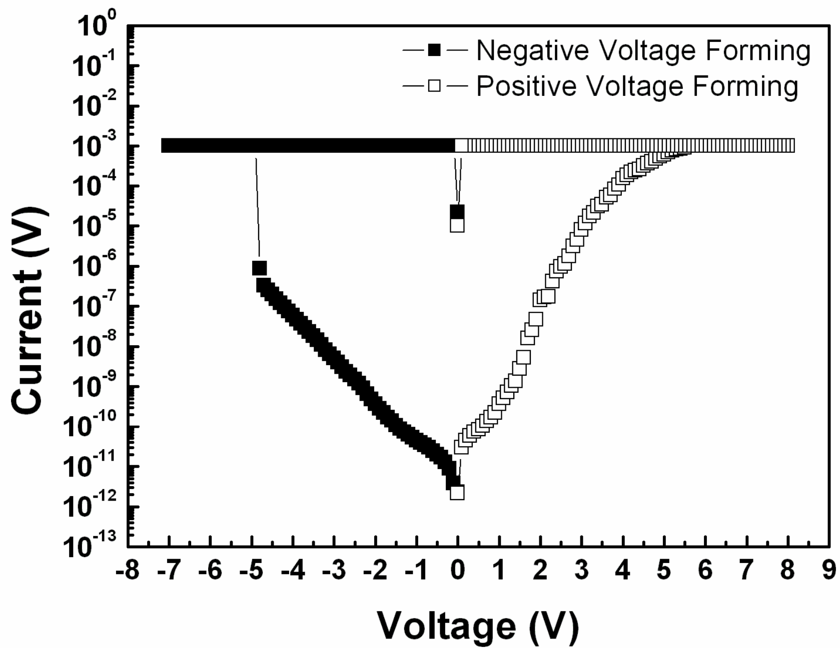

Fig. 3-70 The forming process of RTA 600℃ pure-SZO by negative and positive bias voltage.

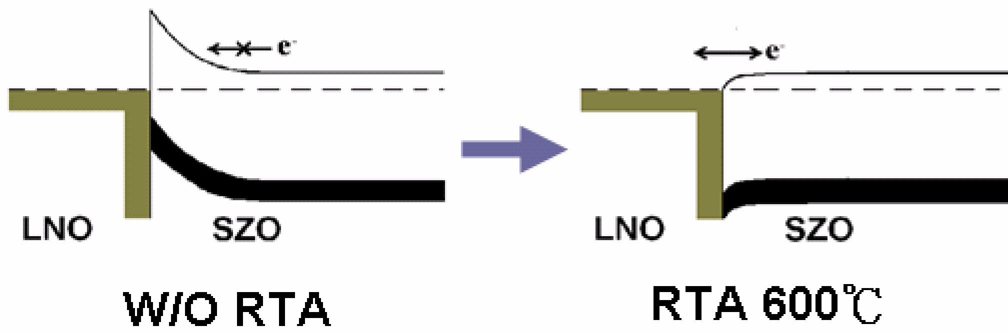

Fig. 3-71　Hypothetical diagram of barrier modulation by RTA thermal treatment.

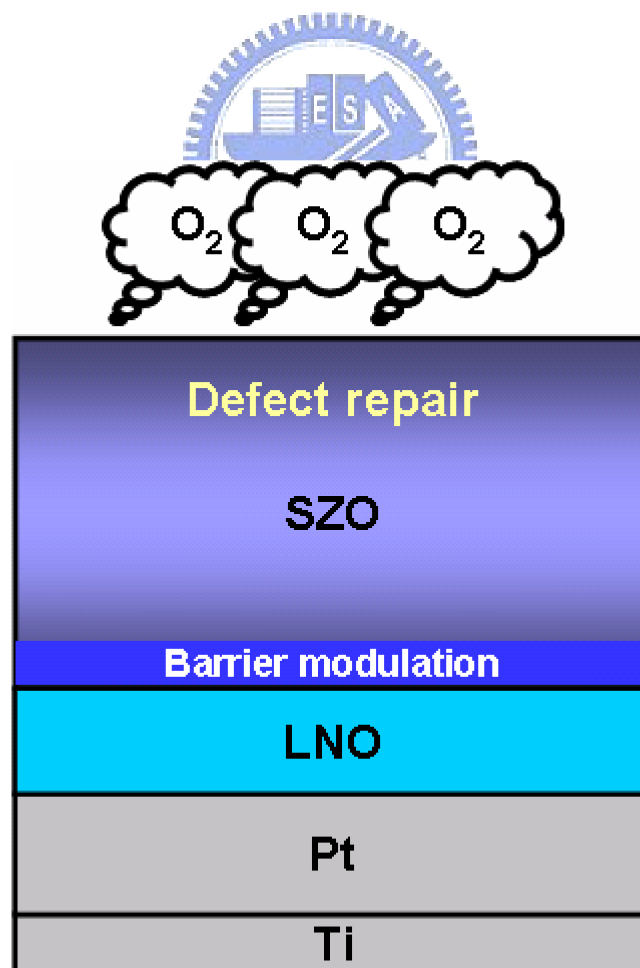

Fig. 3-72　Hypothetical diagram of RTA process and possible mechanism.

Chapter 4

Conclusions

The experimental results reported in this thesis indicate that the resistive switching properties significantly are affected by the V-doping and thermal treatment effects. The turn-on voltage increases with V-doping concentration. This is due to the formation of shallow defects would be suppressed by V-doping. And the pure-SZO has the lowest turn-on voltage. L-state resistance and resistance ratio are increased with V dopant concentration. The conduction mechanism of L-state at low field dominated by ohmic conduction, and carriers transport through shallow defects. At high field dominated by Frenkel-Poole emission, and the most carriers transport through deep defects. Then, the voltage sweep to H-state, the current paths would be formed by deep defects. The conduction mechanism of H-state is dominated by ohmic conduction. The turn-on voltage of pure-SZO is the lowest, and the power consumption is also the lowest. But the turn-on voltage is unstable. Then, the unstable switching property would be improved by thermal treatment RTA 600℃ with O_2 for 60 sec, and the device yield also increased by RTA thermal treatment. The defects would be repaired in SZO film by RTA 600℃ with O_2. The RTA 600℃ pure-SZO memory device has the stable switching property. And the cycle number of turn-on by positive bias voltage operation mode increased by RTA 600℃. The thermal treatment would decrease the defects of LNO/SZO interface, and the barrier of LNO/SZO interface would be reduced by RTA 600℃. RTA 600℃ with O_2 for 60 sec is the best thermal treatment condition for pure-SZO, which has stable switching property and shows good nondestructive readout properties and storage ability at room temperature and 85 ℃. The endurance exceed 120 times. Therefore, the Al/O_2 RTA 600℃

pure-SZO/LNO/Pt memory device having good switching properties and memory characteristics is a possible candidate for next-generation NVM applications.

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