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所提論文：利用齊納接面改善氧化矽/氮化矽/氧化矽堆疊式快閃記憶體之特性

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利用齊納接面改善氧化矽/氮化矽/氧化矽
堆疊式快閃記憶體之特性

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摘要

目前論文的題目主要是以探討在現今被廣泛使用的浮動閘極(Floating Gate)非揮發性記憶體。就快閃記憶體而言，通常會遇到兩個問題：首先是在元件的穿隧氧化層厚度小於10奈米時，雖可改善快閃記憶體的讀寫速度，但電荷保存時間亦隨之下降。再來是經過多次讀寫後在穿隧氧化層品質容易劣化而產生漏電路徑，而一旦有一條漏電路徑產生，所有儲存在浮動閘極的電荷都會經由此漏電路徑而全部流失掉，這也是目前浮動閘極非揮發性記憶體最嚴重的問題。

氧化矽/氮化矽/氧化矽堆疊式（SONOS）結構的記憶體元件，是使用氮化矽作為電荷陷捕層，在此種結構內，因為電荷是被儲存在分離式的陷捕位置中，故可改善在浮動閘極結構中對於資料保存性的問題。但是因為氮化矽與穿隧氧化層之間的導電帶位能差太低，會使得元件的寫入/抹除(program/erase)速度降低，而現在記憶體的基本要求不外乎在加快寫入/抹除的速度，增加資料保存的期限（retention），在連續的寫入/抹除的重複性動作下，去提升元件對此動作的忍受度（endurance）。

而在本篇論文中，我們將在源極（source）端和汲極（drain）端形成一個齊納接面（Zener junction），利用齊納接面（Zener junction）的特性去改善傳統氧化矽/氮化矽/氧化矽堆疊式快閃記憶體（SONOS）的寫入及抹除的特性。

在本篇論文的第二章中，首先探討不同條件的齊納接面對P型基板之SONOS記憶體元件的寫入及抹除速度帶來的影響，並且進一步觀察此齊納接面是否對元件其他的特性有負面影響，並分析元件特性的原理。

在本篇論文的第三章中，探討不同條件的齊納皆面對N型基板之SONOS記憶體元件的寫入及抹除速度產生的影響，並同時觀察記憶體其他特性，受到齊納接面結構影響後，是改善或者劣化，最後會分析元件特性的原理。

在本篇論文的第四章中，會做一個簡單的結論，比較n-channel和p-channel之間的優缺點。

Study on SONOS Flash Memory with Zener Junction at Source/Drain Side

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Department of Electronics Engineering &
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ABSTRACT

The topic of the paper is the floating gate non-volatile flash memory which is extensively used in the present. For the non-volatile flash memory, there are two problems： First, when the thickness of tunneling oxide is scaled down to 10 nano-meter, the programming speed of flash memory is improved, but the retention time is decreased. Second, after the programming and erasing operation cycles, it will cause the tunneling oxide damage and make the oxide quality degradation. The oxide damage would generate a leakage path which will cause the charges stored in floating-gate layer lost by the leakage path. The leakage issue is the most serious problem of the floating-gate non-volatile flash memory.

In order to solve the leakage path problem, we use the silicon-oxide/silicon-nitride/silicon-oxide stack structure memory device. The silicon-nitride layer is used to be the charge trapping layer. Because the charge stored in the trapping is in the discrete trapping site in the stack structure device, it can improve the data retention reliability compared with the floating-gate flash memory. Because of the difference of conduction band between silicon-nitride trapping layer

and silicon-oxide tunneling layer is too small, the programming speed and the erasing speed of the stack structure will decrease. But the operation speed, well data retention reliability, and the endurance of the device under the stress by the repeated program and erase cycles in the memory device are the most important requirements.

In the thesis, we will form a Zener junction at the source side and the drain side, then we employ the Zener junction to improve the program and erase characteristic of SONOS stack structure memory.

In the Chapter 2, we will use the different dose of boron doping to perform the reverse halo implantation. Then we would discuss the effect on the programming speed and the erasing speed of P-type substrate SONOS memory with the different condition of the Zener junction. Finally, we will observe if the Zener junction caused the degradation on the other characteristics of memory, and explain these phenomenons further.

In the Chapter 3, we will talk about the effects on the characteristics of the n-type substrate SONOS memory , especially on the programming and erasing speed. We use the different does of phosphorus doping to accomplish the reverse halo implantation. And we would observe the characteristics of SONOS memory such as programming speed, erasing speed, data retention, endurance, and so on. Finally, we will find the theorem to explain the phenomenon. At last, we will give an conclusion in Chapter 4.

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CHAPTER 1

INTRODUCTION

1.1 Overview of Flash Memory

Because of the memory devices used in the currently 3C products widely, such as mobile capabilities, Personal Digital Assistant (PDA), Digital Camera, computer, and some other electric consumer products, as figure 1-1 shows. Hence the memory device technology is developing rapidly in present.

The semiconductor memories based on complementary CMOS (metal-oxide-semiconductor) technology can be divided into two main parts by whether the storage data can be kept without power supply. If the memory devices can not keep the data without power supply, we call these memory devices as the volatile memory. And the other memory devices can keep data without power supply called the non-volatile memory. The volatile memory: like static random access memory (SRAM) and dynamic random access memory (DRAM). The non-volatile memory: like electrically programmable read only memory (EPROM), electrically erasable programmable read only memory (EEPROM), and the flash memory. We show them in figure 1-2.

The most explosive growth field of the semiconductor is the flash memory. The advantages of the flash memory are that it can be electrically written and erased more than 100k times with byte programming and sector erasing and being with the smallest cell size [1]-[2].

In 1967, the first floating gate non-volatile semiconductor memory was invented by S. M. Sze and D. Kahng at Bell Labs [3]. The conventional floating gate memory used poly-silicon as a charge storage layer surrounded by the dielectric [1], as figure 1-3. The floating gate structure can achieve high densities, good program/erase speed, and good reliability for flash memory application. But the floating gate memory meets the limitation of scaling down. When the tunneling oxide thickness was scaled down to 10nm, the charge stored in the poly-silicon floating gate would be easy to leak by a leakage path of the tunneling oxide or direct tunneling current, as figure 1-4. The reason of the leakage path forming is that some defect would generate during repeated write/erase cycles.

In order to reach higher cell density, the scaling down issue of the memory devices is unavoidable. First, we must solve the leakage problem of the floating gate memory with the thickness of the tunneling oxide thinner than 10nm. The SONOS (Poly-silicon/Oxide/Nitride/Oxide/Silicon) stack structure flash memory has been invented to solve the issue of the floating gate memory recently. SONOS memory has better charge retention ability than the floating gate memory when the tunneling oxide thickness reduced [4]-[5]. Because that the trapping sites in the nitride trapping layer are spatially isolated deep-level traps. Hence, a single leakage path in the tunneling oxide will not induce the whole charges in trapping layer lost [6], as figure 1-6. The structure of SONOS memory is depicted in Fig 1-5. The Id-Vg curve characteristic of the flash memory is shown in Fig 1-7 [7]. The shift of threshold voltage between program state and erase state is named memory window.

The SONOS memory solves the leakage path issue and has several advantages including fast programming, low power operation, high-density integration, and good endurance characteristics [8]-[11], but the retention characteristics of the SONOS memory are not good enough. Because the trapping sites in the nitride trapping layer of the SONOS memory are shallower trapping level. Hence, we need to make tunneling oxide and blocking oxide thicker, but it will decrease the operation speed [12]-[15]. To improve the programming and erasing speed of the SONOS memory with well retention characteristics is one of the most popular topics in the research today. There are many ways to improve the programming and erasing speed without retention degradation, such as using high-k dielectric as tunneling oxide [16]-[18]. When we apply a voltage on memory device, the partial voltage on the tunneling oxide is larger. Then, we can enlarge tunneling oxide energy band bending to increase programming and erasing speed. But the high-k material has some new troubles, like the compatibility to the process flow today, the stability under high temperature process environment, and so on. Here, we do not use the high-k material to improve the programming and erasing speed of the SONOS memory. Instead of the high-k material techniques is using heavily reverse type halo-implantation to from the Zener junction by the side of the drain in the channel.

1.2 Motivation

When the problem of the leakage path inducing charge stored in the floating gate memory lost was solved by the SONOS stack structure memory, the new problem of the SONOS memory is coming together. The discrete trapping site solved the charge lost issue in the floating gate memory, but it also caused the programming and erasing speed degradation at the same time. And the high-k material still has some troubles, like the compatibility to the process flow today, the stability under high temperature process environment. Hence, we use the reverse halo-implantation forming the Zener junction in the thesis to improve the programming and erasing speed without using high-k material. Using this method will not meet the problems of high-k material. Especially, we do not need add any more exposure and develop process steps to complement the reverse halo-implantation because it can be done in sequent process step with the source/drain implantation. By the reason, we don’t need one more masks, and the cost won’t add.

1.3 Thesis Organization

In this thesis, we study the performance of the SONOS stack structure memory device used the Zener junction to improve the programming and erasing speed.

In the Chapter 2, we will use the different dose of boron doping to perform the reverse halo implantation. Then we would discuss the effect on the programming speed and the erasing speed of P-type substrate SONOS memory with the different condition of the Zener junction. Finally, we will observe whether the Zener junction causing the degradation on the other characteristics of memory, and explain these phenomenon further.

In the Chapter 3, we will talk about the effects on the characteristics of the n-type substrate SONOS memory, especially on the programming and erasing speed. We use the different does of phosphorus doping to accomplish the reverse halo implantation. And we would observe the characteristics of SONOS memory such as programming speed, erasing speed, data retention, endurance, and so on. Finally, we will find the theorem to explain the phenomenon.

At the end of this thesis, we make a conclusion in chapter 4.

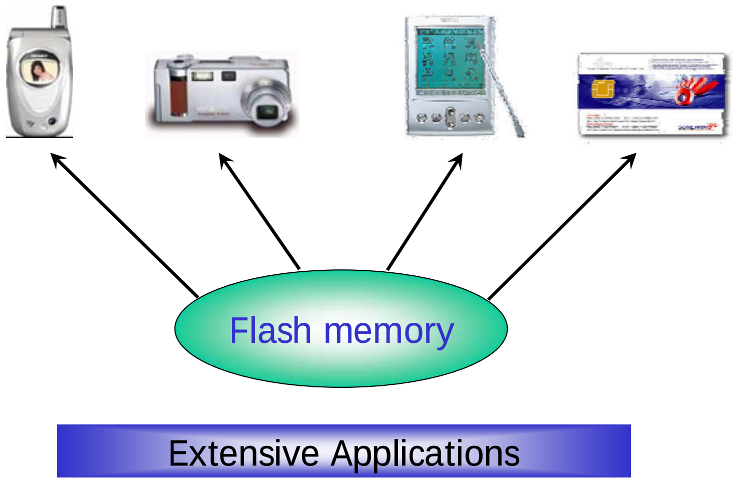

Fig. 1-1 The applications of flash memory

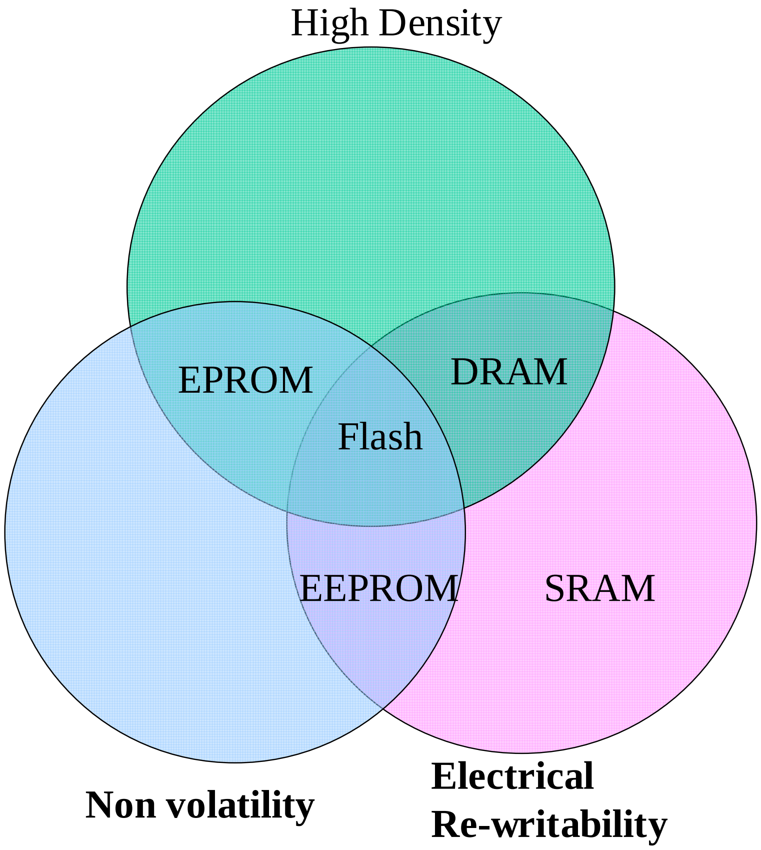

Fig. 1-2 The semiconductor memory

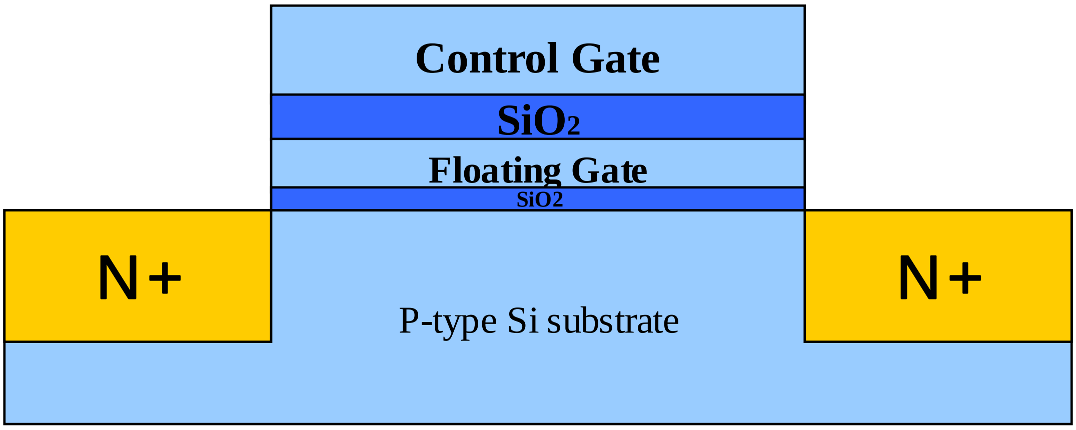

Fig. 1-3 Structure of floating gate memory

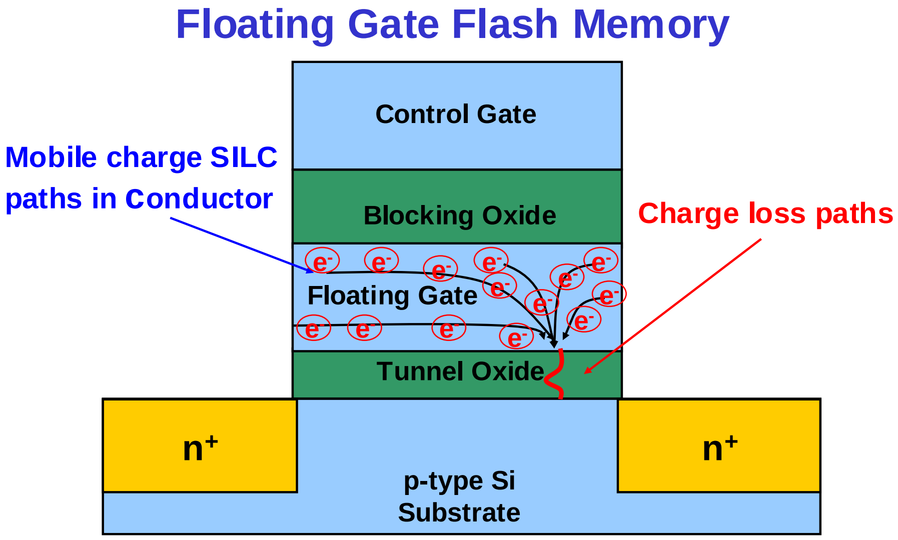

Fig. 1-4 Leakage paths induce all charge lost in the floating gate

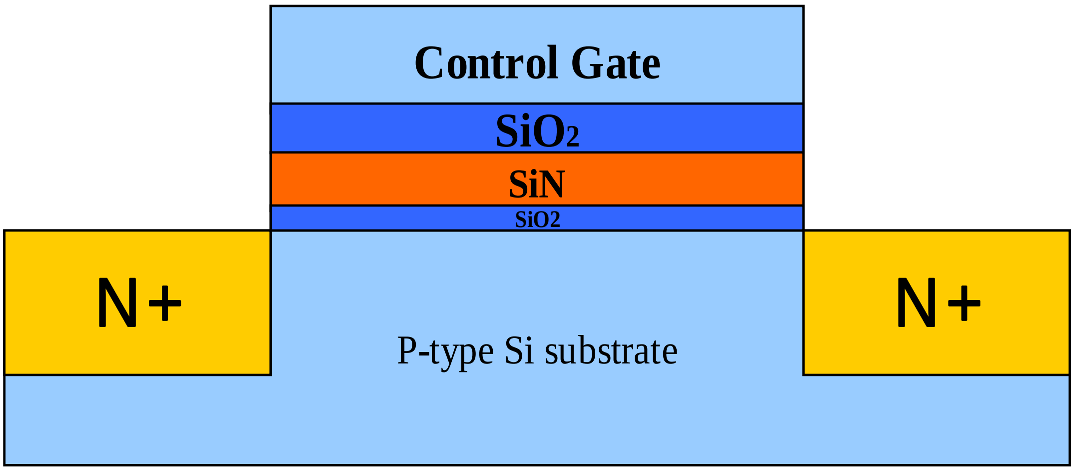

Fig 1-5 Structure of SONOS memory

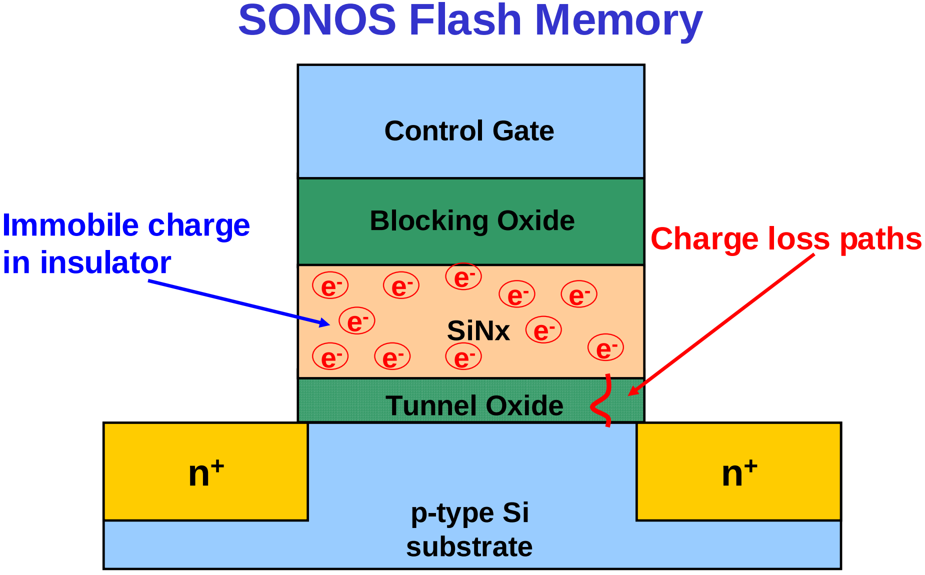

Fig. 1-6 Leakage paths induce partial charge lost in the Nitride trapping layer

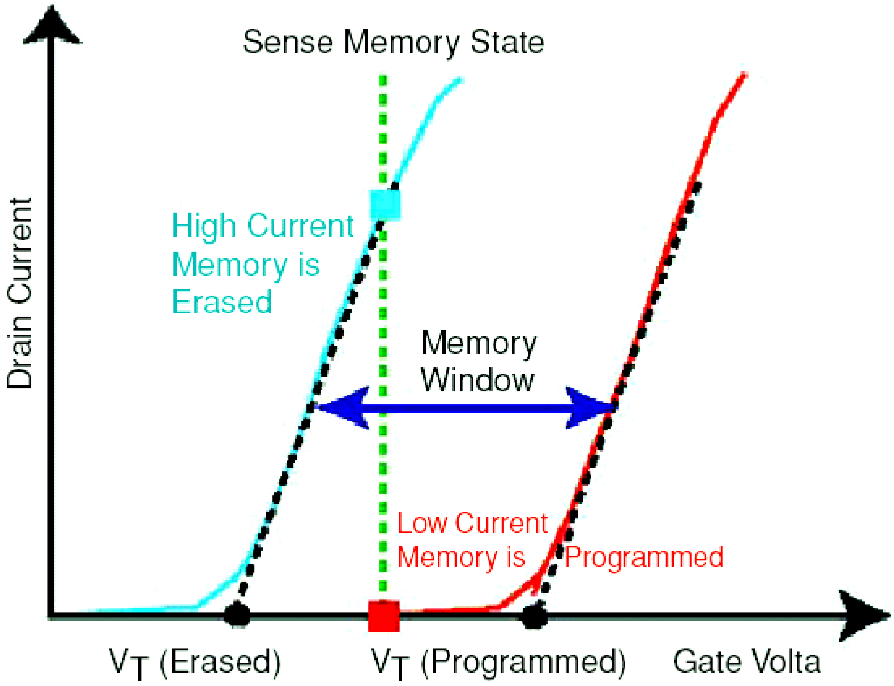

Fig 1-7 The Id-Vg curve the flash memory

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CHAPTER 2

Improve N-Channel SONOS Memory with Zener Junction

2.1 Introduction

Recently SONOS-type memory has received considerable interest as one of the most promising candidates to replace the conventional floating-gate flash memory. Because as the tunneling oxide thickness is scaled below 80Å, the stress-induced leakage current (SILC) [1]-[3] has become such a severe problem that it will be a formidable challenge for floating-gate devices to meet the 10-year retention requirement. However, for the SONOS devices, due to its discrete charge trapping nature, it is more robust to SILC since there is no lateral charges movement to discharge the whole memory as one single defect is generated in the tunnel oxide [4]. In addition SONOS memory has low operation voltage, better endurance, and good compatibility with conventional CMOS process. However, achieving fast programming and long retention at the same time remains to be one challenge for SONOS devices [5]-[8]. Various approaches have been proposed for improving the SONOS performance and reliability.

In this work, we purpose a high operation speed SONOS memory with using reverse halo implant in the channel near by Source / Drain sides to improve the programming / erasing speed. The problem of injection efficiency not enough high in the SONOS memory is solved by the method here. Hence we can both have higher injection efficiency and well data retention at the same time. And the higher operation speed can reduce the stress time, so that the endurance will be better in the Zener devices.

2.2 Experiment

Figure 2-1(a) ~ 2-1(k) schematically depicts the process flow of the proposed SONOS flash memory with Zener junction. The fabrication process of the Zener junction SONOS flash memory devices involved was started with the LOCOS isolation process on p-type, 5-10 ohm-cm, (100) orientation, 150 mm silicon substrates. First, the tunneling oxide was thermally grown at 1000℃ with N_2O and O_2 in vertical furnace system. The trapping layer Si_3N_4 was deposited at by low temperature chemical vapor deposition (LPCVD) at 780℃, 350mTorr. Then, we do a re-oxidation process step to slightly oxidize the surface of the nitride layer in order to improve the interface quality between the trapping layer and the blocking oxide (top oxide) layer. The locking oxide (top oxide) layer was deposited by LPCVD at 700℃, 300mTorr. Finally, the poly-gate was deposited by LPCVD at 660℃, 300mTorr. The thickness of poly-gate / oxide (blocking oxide) / nitride / oxide (tunneling oxide) are 200nm / 15nm / 8nm / 3nm respectively. Then, the gate was patterned by the exposure, development, and the etching step. Before the next implant steps, we deposited a oxide layer by LPCVD and then etch the oxide layer by dry etch process to from the sidewall spacer. The sidewall spacer is used to prevent the sidewall of the gate stack from being damaged during the implant process steps. For the n-channel SONOS memory devices, we first accomplished the reverse halo-implantation step using a tilt angle implantation with BF_2 ion to forming the p+ region. The dose and energy of the reverse halo implantation are shown in Table 2-1. The control devices is without the reverse halo implantation. Then, the source/drain n+ region was completed by P_{31} implant without tilt angle. The dose and energy of the P_{31} implant are 5E15 cm^{-2} and 30 keV. Then, the substrate contact was patterned and the sub-contact was implanted with BF_2 at the does 5E15 cm^{-2} and energy 40 keV. After these implantation process steps, the dopants were activated at 950℃ for 10 seconds by Rapid Thermal Anneal (RTA) system. Then, the 400nm passivation oxide was deposited by LPCVD. The contact holes were patterned and the Al metal deposition was done by PVD. Finally, we define the contact pad by metal etch.

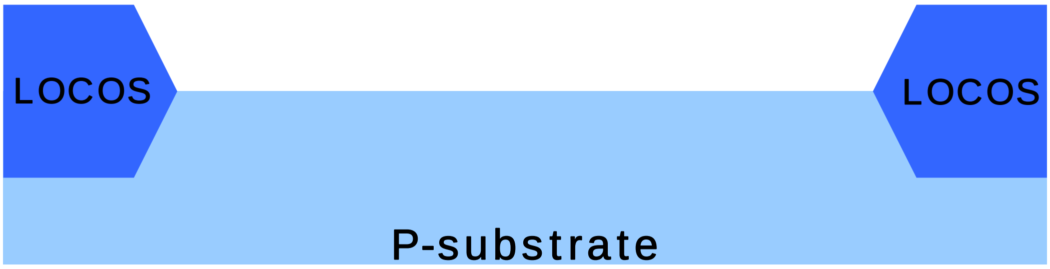


Fig. 2-1 (a)

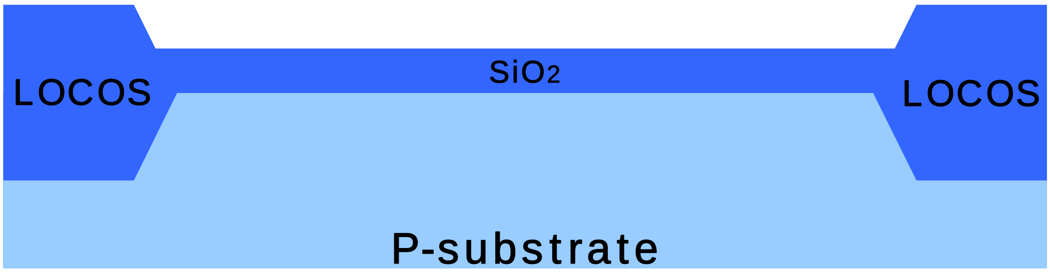


Fig. 2-1 (b)

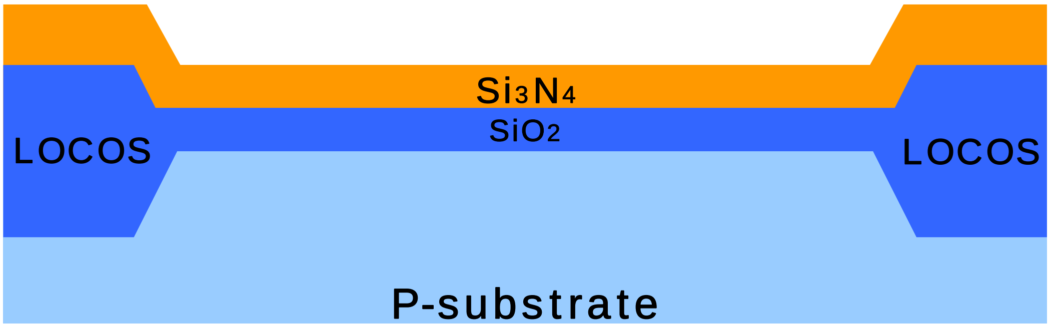


Fig. 2-1 (c)

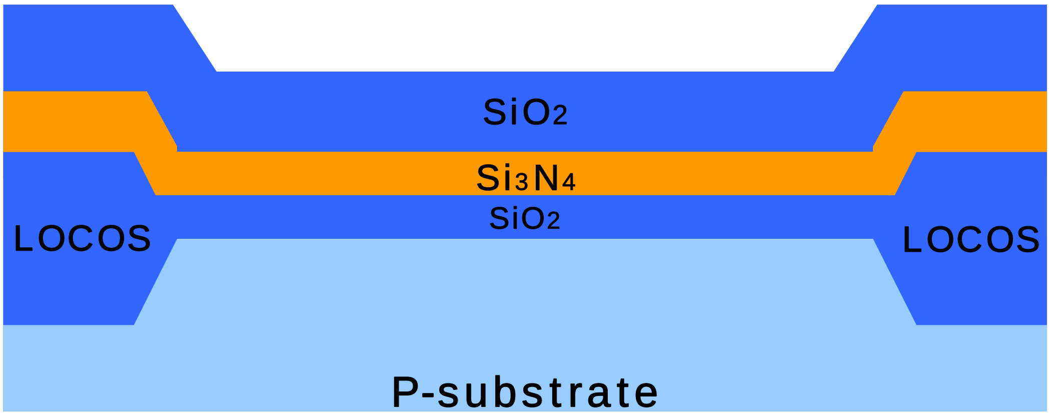


Fig. 2-1 (d)

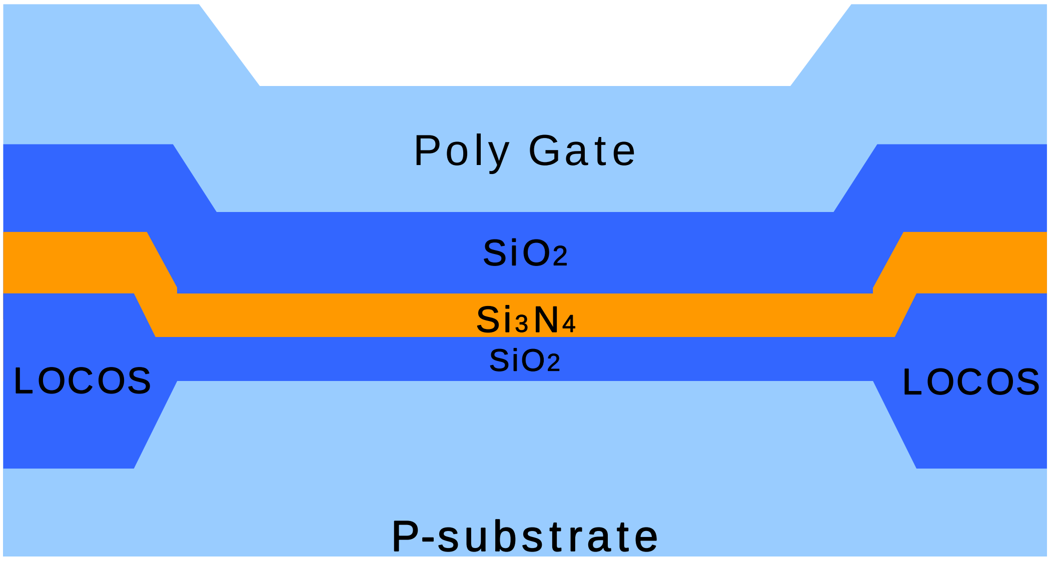


Fig. 2-1 (e)

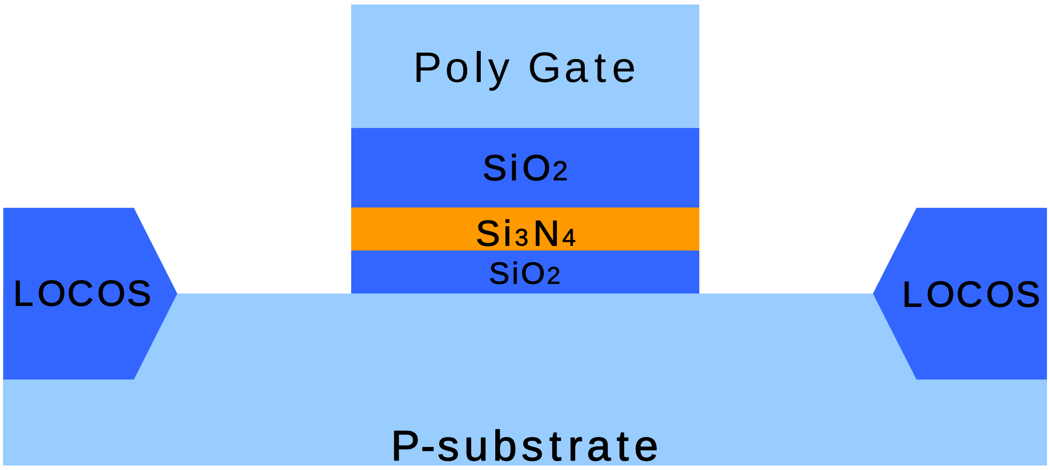


Fig. 2-1 (f)

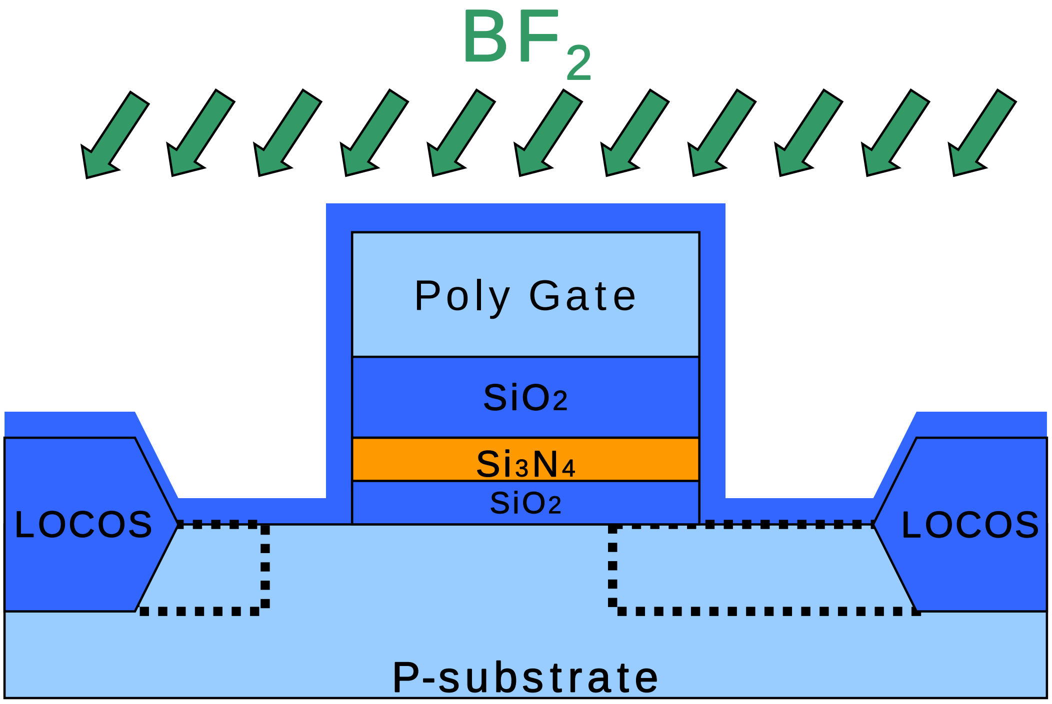


Fig. 2-1 (g)

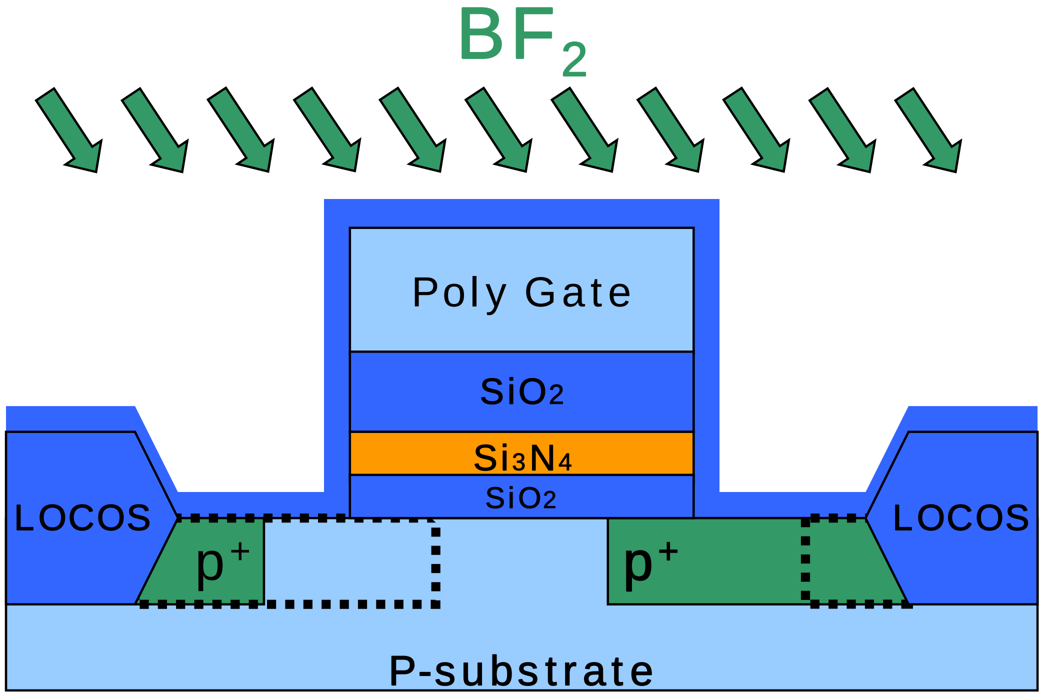


Fig. 2-1 (h)

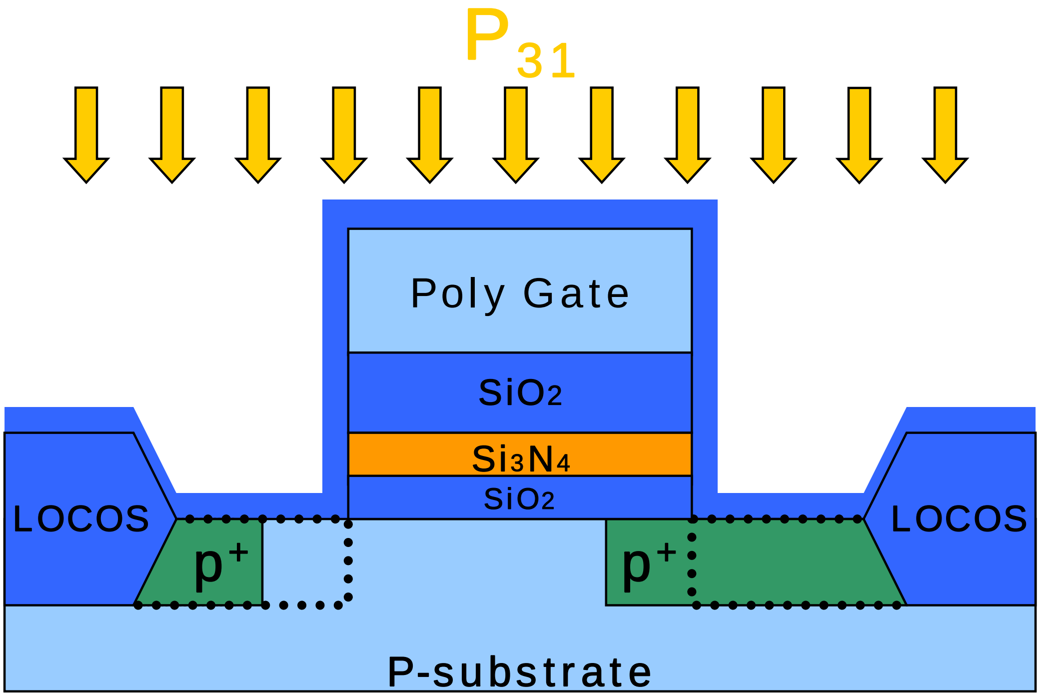


Fig. 2-1 (i)

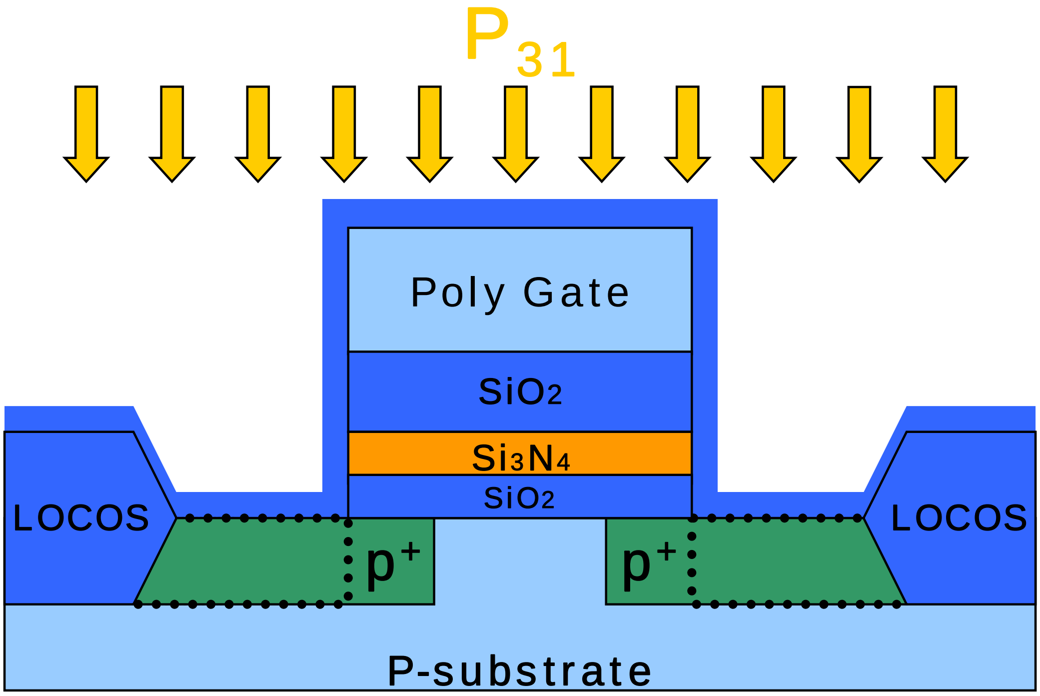


Fig. 2-1 (j)

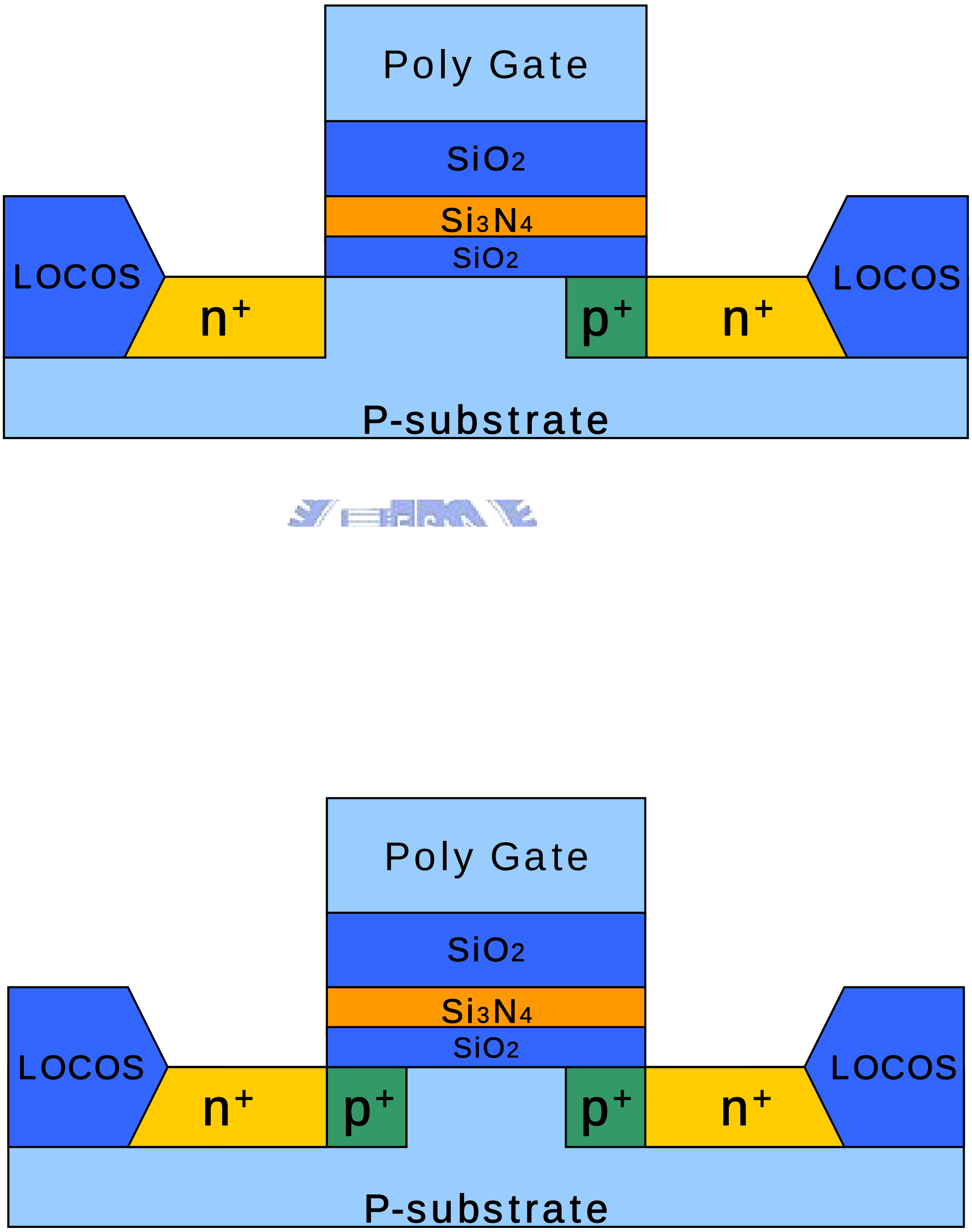

Poly Gate
SiO2
Si3N4
SiO2
LOCOS
n+
p+
n+
LOCOS
P-substrate
Poly Gate
SiO2
Si3N4
SiO2
LOCOS
n+
p+
p+
n+
LOCOS
P-substrate

Fig. 2-1 (k)

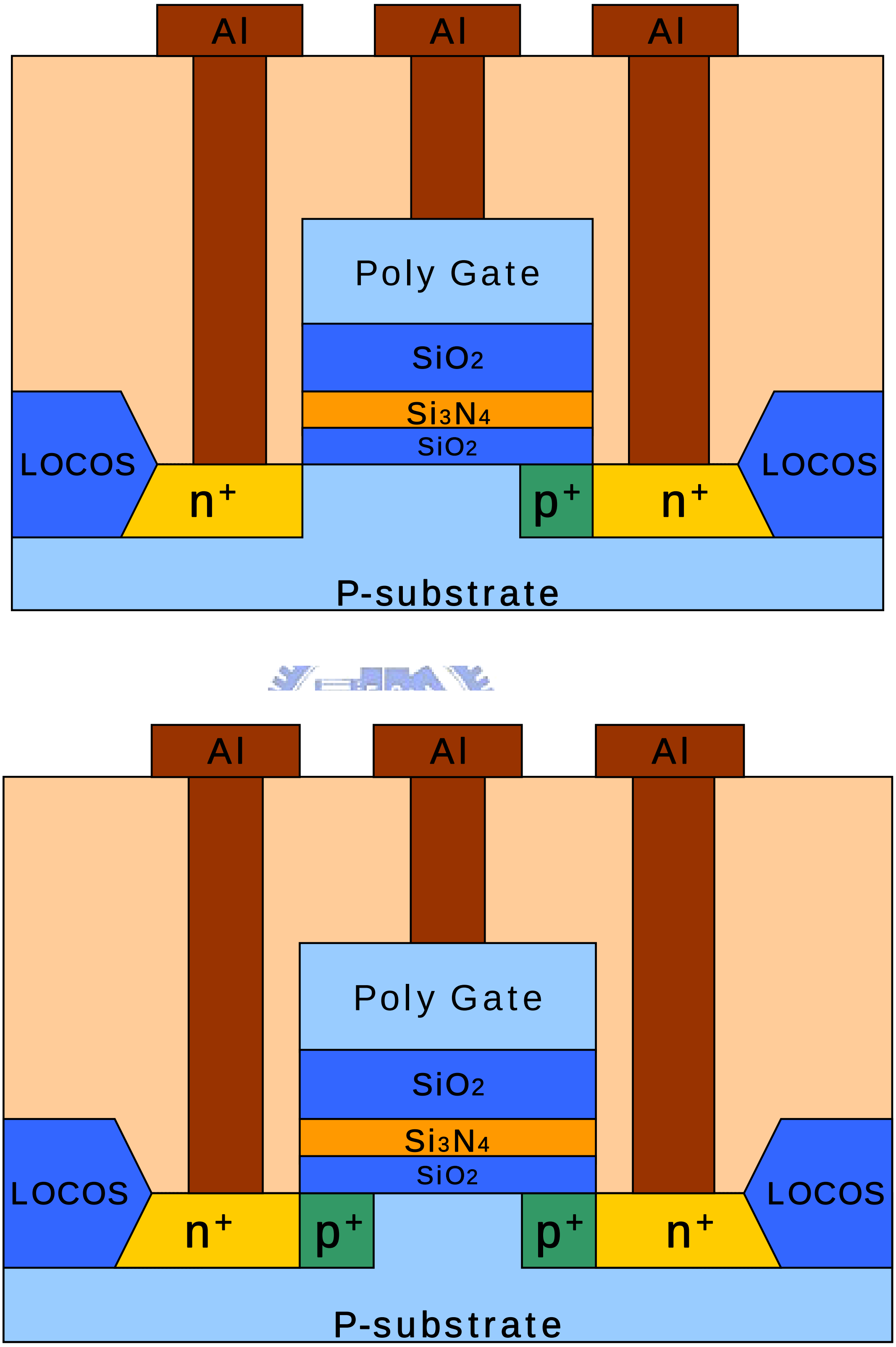


Fig. 2-1 (l)

Fig. 2-1 Process flow of the Zener junction SONOS memory

Tilt Implantation			
Number	**Source**	**Does (cm^{-2})**	**Note**
NMOS-S5E13	**BF$_2$**	**5E13**	**single side tilt implantation**
NMOS-S1E14	**BF$_2$**	**1E14**	
NMOS-S5E14	**BF$_2$**	**5E14**	
NMOS-D5E13	**BF$_2$**	**5E13**	**double sides tilt implantation**
NMOS-D1E14	**BF$_2$**	**1E14**	
NMOS-Con.	**Substrate : 1E12~5E12**		**None**

Source/Drain Implantation		
Number	**Source**	**Does (cm^{-2})**
NMOS-S5E13	**P$_{31}$**	**5E15**
NMOS-S1E14	**P$_{31}$**	**5E15**
NMOS-S5E14	**P$_{31}$**	**5E15**
NMOS-D5E13	**P$_{31}$**	**5E15**
NMOS-D1E14	**P$_{31}$**	**5E15**
NMOS-Con.	**P$_{31}$**	**5E15**

Table 2-1 Split Table of Implantation

2.3 Result and Discussion

In this section, the electrical characteristics of n-channel SONOS flash memory were discussed.

2.3.1 Id-Vg Curve

Figure 2-2 shows the Id-Vg curve of the conventional devices under programming and erasing operations and figure 2-3 shows the Zener devices. The constant current method was used to define the Vth (Id = 1nA). The program condition is Vg = 10V, Vd = 8V with 1ms stress. The erase condition is Vg = -10V, Vd = 8V with 1ms stress both in the conventional devices and in the Zener devices. The program condition is Vg = 10V, Vd = 8V with 1ms stress in both devices. The memory window in the conventional devices is about 2.6V, and it’s about 3.1V in the Zener devices. We use channel hot electron injection (CHE) as programming method and band to band hot hole (BBHH) as erasing method. Figure 2-4 shows the plot of CHE programming mechanism and figure 2-5 show the plot of BBHH erasing mechanism. We think the Vth Shift rightward is due to electron trapping in the trapping layer. Because that as we apply voltage on memory devices, the energy band will bend. And then electron trapping occurred. During program, the electrons in the substrate gain energy from applied Vg and Vd. If the energy is enough to overcome the energy barrier of tunneling oxide layer, the hot electrons will inject into the nitride trapping and be trapped. This phenomenon cause Vth shift. As erasing, a negative Vg and positive Vd were applied to generate hot holes in the substrate. If the hot hole gets enough energy to overcome the tunneling oxide energy barrier, it will arrive at trapping layer and then combine with electron in the nitride trapping layer. Then the Id-Vg curve shifts leftward.

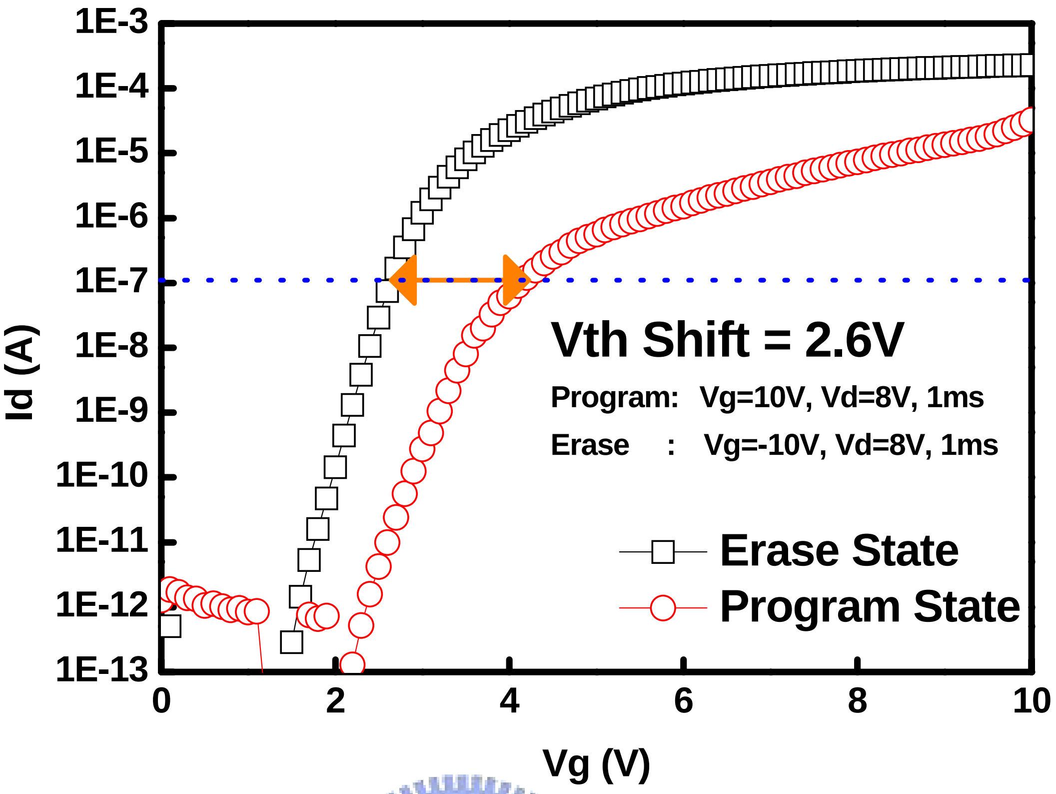


Fig. 2-2 Id-Vg curve of the conventional devices

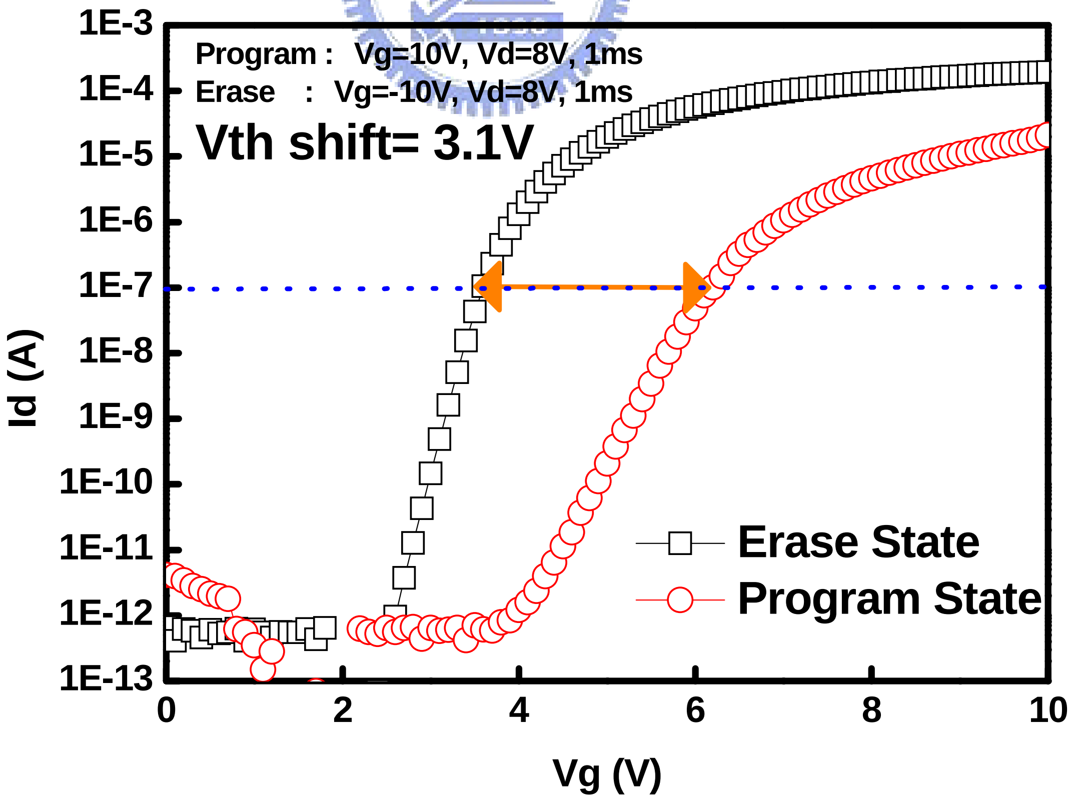


Fig. 2-3 Id-Vg curve of the Zener devices

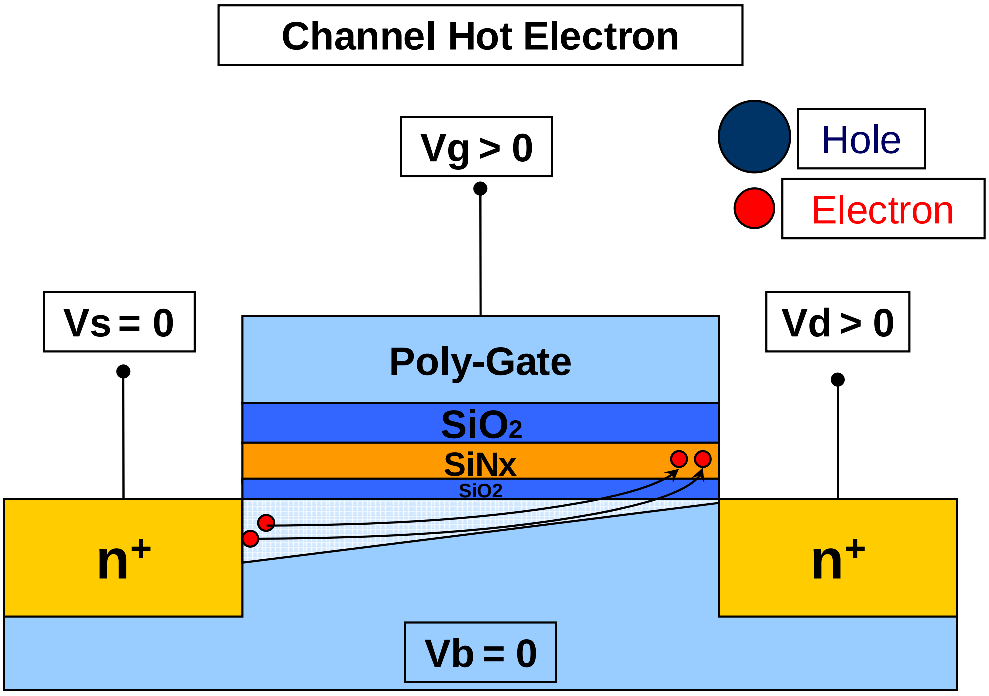


Fig. 2-4 Channel hot electron injection (CHE) programming mechanism

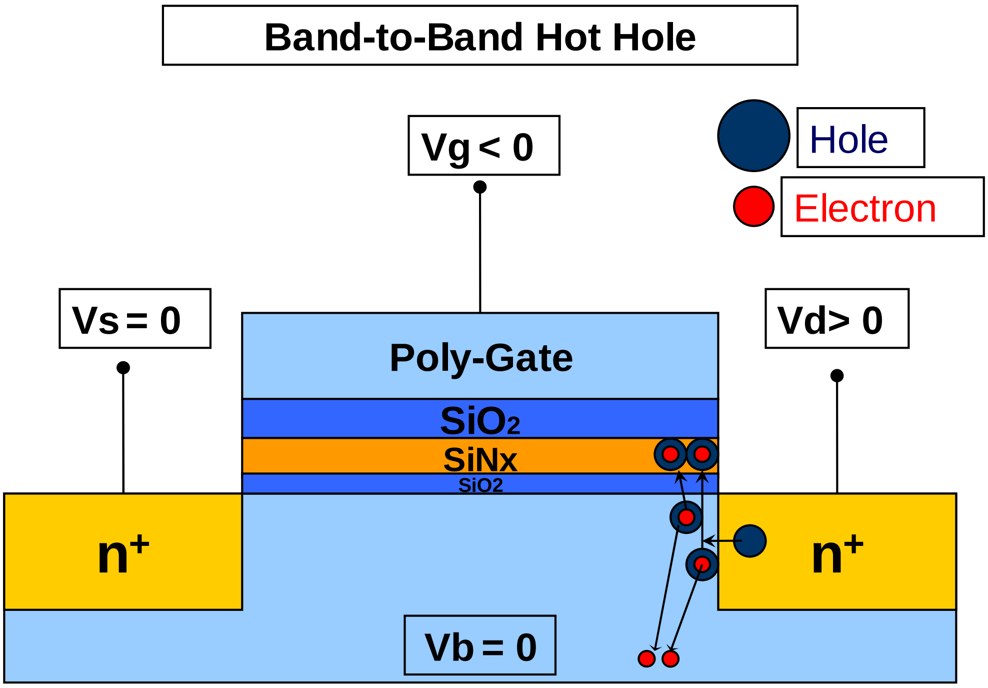


Fig. 2-5 Band to band hot hole (BBHH) erasing mechanism

2.3.2 Program and Erase Speed

Figure 2-6 shows the programming speed of the single side Zener devices and the conventional devices. Fig. 2-7 shows the programming speed of the double side Zener devices and the conventional devices It show that the Zener devices is faster than the convention devices. The programming speed of Zener devices increases as the concentration of p+ region increasing. First, Figure 2-8 shows the tunneling oxide band diagram as programming state. First, because the electric field in p+/n+ junction is higher than in p/n+ junction, channel hot electron can get higher energy to overcome the tunneling oxide barrier. Second, when the p+ channel is in programming operation, the Zener devices will have more tunneling oxide bend banding than the conventional devices. Hence the electron injection efficiency in the Zener devices is higher than the conventional devices. From these two points, the programming speed can be improved with the Zener junction. And we can see the comparison between the single side Zener devices and the double sides Zener devices in figure 2-9. Because the double sides Zener has higher potential voltage (Vbi) at the source side junction as figure 2-10, it will decrease more electron energy of lateral direction.

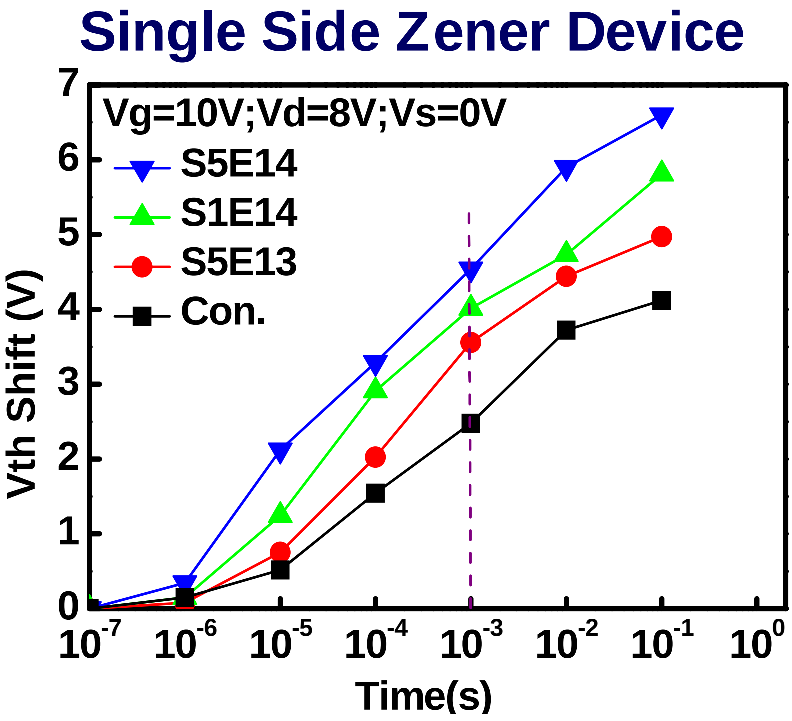


Fig. 2-6 Programming speed of the single side Zener devices and the conventional devices

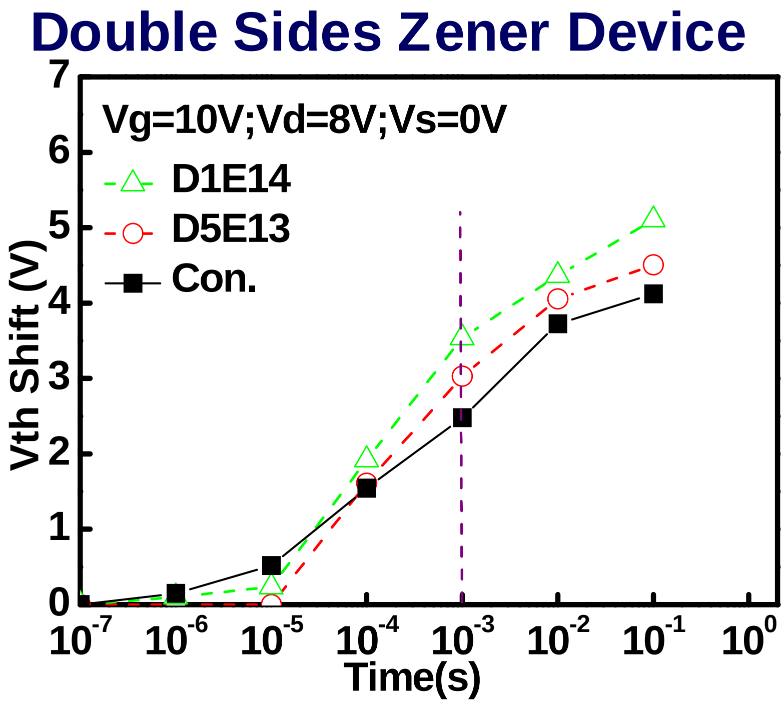
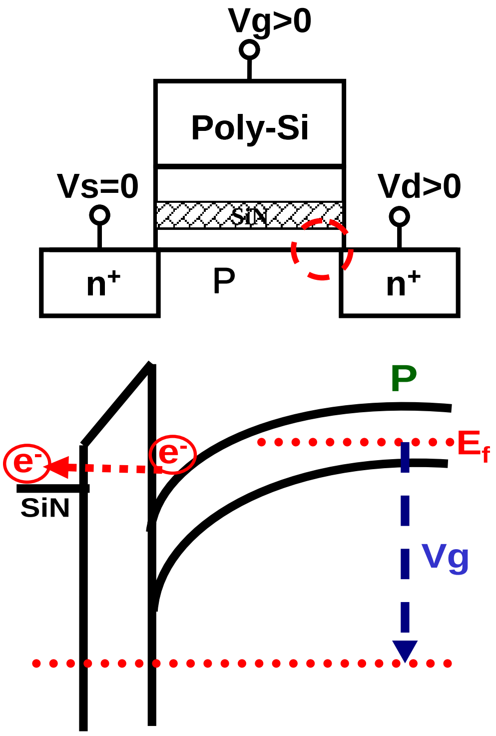
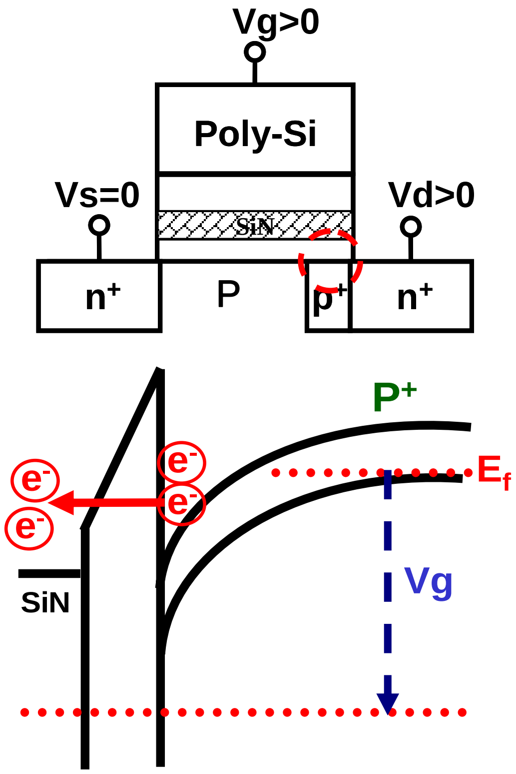


Fig. 2-7 The programming speed of the double side Zener devices and the conventional devices

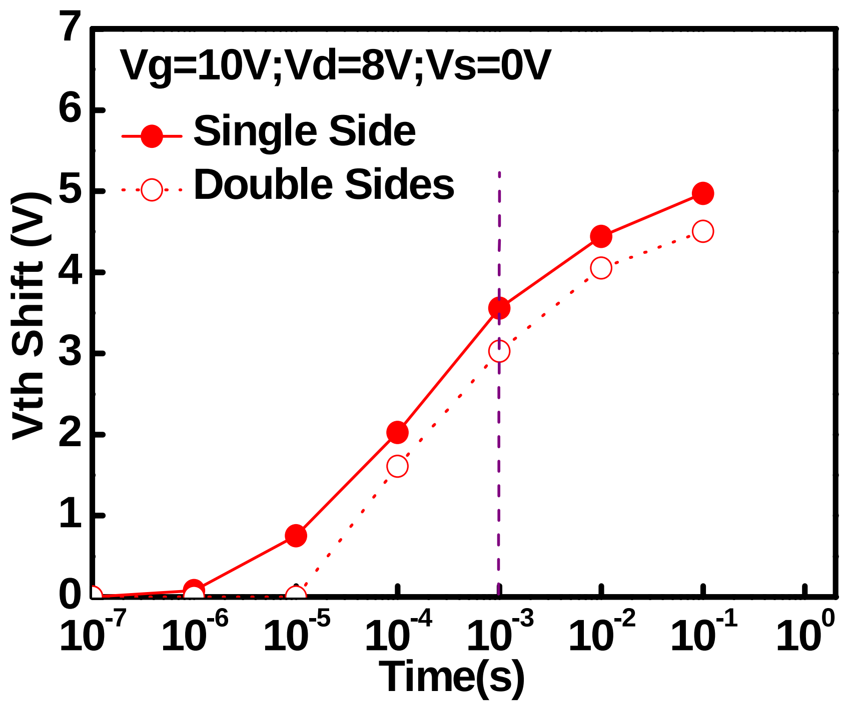


(a) The conventional devices

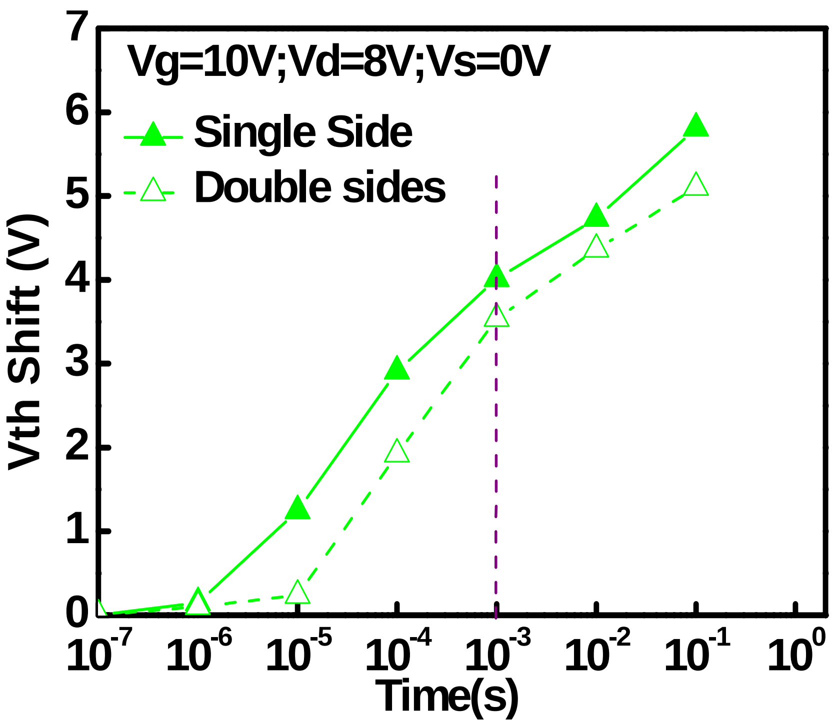


(b) The Zener devices

Figure 2-8 Tunneling oxide band diagram at programming state



(a) Does = 5E13 cm^{-2}



(b) Does =1E14 cm^{-2}

Fig. 2-9 Programming speed comparison of the single side Zener devices and the double sides Zener devices

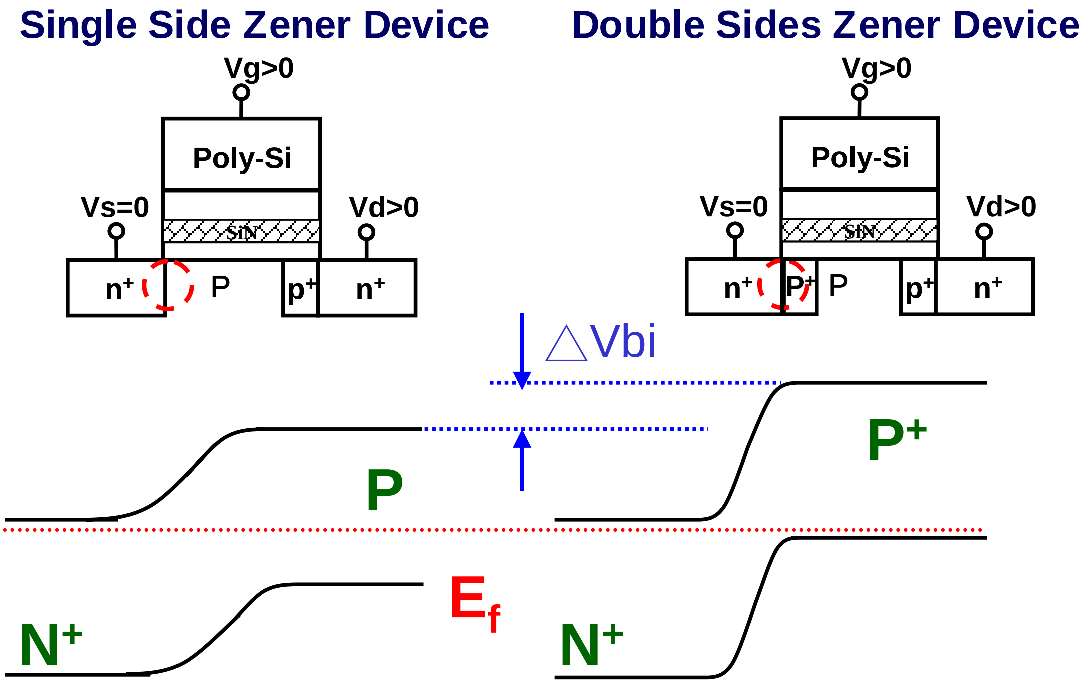


Figure 2-10 Band diagram comparison between the single side devices and the double sides Zener devices at Source side

Figure 2-11 and figure 2-12 show the erasing speed in which the Zener devices is faster than the convention devices. The erasing speed of the Zener devices increased as the concentration of p+ region increasing. Figure 2-14 is the erasing state junction band diagram plot in our devices. When a positive voltage apply to gate node and negative bias to drain node, the n+/p+ junction were biased at reversed condition. The Zener devices shows the larger energy band bending, and it induces more hot holes direct band to band tunneling into the channel. So, the Zener devices have better erasing characteristics than the conventional devices. Figure 2-13 displays that in the same does condition the erasing speed of the single side Zener devices and the double sides Zener devices are similar.

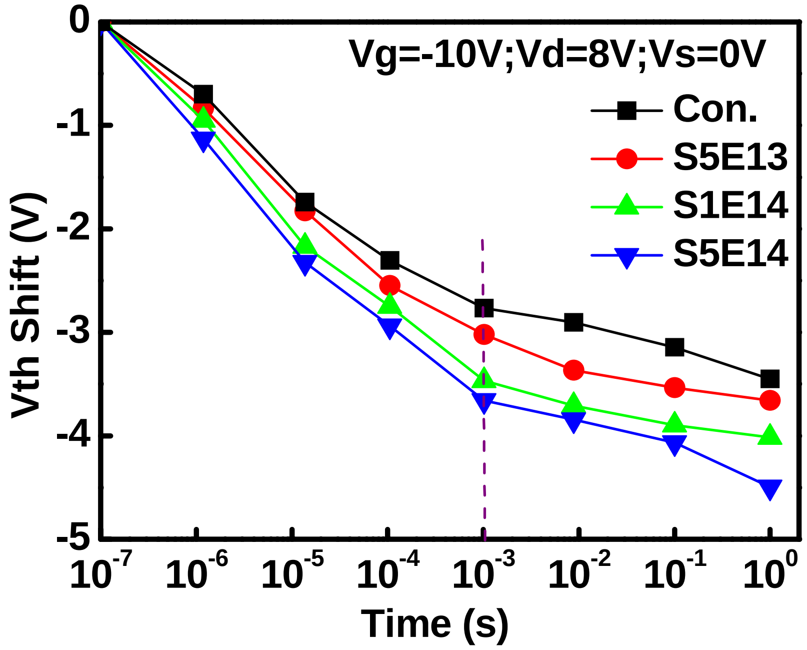


Figure 2-11 Erasing speed of the single side Zener devices and the convention devices

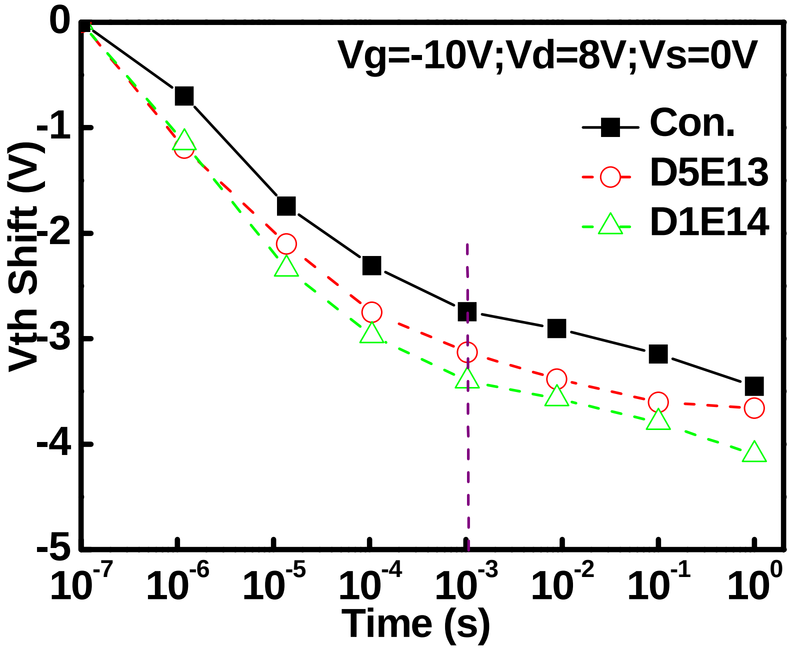
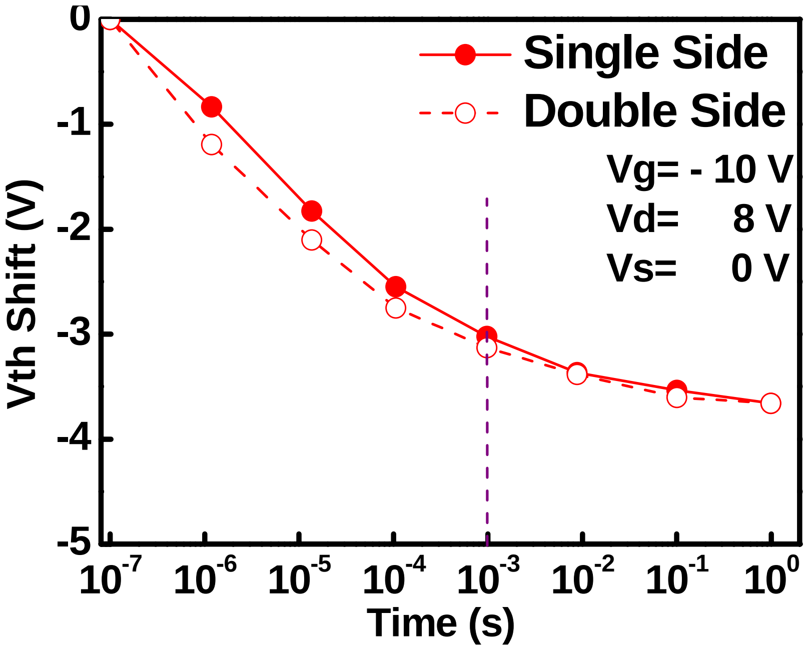
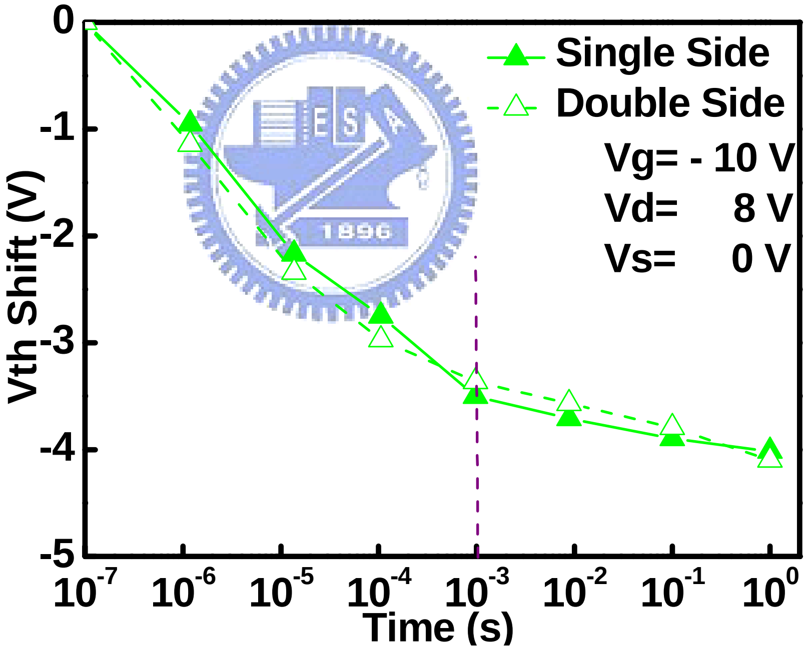


Figure 2-12 Erasing speed of the double sides Zener devices and the convention devices

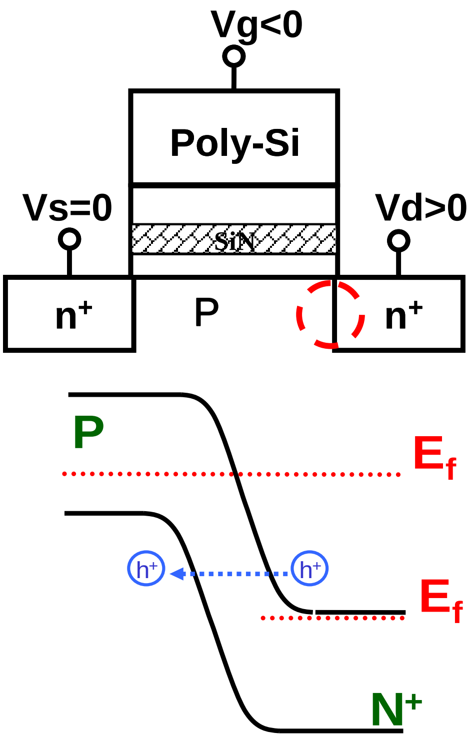


(a) Does = 5E13 cm^{-2}

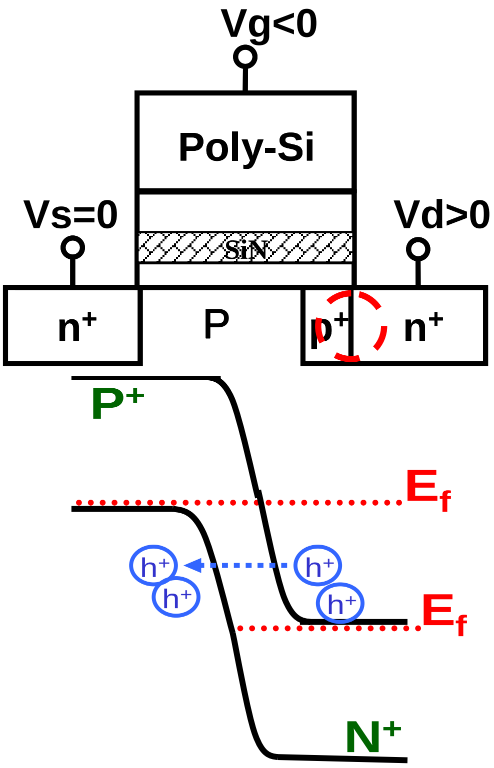


(b) Does = 1E14 cm^{-2}

Fig. 2-13 Erasing speed of the single side Zener devices and the double sides Zener devices



(a) The conventional devices



(b) The Zener devices

Fig. 2-14 Junction band diagram at erasing state

2.3.3 Data Retention Characteristic

Figure 2-15 is the data retention characteristic of the single side Zener devices and the conventional devices measured at room temperature, and figure 2-16 is retention compared between the double sides Zener devices and the conventional devices. We find the charge loss after 1E4 seconds of the double sides Zener junction memory devices shows little difference with the conventional devices. But the single side Zener junction memory devices has much more charge loss comparing to the conventional devices as the does of halo implantation increasing. The curve shows 10% ~ 20% charge loss as measure time up to 1E4 seconds at room temperature. Because the larger lateral electrical field in the single side Zener devices, it caused the gate control ability lowing. And the partial charge stored in the trapping layer and the tunneling oxide interface and in the tunneling oxide layer, as figure 2-17, the charge in this region loss easily. But the most of the stored charge is in the trapping layer in the double sides devices, because of the better gate control ability, as figure 2-18. Hence, the double sides Zener devices have better data retention compared with the single side Zener devices.

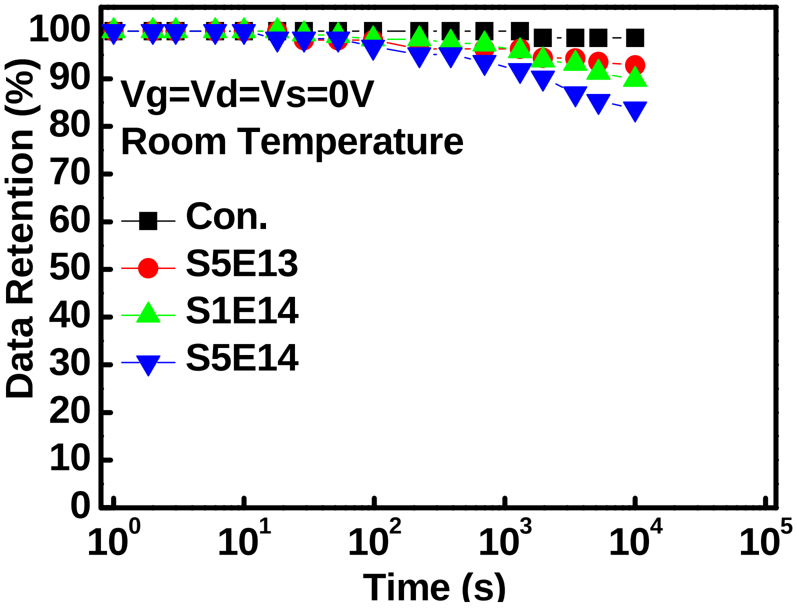


Fig. 2-15 Data retention characteristic of the single side Zener devices and the conventional devices

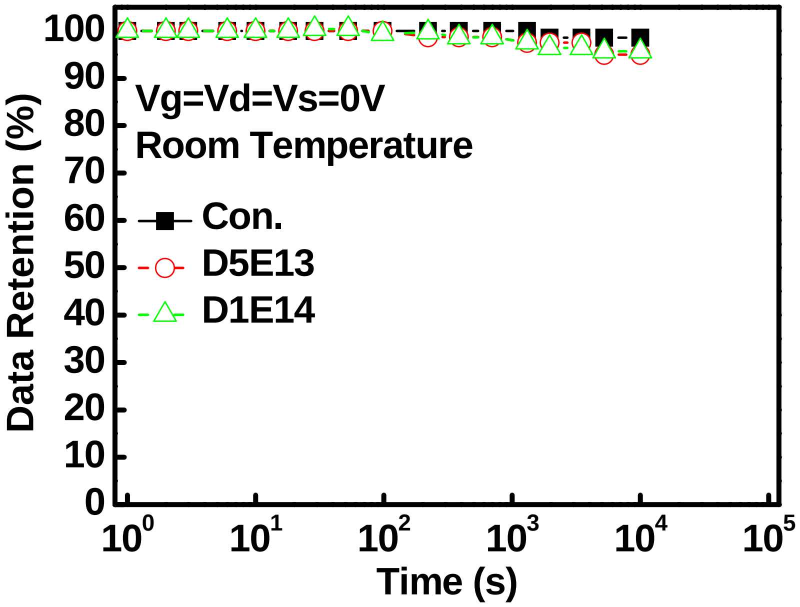


Fig. 2-16 is retention compared between the double sides Zener devices and the conventional devices.

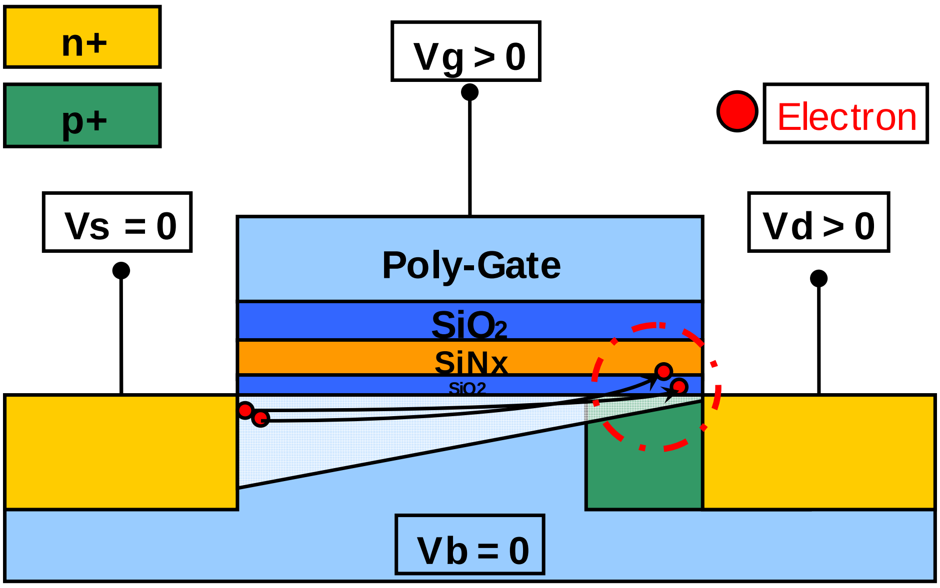


Fig. 2-17 Charge stored location in the single side Zener devices

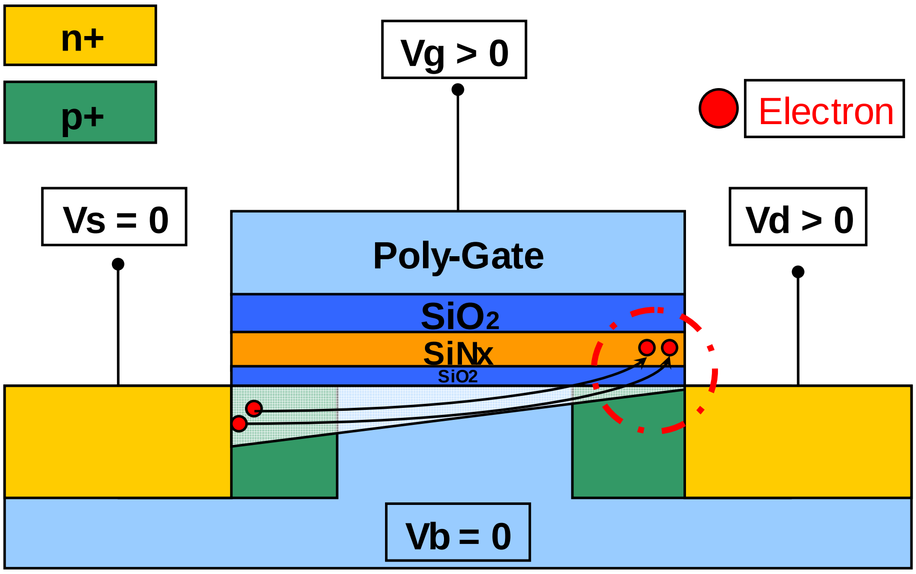


Fig. 2-18 Charge stored location in the double sides Zener devices

2.3.4 Drain Disturbance Measurement

When we operate the memory devices at either programming state or erasing state, we always apply a positive drain voltage to the bit line. Hence, the drain voltage does not only be applied to the cell we want to operate but also to the other devices cell, figure 2-19. And then the voltage maybe enhances the charge loss in the trapping layer, and this is called drain disturbance. Figure 2-20, 2-21, 2-22, and 2-23 show drain disturbance measurement of the Zener devices and the conventional devices. We applied two drain bias conditions, Vd = 8V and 10V with Vg = Vs = Vb = 0V to the all devices. From figure 2-21 and 2-23, we find that the drain disturbance is more serious in the single side Zener devices than the conventional devices. But it is still acceptable to the double sides Zener devices. The reason is that the p+/n+ junction has higher electric field with positive Vd applied than the p/n+ junction. And the charge stored location in the single side Zener devices is in the tunneling oxide or the interface of the trapping layer and the tunneling oxide layer, the charge losses in the region more easily than in the trapping layer.

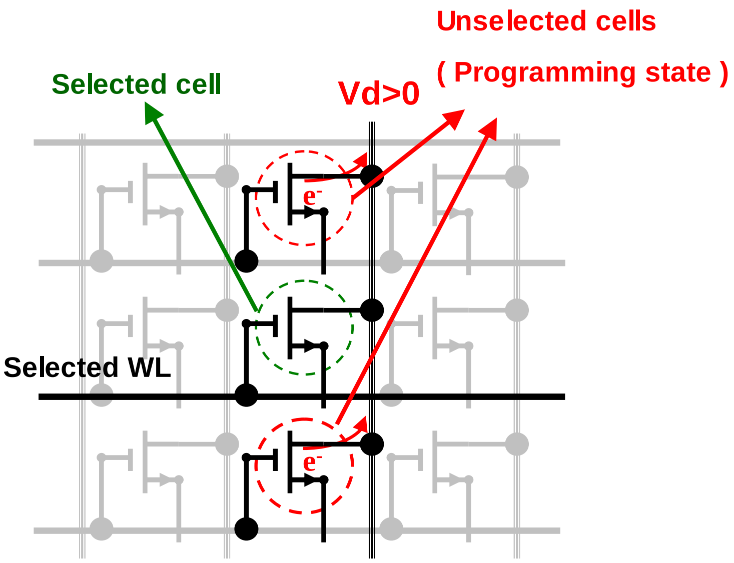


Fig. 2-19 Drain disturbance in the memory devices

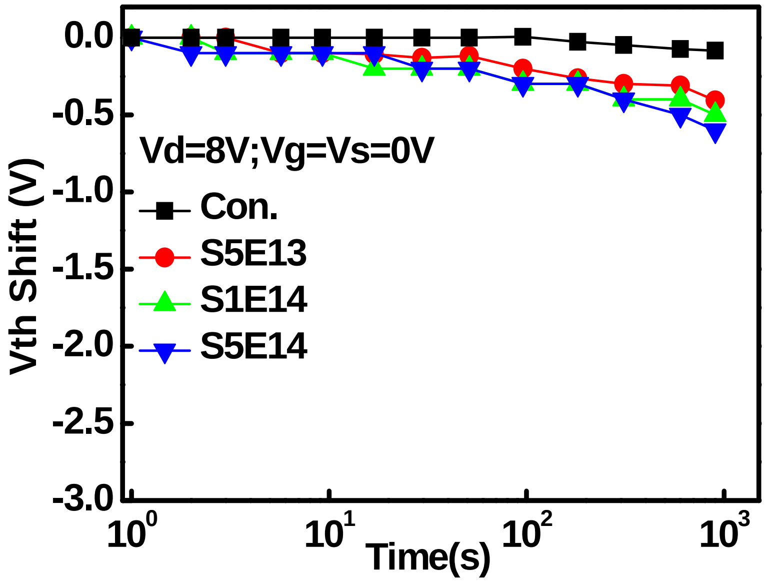


Fig. 2-20 Drain disturbance between the single side Zener devices and the conventional devices at Vd = 8V

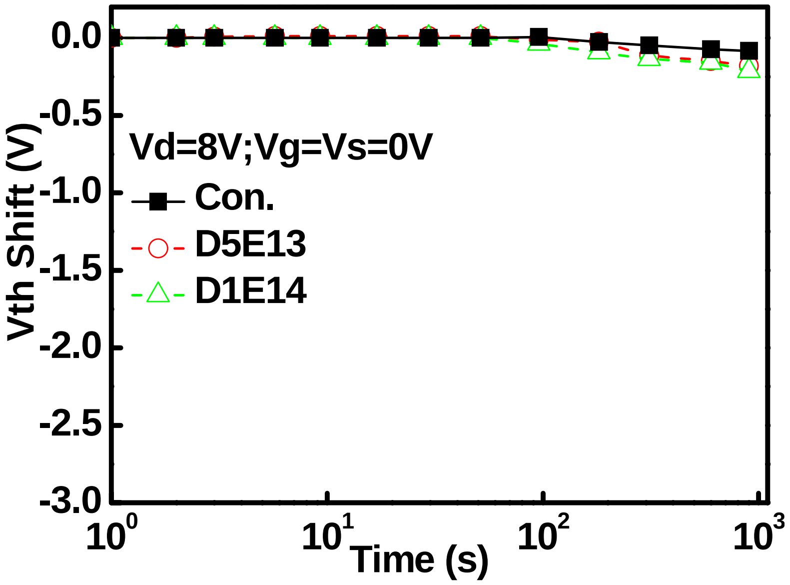


Fig. 2-21 Drain disturbance between the double sides Zener devices and the conventional devices at Vd = 8V

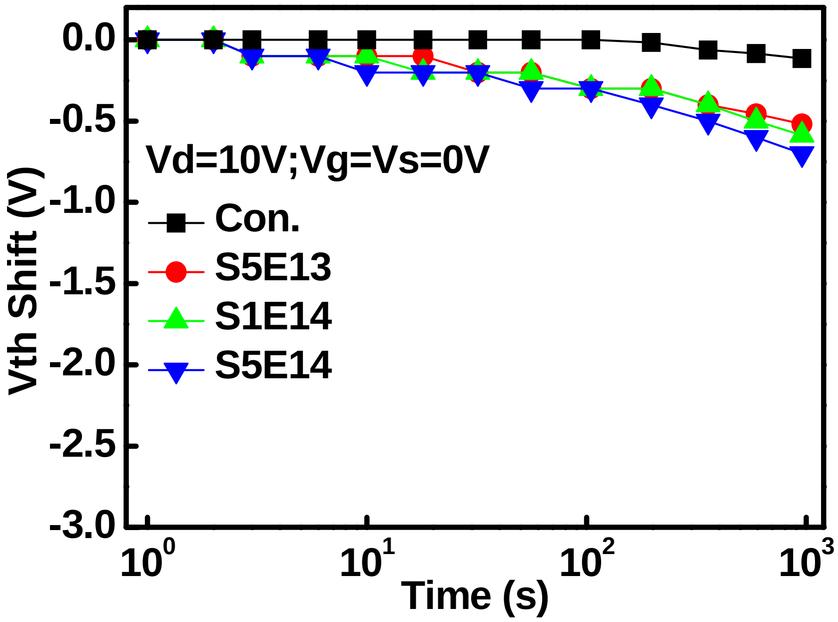


Fig. 2-22 Drain disturbance between the single side Zener devices and the conventional devices at Vd = 10V

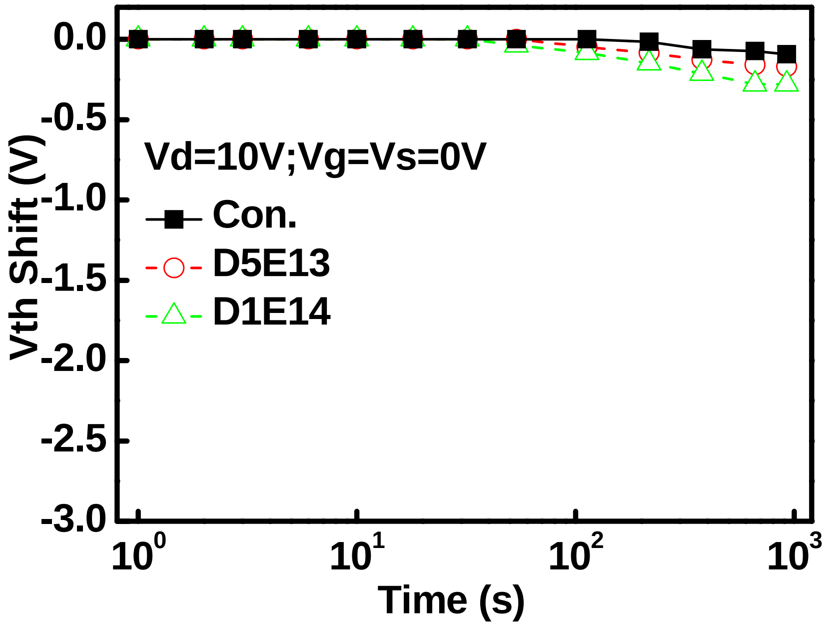


Fig. 2-23 Drain disturbance between the double sides Zener devices and the conventional devices at Vd = 10V

2.3.5 Endurance Characteristic

Figure 2-24, 2-25, and 2-26 display the endurance characteristic of the conventional devices, the single side Zener devices, and the double sides Zener devices. We find that the endurance in the conventional is the worst case and the Zener shows the better endurance characteristic. First, because the higher operation speed can reduce the stress time and reduce the nitride quality degradation. Second, due to the difference between the programming and erasing mechanism, the locations of charge stored are not wholly the same. Then the stored electron by CHE programming mechanism can not be combined with hole injection by BBHH erasing mechanism. In the Znener devices, the locations of charge injection between programming and erasing are more closely, due to the higher electric field region could make the charge more convergent.

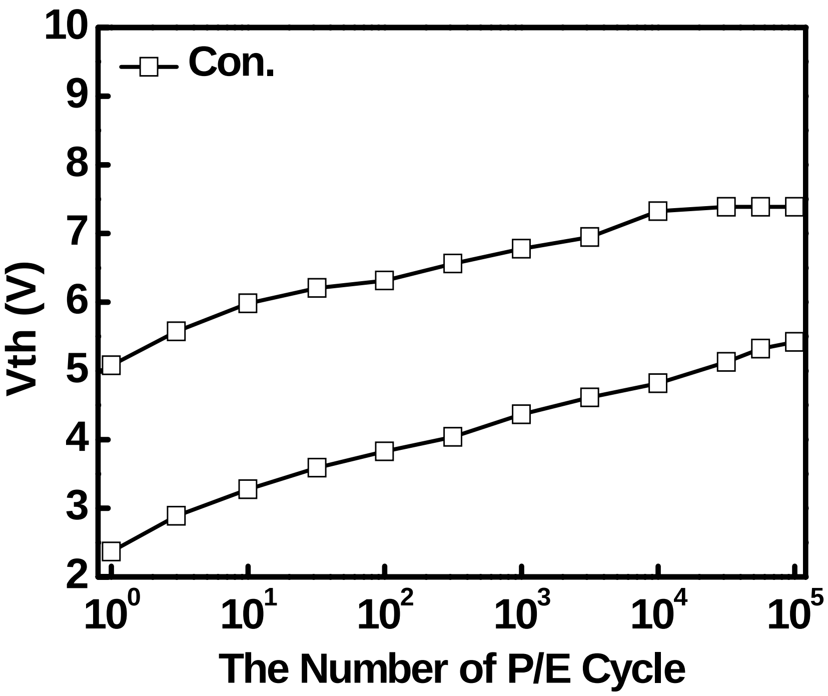


Fig. 2-24 Endurance characteristic of the conventional devices

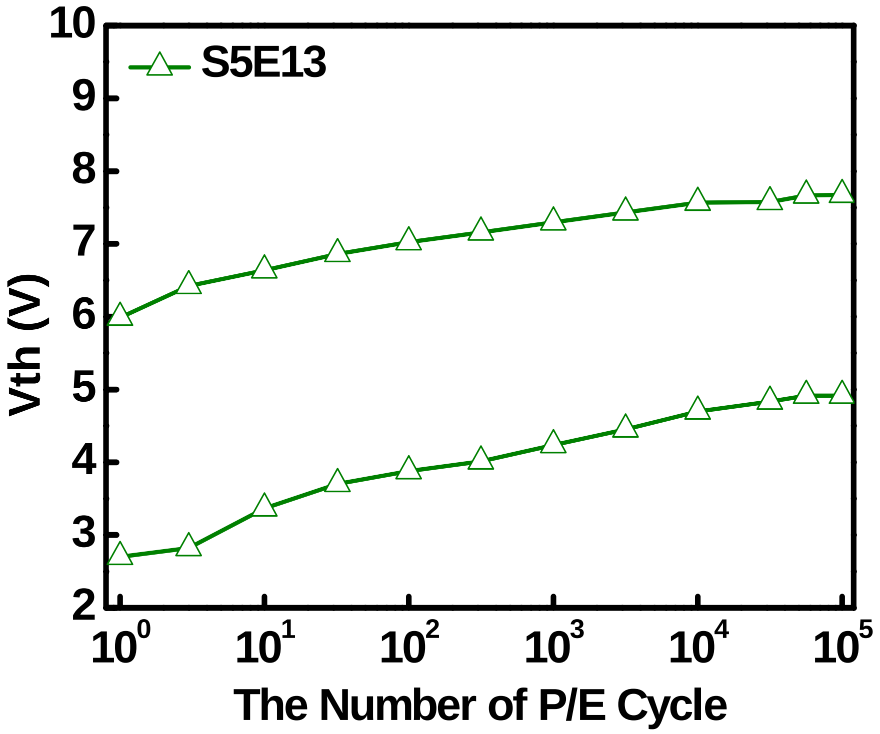


Fig. 2-25 Endurance characteristic of the single side Zener devices

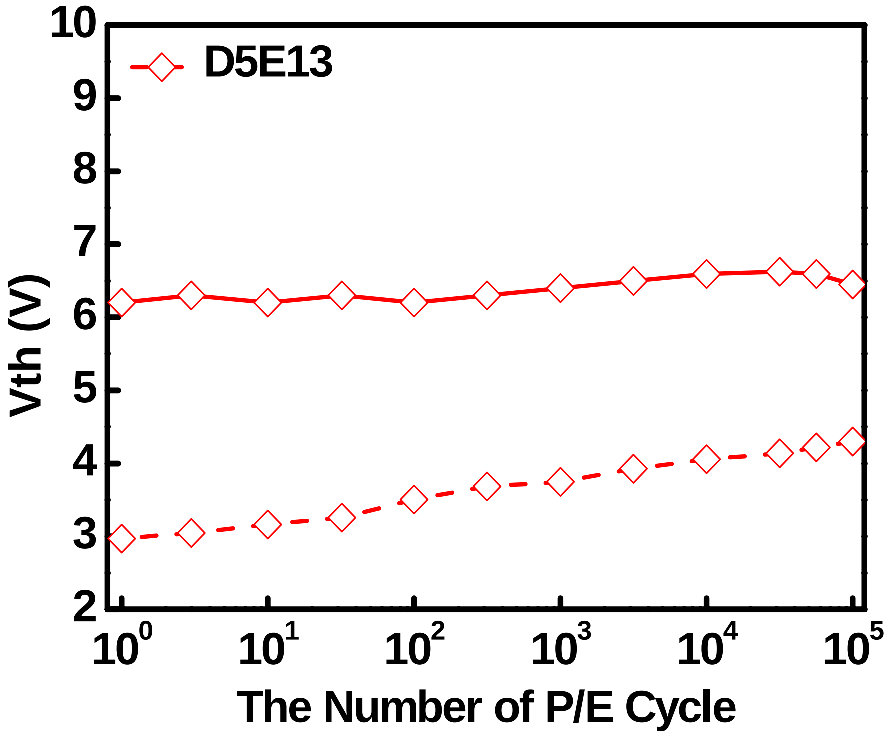


Fig. 2-26 Endurance characteristic of the double sides Zener devices

2.4 Summary

The impacts of tilt implantation on programming and erasing performance are beneficial for the SONOS devices. We can make injection efficiency higher during CHE programming and BBHH erasing to get better programming and erasing speed with the higher electrical field. Although the Zener devices shows degradation in the data retention and drain disturbance, but it is still acceptable in the SONOS memory. Because we decrease the programming and erasing stress time at the same bias condition, the endurance characteristics in both single side Zener devices and double sides Zener devices are better than the conventional devices. So we think that the Zener devices surely could improve the SONOS memory characteristics.

2-5 Reference

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CHAPTER 3

Characteristics of P-Channel SONOS Memory with Zener Junction

3.1 Introduction

Due to its low voltage, low power and high speed programming features, p-channel flash memories [1]-[2] have been evolved as a promising cell for real applications in the future. In a certain design of p-channel flash cells, programming of the cell can be achieved either by band-to-band tunneling induced hot electron injection (BBHHIHE)at the drain side or by channel hot hole impact ionization induced channel hot electron injection (CHHIHE). Erasing of the cell can be accomplished by electron channel Fowler-Nordheim(F-N) ejection from the floating gate. Here, both Programming schemes, CHHIHE and BBHHIHE, will generate the so-call oxide damages, which include the interface state and the oxide trap charge [3]. The interface traps density generated under these kinds of Fowler-Nordheim (F-N) stress and Substrate-hot-hole stress. The injection of impact ionization generated hot holes is found to be the most important reason for interface trap generation under $V_G<0$ F-N stress at high oxide field. The generated interface-trap density under Substrate hot hole stress increases with increasing gate oxide field. It is also found that the Substrate hot hole stress induces more interface traps than Substrate hot electron stress.

Instead of using N-channel cells, P-channel cells[5]-[13], known for the high injection efficiency and low programming drain current, are quite suitable for low-voltage and low-power applications. The developing trend of Flash memory has gone in the way of multi-level storages. The most important issue is to precisely control a tight threshold voltage distribution at different levels. To achieve tight threshold voltage distribution in multi-level Flash memory, the bit-by-bit verification which slows down the programming speed can be performed. The multi-level applications of P-channel Flash memory was first proposed in [14-19].

In this work, we purpose a high operation speed SONOS memory with using reverse halo implant in the channel near by Source / Drain sides to improve the programming / erasing speed. Figure 3-1, 3-2 and 3-3 display the programming mechanism and the erasing mechanism of p-channel SONOS memory respectively. Because the erasing mechanism in the p-channel memory is F-N tunneling, the erasing speed is not fast enough. We make a little change in the erasing mechanism here. Because the charge stored locations by CHHIHE and BBHHIHE are near the drain edge, we focus on this region. Hence we use drain side FN tunneling to be our erasing mechanism, and this way also can be improved by higher field. Then the problem of the injection efficiency during erasing is improved in the p-channel SONOS memory. Due to the CHHIHE mechanism is slower than BBHHIHE mechanism; we use the BBHHIHE as programming mechanism in our study. Because of the injection locations between BBHHIHE and drain side FN tunneling in p-channel memory are more closely than n-channel memory, we expect that the endurance will be improved.

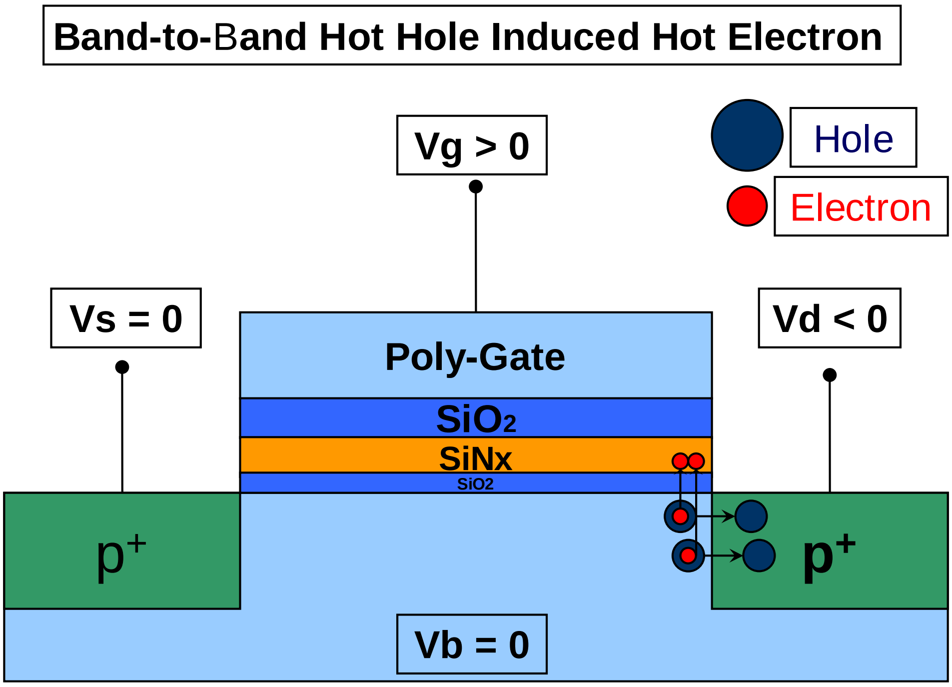


Fig 3-1 Band to band hot hole induced hot electron programming mechanism

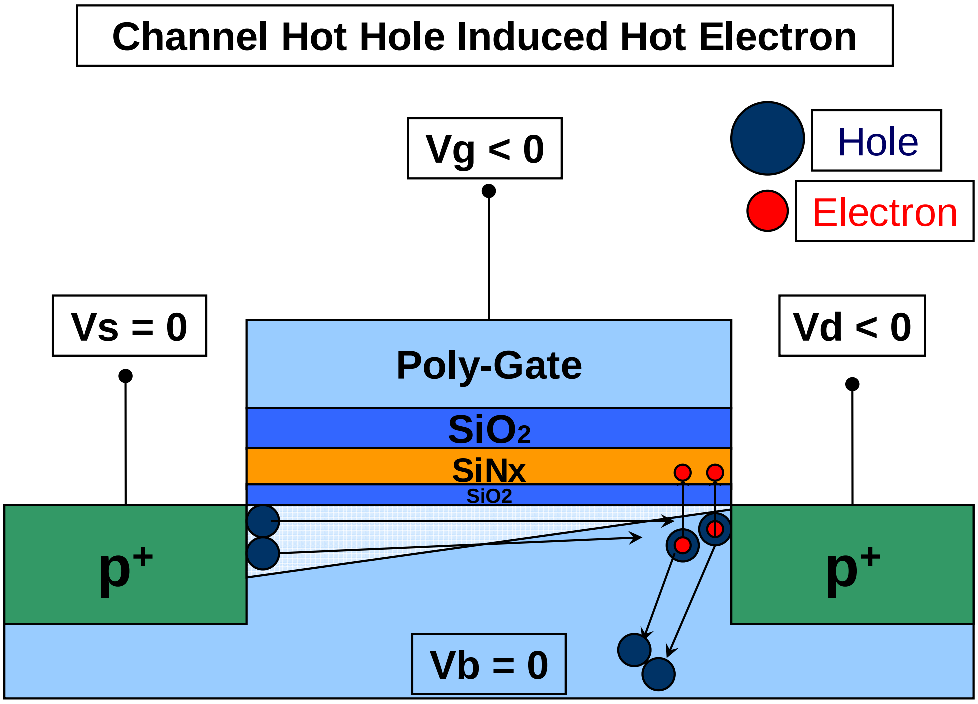


Fig 3-2 Channel hot hole induced hot electron programming mechanism

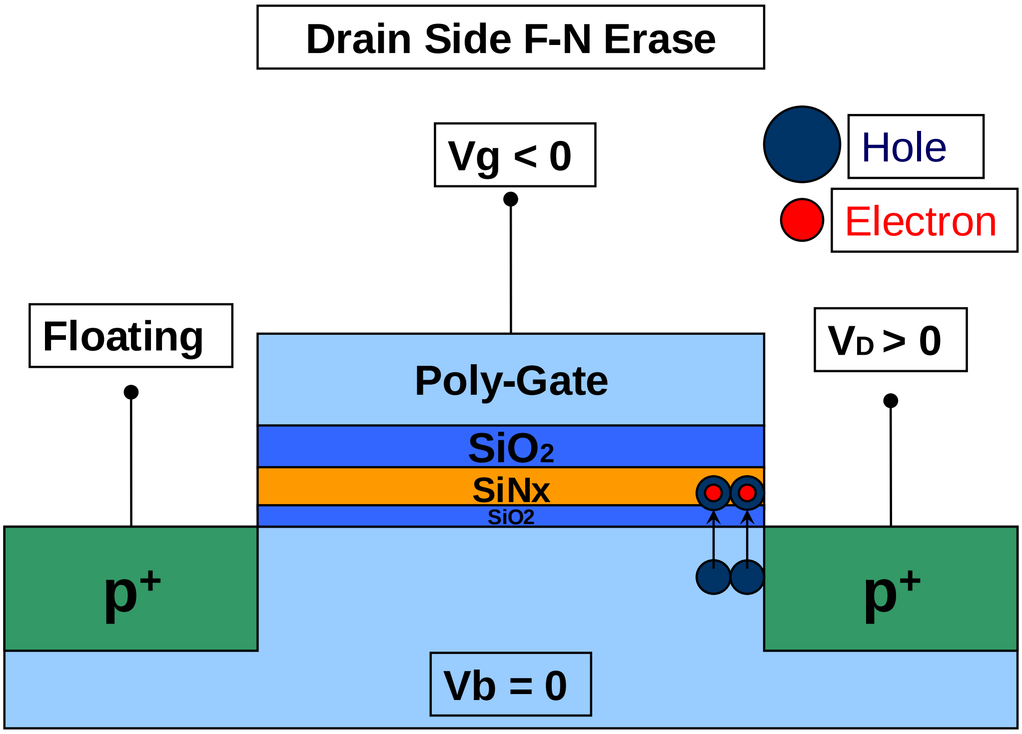


Fig 3-3 Drain side FN erasing mechanism

3.2 Experiment

Figure 3-4 schematically depicts the process flow of the proposed SONOS flash memory with Zener junction. The fabrication process of the Zener junction SONOS flash memory devices involved was started with the LOCOS isolation process on p-type, 5-10ohm-cm, (100) orientation, 150mm silicon substrates. First, the tunneling oxide was thermally grown at 1000℃ with N_2O and O_2 in vertical furnace system. The trapping layer Si_3N_4 was deposited at by low temperature chemical vapor deposition (LPCVD) at 780℃, 350mTorr. Then, we do a re-oxidation process step to slightly oxidize the surface of the nitride layer in order to improve the interface quality between the trapping layer and the blocking oxide (top oxide) layer. The locking oxide (top oxide) layer was deposited by LPCVD at 700℃, 300mTorr. Finally, the poly-gate was deposited by LPCVD at 660℃, 300mTorr. The thickness of poly-gate / oxide (blocking oxide) / nitride / oxide (tunneling oxide) are 200nm / 15nm / 8nm / 3nm respectively. Then, the gate was patterned by the exposure, development, and the etching step. Before the next implant steps, we deposited a oxide layer by LPCVD and then etch the oxide layer by dry etch process to from the sidewall spacer. The sidewall spacer is used to prevent the sidewall of the gate stack from being damaged during the implant process steps. For the n-channel SONOS memory devices, we first accomplished the reverse halo-implantation step using a tilt angle implantation with P_{31} ion to forming the n+ region. The dose and energy of the tilt implantation are shown in Table 3-1. The control device is without the reverse halo implantation. Then, the source/drain p+ region was completed by BF_2 implant without tilt angle. The dose and energy of the BF_2 implant are 5E15cm^{-2} and 50keV. Then, the substrate contact was patterned and the sub-contact was implanted with P_{31} at the does 5E15cm^{-2} and energy 40keV. After these implantation process steps, the dopants were activated at 950℃ for 10 seconds by Rapid Thermal Anneal (RTA) system. Then, the 400nm passivation oxide was deposited by LPCVD. The contact holes were patterned and the Al metal deposition was done by PVD. Finally, we define the contact pad by metal etch.

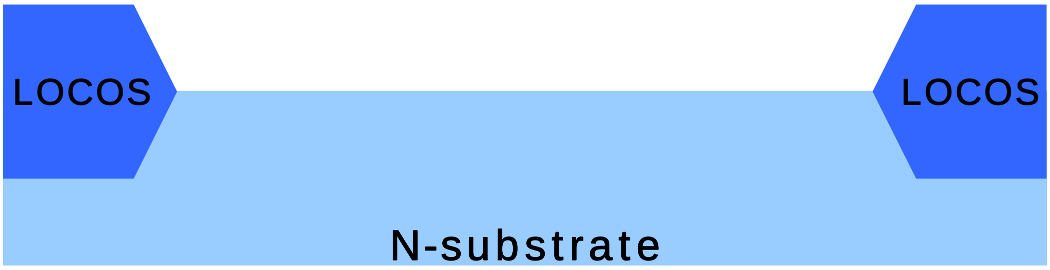


Fig. 3-4 (a)

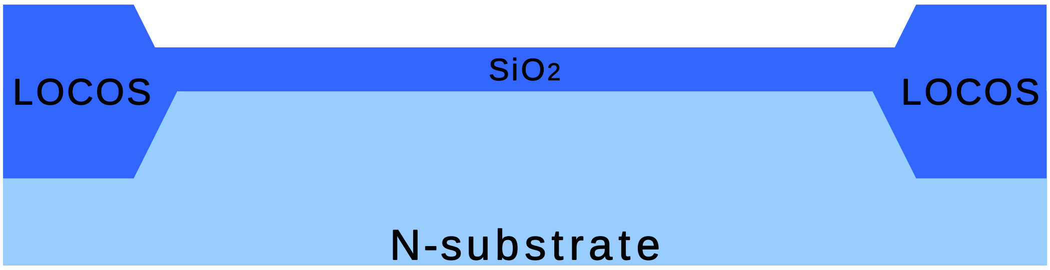


Fig. 3-4 (b)

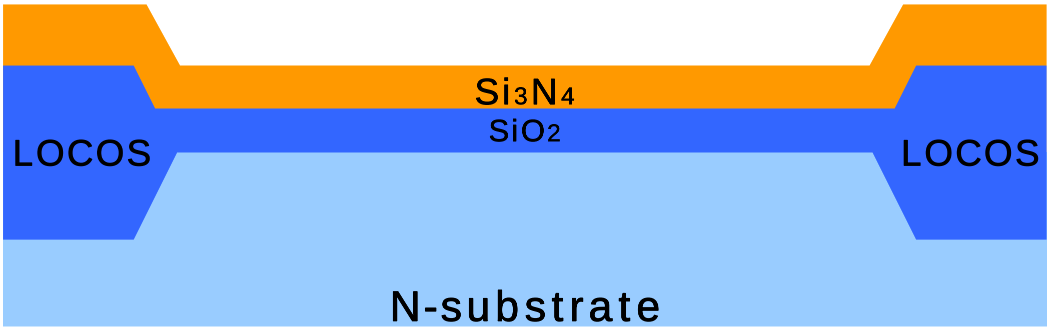


Fig. 3-4 (c)

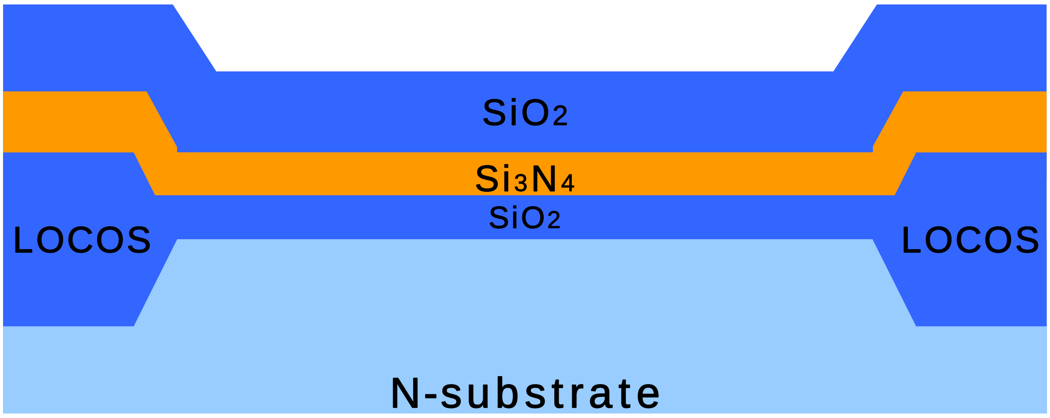


Fig. 3-4 (d)

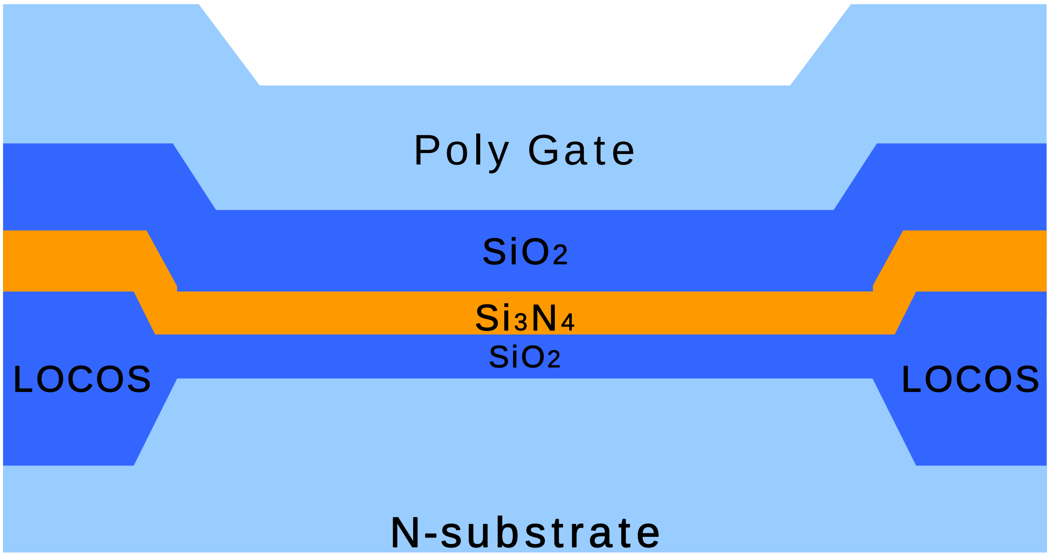


Fig. 3-4 (e)

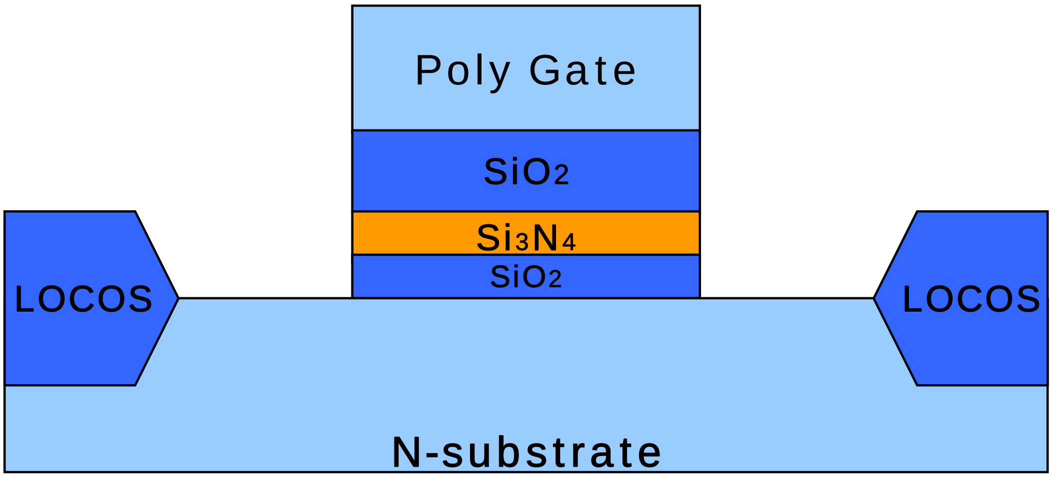


Fig. 3-4 (f)

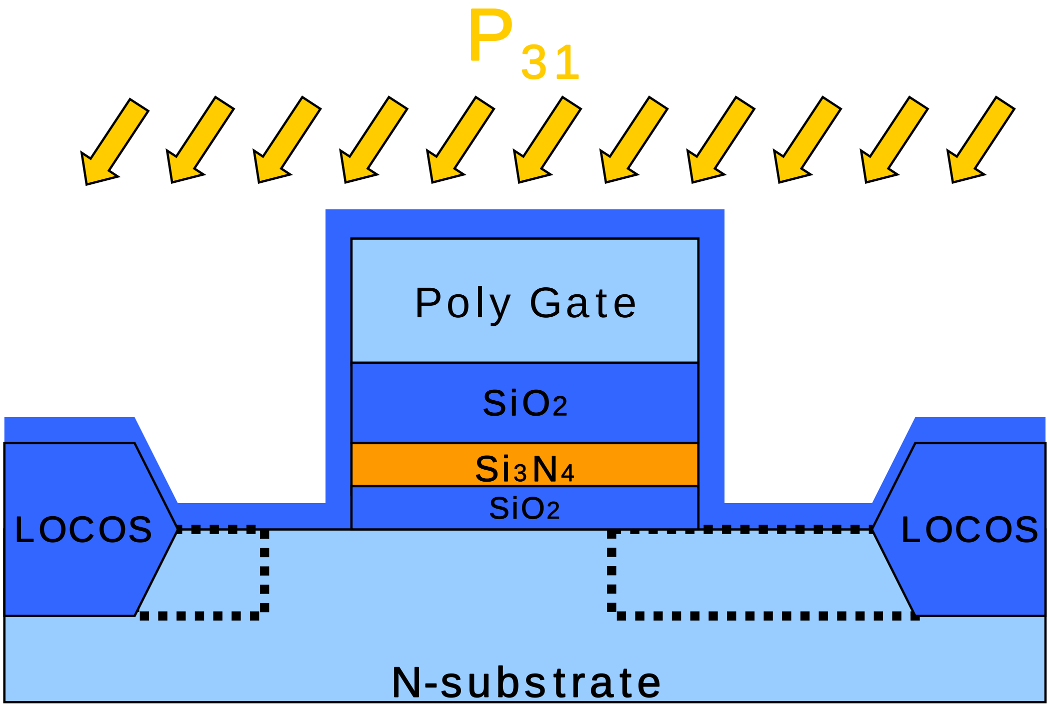


Fig. 3-4 (g)

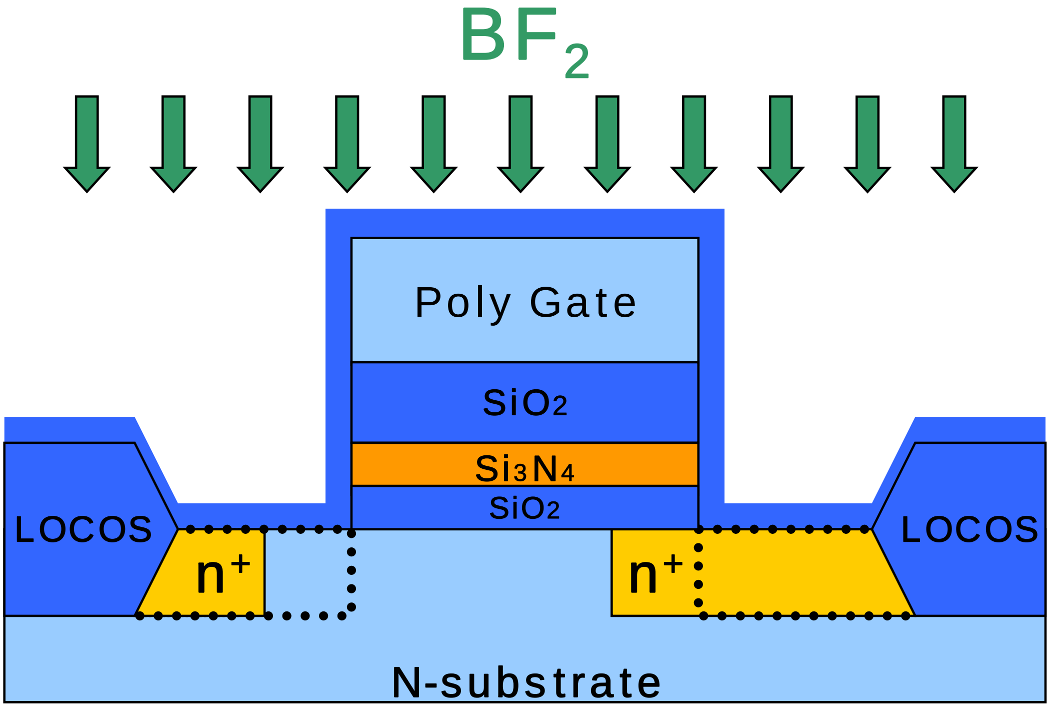


Fig. 3-4 (h)

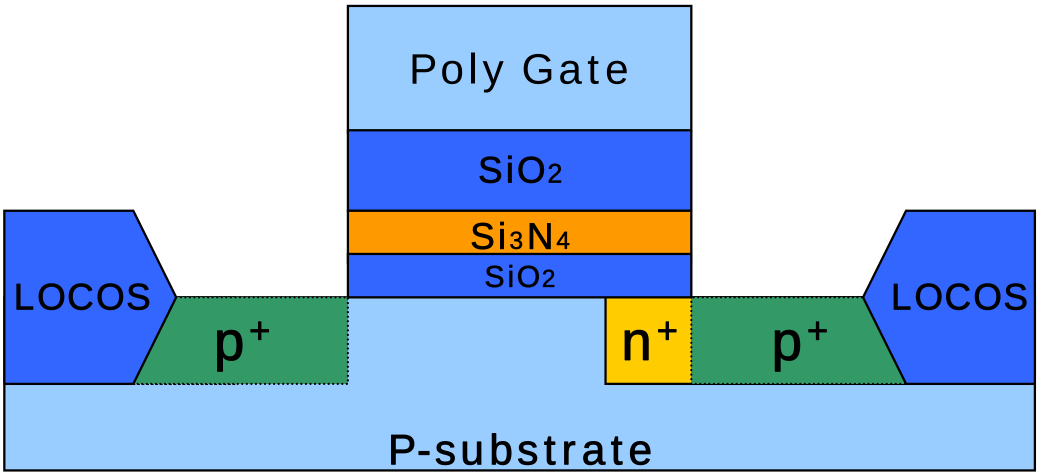


Fig. 3-4 (i)

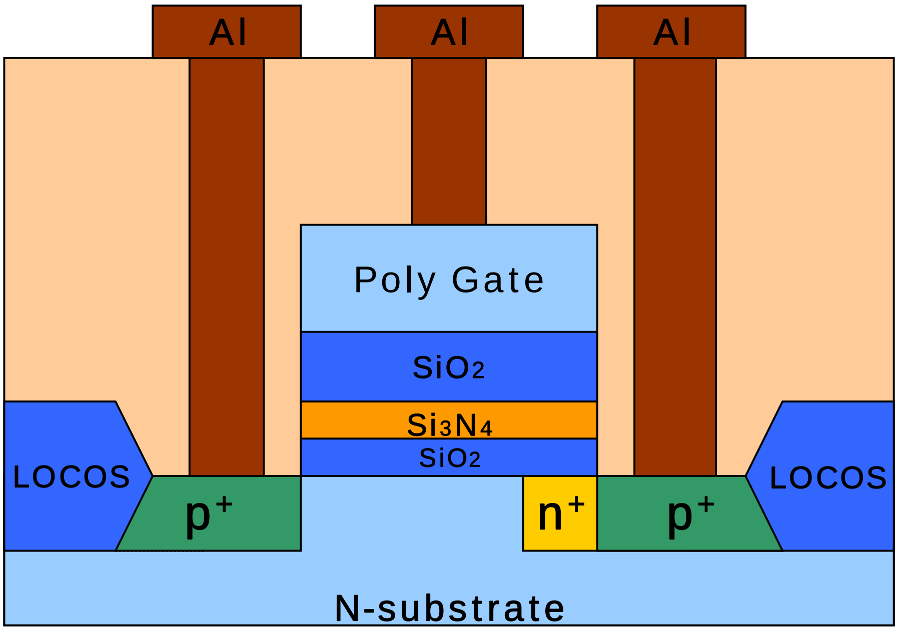


Fig. 3-4 (j)

Fig 3-4 Process flow of the Zener junction SONOS memory

Tilt Implantation			
Number	**Source**	**Does (cm^{-2})**	**Note**
PMOS-5E13	**P_{31}**	**5E13**	**Single side tilt implantation**
PMOS-1E142	**P_{31}**	**1E14**	
PMOS-5E14	**P_{31}**	**5E14**	
PMOS-Con.	**Substrate:1E12~5E12**		

Source/Drain Implantation		
Number	**Source**	**Does (cm^{-2})**
PMOS-S5E13	**BF2**	**5E15**
PMOS-S1E14	**BF2**	**5E15**
PMOS-S5E14	**BF2**	**5E15**
PMOS-Con.	**BF2**	**5E15**

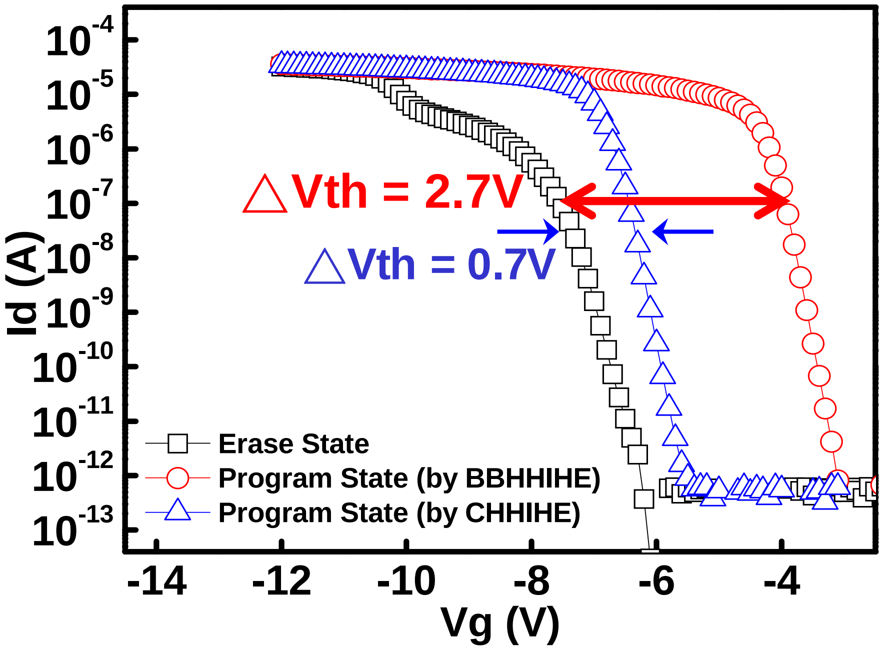
Table 3-1 Split Table of Implantation

3.3 Results and Discussion

In this section, the electrical characteristics of n-channel SONOS flash memory were discussed.

3.3.1 Id-Vg Curve

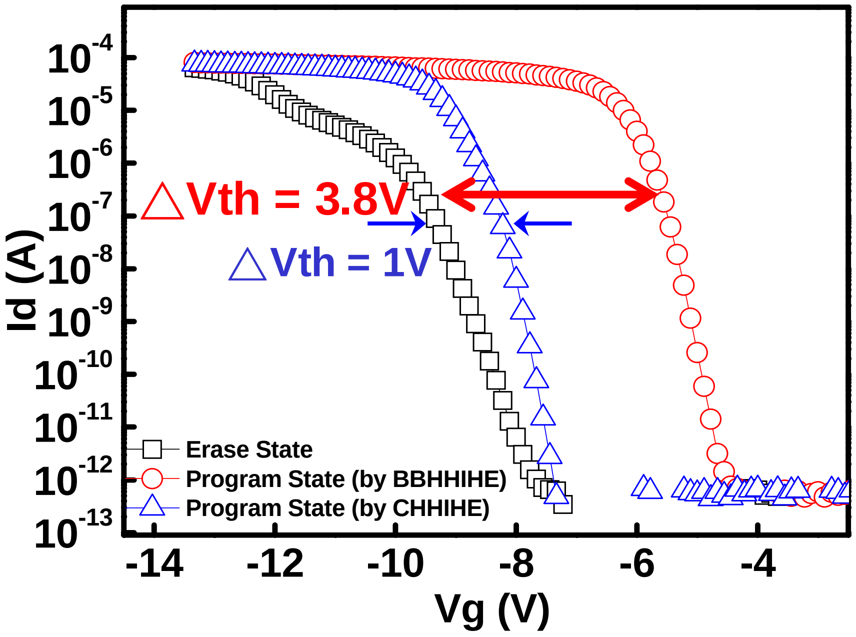
Figure 3-4 shows the Id-Vg curve of the conventional device under programming and erasing operations and figure 3-5 shows the Zener device ones. We use the constant current method to define the Vth (Id = 1 nA) here. We employ band-to-band tunneling induced hot electron injection (BBHHIHE) method to program the device and drain side FN method to erase device. And, because of the programming speed by the CHHIHE method is not efficiency, we employ the BBHHIHE method as our programming operation. The programming condition is Vg = 10V, Vd = -8V with 50 ms stress. The erasing condition is Vg = -10V, Vd = 8V with 10 ms stress and the source node is floating. Figure 3-1 shows the programming mechanism plot and figure 3-3 shows the erasing mechanism plot. The Vth of the conventional device between programming state and erasing state is about 2.7V shift. And the Vth of the Zener device between programming state and erasing state is about 3.8V shift. We think the Vth Shift rightward is due to electron injection into the trapping layer. When we give a voltage to memory device, the energy band bending will occur. And then carriers injection occurred during programming and erasing operation. Under programming operation, the electrons in the substrate gain energy from applied Vg and Vd. If the energy is enough to overcome the energy barrier, the hot electrons will inject into the nitride trapping and then be trapped. The phenomenon caused Vth shift. As erasing, the positive Vd would make the p+/n+ junction at forward state, and generate more electron-hole pairs in the substrate. Then the negative Vd would supply holes energy to injecte into the trapping layer, and then Id-Vg curve shifts leftward.



Program：Vg=10V, Vd=-8V, tp=50ms

Erase：Vg=-10V, Vd=8V, te=10ms

Fig. 3-5 Id-Vg curve of the conventional device



Program：Vg=10V, Vd=-8V, tp=50ms

Erase：Vg=-10V, Vd=8V, te=10ms

Fig. 3-6 Id-Vg curve of the Zener device

3.3.2 Program and Erase Speed

Figure 3-7 shows the programming speed of the conventional device and the Zener device. It show that the Zener device is faster than the convention device. Just like the plot showing, the programming speed of Zener device increased as the concentration of n+ region increasing. Figure 3-8 depicts the junction band diagram as programming bias state. First, because the electric field in n+/p+ junction is higher than in n/p+ junction, hot electron generated by band-to-band hot hole can get higher energy to overcome the tunneling oxide barrier. Second, the n+/p+ junction has larger energy band bending at the junction with programming bias as figure 3-8, the Zener device will have more band-to-band hot hole current than the conventional device. Hence the electron injection efficiency in the Zener device is higher than the conventional device. From these two points, the programming speed can be improved with the Zener junction.

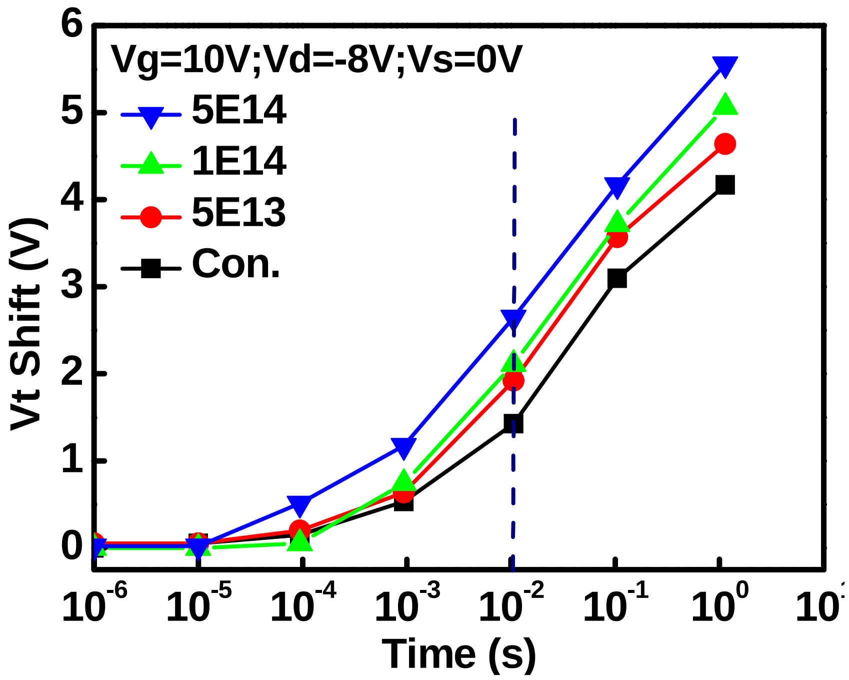
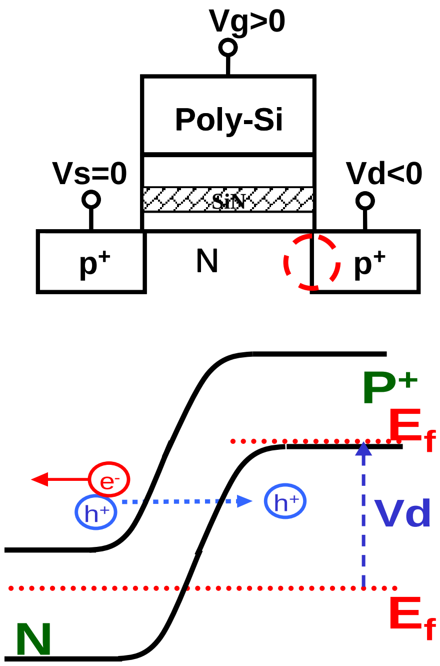
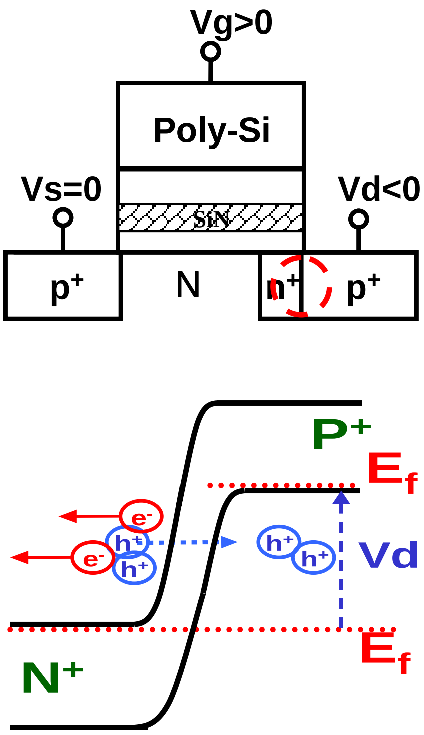


Fig. 3- 7 Programming speed of the Zener device and the conventional device



(a) The conventional device



(b) The Zener device

Fig. 3- 8 Tunneling oxide band diagram at programming state

Figure 3-9 depicts the erasing speed mechanism. It shows that the Zener device is faster than the convention device. The erasing speed of the Zener device increased as the concentration of n+ region increasing. Figure 3-10 shows the tunneling oxide band diagram as erasing state. When the n+ channel is in erasing operation, the Zener device will have more tunneling oxide bend banding than the conventional device. Hence the electron injection efficiency in the Zener device is higher than the conventional device. We suggest another reason is the higher electric field near the junction of the Zener device. When a positive voltage apply to drain node, the n+/p+ junction were biased at forward condition. Because the drain side FN could be assisted by the forward current generating more number of electron-hole pairs, the erasing efficiency is higher than FN erase only with large negative bias. Last, the Zener device has the larger electric field, and it makes more hot holes tunneling into the trapping layer with negative gate bias. So, the Zener device has better erasing characteristics than the conventional device.

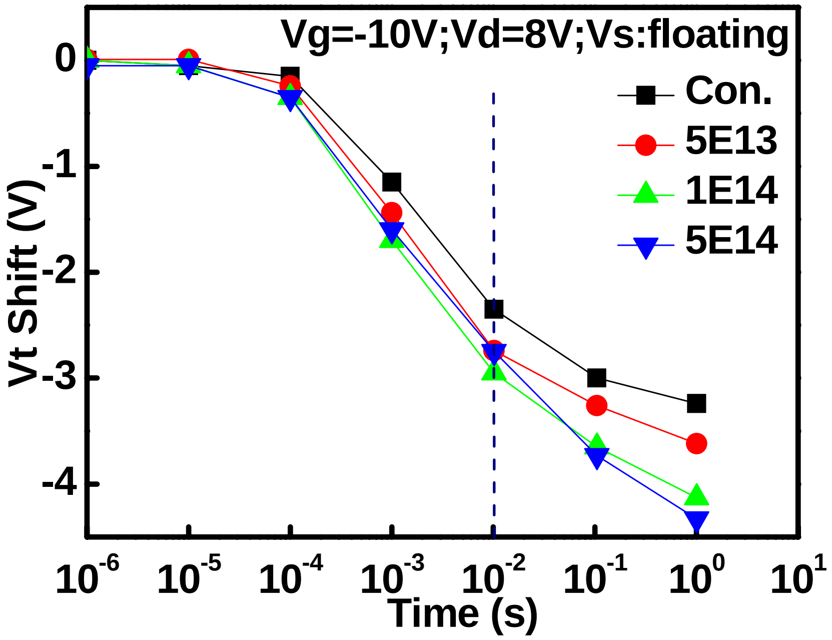
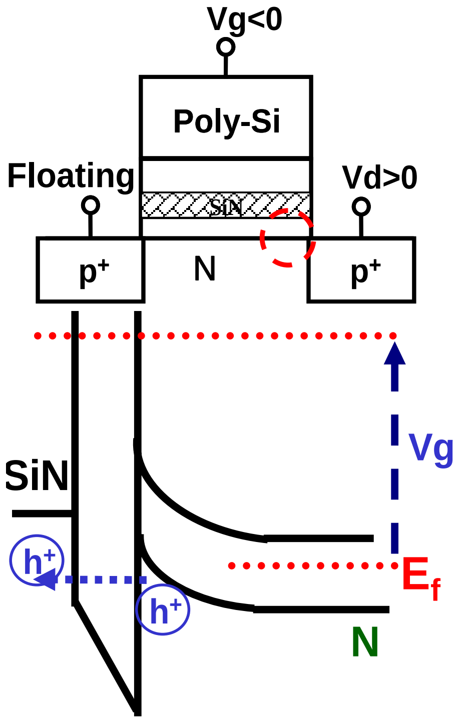
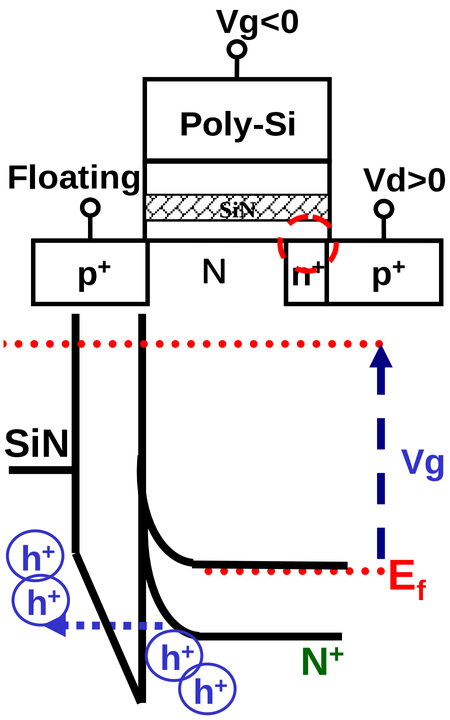


Fig. 3- 9 Erasing speed of the Zener device and the convention device



(a) The conventional device



(b) The Zener device

Fig. 3-10 Junction band diagram at erasing state

3.3.3 Data Retention Characteristic

Figure 3-11 is the data retention characteristic of the Zener device and the conventional device measured at room temperature. We find the charge loss after 1E4 seconds of the Zener device with similar chare loss mount to the conventional device. The curve shows 5%~10% charge loss of the Zener device as measure time up to 1E4 seconds at room temperature. Because the larger electrical field in the Zener device, they caused the tunneling oxide degradation a little serious. But it is acceptable in the Zener device.

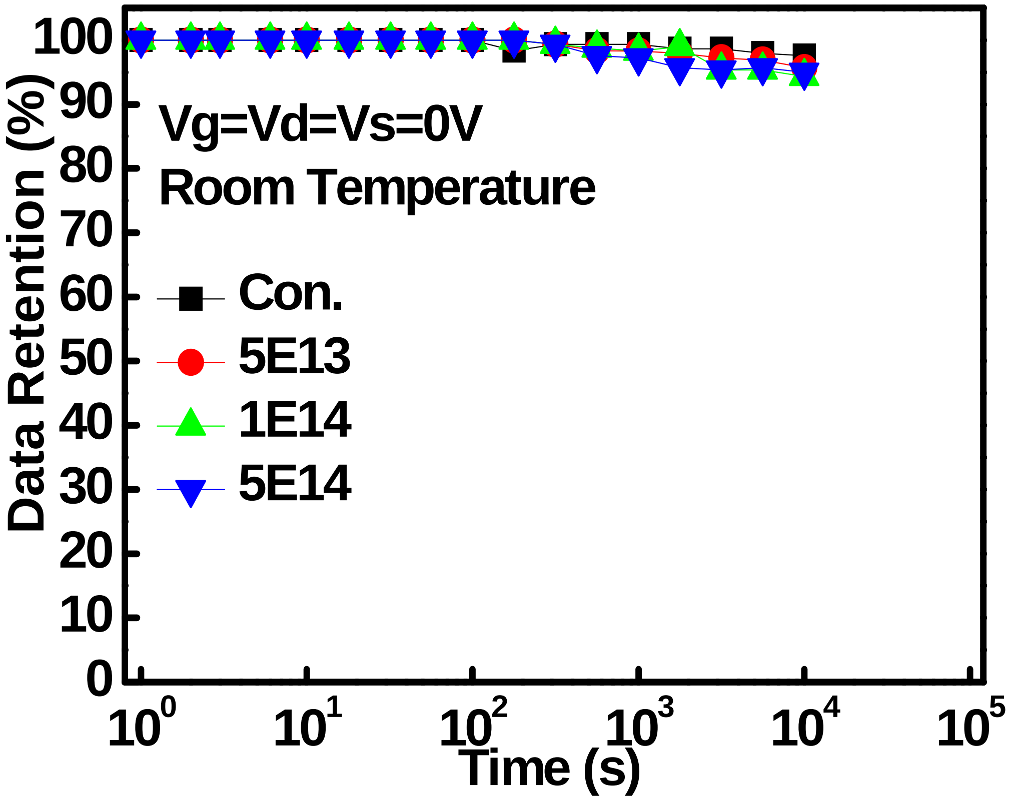


Fig. 3-11 Data retention characteristic of the Zener device and the conventional device

3.3.4 Drain Disturbance Measurement

Figure 3-12 shows drain disturbance measurement of the Zener device and the conventional device. We applied Vd = -10V and Vd = -8V with Vg = Vs = Vb = 0V to the all device. From figure 3-13, we find that the drain disturbance is slightly serious in the Zener device than the conventional device, and in the figure 3-14 the drain disturbance is much lightly compared with figure 3-13. The reason is that the Zener device has higher electric field with positive drain voltage. The larger drain voltage will make drain disturbance more seriously.

And the memory device is operated at Vd= -8V as erasing, the drain disturbance characteristics of 5E13cm^{-2} dose is better in all Zener device.

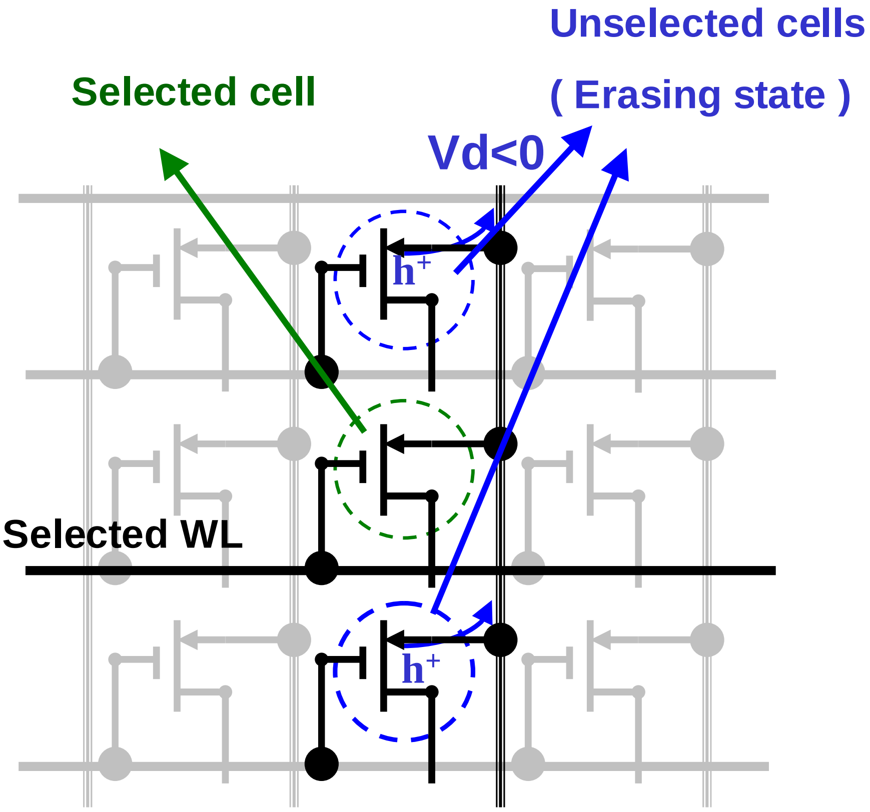


Fig. 3-12 Drain disturbance as the memory device at erasing state

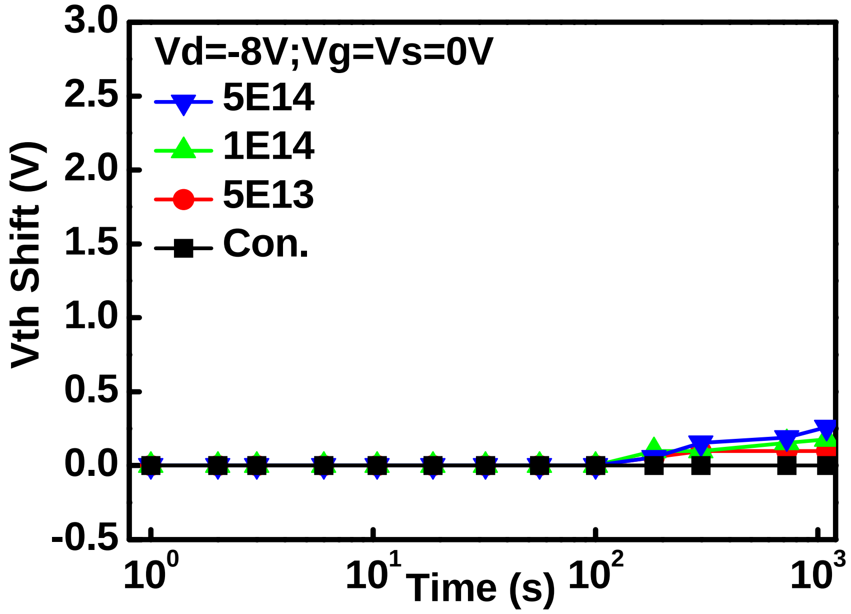


Fig. 3-13 Drain disturbance between the Zener device and the conventional device at Vd = -8 V

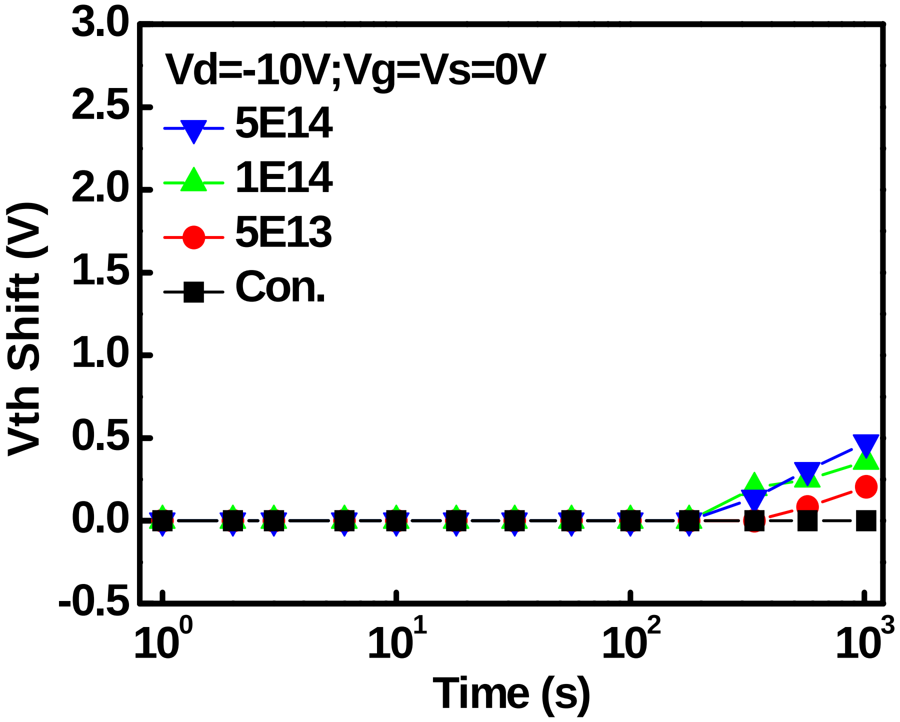


Fig. 3-14 Drain disturbance between the Zener device and the conventional device at Vd = -10 V

3.3.5 Endurance Characteristic

Figure 3-15 displays the endurance characteristic of the conventional device and figure 3-16 displays it the Zener device. We find that the endurance in the conventional is the worst case and the Zener shows the better endurance characteristic. Because charge injection region in our operation mechanisms between the programming operation and the erasing operation are similar as figure 3-17. The charge injection location may be more closely between program and erase, so the endurance is better. And the Zener junction device has narrower electric field distribution and higher maximum electric field magnitude. Hence we think that the charge is more concentrated in the Zener device, and the endurance can be improved.

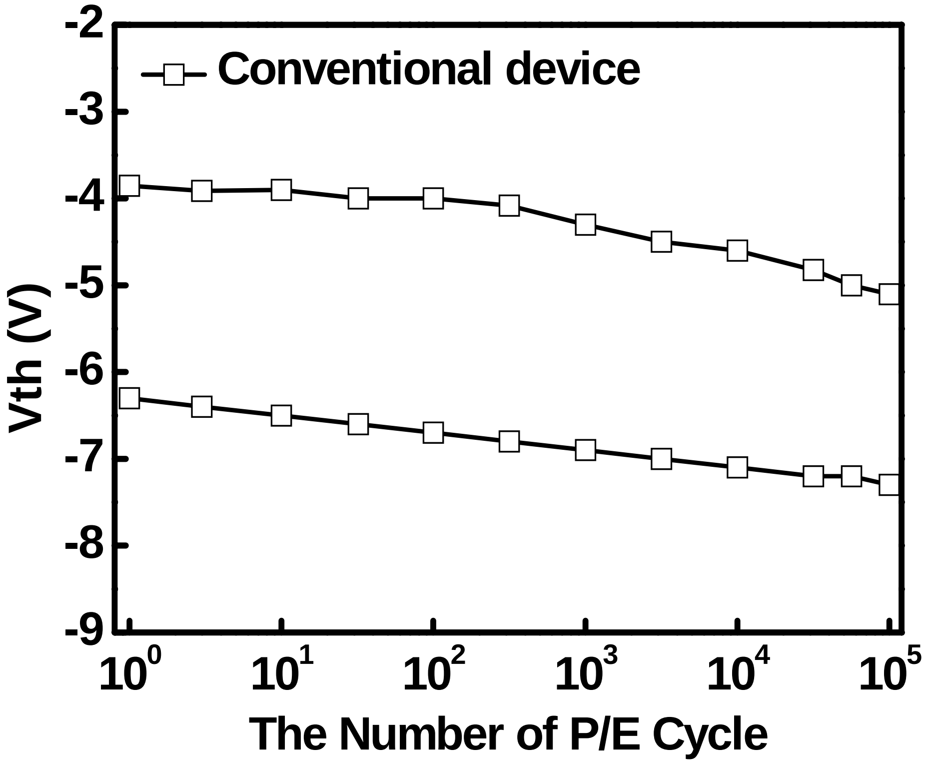


Fig. 3-15 Endurance characteristic of the conventional device

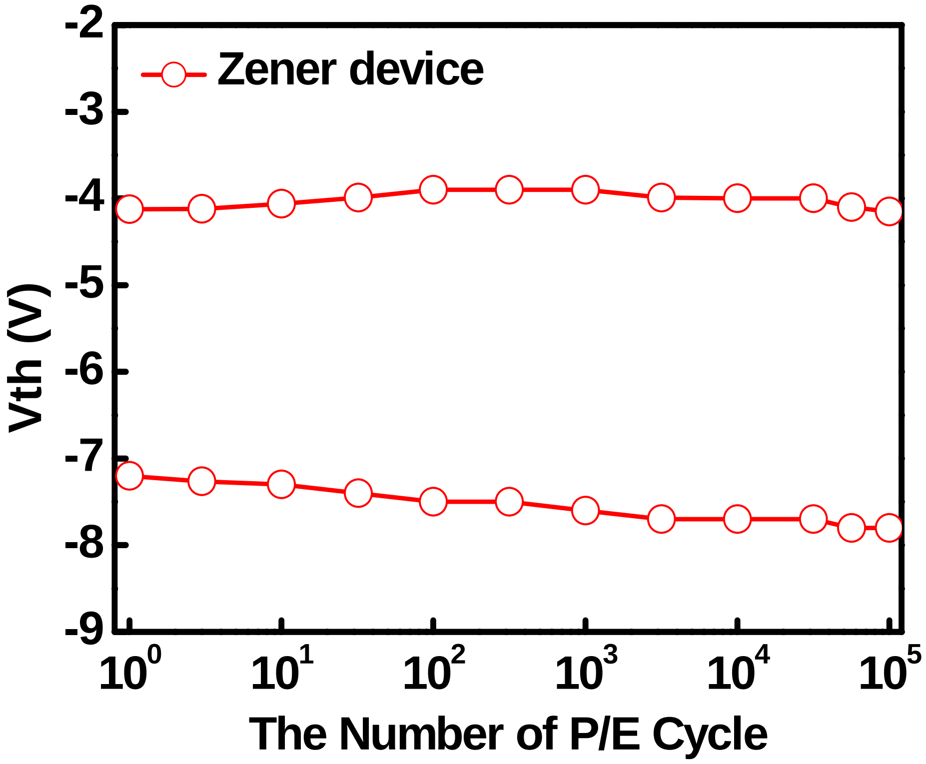
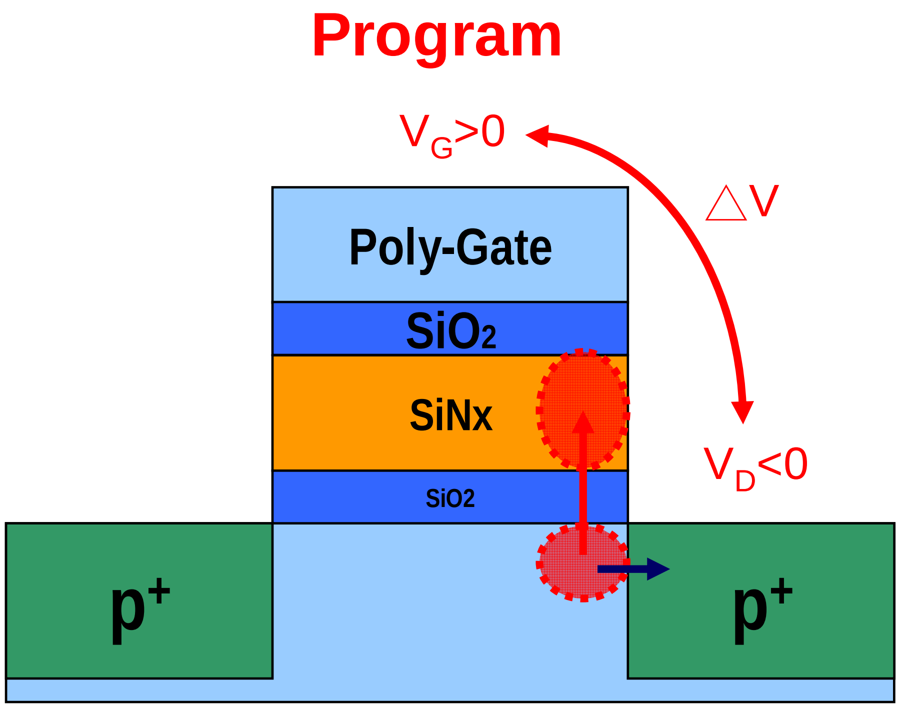
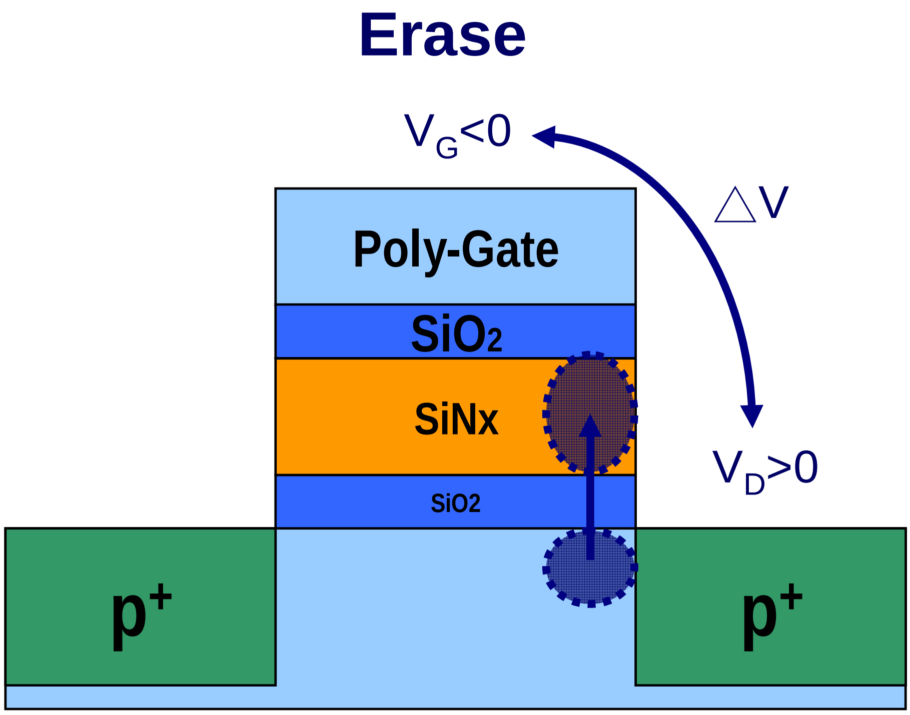


Fig. 3-16 Endurance characteristic of the Zener device



(a) Programming operation



(b) Erasing operation

Fig. 3-17 Charge injection region in the P-channel memory as programming and erasing operation

3.4 Summary

The impacts of tilt implantaion on programming and erasing performance are beneficial for the SONOS device. We can make injection efficiency higher by higher electrical field during programming and erasing operation to get better programming and erasing speed. Due to the narrower electric field distribution and the closely charge stored region because of the similar operation methods of programming and erasing, we improve the endurance characteristic. The Zener device shows a little degradation in the data retention and drain disturbance than the conventional device. We can choice the lightly tilt implantation dose to avoid these disadvantages.

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CHAPTER 4

Conclusion

The thesis of “ The Characteristic of SONOS Flash Memory with Zener Junction ” was proposed. The results of each chapter are summarized as below.

In chapter 2, the impact of Zener junction on programming and erasing performance is beneficial for the SONOS device. The injection efficiency increased by higher electric firld during programming and erasing gets faster programming and erasing speed. The double sides Zener device just shows a little degradation in the data retention compared with the conventional device.

In chapter 3, the impact of Zener junction on programming and erasing performance is beneficial for the SONOS device. We can make injection efficiency higher during programming and erasing to get better programming and erasing speed. Due to the narrower electric field distribution and the closely charge injection region during programming and erasing operation, we improve the endurance characteristics. But the Zener device shows much degradation in the data retention and drain disturbance, it is still a difficult in our study.

In the thesis, we improve the carrier injection efficiency of both n-channel memory and p-channel memory with the Zener junction structure. And the drain side FN erasing method in p-channel SONOS memory shows higher hole injection efficiency in p-channel memory.Endurance characteristics are also improved by the Zener junction structure because of the less stress time during programming and erasing. This memory cell with Zener junction can be implemented in advance charge trapping memory application.

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（民國96年7月）

論文題目：利用齊納接面改善氧化矽/氮化矽/氧化矽
堆疊式快閃記憶體之特性
Study on SONOS Flash Memory with Zener Junction
at Source/Drain Side

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