國 立 交 通 大 學

電子工程學系 電子研究所

碩 士 論 文

背向散射理論應用於金氧半場效電晶體之非匹配特性研究

Backscattering-Oriented MOSFET Mismatch Experiment

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中華民國九十七年七月

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摘要

在這篇論文中我們提出了幾個數學模型來呈現背向散射理論中金氧半場效電晶體裡數個參數的不匹配特性。我們從實驗中萃取了 K_BT 層的寬度加以分析，並且運用拋物線能障理論提出了物理模型來呈現它的不匹配特性。除此之外，這篇論文中也討論到了平均自由路徑和背向散射係數的不匹配特性。為了精準的理由，我們將汲極和源極電阻考慮在我們的參數萃取和模型上。最後我們提出了一個物理模型來計算飽和區電晶體的電流不匹配效應。

Backscattering-Oriented MOSFET Mismatch Experiment

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Abstract

In this thesis, we have derived several mathematical models to express the mismatch properties of MOS transistors based on the backscattering theory. We have extracted the K_BT layer's width from the experimental analysis and we have found a simple model to express its mismatch properties based on the parabolic potential barrier. The mean-free-path and the backscattering coefficient have also been discussed in this thesis. For the purpose of the accuracy, the source/drain series resistance has been incorporated in to our parameters extraction. Straightforwardly, we have developed a drain current mismatch model based on backscattering theory in the saturation region.

Acknowledgement

就在打這頁的同時，長達六年的交大生涯也即將結束，當然也包括兩年的研究所時光。在這段期間，遇到了很多事情，也學到了不少東西。雖然這些年的生活得到許多有趣的理工知識，但我始終認為最珍貴的，是我在這段時間所遇到的"人"。因為有這些夥伴，我才有動力可以往前，才能有去體驗不同事物的渴望。因為有陳明哲教授的教導，使得我了解到做研究所需要的精神和方法；因為有謝振宇、李建志、許智育和李韋漢學長們在知識上的傳承，使的我做研究的過程更為順利；呂立方、周佳弘、林以唐、梁惕華、陳彥銘、簡鶴年同學以及湯侑穎、陳又正、陳以東學弟們的陪伴，使得兩年多的研究時光並不孤單；除了實驗室的夥伴，無論是大學四年的同學、室友，或者是打球的球友，都讓這些日子的生活更益多采多姿，在此要感謝每個人的幫助和陪伴。最後要感謝的就是在美國默默支持我的家人，雖然這段時間每年見面的時間並不多，但是學期中透過短暫的電話以及信件，都讓我獲得莫大的力量。這篇論文的完成並不是一個結果，只是一個過程，因此在往後的人生旅途上，希望這份羈絆可以繼續延續下去。

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Chapter 1
Introduction

Section 1.1 Mismatch in MOS Transistors

This dissertation is a contribution to the discussion on the mismatch properties of MOS transistors based on backscattering theory. Mismatch is the process that causes time-independent random variations in physical quantities of identically designed devices. In MOS transistors, It is well recognized that most MOS parameters variations are mainly caused by the doping variation , such as threshold voltage, drain induced barrier lowering(DIBL), backscattering coefficient, etc. And these variations will directly effect the MOS transistor properties and performance, thus mismatch research plays an important role in the design of accurate analog circuits and digital circuits in the future. What we want is deriving a mismatch model to express the variation from long channel to short channel at different electric field and the mismatch properties of the nanoscale device in the future will also be clearly showed.

Section 1.2 Organization of This Thesis

Chapter 1 is a brief introduction about this dissertation and our work. In Chapter 2 of this dissertation, we have discussed the backscattering theory and some parameters

extraction method, including the traditional backscattering coefficient extraction and parabolic potential model [1]. On the other hand, we applied the drain/source series resistance theory in our parameter extraction by using constant mobility method [2].

In Chapter 3, we have derived several mismatch model based on the backscattering theory. The first mismatch model is derived by the parabolic potential theory [1]. On the other hand, it is well-known that the backscattering coefficient can be expressed as:

$$r_c = \frac{\ell}{\lambda + \ell}$$

where ℓ and λ are the critical length in the channel near the source that the conduction band bends down by a thermal energy of K_BT (K_BT layer's width) and mean free path. The ℓ variation will be analyzed in this part. Based on this mismatch model, R_C mismatch model is also derived and discussed. The third mismatch model is developed by using drain current equation in saturation region:

$$I_D = W \times C \times V_{inj} \times \left[V_G^{'} - \left(V_{tho} - DIBL \times V_D^{'} \right) \right] \times \frac{1 - R_C}{1 + R_C}$$

where V_{ing}, V_{tho} are the thermal injection velocity at the top of source-channel junction barrier and the quasi- equilibrium threshold voltage. In this model, the drain current mismatch can be expressed as a function of three parameters variation: V_{tho}, Rc, and DIBL. We have also compared our mismatch models with experiments in chapter 3, whereas the details of data extraction about experiment will be discussed in the chapter 2.

Chapter 2
Backscattering Theory and Parameters Extraction

Section 2.1 Backscattering Theory

The backscattering theory describes the near-equilibrium scattering process near the source when the electrons travel across the channel. Electrons are injected from the source into the channel and only those over a potential barrier can be collected by the drain. This potential barrier is the conduction band which bends "up" due to the presence of the source-channel junction and then bends down due to the channel electric field caused by drain voltage. This barrier may be linked to drain-induced barrier lowering. As schematically shown in Fig. 1, ℓ is the length across which the conduction band bends down by a thermal energy of K_BT, where T is the temperature, and K_B is the Boltzmann's constant. This length is known as the width of K_BT layer. Backscattering is mainly occurring in the K_BT layer due to the lattice and carrier. The backscattering coefficient, R_C, is determined to describe the scattering in the K_BT layer, as shown in Fig. 1, R_C can be written as:

$$R_C = \frac{\ell}{\ell + \lambda} \qquad (1)$$

where λ is the mean-free-path and ℓ is the width of K_BT layer. We note that R_C is determined by the electric field profile very near the source where the electrons have been heated to no more than K_BT/q. Thus the λ can be estimated by the near-equilibrium low–field mobility. To derive an equation about drain current based

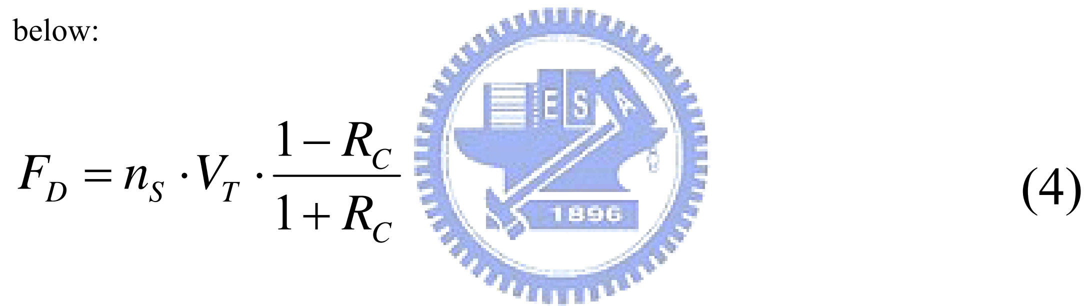
on the backscattering coefficient, we assume that there is a source flux F injected into the channel and part of F will be reflected back to the source. From Fig. 1, the flux entering the drain can be expressed as:

$$F_D = F_S\left(1 - R_C\right) \tag{2}$$

Here we assume the flux reflected back to the source from the channel does not reflect. Thus the electron density in the source side can be expressed as:

$$n_s = \frac{F_S \cdot (1 + R_C)}{V_T} \tag{3}$$

where the V_T is the velocity of the flux. From (2) and (3), we can obtain an equation below:



$$F_D = n_S \cdot V_T \cdot \frac{1 - R_C}{1 + R_C} \tag{4}$$

As a result, we find

$$I_D = Q \cdot V_T \cdot \frac{1 - R_C}{1 + R_C} \tag{5}$$

where Q is the charge density per unit area. In the saturation region, above equation can be also written as:

$$I_D = W \cdot C_{eff} \cdot \left(V_G - V_{th}\right) \cdot V_T \cdot \frac{1 - R_C}{1 + R_C} \tag{6}$$

This is the backscattering theory based current equation in saturation region used in this thesis. We can note that there is no mobility parameter in this formula and the drain current heavily depends on the new parameter: R_C. For example, in the ballistic situation R_C =0, the drain current is governed by the thermal injection velocity [1].

From (6), we can extract R_C from several processes in the experiment. In order to get the parameter accurately, the drain-induced-barrier-lowering and drain/source series resistance must be considered. Thus equation (6) should be modified as:

$$I_D = W \cdot C_{eff} \cdot \left[\left(V_G - I_D R_S \right) - \left(V_{tho} - DIBL \cdot \left(V_D - I_D \cdot R_{SD} \right) \right) \right] \cdot V_T \cdot \frac{1 - R_C}{1 + R_C} \quad (7)$$

The R_S, R_D and DIBL parameters extraction will be discussed later.

Section 2.2 Parabolic Potential Barrier

If there is no electric field, the backscattering coefficient can be simply written as [4]:

$$R_C = \frac{L}{L + \lambda} \quad (8)$$

When the electric field is present, the conduction band will bend down and the backscattering coefficient should be expressed as [5]:

$$R_C = \frac{\ell}{\ell + \lambda} \quad (9)$$

Because the value of backscattering coefficient highly depends on ℓ which is the width of K_BT layer, the quantity of ℓ is an important issue in the backscattering theory. The parabolic potential barrier-oriented compact model is a key to solving this

problem. We assume that the conduction band bends down as a parabolic situation and the equation of potential drop can be described as:

$$V(x) = V_D\left(x / \tilde{L}\right)^2 \qquad (10)$$

$\tilde{L}$ is the distance that the conduction band drop from the top of the barrier to V_D. The definition of the width of the K_BT layer is that the critical distance that the conduction band potential drops K_BT /q. So we substitute x and V(x) in above equation as ℓ and K_BT/q. Thus the equation can be rewritten as:

$$\ell = \tilde{L}\left(\frac{K_B T}{q V_D}\right)^{0.5} \qquad (11)$$

This is an equation about the relation of $\tilde{L}$ and ℓ based on parabolic potential model, whereas $\tilde{L}$ is expected to be a function of channel length, drain voltage, gate voltage, and temperature. To derive the relation between $\tilde{L}$ and L, thus V_{G0}, V_{D0}, and T_0 must be defined in order to ensure that $\tilde{L}$ = L in these situations and ℓ_0 can be calculated from this function in these situations (V_D-> V_{D0}, V_G-> V_{G0}, T->T_0). To find the relation of these parameters, the different parameters should be discussed separately. The process of the equation derivation between $\tilde{L}$ and each parameter was discussed in [1] and $\tilde{L}$ can be expressed as:

$$\tilde{L} = \eta L \frac{V_D^{0.25}}{(V_G - V_{th})^{0.5}}\left(\frac{K_B T}{q}\right)^{0.5} \qquad (12)$$

where $\eta = (K_B T_0 / q)^{-0.5}(V_{G0} - V_{th})^{0.5} V_{D0}^{-0.25}$ and it is a constant that can be known by fitting in experiment [1]. In this thesis, we consider that n=4.1($V^{-0.25}$). Substituting

the $\tilde{L}$ in equation (12) to equation (11), a compact relation between ℓ and bias, device geometrical parameters can also be obtained:

$$\ell = \eta L \frac{V_D^{-0.25}}{(V_G - V_{th})^{0.5}} \left(\frac{K_B T}{q}\right) \tag{13}$$

From equation (13), We have extracted ℓ for W/L = 0.13um/0.065um, 0.24um/0.065 um, 1um/0.065um, 0.13um/0.1um, 0.24um/0.1um, 1um/0.1um, 0.13um/1um, 0.24um/1um, 1um/1um, 0.13um/10um, 0.24um/10um, and 1um/10um all at V_G = 1 V, V_G = 0.7 V, and V_G = 0.5V for V_D = 1 V. On the other hand, ℓ extracted experimentally is also shown for comparison. In Fig. 2, open circle represents the mean value of ℓ extracted by parabolic potential model and open triangle represents the mean value of ℓ extracted experimentally.

Section 2.3 Mean-Free-Path

The backscattering coefficient can be written as (1). λ is the low-field mean-free-math and can be linked to μ_{n0} through

$$\lambda = 2\mu_{n0}(K_B T / q)/V_{inj} \tag{14}$$

where V_{ing} is the thermal velocity and μ_{n0} is the near-equilibrium mobility because that the backscattering occurs very near the source and it can be regard as a near-equilibrium case even there is a strong electric field in the channel due to the drain voltage [3]. Fig. 3 shows the mobility versus channel length, whereas the mobility is obtained from G-D method. It can be seen that there is a drop of the mobility when the channel length decreases due to the short channel effect. Fig. 4

displays the mobility versus gate voltage and the three components, which affect the curve of the mobility, can be clearly expressed by the following scatterings: Coulomb scattering, phonon scattering, and surface roughness scattering. Substituting above mobility data into equation (13), the mean-free-path can be obtained. Fig. 5 and Fig. 6 show the mean-free-path versus the channel length at V_G = 1V, and 0.5V, and the mean-free-path versus the intrinsic gate voltage, respectively. Here the thermal velocity is substituted as 10^7 cm/sec in equation (14). In order to get the backscattering coefficient, we substitute the mean-free-path obtained and the ℓ extracted from parabolic potential model into equation (2). Fig. 7 displays the backscattering coefficient versus channel length at different device widths for V_G = 1V. The open circle represents the backscattering coefficient extracted from different mean-free -paths for different channel lengths. The open triangle represents the backscattering coefficient extracted from the same mean free path in the long channel case because we consider the mean free path as a parameter due to the material (independent of L). The backscattering coefficient extracted from experiment is also shown in Fig. 7 and labeled by the open square. It can be seen that the backscattering coefficient decreases as the channel length decreases in these cases and the open triangle are closer to the experimental data compared to those of short channel length devices.

Section 2.4 Drain/Source Series Resistance Extraction

In order to extract the accurate parameters such as backscattering coefficient in this work, the existence of the series resistance R_{SD} should be considered. The series resistance R_{SD} is the resistance in source and drain side of MOSFET. In the past,

because the channel resistance of the long channel device is huge compared with the series resistance, the series resistance can be ignored. But in today's MOSFET nanoscale technology, the existence of the R_{SD} may lead to many problems such as the drive current degradation and parameter extraction accuracy. In the traditional method, the R_{SD} can be extracted from different gate voltage and devices of different channel lengths. The conventional method is not accurate at short channel situations. So we use a new method called constant-mobility-method to extract R_{SD} [2]. The constant mobility method is used to extract R_{SD} in the high oxide electric field region where surface roughness scattering becomes the dominant mechanism. In the high electric region, a constant mobility is achieved for a given effective vertical electric field, regardless of impurity scattering and phonon scattering, and the change of V_{BS} will lead to the same mobility in this region. The current equation of MOSFETs operating in the linear region can be expressed as:

$$I_D^{(1)} = \frac{C_{ox} W_{eff} \mu^{(1)}}{L_{eff}} (V_{gs}^{(1)} - V_{th}^{(1)} - \frac{1}{2} V_{ds}) \left(V_{ds} - R_{sd} I_d^{(1)} \right) \quad (15)$$

$$I_D^{(2)} = \frac{C_{ox} W_{eff} \mu^{(2)}}{L_{eff}} (V_{gs}^{(2)} - V_{th}^{(2)} - \frac{1}{2} V_{ds}) \left(V_{ds} - R_{sd} I_d^{(2)} \right) \quad (16)$$

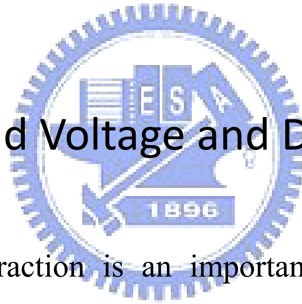
Equation (15) and equation (16) apply to linear operation mode at different V_{BS} and V_{DS} =0.01 V. To extract R_{SD}, we assume that $\mu^{(1)} = \mu^{(2)}$ and substitute the mobility of equation (15) as equation (16). Then the R_{SD} can be written as:

$$R_{sd} = \left(\frac{B}{I_d^{(2)}} - \frac{A}{I_d^{(1)}} \right) \frac{V_{ds}}{\eta (V_{th}^{(1)} - V_{th}^{(2)})} \quad (17)$$

$$A = V_{gs}^{(1)} - V_{th}^{(1)} - \frac{1}{2} V_{ds}$$

$$B = V_{gs}^{(1)} + (\eta - 1)V_{th}^{(1)} - \eta V_{th}^{(2)} - \frac{1}{2}V_{ds}$$

Fig. 8 shows the R_{SD} extracted by equation (17) for W/L=0.24um/0.1um and W/L=0.24um/0.065um and we focus on V_G>1V to ensure a high electric field condition. Fig. 9 shows the R_{SD} extracted at different V_{BS} conditions. Fig. 10 shows the R_{SD} extracted from different devices at the same scale. We have done many experiments in order to ensure that the R_{SD} extracted from different channel length and bias conditions should be a constant. The R_{SD} value extracted from the constant mobility method at different device dimensions will be used in some parameters extraction in this thesis.



Section 2.5 Threshold Voltage and DIBL

The threshold voltage extraction is an important part in the MOS transistors research and a key parameter in this work. We employ a maximum tran-conductance method in the linear region to assess quasi-equilibrium threshold voltage and the constant subthreshold current method in the saturation region to extract the DIBL. The maximum tran-conductance is a method establishing a tangent line from the point where the tran-conductance is the maximum to show the threshold voltage in the I_D-V_G gragh. We set the drain voltage V_D = 10mV to ensure the quasi- equilibrium case. Fig. 11 shows drain current versus gate voltage and the maximum tran-conductance method.

The Drain Induced Barrier-Lowering is the decreasing of the threshold voltage when the drain voltage increases, caused by conduction band bends lowering. In other words, the channel control from the gate will weaken at high drain electric field,

especially in the short channel devices. To develop the mismatch model accurately, the DIBL must be considered. We use the constant subthreshold current method to calculate the threshold voltage shift due to the V_D increase and measure the DIBL in the saturation region. We set the drain voltage V_D = 1V to ensure that the device is operated in the saturation region.

Chapter 3
Mismatch Experiment and Results

Section 3.1 Mismatch Model

The mismatch model is a mathematical equation to express the variation of the parameter. The mismatch properties have two features: the total mismatch of the parameter is composed of many single events of the mismatch-generating process and the effects on the parameter are so small that the contributions to the parameter can be summed [6]. The mismatch properties of threshold voltage are the main topic of mismatch since 1970s. In this thesis, our mismatch model is developed based on the research of threshold voltage in the traditional theory and the backscattering theory. To reach for our goal, we must develop the mismatch model step by step. First of all, we focus on the width of the K_BT layer and analyse its mismatch properties. Then we develop the backscattering coefficient mismatch properties in the next step.

One of the fundamental factors limiting the accuracy of MOS circuits is the current mismatch between identically devices. So, based on above considerations and series resistance extraction, the drain current mismatch model will be presented later. The transistors in the circuits usually operate in the saturation region. Thus, the mismatch models in this thesis are all developed and discussed in saturation region.

Section 3.2 Experiment

The measurement procedure is an important part in the mismatch work. Generally, to obtain the statistical variation, we need to measure a lot of devices. In this work, we measure over than 20 different dimensions of n-channel devices, whereas each scale has more than 30 dies on the wafer. All dies are made from the same process and have the same structure. They were fabricated using 65nm CMOS process. We measure our drain current by sweeping gate voltage from 0 to 1.2 V in a step of 25 mV when we fixed the drain voltage at 0.01 V, 0.1 V, and 1 V in order to cover both the equilibrium case and the saturation region case. In the extraction of the series resistance, we set substrate bias VB at = -0.4 V, -0.8 V, and 0 V. The temperature was fixed at 298 K. The measurement setup includes the HP4156B and a Faraday box for shielding the wafer.

Section 3.3 Mismatch Properties of K_BT Layer's Width

The mismatch properties can be expressed as the standard deviation: σ. The standard deviation can be calculated from the parameters extracted in the experiment. In statistics, there should be more than 20 measured devices to ensure that the standard deviation calculated can be considered as the mismatch properties of all dies on the wafer. In this section, the standard deviations are calculated from over than 20 dies. The extreme variance of the parameter would be lead to high standard deviation. Fig. 12 shows the standard deviation of K_BT layer's width versus the gate voltage from experiments. It can be seen that the variance would decrease when the gate

voltage increases. To propose a simple statistical model to explain the phenomenon observed, we pay attentions to the equation of the K_BT layer's width. In Chapter 2, we introduce the parabolic potential barrier model to calculate the width of K_BT layer:

$$\ell = \eta L \frac{V_D^{0.25}}{(V_G - V_{th})^{1/2}} \left(\frac{k_B T}{q} \right)^{1/2} \left(\frac{k_B T}{q V_D} \right)^{1/2} \tag{18}$$

From above equation, we will express the mismatch of ℓ as a function of the variance of threshold voltage. The variance of standard deviation with one random variable x can be expressed as:

$$\sigma_\ell = \left(\frac{\partial \ell(x)}{\partial x} \right) \cdot \sigma_x \tag{19}$$

Thus, from equation (18) and equation (19), the standard deviation of K_BT layer's width can be written as:

$$\sigma_\ell = \left(\frac{A}{2 \cdot (V_G - V_{th})^{1.5}} \right) \cdot (\sigma_{Vth}) \tag{20}$$

where $A = \frac{K_B T}{q} \cdot \eta \cdot V_D^{-0.25} \cdot L (nm \cdot V^{0.5})$. The standard deviation can be expressed as a function of inverse square root of the device area [6]. Thus we obtain a compact model:

$$\sigma_\ell = \left(\frac{A}{2 \cdot (V_G - V_{th})^{1.5}} \right) \cdot \left(\frac{A_{Vth}}{\sqrt{WL}} \right) \tag{21}$$

where A is a constant depending on channel length and drain voltage and is independent of gate voltage. $A_{V_{th}}$ is the size proportionality constant for the variance

of threshold voltage, as shown in Fig. 13. From the threshold voltage term in above equation, we can observe that the variance of K_BT layer's width would decrease when the gate voltage increases because that the effect of the threshold voltage fluctuation would become smaller. In other words, the variance of K_BT layer's width is sensitive to threshold voltage in the weak inversion region. This is a simple mathematical model to understand the mismatch properties of K_BT layer's width and can calculate it from just three simple parameters: threshold voltage, device size, and drain voltage. Fig. 14 displays the mismatch calculations compared with the experiments for W/L=0.13um/0.1um, 0.24um/0.1um, and 1um/0.5um at drain voltage VD=1V. We can observe that the differences between the two are small. Fig. 15 shows that the variance of ℓ versus square root of L/W for different devices at fixed gate voltage VG=1V. When the gate voltage is high, the difference of the threshold voltage in equation (21) can be ignored and the standard deviation of K_BT layer's width can be proportional to the square root of channel length divided by device width (L/W). It can be clearly shown in equation (21) by separating the channel length (L) term from constant A and multiplied by the inverse square root of area. Another relation can be observed from dividing each sides of equation (21) by K_BT layer's width, where the channel length term in constant A would be deleted. Then the standard deviation divided by the mean of K_BT layer's width is proportional to the inverse square root of device area when gate voltage is high. Fig. 16 displays this relationship which is a traditional relationship like current factor or mobility [6].

Section 3.4 Backscattering Coefficient Mismatch

The backscattering coefficient R_C can be expressed as (1), whereas R_C is a function of two variables: mean free path and K_BT layer's width. To express the mismatch as these two parts, we applied a differential equation below for analysis:

$$\sigma^2_{P(x,y)} = \left(\frac{\partial P}{\partial x}\right)^2 \sigma_x^2 + \left(\frac{\partial P}{\partial y}\right)^2 \sigma_y^2 + 2C_{ov}(x,y)\left(\frac{\partial P}{\partial x}\right)\left(\frac{\partial P}{\partial y}\right) \quad (22)$$

where σ_x and σ_y, are the variance of x and y, respectively. C_{OV} (x, y) is the correlation coefficient between (x, y). We assume that the mean-free-path and K_BT layer's width are independent of each other, that is, the correlation coefficient C_{OV} (x, y) is zero. Thus the R_C mismatch model can be expressed as:

$$\sigma^2_{R_C(\ell,\lambda)} = \left(\frac{\partial R_C}{\partial \ell}\right)^2 \sigma_\ell^2 + \left(\frac{\partial R_C}{\partial \lambda}\right)^2 \sigma_\lambda^2$$

$$= \left(\frac{\lambda}{\lambda+\ell}\frac{R_C}{\ell}\right)^2 (\sigma_\ell)^2 + \left(\frac{-\lambda}{\lambda+\ell}\frac{R_C}{\lambda}\right)^2 (\sigma_\lambda)^2 \quad (23)$$

This is a simple mathematical model to estimate the fluctuation of R_C in the saturation region. The σ_ℓ is already discussed in Section 3.3 and the ratio σ_λ/mean(λ) can be obtained by the experiment. Both of them have a proportional relationship with the inverse square root of area. From these two different mismatch properties, the standard deviation of R_C can also be obtained, so does the standard deviation divided by the mean: σ_{RC}/mean(R_C). The mismatch properties of the mean-free-path should have the same properties as mobility in [7]. Fig. 17 shows the relationship between the σ_λ/mean(λ) and the inverse square root of area. Fig. 18 displays the standard deviation R_C versus gate voltage V_G from equation (23), compared with experiments

for W/L=0.13um/0.1um, and W/L=0.24/0.1um, all at VD=1V to ensure the saturation region. We can observe that the model and the experiments are quite close to each other.

Section 3.5 Drain Current Mismatch

Drain current mismatch properties is the last part of this work which directly affects the performance of the circuit. To develop the drain current mismatch model accurately, we considered the extracted series resistance:

$$I_D = W \cdot C_{eff} \cdot \left[\left(V_G - I_D R_S \right) - \left(V_{tho} - DIBL \cdot \left(V_D - I_D \cdot R_{SD} \right) \right) \right] \cdot V_T \cdot \frac{1 - R_C}{1 + R_C} \quad (24)$$

This is a whole drain current equation based on backscattering theory. We define that the current mismatch is the standard deviation divided by the mean: σ_{ID}/mean(ID). The standard deviation $\sigma_{g(x,y,z)}$ with three variables of x, y and z can be expressed as:

$$\sigma^2{}_{g(x,y,z)} = \left(\frac{\partial g}{\partial x}\right)^2 \sigma_x^2 + \left(\frac{\partial g}{\partial y}\right)^2 \sigma_y^2 + \left(\frac{\partial g}{\partial z}\right)^2 \sigma_z^2 + 2\left(\frac{\partial g}{\partial x}\right)\left(\frac{\partial g}{\partial y}\right) C_{OV}(x,y)$$
$$+ 2\left(\frac{\partial g}{\partial y}\right)\left(\frac{\partial g}{\partial z}\right) C_{OV}(y,z) + 2\left(\frac{\partial g}{\partial x}\right)\left(\frac{\partial g}{\partial z}\right) C_{OV}(x,z) \quad (25)$$

where σ_x, σ_y and σ_z are the standard deviation of x, y and z, respectively; and C_{OV}(x, y), C_{OV}(y, z), and C_{OV}(x, z) are the correlation coefficients of each variables. In this equation, we assume that these three coefficients are so small, leading to C_{OV}(x, y), C_{OV}(y, z), and C_{OV}(x, z) all being zero. Then the drain current can be expressed as:

$$\left(\frac{\sigma_{ID}}{I_D}\right)^2 = \left(\frac{1}{V_G - V_{tho} + DIBL \times V_D}\right)^2 \sigma_{Vtho}^2$$
$$+ \left[\frac{(1+\alpha+\beta)V_D - W \cdot C \cdot R_{SD}(V_G - V_{tho} + DIBL \times V_D)(1 - R_C / 1 + R_C)}{(1+\alpha+\beta)(V_G - V_{tho} + DIBL \times V_D)}\right]^2 \sigma_{DIBL}^2$$
$$+ \left(\frac{1}{1+\alpha+\beta}\right)^2 \frac{4R_C}{(1-R_C^2)^2} \left(\frac{\sigma_{R_C}}{R_C}\right)^2 \qquad (26)$$

$$\begin{cases} \alpha = W \cdot C \cdot V_{ing} \cdot R_s \cdot \dfrac{1-Rc}{1+Rc} \\ \beta = W \cdot C \cdot V_{ing} \cdot DIBL \cdot R_{sd} \cdot \dfrac{1-Rc}{1+Rc} \end{cases}$$

where σ_{Vth}, σ_{DIBL} and σ_{RC} can be proportional to the inverse of square root of area. Fig. 19 and Fig. 20 display the relationship between threshold voltage, DIBL and area. The variance of backscattering R_C is discussed in Section 3.4 already. Thus we have:

$$\sigma_{vth0} = \frac{A_{vtho}}{\sqrt{W \cdot L}}, \sigma_{DIBL} = \frac{A_{DIBL}}{\sqrt{W \cdot L}}, \sigma_{RC} = \frac{A_{RC}}{\sqrt{W \cdot L}} \qquad (27)$$

Substituting equation (27) into the drain current mismatch model, we obtain the compact model:

$$\left(\frac{\sigma_{ID}}{I_D}\right)^2 = \left(\frac{1}{V_G - V_{tho} + DIBL \times V_D}\right)^2 \left(\frac{A_{vtho}}{\sqrt{W \cdot L}}\right)^2$$
$$+ \left[\frac{(1+\alpha+\beta)V_D - W \cdot C \cdot R_{SD}(V_G - V_{tho} + DIBL \times V_D)(1 - R_C / 1 + R_C)}{(1+\alpha+\beta)(V_G - V_{tho} + DIBL \times V_D)}\right]^2 \left(\frac{A_{DIBL}}{\sqrt{W \cdot L}}\right)^2$$
$$+ \left(\frac{1}{1+\alpha+\beta}\right)^2 \frac{4}{(1-R_C^2)^2} \left(\frac{A_{RC}}{\sqrt{W \cdot L}}\right)^2 \qquad (28)$$

Fig. 21 shows the mismatch of current versus gate voltage for W/L=0.13um/0.1um, and 0.24um/0.1um, at V_D=1V to ensure the saturation region. We can observe that the current mismatch decreases when the gate voltage increases because that the

fluctuation of the threshold voltage, DIBL and backscattering coefficient would have smaller effects at high gate voltages. And we can also observe that the difference between the model and the experiments are small. In this mismatch, the variance of R_C is the dominant parameter which affects the drain current mismatch compared with threshold voltage and DIBL.

Chapter 4
Conclusion

We have developed a compact mathematical model for mismatch properties of MOS transistors in this thesis. Unlike the traditional research focused on threshold voltage variance only, we have incorporated additional parameters into discussion: DIBL and backscattering coefficient. We have done many works in detail based on the backscattering theory, covering K_BT layer's width and mean-free-path. Besides, many data have been measured in order to verify our mismatch model. Step by step, several mismatch models have been successfully developed to express the matching properties of each involved parameters, especially the K_BT layer's width and the drain current mismatch.

Reference:

[1] M. J. Chen, and Li-Fang Lu, “A Parabolic Potential Barrier-Oriented Compact Model for the K_BT Layer’s Width in Nano-MOSFETs,” *IEEE Transactions on Electron Devices, vol. 55, no. 5, pp. 1265-1268, May 2008.*

[2] Da-Wen Lin, Ming-Lung Cheng, Shyh-Wei Wang, Chung-Cheng Wu, and Ming-Jer Chen,” A Constant-Mobility Method to Enable MOSFET Series-Resistance Extraction,” *IEEE Electron Device Letters, vol. 28, no. 12, pp. 1132-1134, December 2007.*

[3] M. J. Chen, Huan-Tsung Huang, Yi-Chin Chou, Rong-Ting Chen, Yin-Ta Tseng, Po-Nien Chen, and Carlos H. Diaz, “Seperation of Channel Backscattering Coefficients in Nanoscale MOSFETs,” *IEEE Transactions on Electron Devices, vol. 51, no. 9, pp. 39-42,September 2004.*

[4] Raphael Clerc, Pierpaolo Palestri, and Luca Selmi, “On the Physical Understanding of the KT-layer Concept in Quasi-Ballistic Regime of Transport in Nanoscale Devices,” *IEEE Transactions On Electron Devices, vol. 53, no. 7, pp. 1634-1640, July 2006.*

[5] M. S. Lundstrom, “Elementary scattering theory of the si MOSFET,” *IEEE Electron Device letters, vol. 18, no. 7, pp. 361-363, Jul. 1997.*

[6] Marcel J. M. Pelgrom C. J. Duinmaijer, and Anton P. G. Welbers, “Matching Properties of MOS Transistors,” *IEEE Journal of Solid-State Circuits, vol. 24, no. 5, pp 1433-1440, October 1989.*

[7] Kadaba R. Lakshmikumar, Robert A. Hadaway, and Miles A. Copeland, "Characterization and Modeling of Mismatch in MOS Transistors for Precision Analog Design," *IEEE Journal of Solid-State Circuits, vol. sc-21, no. 6, pp. 1057-1066 ,December 1986.*

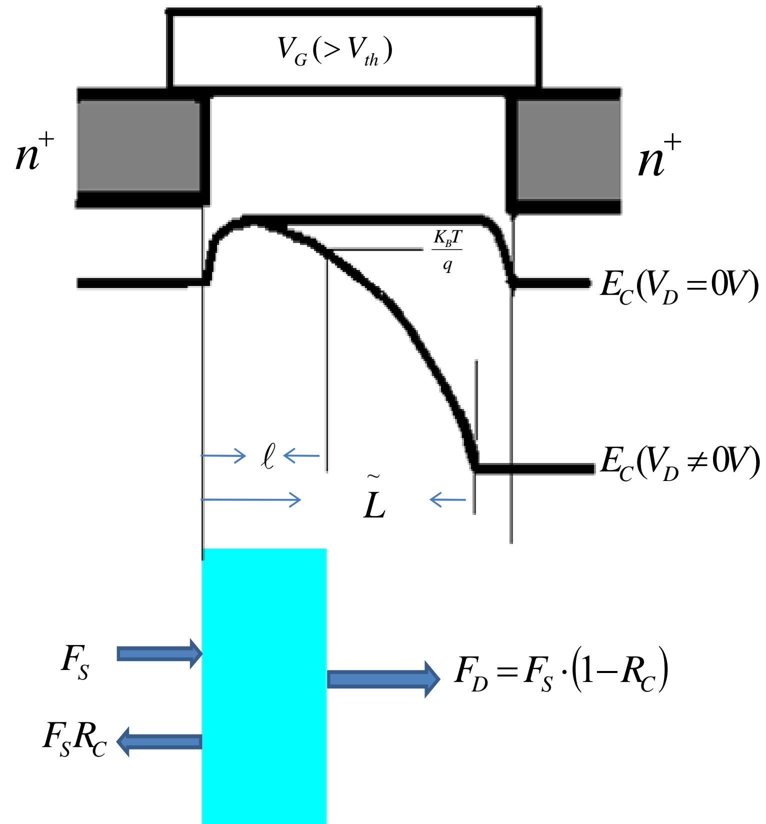
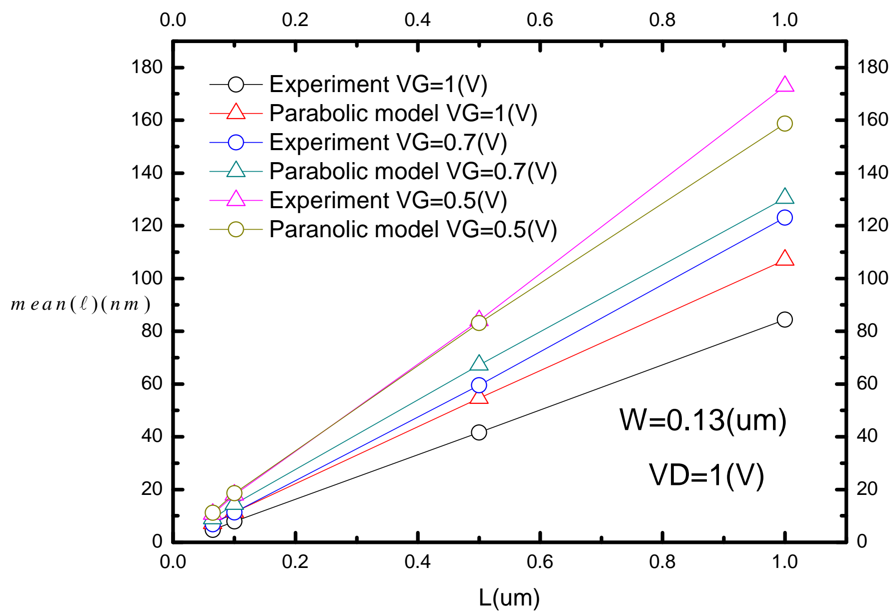
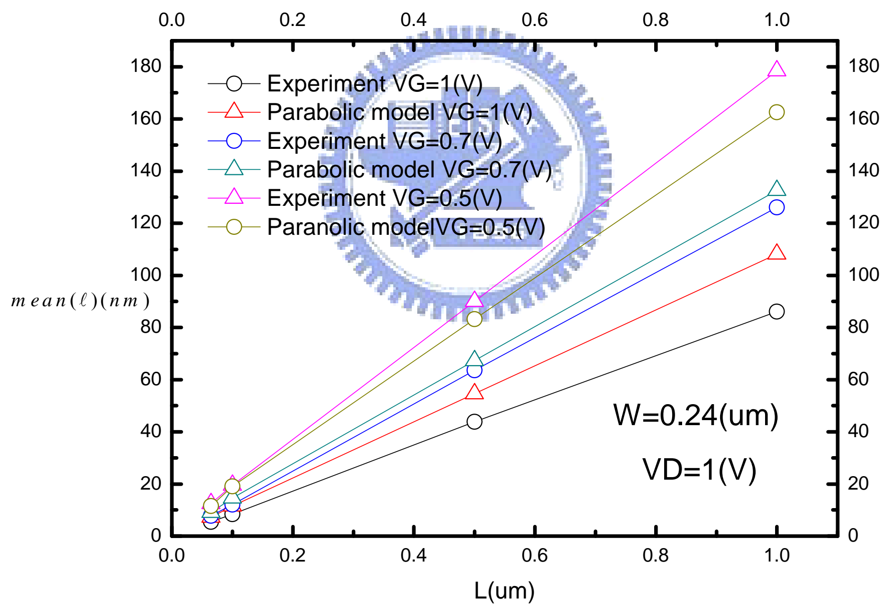


Fig.1





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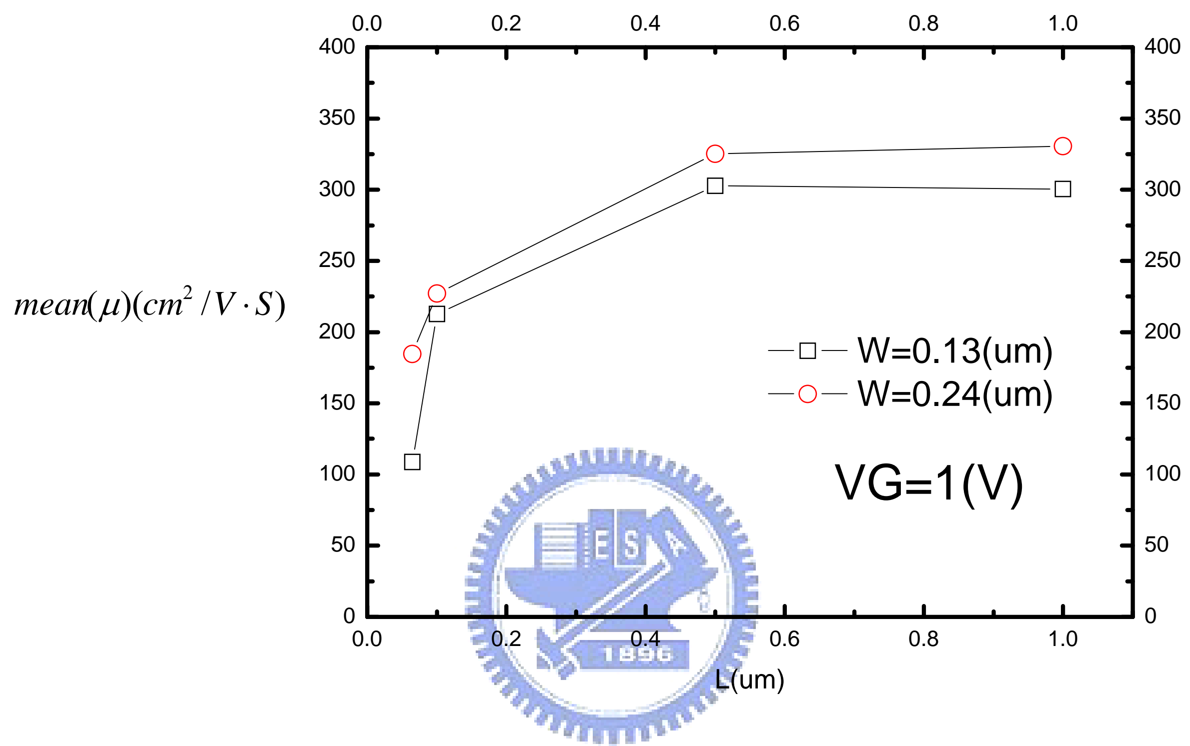

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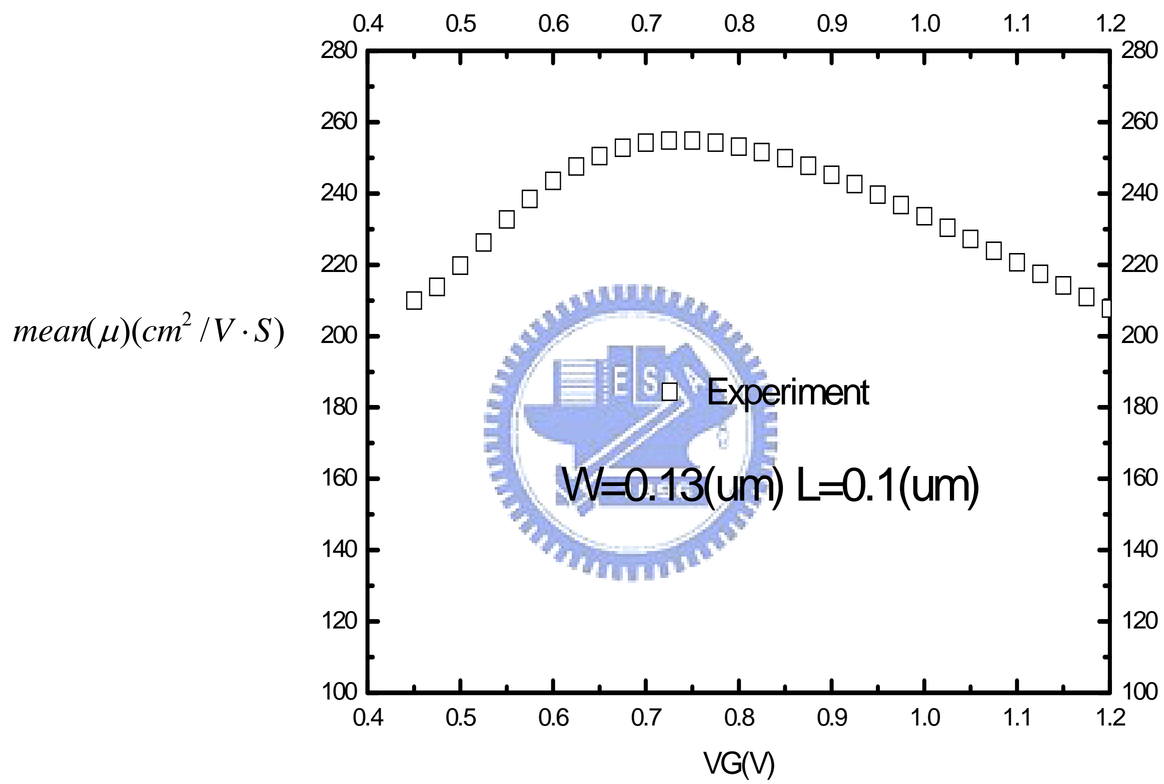

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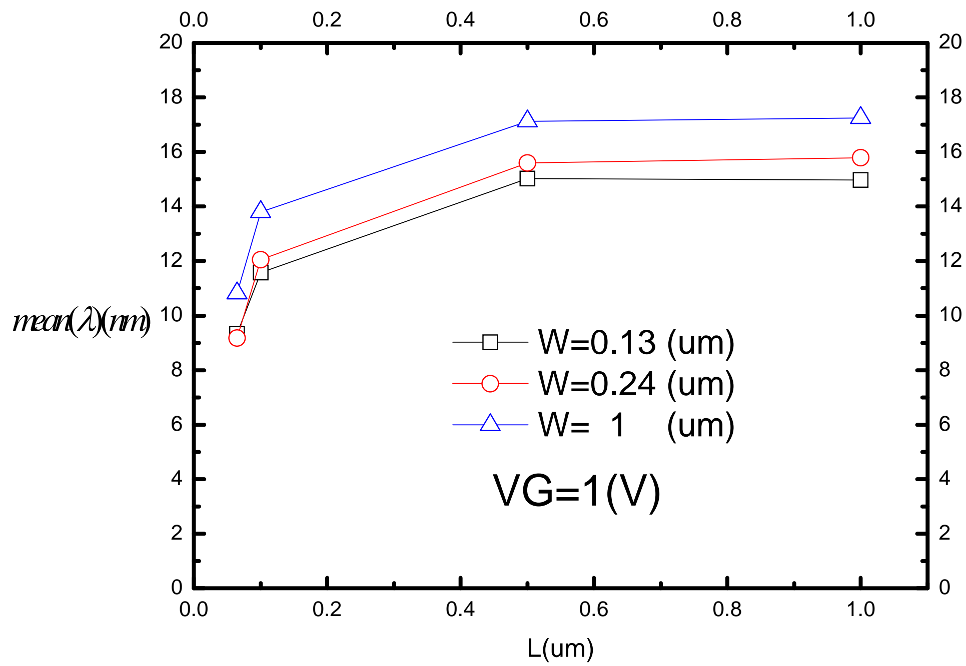

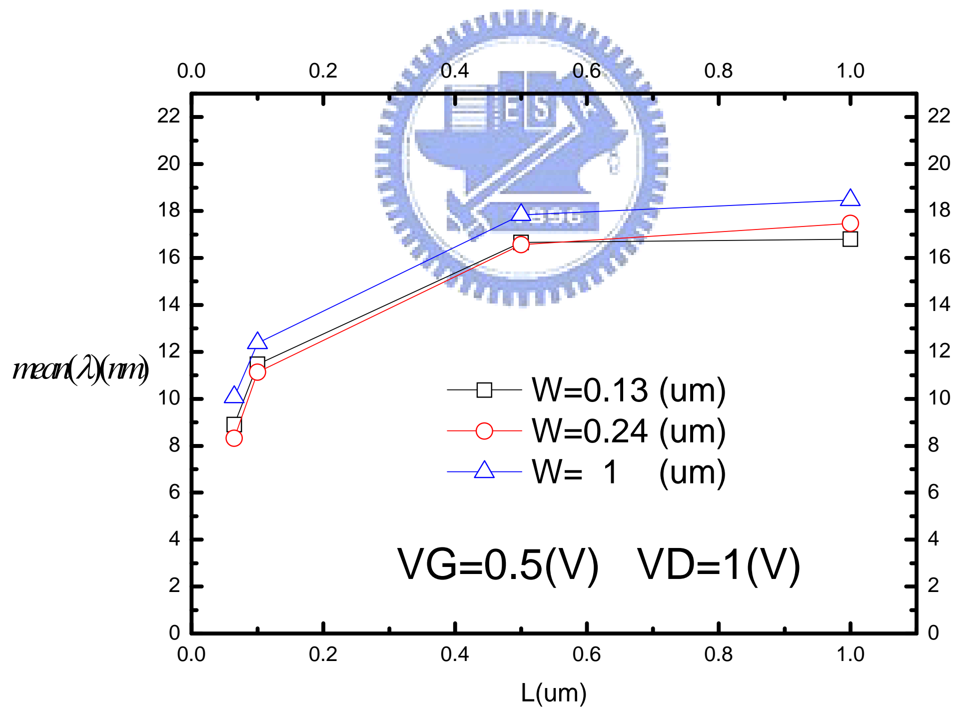

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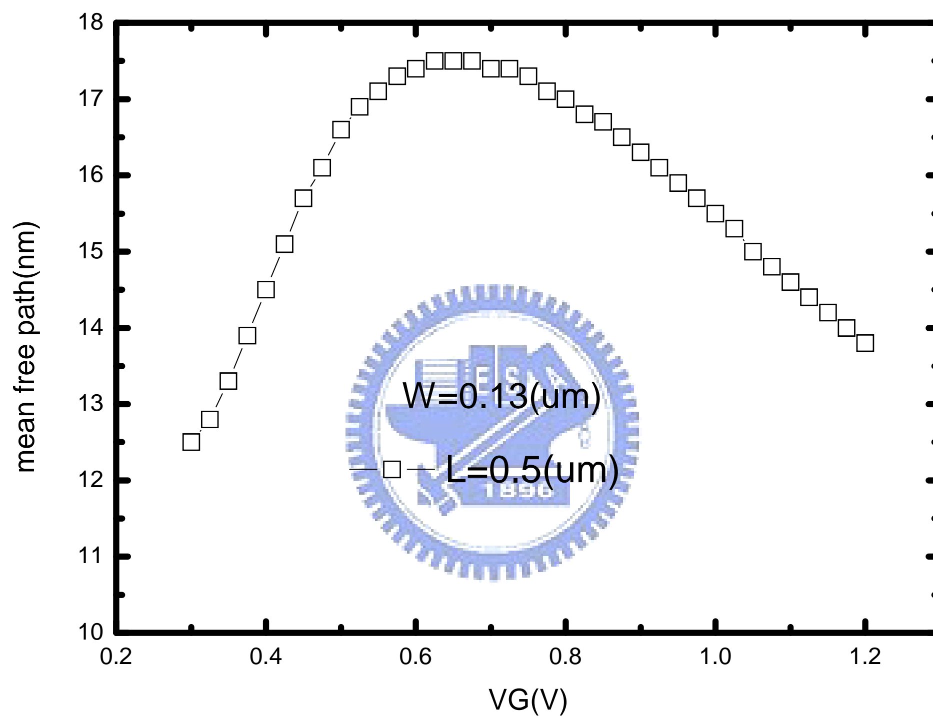

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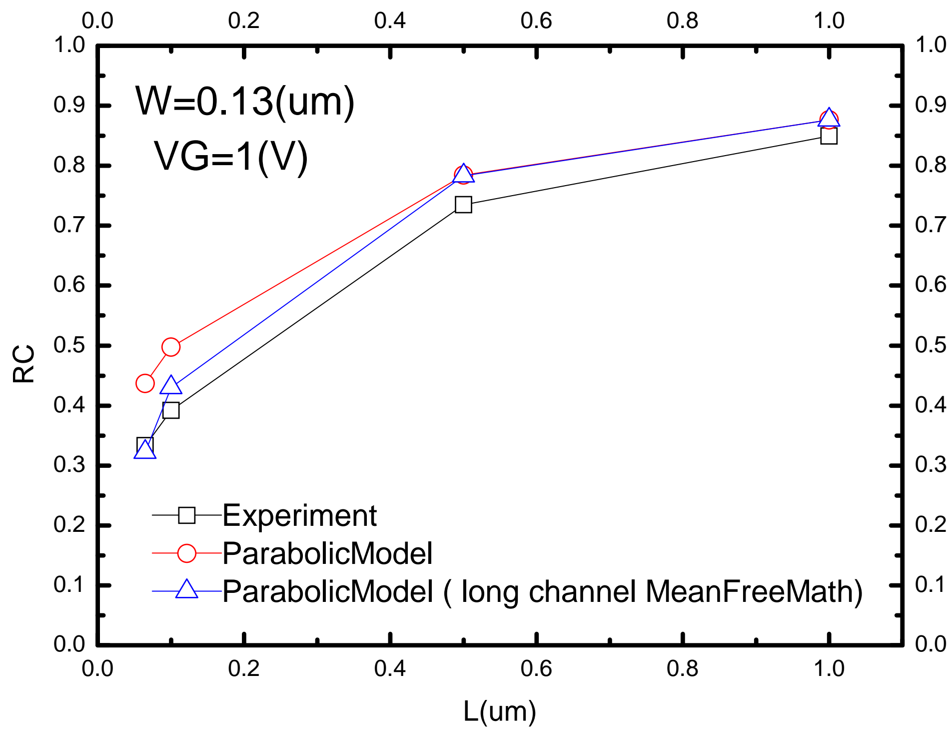

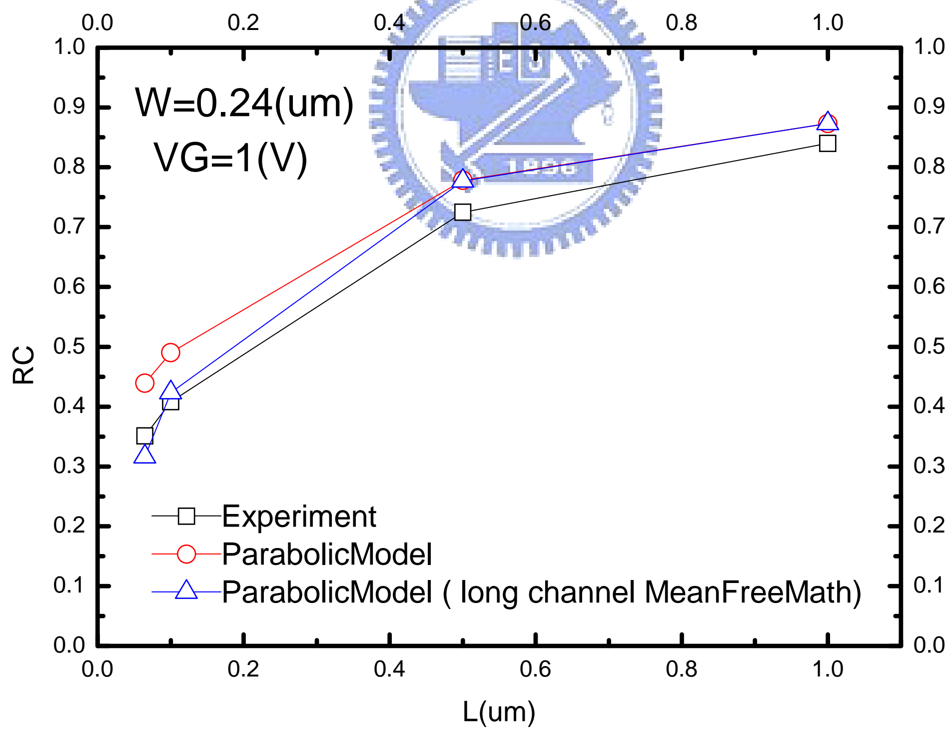

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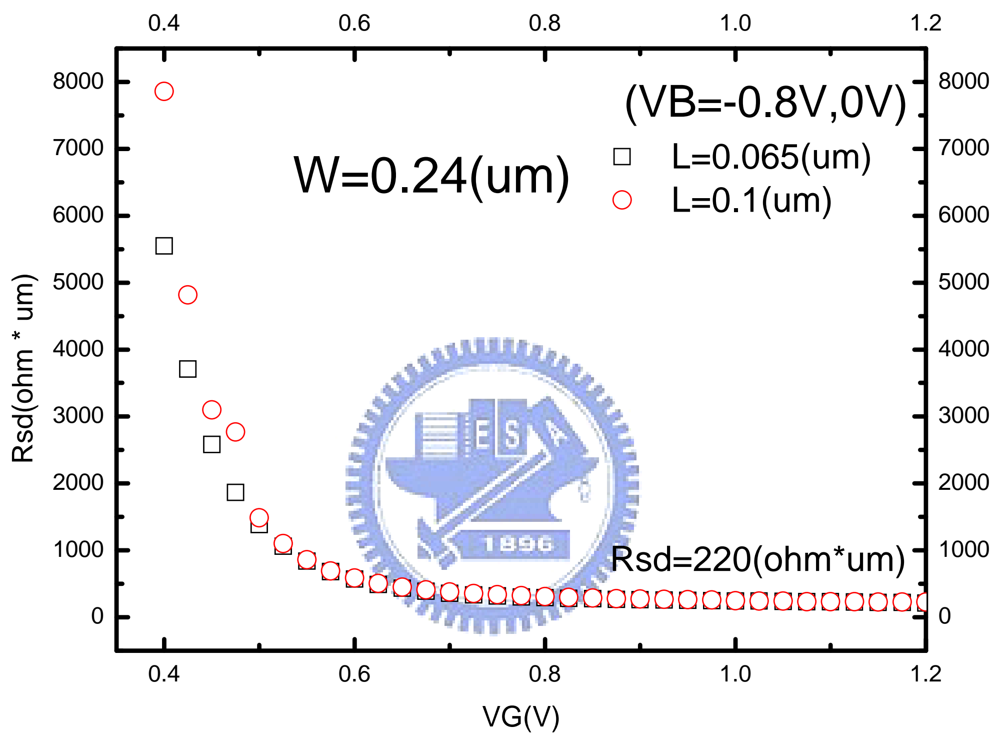

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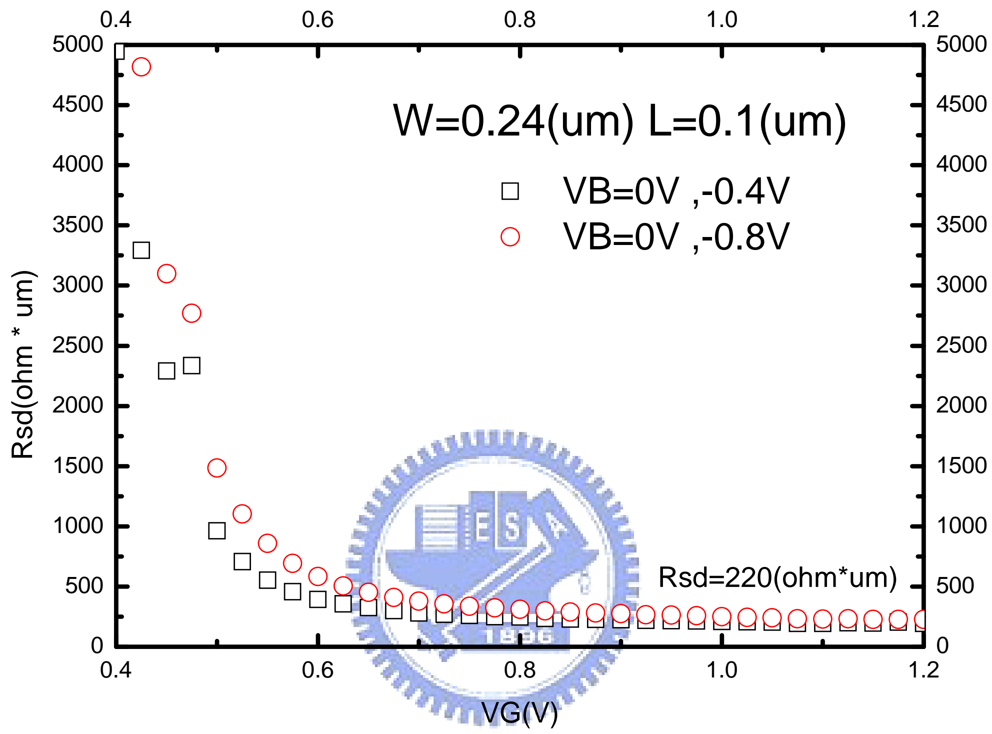

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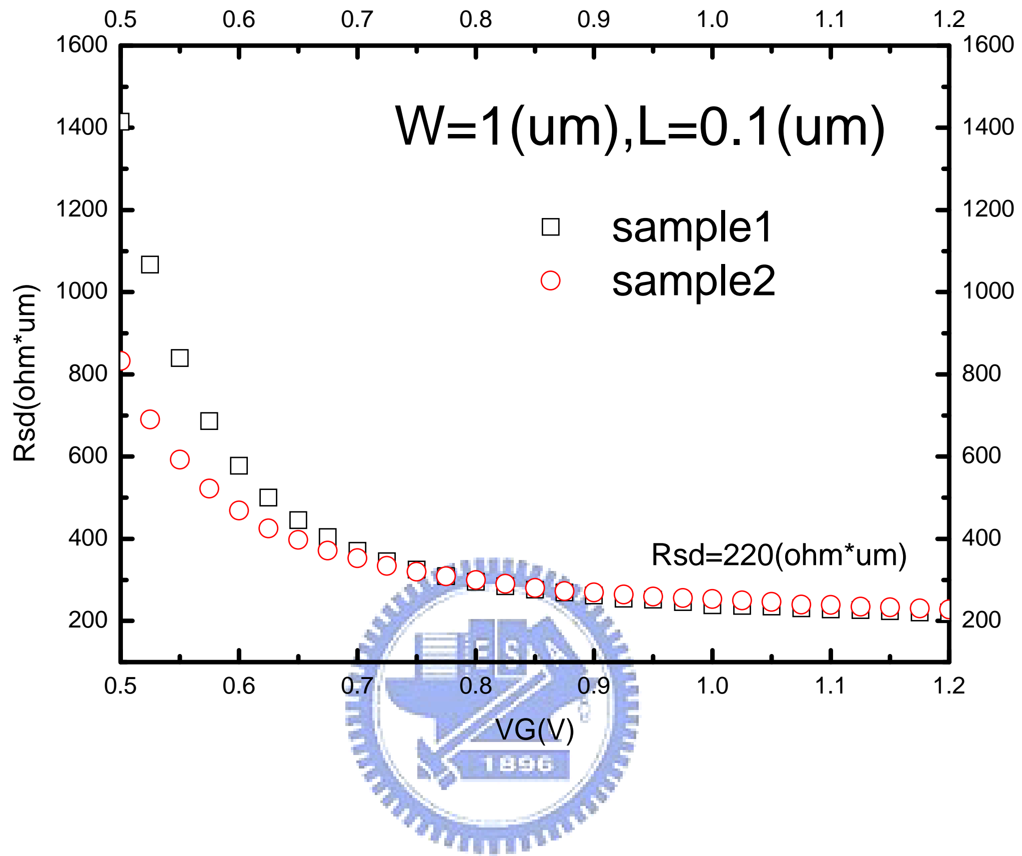


Fig.10

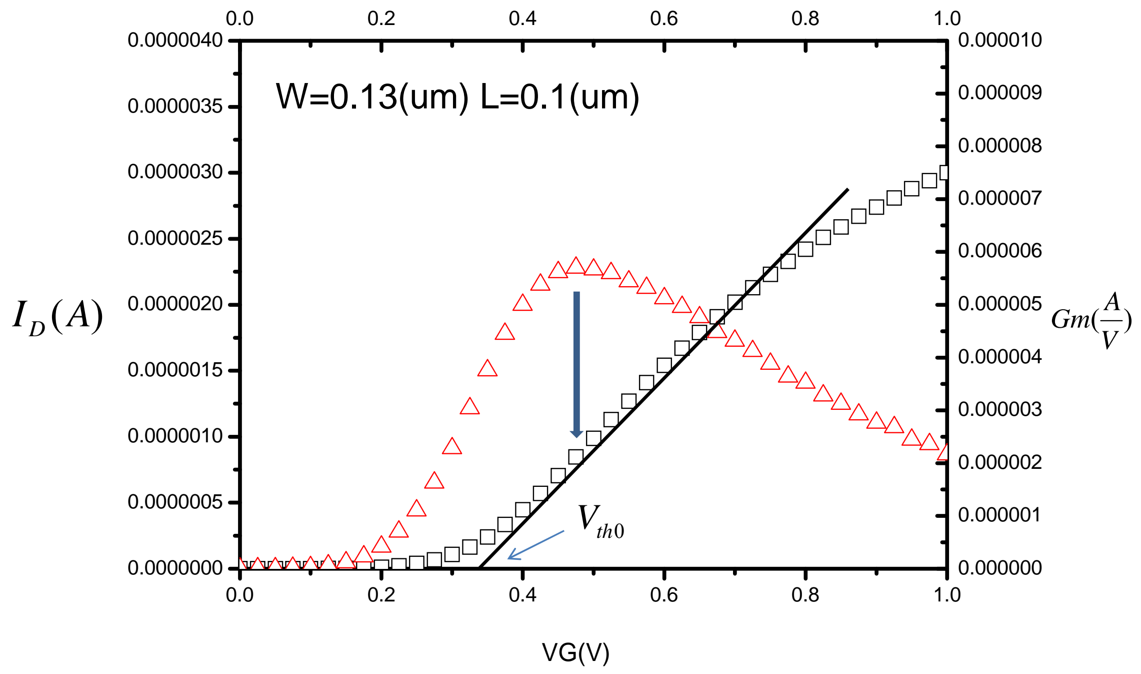


Fig.11

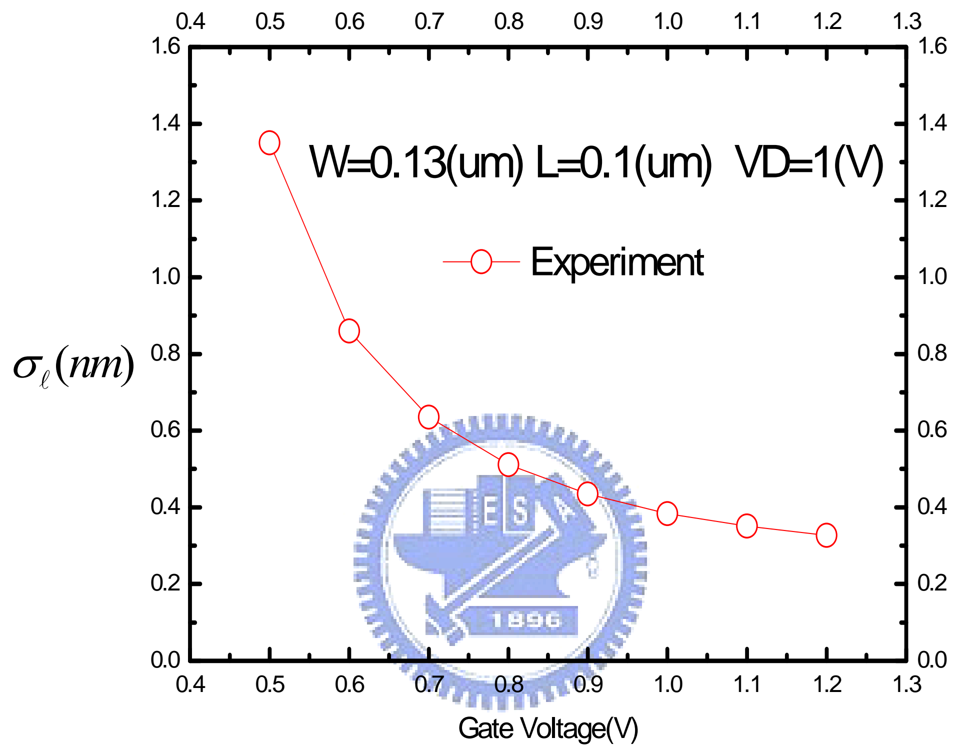


Fig.12

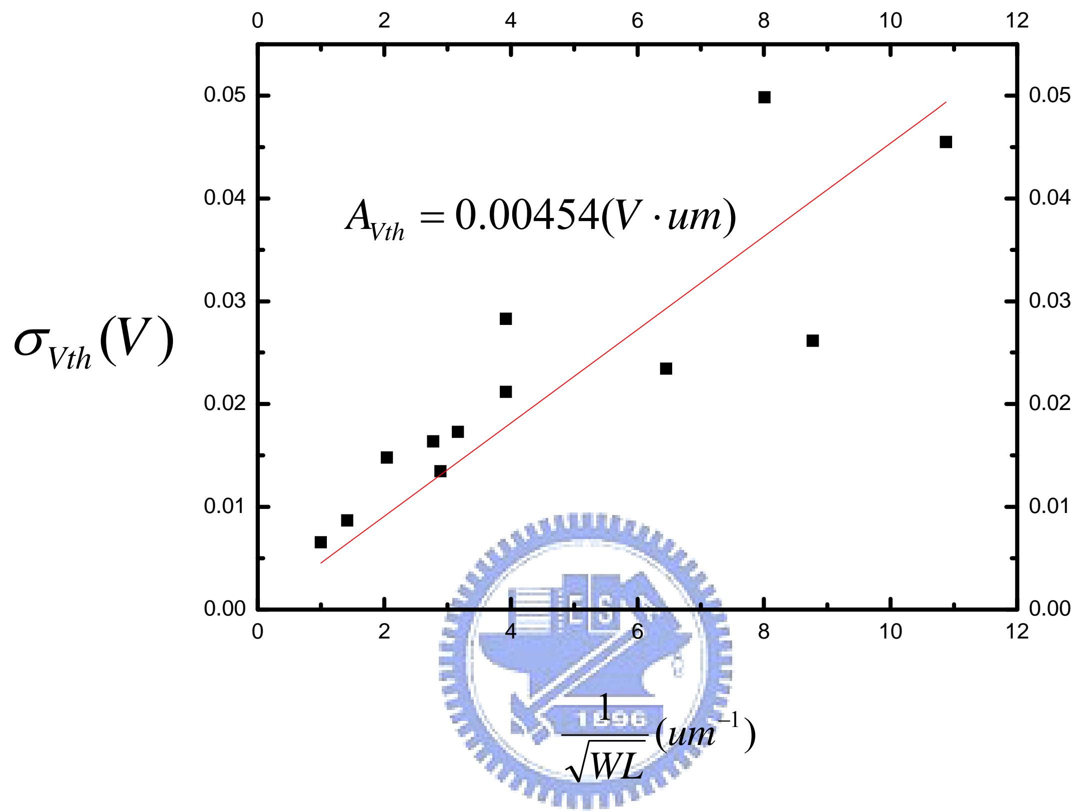
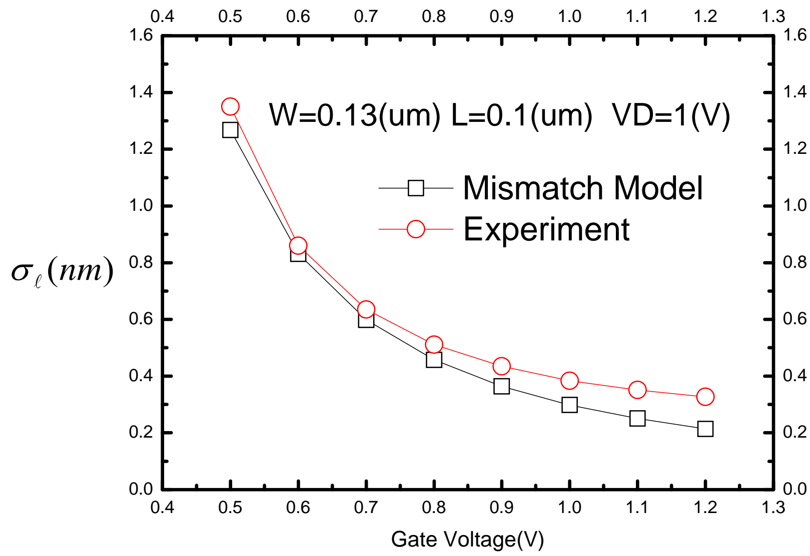
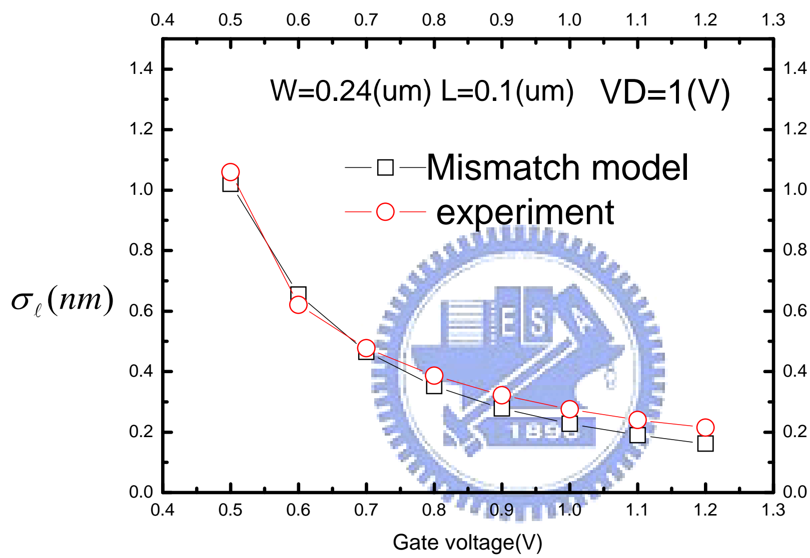


Fig.13





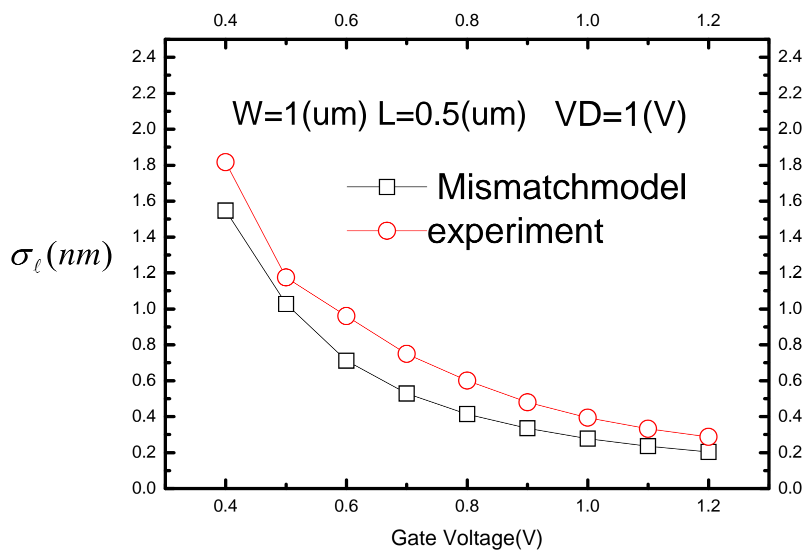


Fig.14

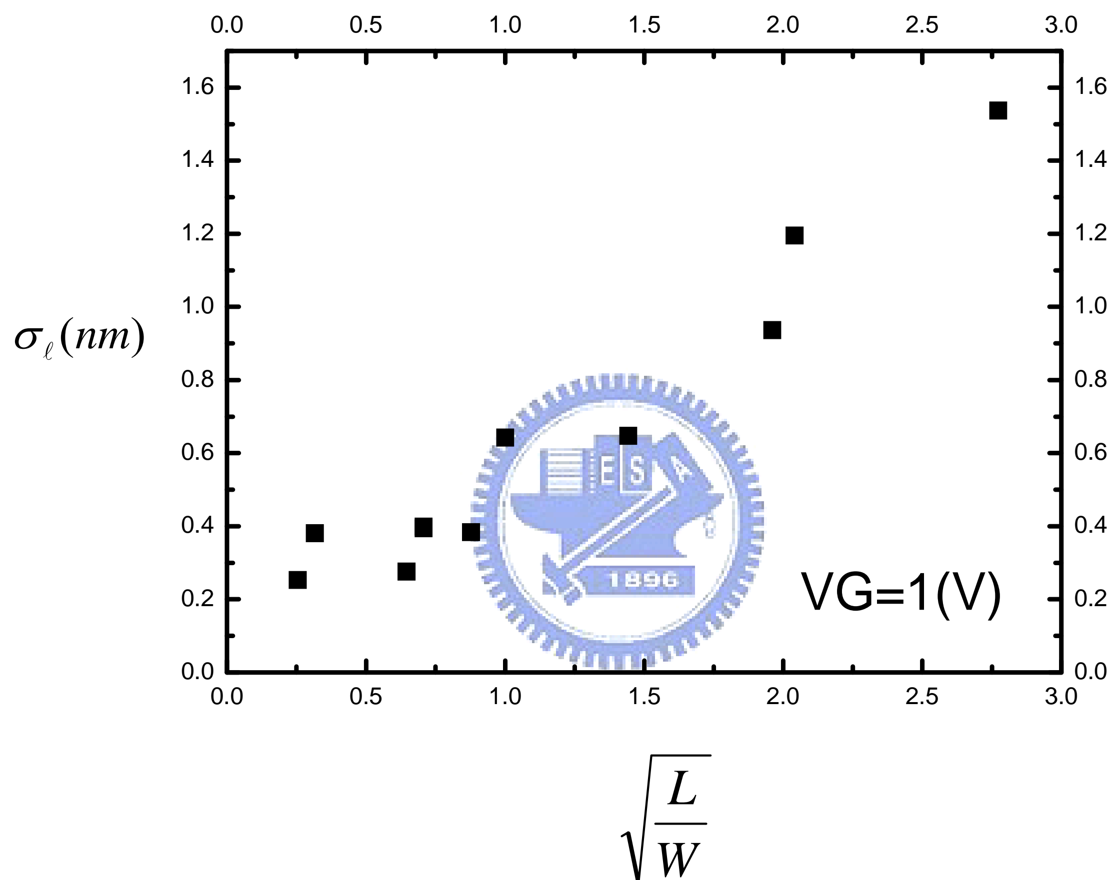


Fig.15

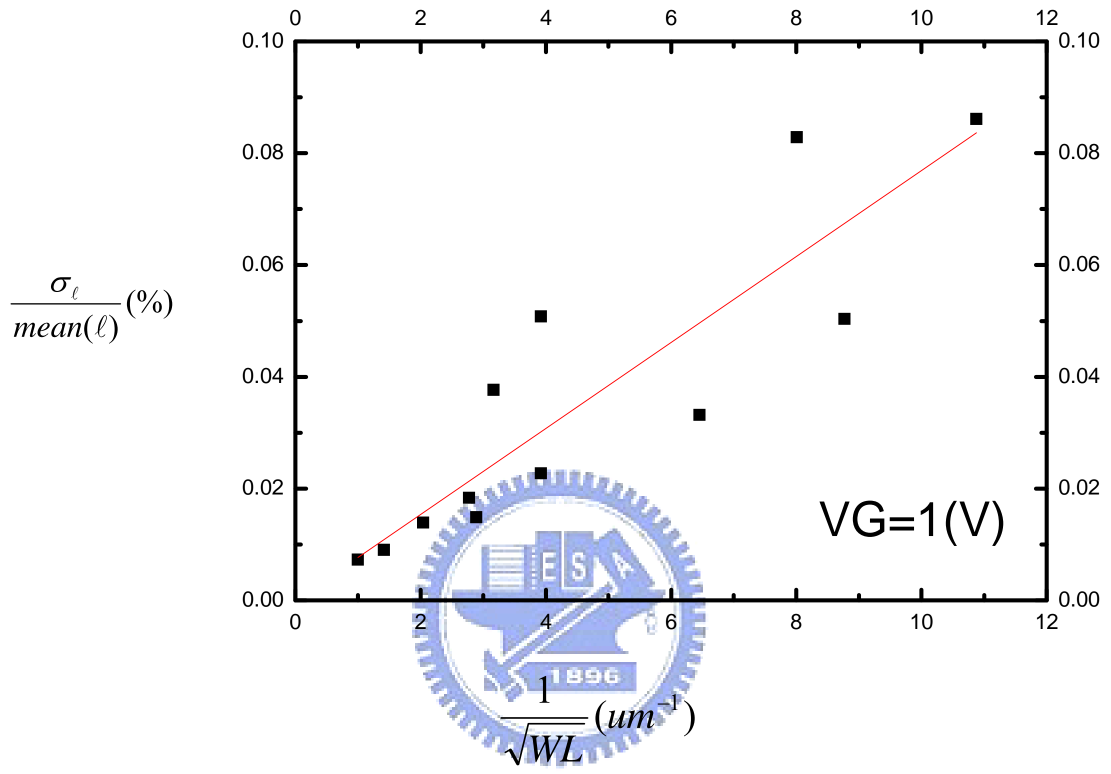


Fig.16

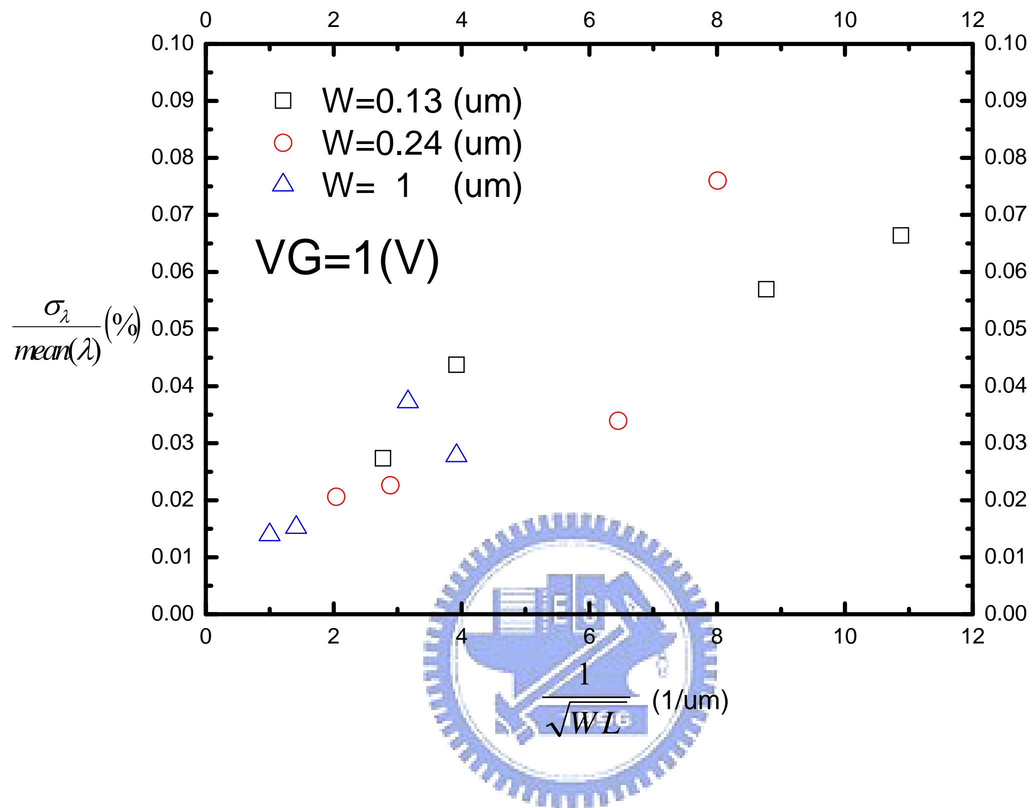
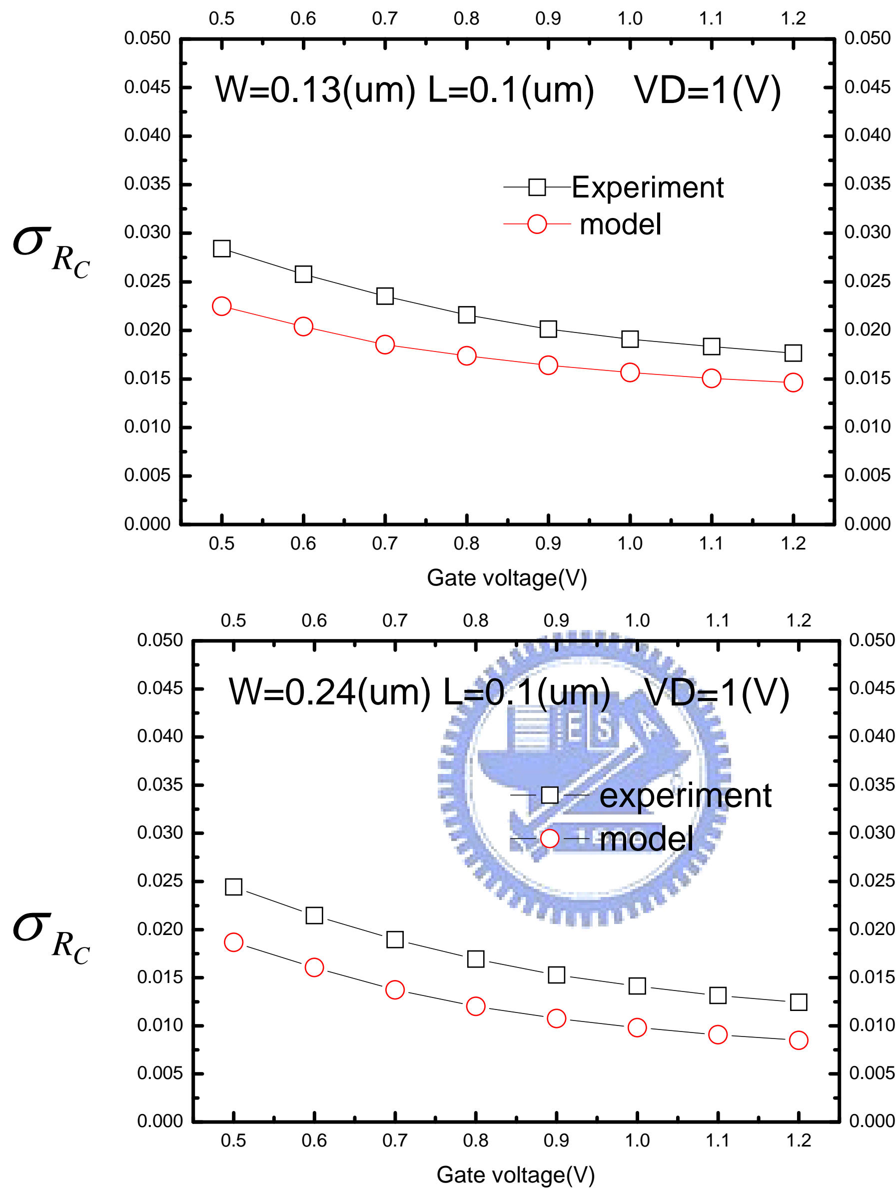


Fig.17



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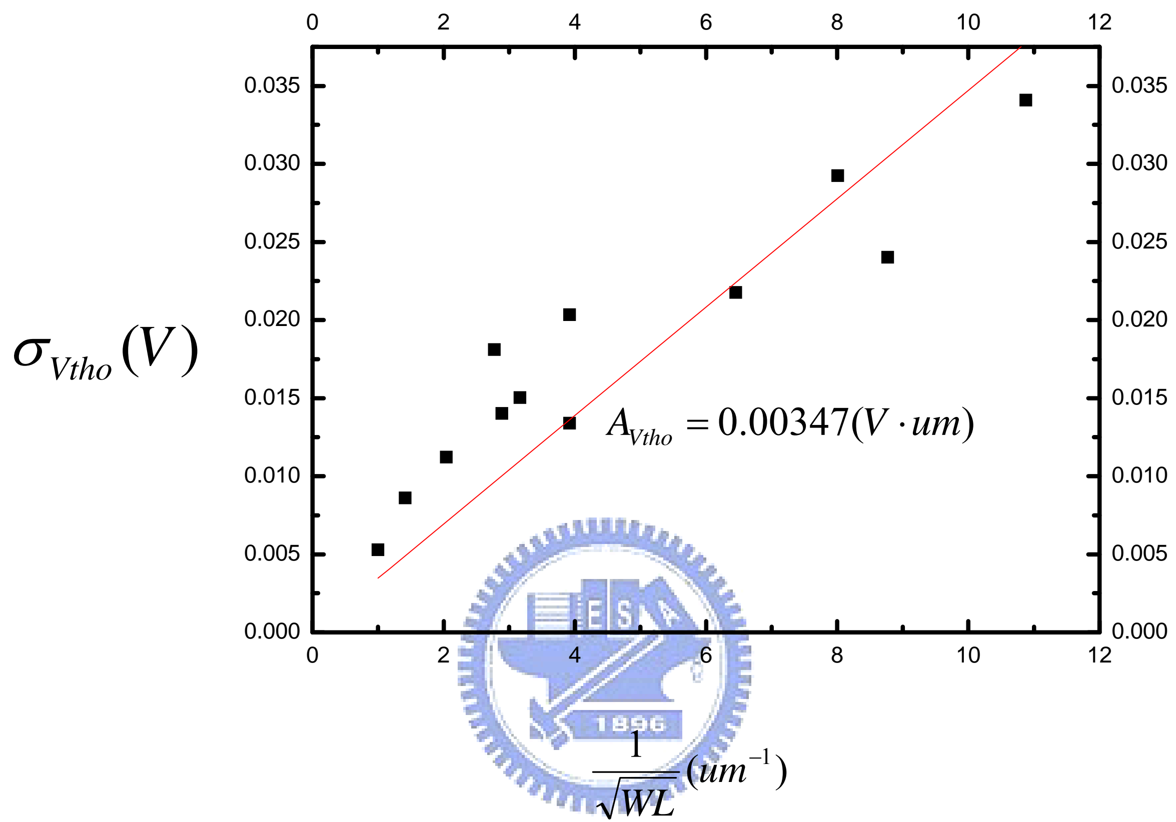

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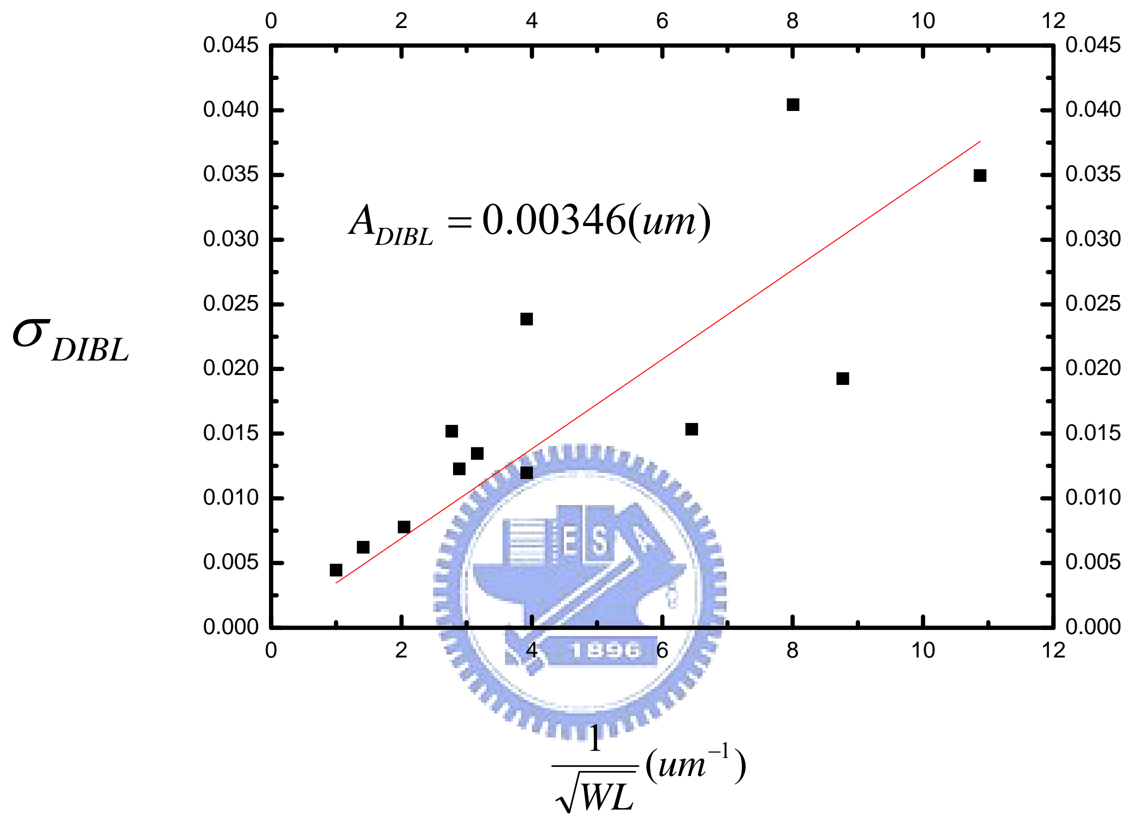
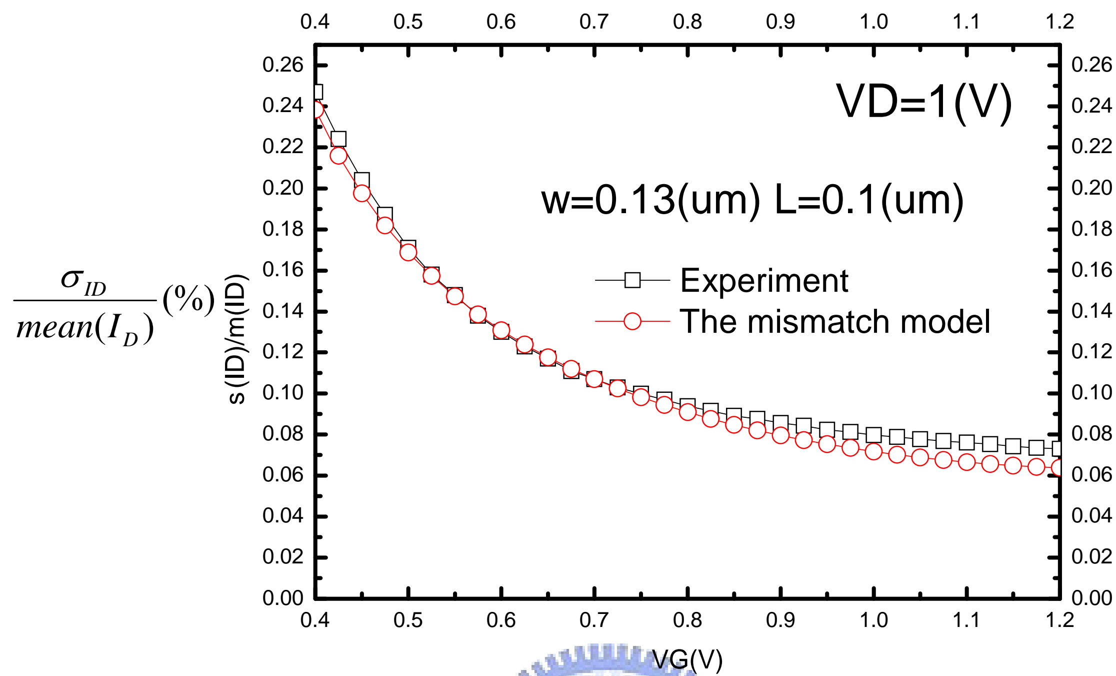


Fig.20



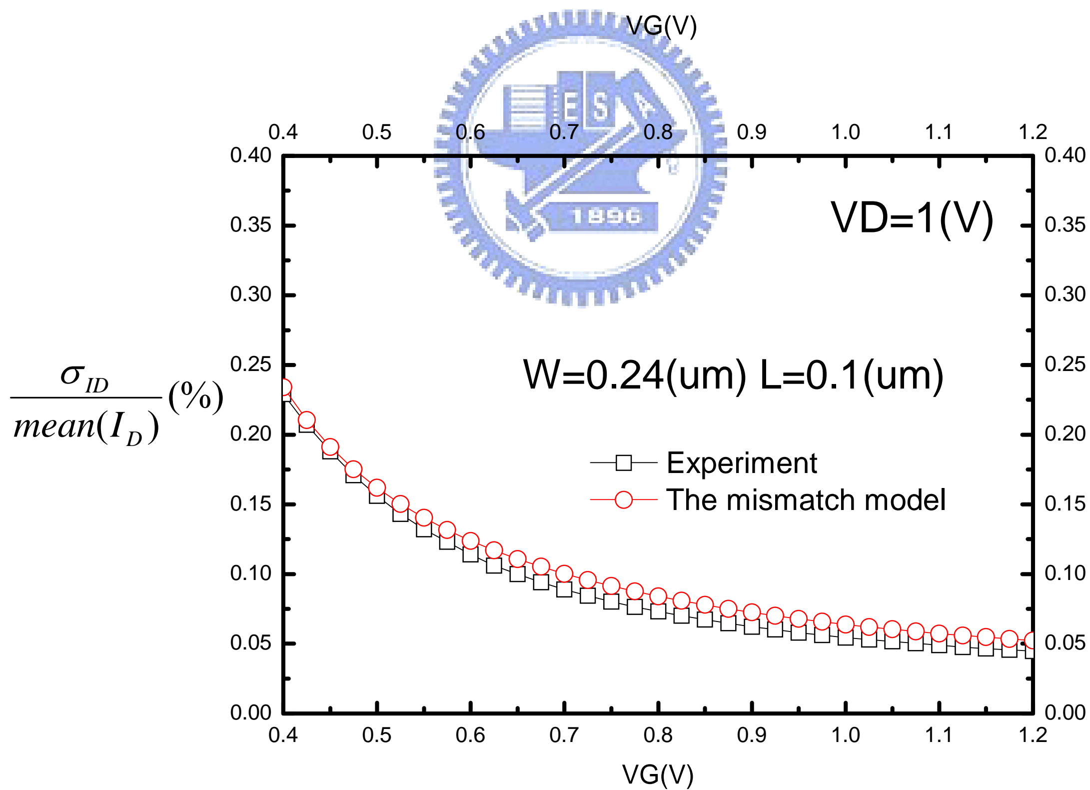


Fig.21