國 立 交 通 大 學

電子工程學系電子研究所

碩 士 論 文

使用完全矽化閘極-高介電常數介電質之低臨界電壓金氧半電晶體

A Low Threshold Voltage n-MOSFET Using Fully Silicided Gate and High-κ Dielectric

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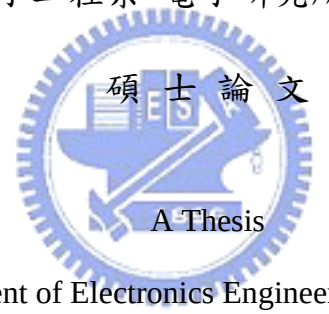

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摘要

為了降低傳統使用二氧化矽介電質的電晶體的漏電流，45 nm 節點的互補式金氧半電晶體技術必須要使用金屬閘極/高介電常數介電質。金屬閘極理想的有效功函數，對 n 型金氧半電晶體來說需接近矽的導帶。然而，金屬閘極/高介電常數介電質結構仍有許多重大挑戰，其中之一為費米能階釘扎所造成的高臨界電壓。為了降低臨界電壓，其中一個方法就是使用完全矽化閘極。

在本論文中，我們做出使用完全矽化的矽化鉿閘極/氮氧鑭鉿介電質的金氧半電晶體。從量測結果中，我們得到了 0.18 V 的低臨界電壓、215 cm^2/V-s 峰值電子遷移率以及 1.2 nm 的等效氧化層厚度，而且其漏電流比起相同等效氧化層厚度下的二氧化矽還小了約五個數量級。此外，閘極優先的製程和熱穩定性也使得矽化鉿閘極/氮氧鑭鉿介電質電晶體與現行超大型積體電路的製程相容。

A Low Threshold Voltage n-MOSFET Using Fully Silicided Gate and High−κ Dielectric

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Abstract

Metal-gate/high-κ is required for 45 node CMOS technology to reduce the intolerable leakage current of the conventional SiO_2-based CMOSFETs. The desirable effective work function of metal gate should be close to conduction band edge of Si (~4 eV) for nMOSFETs. However, one of the key challenges for metal-gate/high-κ is the large threshold voltage due to Fermi-level pinning effect. In order to reduce the threshold voltage, it is one of the solutions to use the fully silicided gate.

In this thesis, we have fabricated n-MOSFETs using fully sicilided (FUSI) $HfSi_x$ gate and $Hf_{0.7}La_{0.3}ON$ gate dielectrics. From the measurement, a low threshold voltage of 0.18 V and a peak electron mobility of 215 cm^2/V-s is obtained at 1.2 nm equivalent oxide thickness (EOT). Also, the leakage current is about 5 orders of magnitude lower than that of SiO_2 at the same EOT. In addition, the gate-first process and thermal stability of $HfSi_x/Hf_{0.7}La_{0.3}ON$ nMOSFETs make them compatible with current VLSI fabrication process.

致　　謝

首先，我要感謝我的指導老師荊鳳德教授，他在這兩年中的熱心指導及諄諄教誨，使我不僅在專業上有所精進，並得到了許多做人處事上的道理，在此表達我最由衷的感謝。

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最後我要感謝我的父親陳進長先生、母親蔡麗嬌女士，還有我的哥哥陳冠丞先生，由於你們的栽培、支持和鼓勵，我才能有今日的表現。

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Chapter 1

Introduction

1.1 Overview of high-κ dielectrics

The trend of silicon technology is to manufacture Complementally Metal-Oxide-Semiconductor Field-Effect Transistors (CMOSFETs) with higher density. According to Moore's Law of scaling, the number of devices on an integrated circuit doubles over a period of 2-3 year. However, the scaling of Moore's law cannot go forever. One of the most serious problems in CMOS is the "gate stack", which is the gate electrode and the gate dielectric layer.

When the thickness of SiO_2 layer is thinner than 2 nm, the gate leakage current due to the direct tunneling of electrons would be extremely high (Fig. 1-1) [1], which causes unacceptable power dissipation. In addition, the reliability issue resulting from low breakdown voltage in thin SiO_2 leads to a desire to replace SiO_2 as a gate oxide.

The direct tunneling depending strongly on film physical thickness can be expressed as:

$$J_{DT} \alpha \exp - \left[\sqrt{\frac{2mq\phi}{(h/2\pi)^2}} t_d \right] \tag{1.1}$$

Where t_d is the film physical thickness. Direct tunneling currents decrease exponentially with increasing physical thickness from this equation. A MOSFET is capacitance-operated device, where the drive current of the MOSFET depends on the gate capacitance density:

$$C_{ox} = \frac{\varepsilon_0 \kappa}{t_{ox}} \tag{1.2}$$

where ε_0 is the permittivity of free space, κ is the dielectric constant, t_{ox} is the oxide thickness. Therefore, the solution to reduce the tunneling current is to replace SiO_2 with a new material of higher dielectric constant. This will keep the same capacitance with thicker layer, which decreases the tunneling current. The new material is so-called "high-κ materials".

It is convenient to define an electrical thickness of the new gate material in terms of its equivalent oxide thickness (EOT) as:

$$EOT = \frac{\kappa_{SiO_2}}{\kappa_d} t_d \tag{1.3}$$

where κ_{SiO_2} is the dielectric constant of SiO_2. The parameters κ_d and T_{phys} are the dielectric constant and physical thickness of the gate insulator. The objective is to develop high-κ materials to allow scaling to continue to lower values of EOT.

Since the EOT target prescribed by the ITRS in 2008 is only 0.9 nm for 22nm CMOS (Fig. 1-2) [2], the use of high-κ materials is evitable for reducing the leakage current. Many materials are currently under consideration to replace SiO_2 as the gate dielectric material for 45 nm node CMOS technology. The requirements to select a suitable high-κ dielectric include:

- Moderate κ value: The preferred κ value should be 25-30. There is a trade off with the band gap. Fig. 1-3 shows the κ value varies inversely with the band gap [3]. Thus, materials with extremely large κ value would have a too low band gap, which gives rise

to a too low band offset. In addition, a very large κ is not suitable due to the fringing-induced barrier lowering (FIBL) effect, which causes undesirable large fringing fields at the source and drain junctions [4].

- Band offsets with Si of over 1 eV to minimize carrier injection: High-κ materials should act as a barrier to both electrons and holes. This requires that both their valence and conduction band offsets to Si must be over 1 eV to prohibit conduction by the Schottky emission of electrons or holes. Fig. 1-4 surmises the band offsets of some popular gate dielectric candidates. From the Fig. 1-4, the oxides that satisfy the requirement are Al_2O_3, ZrO_2, HfO_2, Y_2O_3, La_2O_3, and $ZrSiO_4$.
- Thermal stability on Si when in direct contact with the Si channel: Most high-κ dielectrics are thermally unstable on Si: that is, they react with Si under equilibrium conditions to form a SiO_2 or silicate layer at the interface. The interfacial layer would increase the EOT and negate the effect of using high-κ materials. By the condition, the choices of high-κ dielectrics are restricted to very few oxides, such as SrO, Al_2O_3, ZrO_2, HfO_2, Y_2O_3 and La_2O_3 [5].
- Remaining amorphous structure after high temperature process: The gate dielectric must withstand the high temperature process, a rapid thermal annealing (RTA) at 1000^{o}C, 5s. Most metal oxides will crystallize at this temperature, unlike SiO_2. In particular, ZrO_2 and HfO_2 crystallize at mush lower temperature; Al_2O_3 is amorphous after the RTA but

has a low κ value; Ta_2O_5 is also amorphous but is reactive with Si [6]. The crystalline oxide offers a path for leakage current and undesired dopants. It also causes device-to-device variations in leakage, threshold voltage, etc. The incorporation of Si [7] and Al [8] has been proved to prevent the crystallization problem. However, the κ value will decrease as the extent of the incorporation increase. The addition of nitrogen has been found to be beneficial to hafnium silicates to further raise the crystallization temperature [9-11].

- Good interface with Si to retain high mobility: The carrier in the channel is near the dielectric/Si interface, so the interface must keep high quality, in terms of roughness and the absence of interface defects.
- Few defects: The electrically active defects which give rise to energy states in the band gap of oxides are sites of excess or vacancies of oxygen or impurities. These defects might be the starting point of breakdown and cause the device failure. Charge trapped in defects would shift the threshold voltage. The trapped charge changing with time causes the threshold voltage also shift with time. In addition, trapped charge scattering carriers in the channel would lower the mobility [6].

1.2 Overview of Metal gates

Metal gates such as Al were a mainstream of CMOS technology for many years until the need for denser circuits brought about the end of Al gates and the beginning of poly-silicon gate electrodes afforded by self-aligned approach. Today, a transition from the poly-silicon to metal gates is inevitable in high performance devices. Such gate electrodes include many merits of:

- No boron penetration: Boron from the poly-silicon gate penetrating to channels through very thin gate dielectric becomes a severe problem, because the high carrier activation in poly-silicon is required to avoid the gate depletion, which causes a positive flat-band voltage (V_{FB}) shift [12].
- Much lower gate resistance: Gate resistance-capacitance (RC) delay becomes a significant concern in designing circuits with very short gates. The low resistivity of metal gates compared to poly-silicon shows the potential to reduce the RC delay.
- No gate depletion length: As shown in Fig. 1-5, the capacitance equivalent thickness (CET) can be defined as:

$$CET = EOT + t_{gate} + t_{Si} \tag{1-4}$$

where t_{gate} is the gate depletion depth and t_{Si} arises from quantum delocalization. t_{Si} is intrinsic and cannot easily be removed. On the other hand, t_{gate} (normally 3-5 Å) from the gate depletion can be removed by replacing the poly-silicon with a normal

metal.

Metal electrodes with suitable work functions and sufficient physical and electrical stability are being investigated. According to ITRS (Fig. 1), it can be found that the saturation threshold voltage should be below 0.1 V in 2008. In order to achieve this goal, the preferred work functions should be close to Si conduction band (4.0 eV) for n-MOSFET and Si valance band (5.1 eV) for p-MOSFET to control the threshold voltage. The dependence of the work-function on atomic number is shown in Fig. 1-6 [13] to guide the choice of proper metals. Possible candidates for n-MOSFET are group-IA, group-IIA and Lanthanide elements. The metals in column IA and IIA cannot be used for metal gates because they are very reactive. For p-MOSFET, only Ir (5.27 eV) and Pt (5.65 eV) in the Periodic Table have work function over the desired 5.2 eV. However, Pt is difficult to etch by reactive ion etching (RIE) [14] and Ir will penetrate through the gate dielectric at temperature more than 800^{o}C [15].

Another notable issue for metal gates is that they might react with the gate dielectric at high temperature. This would shift the effective work function towards mid-gap [Fermi thermal]. The solution is to use metal compounds with high thermal stability. TiN [16], TaC [17], and MoO_x [18] are all stable enough and investigated widely. Metal alloy systems such as Ni-Ti [19], Ru-Mo [20] are also under consideration. The work function of these alloys can be tuned by changing compositions or employing N, C incorporation.

Metal gates can be realized by two integration schemes: gate-first and gate-last. The

former method is compatible with current poly-silicon gate process flow. Its main disadvantages are [21]: (1) Contamination of front-end tools during processing, (2) Difficult metal etching, and (3) Integrity of gate stack during high-temperature annealing. The gate-last approach is also called a replacement gate technique, where a dummy gate is removed after all doping and high-temperature processes are completed. Its main challenge is the dummy gate stack removal and replacement [21].

Several kinds of gate stack have been developed to realize high-performance CMOS with band-edge work functions for NMOS and PMOS:

- Two-metal/one-dielectric: Two different metals with band edge work functions (conduction band edge and valance band edge work functions for NMOS and PMOS, respectively) on the same dielectric.
- One-metal/two-dielectric: One metal with conduction band edge work function on the dielectric for NMOS (PMOS), and dielectric with surface modification for PMOS (NMOS).
- Two- metal/two-dielectric: Two different metals on two different dielectrics.
- FUSI gate: Two FUSI gate with different phases and /or segregated dopants on the same dielectric.

1.3 Overview of fully-silicided (FUSI) gates

Fully silicided metal gates have received increasing attention in recent years due to the simple integration scheme for implementation and ease of passivation of the underlying gate dielectric. Over the past several years, devices with nickel silicide [22], hafnium silicide [23], platinum silicide [24], and titanium silicide gates [25] were reported.

Nickel silicide gates have drawn a lot of attention in recent years due to its mid gap work function, which is necessary to tailor the process to obtain dual work function. It has been shown that the presence of dopants (such as As, P, and B) in poly-silicon can modulate the work function of NiSi gate upon full silicidation. On full consumption of poly-silicon by silicidation, a thin and highly concentrated layer was formed between the metal silicide and gate dielectric. This dopant-rich film at the interface between gate dielectric and metal silicide layer modulates the work function in FUSI gates. The ability to form a pileup of dopant at the silicide/dielectric interface and hence to modulate work function appears to be strongly related to the silicidation conditions. It has been reported that the silicidation temperature and the ratio of Si and Ni thickness determine the phase of the FUSI gate. A two-step RTA FUSI experiment with varying Si:Ni and the temperature of the first step shows formation of different phases of the Ni-Si system. Ni-rich phase does not result in dopant pileup at the Ni_3Si_2/SiO_2 interface. Electrical data corroborates this finding, indicating that phosphorous- or arsenic-doped NMOS and boron-doped PMOS FUSI gates all resulted in the same work

function of ~ 4.65 eV. This likely represents the work function of Ni_3Si_2 [21].

It has been observed that higher dopant doses give rise to a larger amount of work function shift [26]. This is accompanied by higher amounts of dopant accumulated at the interface between silicide and dielectric [26]. The actual amount and type of dopant accumulated at the silicide/dielectric interface and the phase of the silicide in its immediate vicinity are responsible for setting the work function, while actual experimental conditions, such as dopant dose, energy of implantation, poly-silicon thickness and pre-silicidation annealing might differ. It was observed that the total amount of work function shift saturates at a certain amount of dopant dose. The saturated values of work function shift appear to relate proportionally to the size of the atomic specie of the dopant, the bigger the atom is the larger work function shift attainable [26].

FUSI devices are fabricated using a self-aligned process with independent silicidation of source/drain and the poly-Si gate to avoid thick silicidation in the S/D areas. Fig. 1-7 illustrates the whole process flow. Unlike the common replacement gate approach used for metal gates, this approach retains original dielectric and electrode and only modifies the latter. An alternative and simpler approach to siliciding the gate and source/drain at the same time would require the poly-silicon gate to be substantially thinner than source/drain junction depth, a condition difficult to realize if poly-silicon implantation doping is required.

1.4 Fermi-level pinning effect

According to the Schottky model, the band alignment is determined solely by the difference between the work function of the metal in vacuum and the electron affinity of Si. However, when a metal is deposited on a dielectric, a lot of energy states form at the interface between the metal and the dielectric. The states in the forbidden band gap of the dielectric are known as metal-induced gap states [27]. They are mainly donor-like from charge neutrality level (E_{CNL}) to E_V and acceptor-like from E_{CNL} to E_V. The acceptor-like state is neutral when empty and negatively charged when full of electrons, while the donor-like state is neutral when full of electrons and positively charged when empty. Charging of these interface states creates a dipole that tends to drive the band lineup toward a position that would give a zero dipole charge. Hence, the effective work function ($\phi_{m,eff}$) is different from the work function in vacuum ($\phi_{m,vac}$). Fig. 1-8 illustrates the dipole with negative charge on the dielectric side [28]. The work function change is proportional to the difference between $\phi_{m,vac}$ and $\phi_{CNL,d}$ $[=(E_{vac}-E_{CNl,d})/q]$. Thus, $\phi_{m,eff}$ can be expressed as

$$\phi_{m,eff} = \phi_{CNL,d} + S(\phi_{m,vac} - \phi_{CNL,d}) \tag{1.4}$$

S and $\phi_{CNL,d}$ can be extracted from the experimental $\phi_{m,eff} - \phi_{m,vac}$ plot. When $S \rightarrow 0$, it means the Fermi level is pinned by charge neutrality level. In contrast, when $S \rightarrow 1$, it returns to the ideal Schottky case. Typically, the smaller S means the larger Fermi-level pinning [28].

1.5 Motivation to use the HfLaON film

Hf-based high-κ dielectrics have been recognized as the most promising candidates due to their moderate dielectric constant (~20-25), large energy band gap (5.7 eV), high conduction band offset (1.5 eV), excellent thermal stability on the Si substrate [5, 29, 30]. Hence, Hf-based high-κ dielectrics have been the most popular candidates in recent years, as shown in Fig. 1-7 [31]. However, HfO_2 do undergo substantial changes during thermal processing. Dopant activation requires annealing to temperatures of 1000^{o}C or more, much higher than crystallization temperatures of HfO_2. The grain boundaries induced by crystallization offer a path for gate leakage current or other undesired dopants to diffuse into gate dielectrics.

Several studies have focused on the improvement of the thermal stability of Hf-based dielectrics during the subsequent thermal process. Those studies incorporated Al [8], Si [7], N [9-11] and Ta [32] into HfO_2 to form HfO_2-based dielectrics, respectively. The incorporation of these elements have been known to retard crystallization of HfO_2, but the dielectric constant Si are degraded as the extent of incorporation increases. In addition, the Fermi-level pinning between the metal gate and HfO_2 makes it difficult to obtain a CMOS with low threshold voltage [33].

In this thesis, HfLaON is used for the gate dielectrics in the $HfSi_x/Hf_{0.7}La_{0.3}ON/Si$ n-MOSFET structure. The incorporation of La has been shown to preserve Hf-based dielectric

from crystallization after 1000 ◦C RTA, similar to the incorporation of Si. The HfO_2 with La also improves significantly the electrical performances of NMOS in terms of drive current with no gate leakage degradation compared to pure HfO_2 gate dielectric [34]. Additionally, it has been found that the changing La composition in HfO_2 films can effectively tune the work function of the metal gates continuously from Si mid-gap to around 4 eV, which can fit the requirement of NMOS [34]. Therefore, it is worth further studying on the electrical and material characterization of HfLaON.

1.6 Motivation to use FUSI $HfSi_x$ gates

In this thesis, FUSI $HfSi_x$ is used for the gate in the $HfSi_x/Hf_{0.7}La_{0.3}ON/Si$ n-MOSFET structure. Hf has a very low work function of about 4.0 eV and its silicide has an excellent thermal stability up to 950°C [23]. FUSI HfSi gate also shows a low work function value, which is suitable for gate electrode application [23]. Therefore, FUSI $HfSi_x$ is a promising candidate for dual-metal CMOS process.

1.7 Thesis organization

In this thesis, we used FUSI $HfSi_x$ as metal gate and $Hf_{0.7}La_{0.3}ON$ as gate dielectric for n-MOSFETs.

In chapter 1, a brief review of high-κ/metal gate technology was given to describe their

application in CMOSFETs. It also shows the motivation to use FUSI $HfSi_x$ metal gate and $Hf_{0.7}La_{0.3}ON$ dielectrics.

In chapter 2, the detailed fabrication process of $HfSi_x/Hf_{0.7}La_{0.3}ON$ n-MOSFETs and measurement procedure will be described.

In chapter 3, the device parameter extraction will be discussed first. Chapter 3.2 and 3.3 shows the results from the measurement and the detailed discussion of characteristics of $HfSi_x/Hf_{0.7}La_{0.3}ON$ capacitors and n-MOSFETs. From the measurement, low EOT, low effective work function, low threshold voltage, low leakage current and high electron mobility were extracted. It also shows the comparison with other reported n-MOSFETs.

Chapter 4 summarizes the findings in this thesis and provides the suggested directions of future studies.

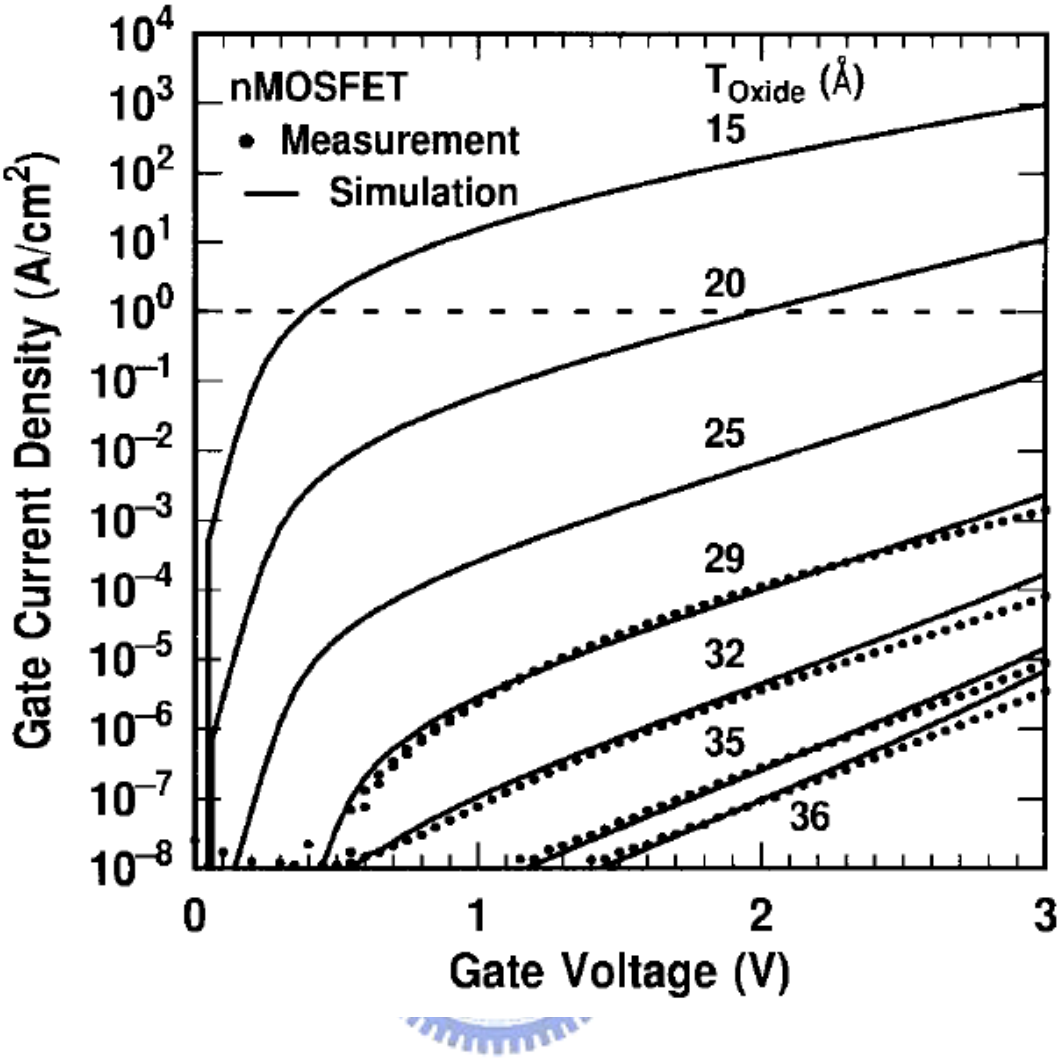


Fig. 1-1 Leakage current versus gate voltage for various thickness of SiO_2 layers [1].

Year of Production	2007	2008	2009	2010	2011
MPU/ASIC Metal1 ½ Pitch (nm) (contacted)	68	59	52	45	40
Physical Gate Length (nm)	25	22	20	18	16
Equivalent Oxide Thickness (EOT) Requirements					
Extended Planar Bulk (Å)	11	9	7.5	6.5	5.5
UTB FD-SOI (Å)				7	6
DG MOSFET (Å)					8
Gate Poly Depletion and Inversion-Layer Thickness Requirements					
Extended Planar Bulk (Å)	7.4	3.1	2.9	2.8	2.7
UTB FD-SOI (Å)				4	4
DG MOSFET (Å)					4
Saturation Threshold Voltage Requirements					
Extended Planar Bulk (mV)	134	94	94	103	101
UTB FD-SOI (mV)				103	89
DG MOSFET (mV)					115

Manufacturable solutions exists, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufactruable solutions are not known

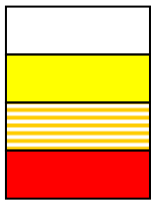


Fig. 1-2 International Technology Roadmap for Semiconductors (ITRS) 2007 for high performance logic technology. [2]

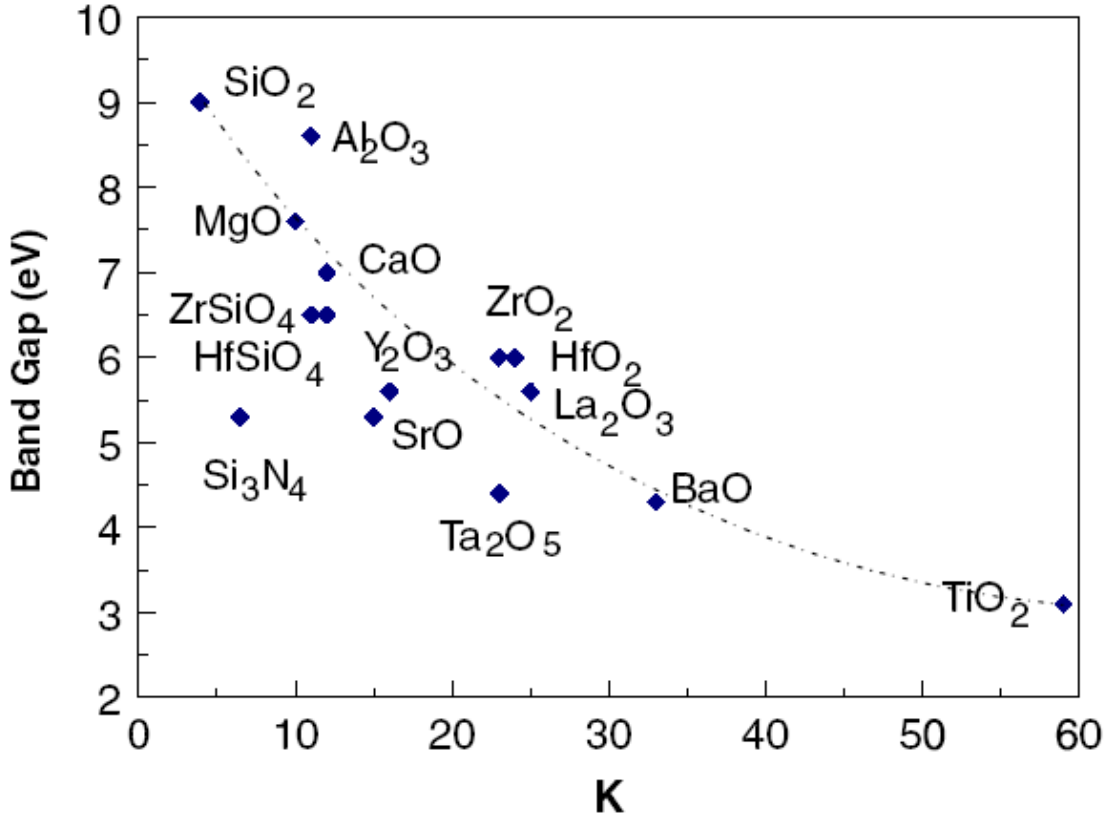


Fig. 1-3 Static dielectric constant verse band gap for several popular metal oxides [3].

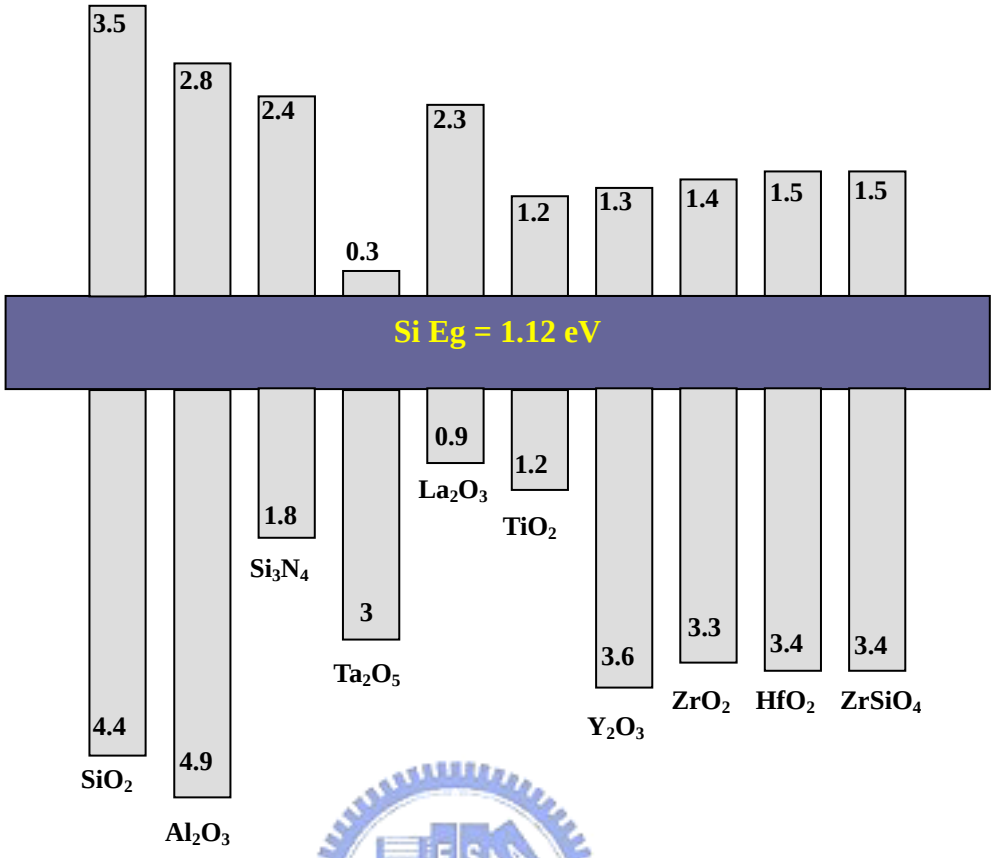


Fig. 1-4 Energy band offset of popular high-κ materials.

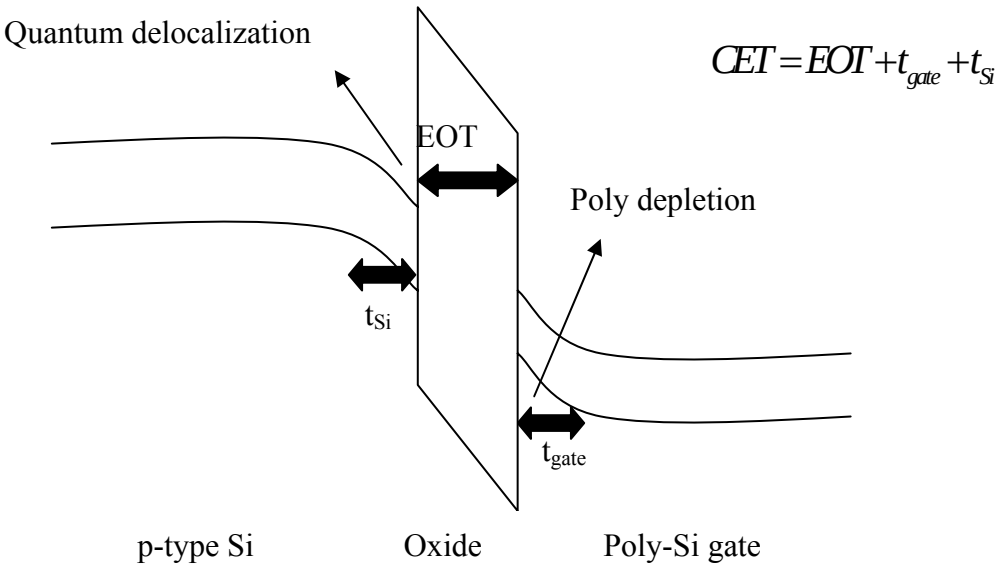


Fig. 1-5 The three contributions to the capacitance equivalent thickness (CET): gate oxide, poly depletion, and quantum delocalization.

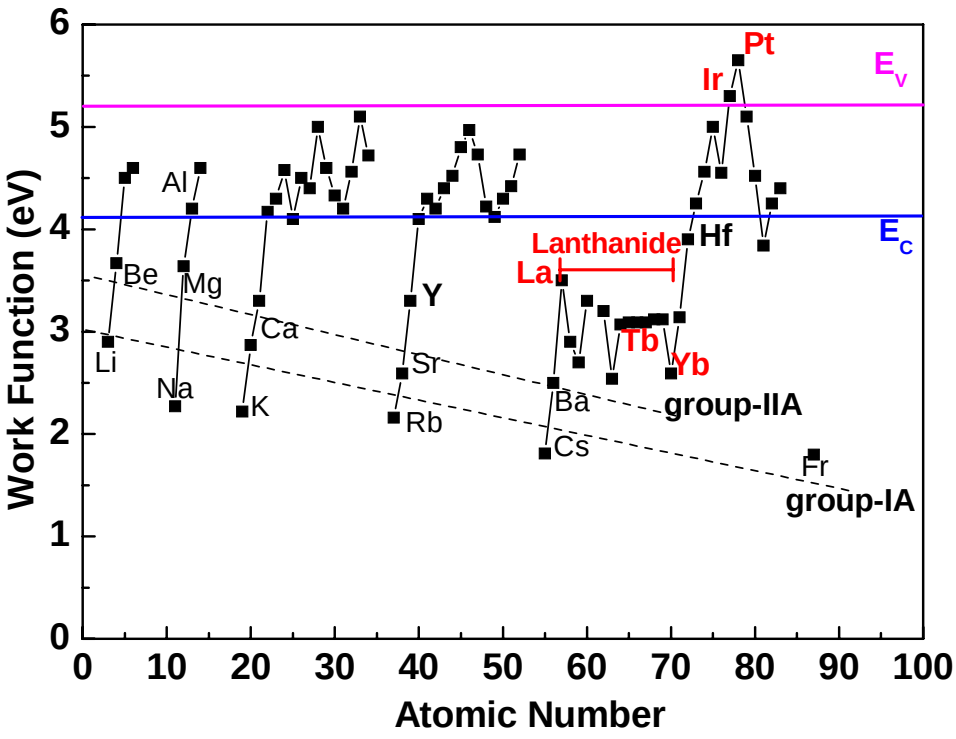


Fig. 1-6 The relationship between work function and atomic number. [13]

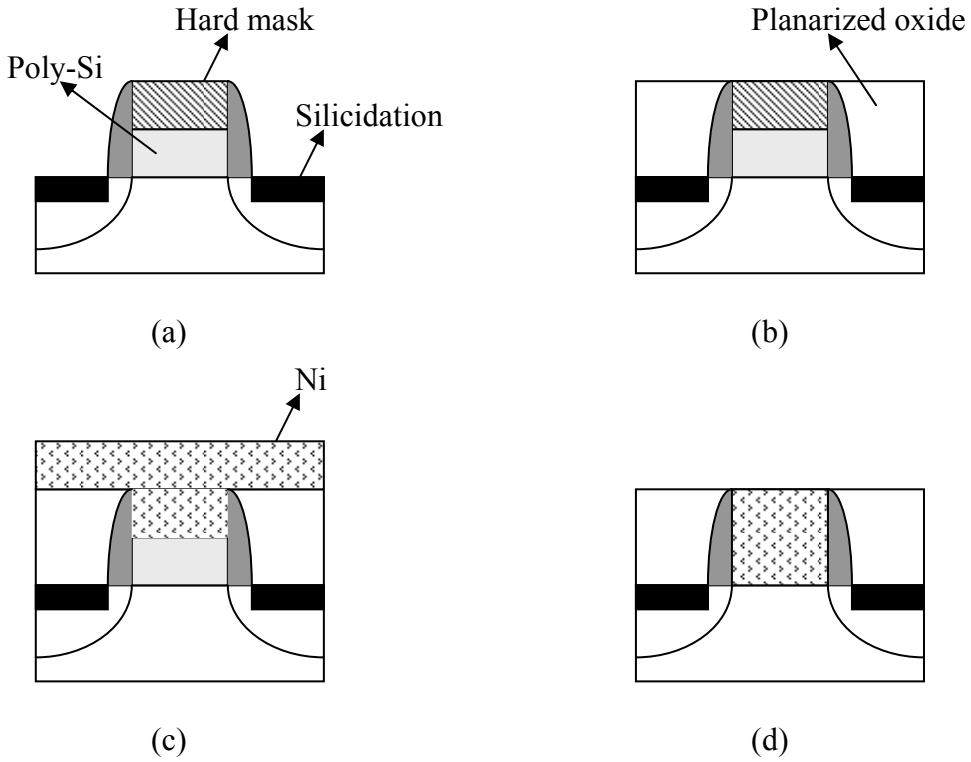


Fig. 1-7 The process flow of FUSI gate. (a) Gate patterning and S/D silicidation. The hard mask is not removed after pattering so that it can protect the gate from being silicided during the S/D silicidation, (b) Dielectric deposition and planarization, (c) Hard mask removal and Ni deposition, (d) Ni fully silicidation and removal of the remaining Ni.

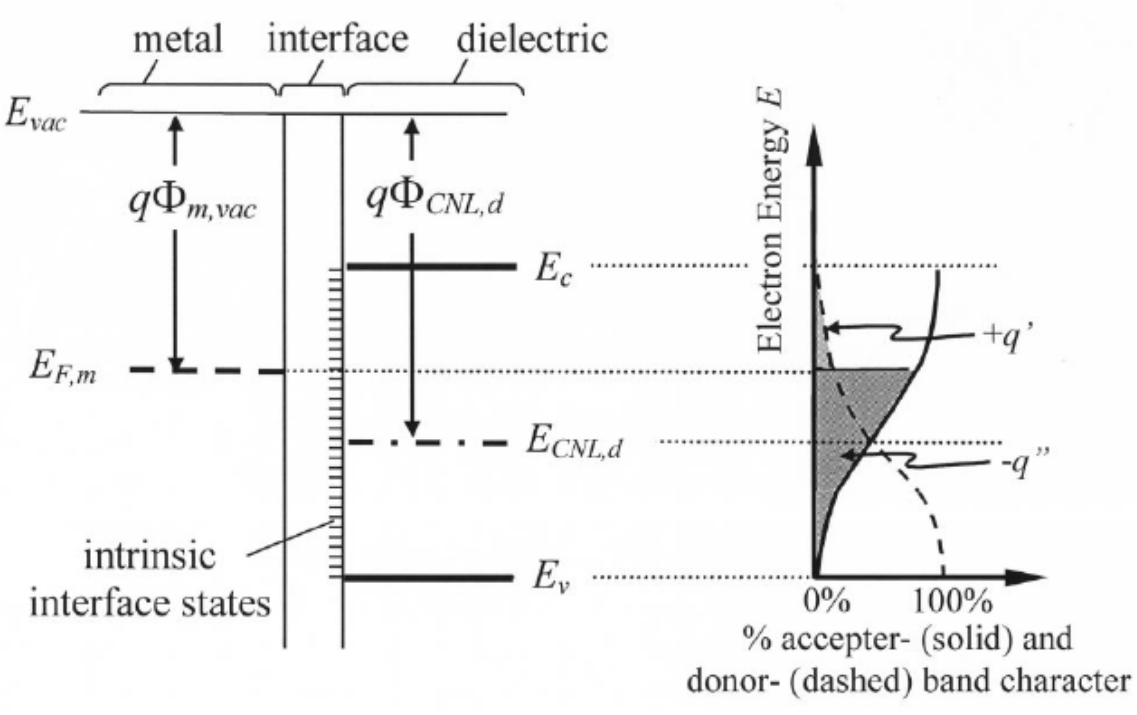


Fig. 1-8 Energy band diagram and charging characteristic of interface states for the metal-dielectric system [28].

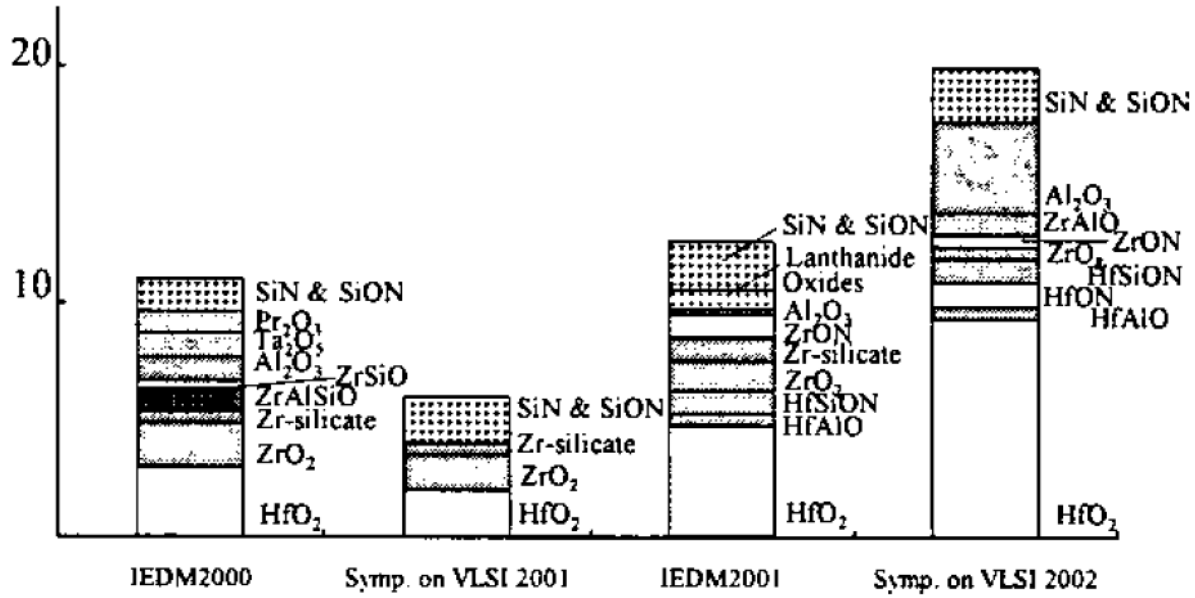


Fig. 1-9 Reported high-k materials in recent years. [31]

Chapter 2

The Experimental Steps and Measurements

In this thesis, $HfSi_x/Hf_{0.7}La_{0.3}ON/Si$ MIS capacitor and transistor were fabricated to investigate their electrical characteristics. The starting wafer was 4-inch, (100) oriented p-type wafer with one side polished. After standard RCA clean (Fig. 2-1), wafers were put into the chamber of the physical vapor deposition (PVD) system, where $Hf_{0.7}La_{0.3}O$ thin films were deposited on the wafers. Subsequently, oxygen post deposition anneal (PDA) was imposed on these samples.

After the PDA, a plasma nitridation were imposed on the $Hf_{0.7}La_{0.3}O$ surface wafers to form $Hf_{0.7}La_{0.3}ON$ film. Then, amorphous Si of 5 nm was deposited on the $Hf_{0.7}La_{0.3}ON$ surface followed by a PVD deposition of 20 nm Hf. For the $HfSi_x/Hf_{0.7}La_{0.3}ON/Si$ MIS capacitor, a 30 nm thick Mo was deposited by PVD to prevent Hf oxidation after the Hf deposition. For $HfSi_x/Hf_{0.7}La_{0.3}ON/Si$ transistor, an additional amorphous-Si layer of 150 nm was deposited by PVD to avoid ion implantation damage through the gate. Gates of all samples were defined by lithography and etching.

After defining the gate, a phosphorous ion implantation at 35 KeV, 5×10^{15} cm^{-2} dose was used to form n^+ source/drain (S/D) regions of transistors. Afterwards, rapid thermal anneal (RTA) at 1000^oC, 5 sec was used to activate carriers in S/D region. The FUSI $HfSi_x$ gate was

also formed at this high temperature RTA, which is different from a conventional low temperature FUSI process. For comparison, TaN gates were also deposited on the $Hf_{0.7}La_{0.3}ON$ to form the TaN/$Hf_{0.7}La_{0.3}ON$/Si MIS capacitor.

To analyze the electrical characteristics of these devices, we used HP4156 semiconductor parameter analyzer to measure the *I-V* characteristics. Besides, the HP4284A precision LCR meter was used to evaluate the C-V characteristic. The whole process is shown in Fig. 2.2 ~ Fig. 2.15.

1. DI water rinse, 5 min
2. H_2SO_4 : H_2O_2 = 3:1 , 10 min, 75~85^oC
3. DI water rinse, 5 min
4. HF : H_2O = 1:100, 10~15 s
5. DI water rinse, 5 min
6. NH_4OH : H_2O_2 : H_2O = 1:4:20 , 10 min, 75~85^oC
7. DI water rinse, 5 min
8. HCl : H_2O_2 : H_2O = 1:1:6, 10 min, 75~85^oC
9. DI water rinse, 5 min
10. HF : H_2O = 1:100, 10~15 s
11. DI water rinse
12. Spinner dry

Fig. 2-1 Standard RCA clean process.

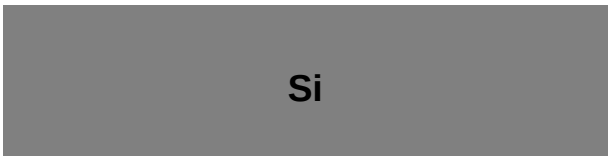


Fig. 2-2 4-inch (100) P-type wafer.

Fig. 2-3 Standard RCA clean.

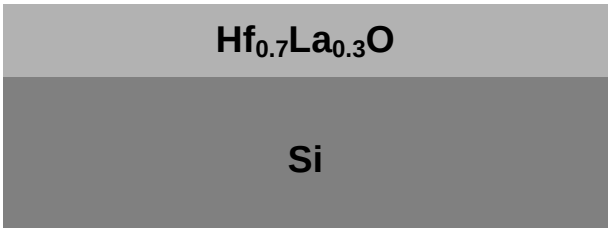


Fig. 2-4 $Hf_{0.7}La_{0.3}O$ deposition by PVD.

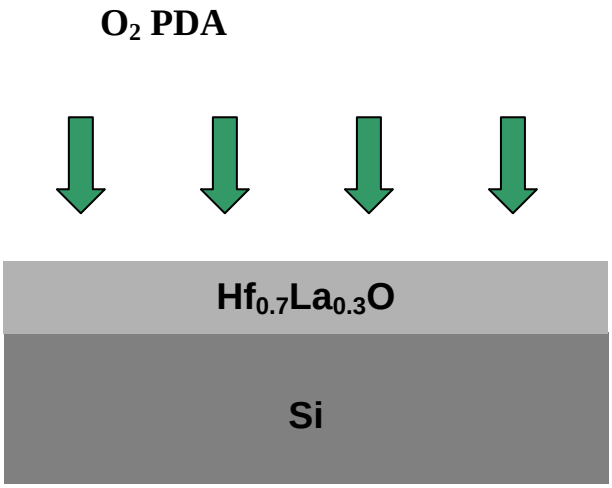


Fig. 2-5 Low temperature oxygen PDA.

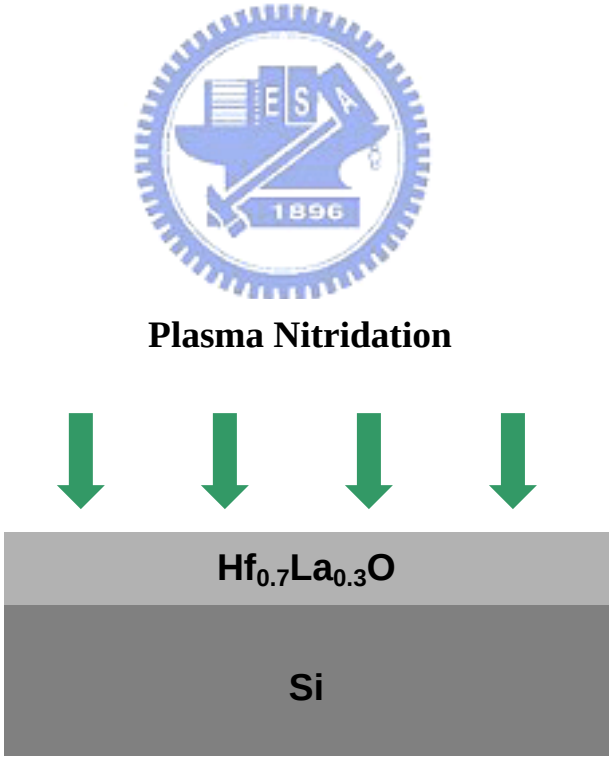


Fig. 2-6 Plasma nitridation to form $Hf_{0.7}La_{0.3}ON$.

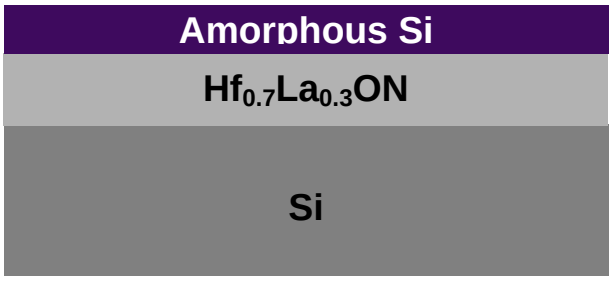


Fig. 2-7 Amorphous Si deposition by PVD (5 nm).

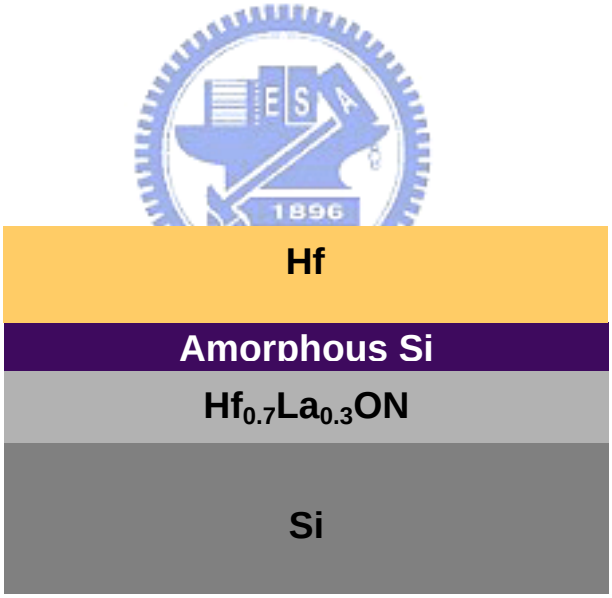


Fig. 2-8 Hf deposition by PVD (20nm).

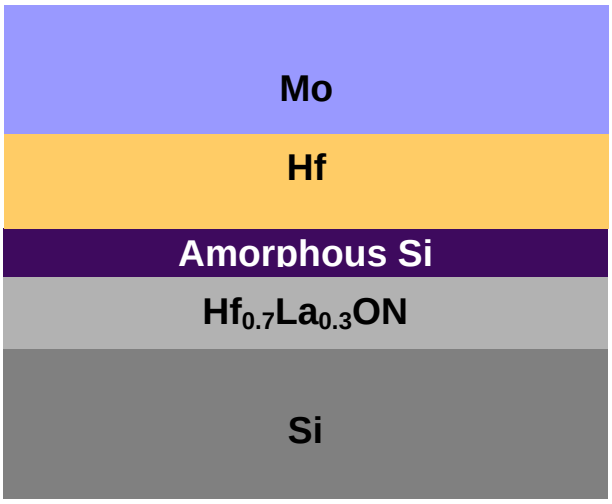


Fig. 2-9 Mo deposition by PVD (30 nm) for capacitors.

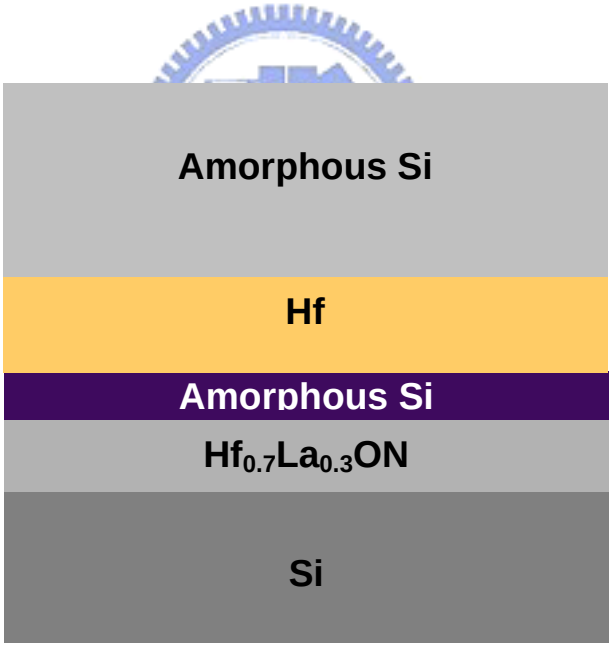
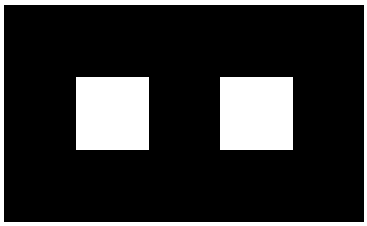


Fig. 2-10 Amorphous Si deposition by PVD (150 nm) for n-MOSFETs.

MASK



Lithography Patterning

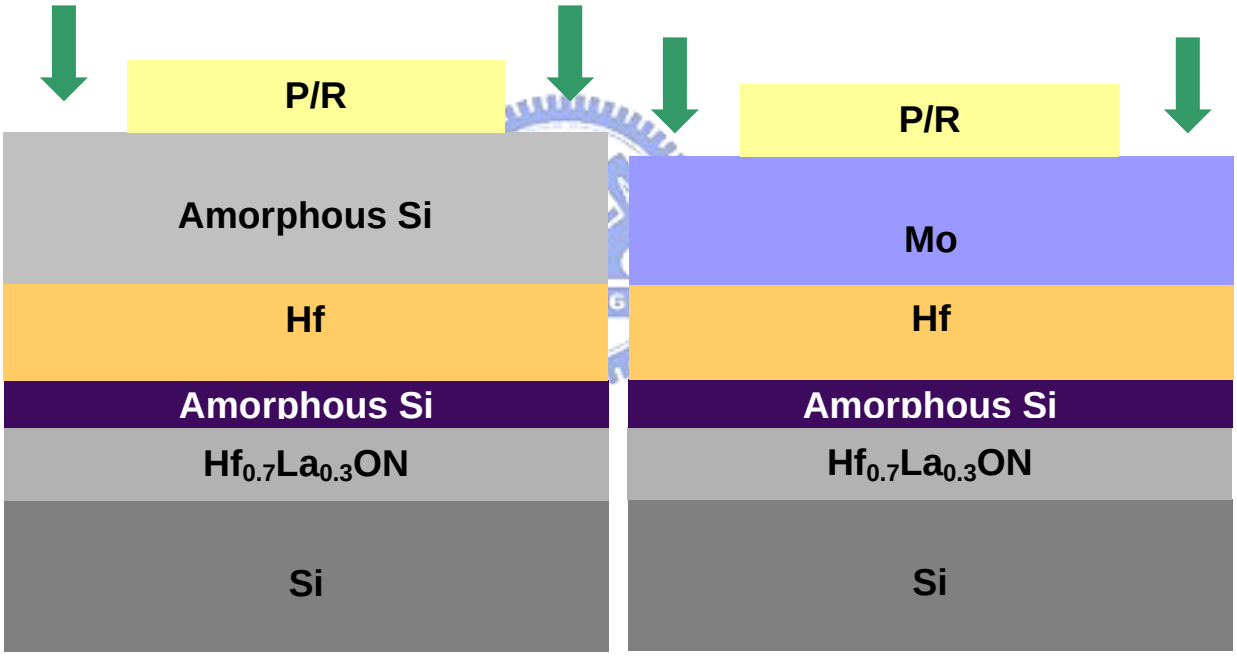


Fig. 2-11 Lithography patterning for capacitors and n-MOSFETs.

Etching

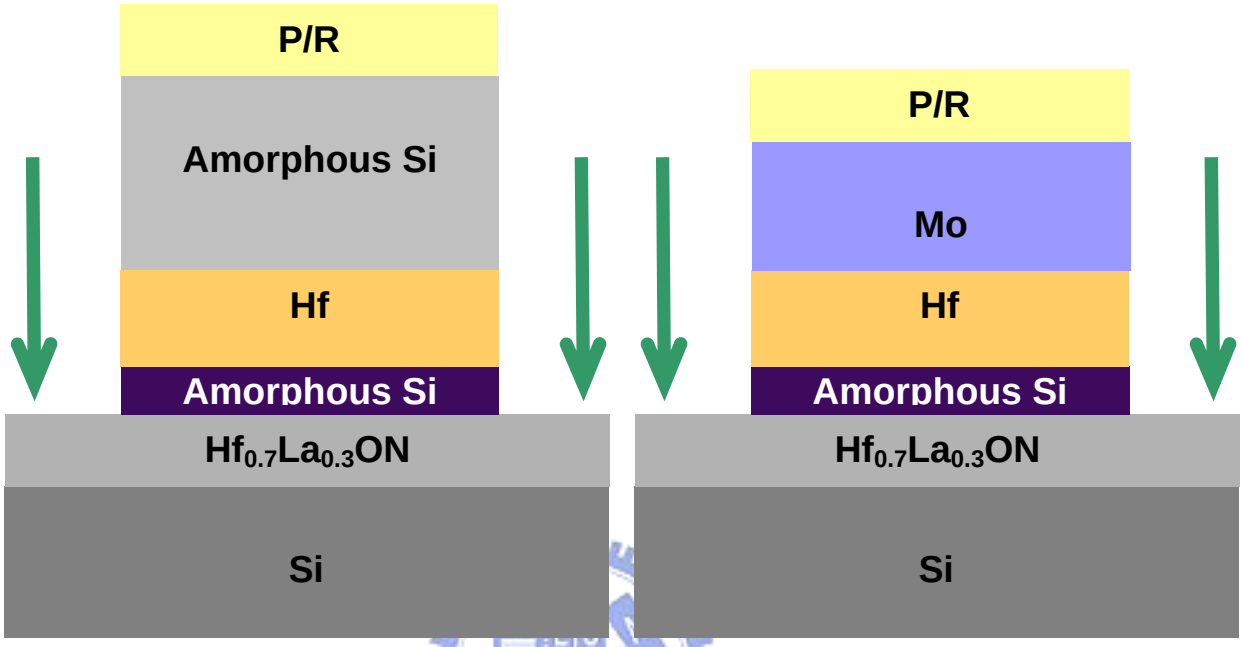


Fig. 2-12 Etching for capacitors and n-MOSFETs.

Ion Implantation

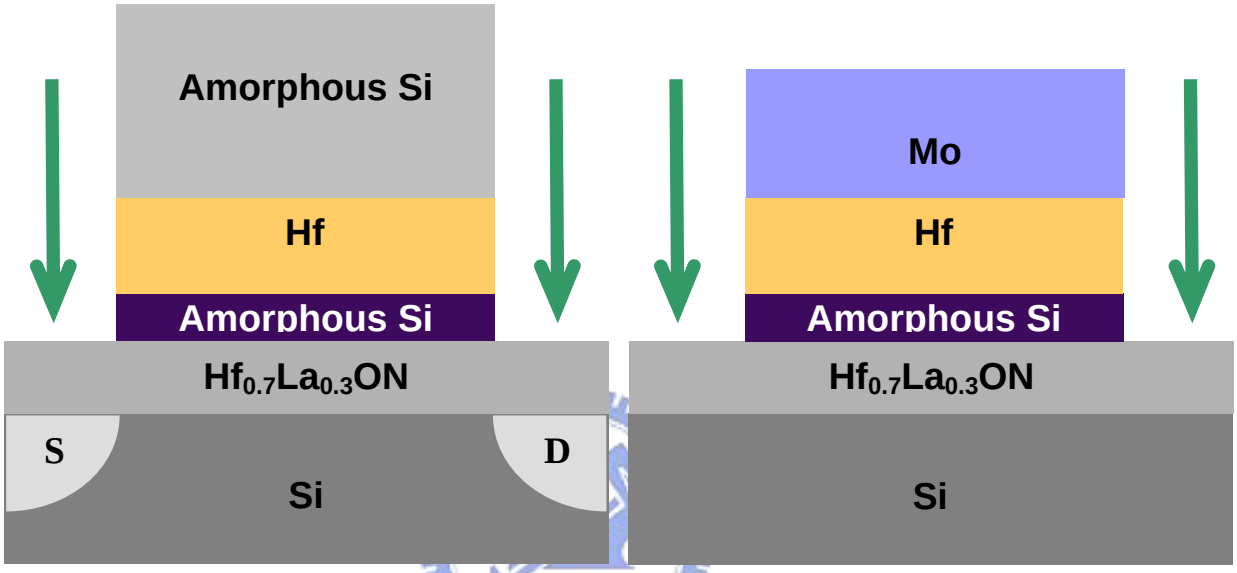


Fig. 2-13 Phosphorus ion implantation to form n^+ source/drain for n-MOSFETs (35 KeV, 5×10^{15} cm^{-2} dose).

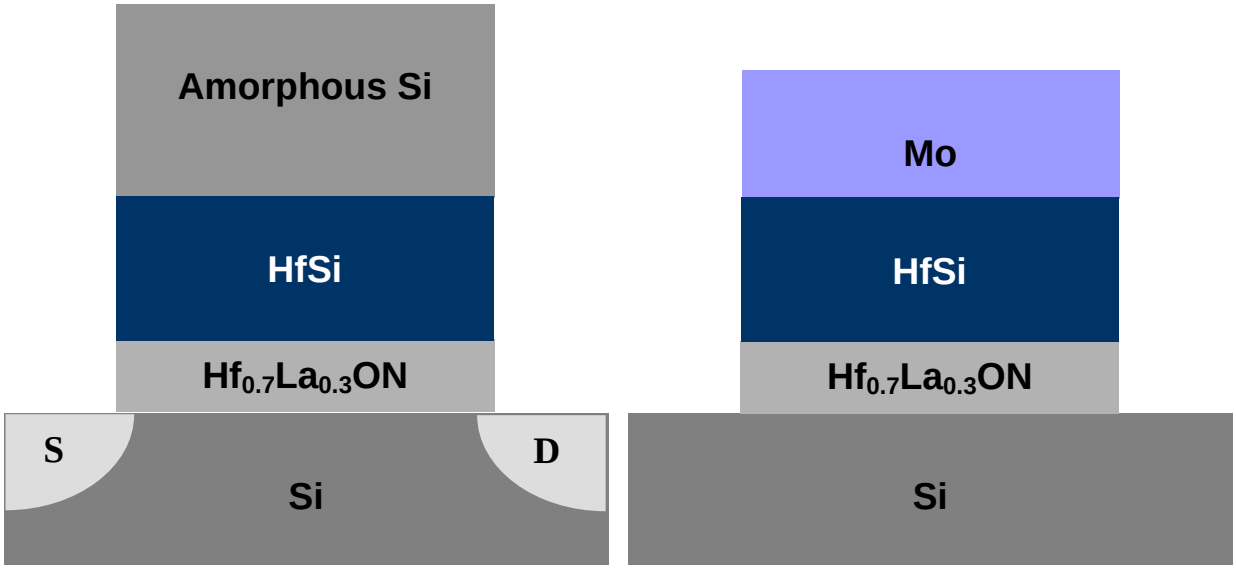


Fig. 2-14 RTA at 1000˚C, 5 sec for capacitors and n-MOSFETs.

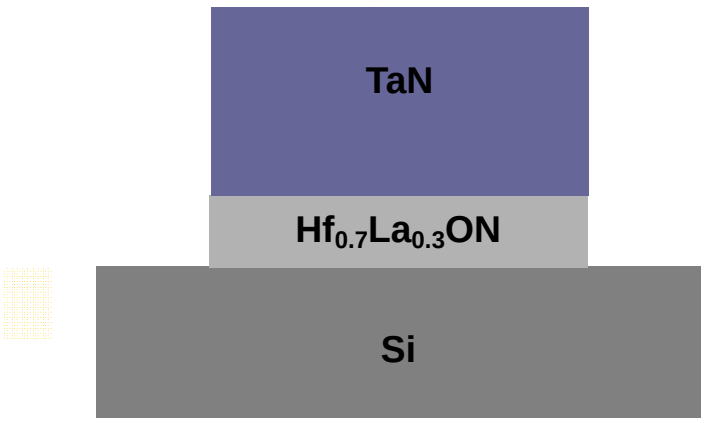


Fig. 2-15 A TaN gate capacitor for comparison.

Chapter 3

Result and Discussion

3.1 Device parameter extraction

In this thesis, EOT and V_{FB} were extracted from the Quantum *C*-*V* simulation. Threshold voltage and mobility extraction was described in detail in the following sections.

3.1.1 Threshold voltage extraction

There are various methods for determining the threshold voltage. Here we use the linear extrapolation method, which is one of the most common techniques to extract the threshold voltage. This method is based on:

$$I_D = \frac{W}{L} C_{ox} \mu_{eff} \left(V_G - V_{th} - \frac{V_D}{2} \right) V_D \tag{3.1}$$

where W and L are channel width and channel length, respectively. C_{ox} is the gate oxide capacitance per unit area and V_{th} is the threshold voltage. μ_{eff} is the field effect mobility, which will be discussed in the next sub-section.

The drain current is measured as a function of gate voltage at a low drain voltage = 0.1 V. The low drain voltage is to ensure that the operation is under the linear region. The I_{DS}-V_{GS} curve differs from a straight line at $V_{GS} < V_{th}$ due to sub-threshold current and at $V_{GS} > V_{th}$ due to series resistance and mobility degradation. There is a linear region at the neighboring of

V_{GS} at which g_m is maximum. The I_{DS}-V_{GS} curve can be fitted a straight line to extrapolate to I_D=0 by means of finding the point of $g_{m,\,max}$. Therefore, the V_{th} is extracted from the V_G-axis intersection. The resultant threshold voltage is given by:

$$V_{th} = V_{GSi} - \frac{V_{DS}}{2} \tag{3.2}$$

where V_{GSi} is the value of the intersection point.

3.1.2 Mobility extraction

According to Eq. (3.1), the effective mobility can be expressed as:

$$\mu_{eff} = I_D \frac{L}{C_{ox} W \left[(V_G - V_{th}) V_D - V_D^2 / 2 \right]} \tag{3.3}$$

The effective mobility is usually plotted against an effective normal field E_{eff}, which is defined as:

$$E_{eff} = \frac{V_{th} + 0.2}{3t_{ox}} + \frac{V_g - V_t}{6t_{ox}} \tag{3.4}$$

3.2 Characteristics of $HfSi_x/Hf_{0.7}La_{0.3}ON$ capacitors

Fig. 3-1 shows the *C*-*V* characteristic of the $HfSi_x/Hf_{0.7}La_{0.3}ON$/Si MIS capacitor. The characteristic of the $TaN/Hf_{0.7}La_{0.3}ON$/Si capacitor is also shown in Fig. 3-2 for comparison. The FUSI $HfSi_x$ gate was formed by depositing 20 nm Hf on thin 5 nm amorphous-Si followed by 1000°C RTA while the TaN gate was formed by depositing 150 nm TaN directly on $Hf_{0.7}La_{0.3}ON$. The result shows the $HfSi_x/Hf_{0.7}La_{0.3}ON$/Si capacitor has a high capacitance

density, close to that using the TaN gate. This result proves that the FUSI $HfSi_x$ has no poly-Si depletion. In addition, the V_{FB} of the $HfSi_x$ gate is more negative than for the TaN gate by 0.05 V, which is needed for low V_{th} operation. An EOT of 1.2 nm was obtained by the quantum-mechanical (QM) *C-V* simulation. A low $\phi_{m,eff}$ of 4.33 eV was obtained from a V_{FB}-EOT plot for the $HfSi_x/Hf_{0.7}La_{0.3}ON/Si$ capacitor, as shown in Fig. 3-3. This low effective work function makes them suitable for NMOS applications.

In Fig. 3-4, the leakage current of $HfSi_x$ is 9.2×10^{-4} A/cm^2 at 1 V below the V_{FB}. It is about 5 orders of magnitude lower than that of SiO_2 at a 1.2 nm EOT. This low leakage current is mainly due to the higher dielectric constant of $Hf_{0.7}La_{0.3}ON$. $Hf_{0.7}La_{0.3}ON$ with higher dielectric constant can have larger physical thickness at the same EOT as SiO_2. Therefore, the direct tunneling current can be highly decreased. The low leakage current also proves the good thermal stability of the $HfSi_x/Hf_{0.7}La_{0.3}ON$ gate structure after a 1000^{o}C RTA. In contrast, the leakage current of TaN is 2.8×10^{-3}/cm^2 at 1 V below the V_{FB}, as shown in Fig. 3-5. The higher leakage current at low voltages using TaN gate than that of $HfSi_x$ may be due to the sputter-induced damage to the $Hf_{0.7}La_{0.3}ON$ gate dielectric.

3.3 Characteristics of $HfSi_x/Hf_{0.7}La_{0.3}ON$ n-MOSFETs

Figures 3-6 and 3-7 show the I_D-V_D and I_D-V_G transistor of the 1.2 nm EOT $HfSi_x/Hf_{0.7}La_{0.3}ON$ n-MOSFETs. Good transistor characteristics can be seen from Fig. 3-6

and 3-7. A small V_{th} of only 0.18 V was extracted from the linear I_D-V_G plot, as shown in Fig. 3-8. This is due to the low $\phi_{m,eff}$ of 4.33 eV found from the *C-V* measurements.

The mobility as a function of effective electric field for the $HfSi_x/Hf_{0.7}La_{0.3}ON$ n-MOSFETs is shown in Fig. 3-8. High peak electron mobility of 215 cm^2/V-s is obtained at a small EOT of 1.2 nm.

Altogether, the small EOT of 1.2 nm, low V_{th} of 0.18 V, good peak mobility of 215 cm^2/V-s and simple high-temperature FUSI processing makes $HfSi_x/Hf_{0.7}La_{0.3}ON$ device a potential candidate for n-MOSFET application.

Table 3-1 summarizes and compares the important transistor characteristics for various FUSI gate/high-κ n-MOSFETs.

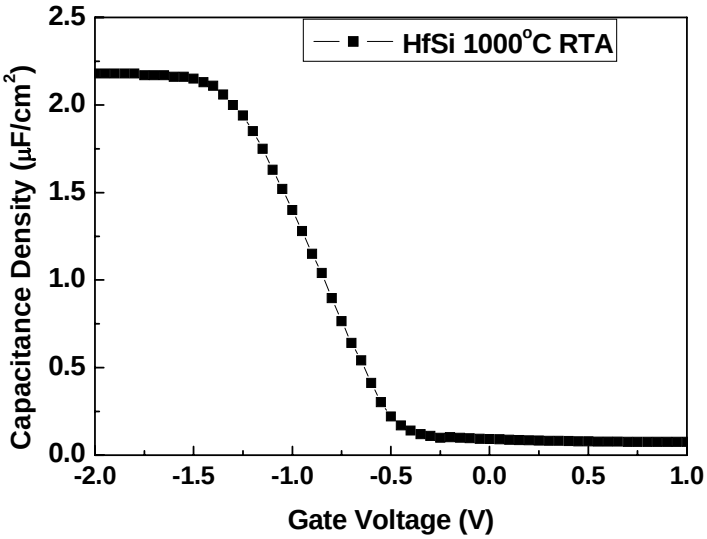


Fig. 3-1 *C-V* characteristics of the $HfSi_x/Hf_{0.7}La_{0.3}ON/Si$ capacitor.

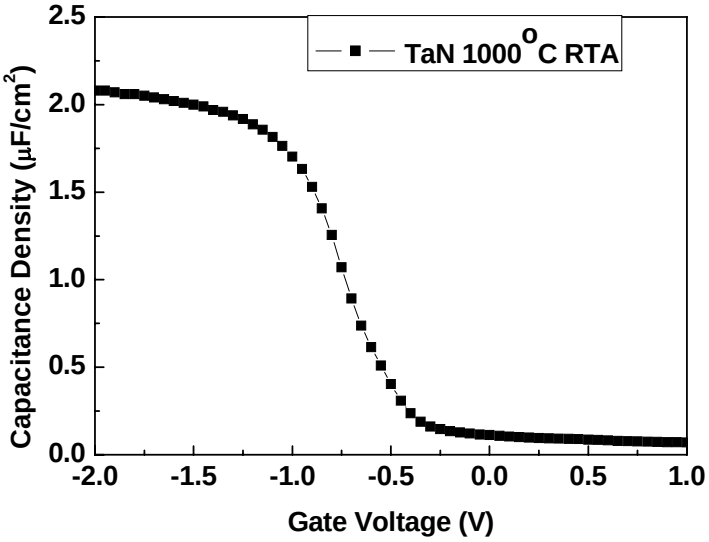


Fig. 3-2 *C-V* characteristics of the TaN/$Hf_{0.7}La_{0.3}ON$/Si capacitor.

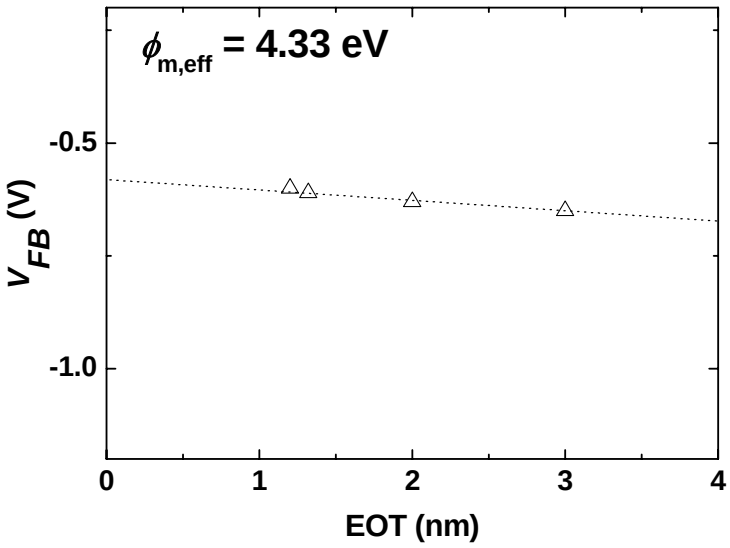


Fig. 3-3 V_{FB}-EOT plot of the $HfSi_x/Hf_{0.7}La_{0.3}ON/Si$ capacitor. The extracted effective work function of $HfSi_x$ from the plot is 4.33 eV.

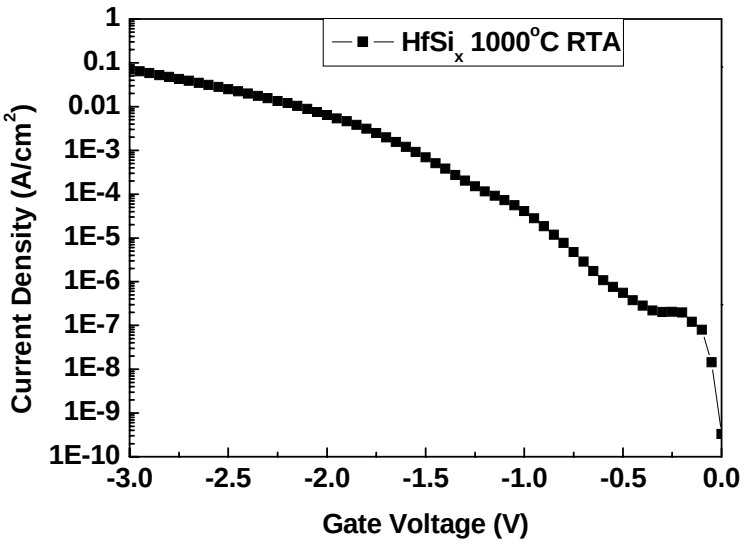


Fig. 3-4 *J-V* characteristic of the $HfSi_x/Hf_{0.7}La_{0.3}ON/Si$ capacitor.

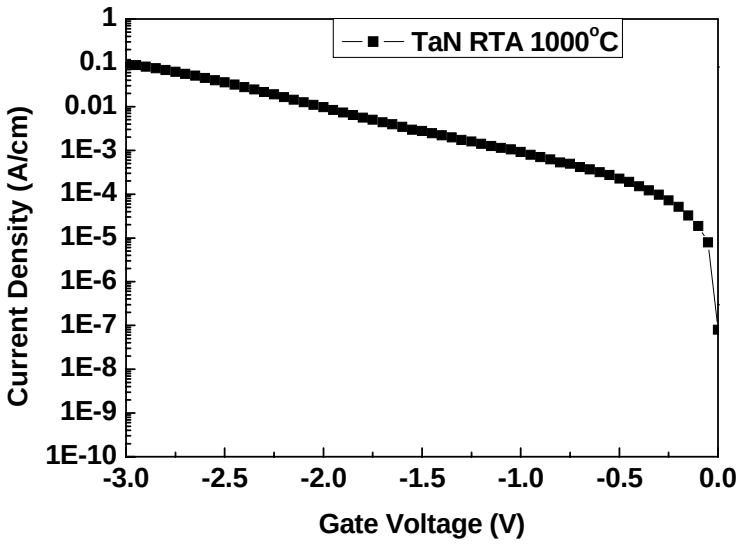


Fig. 3-5 *J-V* characteristic of the TaN/$Hf_{0.7}La_{0.3}ON$/Si MIS capacitor.

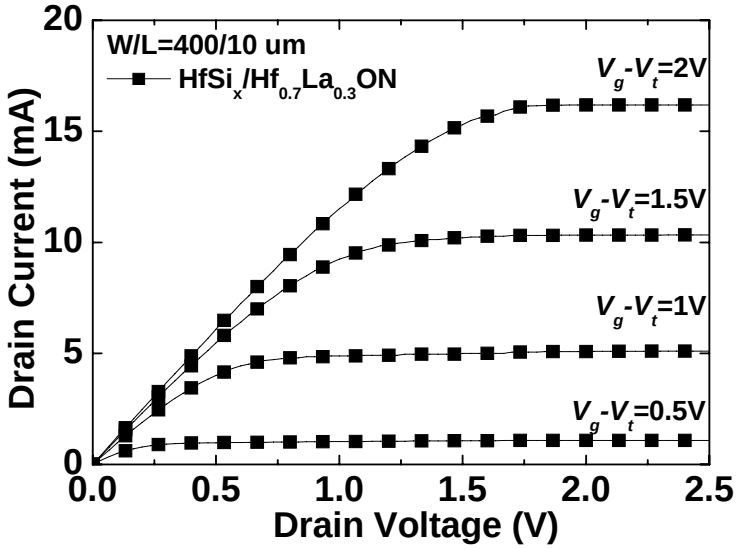


Fig. 3-6 I_D-V_D characteristic of the $HfSi_x/Hf_{0.7}La_{0.3}ON$ n-MOSFET.

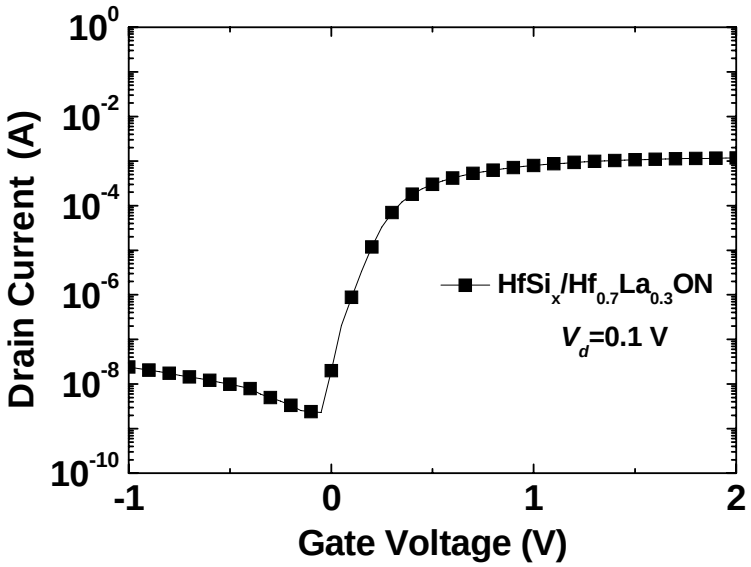


Fig. 3-7 I_D-V_G characteristic of the $HfSi_x/Hf_{0.7}La_{0.3}ON$ n-MOSFET.

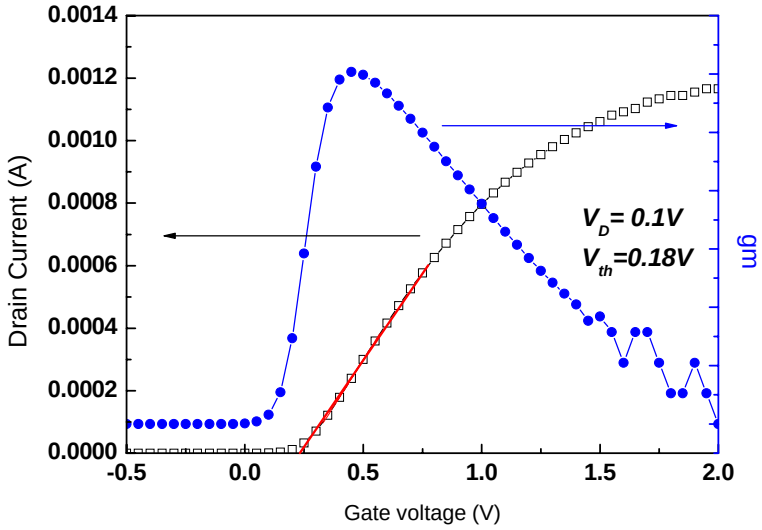


Fig. 3-8 I_D-V_G characteristic of $HfSi_x/Hf_{0.7}La_{0.3}ON$ n-MOSFETs in linear scale. The extracted V_{th} is 0.18 V.

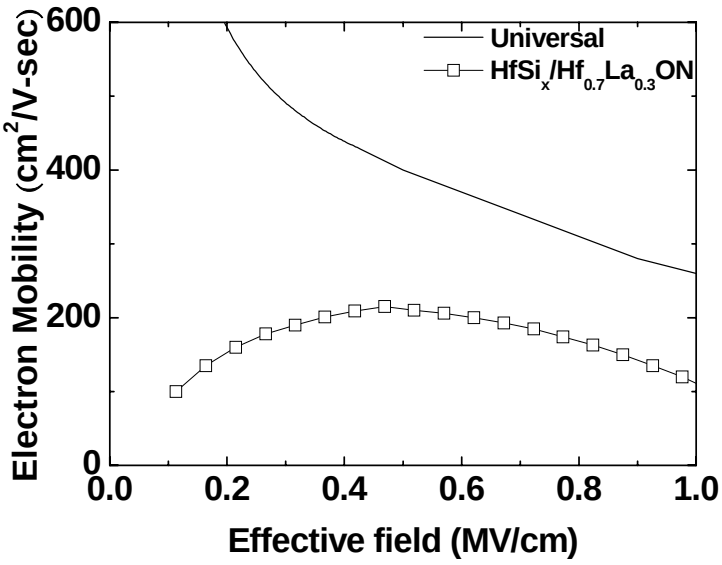


Fig. 3-9 The mobility of the $HfSi_x/Hf_{0.7}La_{0.3}ON$ n-MOSFET.

Table 3-1 Comparison of device parameters for several FUSI gate/high-κ n-MOSFETs.

Ref.	Metal gate	High-κ	V_{th} (V)	EOT (nm)	RTA temp.
[35]	FUSI NiSi	La_2O_3	0.12	1.5	400°C, 30 s
[36]	FUSI Yb_xSi	HfAlON	0.1	1.7	Low temp.
[37]	FUSI $NiSi_2$	HfSiON	0.47	1.7	450-650 °C, 1 min
[38]	FUSI NiSi	HfSiON	0.5	1.43	Low temp.
[39]	TaN	HfLaON	0.18	1.6	1000°C
This work	FUSI $HfSi_x$	HfLaON	0.18	1.2	1000°C, 5 s

Chapter 4

Conclusion

In this thesis, $HfSi_x$ and $Hf_{0.7}La_{0.3}ON$ have been studied for n-MOSFET applications. This structure has been demonstrated with good device characteristics. We have fabricated the FUSI $HfSi_x$ gate on $Hf_{0.7}La_{0.3}ON$ with 1.2 nm EOT. After 5 sec, 1000°C RTA, the device displayed a low threshold voltage of 0.18 V, low effective work function of 4.33 eV, low leakage current of 9.2×10^{-4} A/cm^2 at 1 V and high peak electron mobility of 215 cm^2/V-s. Thermal stability at 1000°C RTA ensures that the device can endure the high temperature at the gate-first process. The gate-first and self-aligned process of $HfSi_x$/HfLaON n-MOSFETs make this device compatible with current VLSI lines.

It has been shown that FUSI $HfSi_x$, like FUSI $NiSi_x$ has a wide range of work-function tuning [23]. The incorporation of n-type dopants to the poly-Si pre-gate has the potential to shift the effect work function to a lower value, which is suitable for NMOS operation. On the other hand, the incorporation of p-type dopants into the poly-Si or phase control technique might be used for PMOS application. The band-edge FUSI $HfSi_x$ CMOS still needs to be further developed.

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論文題目：

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A Low Threshold n-MOSFET Using Fully Silicided Gate and High-κ Dielectric