國立交通大學

電子工程學系　電子研究所碩士班

碩士論文

常壓式電漿系統沈積之二氧化矽在有機薄膜電晶體應用上之研究

The study on the silicon dioxide deposited by Atmospheric-Pressure Plasma Technology for Organic Thin-Film Transistor application

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中華民國 九十七年 七 月

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常壓式電漿系統沈積之二氧化矽在有機薄膜電晶體應用上之研究

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摘　　要

我們已成功的利用大氣壓電漿技術在有機薄膜電晶體上沈積閘極矽氧化物。大氣壓電漿技術的優點在於可不必抽真空亦可於一般室溫下進行沈積動做。此優點正好適合有機薄膜電晶體的低溫製程條件。此篇論文中我們將研究大氣壓電漿技術所沈積閘極矽氧化物在有機薄膜電晶體上的特性。我們利用金屬-絕緣層-金屬的結構來探討大氣壓電漿技術所沈積閘極矽氧化物的漏電流，其中我們得到經過電漿處理過後的閘極介電層有較低的漏電流。在這次研究中，我們的有機薄膜電晶體操作電壓小於-3 伏特，在可攜式的電子產品上低的操作電壓與低的漏電流是必要的條件。在本文可以觀察OTFT在大氣壓電漿技術所沈積的二氧化矽上的特性，其臨界電壓可在-1伏特以內，載子遷移率也達到0.5-0.8 cm^2/Vs以及 on/off ratio 約在10^3。

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ABSTRACT

We have successfully fabricated pentacene-based organic thin film transistor at a low temperature process with silicon oxide as a gate dielectric deposited by atmospheric-pressure plasma technology (APPT). The advantage of the atmospheric-pressure plasma technology is that it needn't vacuum and at general room temperature to deposit insulator. This merit happen to suits the organic thin film transistor the low temperature system regulation condition. In this article we will study the characteristic of gate silicon oxide which is deposited by atmospheric-pressure plasma technology on the organic thin film transistor. We make use of metal - insulator - metal structure to probe into leakage current of the gate silicon oxide deposited by APPT, and we

obtain the lower leakage current of gate dielectric after plasma treatment. In the research, the organic thin film transistor can operate at the voltage less than - 3 volts, and the low operation voltage and low leakage current properties are required in portable applications. In this article we can observe the OTFT characteristic on silicon oxide deposited by APPT. The field-effect transistor has a threshold voltage less than -1V, the mobility of 0.5-0.8 cm^2/Vs and on/off ratio about 10^3.

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Chapter 1
Introduction

1.1 History of OTFT and motivation

With the invention of the transistor around the middle of the last century, inorganic semiconductors like Si, Ge, GaAs, InP, etc. began to take over the role as dominant material in electronics from the before prevailing metals. At the same time, the replacement of vacuum tube based electronics by solid state devices initiated a development which by the end of the 20^{th} century has lead to the omnipresence of semiconductor microelectronics in our everyday life. Now at the beginning of the 21^{st} century we are facing a new electronics revolution that has become possible due to the development and understanding of a new class of materials, commonly known as Organic Semiconductors.

Research in organic semiconductor materials continues to create innovative application areas requiring low temperature processing, large area coverage, mechanical flexibility, and low overall cost [1,2]. A number of applications have been recognized as organic thin-film transistors (OTFTs), including active matrix flexible displays, electronic paper (e-paper), low-end data storage such as smart cards, radio-frequency identification devices, and low-cost disposable sensor arrays [3]. Polymeric substrates are more sympathetic for OTFT than conventional silicon-based transistors because they can be fabricated with a low-temperature process. Therefore, OTFT on polymeric substrates have been developed to construct organic integrated circuits [4~6], active-matrix liquid crystal displays (AMLCDs) [7,8], and active matrix organic electroluminescent displays [9].

In the last two decades, the performance of OTFT has steadily improved. As a result of the development of new organic semiconductors, the optimization of deposition conditions and gate dielectric surface treatments [10~13].

On the other hand, the improvement in organic semiconductor material characteristic, the process enhances the technology and the improvement in OTFT structure, the OTFT application gradually is realized on integrated circuits. Mobility magnitude decides the performance of the OTFT transistor. However, the high operating voltage remains a limitation on organic transistors. The large operating voltage which is often higher than 10V is one of the most critical problems for organic TFT. Consequently, account for the power consumption of the transistor to increase and the performance of the transistor to reduce.

1.2 Introduction of OTFT

1.2.1 Introduction of organic semiconductor

The molecules of the organic semiconductor are joined to by van der Waals power with energy smaller than 10 kcal mol^{-1}. This weak interaction energy of molecules may take responsibility for the low upper limit of carrier motilities, falls between 1-10 ㎠/Vs by time-of-flight measurement [14], due to the energy of vibrations of the molecule is close to this value. Interaction energy of molecules of inorganic semiconductors is strong such as 76 kcal mol^{-1} in silicon. Thus the carriers move as highly delocalized plane waves in wide band with high mobility.

Organic semiconductor materials such as polythiophene, poly (3-hexylthiophene) (P3HT) have been investigated for use in field effect transistors [15]. We presented a semilogarithmic plot of the highest yearly reported field-effect mobility value measured from thin-film transistors based on specific organic semiconductors, beginning in 1986. An update of that plot is shown in Fig 1-1 and, which is based on Table 1-1 [16]. Pentacene based FETs show the high mobility.

1.2.2 Contact resistance of OTFT

The performance of OTFT will be influenced by a lot of parameters. The contact resistance between the source/drain electrodes and the organic semiconductor is an important one of them [17~19]. It may be the important blocking in contact resistances at the source and drain terminals in organic TFTs as to electric current. In recent years, work by a number of research groups has shown that the properties of the source and drain contacts in organic TFTs can have an important effect on the overall devices performance. For example, a transmission line study of contact resistances in pentacene TFTs has been published by Jackson [20] and it shows significant differences in the contact properties for top versus bottom contact devices. In a more previous research, Dimitrakopoulos and co-workers demonstrated that for bottom contact TFTs there is a region of disorder in the pentacene thin near the contact interface, though the disorder can be mitigated by thiolating the contacts [21].

It is a straightforward method to find a suitable electrode material which forms ohmic contact with the organic active layer and thus to improve the performance of OTFT. Pentacene can form an ohmic contact with material for its work function larger than 5.1eV because the work function of pentacene is 5.1eV. Work functions of all materials we used are larger than 5.1eV; they include Ni (5.1eV), Pt (5.65eV), Cr (4.5eV).

1.2.3 Pattern of active region

For obtains the high efficiency experiment, develops many conveniences process technology. A variety of strategies have been used to create integrated arrays of transistors including photolithography, stamping, and shadow masking. Photolithography has established infrastructure thanks to its extensive use in silicon fabrication, printing process in which the printing surface is neither raised no retched into the plate , and printing is affected by means of a chemical process that allows ink to adhere to only the parts of the surface to be reproduced. Photolithographic patterning has several advantages: the first is arbitrary patterns can be used, the second is a variety of deposition techniques can be used and the third is photolithography can be applied over large areas in multilayer process.

1.2.4 The structure of organic TFT

Figure 1-3 (a) (b) show the standard two kind of organic TFTs configuration, (a) is the inverted staggered type TFT and (b) is the inverted coplanar type TFT. Usually, the former is also called the top contact (TC) and the latter is called the bottom contact (BC) TFT.

1.2.5 The electron transport of organic materials

Most organic solids are insulators due to two principle reasons. First, It is completely filled the highest occupied molecular orbital (HOMO) of most molecules, and there is a significant energy dissimilarity to the lowest unoccupied molecular orbital (LUMO). Secondly, the solids are usually molecular, not posessing a system of covalent bonds extending over macroscopic distances and hence quantum mechanical interactions between the HOMOs of adjacent molecules are small and the valence band formed by these interactions is very narrow. Similarly, it is also small that the conduction band arising from the interactions between the LUMOs, so the band gap is essentially that of the free molecule. This is also true for any σ-bonded polymers (e.g. polyethylene). To gain a larger conductivity and hence semiconducting behaviour, the HOMO–LUMO gap needs to be reduced; this can be achieved with extensive π-bonding, or including heteroatoms with lone pair electrons (e.g. polyacetylene, polyaniline or polyaromatics). This reduced band gap allows electrons to more easily jump between conduction and valence bands and gives rise to the semiconductive properties [22].

1.3 Introduction of pentacene and fabrication method

Pentacene (from *penta* = five, and *acenes* = polycyclic aromatic hydrocarbons with fused benzene rings) is a fused-ring polycyclic aromatic hydrocarbon. Structure of pentacene is shown in Figure 1-2.The lattice parameters of Structure of pentacene are shown in Table 1-2. And the other important parameters are descry bed as follows: [23,24]

Pentacene Formula: $C_{22}H_{14}$; Molecular weight: 278.3 ; Melting point:

573K ; Volume of the unit cell: 705.0°Å³ ; Density: 1.303g.cm^{-3}(calculated with Z = 2), 1.30 g.cm^{-3}(measured) ; Optical Bandgap: 2.8eV ; Absorption coefficient for X-rays: λ = 1.542nm ; Resistivity: ~10^{14}-10^{15} ohm-cm;

On organic small molecules, the highest hole and electron mobility has been demonstrated by pentacene($C_{22}H_{14}$). Pentacene has a strong inclination to form molecular crystals and when deposited by evaporation will typically form well-ordered films even for low substrate temperatures. For example, pentacene is deposited by evaporation at room temperatures can be obtained ordered films. For organic semiconductor, the well-ordered films are extremely important.

A more promising process to realize large area electronics is the thermal evaporation of organic material. The thermal evaporated material is poly crystalline with large grain sizes, usually in the range of a few microns. The mobility of polycrystalline transistors at room temperature can achieve the same range as amorphous silicon, is about 0.1-1 ㎝²/Vs.

1.4 Thesis Organization

In our work, the TEOS films that are deposited by atmospheric-pressure plasma technology (APPT) as gate dielectric layers of OTFT and we will use PECVD to do plasma treatment. Then pentacene films are deposited by a thermal evaporation system as active layers in OTFT. Last we will discuss the influence.

In chapter 1, we describe history of OTFT and motivation of our study. And we introduce to organic semiconductor and structure.

In chapter 2, we will introduce a new process, APPT, which can be operated under low temperature and atmospheric ambient. And APPT will make use of deposit dielectric layer SiO_2 for our experiment. We will treat the dielectric layer by PECVD and fabricate it on OTFT device.

In chapter 3, we compare the various methods of MIM fabrication and we select the best parameter to fabricate OTFT. Last we discuss the results.

In chapter 4, we will describe the conclusions and the future works.

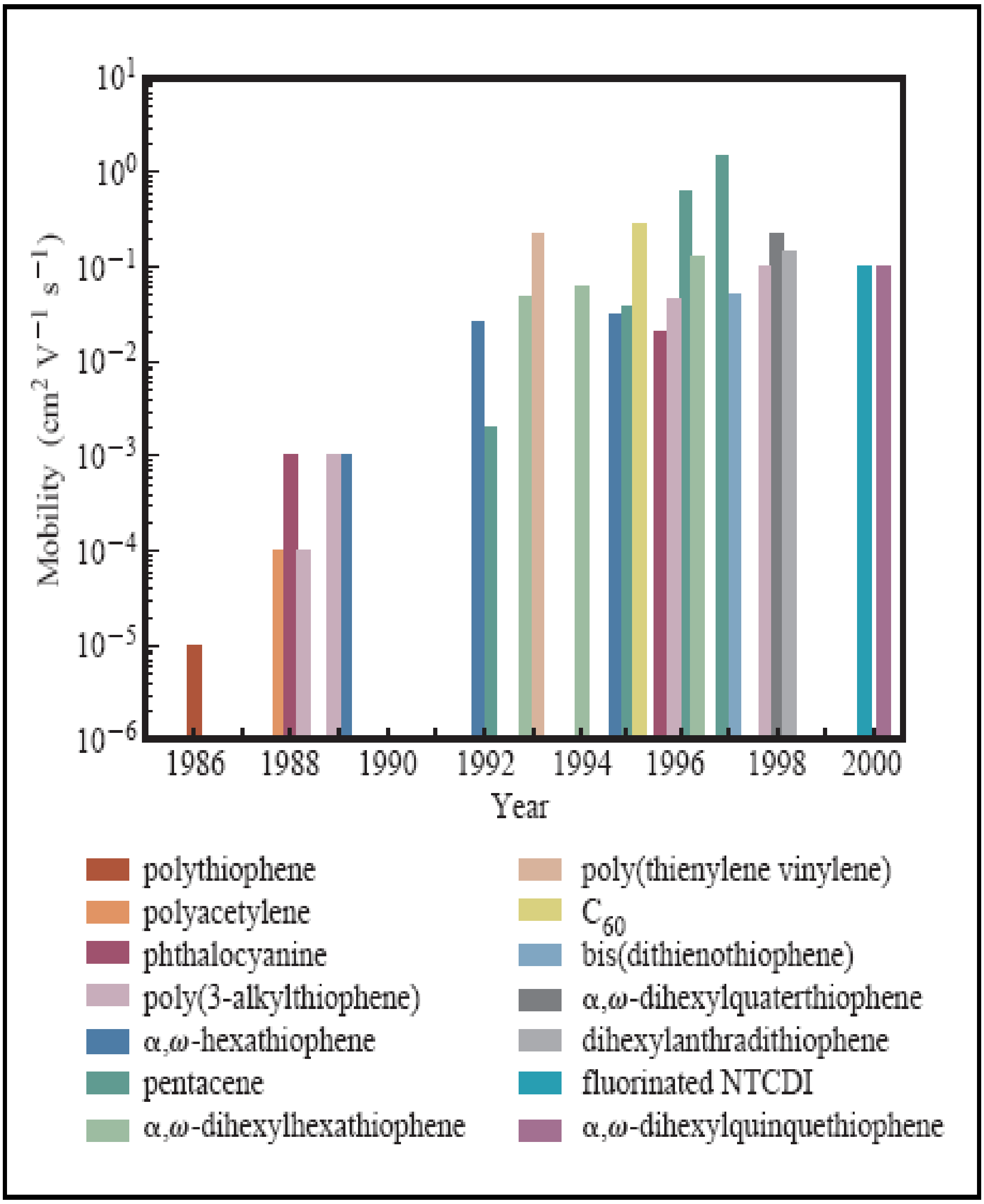
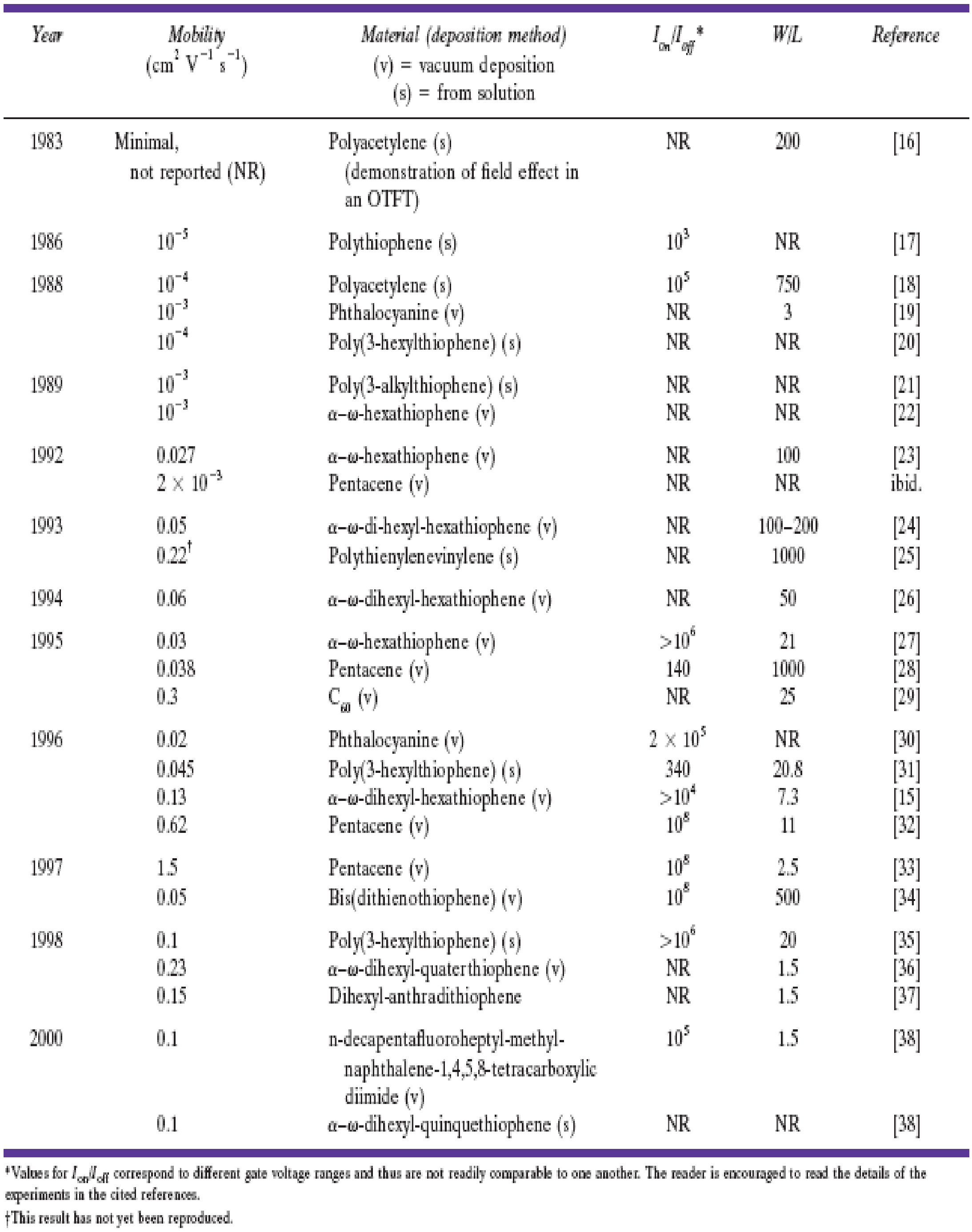


Figure 1-1 Semilogarithmic plot of the highest field-effect mobility(μ) Reported for OTFT fabricated from the most promising polymeric and oligomeric semiconductors versus year from 1986 to 2000[16]



Year	Mobility ($cm^2 V^{-1} s^{-1}$)	Material (deposition method) (v) = vacuum deposition (s) = from solution	I_{on}/I_{off}*	W/L	Reference
1983	Minimal, not reported (NR)	Polyacetylene (s) (demonstration of field effect in an OTFT)	NR	200	[16]
1986	10^{-5}	Polythiophene (s)	10^3	NR	[17]
1988	10^{-4}	Polyacetylene (s)	10^5	750	[18]
	10^{-3}	Phthalocyanine (v)	NR	3	[19]
	10^{-4}	Poly(3-hexylthiophene) (s)	NR	NR	[20]
1989	10^{-3}	Poly(3-alkylthiophene) (s)	NR	NR	[21]
	10^{-3}	α–ω-hexathiophene (v)	NR	NR	[22]
1992	0.027	α–ω-hexathiophene (v)	NR	100	[23]
	2×10^{-3}	Pentacene (v)	NR	NR	ibid.
1993	0.05	α–ω-di-hexyl-hexathiophene (v)	NR	100–200	[24]
	0.22†	Polythienylenevinylene (s)	NR	1000	[25]
1994	0.06	α–ω-dihexyl-hexathiophene (v)	NR	50	[26]
1995	0.03	α–ω-hexathiophene (v)	$>10^6$	21	[27]
	0.038	Pentacene (v)	140	1000	[28]
	0.3	C_{60} (v)	NR	25	[29]
1996	0.02	Phthalocyanine (v)	2×10^5	NR	[30]
	0.045	Poly(3-hexylthiophene) (s)	340	20.8	[31]
	0.13	α–ω-dihexyl-hexathiophene (v)	$>10^4$	7.3	[15]
	0.62	Pentacene (v)	10^8	11	[32]
1997	1.5	Pentacene (v)	10^8	2.5	[33]
	0.05	Bis(dithienothiophene) (v)	10^8	500	[34]
1998	0.1	Poly(3-hexylthiophene) (s)	$>10^6$	20	[35]
	0.23	α–ω-dihexyl-quaterthiophene (v)	NR	1.5	[36]
	0.15	Dihexyl-anthradithiophene	NR	1.5	[37]
2000	0.1	n-decapentafluoroheptyl-methyl-naphthalene-1,4,5,8-tetracarboxylic diimide (v)	10^5	1.5	[38]
	0.1	α–ω-dihexyl-quinquethiophene (s)	NR	NR	[38]

*Values for I_{on}/I_{off} correspond to different gate voltage ranges and thus are not readily comparable to one another. The reader is encouraged to read the details of the experiments in the cited references.

†This result has not yet been reproduced.

Table 1-1: Highest field-effect mobility(μ) values measured from OTFT as reported in the literature annually from 1986 through 2000[16].

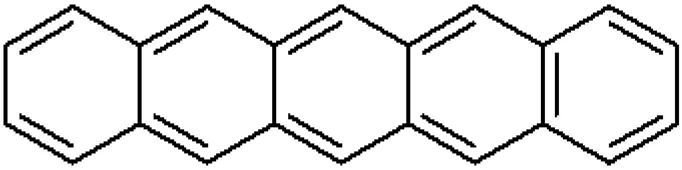
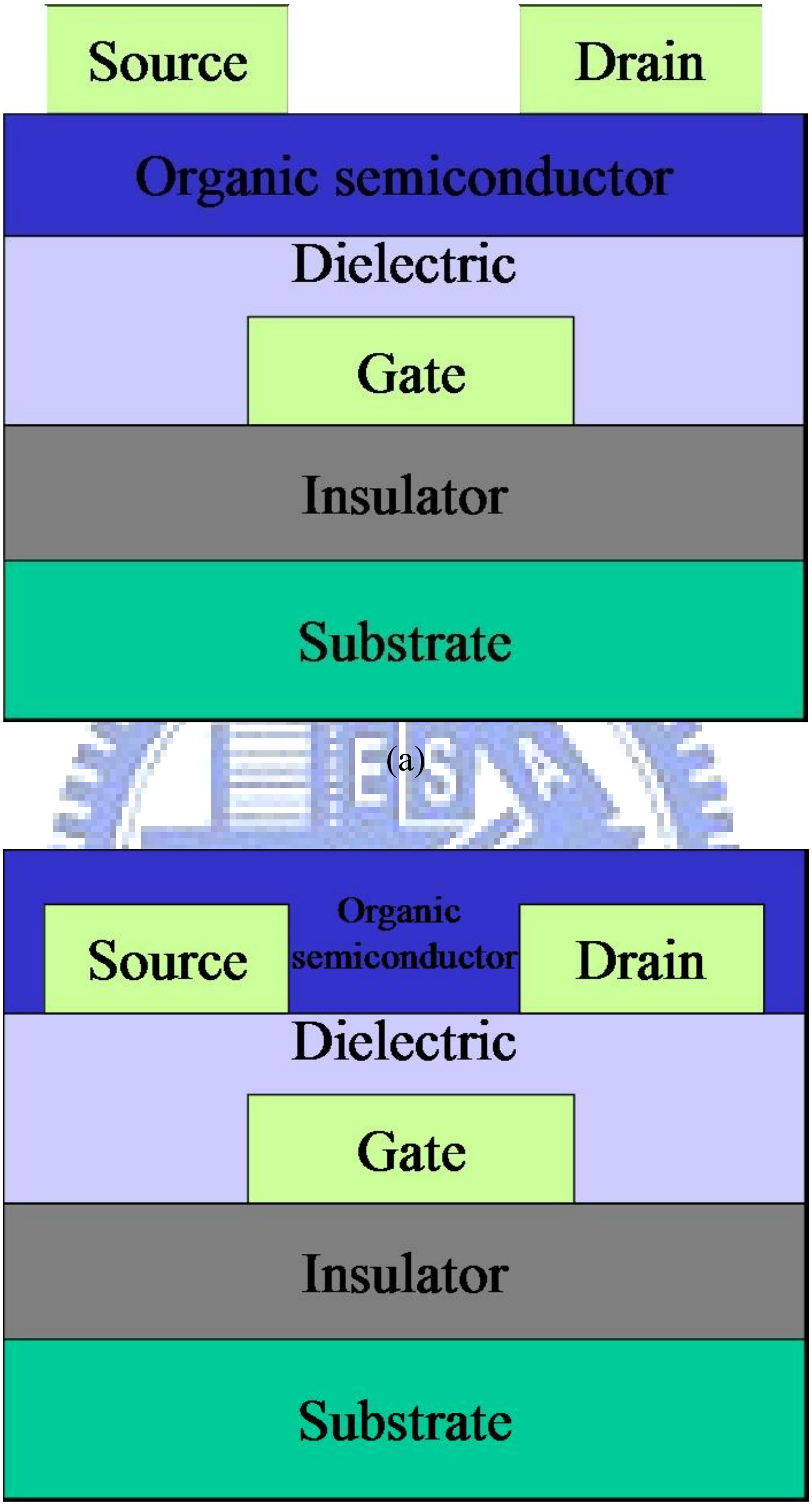


Figure 1-2 The Structure of Pentacene

Oligomer materials	Channel	Thin film deposition	Mobility (cm^2/V-s)	Comments
α-6T(α-hexathienylene)	p-type	Vacuum evaporation	0.01～0.03	Highly purified oligomers
α-6T	p-type		0.075	
DH-α-6T(dihexyl-α-6T)	p-type	Vacuum evaporation	0.03～0.05	Thermal annealing at 100～250℃
Pentacene	p-type	Vacuum evaporation	0.06～2.1	Substrate at T>25℃
Pentacene	p-type		10^{-5}～10^{-3}	
Pentacene	p-type		3.2	
C_{60}(fullerene)	n-type	Vacuum evaporation	0.08	
TCNQ (tetracyanoquinodimethane)	n-type	Vacuum evaporation	10^{-10}～10^{-4}	
NTCDA	n-type	Vacuum evaporation	1～3×10^{-3}	Substrate at T=25℃
PTCDA	n-type	Vacuum evaporation	10^{-5}～10^{-4}	
F_{16}CuPc	n-type	Vacuum evaporation	0.03	

Table 1-2: Thin film transistor performances for different oligomer active layers



(a)

(b)

Figure 1-3 (a) Cross section view of top contact structure of OTFT; (b) Cross section view of bottom contact structure of OTFT

Chapter 2
Experiment

2.1 Introduction of APPT

2.1.1 Introduction of plasma

Plasma can be described as a partially or wholly ionized gas with a roughly equal number of positively and negatively charged particles. Some scientists have called plasma the "fourth state of matter" because while plasma is neither gas nor liquid, its properties are like those of both gases and liquids.

High temperature plasma and low temperature plasma are two kind of plasma. The lightning is a good example of naturally occurring high temperature plasma. This type of plasma can be artificially generated using a high voltage, high temperature arc, which is the basis for the corona discharge process and for the plasma torch used to vaporize and redeposit metals. Low temperature plasmas, used in surface modification and organic cleaning, are ionized gases generated at pressures between 0.1 and 2 torr. Working within a vacuum chamber where atmospheric gases have been evacuated typically below 0.1 torr by these types of plasmas. Accelerated electrons and ions are allowed for a relatively long free path by low pressure. Since the ions and neutral particles are at or near ambient temperatures and the long free path of electrons, which are at high temperature or electron volt levels, have relatively few collisions with molecules at this pressure the reaction remains at low temperature.

2.1.2 Applications of APPT

The atmospheric-pressure plasma technology (APPT) is useful for treating and modifying the surface properties of organic and inorganic materials. The APPT apparatus does not require any vacuum systems, produces a high density plasma, and provides treatment of various substrates at low temperatures while operating open to the atmosphere. The plasma system has used for a wide variety of applications including treatment of polymer films, paper, wood, and foils; plasma grafting and plasma polymerization; ash various materials in the microelectronics industry; barrier layer deposition for the packaging industry; and sterilizing biologically contaminated materials. For polymer films, the technique offers the following advantages:

- Uniform treatment and No backside treatment.
- Improved surface energy with concomitant improved wettability, printability, and adhesion
- No additional vacuum system and low cost
- Continuous fabrication availably and high speed for production
- High plasma density

As shown in Figure 2-1 (a), we exhibited the atmospheric-pressure plasma system which was used in our experiment, and also showed the other atmospheric-pressure plasma systems in Figure 2-1 (b).

2.1.3 Surface treatment

The dielectric polarity is modified by the self-assembled monolayer (SAM) on inorganic dielectrics. Inorganic dielectrics with lower surface energy proffer improved device performance; such surfaces reduce many of interface traps in OTFTs [25,26]. However, it is an extra difficulty to control gate leakage [27]. As well as the increase in capacitance, it is an important factor for the surface polarity (hydrophilic or hydrophobic) of the gate dielectric [28]. However, the inorganic metal oxide dielectric with higher polarizability leads to the higher O-H group density on the interface and oppositely rough surface morphology. The formed O-H groups and the rough surface further affection the unprofitable quality of device performances. By this reason, the polymer-coating manner appears to be absolutely pervasive and thus could be used to any dielectric surface before organic semiconductor deposition [29~31]. In order to successfully integrate with OTFTs technology, there are a few important issues to be addressed, including degradation in channel mobility, charge trapping, and thermal stability.

2.1.4 Surface modification by plasma

Figure 2-2 shows the mechanisms of plasma surface modification, a glow discharge plasma is created by evacuating a reaction chamber and then refilling it with a low-pressure gas. The gas is then energized by one of the following types of energy: radio frequency, microwaves, and alternating or direct current. The energetic species in gas plasma include ions, electrons, radicals, metastables, and photons in the short-wave ultraviolet (UV) range. Surfaces in contact with the gas plasma are bombarded by these energetic species and their energy is transferred from the plasma to the solid. These energy transfers are dissipated within the solid by a variety of chemical and physical processes to result in a unique type of surface modification that reacts with surfaces in depths from several hundred angstroms to 10μm without changing the bulk properties of the material.

A wide variety of parameters can greatly affect the physical characteristics of plasma and subsequently affect the surface chemistry obtained by plasma modification. Processing parameters, such as gas types, treatment power, treatment time and operating pressure, can be varied by the user; however system parameters, such as electrode location, reactor design, gas inlets and vacuum are set by the design of the plasma equipment. This broad range of parameters offers greater control over the plasma process than that offered by most high-energy radiation processes.

Plasma treatment is aiming for various goals as for example:

- Improved adhesion
- Removal of the "water skin"
- Activation of the substrate surface
- Modification of the substrate surface
- Cleaning of substrate surfaces

Since the organic film of OTFT is fabricated on to the dielectric layer under the influence of the physical and chemical interactions between organic and dielectric layer, the OTFT performance strongly depends on the semiconductor/dielectric interface. The purpose of this work is to show the improvement of OTFT performance by controlling the surface treatments of dielectric/polymer interface. The surface properties such as frictional or abrasion, permeability, insulating properties, wettability and chemical reactivity are strongly dependent on a molecular aggregation state of the surface [32,33]. Therefore, the control of a molecular aggregation state in the film is important to construct a highly functionalized surface. One of the most effective ways of studying surface properties is contact angle measurement. The contact angle is the angle between the tangent to the drop’s profile and the tangent to the surface at the interaction of the vapor, the liquid, and the solid. The contact angle is an index of the wettability of the solid surface. A low contact angle between solid surface water-drop indicates that the surface is hydrophilic and has a high surface energy. On the contrary, a high contact angle means that the surface is hydrophobic and has a low surface energy. The surface free energy was traditionally quantified by contact angle measurements [34,35].

2.2 Operation of organic thin film transistors

Mode (I): When zero bias is applied to three electrodes of OTFT. The schematic diagram is shown in Figure 2-3 (a), it is called cut-off. If applied a small drain bias, Vd, and the source-current, Ids, will be small and ohmic.

Mode (II): When a positive bias applied, the bend bending will occur in the interface between dielectric layer and semiconductor layer. Negative charges will locate at interface and form the depletion region. The schematic diagram is shown in Figure 2-3 (b). The channel resistance is so large that the current will smaller than that of mode (I). Because of the large band gap, inversion layer cannot be observed in the organic thin-film transistor.

Mode (III): When gate bias is negative, the schematic diagram is shown in Figure 2-3 (c), the voltage is dropped over the insulator and over the semiconductor near the interface between dielectric layer and semiconductor layer. More positive charges will be accumulated in the accumulate region. When a small bias is applied to drain, the source-drain current will be larger than that of Mode (I), the schematic diagram is shown in Figure 2-3 (d).

Mode (IV): When drain voltage is negative enough that the voltage difference of gate and drain, Vgd, which is lower than Vth(<0), therefore, the depletion region will form near drain and pitch-off (Figure 2-3(e)). If drain voltage is more negative, the depletion region will grow and approach source. The schematic diagram is shown in Figure 2-3 (f).

2.3 Affect to capacitance of different conditions

2.3.1 Silicon oxide deposited by APPT on the metal insulator metal (MIM) structure and relation with flow of APPT

In this section, we are resolution to deposit silicon oxide dielectric on the bottom contact electrode metal by atmospheric-pressure plasma technology with different flows. But silicon oxide is not deposited on the metal at room temperature. Accordingly, we heat the bottom of n^+-Si substrate and enable TEOS to be deposited on the metal.

First, an n-type bare silicon wafer is cleaned by the standard RCA cleaning process. An insulating layer of silicon dioxide is grown by thermal oxidation (wet oxidation) 34min at 1000℃ for isolation purpose. The thickness of silicon dioxide is 3040 Å measured by n&k system. And deposited 300 nm aluminum as the bottom electrode. Heats up the Tetraethoxy silane (TEOS) to 180℃ was injected by nitrogen (50%) and oxygen (50%) as carrier gases which is the deposition source of silicon oxide. Silicon oxide is deposited on the top of aluminum metal gate at room temperature under an atmospheric-pressure with the plasma power is established around 50 W with an appropriate scanning rate (cycle). Silicon oxide is deposited on the aluminum thin film by atmospheric-pressure plasma technology (APPT) with varied flow (0.1sccm, 1sccm and 5sccm respectively). We adopt 60 times and heat 150 ℃ in the substrate parameters to compare with different flow of APPT.

Finally, all top contact electrodes are deposited 300 nm thick aluminum layer defined with shadow mask by thermal coater system. The active region pad of all capacitors is diameter 200 μm. The process flow is shown in Figure 2-4.

2.3.2 Silicon oxide deposited by APPT on the metal insulator metal (MIM) structure and relation with different metal gates

In this section, we are resolution to deposit silicon oxide dielectric on the bottom contact electrode metal by atmospheric-pressure plasma technology with different metal gate. But silicon oxide is not deposited on the metal at room temperature. Accordingly, we heat the bottom of n^+-Si substrate and enable TEOS to be deposited on the metal.

First, an n-type bare silicon wafer is cleaned by the standard RCA cleaning process. An insulating layer of silicon dioxide is grown by thermal oxidation (wet oxidation) 34min at 1000℃ for isolation purpose. The thickness of silicon dioxide is 3040Å measured by n&k system. And deposited 30 nm different metals (Al(300nm), Ni, Pd, Ir, TaN) and different temperature of substrate as the bottom electrode. Heats up the Tetraethoxy silane (TEOS) to 180℃ is injected by nitrogen (50%) and oxygen (50%) as carrier gases which is the deposition source of silicon oxide. Silicon oxide is deposited on the top of different metal gate at room temperature under an atmospheric-pressure with the plasma power is established around 50 W with an appropriate scanning rate (sccm /cycle). We adopt 60 times and flow 0.1 sccm and heat 100, 150 and 200 ℃ in the substrate parameters to compare with different metal gates.

Finally, all top contact electrodes are deposited 300 nm thick aluminum layer defined with shadow mask by thermal coater system. The active region pad of all capacitors was diameter 200 μm. The process flow rate is shown in Figure 2-5.

Additional we used atomic force microscope (AFM) to observe the surface morphology.

2.3.3 Plasma treatment of silicon oxide deposited by APPT on the metal insulator metal (MIM) structure

In this section, we are resolution to try plasma treatment for silicon dioxide dielectric which is deposited by APPT. First, an n-type bare silicon wafer is cleaned by the standard RCA cleaning process. An insulating layer of silicon dioxide is grown by thermal oxidation (wet oxidation) 34min at 1000℃ for isolation purpose. The thickness of silicon dioxide is 3040Å measured by n&k system. And we deposited 30nm nickel as the bottom electrode. Heats up the Tetraethoxy silane (TEOS) to 180℃ was injected by nitrogen (50%) and oxygen (50%) as carrier gases which is the deposition source of silicon oxide. Silicon oxide is deposited on the top of nickel metal gate at room temperature under an atmospheric-pressure with the plasma power is established around 50 W with an appropriate scanning rate (sccm/cycle). Silicon oxide is deposited on the nickel thin film by atmospheric-pressure plasma technology (APPT) with 0.1 sccm and 60 times.

Then we use PECVD to do plasma treatment. The plasma power is established around 20 W and the treatment pressure is 68 Pa. We use of N_2 and NH_3 and to do plasma treatment. We divide two stages into the step. First, we regular the treatment time (1min) then change the gas quantity (50, 100, 200 and 400 sccm). Second, we select the better treatment flow then change the treatment time (0.5, 1, 2 and 4 min).

Finally, all top contact electrodes are deposited 30 nm thick nickel layer defined with shadow mask by Dual E-Gun system. The active region pad of all capacitors was diameter 200 μm. The process flow is shown in Figure 2-6.

In order to further analyze the phenomenon about surface treatment, we used atomic force microscope (AFM) to observe the surface morphology. Contact angle was measured to judge the surface state. We use SEM to measure the films thickness.

2.4 Fabrication of OTFT

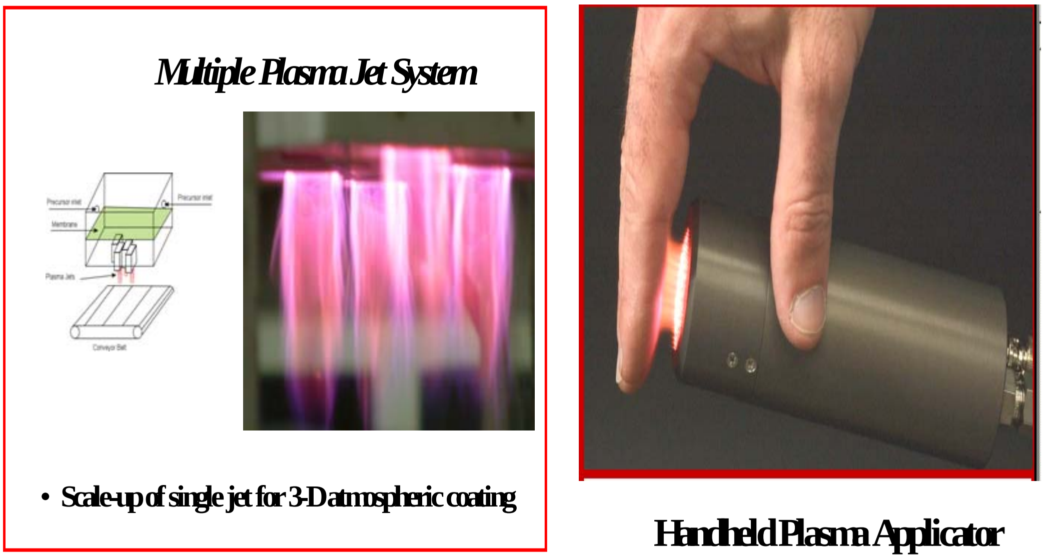
In this section, for a start, we are resolution to choose nickel as gate in our experiment. Subsequently, silicon oxide is deposited by 0.1 sccm and 60 times of APPT. After we deposit the insulator, we choose the best plasma treatment parameter to treat the gate dielectric layers.

First, an n-type bare silicon wafer is cleaned by the standard RCA cleaning process. An insulating layer of silicon dioxide is grown by thermal oxidation (wet oxidation) 34min at 1000℃ for isolation purpose. The thickness of silicon dioxide is 3040Å measured by n&k system. And deposit 30 nm thick nickel layer as the gate electrode. The nickel layer is deposited by Dual E-Gun and silicon oxide deposited by atmospheric-pressure plasma technology (APPT) at 200℃ under an atmospheric pressure with 0.1 sccm scanning 60 times is used as gate insulator. Then we use thermal coater to deposit 30 nm thick gold as source/drain electrodes. Pentacene is evaporated by thermal coater as active layer in our study. The channel length, L, is 100 μm and width, W, is 2000 μm. During deposition of pentacene active layer, the substrate is heated to 70℃ at power 17 W at a pressure chamber of around 1x10^{-6} Torr. The process flow is shown in Figure 2-7.

2.5 Characteristic measurement of devices

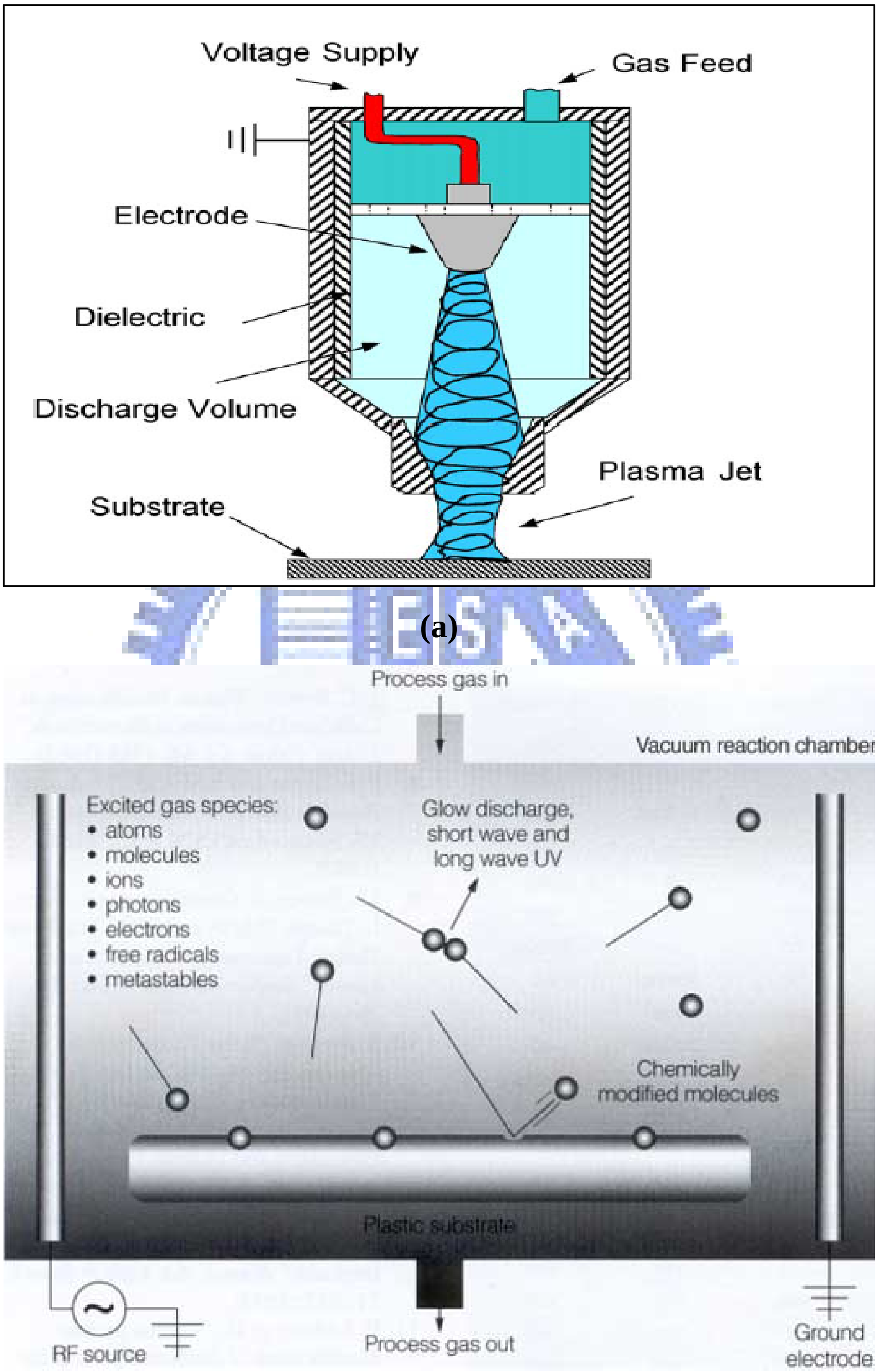
We use HP 4284A precision LCR meter parameter to analyze Capacitance-Voltage (C-V) characteristic diagrams at 1MHz and the characteristic curves of Current-Voltage (I-V) are measured with semiconductor parameter analyzer by HP 4156. We measure all measurements are at room temperature in an air atmosphere.

(a)



(b)

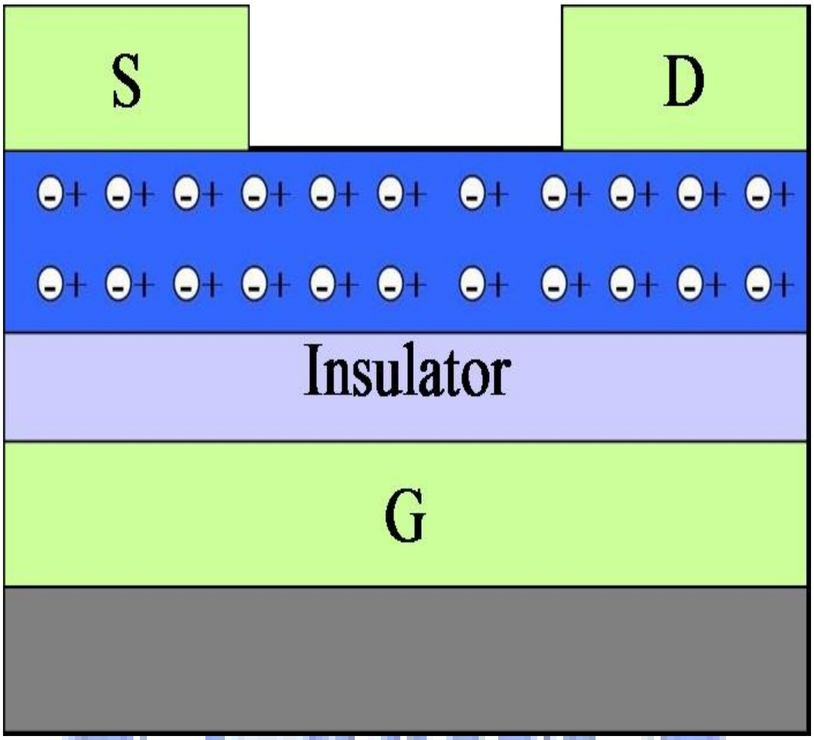
Figure 2-1 (a) APP system of ITRI (b) the other APP systems



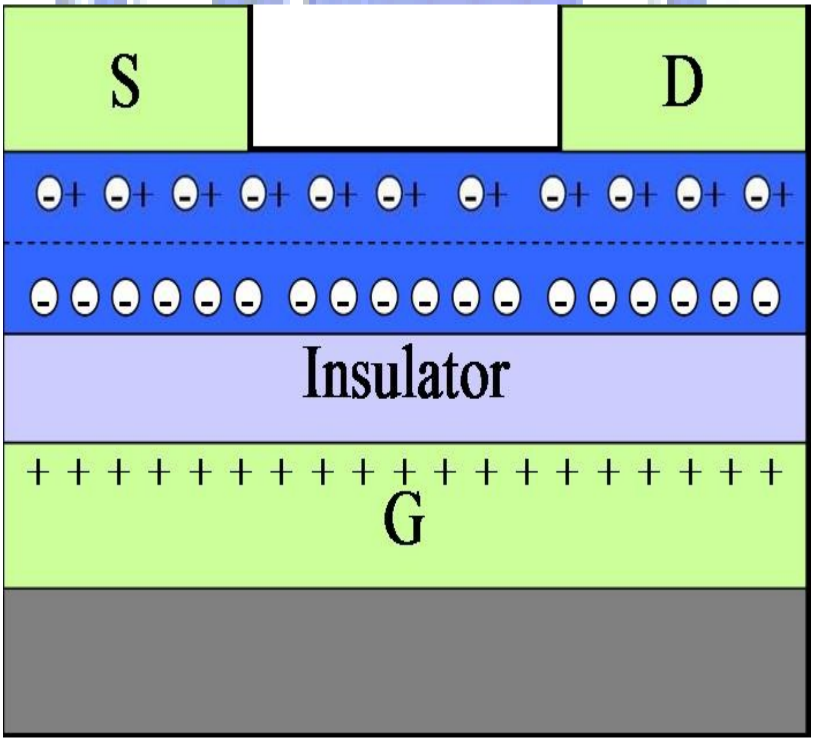
(a)

(b)

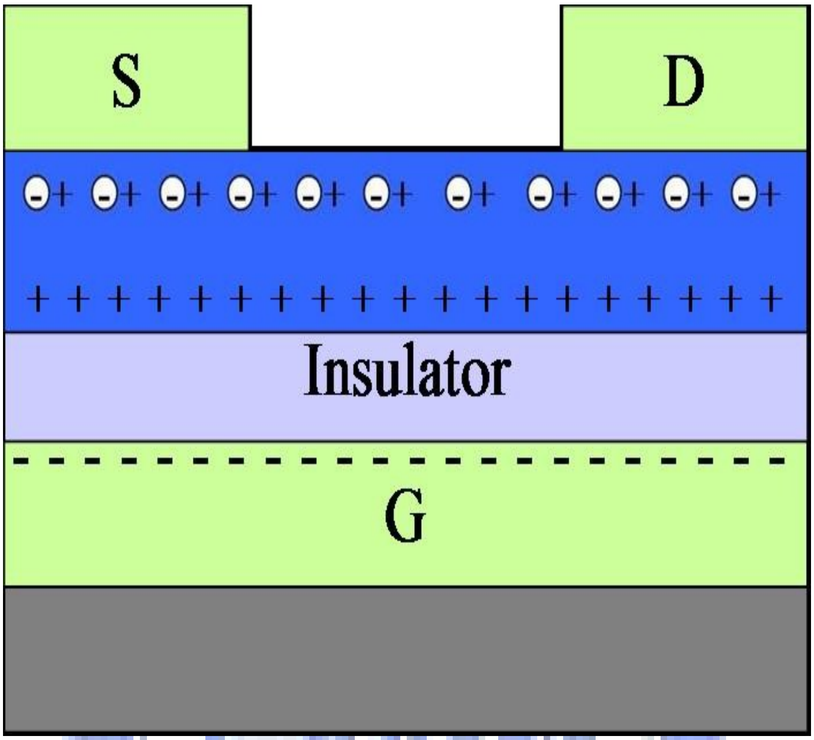
Figure 2-2 (a)The structure of APPT (b)The diagram of plasma surface treatment



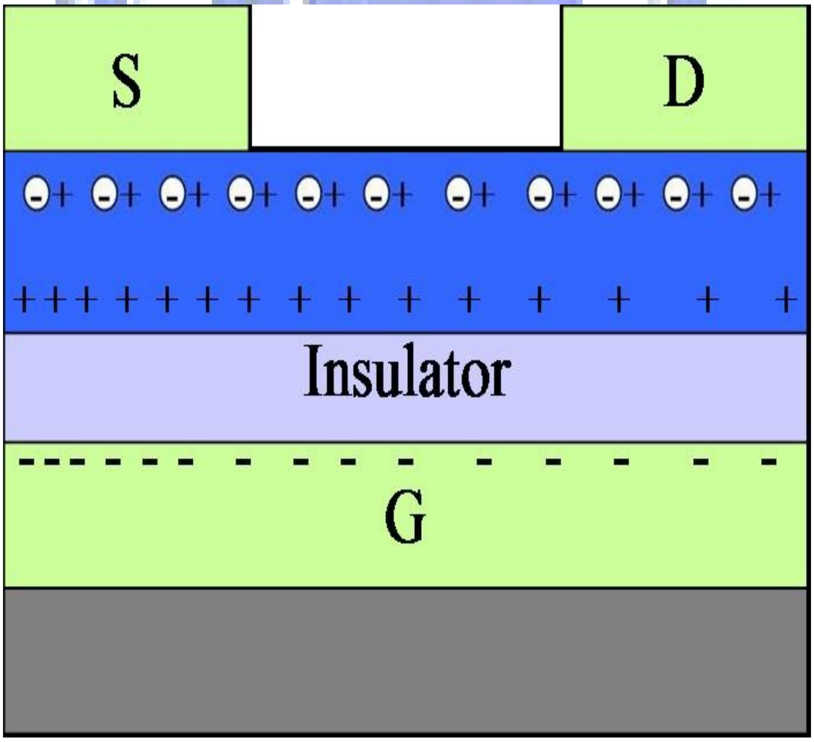
(a) Vg = Vs = Vd = 0



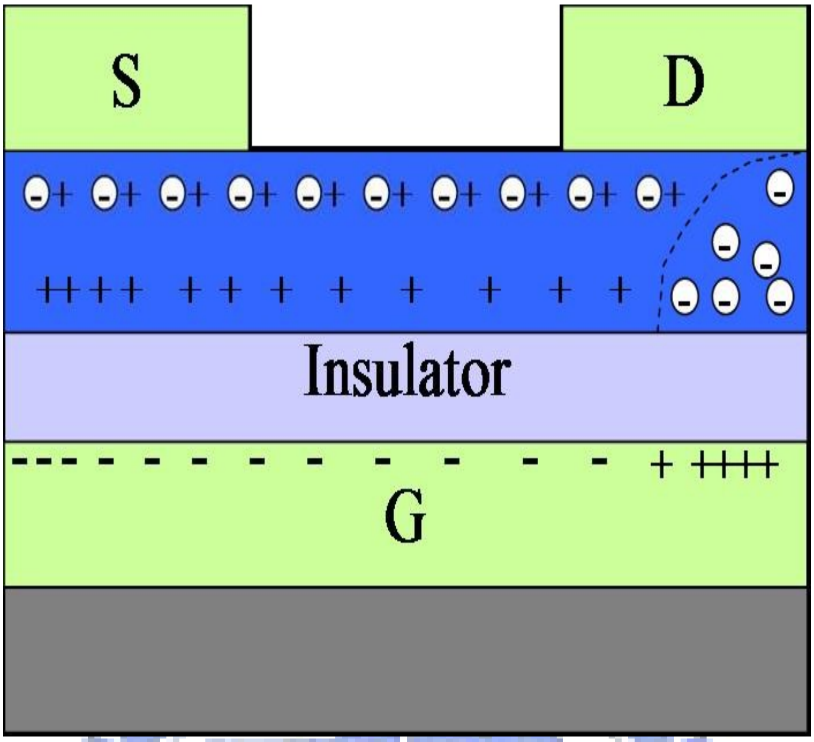
(b) Vs = Vd = 0, Vg > 0



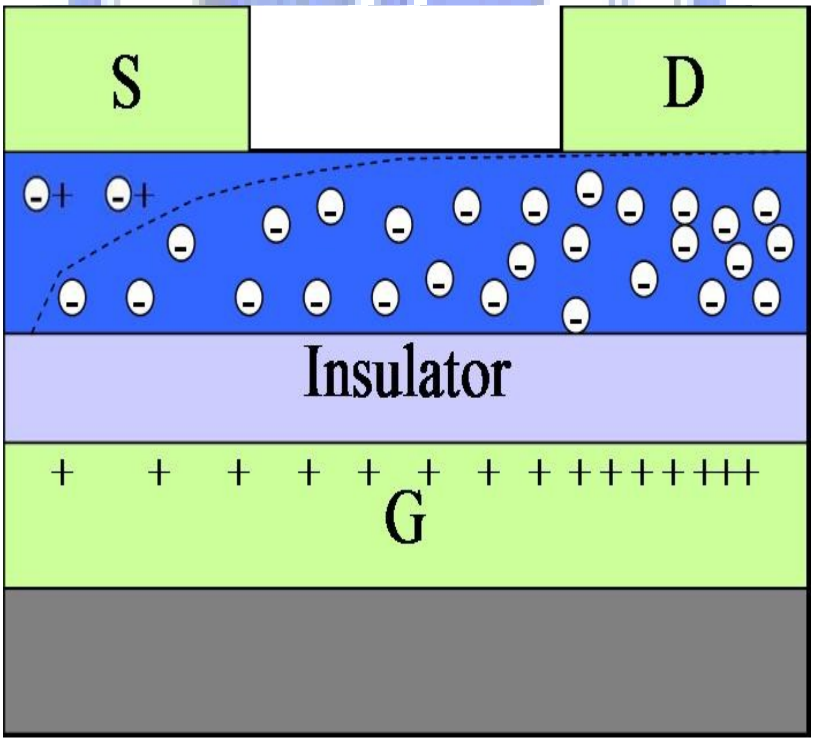
(c) Vs = Vd = 0, Vg < 0



(d) Vs =0, Vg < Vd < 0

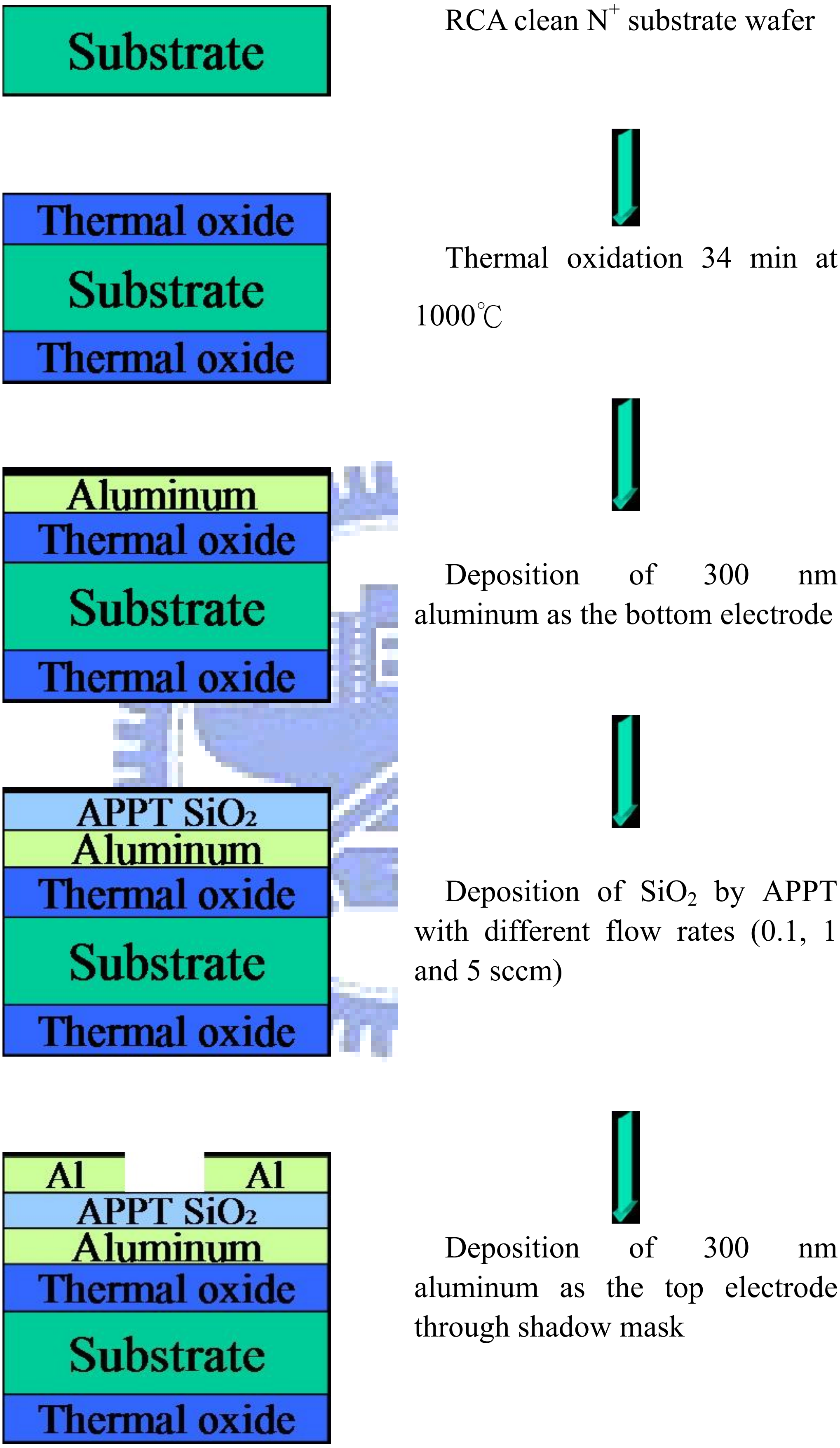


(e) Vs =0, Vd < Vg < 0



(f) Vs = Vg = 0, Vd < 0

Figure 2-3 Schematic of operation of organic thin film transistor, showing a lightly doped semiconductor; + indicates a positive charge in semiconductor; - indicates a negatively charge in semiconductor. (a) No-bias; (b) Depletion mode; (c) Accumulation mode; (d) Non-uniform charge density; (e) Pinch-off of channel; (f) Growth of the depletion zone



RCA clean N^+ substrate wafer

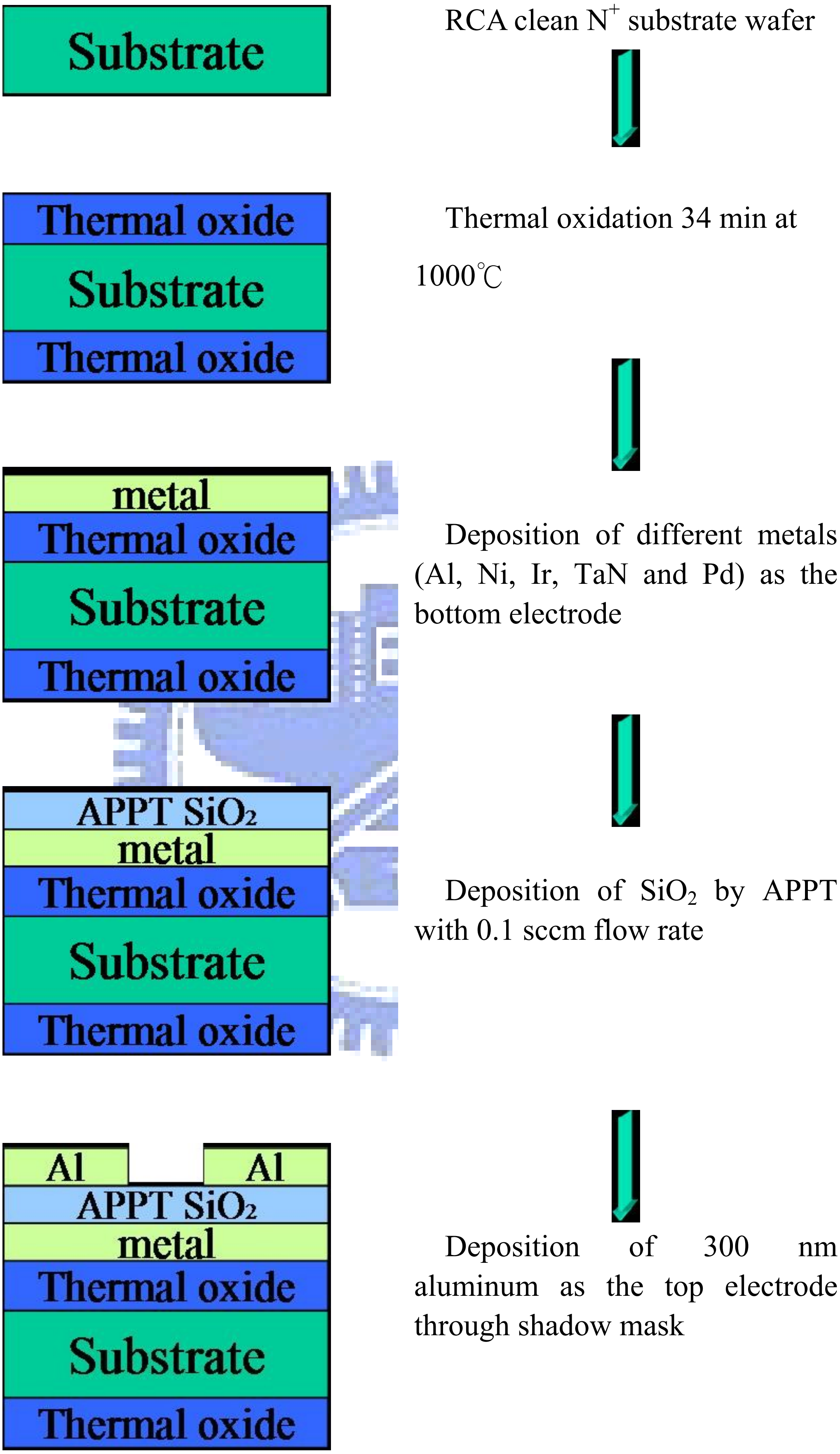
Thermal oxidation 34 min at 1000℃

Deposition of 300 nm aluminum as the bottom electrode

Deposition of SiO_2 by APPT with different flow rates (0.1, 1 and 5 sccm)

Deposition of 300 nm aluminum as the top electrode through shadow mask

Figure 2-4 The MIM structure of different APPT flow rates



RCA clean N^+ substrate wafer

Thermal oxidation 34 min at 1000℃

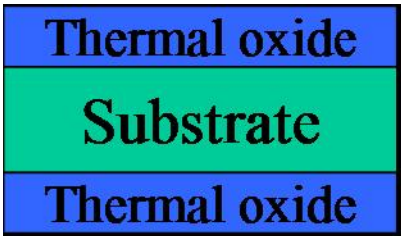
Deposition of different metals (Al, Ni, Ir, TaN and Pd) as the bottom electrode

Deposition of SiO_2 by APPT with 0.1 sccm flow rate

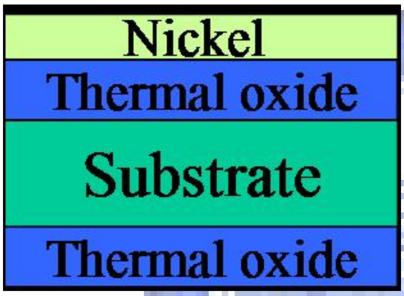
Deposition of 300 nm aluminum as the top electrode through shadow mask

Figure 2-5 The MIM structure of different metal gates

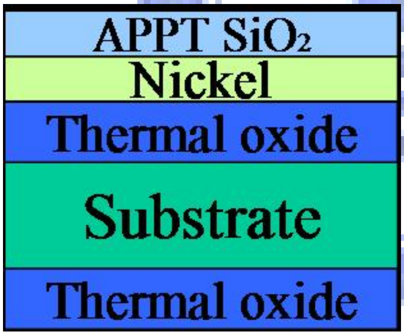
RCA clean N^+ substrate wafer



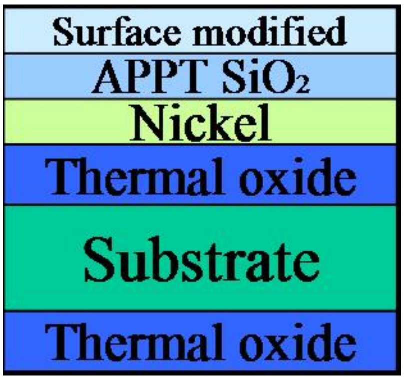
Thermal oxidation 34 min at 1000℃



Deposition of nickel as the bottom electrode

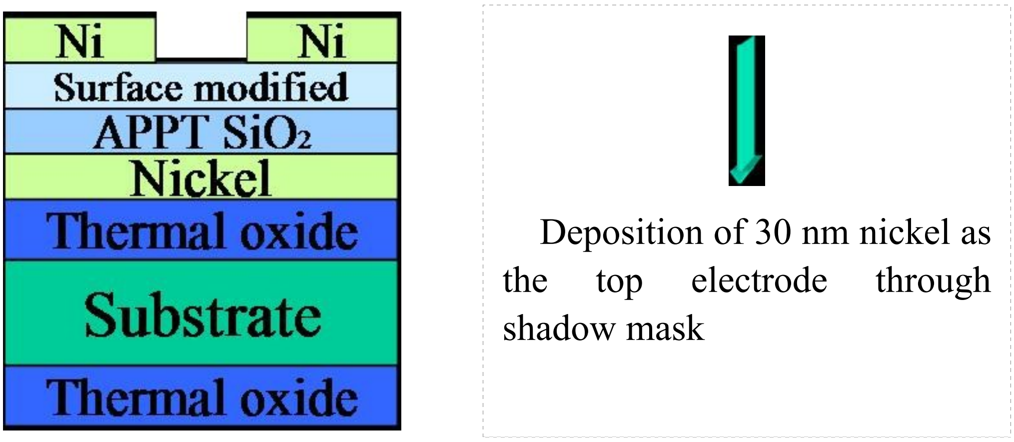


Deposition of SiO_2 by APPT with 0.1sccm flow rate 60 times



Surface treatment:

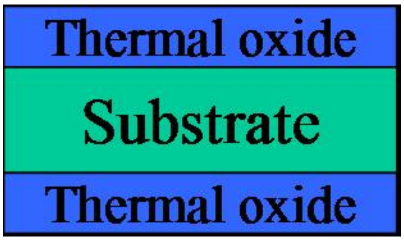
1. N_2 plasma
2. NH_3 plasma



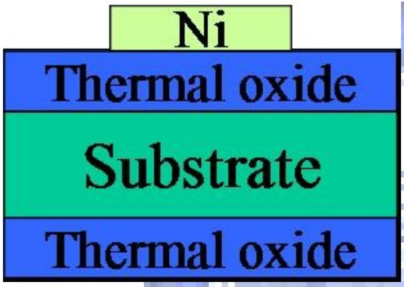
Deposition of 30 nm nickel as the top electrode through shadow mask

Figure 2-6 The MIM structure of plasma treatment dielectric gate

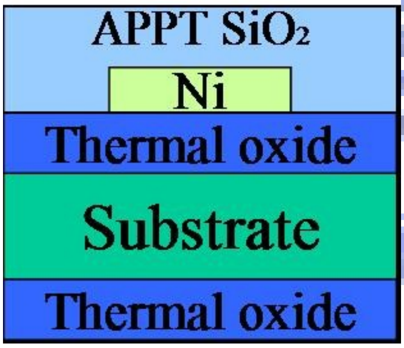
RCA clean N^+ substrate wafer



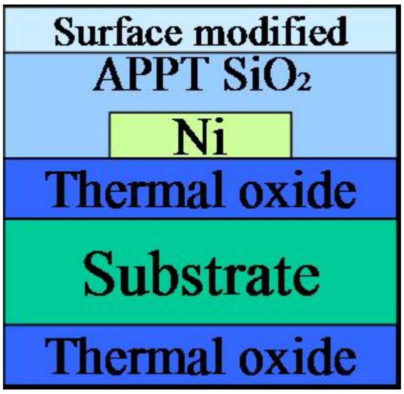
Thermal oxidation 34 min at 1000℃



Deposition of 30 nm nickel as the gate electrode

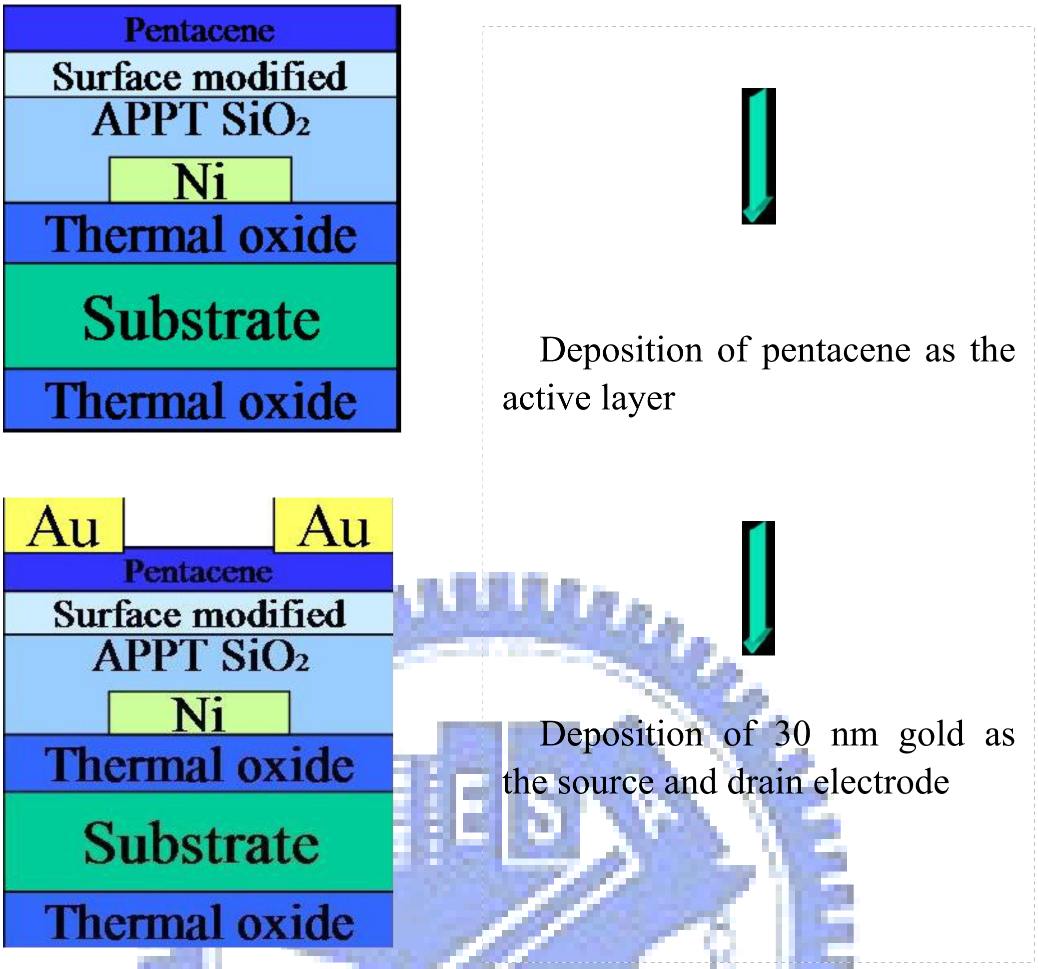


Deposition of SiO_2 by APPT with 0.1sccm flow rate 60 times



Surface treatment:

1. N_2 plasma
2. NH_3 plasma



Deposition of pentacene as the active layer

Deposition of 30 nm gold as the source and drain electrode

Figure 2-7 The OTFT structure

Chapter 3
Results and Discussion

3.1 Determination of threshold voltage and mobility

The linear regime field effect mobility can be obtained by the calculation described below. At low V_D, I_D increases linearly with V_D (linear regime) and is approximately determined by the following equation:

$$I_D = \frac{W\mu_n C_{ox}}{2L}\left[2(V_G + V_T)V_D - V^2{}_D\right] \qquad \textbf{(3-1)}$$

where L is the channel length, W is the channel width, C_{ox} is the capacitance per unit area of the insulating layer, V_T is the threshold voltage, and μ is the field effect mobility, which can be calculated in the linear regime from the transconductance,

$$G_m = \frac{\partial I_D}{\partial V_G} = \frac{Z}{L}\mu_n C_{ox} V_D \qquad \textbf{(3-2)}$$

by plotting I_D versus V_G at a constant low V_D, with $-V_D <<-(V_G - V_T)$, and equating the value of the slope of this plot to Gm, then find Gm,max which can gain the value of threshold voltage (V_T) and linear mobility. For the known values included C_{ox}, $V_{T,}$ and W/L, the value of saturation mobility can be obtained from equation (3-3)

$$I_D(sat) = \frac{W\mu_n C_{ox}}{2L}(V_G + V_T)^2 \qquad \textbf{(3-3)}$$

3.2 Result of different conditions

3.2.1 The influence of different flow rates

In our experiments, we try to test the different flow rates of APPT and discuss their influence. There are three different flow rates of APPT which 0.1, 1, and 5 sccm are used in our experiment. The other detail process will be not repeated in this section. Silicon oxide is deposited by APPT on the bottom electrode surface with different flow rates of APPT at substrate temperature at 150℃. The I-V and C-V characteristic is shown in Figure 3-1**.** The horizontal axis and vertical axis of Figure 3-1 (a) represent the swept voltage set and the value of capacitance respectively. We can see the values of capacitor from Figure 3-1 (a) is influenced by the flow of APPT. We can know from the Figure 3-1 (a) the flow of carrier gases will influence the quantity that the TEOS gas comes out. The flow of carrier gases increases and leads to the fact the coming out amount of TEOS gas to increase.

To summarize this section, we would choose 0.1 sccm as our optimal parameter. The leakage current density of 0.1 sccm is minimum and the breakdown voltage is maximum between the three deposition flow rates of APPT.

3.2.2 The influence of different metal gates

In our experiments, we try to test the different metal gates and discuss their influence. There are five different metal gates which Al, Ni, Ir, TaN and Pd are used in our experiment. The other detail process will be not repeated in this section. Silicon oxide is deposited by APPT on the bottom electrode surface with different metal gates at substrate temperature at 100, 150 and 200℃. The I-V and C-V Characteristic is shown in Figure 3-2 ~ Figure 3-7**.** The horizontal axis and vertical axis of Figure 3-2(a) ~ Figure 3-7(a) represent the swept voltage set and the value of capacitance respectively. We can learn from the Figure 3-7 that different metal gate under the same conditions of APPT depositing have different results. The leakage current and capacitor are influenced by different metal gates.

Additional measured values such as surface roughness also are shown in Table 3-1. The roughness of Al, Ni, TaN, Ir and Pd gate electrode is about 8.724, 0.663, 1.132, 0.706 and 1.582 nm (the corresponding AFM analysis), the roughness of the silicon oxide deposited by APPT on the top of Al, Ni, TaN, Ir and Pd gate electrode with substrate temperature at 100, 150 and 200℃ is around 10.895, 9.937, 8.601; 11.695, 3.778, 1.950; 6.421, 3.882, 2.090; 18.422, 4.134, 3.013; 3.093, 2.075, 2.467 nm (see Figure 3-8 ~ Figure 3-12). Figure 3-13 shows the trend of surface roughness with increasing the substrate temperature.

To summarize this section, we would choose Ni as our optimal parameter. The leakage current density of Ni metal gate is minimum. Relatively other metal, the depositing of TEOS is easy at Ni, so the same TEOS amount can be deposited smooth. Ni relatively accords with the economic benefits.

3.2.3 The influence of plasma treatment

In our experiments, we try to test the plasma treatment and discuss their influence. There are two different plasma treatments which N_2, and

NH_3 are used in our experiment. The other detail process will be not repeated in this section. Silicon oxide is deposited by APPT on the bottom electrode surface with 0.1 sccm of APPT at substrate temperature at 200℃.

We regular the treatment time at the first stage. The I-V and C-V characteristic is shown in Figure 3-14 ~ Figure 3-15. The horizontal axis and vertical axis of Figure 3-14 (a) ~ Figure 3-15 (a) represent the swept voltage set and the value of capacitance respectively. We can know from the Figure 3-14 (b) ~ Figure 3-15 (b) that the influence of plasma flow on leakage current is transparent.

And we change the treatment time at the second stage. The I-V and C-V characteristic Figure 3-16 ~ Figure 3-17. The horizontal axis and vertical axis of Figure 3-16 (a) ~ Figure 3-17 (a) represent the swept voltage set and the value of capacitance respectively. We can know from the Figure 3-16(b) ~ Figure 3-17 (b) and Figure 3-18 that the influence of treatment time on leakage current is conspicuousness.

We select the best parameter to measure their surface roughness, contact angle and the film thickness. This best parameter respectively is N_2 plasmas treatment 0.5 minute with 50 sccm, NH_3 plasmas treatment 0.5 minute with 50 sccm.

Additional measured values such as surface roughness, contact angle and the film thickness also are shown in Table 3-2. The roughness of no, N_2, NH_3, plasma treatment is around 1.246, 1.190, 1.089 nm (see Figure 3-19). The film thickness measured by SEM and the contact angle is shown in Figure 3-20. Causing the contact angel becomes small reason, it is probably to the organic impurity on surface is removed by plasma treatment (see Figure 3-21) [36,37]. And Figure 3-22 shows the film thickness.

To summarize this section, we can know from the Figure 3-16 (a) ~ Figure 3-17 (a) and Table 3-2 to calculate the permittivity of no、N_2、NH_3 treatment is 4.06、3.75、3.70. We may see that plasma treatment have the effect to reduce leakage current. So we can select the best plasma treatment parameter to fabricate OTFT device.

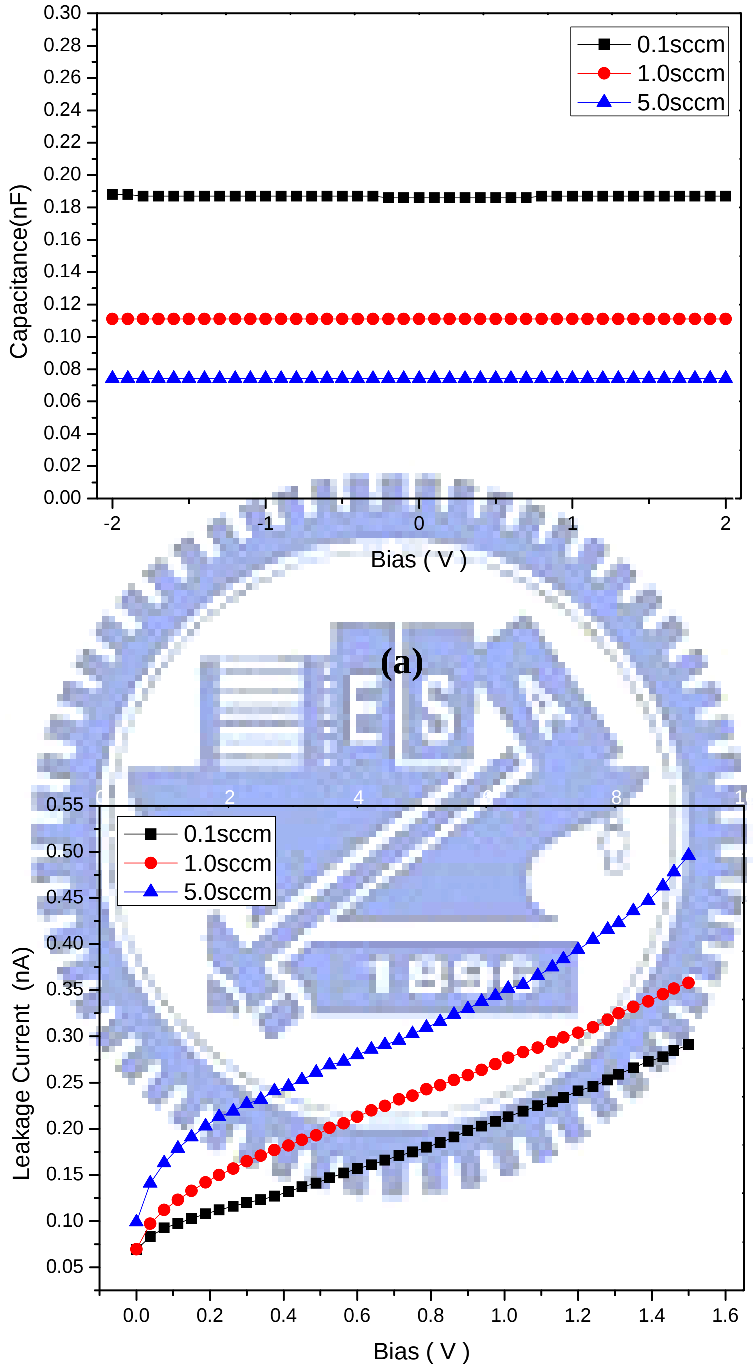
3.3 Analysis and discussion OTFT electric characteristics

Here we focus on the influence of plasma treatment under varied conditions which have different gas of PECVD. They are N_2, NH_3 and no treatment respectively.

As shown from Figure 3-23 to Figure 3-25, design of drain current I_D versus gate voltage V_D at various drain voltage V_G, drain current I_D versus gate voltage V_G at various drain voltage V_D and drain current I_D versus radical gate voltage V_G at various drain voltage V_D with different plasma treatments.

In all figures of different treatment conditions, we can observe that no treatment has best electrical characteristic about I_D-V_G and NH_3 treatment has best electrical characteristic about I_D-V_D. Additionally, we plot the comparison of I_D-V_D , I_D-V_G and $|I_D|^{1/2}$-V_G in the same figure due to observe clearly, they are shown in Figure 3-26. The magnitude of current at the same operating voltage, NH_3 > no > N_2 . Besides, threshold voltage and mobility would be calculated by taking measured data into **Eq.(3-1) ~ (3-3)**. Arrangement of threshold voltage, mobility and on/off ratio is shown in Table 3-3 (labeled as no treatment, N_2 and NH_3) and Figure 3-27. The mobility in the saturation region and the threshold voltage and on/off ratio of the OTFT are 0.72 cm^2/Vs and -0.616 V and ~10^3, respectively.

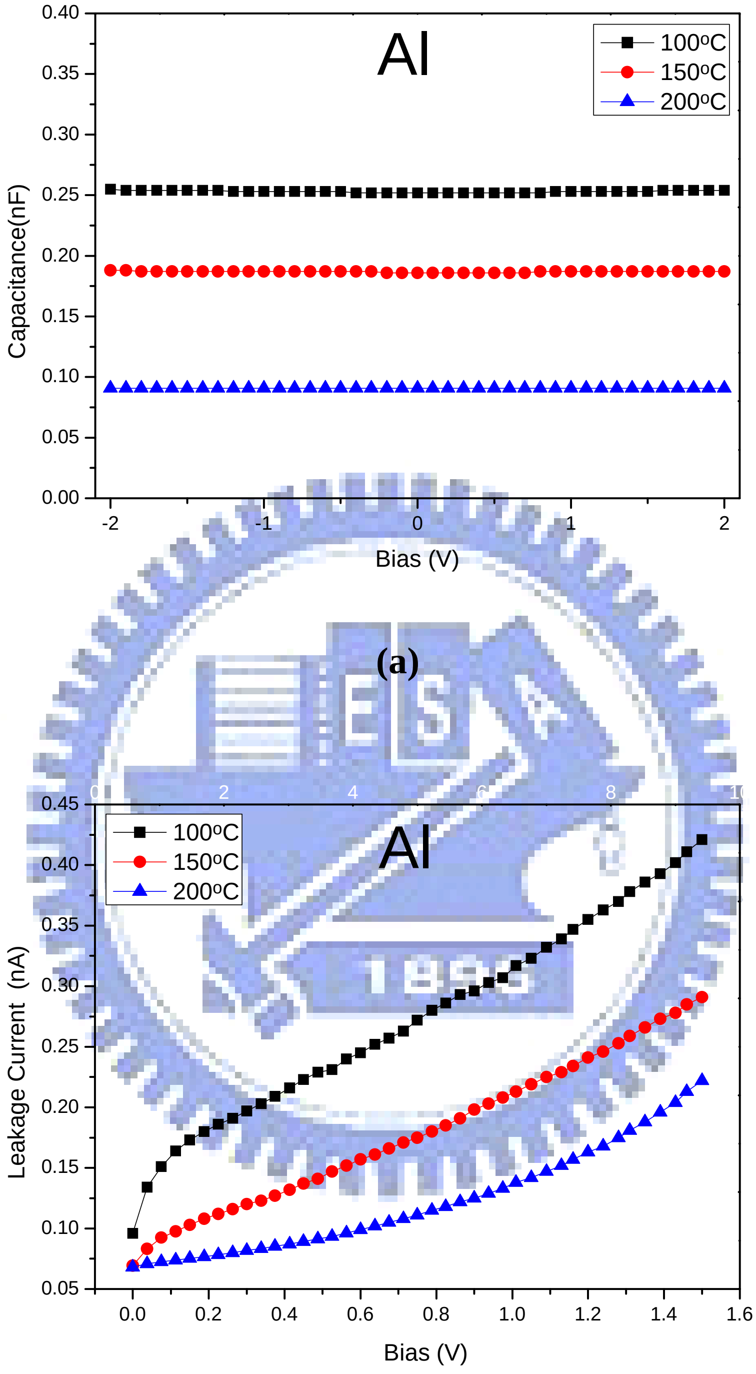
To summarize this section, we can know from the experiment the atmospheric-pressure plasma technology silicon dioxide is worth studying. The advantage of the atmospheric-pressure plasma technology is that it needn't vacuum and at general room temperature to deposit insulator. This advantage is an asset condition to fabricate OTFT.



(a)

(b)

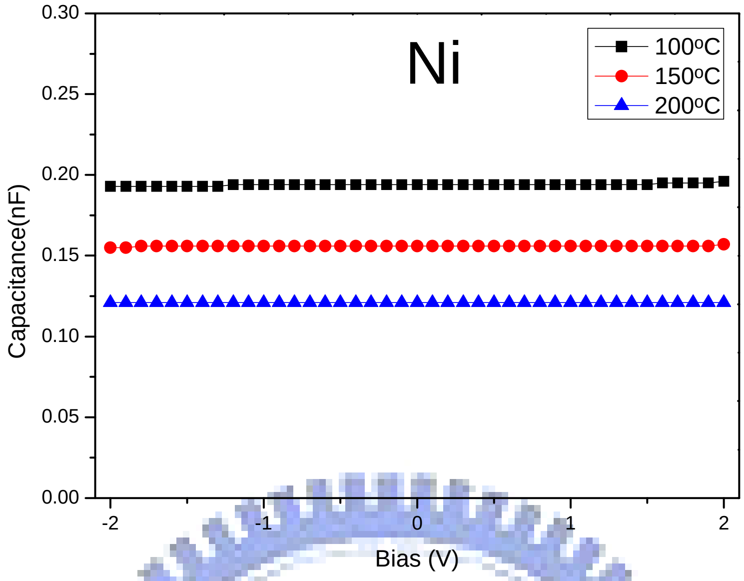
Figure 3-1 The (a)C-V and (b)I-V characteristic of MIM structure with different APPT flow rates



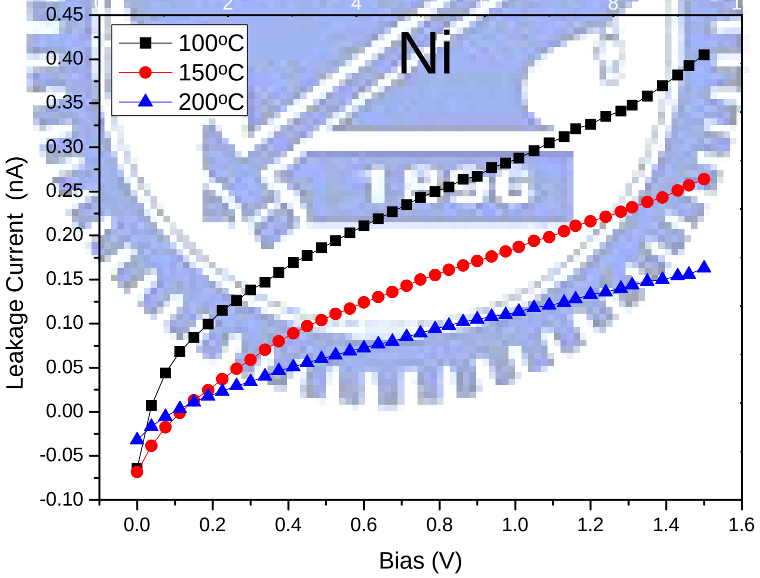
(a)

(b)

Figure 3-2 The (a)C-V and (b)I-V characteristic of MIM structure with Al gate

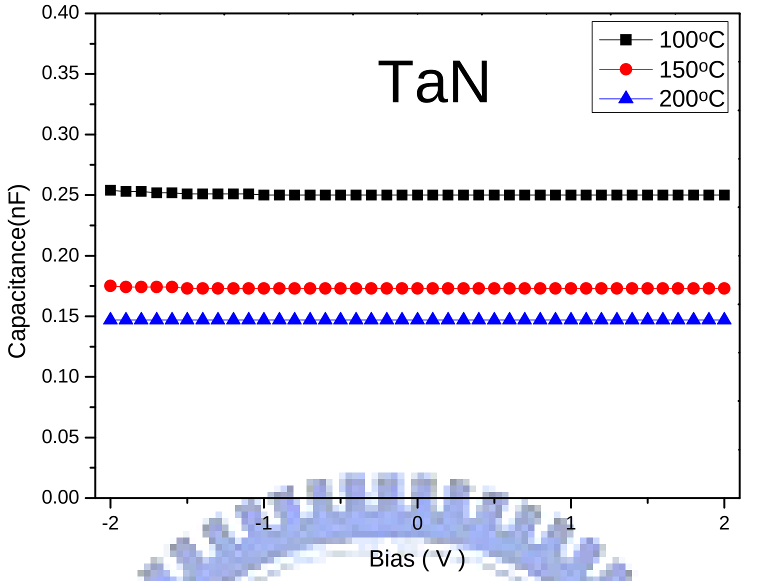


(a)

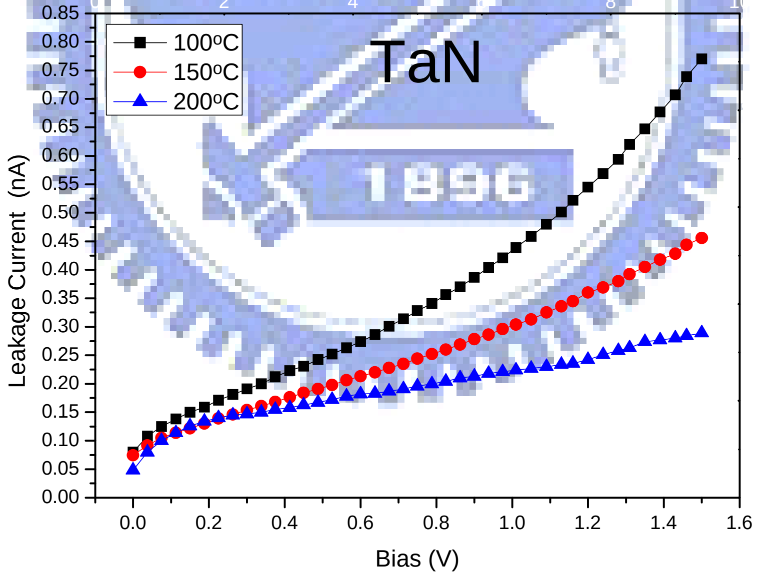


(b)

Figure 3-3 The (a)C-V and (b)I-V characteristic of MIM structure with Ni gate

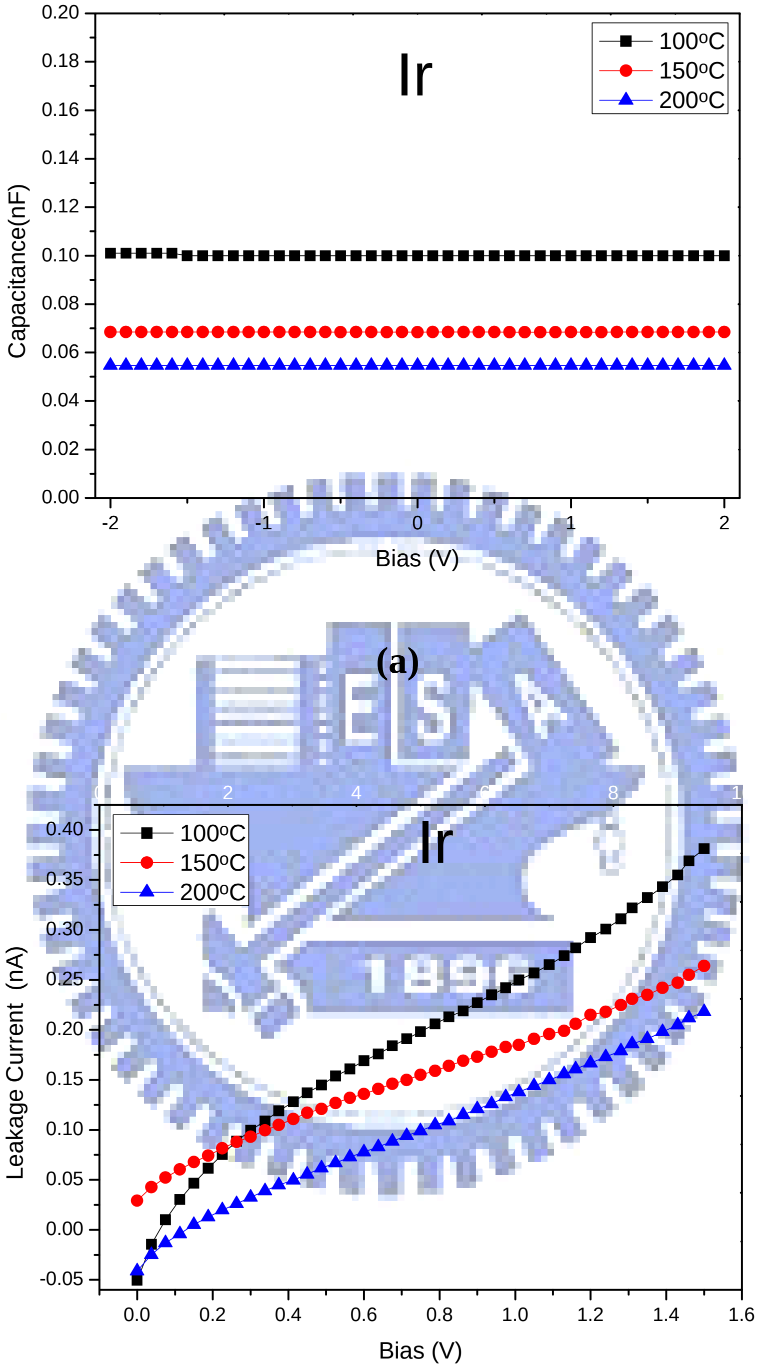


(a)



(b)

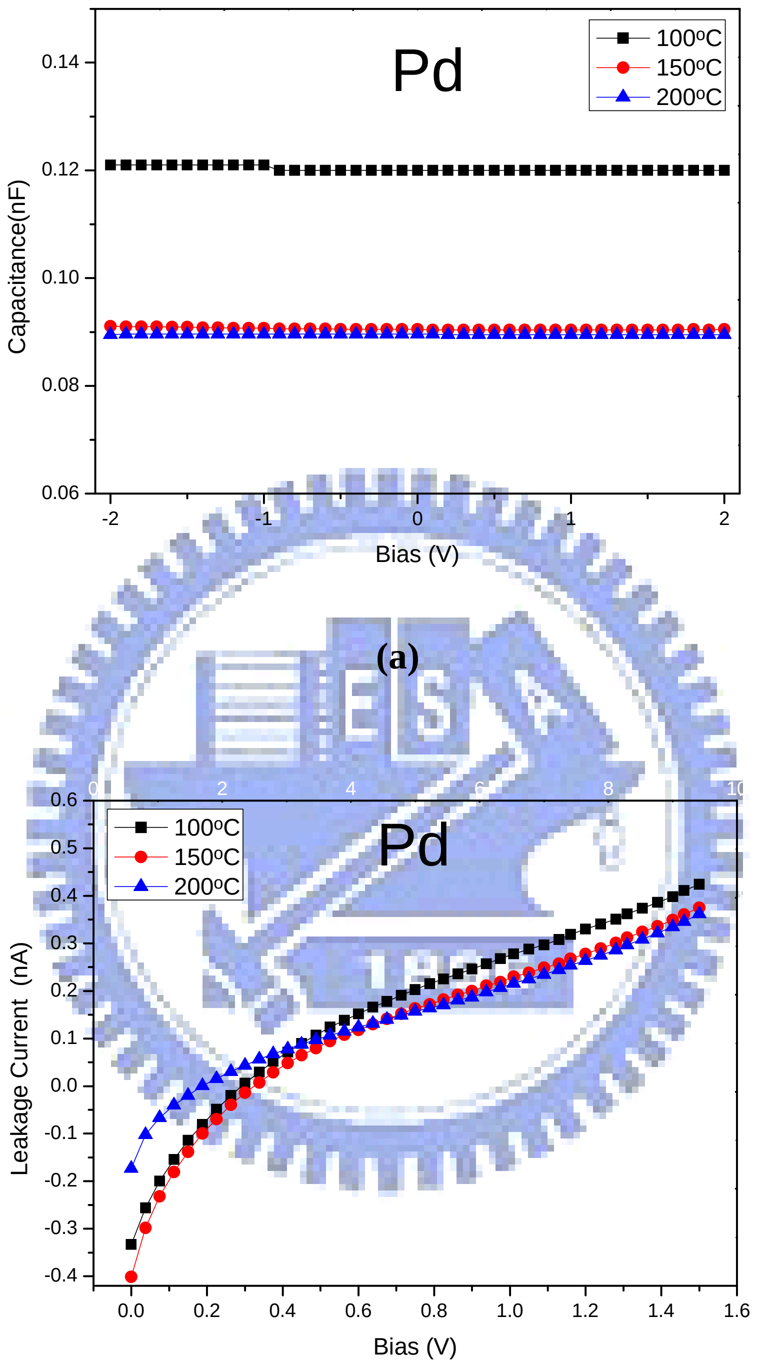
Figure 3-4 The (a)C-V and (b)I-V characteristic of MIM structure with TaN gate



(a)

(b)

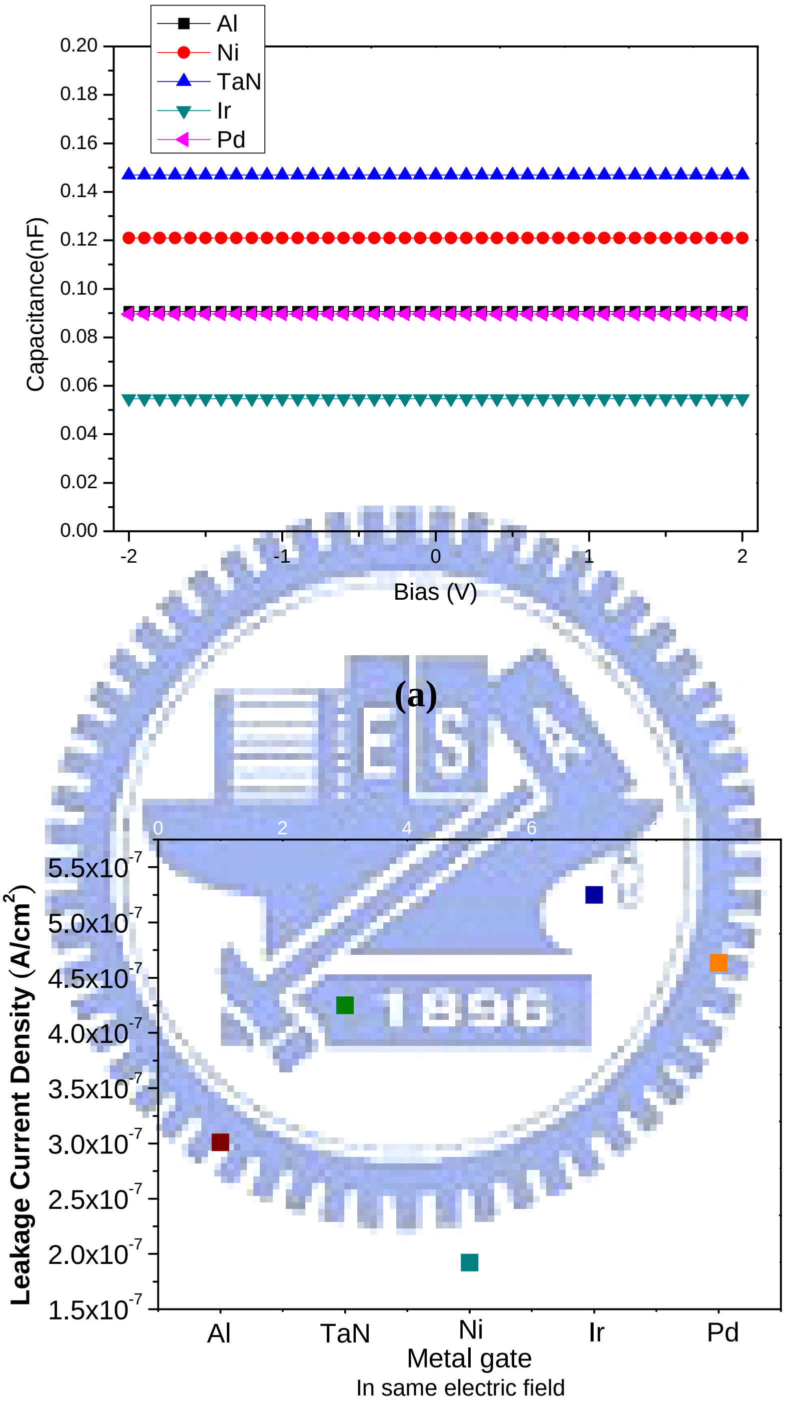
Figure 3-5 The (a)C-V and (b)I-V characteristic of MIM structure with Ir gate



(a)

(b)

Figure 3-6 The (a)C-V and (b)I-V characteristic of MIM structure with Pd gate



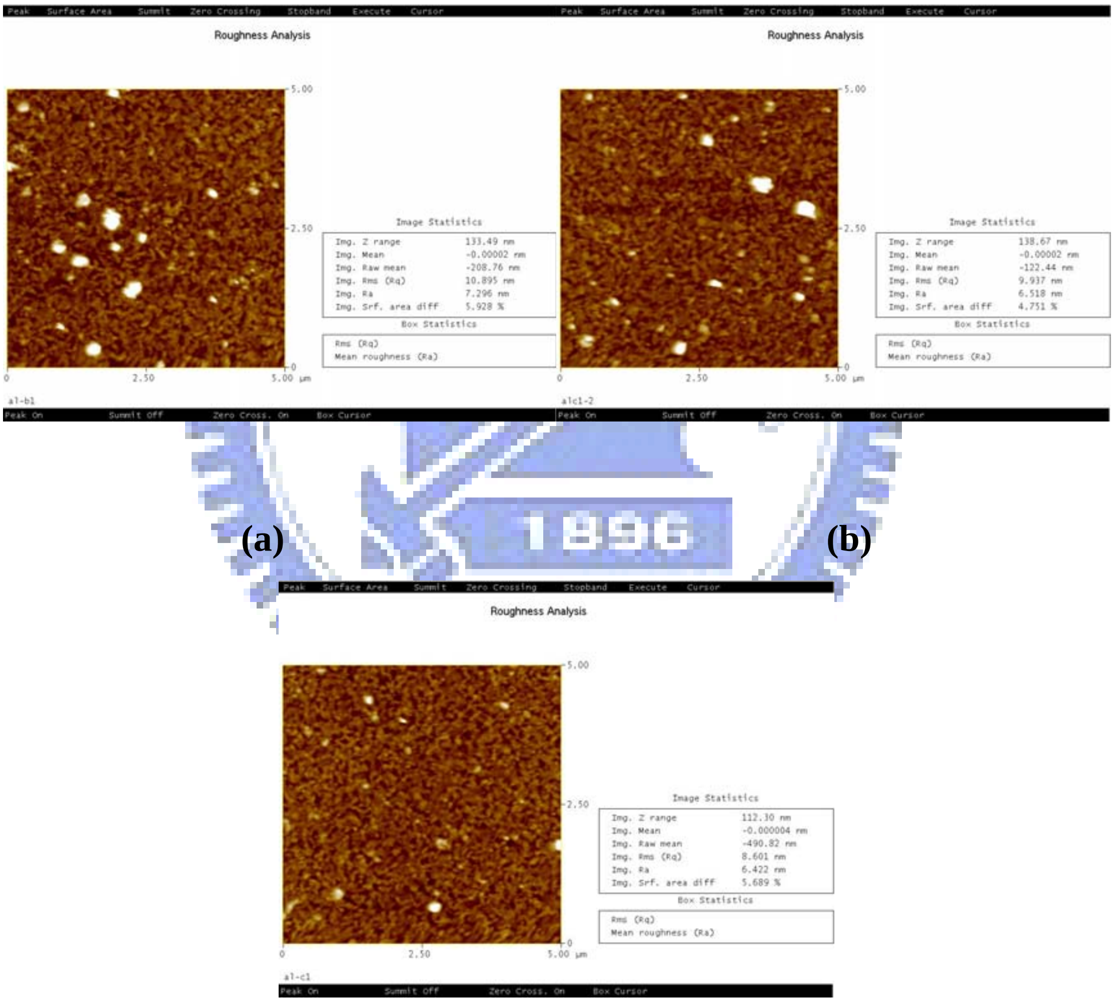
(a)

(b)

Figure 3-7 The (a)C-V and (b)I-E characteristic of MIM structure with different metal gates at 200℃

Table 3-1: The surface roughness of different conditions

溫度 金屬	100℃	150℃	200℃
Al	10.895 nm	9.937 nm	8.601 nm
Ni	11.695 nm	3.778 nm	1.950 nm
TaN	6.421 nm	3.882 nm	2.090 nm
Ir	18.422 nm	4.134 nm	3.013 nm
Pd	3.093 nm	2.075 nm	2.467 nm



(a)

```
Image Statistics
Img. Z range              133.49 nm
Img. Mean                 -0.00002 nm
Img. Raw mean             -208.76 nm
Img. Rms (Rq)             10.895 nm
Img. Ra                   7.296 nm
Img. Srf. area diff       5.928 %
Box Statistics
Rms (Rq)
Mean roughness (Ra)
```

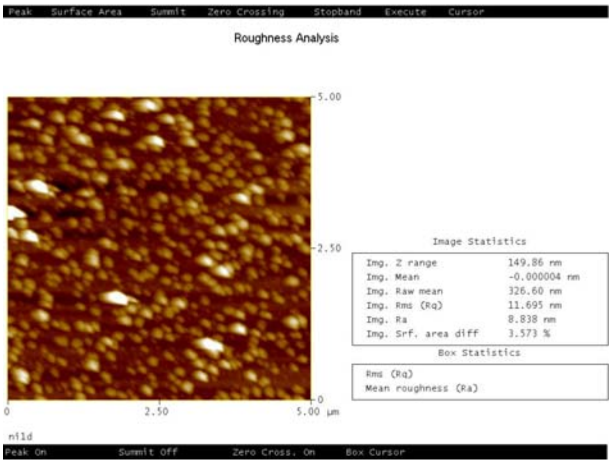
(b)

```
Image Statistics
Img. Z range              138.67 nm
Img. Mean                 -0.00002 nm
Img. Raw mean             -122.44 nm
Img. Rms (Rq)             9.937 nm
Img. Ra                   6.518 nm
Img. Srf. area diff       4.751 %
Box Statistics
Rms (Rq)
Mean roughness (Ra)
```

(c)

```
Image Statistics
Img. Z range              112.30 nm
Img. Mean                 -0.000004 nm
Img. Raw mean             -490.82 nm
Img. Rms (Rq)             8.601 nm
Img. Ra                   6.422 nm
Img. Srf. area diff       5.689 %
Box Statistics
Rms (Rq)
Mean roughness (Ra)
```

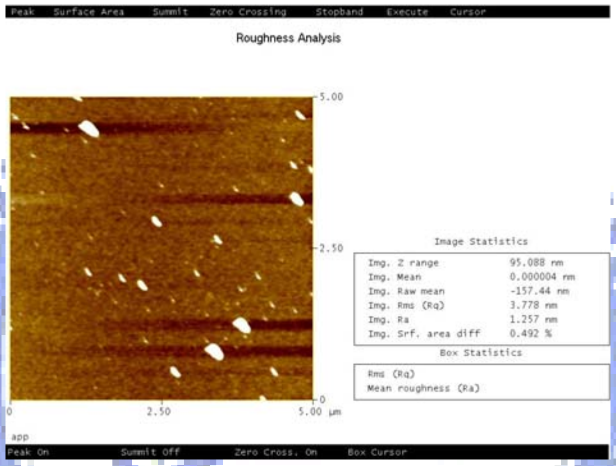
Figure 3-8 The surface roughness of APPT SiO_2 on Al gate at (a)100, (b)150, (c)200 substrate temperature



```
Img. Z range           149.86 nm
Img. Mean              -0.000004 nm
Img. Raw mean          326.60 nm
Img. Rms (Rq)          11.695 nm
Img. Ra                8.838 nm
Img. Srf. area diff    3.573 %
```

```
Rms (Rq)
Mean roughness (Ra)
```

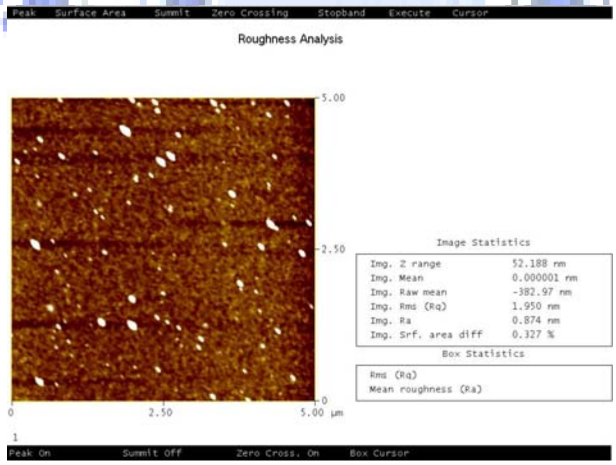
(a)



```
Img. Z range           95.088 nm
Img. Mean              0.000004 nm
Img. Raw mean          -157.44 nm
Img. Rms (Rq)          3.778 nm
Img. Ra                1.257 nm
Img. Srf. area diff    0.492 %
```

```
Rms (Rq)
Mean roughness (Ra)
```

(b)

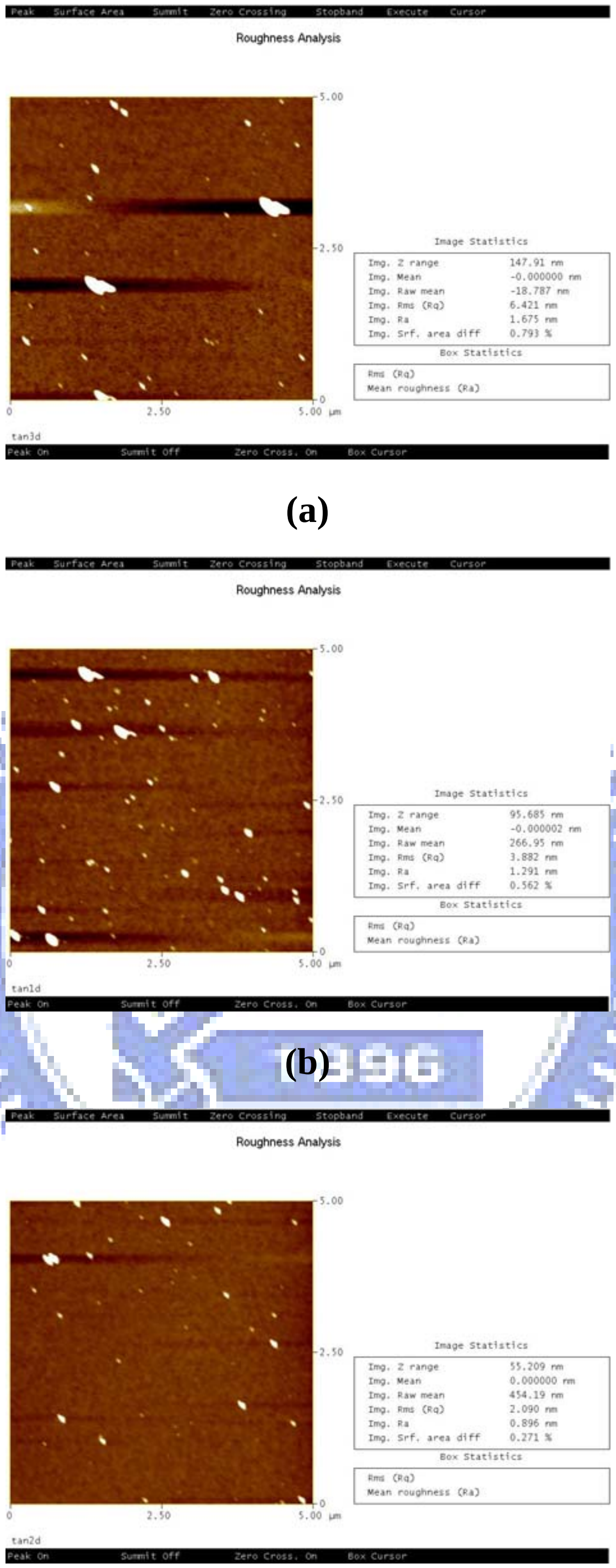


```
Img. Z range           52.188 nm
Img. Mean              0.000001 nm
Img. Raw mean          -382.97 nm
Img. Rms (Rq)          1.950 nm
Img. Ra                0.874 nm
Img. Srf. area diff    0.327 %
```

```
Rms (Rq)
Mean roughness (Ra)
```

(c)

Figure 3-9 The surface roughness of APPT SiO_2 on Ni gate at (a)100, (b)150, (c)200 substrate temperature



```
Image Statistics
Img. Z range            147.91 nm
Img. Mean               -0.000000 nm
Img. Raw mean           -18.787 nm
Img. Rms (Rq)           6.421 nm
Img. Ra                 1.675 nm
Img. Srf. area diff     0.793 %
Box Statistics
Rms (Rq)
Mean roughness (Ra)
```

(a)

```
Image Statistics
Img. Z range            95.685 nm
Img. Mean               -0.000002 nm
Img. Raw mean           266.95 nm
Img. Rms (Rq)           3.882 nm
Img. Ra                 1.291 nm
Img. Srf. area diff     0.562 %
Box Statistics
Rms (Rq)
Mean roughness (Ra)
```

(b)

```
Image Statistics
Img. Z range            55.209 nm
Img. Mean               0.000000 nm
Img. Raw mean           454.19 nm
Img. Rms (Rq)           2.090 nm
Img. Ra                 0.896 nm
Img. Srf. area diff     0.271 %
Box Statistics
Rms (Rq)
Mean roughness (Ra)
```

(c)

Figure 3-10 The surface roughness of APPT SiO_2 on TaN gate at (a)100, (b)150, (c)200 substrate temperature

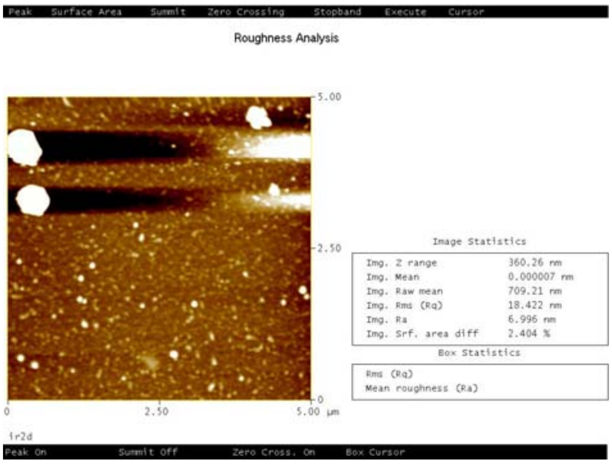


Image Statistics

Img. Z range	360.26 nm
Img. Mean	0.000007 nm
Img. Raw mean	709.21 nm
Img. Rms (Rq)	18.422 nm
Img. Ra	6.996 nm
Img. Srf. area diff	2.404 %

Box Statistics

Rms (Rq)
Mean roughness (Ra)

(a)

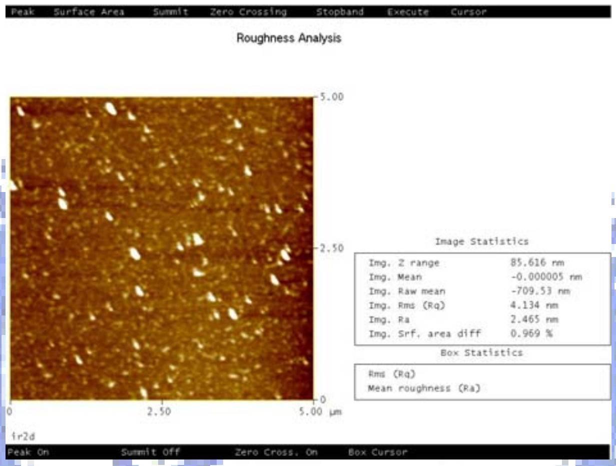


Image Statistics

Img. Z range	85.616 nm
Img. Mean	-0.000005 nm
Img. Raw mean	-709.53 nm
Img. Rms (Rq)	4.134 nm
Img. Ra	2.465 nm
Img. Srf. area diff	0.969 %

Box Statistics

Rms (Rq)
Mean roughness (Ra)

(b)

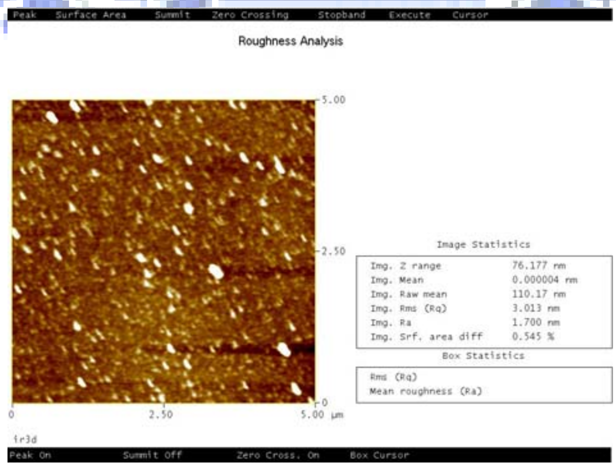


Image Statistics

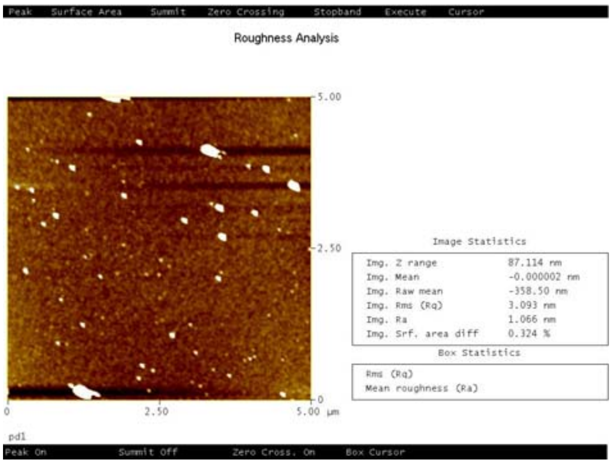
Img. Z range	76.177 nm
Img. Mean	0.000004 nm
Img. Raw mean	110.17 nm
Img. Rms (Rq)	3.013 nm
Img. Ra	1.700 nm
Img. Srf. area diff	0.545 %

Box Statistics

Rms (Rq)
Mean roughness (Ra)

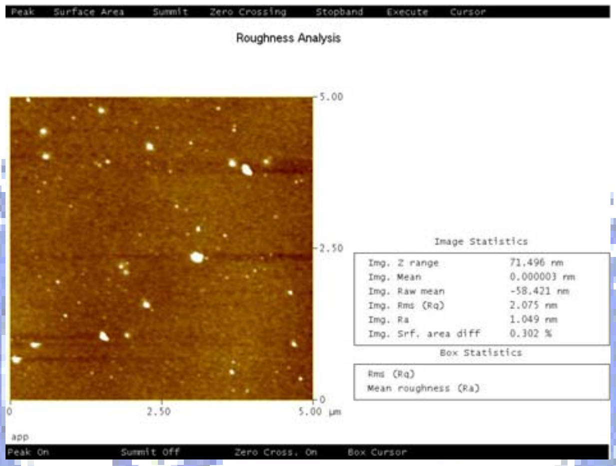
(c)

Figure 3-11 The surface roughness of APPT SiO_2 on Ir gate at (a)100, (b)150, (c)200 substrate temperature



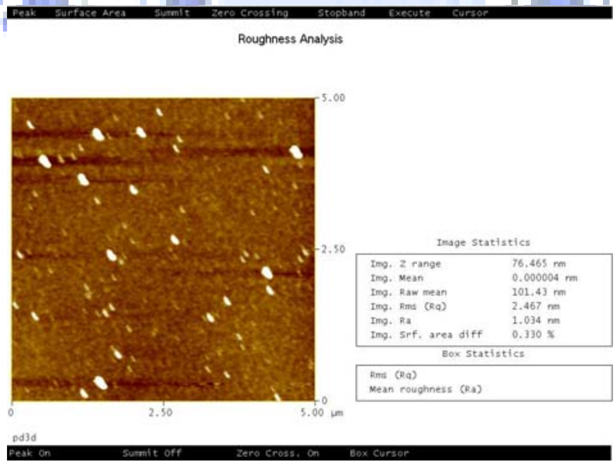
```
Image Statistics
Img. Z range            87.114 nm
Img. Mean               -0.000002 nm
Img. Raw mean           -358.50 nm
Img. Rms (Rq)           3.093 nm
Img. Ra                 1.066 nm
Img. Srf. area diff     0.324 %
Box Statistics
Rms (Rq)
Mean roughness (Ra)
```

(a)



```
Image Statistics
Img. Z range            71.496 nm
Img. Mean               0.000003 nm
Img. Raw mean           -58.421 nm
Img. Rms (Rq)           2.075 nm
Img. Ra                 1.049 nm
Img. Srf. area diff     0.302 %
Box Statistics
Rms (Rq)
Mean roughness (Ra)
```

(b)



```
Image Statistics
Img. Z range            76.465 nm
Img. Mean               0.000004 nm
Img. Raw mean           101.43 nm
Img. Rms (Rq)           2.467 nm
Img. Ra                 1.034 nm
Img. Srf. area diff     0.330 %
Box Statistics
Rms (Rq)
Mean roughness (Ra)
```

(c)

Figure 3-12 The surface roughness of APPT SiO_2 on Pd gate at (a)100, (b)150, (c)200 substrate temperature

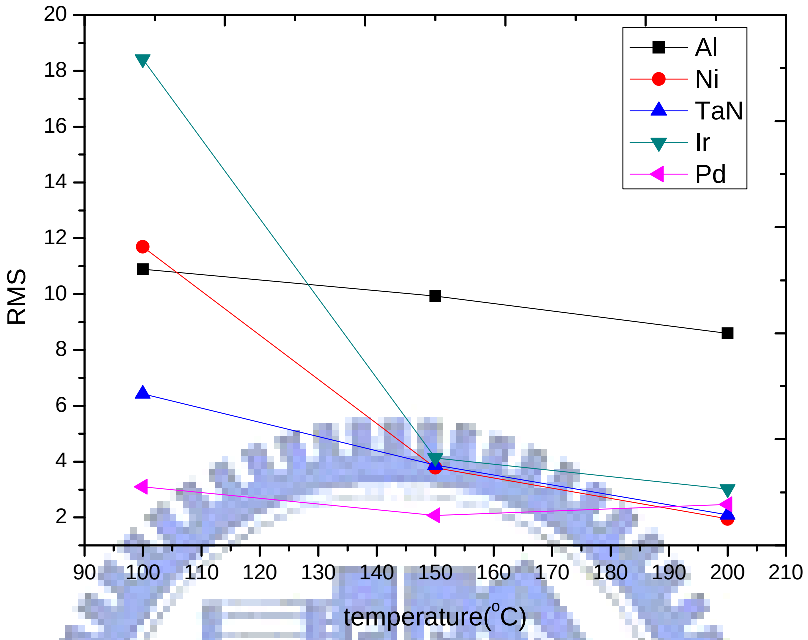
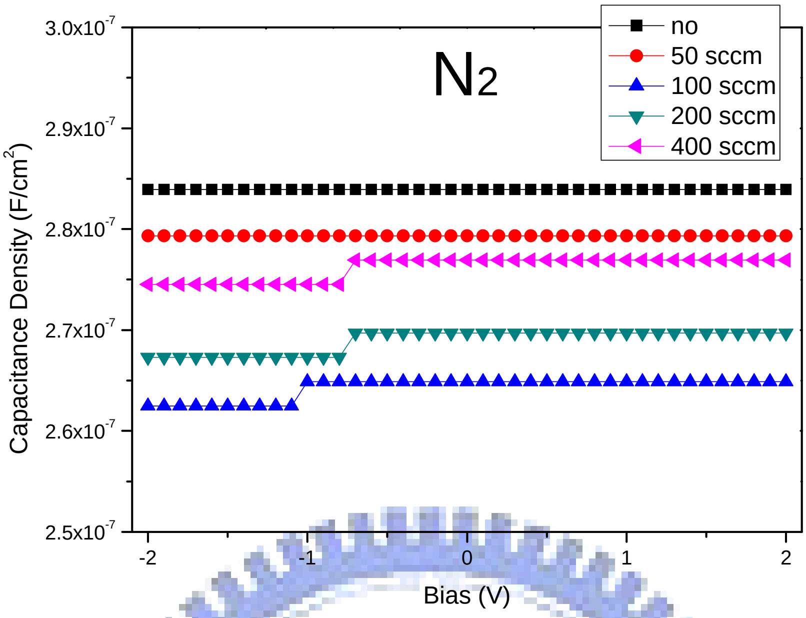
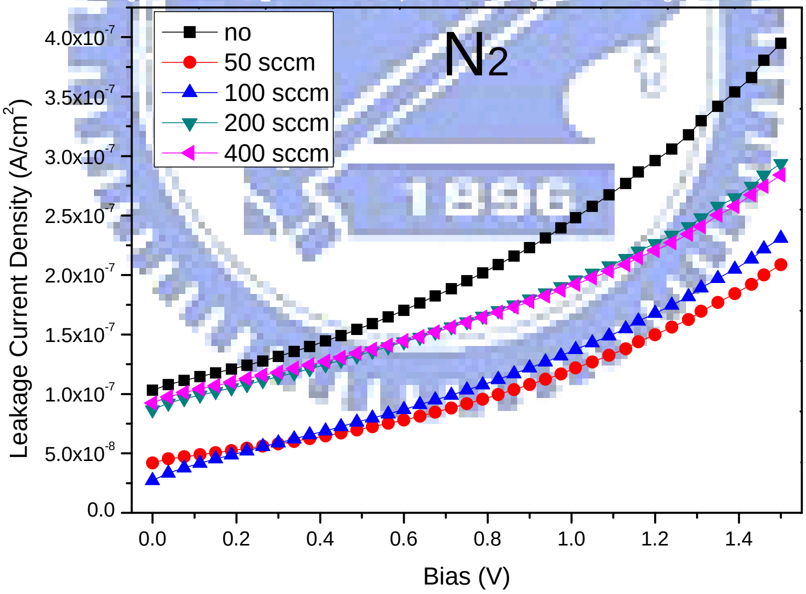


Figure 3-13 The trend of surface roughness of different conditions

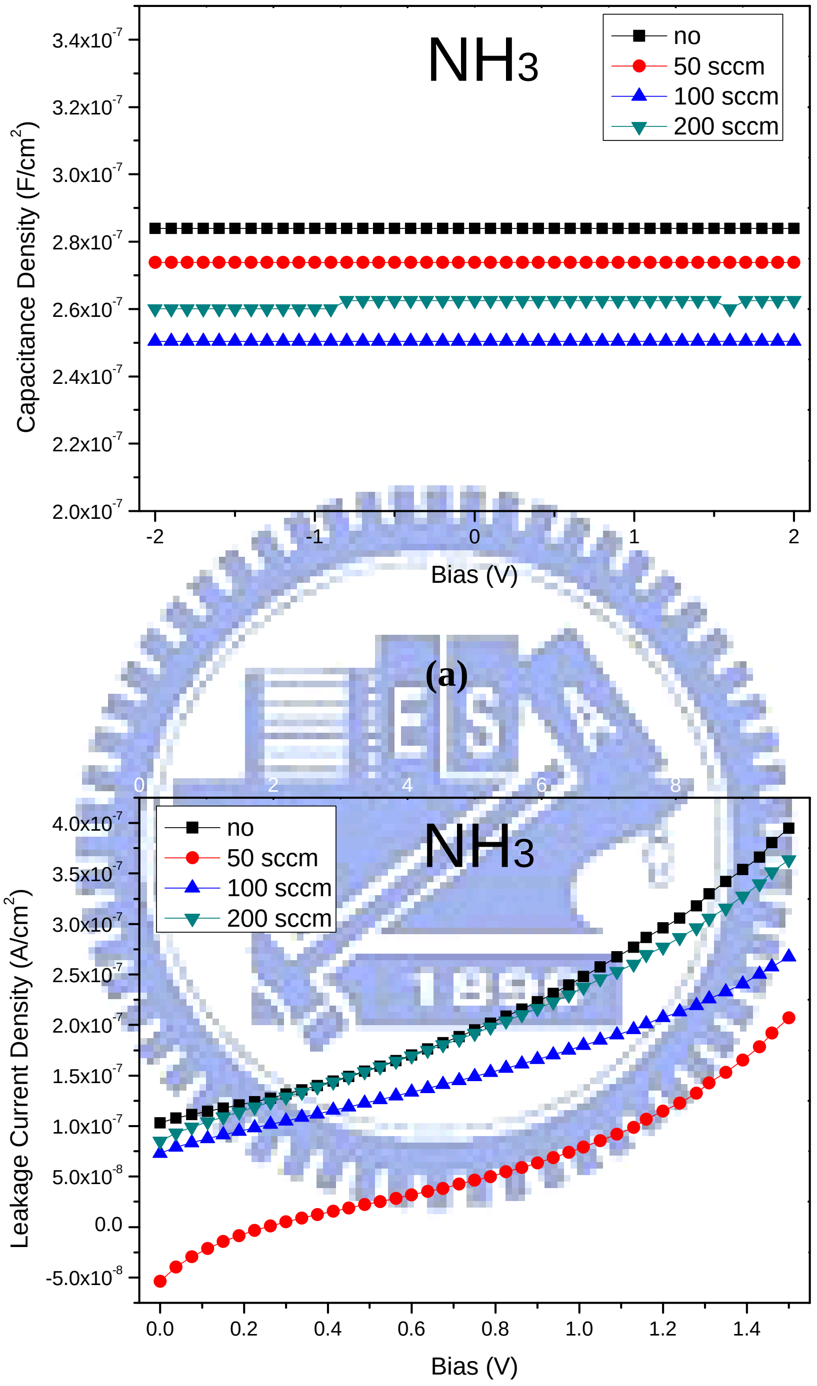


(a)



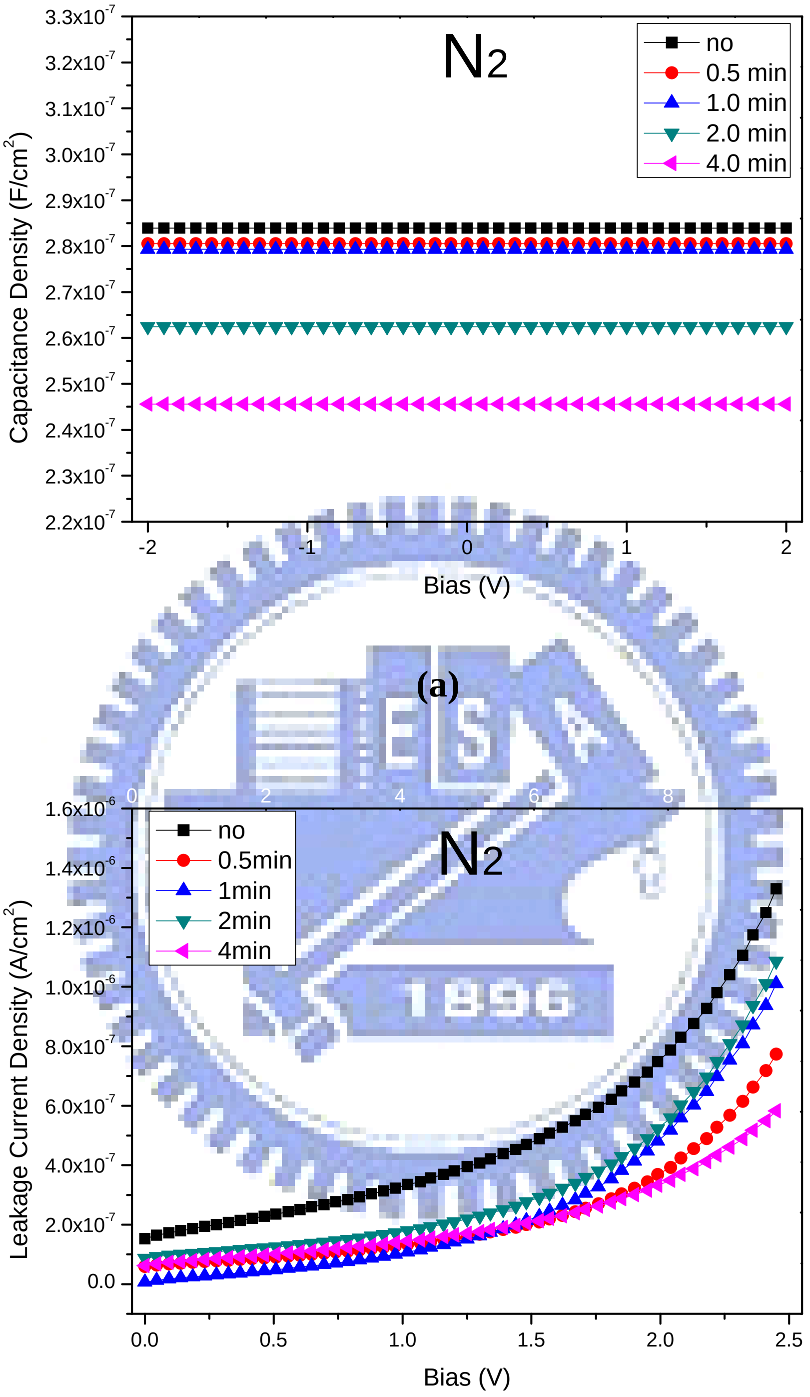
(b)

Figure 3-14 The (a)C-V and (b)I-V characteristic of MIM structure by N_2 plasma treatment with different flow rates



(b)

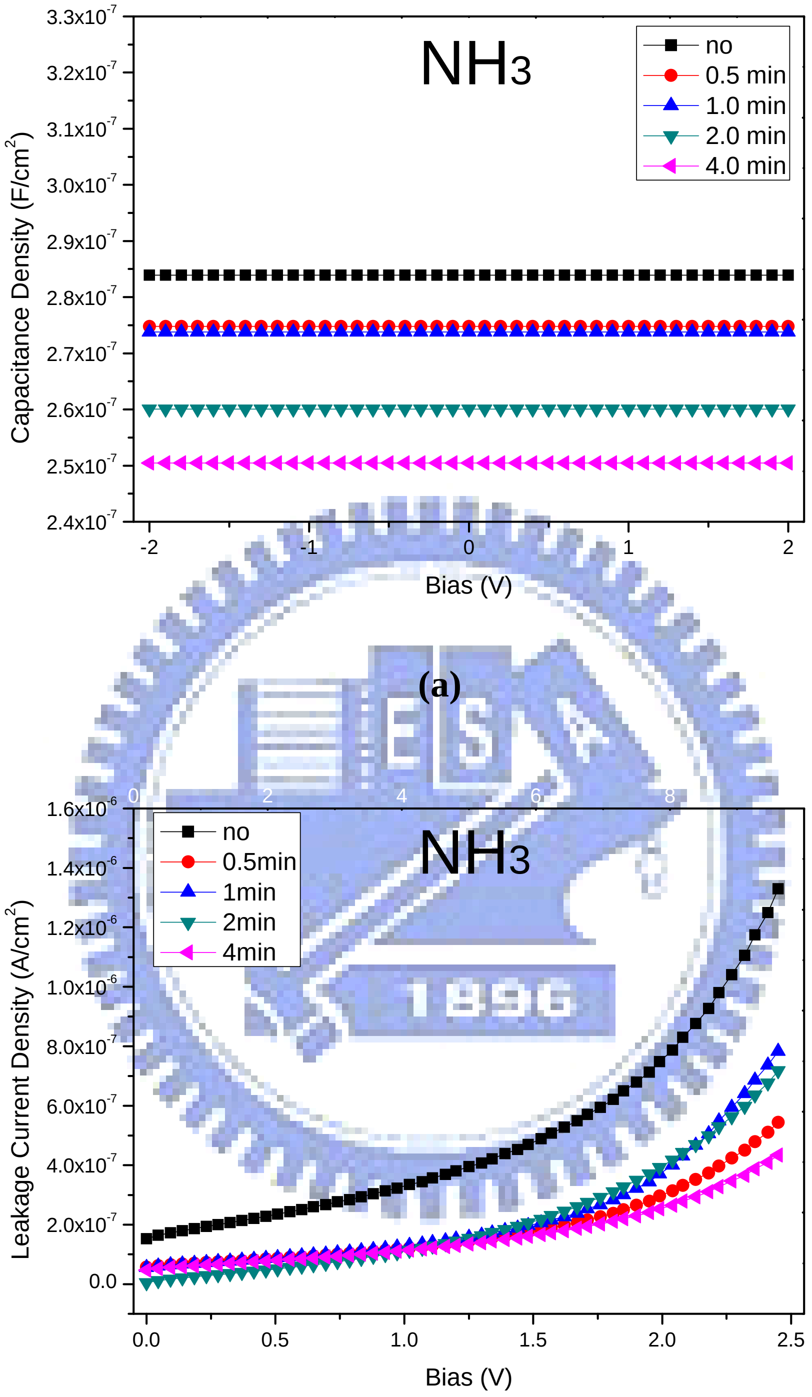
Figure 3-15 The (a)C-V and (b)I-V characteristic of MIM structure by NH_3 plasma treatment with different flow rates



(a)

(b)

Figure 3-16 The (a)C-V and (b)I-V characteristic of MIM structure by N_2 plasma treatment with different time



(a)

(b)

Figure 3-17 The (a)C-V and (b)I-V characteristic of MIM structure by NH_3 plasma treatment with different time

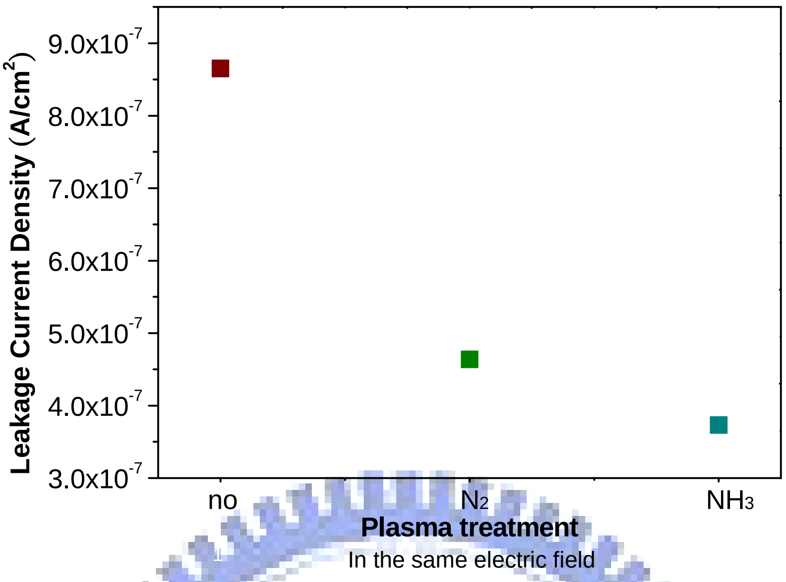


Figure 3-18 The I-E characteristic of MIM structure with different plasma treatment

Table 3-2: The surface roughness, contact angle and the film thickness of different conditions

Plasma treatment	no	N$_2$	NH$_3$
RMS	1.246 nm	1.190 nm	1.089 nm
Contact Angle	24.80°	20.70°	20.70°
Thickness	12.2 nm	12.6 nm	12.5 nm

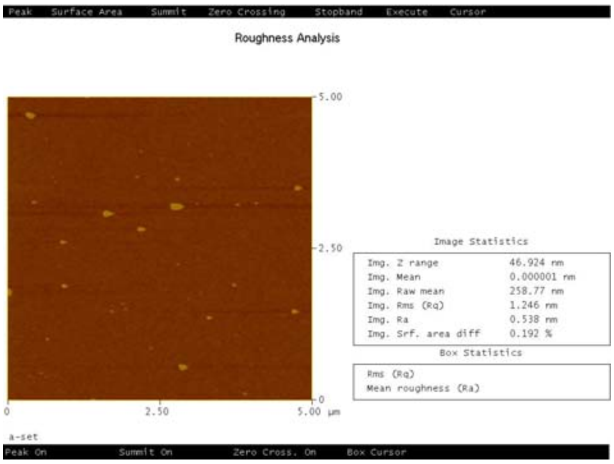


Image Statistics

Img. Z range 46.924 nm
Img. Mean 0.000001 nm
Img. Raw mean 258.77 nm
Img. Rms (Rq) 1.246 nm
Img. Ra 0.538 nm
Img. Srf. area diff 0.192 %

Box Statistics

Rms (Rq)
Mean roughness (Ra)

(a)

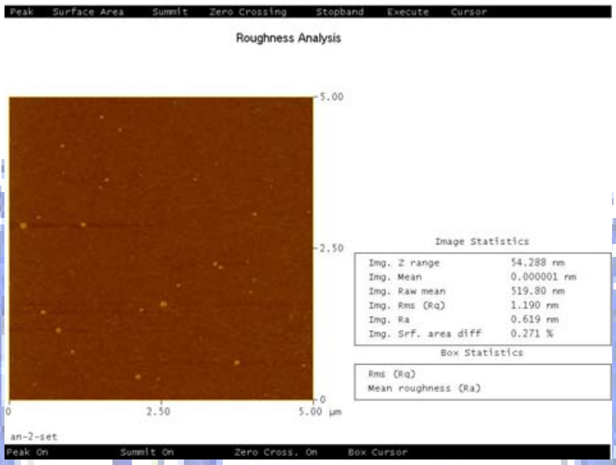


Image Statistics

Img. Z range 54.288 nm
Img. Mean 0.000001 nm
Img. Raw mean 519.80 nm
Img. Rms (Rq) 1.190 nm
Img. Ra 0.619 nm
Img. Srf. area diff 0.271 %

Box Statistics

Rms (Rq)
Mean roughness (Ra)

(b)

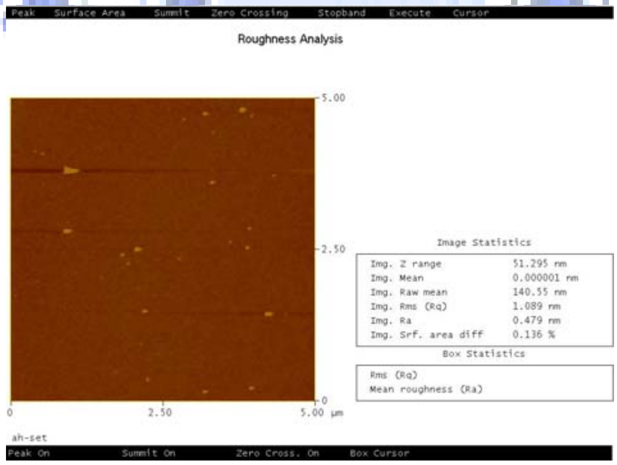


Image Statistics

Img. Z range 51.295 nm
Img. Mean 0.000001 nm
Img. Raw mean 140.55 nm
Img. Rms (Rq) 1.089 nm
Img. Ra 0.479 nm
Img. Srf. area diff 0.136 %

Box Statistics

Rms (Rq)
Mean roughness (Ra)

(c)

Figure 3-19 The roughness of (a)no, (b)N_2, (c)NH_3 plasma treatment

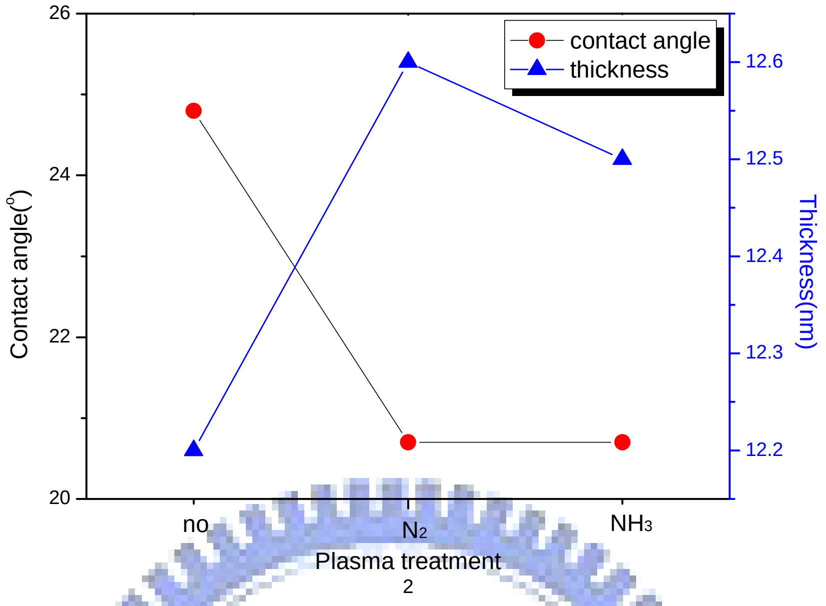


Figure 3-20 The film thickness and the contact angle of different plasma treatments

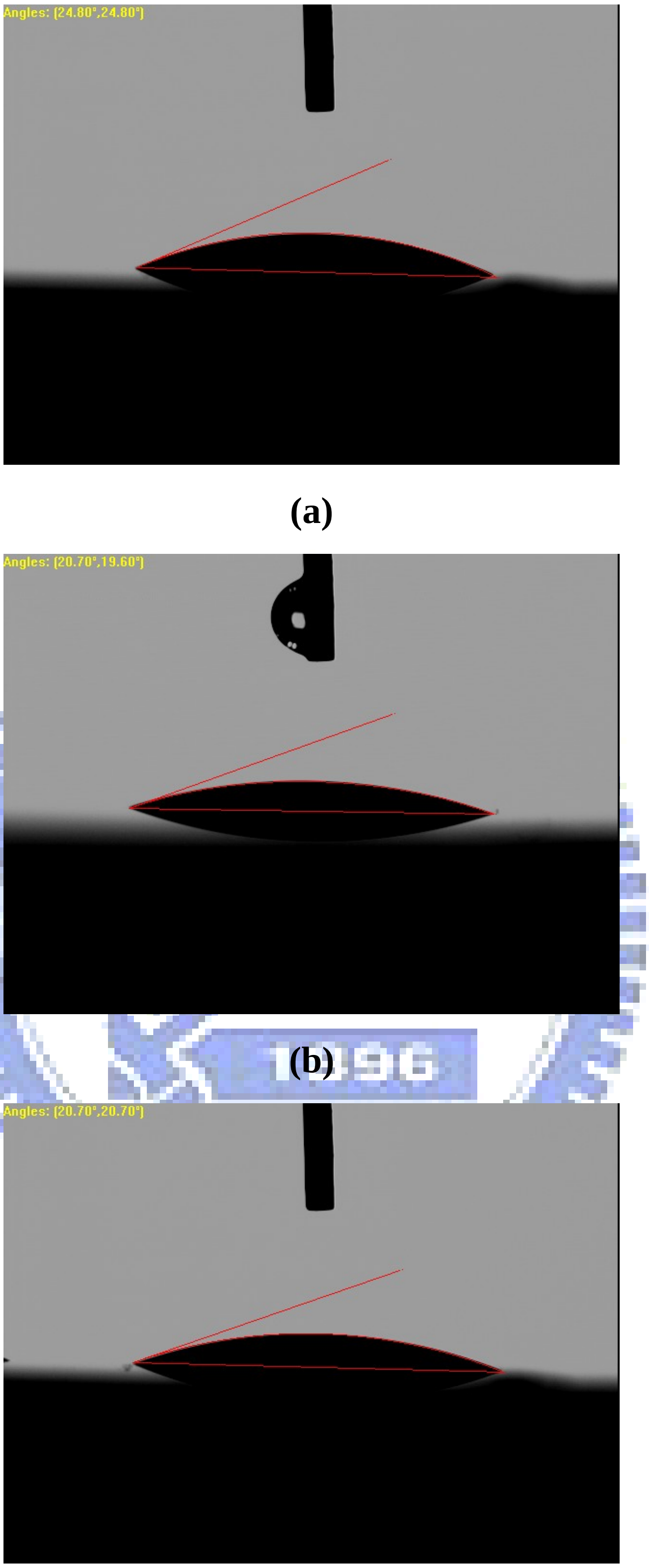
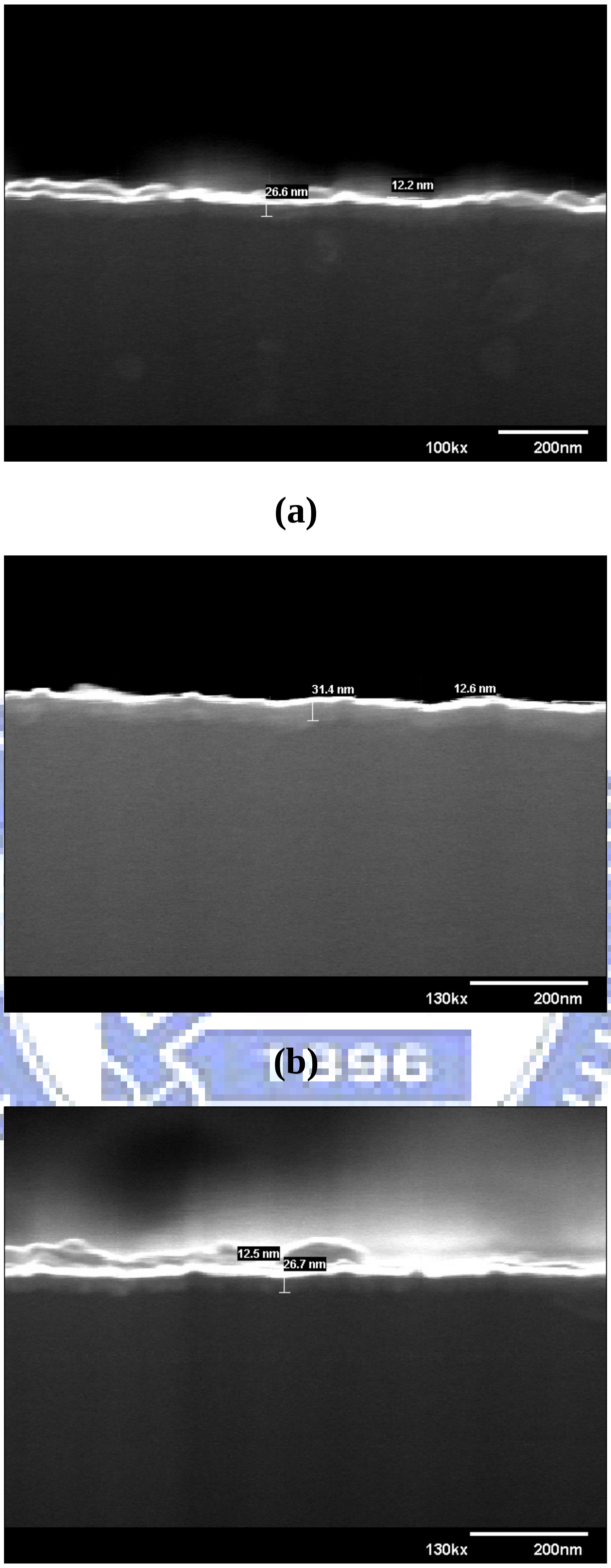


Figure 3-21 The contact angel of (a)no, (b)N_2, (c)NH_3 plasma treatment



(a)

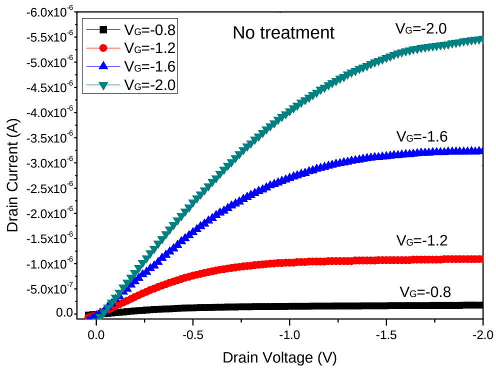
(b)

(c)

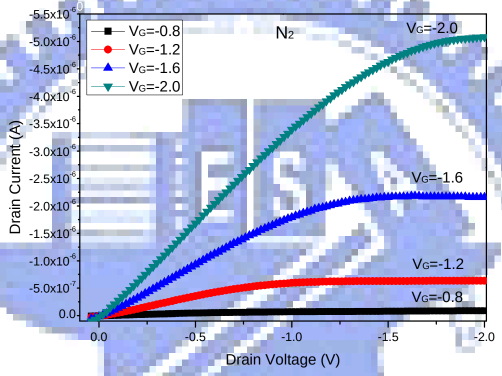
Figure 3-22 The film thickness of (a)no, (b)N_2, (c)NH_3 plasma treatment

Table 3-3 The s threshold voltage, mobility and on/off ratio of different conditions

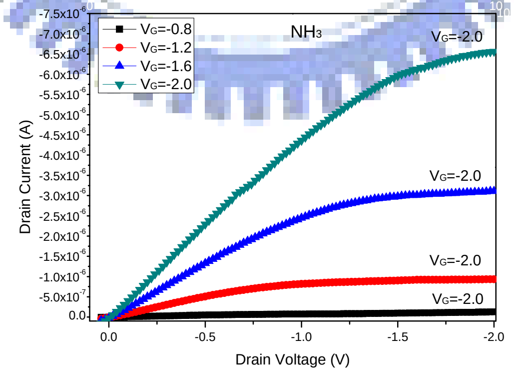
Plasma treatment	threshold voltage(Volt)	Mobility(cm^2/V·s)	on/off ratio
no	-0.616 V	0.56 cm^2/V·s	0.81×10^3
N_2	-0.953 V	0.59 cm^2/V·s	0.47×10^3
NH_3	-0.886 V	0.72 cm^2/V·s	0.41×10^3



(a)

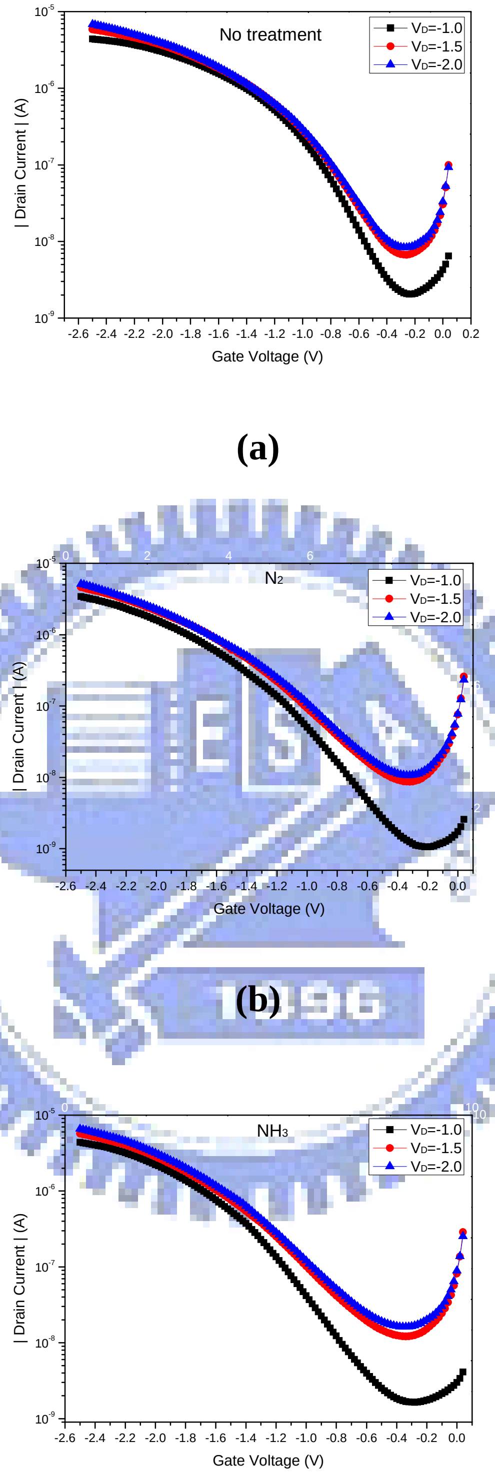


(b)



(c)

Figure 3-23 I_D-V_D for different plasmas treatments (a) no treatment (b) N_2 treatment (c) NH_3 treatment

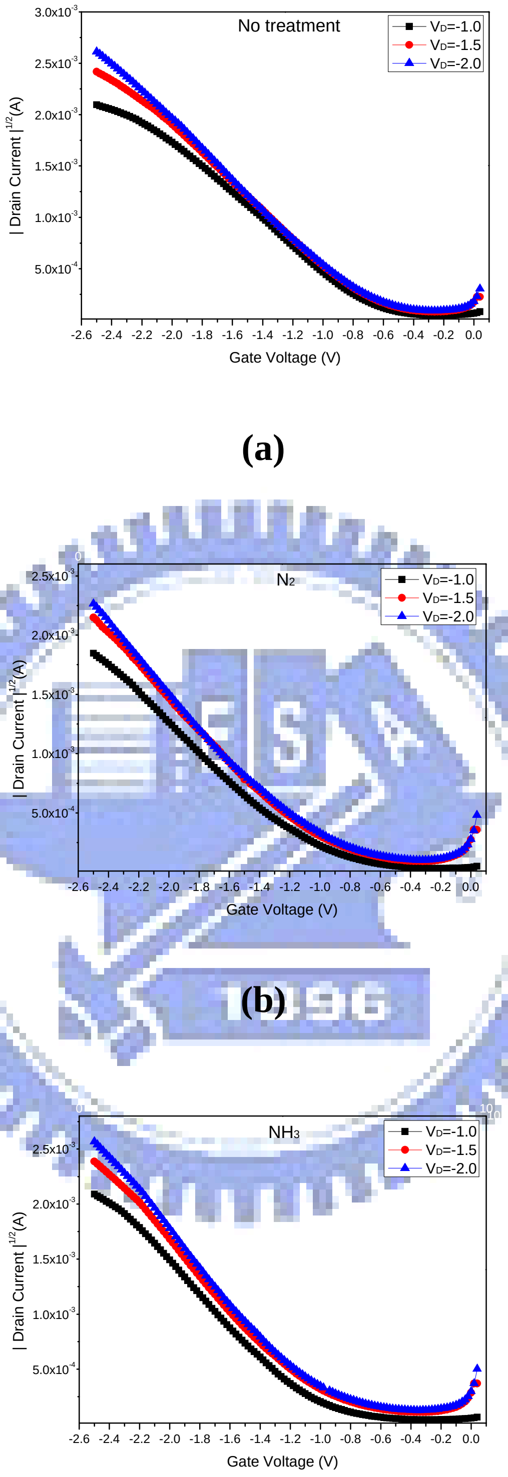


(a)

(b)

(c)

Figure 3-24 I_D-V_G for different plasmas treatments (a) no treatment (b) N_2 treatment (c) NH_3 treatment



(a)

(b)

(c)

Figure 3-25 $|I_D|^{1/2}$-V_G for different plasmas treatments (a) no treatment (b) N_2 treatment (c) NH_3 treatment

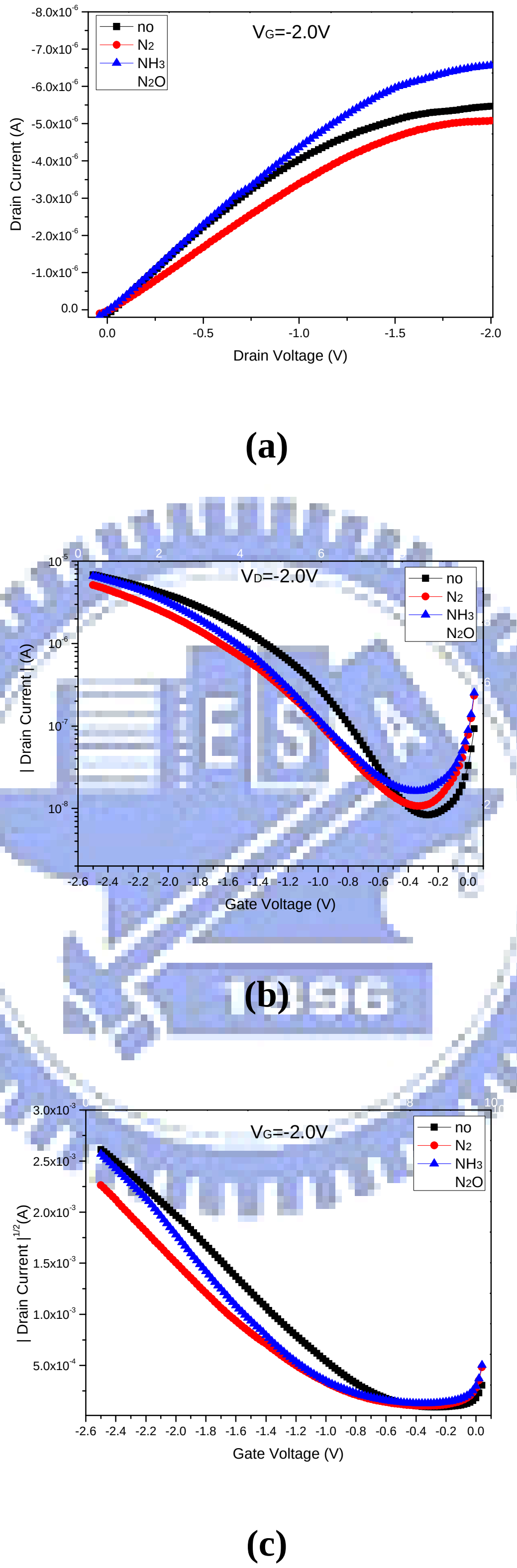


Figure 3-26 The comparison of (a) I_D-V_D (b) I_D-V_G (c) $|I_D|^{1/2}$-V_G with different treatments

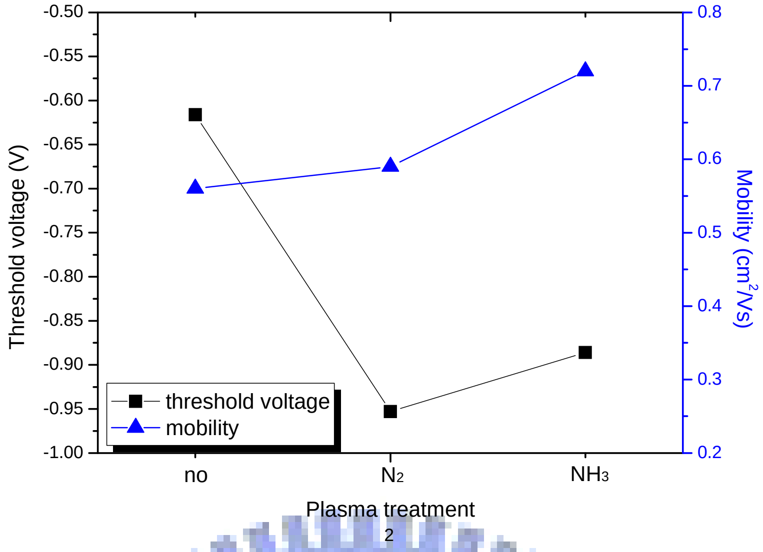


Figure 3-27 The s threshold voltage, mobility and on/off ratio of different conditions

Chapter 4

Conclusions and Future work

4.1 Conclusions

We can know from the experiment the flow of carrier gases will influence the quantity that the TEOS gas comes out. The increasing of the flow rate about carrier gases leads to the increasing of released TEOS gas. But depositing is too quickly to make good quality of insulator.

And we can learn from the experiment the nickel is most suitable for using APPT to deposit the oxidize layer.

After plasma treatment, the insulator surface characteristic is caused to have exiguity changes. For example, there are the change of the surface roughness and contact angle. And the plasma treatment has the effect to reduce leakage current.

In summary, OTFT using pentacene as an active layer are fabricated on insulator deposited by APPT. The mobility in the saturation region and the threshold voltage and on/off ratio of the OTFT are 0.72 cm^2/Vs and -0.616 V and $\sim 10^3$, respectively. The advantage of the atmospheric-pressure plasma technology is that it needn't vacuum and at general room temperature to deposit insulator. This advantage is an asset condition to fabricate OTFT.

4.2 Future work

The new method, for example, use plastics substrate as the base, so that it's more suitable for OTFT which is flexibility and lightness.

Spinning organic polymeric gate dielectrics on oxide which is deposited by APPT achieve the result of reducing roughness. Simultaneously, we can improve the hydrophilic and hydrophobic question for organic semiconductor by organic polymeric gate dielectrics.

Because pentacene OTFT is sensitive to ambient conditions. Protection from the environment by encapsulation is critical to the stability of pentacene OTFT. Therefore, using a suitable material as passivation to protect pentacene film from environmental effect is another important topic.

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國立中興大學物理學系

（民國 91 年 09 月～民國 95 年 06 月）

國立交通大學電子工程研究所碩士班

（民國 95 年 09 月～民國 97 年 07 月）

碩士論文：常壓式電漿系統沉積之二氧化矽在有機薄膜電晶體應上之研究

The study on the silicon dioxide deposited by Atmospheric-Pressure Plasma Technology for Organic Thin-Film Transistor application